

ELEKTOR
ELECTRONICS

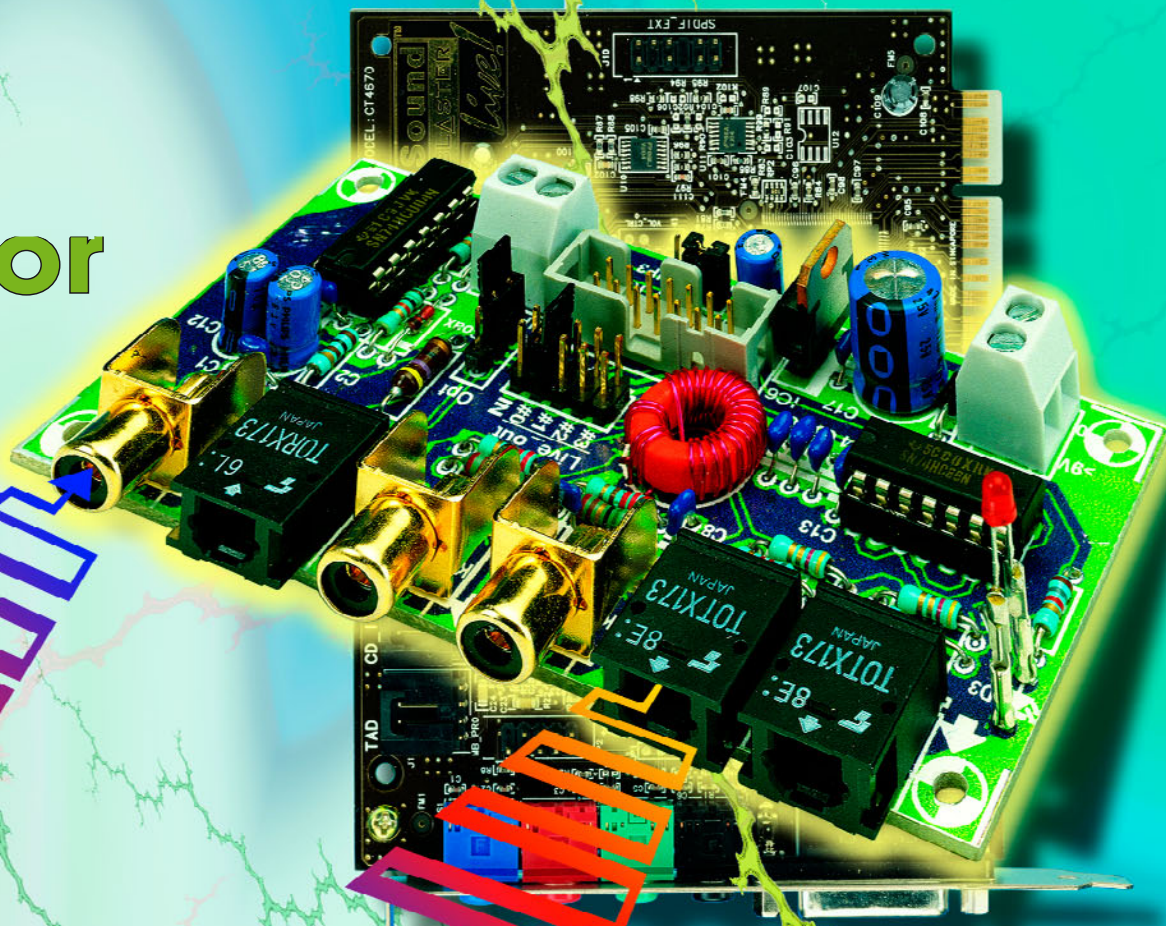
PC TOPICS:

- universal measurement interface •
- CPU thermometer •
- removable hard disk •

BUMPER CHRISTMAS ISSUE
extra: 35+ small projects

digital inputs/outputs
for Soundblaster Live Value

mains
adaptor
switch



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Into the new Millennium with Elektor Electronics!

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flashing Christmas star

a lively Christmas decoration

The Christmas star described in this article is a far cry from the shoddy and unadventurous gadgets that light and flash around us at Christmas time. A separate control board supplies 128 different patterns for a Christmas star. By arranging the LEDs in different positions on the display board, other eye catchers and ornaments may be created, say, a flashing Easter egg.

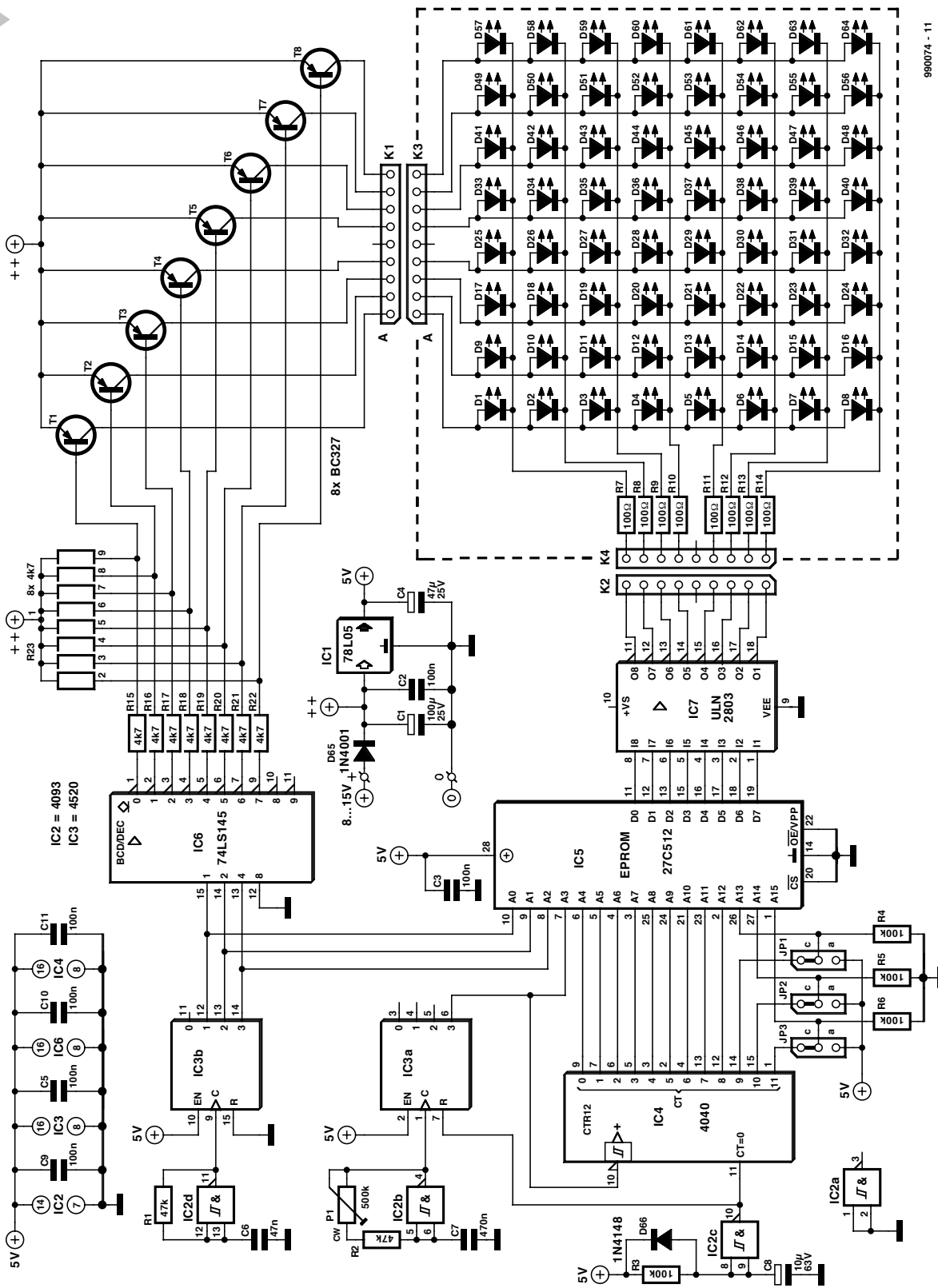


The star-shaped display board contains 64 LEDs and is driven by a plug-on control board. The latter contains an EPROM type 27C512 as the memory device, offering storage space for more than 8,000 patterns. The EPROM data outputs drive the LED cathodes via ULN2803 buffers. The cathodes may be said to represent the rows of the 8×8 LED matrix shown in **Figure 1**. Column control is assigned to a binary counter (IC3b), which is clocked by an oscillator (IC2d, R1 and C6) at a rate of about 500 Hz. After binary-to-decimal conversion by IC6, a 74LS145, discrete transistor type BC327 act as the eight

column drivers. The three least-significant address inputs of the EPROM are driven by the 3-bit binary counter.

A second oscillator (IC2b, C7, R2+ P1) clocks a 13-bit binary counter consisting of two sections of a 4520 and a counter type 4040. The counter outputs are directly connected to EPROM address inputs A3-A15, allowing each program state to be selected sequentially and individually.

In principle, eight of these program states together act as a program which is repeated eight times. Consequently an EPROM with a storage capacity of 64 kBytes may contain 128 programs.



990074 - 11

Figure 1. The EPROM contents is 'visualised' in a cyclic manner using an 8x8 LED matrix.

The EPROM supplied by us under order code **996526-1** contains 32 different programs in the first quarter of its storage space. The second quarter contains the same programs with the LEDs lighting in the opposite direction, that is, the patterns 'move' from the outside to the centre of the star instead of the

other way around. The second half of the EPROM is similar to the first, only the programs are inverted.

There is a total of 128 programs available, each with eight repetitions and states. With a whopping 8,192 different states and a clock rate of 0.8 Hz it takes more than two hours before a

pattern is repeated.

Together with components R3, D2 and C8, gate IC2c forms a reset generator which clears the address counter to zero when the circuit is switched on.

The flashing Christmas star is powered by a mains adaptor with an output rating of 8-15VDC/1.5 A. A voltage regulator, IC1, is used to turn the unregulated input voltage into one

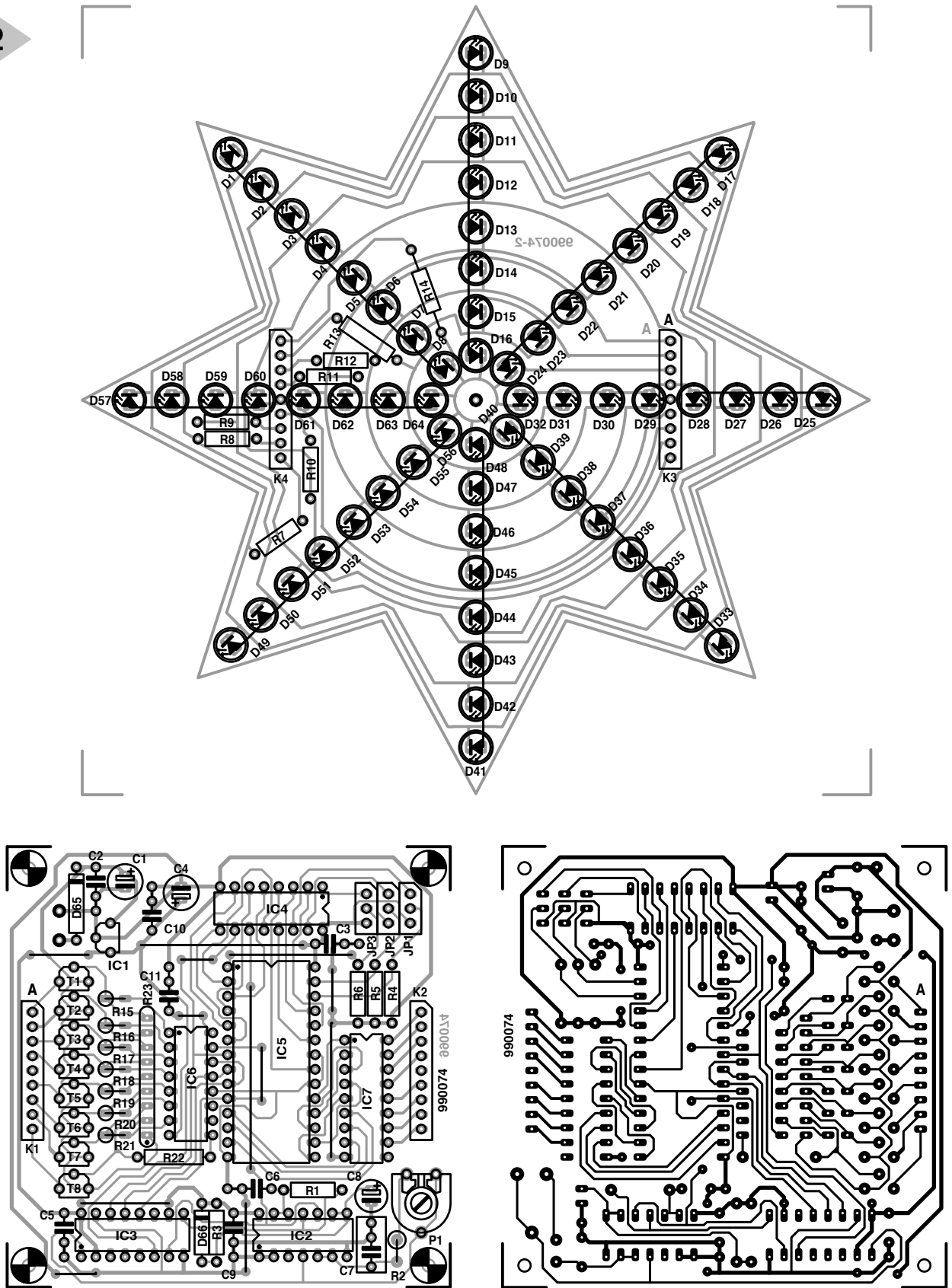


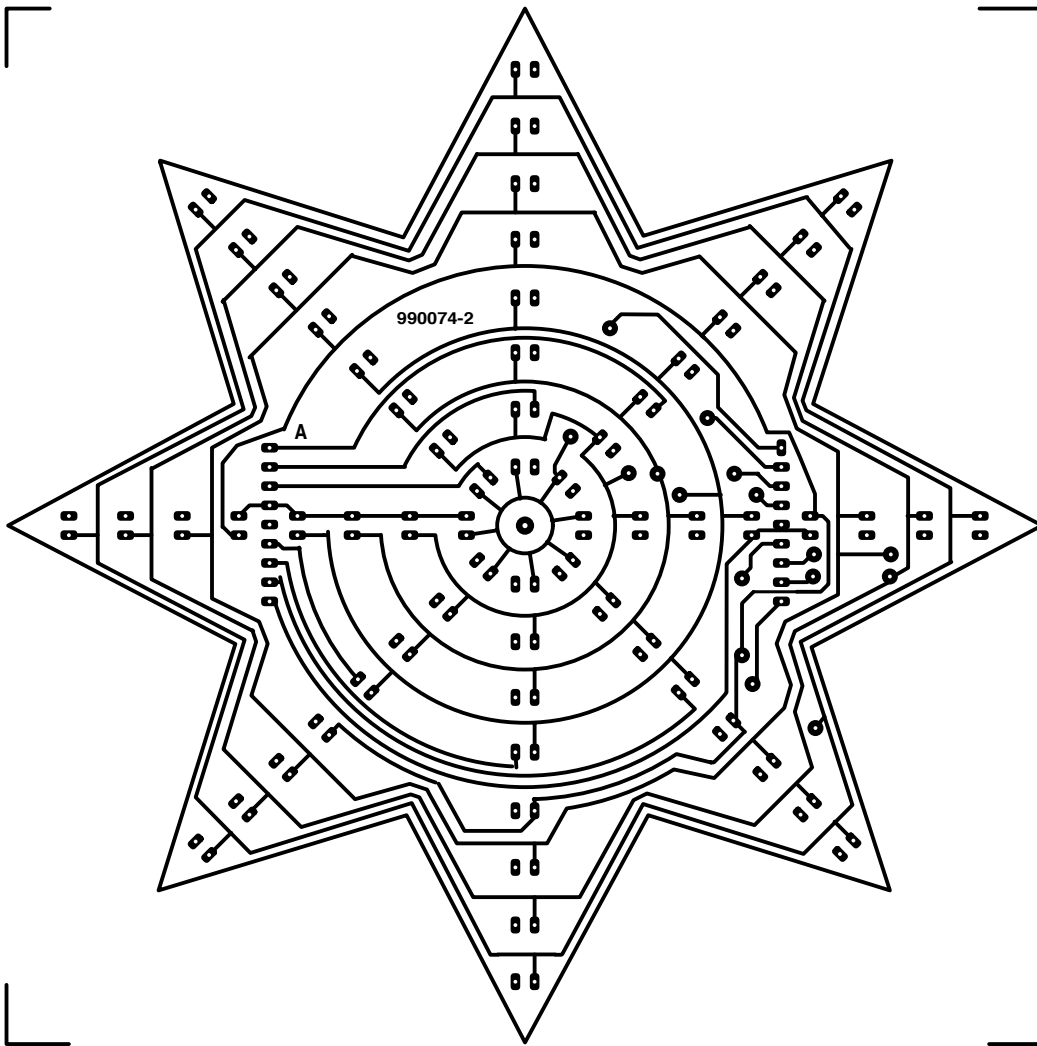
Figure 2. Control board and LED star board. If desired, different patterns may be programmed on the control to create other figures (PCB not available ready-made).

that can be used to power the integrated circuits. Because the LED current does not flow via the regulator, the voltage regulator will not require a

heatsink. The number of different patterns may be expanded almost indefinitely. The largest memory device that can be accommodated is a 512-kByte EPROM with room for 65,536 states.

Jumpers JP1, JP2 and JP3 select the EPROM type used:

EPROM	JP3	JP2	JP1
27C512	c	c	c
27C256	a	c	c
27C128	a	a	c
27C64	a	a	a



COMPONENTS LIST

Resistors:

R1, R2 = 47k Ω
 R3-R6 = 100k Ω
 R7-R14 = 100 Ω (1k Ω when using high-efficiency LEDs)
 R15-R22 = 4k Ω
 R23 = 8-way SIL array, 4k Ω
 P1 = 500k Ω preset H

Capacitors:

C1 = 100 μ F 25V radial

C2, C3, C5, C9, C10, C11 = 100nF

C4 = 47 μ F 25V radial

C6 = 47nF

C7 = 470nF

C8 = 10 μ F 63V radial

Semiconductors:

D1-D64 = LED

D65 = 1N4001

D66 = 1N4148

T1-T8 = BC327

IC1 = 78L05

IC2 = 4093

IC3 = 4520

IC4 = 4040

IC5 = 27C512 (order code 996526-1)

IC6 = 74LS145

IC7 = ULN2803A

Miscellaneous:

JP1, JP2, JP3 = 3-way pinheader with jumper

K1-K4 = 2 off 9-way SIL-connector pair (plug and socket)

When buying the LEDs do not be tempted to buy a 'bulk pack', because you risk being landed with different light intensities from individual devices. If you want to employ high-efficiency LEDs, resistors R7-R14 should be increased to 1 k Ω . Connectors K3 and K4 should be mounted at the track side of the star. Construction generally should not present problems, but do observe the polarity of the LEDs (short terminal = cathode). With all parts fitted, carefully inspect the two boards. Next, plug them together, paying good attention to the orientation of the control board, because it is possible to mount it the wrong way around! K1

should go to K3 (A). With everything secured and in place, apply the supply voltage.

In the first program, individual LEDs are switched on one after another. This test allows you to find and eliminate errors caused by solder bridges, broken tracks or incorrectly mounted LEDs. All LED anodes should be interconnected column-wise. This is best done by leaving the anode wires a bit longer than normal, and then joining them by a 'common' rail made from bare wire. This requires 8 extra solder joints. Preset P1, finally, allows the clock rate be adjusted to individual taste.

(990037-1)

*Merry Christmas
 from all the staff at
 Elektor Electronics*

A4 monitor

a compact high-end loudspeaker

The A4 monitor is an exclusive design for home constructors and is of a quality that should approach the limits of what is currently possible with a two-way system. It is certainly one of the most impressive small loudspeakers that we have ever listened to. Audio enthusiasts with space problems in their home will find the design ideal for their requirements.

The name of the design is derived from the dimensions of the front panel which are the same as those of A4 paper. The A4 has only one drawback: it is not cheap!



Some parameters

◆ Type of enclosure	Bass reflex
◆ Net volume	About 9 litres
◆ Dimensions	298×210×269 mm (11.73×8.27×10.59 in) (h×w×d)
◆ Drive units	Bass/mid-range: Scan-Speak Type 15W8530K00 (15 cm) High-frequency: Scan-Speak Type D2904/980000 (28 mm)
◆ Sensitivity	85.5 dB/W at 1 metre
◆ Nominal impedance	8 Ω
◆ Power rating	60 W
◆ Estimated cost (per loudspeaker, excl enclosure)	About £250

Design by R Smulders

INTRODUCTION

For all sorts of reason, domestic loudspeakers should be as small and unobtrusive as possible. However, the fundamental efficiency equation

$$\eta_0 = k_n f_3^3 V_B$$

(where $k_n = 2 \times 10^{-6}$ for a well-designed bass reflex enclosure, and 10^{-6} for a good-quality sealed enclosure, f_3 is the -3 dB low-frequency rolloff point, and V_B is the volume of the enclosure in litres), shows that any alteration of volume or cutoff frequency affects the efficiency. So, if the volume of the enclosure is reduced, either the low-frequency range must be curtailed or a lower efficiency must be accepted. In these days of high power amplifiers, lowering the efficiency is no problem, so that to a certain degree the bandwidth can be maintained in a small enclosure. Clearly, this cannot be continued *ad infinitum* owing to the thermal power handling limit of the speech coil and the increasing non-linearity of the reflex port and/or air volume.

In the A4 Monitor the designer has succeeded, by careful design, to arrive at the correct compromise of two seemingly incompatible properties: small dimensions and high quality of sound reproduction. The bass reflex tuning is very well calculated, the sturdy enclosure is free of any resonances, the cross-over filter is perfectly tuned, and, last but not least, the A4 uses two brand-new high-end drivers from the Danish manufacturer Scan-Speak.

The result of the meticulous design is that the quality of the A4 is very close to that of much larger units and provides a detailed and realistic sound with a surprising bass performance. In fact, during tests, many listeners (who could not see the loudspeakers) thought they were listening to much larger ones.

TWO-WAY SYSTEM

The times when a two-way system was referred to somewhat disparagingly or even derisively as 'only a two-way system' are long gone. After the short-lived euphoria of four- or five-way systems had died down, many high-end manufacturers happily reverted to two- and three-way systems. An answer to the perennial question of what is better, a two-way or a three-way system, can only be given when all circumstances are known. Even then, it should be borne in mind that any multi-way system is a compromise. The ideal solution would be a loudspeaker with a single driver providing a straight phase and frequency response over the entire audio range from 20 Hz to 20 kHz.

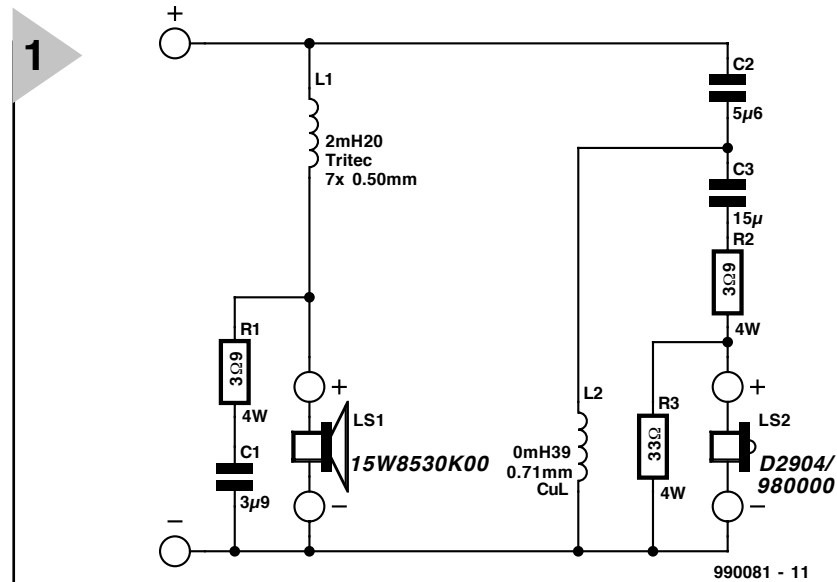


Figure 1. The crossover filter consists of two sections: a 1st-order low-pass for the bass/mid-range driver, and a 3rd-order high-pass for the tweeter.

Since such drive units do not (yet) exist, the audio range is perforce reproduced by two or three drivers. At the cross-over frequencies of these units inevitable errors arise which are not easily obviated or remedied. It is therefore the aim of most manufacturers to limit the number of crossover frequencies, that is, the number of drivers.

The choice of the number of drivers in a multi-way system is determined by the required reproduction. If, for instance, a very high sound pressure level over the bass range is required, a woofer with a diameter of not less than 25 cm is needed. Unfortunately, units with such a large diameter have a tendency of causing bunching at the low middle frequencies. This makes them unsuitable for use at frequencies above about 1 kHz. This precludes their use in a two-way system, because there are no tweeters that cover the frequency range 1–20 kHz. Dome tweeters with a diameter of 28 mm usually cannot reliably handle frequencies below 2–3 kHz, while 19 mm models have a lower limit of 4–5 kHz.

If sound pressure levels below 100 dB in the bass range are acceptable, a smaller woofer may be used. However, since an SPL (sound pressure level) of at least 100 dB is needed to do justice to modest level bass sounds, this normally rules out frequency responses extending below 50 Hz. However, the bass/mid-range driver specified for the A4 is capable of producing an adequate acoustic output at low frequencies.

Bass drivers with a diameter of 13–17 cm are perfectly capable of reliably reproducing frequencies up to

2–3 kHz, which makes the use of a mid-range driver unnecessary. The design of some of these smaller woofers is such that they can reproduce bass frequencies very satisfactorily in a relatively small enclosure. The unit used in the A4 monitor is a good example of one.

CROSSOVER FILTER

The passive crossover filter ensures that the two drivers are provided with the section of the frequency range intended for them. It is carefully designed to match the properties of the drivers and the enclosure. Constructors are advised not to use a different filter (or drive units) since this would result in a highly unsatisfactory loudspeaker.

The circuit diagram in **Figure 1** shows that the design of the filter is straightforward. The 1st-order low-pass section (response rolls off at 6 dB/octave) for the bass/mid-range driver consists primarily of inductor L1. Network R1-C1 corrects the rising impedance of the driver at high frequencies; without it the filter would not function correctly. Since the internal resistance of the inductor must be as low as feasible, it consists of seven turns of 0.5 mm diameter copper wire, which gives an effective wire thickness of 1.5 mm. This construction results in an internal resistance of only 0.52 Ω. Another advantage of using twisted wire is a sharp reduction of the skin effect.

The 3rd-order high-pass section (response rolls off at 18 dB/octave), consists of capacitors C2 and C3, and inductor L2. Potential divider R2-R3 attenuates the power applied to the

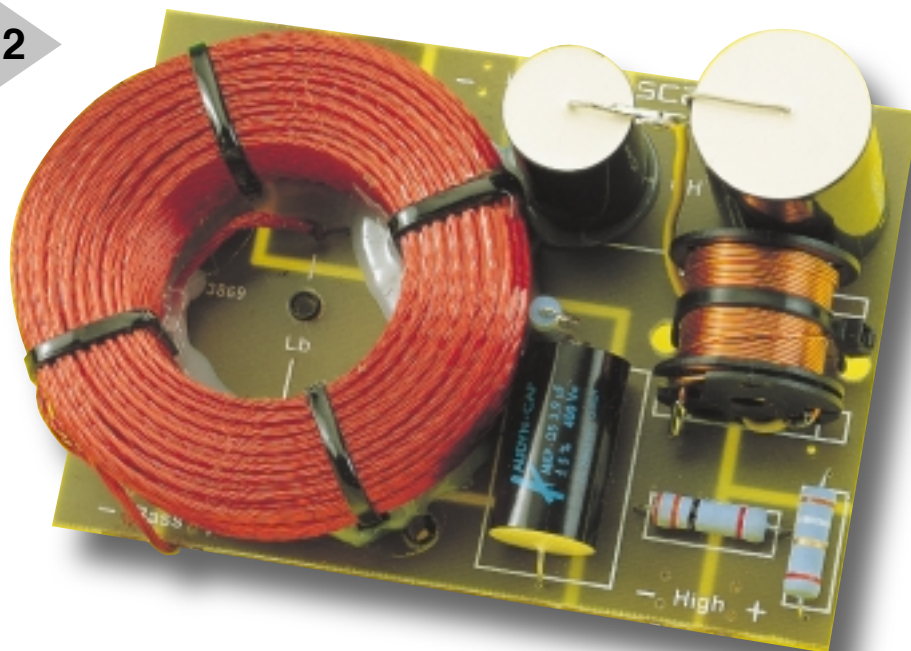


Figure 2. Photograph of a finished prototype crossover filter. Note the special air-cored inductor, L1.

tweeter by about 5 dB, which results in the sound output of the tweeter being in harmony with that of the bass/mid-range unit. This is necessary since, as usual, the sensitivities of the two drivers are dissimilar.

Capacitors C2 and C3 must be of the highest quality since this influences the performance greatly. They should, therefore, be at least metallized polypropylene (MKP, Siemens) types. According to the designer, it is better for C2 to consist of two tin foil (KPSn) types of $1\ \mu\text{F}$ and $4.7\ \mu\text{F}$ respectively, and C3 of two parallel-connected $10\ \mu\text{F}$ MKP types in series with a $4.7\ \mu\text{F}$ KPSn type. However, no differences between a prototype fitted with MKP capacitors and another fitted with KPSn capacitors were discerned during listening tests.

The overall filter is designed for a crossover frequency of 2 kHz. A prime aim of the design was to make the transit from bass/mid-range to high

frequencies seamless, in which, in our opinion, the designer has succeeded very well. A glance at the frequency response characteristic in **Figure 4** will show that the crossover point is not detectable.

Because of the small number of components, these can just be soldered together as appropriate or be housed on a general-purpose filter board, which is available from most audio/loudspeaker retail shops.

It is important to note that, as shown in Figure 1, the bass/mid-range driver and tweeter are connected to the filter in phase. Do not make a mistake in the polarity as this would seriously impair the loudspeaker's performance.

A photograph of a finished prototype of the filter is shown in **Figure 2**.

ENCLOSURE

The construction of the A4 Monitor is relatively simple: just six panels with

some essential openings fastened together — bracing panels or struts are not needed. In fact, the enclosure could readily be built with reference to **Figure 3**, were it not for a few salient details.

To start with, note that the tweeter is not mounted centrally, which, together with the rounded corners of the front panel, is imperative for obtaining the correct radiation pattern.

Further, in contrast to usual practice, the bass reflex port is at the rear of the enclosure. The port consists of a slightly conical 123 mm long PVC pipe with a diameter of about 35 mm. This pipe is commercially available — see the Components List.

Undesired panel resonances are obviated by using 22 mm thick medium-density fibreboard (MDF) for the side, top and bottom panels, and 30 mm thick MDF for the front panel. Internally, all panels are covered with 4 mm thick strips of lead sheet (expen-

COMPONENTS LIST

Drive units:

LS1 = 15W8530K00 (Scan-Speak)
LS2 = D2904/980000 (Scan-Speak)

Components:

R1, R2 = $3.9\ \Omega$, 4 W, low-inductance type
R3 = $33\ \Omega$, 4 W, low-inductance type
C1 = $3.9\ \mu\text{F}$, MKP (polypropylene, Siemens)

C2 = $5.6\ \mu\text{F}$, KPSn or MKP (see text)
C3 = $15\ \mu\text{F}$, KPSn or MKP (see text)
L1 = 2.2 mH, Tritac 7×0.50 mm
L2 = 0.39 mH, air-cored, made with 0.71 mm dia. enamelled copper wire

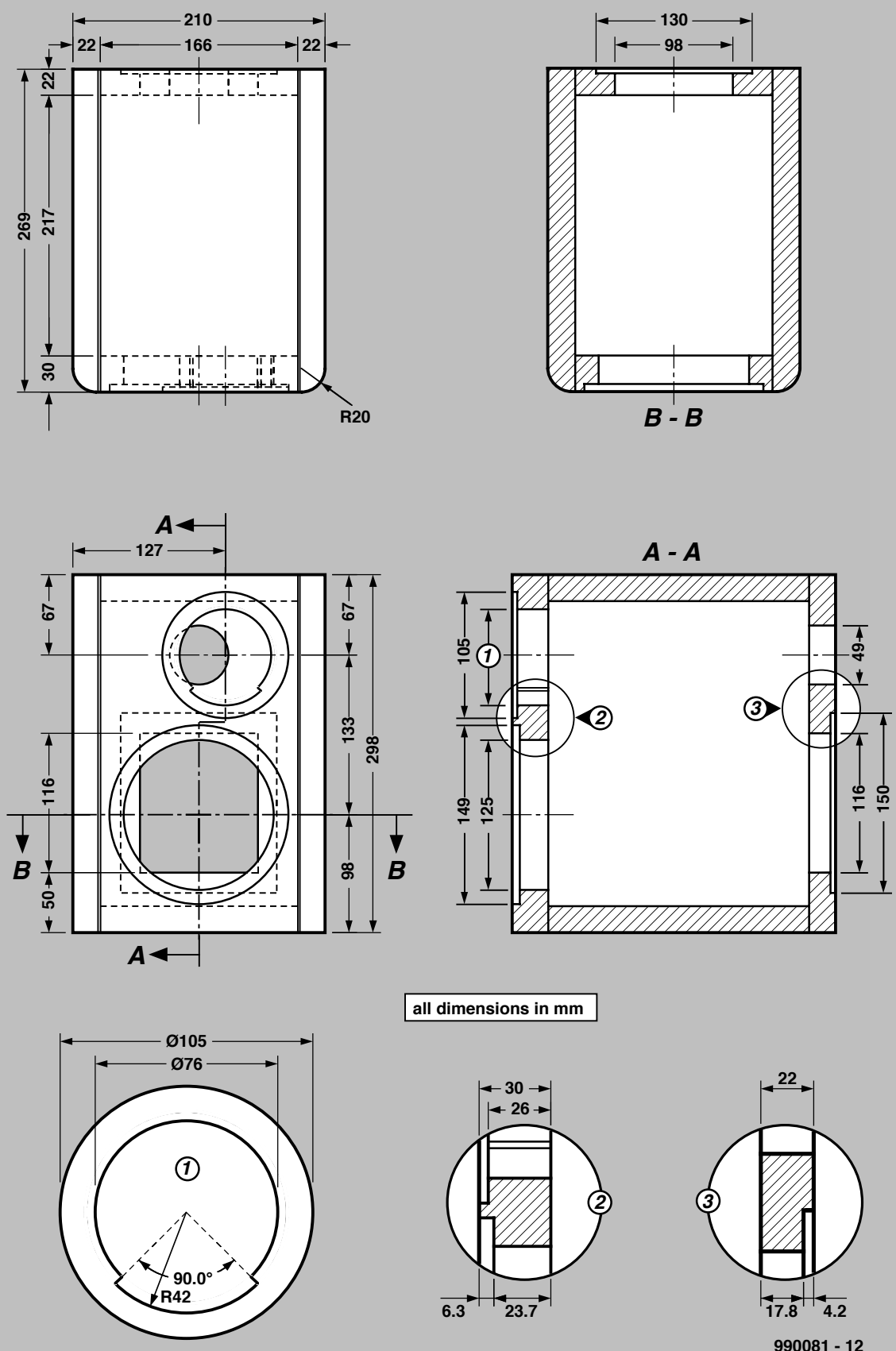
MDF (medium density fibreboard)

front panel: $298 \times 189 \times 30$ mm
back panel: $298 \times 189 \times 22$ mm
side panels: $298 \times 289 \times 22$ mm (2 off)
top and bottom panel: $217 \times 266 \times 22$ mm (2 off)

Miscellaneous:

Terminal board, e.g., Intertechnik Type T150/130
Bass reflex port: Intertechnik Type HP35 (dia. 35 mm; length 125 mm)
Lead sheet or bituminous impregnated felt: 3 strips 25×33 cm (4 mm thick)
Latex foam wadding: as required (42 mm thick)

3



all dimensions in mm

990081 - 12

sive!) or bituminous impregnated felt. Provided all the carpentry work is first class, the enclosure remains stock-still.

As shown in Figure 3, the drivers are flush-mounted — if this is not done, the frequency response will

have a few dips. In the prototype, even the terminal boards are flush-

mounted, but that is of cosmetic interest only.

Figure 3. Construction diagram of the enclosure with all necessary details and dimensions.

4

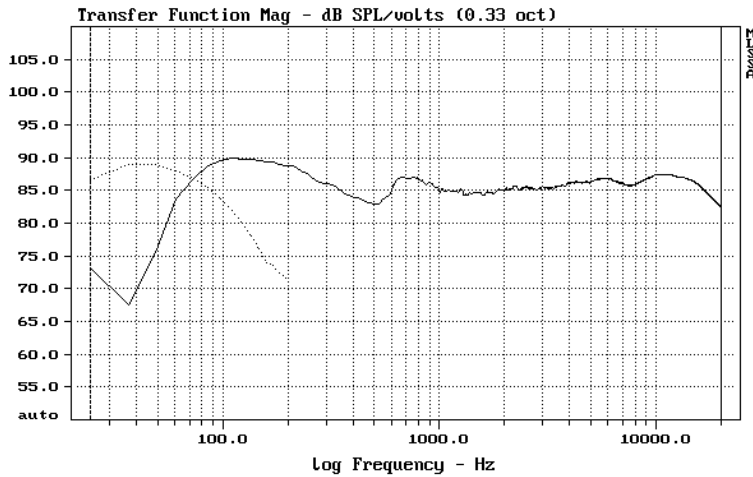


Figure 4. The frequency vs sound pressure level (SPL) characteristic shows an exemplary response.

Although the Components List specifies a heavy-duty terminal board with dual connections from Intertechnik, there are other boards available that are smaller and can still cope with heavy-duty loudspeaker cable. Moreover, there are boards with two terminals and others with four terminals – the choice depends on whether bi-wiring will be used or not.

Acoustic damping is obtained by covering the lead sheet or bituminous felt with latex foam wadding. It is, of course, essential that this material is cut carefully around the various openings, so that it does not get into the way when the drivers or reflex port are being fitted.

The crossover filter is best fitted on the inside bottom panel. Good-quality loudspeaker cable should be used for interwiring the units.

Finishing the exterior of the enclosure is a matter of individual taste. Currently, a lac-

quer finish is very popular, but veneer remains

the choice of many. Lacquering is best carried out by a car body workshop; this will cost a few bob, but the result is good looking and durable.

BENCH TEST

So as to obtain a good and faithful impression of the performance of the A4 Monitor, testing consisted of an introductory listening test, followed by a bench test, and finally an extensive listening test.

The bench test results and listening tests were in good harmony and yielded no unexpected surprises. All the same, the listening tests exceeded the expectations engendered by the bench test results, that is, the loud-

speaker sounds better than the measurements indicate.

The frequency response characteristic is

shown in Figure 4. The generally smooth and flat response with a slight emphasis around 100 Hz does not call for much comment. There is a slight hump of 1.5 dB at about 750 Hz, preceded by a slight dip at about 500 Hz. These tiny blemishes do not detract from the practical performance. They are certainly not caused by the bass/mid-range driver, because the response of this is as straight as a pencil. In fact, they are caused by the small dimensions of the front panel as is the case with most small enclosures.

The response shown by the dotted curve in Figure 4 was measured directly in front of the bass reflex port. The port is tuned to 40 Hz, which is more clearly shown by the impedance characteristic in Figure 5.

The characteristic in Figure 5 also shows that the impedance does not drop below about $7\ \Omega$, which means that the loudspeaker can be driven by virtually any suitable power amplifier. It is advisable, however, to use an amplifier that has a good power reserve, because the sensitivity of the loudspeaker is rather low: about 85.5 dB/W at 1 m.

LISTENING TEST

Although bench testing is important, a loudspeaker's performance can be judged properly only from an extensive listening test.

Although the A4 Monitor is small and inconspicuous, it produces a remarkably open and faithful sound. Good live recordings are particularly well reproduced. The reproduction of sound details in the middle and high ranges is almost reminiscent of an electrostatic unit. Bass performance is dry and taut and extends further down than expected. The $-3\ \text{dB}$ point is at around 40 Hz.

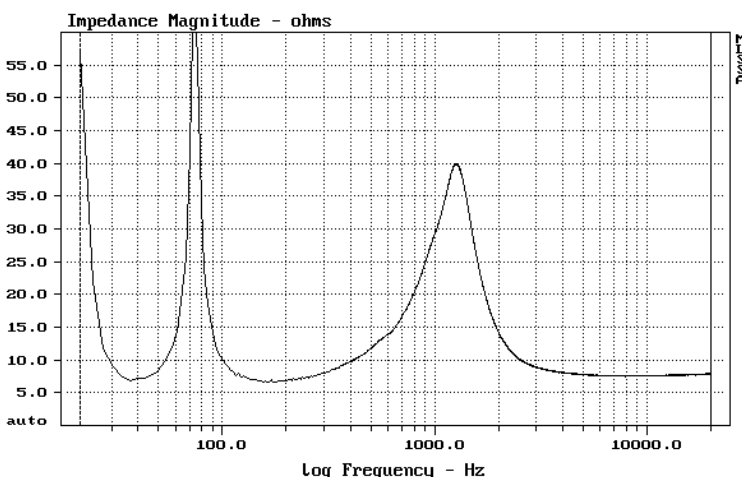
As expected of a quality loudspeaker, the A4 Monitor has no preference for any kind of music: classical music, jazz, and popular music are reproduced equally well: smoothly and in a neutral manner. The characteristic voices of Luciano Pavarotti, Lou Reed, Ella Fitzgerald, and Sarah Brightman, are reproduced as faithfully as the violin of Itzhak Perlman, the clarinet of Benny Goodman, and the guitar of John Williams.

In short, the A4 Monitor is one of those rare loudspeakers that quickly makes you forget that you are testing and gets you wholly absorbed in the music.

Nevertheless, it must be borne in mind that a small loudspeaker, even one as good as the A4 Monitor, has certain limitations at low frequencies. Yet, the A4 does not emphasize these – they only become apparent when a direct comparison is made with a large loudspeaker. Even then, a loud-

Figure 5. The frequency vs impedance characteristic of the loudspeaker shows that the impedance does not drop below $7\ \Omega$. The dip at around 40 Hz corresponds to the tuning of the bass reflex port.

5



The drivers

The drive units used in the A4 Monitor are products of the Danish company Scan-Speak. This company was an independent manufacturer until some years ago when it was acquired by Vifa — it is now the high-end branch of that organization. Most of Scan-Speak's drivers are hand-made, high-quality cone and dome models. The Type D2905/990000 tweeter ('Revelator'), which has been in production since the 1980s, has acquired an enviable reputation throughout the world and is generally considered to be one of the best dome tweeters on the market.

The chassis of both drive units used in the A4 Monitor is relatively new. The bass/mid-range unit is also called 'Revelator' by the manufacturer, which may be seen as an indication of its high quality.

The bass/mid-range driver has a frame designed for optimum air throughput and an exceptionally long travel of the voice coil. Because of the absence of resonances, excellent damping of the reinforced paper diaphragm, and the linearity of the cone suspension, the unit offers virtually unequalled faithful reproduction and dynamic performance for its size.

The tweeter represents a change of direction at Scan-Speak: until now all their tweeters had a textile diaphragm, but the new one used in the A4 Monitor has an aluminium dome.

Any dome has a series of dips (nulls) in its pressure response at frequencies where the path difference between the apex and the rim is a multiple of $\lambda/2$ of that frequency in air. A phase difference ensues near these nulls which causes the axial output to fall gently towards the null.

The frequency, f_n , at which the null occurs is a function of the height, h , of the dome. In a 28 mm aluminium dome ($h = 5$ mm),

$$f_n = c/\lambda = 345/5 \times 10^{-3} = 69 \text{ kHz}$$

so that the first dip occurs at 34.5 kHz. In a dome unit that is driven by a speech coil of the same diameter attached to the rim, the first breakup resonance occurs near or just before the first phase null, that is, here, 34.5 kHz, which is well above audibility.

The tweeter has a low resonant frequency (500 Hz). Its reproduction of the highest frequencies is linearized by a special singly suspended diffusor. Its sound is remarkably open, clean and well detailed.



speaker with a volume ten times greater than that of the A4 Monitor was needed to show up these low-frequency differences.

Since the bass reflex vent is at the rear of the enclosure, the loudspeaker must, of course, not be placed directly against a wall. Even so, it was felt during the test that placing the Monitor close to a wall gave better results than with the unit well away from it. This is because that position gives that

little extra warmth at low frequencies which is missing when the loudspeaker is well away from a wall. In the latter case, the A4 Monitor sounds rather more clinical.

More information on the drive units and filters from

Wilmslow Audio
50 Main Street
Broughton Astley

Leicestershire LE9 6RD
Tel.: 01455 286603
Fax: 01455 286605
e-mail: info@wilmslow-audio.co.uk

Also note Wilmslow Audio's special offer for the drive units, as advertised elsewhere in this issue.

[990081-1]

mains adaptor switch

improves adaptor efficiency

Mains adaptors are used more and more frequently to power small equipment. A drawback of this is that even when the equipment is switched off, the adaptor continues to draw a small current from the mains supply. The present switch reduces this current and at the same time offers the incidental benefit of decreasing the stray field around the adaptor.



INTRODUCTION

The use of a mains adaptor for powering small equipment has an important advantage in that it enables the equipment to be used anywhere in the world. All that is necessary is for the adaptor to be suitable (as far as input voltage and frequency are concerned) for use with the local mains supply. This is inexpensive and efficient. Unfortunately, it also has a drawback: the adaptor works independently of the equipment it powers. This means that even when the load is switched off, the adaptor continues to operate. In other words, it goes on taking energy from the mains supply.

If the adaptor is a modern type based on a switch-mode arrangement, the energy loss is small. However,

many adaptors consist merely of a transformer, rectifier, buffer capacitor and, sometimes, a voltage regulator. This kind of setup is not very efficient which means that there is a certain amount of energy loss: in practice around one watt. Another less pleasant property is that the transformer generates a stray field. This field may be so large that in order to comply with the MPRIII norm the distance between the adaptor and its load must be not less than 30 cm (12 in).

DETECTORS

At the primary side of the transformer, the mains adaptor draws energy from the mains supply. At the secondary side, it supplies energy to a load. In the

Electrical characteristics

Current drain of detector	< 75 μ A
Maximum adaptor rating	20 W
Input voltage	5–18 V
Power reduction factor (with idling adaptor)	> 50

Design by H. Bonekamp

absence of a load or when the load is switched off, no current flows at the secondary side. However, owing to non-ideal properties, a small amount of energy continues to be taken from the mains supply and this must, of course, be limited.

When there is definitely no load at the secondary side of the mains adaptor, the adaptor may be switched off. This function is provided by the switch described in this article. It could be said that the switch monitors the output voltage of the adaptor. It should be noted that the switch can work correctly only when the adaptor uses an internal buffer capacitor.

The switch provides two functions: it switches the adaptor on and off periodically and it works as a voltage-dip and current detector. In practical operation this means that the adaptor is switched on for 200 ms at intervals of 1.5 minute, during which time the buffer capacitor in the mains adaptor is (re)charged.

The detector which signals a drop in voltage monitors the voltage across the buffer capacitor in the mains adaptor. When this potential is about to drop below a certain predetermined value, the adaptor is switched on immediately.

The voltage detector has another important function, which enables the output voltage of the adaptor to be held steady. In many mains adaptors the output voltage rises sharply when the output terminals are open-circuited. In the present adaptor the mains voltage is switched off after about 200 ms as soon as the output voltage rises above the preset value. This function is independent of the current detector.

The current detector determines whether or not the load is switched on. When a current flows through the load, the adaptor is actuated, and the load is switched on. How the theory becomes a practical arrangement is shown in **Figure 1**.

CIRCUIT DESCRIPTION

The lower part at the left of the circuit diagram in **Figure 1** comprises the primary side of the mains adaptor, and the upper section, the secondary side. Although not immediately evident from the diagram, the circuit uses only standard components. At the same time, it has been kept compact and is readily constructed on the printed-circuit diagram in **Figure 2**. Its electrical characteristics are conform relevant specifications.

In the design of the circuit, great care was given to minimizing the energy consumption. Network R_1 - R_2 - C_1 , diodes D_1 - D_3 and buffer capacitor C_2 ensure a fairly steady 5 V supply voltage. The current drawn

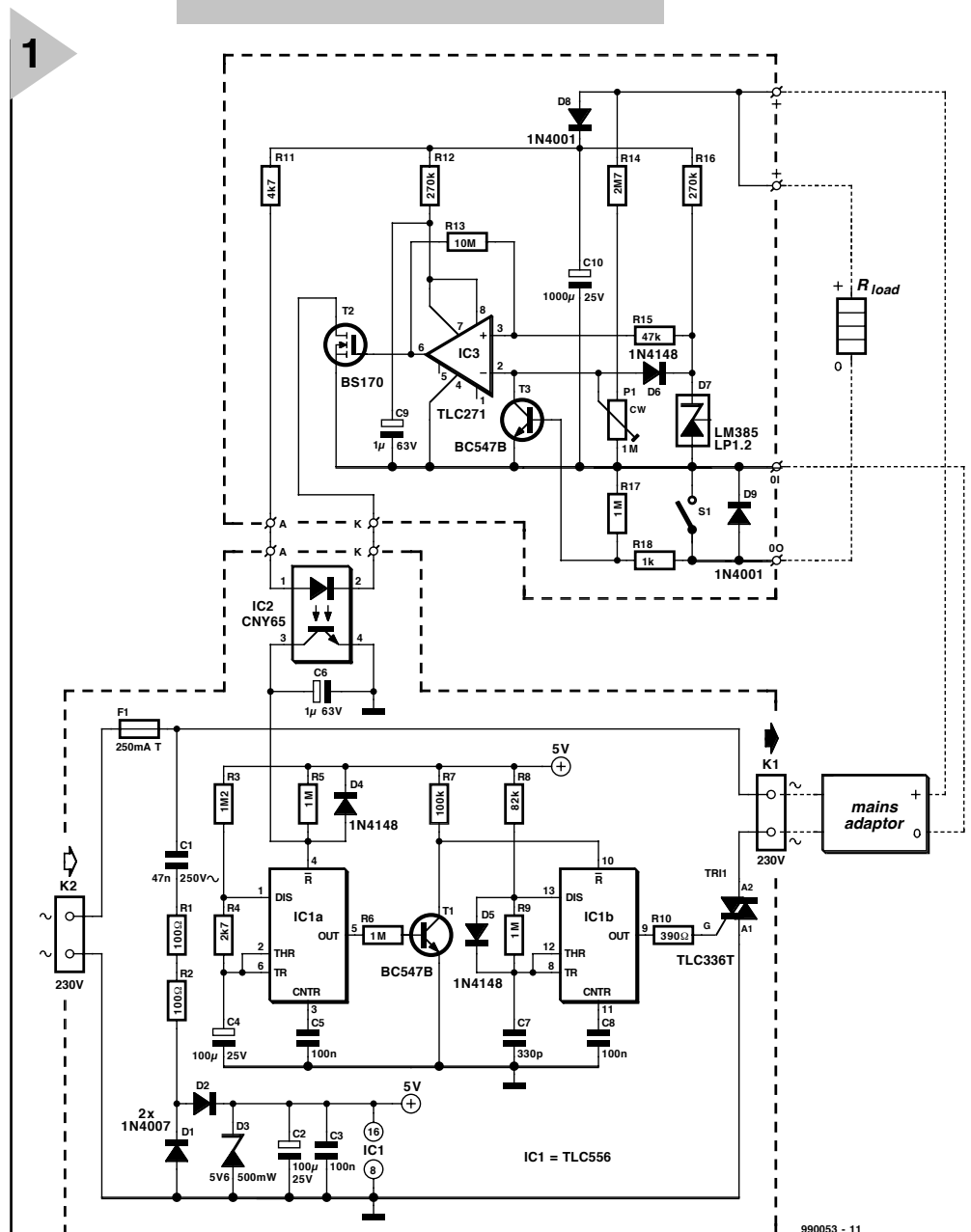
from the mains supply is about 3.4 mA. The energy dissipated in the circuit is small: only 12.8 mW.

The mains adaptor is switched on and off by triac Tri_1 . Since an inductive load is switched, constant drive is needed. Assuming a gate current of 5 mA, the triac may be triggered in each quadrant. To reduce the energy consumption, it was decided to use a pulsating trigger current. The duty factor is 10 per cent and the trigger duration is not smaller than 20 μ s (which is the lower threshold of the triac). Keeping the trigger frequency high ensures minimal asymmetry between the two periods and insignificant direct current. This arrangement results in an average trigger current of only 0.5 mA.

The trigger pulses are generated by IC_{1b} , whose gate current is limited by R_{10} . With component values as specified, the trigger pulses are 27 μ s long (time constant R_8 - C_7), and are repeated every 230 μ s (time constant $0.7R_9$ - C_7). These values result in 78 trigger pulses per 20 ms period, which is high enough to cause the earlier mentioned undesired side effects (direct current) to be suppressed. The trigger circuit is switched via the reset input (pin 10).

The trigger circuit is controlled by a second astable multivibrator (AMV), IC_{1a} . This stage produces a 200 ms pulse every 90 seconds. During the 200 ms that the output is low, the reset input of IC_{1b} is high after the level has been inverted in T_1 , whereupon the

Figure 1. Circuit diagram of the mains adaptor switch. The design is based on standard components: special components and esoteric circuitry are not used.



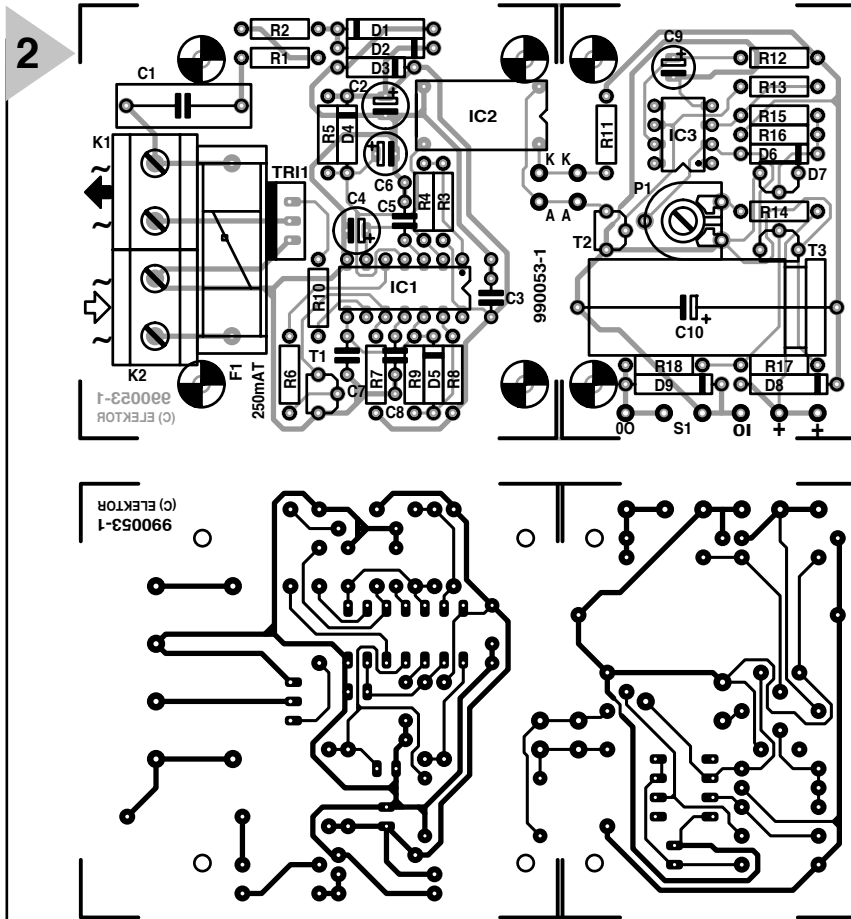


Figure 2. The printed-circuit board for the adaptor switch should normally be cut into two sections as indicated.

Parts list

Resistors:

$R_1, R_2 = 100 \Omega$
 $R_3 = 1.2 \text{ M}\Omega$
 $R_4 = 2.7 \text{ k}\Omega$
 $R_5, R_6, R_9, R_{17} = 1 \text{ M}\Omega$
 $R_7 = 100 \text{ k}\Omega$
 $R_8 = 82 \text{ k}\Omega$
 $R_{10} = 390 \Omega$
 $R_{11} = 4.7 \text{ k}\Omega$
 $R_{12}, R_{16} = 270 \text{ k}\Omega$
 $R_{13} = 10 \text{ M}\Omega$
 $R_{14} = 2.7 \text{ M}\Omega$
 $R_{15} = 47 \text{ k}\Omega$
 $R_{18} = 1 \text{ k}\Omega$
 $P_1 = 1 \text{ M}\Omega$ preset

Capacitors:

$C_1 = 0.047 \mu\text{F}, 250 \text{ V}\sim$
 $C_2, C_4 = 100 \mu\text{F}, 25 \text{ V}, \text{ radial}$
 $C_3 = 0.1 \mu\text{F}, \text{ ceramic}$
 $C_5, C_6 = 0.1 \mu\text{F}, \text{ MKT (metallized polyester)}$
 $C_6, C_9 = 1 \mu\text{F}, 63 \text{ V}, \text{ radial}$
 $C_7 = 330 \text{ pF}, \text{ ceramic}$
 $C_{10} = 1000 \mu\text{F}, 25 \text{ V}$

Semiconductors:

$D_1, D_2 = 1\text{N}4007$
 $D_3 = \text{zener diode}, 5.6 \text{ V}, 500 \text{ mW}$
 $D_4\text{--}D_6 = 1\text{N}4148$
 $D_7 = \text{LM}385\text{LP}1.2$
 $D_8, D_9 = 1\text{N}4001$
 $T_1, T_3 = \text{BC}547\text{B}$
 $T_2 = \text{BS}170$

Integrated circuits:

$\text{IC}_1 = \text{TLC}558$
 $\text{IC}_2 = \text{CNY}85$
 $\text{IC}_3 = \text{TLC}271\text{CP}$
 $\text{Tr}1 = \text{TLC}3361 (\text{STS})$

Miscellaneous:

$K_1, K_2 = 3\text{-way terminal strip for board mounting}, \text{pitch } 7.5 \text{ mm}$
 $S_1 = \text{toggle switch}, \text{single make contact}$
 $P_1 = \text{Fuse holder with protective cap and } 250 \text{ mAAT fuse for board mounting}$
 Mains adaptor case: Bopla (available from Phoenix at 01296 398355)
 PCB Order no. 990053-1 (see Readers Services towards the end of this issue)

triac is triggered.

To ensure that there is sufficient time for the reservoir capacitor in the adaptor to be charged after the system has been switched on, a special start-up circuit, $R_5\text{--}C_6\text{--}D_4$, has been added. The charging of the capacitor is essential to provide the secondary side of the adaptor with a supply voltage.

The reset input of IC_{1a} is also used to trigger the triac in case early recharging of the buffer capacitor becomes necessary. The need for early recharging is signalled by the secondary detector circuit. Since the circuit is powered directly by the mains supply, the secondary detector circuit is linked to IC_{1a} via an optoisolator to ensure the requisite electrical isolation between the two.

Note that the triac is deliberately not provided with a snubber network, since it is disabled without any problem as soon as the buffer capacitor is charged to a sufficient degree.

ADDITIONAL DETAILS

The detector circuit was designed to carry out its work with as little energy dissipation as feasible. The basic design requirement was that the circuit could be operated for not less than 2 minutes by a $1000 \mu\text{F}$ capacitor. A further requirement was that the detector could be set to work with voltages between 5 V and 15 V.

The reference voltage is produced

by zener diode D_7 , which can operate with a current of only $10 \mu\text{A}$.

The series resistor in the supply line for the op amp results in the top end of the voltage range over which the device is to be operated to be raised from 18 V to 20 V.

An interesting aspect of the present design is that the optoisolator is switched via a separate MOSFET, T_2 .

When the adaptor voltage drops below the threshold level set with P_1 , the output of the op amp goes high, whereupon the triac is triggered. Resistors R_{13} and R_{15} provide the requisite hysteresis.

Detector diode D_9 may be switched into circuit, or out of it, by switch S_1 . With component values as specified, a current of only 0.5 mA is sufficient to switch on T_3 . The periodical switching is actuated continuously, which ensures that the mains adaptor remains linked to the mains supply.

A final remark about the stray field produced by the mains adaptor. When the adaptor works without load, it is switched on for only 1/450 of the time. The consequent reduction in the H -field is directly proportional with this factor.

CONSTRUCTION

The small dimensions of the mains adaptor switch make it ideally suitable for being enclosed in a plastic (ABS) case with integral mains supply lead

specially designed for applications like the present. The photograph in **Figure 2** shows that the switch is simply connected between a mains supply outlet and the mains adaptor.

The printed-circuit board (which is available ready made – see Parts List) may be cut into two, which is, in fact, essential when the switch is to be fitted in the special enclosure. The two sections are mounted one above the other with the aid of 10 mm plastic spacers. They are interlinked by short lengths of insulated circuit wire between terminals 'K' and terminals 'A'.

Input terminals O_1 and + , output terminals O_o and + , and switch S_1 , are best located on the front panel of the enclosure.

There is little that can be said about populating the board sections other than that it is advisable to use the specified components and that the fuse holder should preferably be one with a protective cap. It is also advisable, but not essential, to use shrink sleeving on the input and output terminals and the the switch terminals.

Before finalizing the construction, drill a 4 mm hole in the lid of the case

exactly opposite P_1 . This enables the switching level of the voltage detector to be adjusted with P_1 after assembly has been completed.

Insert the plug on the mains adaptor into the socket inlet on the switch; connect the output of the adaptor to the input terminals of the switch, and the equipment to be powered to the output terminals of the switch. Finally, insert the adaptor switch into a suitable mains outlet socket.

[990053]

WHEN ELECTRONICS WAS YOUNG (10)

In 1888, the American researcher Oberlin Smith (1859–1934) published his thoughts on magnetic recording, which in 1898 led Valdemar Poulsen (1869–1942) to publish a method of recording sound — magnetic recording. Poulsen found that by passing the output current from a microphone through an electromagnet and drawing a piano wire rapidly past it, the wire was magnetized to varying degrees. This could be played again and again and could also be erased and re-recorded. Unfortunately, owing to the materials then available, the design was poor and forgotten until the 1930s when it was revived in Germany with the steel wire replaced by magnetic tape. Today, Poulsen is better remembered for his invention in 1902 of the arc generator for the production of radio waves.

When John Ambrose Fleming (1849–1945) visited Edison during a visit to the USA, Edison showed him a carbon-filament lamp in which a metal plate had been sealed. When the plate was connected to the positive terminal of the filament, a current flowed, which did not happen when the plate was linked to the negative terminal. On his return home, Fleming carried out researches which culminated in his filing a patent for the first thermionic valve. This consisted of a vacuum tube containing a cathode heated to incandescence by an electric current and an anode. When the anode was maintained at a positive potential with respect to the cathode, an electric current could flow from cathode to anode, but not in the opposite direction. Thus, this two-electrode tube, or diode, acted as a rectifier that could be used to change alternating current (a.c.) into direct current (d.c.).

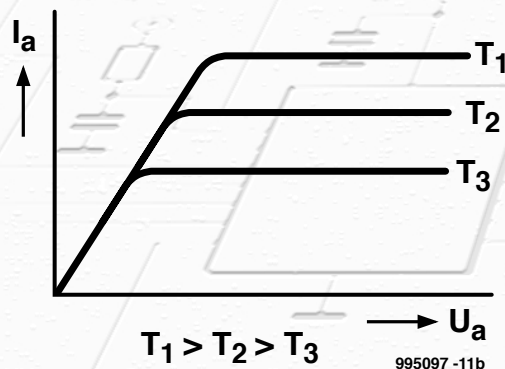
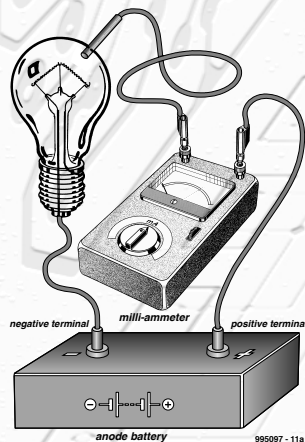
While Fleming was developing the two-electrode thermionic valve,

the American physicist, Dr Lee de Forest (1873–1961) was working on similar lines and in 1906 applied for a patent for a three-electrode vacuum tube — the triode. This device is essentially a diode with an additional electrode (the grid) between cathode and anode, which can be used to amplify weak electrical signals. The amplification is achieved by applying a voltage to the grid with which the anode current can be controlled. Of far greater importance than the diode, the triode was crucial in the development of radio communication, radar, television, and computers. It remained an essential component for over fifty years before it was largely superseded by the transistor.

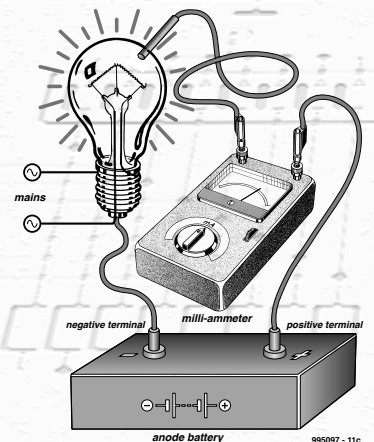
At about the same time, an Austrian inventor, Robert von Lieben, also carried out research on a three-electrode valve, and applied for a patent in 1906. Unfortunately for von Lieben, his patent was lodged later than that of Lee de Forest and has never been acknowledged outside Austria.

Lee de Forest's work was attacked by Fleming in the courts on the basis that de Forest's invention was dependent on his, Fleming's, diode. De Forest has always insisted that he was not aware of Fleming's patent before taking out his own. The court battles lasted from 1907 until 1943. Originally the courts upheld Fleming's claim that the addition of the grid was dependent on his work, but in 1943 the United States Supreme Court finally decided in favour of de Forest on the basis that the original Fleming patent had always been invalid.

[995097-1]



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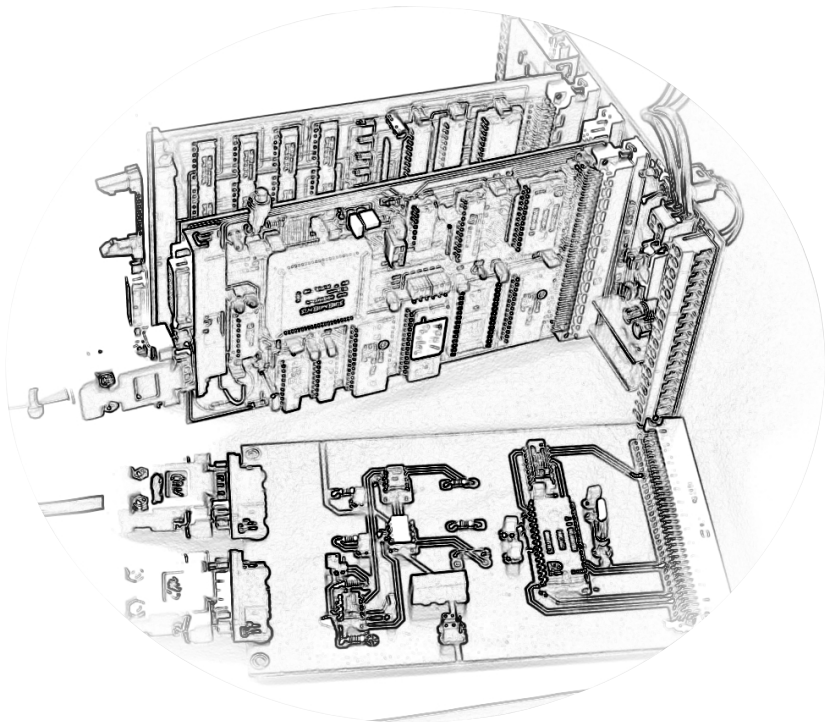
995097 - 11c

Principle of vacuum rectifier

controller area network (CAN)

intelligent, decentralized data communications in practice: Part 4

A Controller Area Network obviously consists of more than just the CAN bus interface described in last month's instalment of this article. In fact, the interface is merely the link between a microcontroller or computer and the CAN bus proper. The hardware described in detail last month clearly needs software for its proper operation and this is described in this fourth instalment of the article.



INTRODUCTION

Each station or node in a CAN bus system needs, apart from the CAN Bus Interface, a microcontroller or computer with appropriate software. Two sets of software are needed for taking the station into use, test it, and operate it: operating software and applications software.

The operating software is needed to provide an effective overall system, and also to test the interface in association with the microcontroller or computer. Such a test shows whether or not the drive from the microcontroller or computer functions correctly, whether or not the interface works correctly, both from a hardware and a

software point of view, and whether the data is transferred correctly onto the CAN bus. The test thus enables a simple communication path between two or more nodes to be set up.

The applications software is specific to the particular role performed by the microcontroller or computer in the network. It therefore depends on what the station is going to be used for: logging of measurements; driving a display; transferring times and dates; and others.

Each node therefore needs its own particular software appropriate to its function. The sum of all the functions carried out by the various stations is the desired overall function of the net-

CAN ADDRESS	SEGMENT	OPERATING MODE		RESET MODE	
		READ	WRITE	READ	WRITE
0	control	control	control	control	control
1		(FFH)	command	(FFH)	command
2		status	–	status	–
3		interrupt	–	interrupt	–
4		(FFH)	–	acceptance code	acceptance code
5		(FFH)	–	acceptance mask	acceptance mask
6		(FFH)	–	bus timing 0	bus timing 0
7		(FFH)	–	bus timing 1	bus timing 1
8		(FFH)	–	output control	output control
9		test	test; note 2	test	test; note 2
10	transmit buffer	identifier (10 to 3)	identifier (10 to 3)	(FFH)	–
11		identifier (2 to 0), RTR and DLC	identifier (2 to 0), RTR and DLC	(FFH)	–
12		data byte 1	data byte 1	(FFH)	–
13		data byte 2	data byte 2	(FFH)	–
14		data byte 3	data byte 3	(FFH)	–
15		data byte 4	data byte 4	(FFH)	–
16		data byte 5	data byte 5	(FFH)	–
17		data byte 6	data byte 6	(FFH)	–
18		data byte 7	data byte 7	(FFH)	–
19		data byte 8	data byte 8	(FFH)	–
20	receive buffer	identifier (10 to 3)	identifier (10 to 3)	identifier (10 to 3)	identifier (10 to 3)
21		identifier (2 to 0), RTR and DLC	identifier (2 to 0), RTR and DLC	identifier (2 to 0), RTR and DLC	identifier (2 to 0), RTR and DLC
22		data byte 1	data byte 1	data byte 1	data byte 1
23		data byte 2	data byte 2	data byte 2	data byte 2
24		data byte 3	data byte 3	data byte 3	data byte 3
25		data byte 4	data byte 4	data byte 4	data byte 4
26		data byte 5	data byte 5	data byte 5	data byte 5
27		data byte 6	data byte 6	data byte 6	data byte 6
28		data byte 7	data byte 7	data byte 7	data byte 7
29		data byte 8	data byte 8	data byte 8	data byte 8
30		(FFH)	–	(FFH)	–
31		clock divider	clock divider; note 3	clock divider	clock divider

990066-3-13

Table 6. Internal SFRs in the controller used in the basic CAN mode.

work. In other words, the spatially distributed network can be controlled, driven and monitored to arrive at the final result.

OPERATING SOFTWARE

The programming of the CAN controller is subject to the same general principles as that of other external peripheral units.

- The function of the controller is fixed or set by programming sets of data by internal Special Function Registers (SFR).
- These internal SFRs are interpreted by the microcontroller or computer as normal memory addresses in the external RAM range, to which data can be written or from which data can be read. This means that the microcontroller or computer is not aware that it is operating in con-

junction with a CAN controller. Only access to specific memory locations is determinative for it as well as for the applications software.

When, therefore, the applications software for controller IC3 is being produced, the following points should be clarified or processed.

- Set the chip-select base address for the SJA1000 controller.
- Understand the internal setup of the structure of the SFRs in the controller.
- Create the routine for the basic initialization of the controller.
- Create the routine for applying data to the CAN bus.
- Create the routine for receiving data from the CAN bus.

The processing of relevant points for

the basic CAN mode of the controller is looked at in some detail in the following paragraphs. Extensive and more detailed information can be found in the data sheets and application notes for the controller (see Reference at end of this article).

SETTING THE CHIP-SELECT BASE ADDRESS

The chip is accessed via the chip-select base address. Since controller IC3 in the basic CAN mode needs a coherent external address range of 32 bytes, and in the PeliCAN mode one of 128 bytes, the maximum range is set at 128 bytes so as not to preclude the use of the PeliCAN mode in future operations.

The SJA1000 controller is enabled by a low level at its \overline{CS} terminal (pin 3). This means that the microcontroller or computer must construct its address

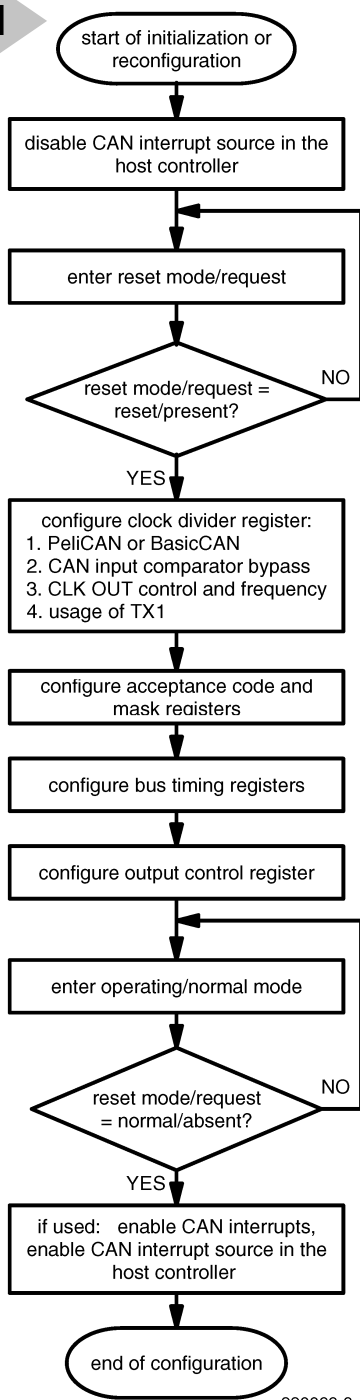


Figure 13. Flow diagram for use when the CAN controller is to be initialized.

coding in such a way that within a coherent address range of not fewer than 128 bytes a low signal is produced at pin 8 of connector K3 to enable the data transfer to be carried out by the CAN controller. The first address at which this is the case becomes the so-called **chip-select base address** of the controller. When the microcontroller or computer accesses a random memory location in this

address range, it receives the byte content of an SFR in the controller or it can write a byte-word in an SFR of the controller.

In the following it is assumed that the chip-select base address of the SJA1000 controller is F000H.

INTERNAL STRUCTURE OF AN SFR

The determinant SFRs of controller IC3 for operation in the basic CAN mode are shown in **Table 6**. The meaning of the various columns is as follows.

1. The first column, CAN address, gives the internal addresses of the relevant SFRs, to which only the chip-select base address of the IC needs to be added. If, for instance, the status register of the controller is to be accessed, F000H must be added to the internal address of the SFR, which is 2. If, therefore, a read or write operation on the register is desired, the software must be programmed to enable the external RAM location to be accessed with address F002H. The Clock Divider Register is from then on accessible at address F01FH (= F000H + 31D – note the use of different number systems).

2. The second column shows the basic division of the SFRs into three different groups: the control group, the transmit buffer group, and the receiver buffer group.

3. The controller supports two software-controlled modes:

- **Operating mode**, which is the normal mode of operation;
- **Reset mode**, which is the mode IC3 is in when it is clearing a hardware reset or when the reset bit in the control register is set. The controller then reverts to the normal operating mode.

The reset mode is necessary when the controller is to be (re)initialized, that is, certain operating parameters can be set only in the reset mode. The reset bit is then set (the controller sets its normal operating mode), whereupon the relevant parameters can be altered, after which the reset bit is disabled. After that, the controller resumes operation with the altered parameters.

4. Columns 4 and 5 show

- the functions of the register;
- the meaning of the contents when the register is read;
- the meaning of the contents when the register is written to in the operating mode.

5. Columns 5 and 6 show the relevant

data for the register in the reset mode. Here is an example of an internal SFR with address 4.

Operating mode (normal operation of the controller):

- Read – although reading the register is possible, there are no usable results since the read-out value is always FFH.
- Write: the register cannot be written to.

Reset mode (the controller is in the reset state).

- Read: reading the register gives the value of the acceptance code.
- Write: a new acceptance code can be written into the register.

This example shows that during normal operation of the controller this SFR has no special function. Note, however, that in the reset mode the acceptance code with which the controller functions during normal operation is set.

CREATING THE ROUTINE FOR BASIC INITIALIZATION

Before work on this routine is begun, a close look at the Application Note for the SJA1000 controller (AN97076 – see Reference) is highly advisable. On page 23 of this document, the manufacturers give a flow diagram with detailed comments on how the initialization of the controller should be proceeded with (see **Figure 13**).

Another close look at the description of a single register should then enable the values of the parameters to be set readily to individual requirements and wishes.

CREATING THE ROUTINE FOR SENDING DATA

As mentioned earlier, CAN controller type SJA1000 assumes most of the tasks involved in sending data. The sending of byte data onto the CAN bus requires only four actions.

- Delivery to the controller of the wanted identifier (ID) for the frame to be transmitted.
- Indicating how many data bytes are to be sent (0–8).
- Determining whether the frame is a remote transmission request (RTR) frame or not.
- Writing the wanted data bytes to the send data buffer of the controller.

That's all! The remainder of the process is carried out automatically by the CAN controller, that is:

- assembling the frame;
- calculation of the CRC sum;

- allocation of the other fields in the frame;
 - accessing the bus;
 - transmitting the frame;
 - checking for errors;
- and so on.

Messages indicating whether the transmission was successful or not are returned to the user via the Status register to enable action to be taken as appropriate.

CREATING THE ROUTINE FOR RECEIVING DATA

In the reception of data, CAN controller types SJA1000 again takes on most of the necessary actions, that is, data are received almost wholly automatically by the controller. The controller processes the received frames and writes the wanted information contained in them to the error detection section and acceptance filter in its RXFIFO (= receiver first in first out memory) – see **Figure 14**.

If the acceptance filter is switched off, each received frame is evaluated. In the RXFIFO, the following data from each frame are stored (see Table 6, address range 20–29):

- frame identifier;
- remote transmission request (RTR) bit;
- data length code (DLC);
- useful data bytes.

As the range of the internal RXFIFO in IC3 is exactly 64 bytes, the number of frames that can be stored in the intermediate memory depends on the length of the frame, and more particularly on the data length code.

The receiver buffer window (see Table 6, addresses 20–29) that can be read by a user is what is shifted by the RXFIFO to the window. This consists of an actually received set of data (frame or message), which can be processed by the user via software.

Communication between the SJA1000 and the microcontroller or computer in the receive mode may take two forms.

- **Interrupt-driven.** When the controller has received a complete and error-free frame, it initiates an interrupt in the microcontroller via its pin 16 (INT). This causes the microcontroller/computer to react immediately to the received message so that this can be read without delay via the controller.
- **Polling* operation.** In this kind of

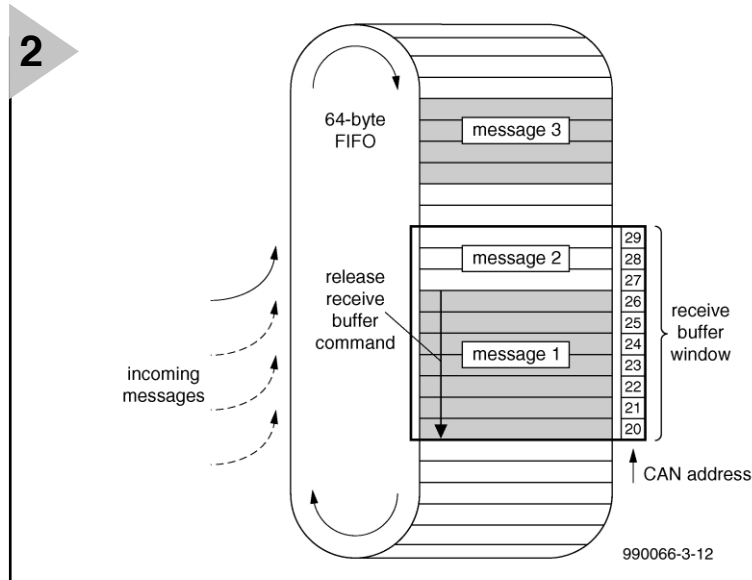


Figure 14. Structure of the receiver memory range.

operation, the receiver buffer status bit in the status register of the controller is continuously interrogated by the microcontroller/computer. When this is set – indicating that the controller has received at least one message correctly – the software reads this frame and processes it as relevant.

When a message has been read, the applications software reenables the receiver buffer window to acknowledge that the earlier message passed to it has been processed. The window is then ready to receive the next frame from the RXFIFO. In this way, the applications software ensures that one frame after another is processed.

There are two further matters to be noted.

- Immediately after a frame (message) has been read and processed, the receiver buffer window must be released by a 'release receive buffer command' so that the controller can shift the next message to the window. If this command is not given, the same message is processed again and again, which causes the RXFIFO to overflow since other received frames are not being shifted.
- When a high frame rate is used, that is, when the data transfer rate is high or many messages are sent one after another, there is a risk of the RXFIFO overflowing rapidly if the messages are not shifted readily. If such situations are likely to occur, a sufficiently powerful micro-

controller or computer must be used in association with high-quality

software.

When an overflow of the RXFIFO occurs, the controller indicates this by setting an error-bit, that is, a Data Overrun Status bit in the status register. The relevant message, which is just about to be shifted into the RXFIFO (and which caused the overflow) is then erased and lost.

[990066-4]

Only part of the software needs to be programmed by the constructor, since in next month's issue a complete applications program in Pascal will be published which enables all basic functions of the CAN bus to be tried and tested. The suggested microcontroller is a Type 80C537. Apart from the 80C537 used in the single-board companion published in the June 1997 issue of this magazine, there is now a smaller, less expensive version of this Single-Board Computer (SBC) available. This version will be highlighted in next month's issue under the title '537-Lite Computer'.

Reference:

CAN bus controller and transceiver modules (Philips Semiconductors)
www.us.semiconductors.philips.com/can/
www-us.semiconductors.philips.com/can/support

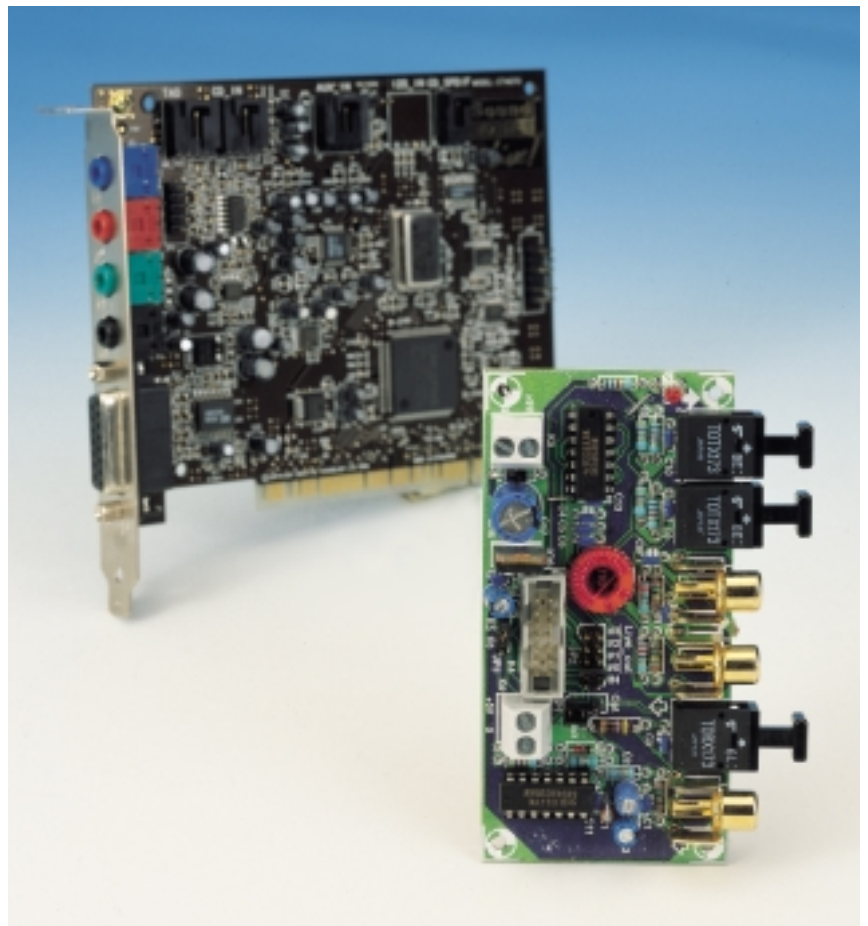
* Polling is a form of time division multiplexing. It is a process by which one node (primary station) in a network can address any other node (secondary station), giving the secondary node access to the communication channel.

digital inputs and outputs

for the SoundBlaster[®] Live!Value card

Without any question, the most popular sound card for the PC is currently the SoundBlaster Live!, together with its less expensive cousin Live!Value. The main difference between the two is that the Live! version has an additional plug-in card with digital inputs and outputs.

The design presented here gives owners of a Live!Value card the opportunity to equip it with the necessary optical and coaxial digital inputs and outputs.



Nowadays, a modern PC cannot do without sound. Most computers thus contain a sound card, which offers a large number of features. Until recently, such cards had only analogue inputs and outputs, but presently there are also models available with connectors that allow digital audio signals to be read in or sent out. This makes it much more convenient to, for example, read in a digital signal from a DAT or MD recorder, edit it on the PC and then play it back or record it on a CD-R, all without any intermediate analogue stage.

The SoundBlaster Live! is one of the most widely distributed sound cards with digital audio I/O. The digital I/O portion is contained on a separate plug-in card with its own bracket, on which the digital connectors are mounted. The 'stripped-down' version of the Live! card set, the Live!Value, is naturally much more attractively priced, but this comes at the expense of the digital I/O card.

Since the Live!Value card has an expansion connector that houses all the necessary signals, it seemed an excel-

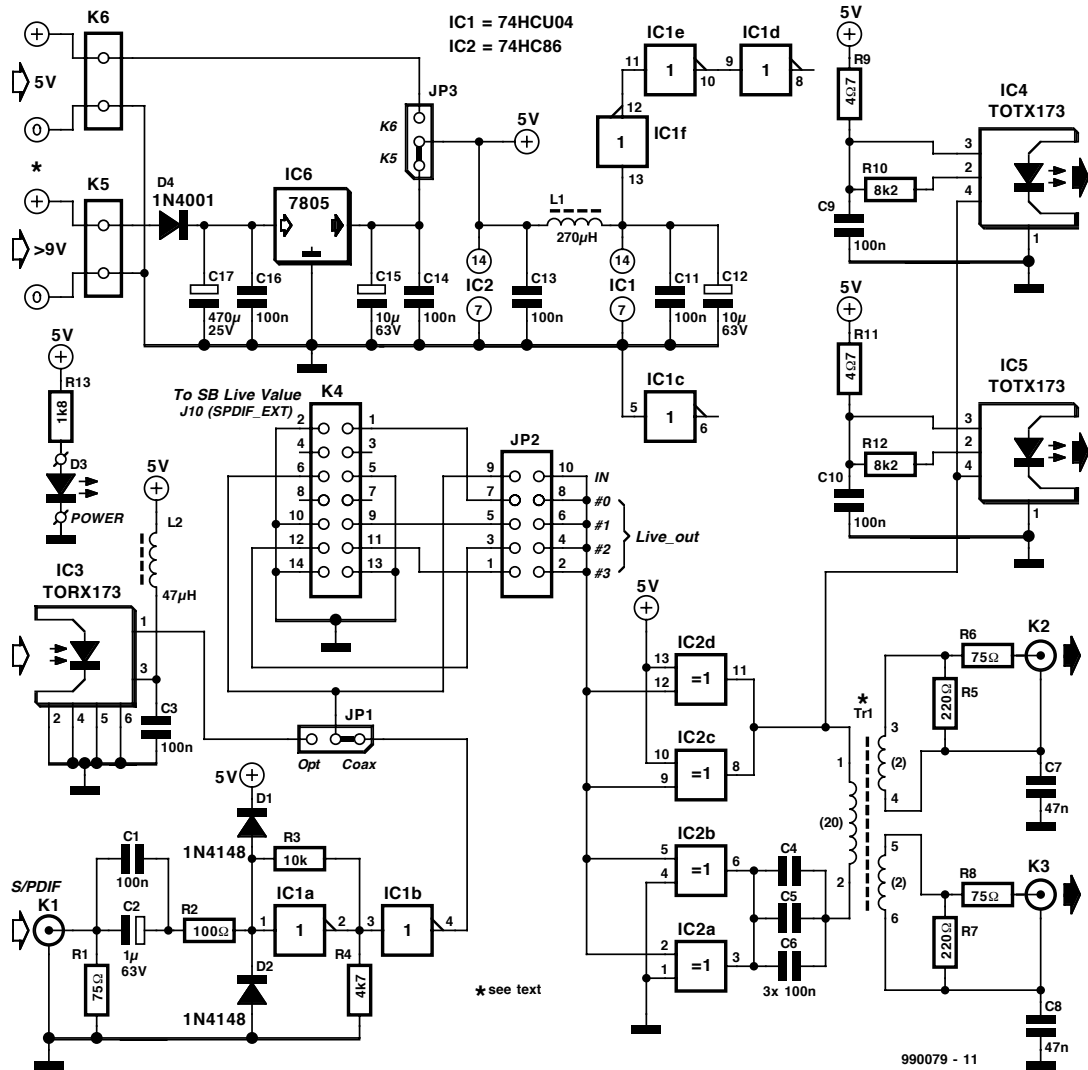


Figure 1. The schematic diagram of the expansion card circuit, which mainly consists of input and output connectors. There are in total two digital inputs and four digital outputs.

lent idea to design a DIY card with digital audio connectors that can simply be connected to the expansion connector via a length of flat cable. In this way, owners of a Live!Value card can easily upgrade it.

To make everything perfectly clear, this design has been developed to work with the standard version of the Live!Value card, which has a 12-pin S/PDIF expansion connector (refer to your owner's manual). At the moment, there is a new version available, called the Live!Value 1024, which has a different type of expansion connector and which already has a coaxial digital output as a standard feature.

MINIMAL HARDWARE

Connector J10 on the Live!Value card is a set of 12 pins arranged in a double row at the edge of the sound card, and labelled SPDIF_EXT (see Table 1). This connector contains one S/PDIF input and four S/PDIF outputs. One pin also provides + 5 V, passed through from the PC supply. No specifications are available for this pin. For this reason, we have assumed that the digital

expansion card will be powered via a direct connection to the internal + 5 V supply line of the PC or — if the card is used external to the PC — via a mains adapter.

Since all required signals are present at the S/PDIF expansion connector, it is only necessary to add a few connectors and buffers. If you look at the schematic diagram in Figure 1, you will see that the active components form a relatively small part of the total.

Two digital inputs are present, one of which is optical (IC3, a standard TOSLINK receiver) and the other coaxial (K1, for an S/PDIF input signal of 0.5 V_{pp} into 75 Ω). The active input connector can be selected via jumper JP1.

A proven circuit, using two inverters of a 74HC04 (IC1), is used to process the incoming S/PDIF signal from the coaxial connector. IC1a is used as an analogue amplifier. The incoming signal is first amplified by a factor of seven (without clipping). The average level of the amplified signal

thus lies in the region of the switching point of the second inverter. IC1b again amplifies the signal to produce clean CMOS logic levels. R4 holds the input of IC1b a bit below the switching point in the

Table 1. Pinout specifications of the 12-pin S/PDIF expansion connector (J10) on the SB Live!Value card.

Pin	Name	Description
1	SPDIFO# 0	S/PDIF-0-output
2	GND	ground
3	KEY	
4	VCC	supply (+ 5 V)
5	GND	ground
6	SPDIF_IN	S/PDIF-input
7	-	not connected
8	-	not connected
9	SPDIFO# 1	S/PDIF-1 output
10	GND	ground
11	SPDIFO# 2	S/PDIF-2 output
12	SPDIFO# 3	S/PDIF-3 output

2

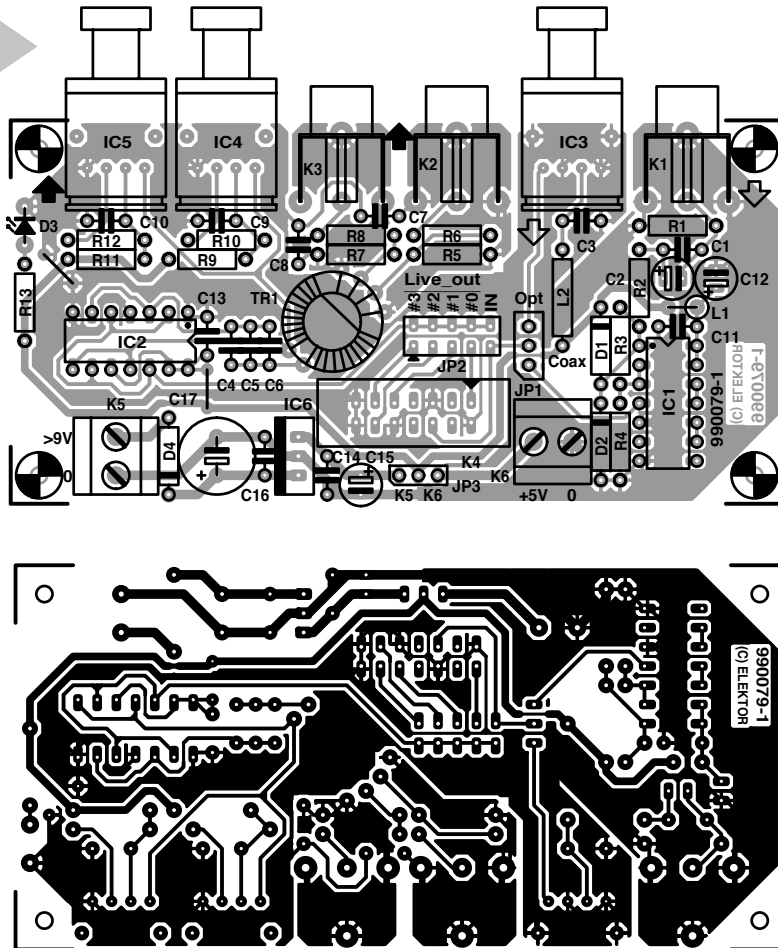


Figure 2. The printed circuit board layout shown here accommodates all of the connectors shown in the schematic diagram, so that the card can readily be fitted into a separate enclosure or on the rear side of a 5¼" panel insert.

COMPONENTS LIST

Resistors:

R1,R6,R8 = 75Ω
 R2 = 100Ω
 R3 = 10kΩ
 R4 = 4kΩ7
 R5,R7 = 220Ω
 R9,R11 = 4Ω7
 R10,R12 = 8kΩ2
 R13 = 1kΩ8

Capacitors:

C1,C3-C6,C9,C10,C11,C13,C14,C16 = 100nF ceramic, pitch 5mm
 C2 = 1μF 63V radial
 C7,C8 = 47nF ceramic
 C12,C15 = 10μF 63V radial
 C17 = 470μF 25V radial

Inductors:

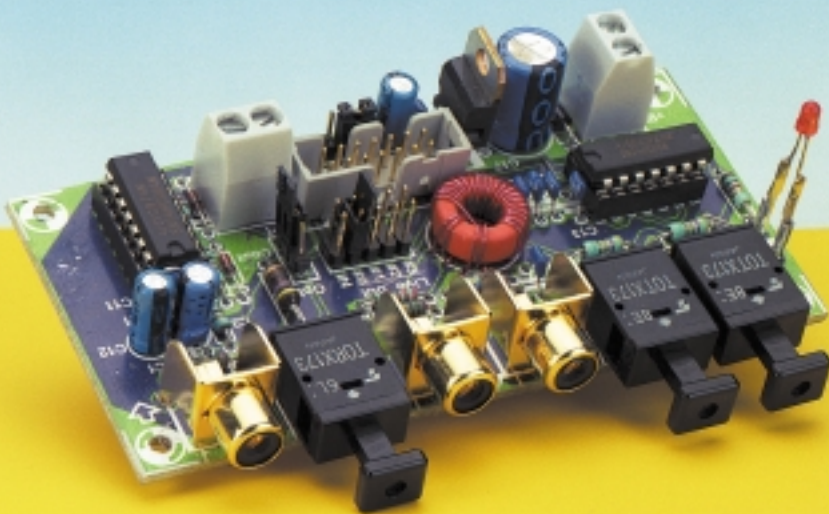
L1 = 270μF
 L2 = 47μF

Semiconductors:

D1,D2 = 1N4148
 D3 = high efficiency LED
 D4 = 1N4001
 IC1 = 74HCU04
 IC2 = 74HC86
 IC3 = TORX173 (Toshiba)
 IC4,IC5 = TOTX173 (Toshiba)
 IC6 = 7805

Miscellaneous:

JP1,JP3 = 3-way pinheader with jumper
 JP2 = 10-way double-row pinheader with 1 jumper
 K1,K2,K3 = cinch socket, PCB mount (Monacor/Monarch T-709G)
 K4 = 14-way boxheader
 K5,K6 = 2-way PCB terminal block, pitch 5mm
 Tr1 = ferrite core transformer, Philips TN13/7,5/5-3E25, primary 20 turns, secondary 2 x 2 turns. Wire: 0.5 mm dia. (24SWG) enamelled copper.
 PCB, order code 990079-1 (see Readers Services page)



absence of an input signal, so that interference signals do not appear at the output of IC1b due to input noise and the like. R1, D2 and D2 protect IC1 against incorrect input signals.

The middle pin of the input selection jumper JP1 is directly connected to the header K4, which provides the link to the expansion connector of the sound card. A 14-pin box header was chosen for K4, since this is a standard component. Pins 1 through 12 match the connections on the sound card. Pins 13 and 14 are connected to earth on the expansion card and can be used for screening if desired.

All four S/PDIF outputs present at the expansion connector of the sound card are passed through to the expansion card. The jumper block JP2 selects one of the four digital outputs of the Live!Value card to be connected to the outputs of the expansion card. In prac-

Transformer trickery

Driving the output transformer symmetrically, as practised in this design, is rather unusual. This is reason enough to provide a few explanatory remarks.

The first reason for driving TR1 symmetrically is that the amplitude of the resulting primary signal ($10 V_{pp}$) allows the turns ratio between the primary and secondary windings to be increased to 10:1. A coaxial cable must be terminated at each end in its characteristic impedance (75Ω in this case). This suppresses signal reflections that would otherwise occur. The output signal amplitude at the transformer secondary side must thus be $1 V_{pp}$ to provide a voltage of $0.5 V_{pp}$ across 75Ω . The large turns ratio yields a lower output impedance as well as increased bandwidth, due to the better coupling factor that results from the fact that the primary winding covers most of the core.

A second reason for driving the transformer symmetrically is that the primary winding can then be split into two equal halves if a toroidal core is used. The primary and secondary connections thus lie at opposite sides of the core, and the connection between the two halves of the primary winding is essentially a virtual earth point, which further reduces crosstalk between the primary and secondary windings. This improves the electrical isolation in the RF region. The outputs are already damped by R5 and R7 to suppress overshoots.

Resistors R6 and R8 essentially determine the output impedance (75Ω). Capacitors C7 and C8 earth the cable screens for RF. Capacitors C4 through C6 are connected in parallel to improve the quality of the resulting capacitor by minimizing the total effective series resistance. These coupling capacitors are needed to prevent the outputs of the buffer (IC2) from being shorted together via the transformer when no signal is present.

tice, it turns out that the output signal is normally found on the SPDIF# 0 output.

The option of selecting the input signal (IN) has been added as an extra feature. With this selection, the input of the expansion card is connected through to its output. This can be useful for checking the inputs and outputs and/or the input and output signals. It also allows the circuit to be used as optical to coaxial converter (or the other way around), or as an S/PDIF splitter.

The signal from jumper JP2 is passed to the inputs of IC2. Two gates of this quad XOR IC are connected in parallel as a non-inverting buffer (IC2a and IC2b). The other two (IC2c and IC2d) are connected in parallel as an inverting buffer. The latter pair drives the two TOSLINK output modules (IC4 and IC5). This means that when the circuit is used as a converter/splitter (jumper JP2 set to 'IN'), the LEDs in the output modules will be off in the absence of an input signal. The design of the circuitry connected to the TOSLINK modules IC3, IC4 and IC5 is standard, and consists mainly of supply-decoupling components.

The home-made output transformer is driven symmetrically by the two pairs of XOR gates. The reason for using XOR gates is that the two configurations have equal propagation delay times, which results in cleanly symmetric outputs. The transformer provides galvanic isolation between the output connectors (K2 and K3) and the rest of the circuit. This helps to prevent earth loops and other possible sources of interference.

As already mentioned, there are two options for the power supply. If the card is fitted in the PC (behind a $5\frac{1}{4}$ " panel insert, for instance), K6 can be connected directly to the +5 V supply line of the PC by attaching a 'Y' adapter to one of the internal power supply connectors. In this case, put jumper JP3 into the 'K6' position. The other option, with JP3 in the 'K5' position, is intended for when the card is used external to the PC. In this case a mains adapter can be used to supply power. For convenience, a standard 5 V regulator is already present on the card, together with a diode and filter capacitors, so that just a small transformer (9 V/1.5 A) would be sufficient. D4 is intended primarily as protection against wrong-polarity connections. A mains adapter with an unstabilized output of 9 V or more can thus be used as the power source.

CONSTRUCTION

Assembling the circuit board, shown in Figure 2, is not a difficult task. All Cinch sockets, TOSLINK modules and other connectors can be soldered to the board straight away. Sockets may be used for the two digital ICs, while the remainder of the passive and active components can be soldered directly to the circuit board. If you take another good look at the photo, you can quickly and clearly see how everything should be fitted. The only difficult component is the transformer, which you will have to wind yourself. You will need half a metre of 0.5-mm diameter enamelled copper wire and a 13×5.5 -mm toroidal core (see the components list for the part number). Put a

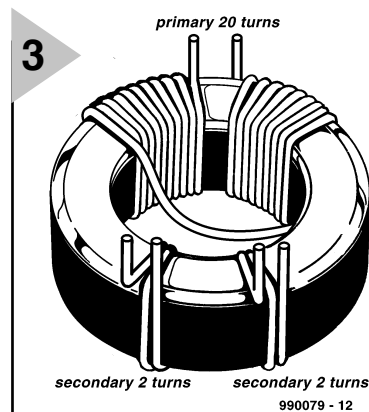


Figure 3. This drawing shows how the output transformer must be wound, with a 20-turn primary and two 2-turn secondaries.

primary winding of 20 turns on the core, and two secondary windings of 2 turns each. The drawing shown in Figure 3 clearly illustrates how the windings should be located on the core.

Depending on where you decide to use the card, you can use a pair of brackets to attach it to the rear of a $5\frac{1}{4}$ " panel insert in which you have made the necessary openings, or you can fit it into a separate enclosure. If the card is fitted inside the PC, it is connected to the Live!Value card with a length of 14-lead flat cable fitted with a 14-way header at each end. When connecting this cable to connector J10 of the sound card, make sure that pin 1 of the cable header is connected to pin 1 of J10.

If the card is mounted external to the PC in its own enclosure, the most convenient solution is to use the flat-cable version of Sub-D connectors. If the same connections are made to the Sub-D connectors at both ends (PC and expansion card), all you have to do is to make sure that pin 1 of the one connector is always connected to pin 1 of the other connector.

Finally, a few general remarks.

You can make the selection of the input connector (between optical and coaxial) variable by connecting the pins of JP1 to a small single-pole, double-throw switch (slide, alternate-action or toggle). Connect the common contact to the centre pin of JP1. Keep the length of the interconnecting wiring to an absolute minimum.

The current consumption of the circuit varies between 60 and 80mA, depending on whether the optical or coaxial input signal is used. If you

Figure 4. The leads from the expansion connector of the SB Live!Value card can be brought to the outside of the PC via a Sub-D connector fitted into a cutout in the computer enclosure.

want to take the risk of powering the expansion card from the + 5V supply of the sound card, you can connect a wire between pin 4 of K4 and the middle pin of the header for JP3. In this case jumper JP3 must not be installed, and the on-board supply components (K4, K6, D4, C14-C17 and IC6) can be omitted.

In conclusion, we would like to remark that driving the additional digital inputs and outputs is only possible with recent versions of the program/driver software (Live!Wire version 2.0 or higher). This is available by download from the special SB Live! web site <http://www.sblive.com>, as well as from other sources.

(990079-1)

Note:

Owners of the newer SB Live!Value 1024 card who want to increase the number of digital inputs and outputs can find the input and output specifications of this card at the on-line help site. With this information, you can even experiment with connecting the expansion card described here to the new version of the sound card, which has several inputs on the expansion connector. We would like to hear about the results!



BASIC Stamp programming course (4)

Part 4: Obstacle Alley

If you drive an automobile, you know the practical application of the Pauli exclusion principle: Two objects can't occupy the same space at the same time. What's true for automobiles is even truer for robots. An autonomous robot has to keep itself from colliding with obstacles. Obstacles might take the form of a wall or post, or they may be mobile like a dog, a person, or another robot.

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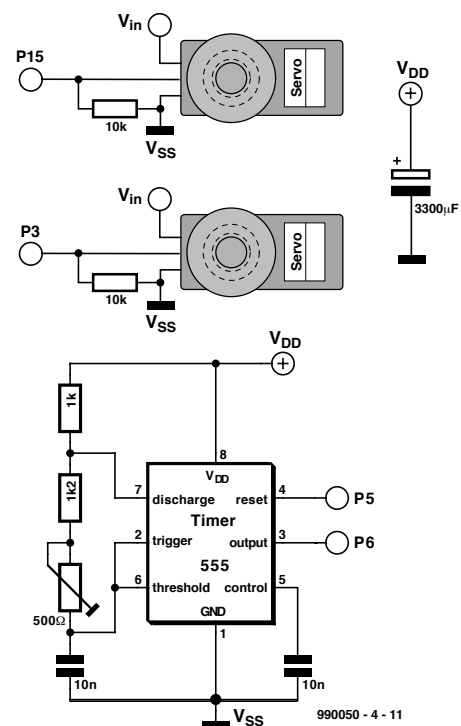


Figure 17. The oscillator and motor drive circuits.

Since the robot can't know the positions of moving objects in advance, it must have some way of detecting obstacles in real time. Humans, of course, use vision. While a robot that can see would be very desirable, it is also quite expensive and difficult to make a vision system appropriate for robotics.

Luckily, detecting obstacles doesn't require anything as sophisticated as machine vision. A much simpler system will suffice. Some robots use RADAR or SONAR (sometimes called SODAR when used in air instead of water). An even simpler system is to use infrared light to illuminate the robot's path and determine when the light reflects off an object. Thanks to the proliferation of infrared (IR) remote

controls, IR illuminators and detectors are easily available and inexpensive.

In this instalment, I'll show you how to add infrared sensors to the BOE-Bot and use them to allow the robot to navigate around objects in its path. Along the way, you'll also see how to program some simple math into the BASIC Stamp and generate random numbers. You'll find the **parts list** close to circuit diagram Figure 18.

IR BASICS

In theory, detecting an object with IR is simple. You simply shine an IR light (an LED) in the forward direction and use a detector to look for the reflected light. In practice, it is somewhat more complicated. If you used this oversimplified approach, the detector will falsely trig-

ger from ambient IR that occurs naturally.

To prevent these false triggers, you'll want to employ detectors that are sensitive to IR modulated at a particular frequency and modulate the IR source to that same frequency. In common remote controls for consumer electronics, the modulation frequency is 38 kHz. You can readily find IR receivers sensitive to this frequency.

While the BASIC Stamp could modulate the light source, the BASIC Stamp can't drive the LED and read the detector at the same time. Therefore, you'll want an external circuit to modulate the LED.

Another refinement useful for the robot is to use two detectors (and possibly two LEDs). You'll place one detector on the left side of the robot and the other on the right. This allows you to detect object and determine its position relative to the robot. If only one detector activates, the object is on that side. If both detectors turn on, the object is dead ahead.

THE OSCILLATOR

IR LEDs are commonplace and work just like regular LEDs. To modulate the LEDs, you can use a 555-based oscillator (see **Figure 17**). The LEDs will operate when input P5 (555 reset) is high. The oscillator output connects to the BASIC Stamp's pin 6. This is not necessary for operation, but it does allow you to calibrate the oscillator to operate at 38 kHz.

To perform the calibration, load the program in **Listing 4** and run it. This displays the frequency in Hertz. You can adjust the frequency by adjusting the potentiometer. The output should be near 38000. Of course, the 555 is not extremely stable, so the value may vary a bit, but it should be close to 38 kHz.

Since IR LEDs don't emit visible light, you might wonder if the circuit is working at all. You should be able to measure the LED's forward voltage across the LED (about 1.2 V). If you measure closer to 5 V, the LEDs are probably installed the wrong way around (usually, the long lead is the anode; the pin that connects to the BASIC Stamp).

Another way to troubleshoot IR LEDs is with a special plastic card that allows you to see the infrared light. Service technicians use these cards to test remote controls. You can buy them where you buy television repair supplies (you can also get them at Radio Shack/Tandy stores). For an electronic alternative, see 'Infra-red Remote Control Tester' in the July/August 1998 issue of *Elektronics*.

IR DETECTION

Once you have the LEDs operational, you'll need to connect the IR detectors

PARTS LIST

Qty	Part
1	Operational BOE Bot
1	3300 μ F 16V electrolytic capacitor
1	500 Ω potentiometer
2	0.01 μ F capacitor
2	0.1 μ F capacitor
1	1k Ω 1/8W or 1/4W resistor
1	1.2k Ω resistor
2	IR LEDs (LD271 or similar)
2	Infrared receiver (Panasonic 4602 or equivalent)
2	470 Ω 1/4W resistor
1	555 Timer IC

(see **Figure 18**). The detectors look like transistors with a bulge on one side. The bulge is the sensitive area. Although these devices have three terminals, they are not transistors. Two of the three pins carry power and ground to the detector. The other pin emits a logic 0 when it detects IR light. Here, a Panasonic type 4602 should be used.

The mounting of the detectors and the LEDs can be a little tricky and depends on the exact construction of your robot. You need to direct the LEDs in the forward direction and minimize the leakage from around the sides of the LEDs. You might consider using a bit of heat shrink sleeving, or cut small tubes from a soda straw, and cover it with electrical tape.

You'll also find that the position of the detectors is crucial. You should mount them as far apart as possible and tilt them slightly away from the LEDs (see **Figure 19**). To experiment with the positioning of the LEDs and detectors, use the program in **Listing 5**. When there is no object in front of the robot, you should not get an indication from the program. If you get false readings you probably have IR light leaking from the sides of the LEDs.

Once you have the detectors aligned properly, it is a simple matter to control the robot's motion based on the input from the detectors. **Listing 6** shows a simple control program that moves forward until it detects something. When the robot finds an obstacle, it stops and turns to avoid the object in its path.

MORE SOPHISTICATED

Once you have the simple control program under your belt, consider the program in **Listing 7**. This program is a bit more complex. Like the original program, this one moves forward until it detects an object. If the object is only visible on the right or left sensor, the robot turns in the opposite direction. If the object is straight ahead, the robot moves backwards and turns either right or left.

This program uses random num-

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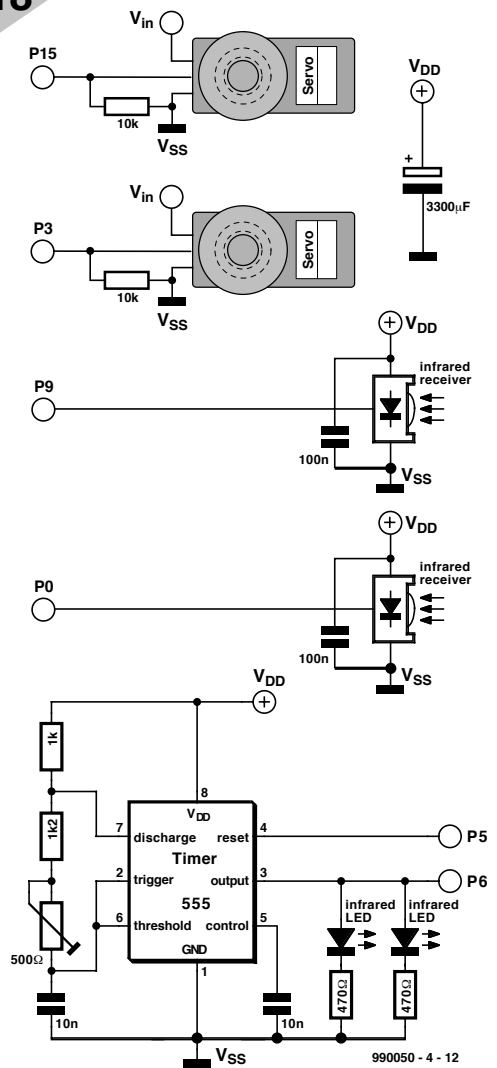


Figure 18. The complete circuit.

bers in several places. First, it uses a random number to select what direction to turn after it reverses in the face of an oncoming object. Also, any time the robot turns to the right or the left, it turns for a random amount of time.

RANDOM NUMBERS

The BASIC Stamp uses the RANDOM command to generate pseudo random numbers. This command takes a number in a variable and manipulates it to produce another number. Although the number is random, you will get the same random number each time you start with the same number.

In this case, random means randomly distributed in the mathematical sense of the word. If you want an unpredictable number, you'll have to make the original number (the seed) vary unpredictably. The robot program adds 1 to the *rnd* variable each time through the main loop. That means that when the program calls *RANDOM*

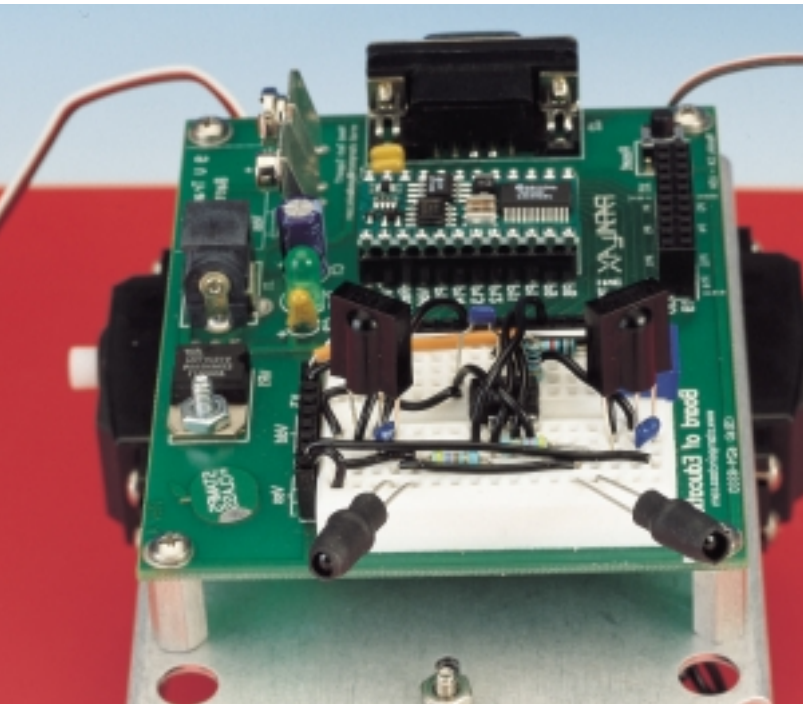


Figure 19. Suggested LED and sensor positioning.

you won't know what the seed value is and therefore won't be able to predict the result.

Because the random number is distributed over the entire possible range of numbers, you should use a *WORD* variable with *RANDOM*. You can then use an AND (&) or mod (//) operator to limit the value of the number. For example, if you want to limit the number to 15 (%1111 in binary), you could write:

```
RANDOM rnd
X=rnd & %111
```

This only works because 15 is one less than a power of 2. A more general-purpose way to limit the number is to use the mod operator (//). This operator

returns the remainder from integer division. So $11//3 = 2$ because 11/3 is 3 with a remainder of 2). To limit a random number to a maximum value of 100, you could write:

```
RANDOM rnd
X=rnd // 100
```

Armed with these simple equations, it is easy to generate random numbers for any range you need. Be careful not to restrict the *rnd* variable in the above example. Doing so will restrict the seed value for the next random number and therefore limit the range of future numbers the command will produce.

MATH EXPRESSIONS

Several spots in the robot program use expressions that have more than a single operator. These require special attention on the BASIC Stamp. When you write:

$5+2*3$

is the answer 21 or is the answer 11? In school, you learn that multiplication takes precedence over addition, so the answer is 11. However, the BASIC Stamp didn't go to the same school you did, so it evaluates math expressions from left to right with no regard to common rules of precedence. So to the BASIC Stamp, the correct answer is 21.

Luckily, the BASIC Stamp does allow you to use parenthesis to group expressions together. To get the above expression to evaluate as a mathematician expects, you could rewrite it as:

$5+(2*3)$

or:
 $2*3+5$

As an example, consider the portion of Listing 7 that causes the robot to turn left (just below the *left* label). Here, the

Listing 4. Calibrating the 555 timer

```
freq var word
high 5 ' osc on
start:
  count 6, 100, freq
  debug dec 5 freq*10, cr
  goto start
```

Listing 5. This Program aids in aligning the sensors

```
high 5 ' osc on
top:
  if in9=1 then nol eft
  debug "l eft"
  nol eft:
  debug 9 ' tab
  if in0=1 then nori ght
  debug "r ight"
  nori ght
  debug cr
  goto top
```

Listing 6. A Simple Motion Control Program

```
' Collision-avoiding robot - Williams
i var word ' loop counter
right_IR var in0 ' right IR eye
left_IR var in9 ' left IR eye
right_servo con 3 ' right servo not or
left_servo con 15 ' left servo not or
IR_out con 5 ' 38kHz enable
delay con 10 ' motor cycle time
center con 750
speed con 100

high IR_out ' turn on IR
pause 50

sense:
  if left_IR=0 or right_IR=0 then turn
```

```
' not hi ng i n si ght , so go f or war d
f or war d:
  for i=1 to del ay*2
    pul sout l eft _servo, cent er - speed
    pul sout r ight _servo, cent er +speed
    pause 20
  next
  goto sense

turn:
  pause 50
  for i=1 to del ay*5
    pul sout l eft _servo, cent er - speed
    pul sout r ight _servo, cent er - speed
    pause 20
  next
  goto sense
```

Listing 7. A Complex Motion Control Program

```
' Collision-avoiding robot - Williams
rnd var word          ' random quantity
i var word            ' loop counter
right_IR var in0     ' right IR eye
left_IR var in9      ' left IR eye
right_servo con 3    ' right servo motor
left_servo con 15    ' left servo motor
IR_out con 5        ' 38kHz enable
delay con 10        ' motor cycle time
center con 750
speed con 100

high IR_out          ' turn on IR
pause 50

sense:
  rnd=rnd+1          ' bump random number
  ' if obstacle in front of both eyes then
  ' go back and turn
  if left_IR=0 and right_IR=0 then back
  ' if obstacle to the left,
  ' move right or vice versa
  if left_IR=0 then right
  if right_IR=0 then left
  ' nothing in sight, so go forward
forward:

  for i=1 to delay*2
    pul sout left_servo, center-speed
    pul sout right_servo, center+speed
    pause 20
  next
  goto sense

back:
  pause 50
  for i=1 to delay*3
    pul sout left_servo, center+speed
    pul sout right_servo, center-speed
    pause 20
  next
  ' randomly turn to the right
  ' or the left after going
  ' backwards
  random rnd
  if rnd&1 then right

left:
  pause 50
  random rnd
  ' turn a random amount
  for i=1 to delay + (rnd&3*5)
    pul sout left_servo, center-speed
    pul sout right_servo, center-speed
    pause 20
  next
  goto sense

right:
  pause 50
  random rnd
  ' turn a random amount
  for i=1 to delay + (rnd&3*5)
    pul sout left_servo, center+speed
    pul sout right_servo, center+speed
    pause 20
  next

  goto sense
```

program generates a random number and then executes this step:

```
for i=1 to delay +
(rnd&3*5) ' turn a random
amount
```

This causes the entire loop to execute at least *delay* cycles. It also adds a random element from 0 to 15 (3 is the maximum random number, and $3*5$ is 15).

TROUBLESHOOTING

If your robot doesn't work correctly, here are a few things to check.

The problem you are most likely to have with this project is correctly positioning the LEDs and the sensors. Be sure to position the sensors far apart and shield the LEDs completely using heat shrink tubing or a soda straw. The shield should completely block the sides of the LEDs only allowing light to escape in the forward direction. Of course, the sensors and LEDs should be as close to the front of the robot as possible.

If the robot's motion seems jerky, be sure the 3300 μ F capacitor is in place. Without this capacitor, noise spikes from the motors can reset the BASIC Stamp, making the motion seem to

start and stop. If you suspect this is the case, try placing the following line at the start of either Listing 6 or Listing 7:

```
DEBUG "RESET", CR
```

Then, when the robot is connected to your PC, you should only see this line execute once. If you see it multiple times, the BASIC Stamp is resetting spuriously.

If the sensors don't seem to register objects, make sure they are wired correctly along with the LEDs. You might consider replacing the LEDs with a visible unit so you can see if the circuit is working (or better still, count the frequency with the BASIC Stamp or an oscilloscope).

If the robot detects objects very far away, you probably need to experiment with the location and direction of the LEDs and sensors. You might also consider using larger resistors with the LEDs (perhaps 2 k Ω) to reduce their output.

THE NEXT STEP

What else can you do with your BoE Bot? Using the information in last month's article, you could easily keep a log of objects detected and store it in EEPROM. You could use a switch to

turn off the robot's motors and dump the object log to the debug terminal. This information might be useful if you were programming the robot to run through a maze.

Speaking of mazes, you could add more IR sensors (and LEDs) to allow the robot to sense objects along its sides as well as straight ahead. Using this extra information could allow the robot to solve the maze more quickly — an important consideration in competition with other robots.

(990050-4)

Internet

<http://www.parallaxinc.com> — BASIC Stamp Manual Version 1.9, BASIC Stamp DOS and Windows Editor, program examples. International distribution sources.

<http://www.stampsinclass.com> — BoE documentation, Robotics curriculum, BoE-Bot *.dxf and *.dwg drawing formats, discussion group for educational uses of BASIC Stamp.

chucks@turbonet.com — creator of the BoE-Bot and author of this series. Technical assistance.

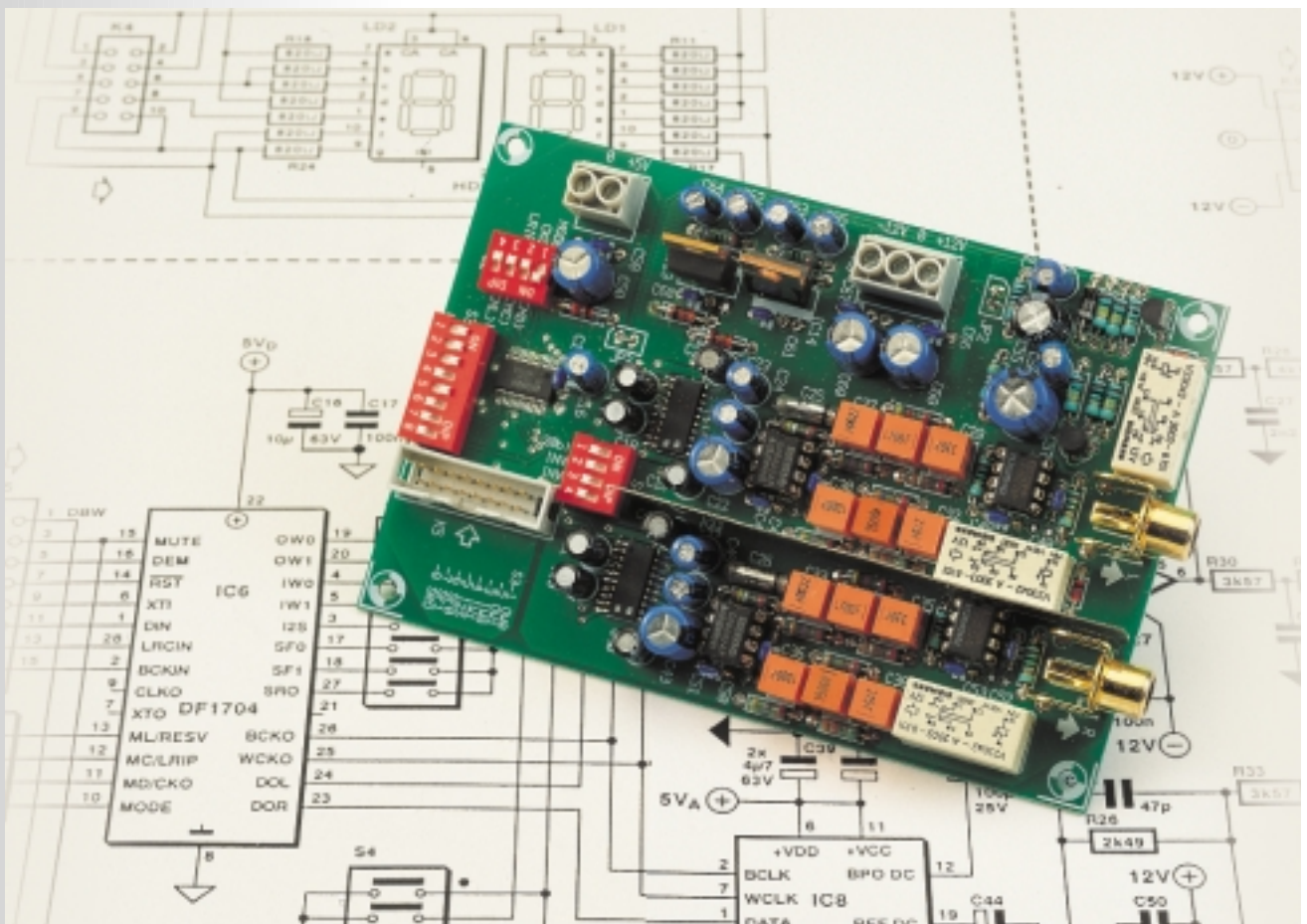
kgracey@parallaxinc.com — co-author of this article. Technical assistance and questions about the educational program.

<http://www.milinst.demon.co.uk> — UK distributor of Parallax BASIC Stamp.

audio DAC 2000

Part 2

digital filter and DACs



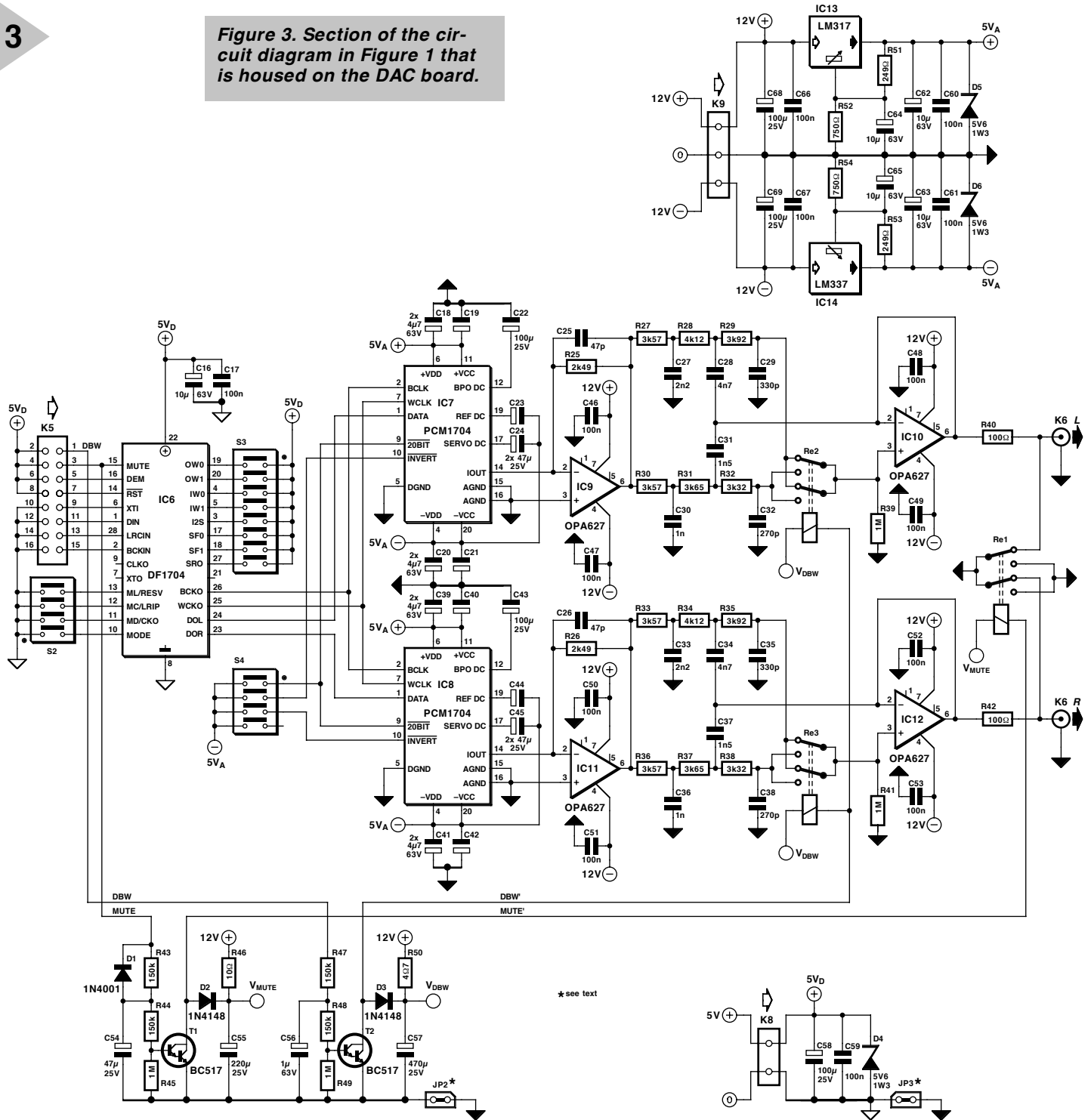
Last month's Part 1 of this article dealt primarily with a general description of the new digital-to-analogue converter (DAC) 'Audio DAC 2000' and details of the input section. In this second and penultimate part the remainder of the circuit, more especially the digital interpolation filter and the actual DACs, is described.

INTRODUCTION

It is clear from the description of the overall design in last month's installment that the Audio DAC 2000 can be divided into four distinct sections: the power supply, the receiver and display driver, the LED display, and the DACs. These sections are identified in the circuit diagram in Figure 1 by dashed lines.

The DAC section includes the digital interpolation filter, the output filter, the various relays, and the DACs. For clarity's sake, these circuits are reproduced in Figure 3.

Figure 3. Section of the circuit diagram in Figure 1 that is housed on the DAC board.



DIGITAL FILTER

The integrated digital interpolation filter, IC₆ (Burr-Brown Type DF1704) is a multipurpose device, which

- ◆ is suitable for sampling rates of 32–96 kHz;
- ◆ can be used as a notch filter providing 115 dB attenuation;
- ◆ has an input suitable for 16/20/24 bits;
- ◆ has an output of 16/18/20/24 bits;
- ◆ provides automatic sensing of the ratios of the clock frequencies (system clock up to $768F_s$ – where F_s is

the sampling rate);

- ◆ can be used as slow roll-off filter;
- ◆ provides a soft mute;
- ◆ provides digital emphasis;
- ◆ has a digital attenuator.

Various input and output formats can be set via hardware or software. In the Audio DAC, setting via hardware has been opted for, since in its standard application the unit will invariably have a fixed place in the audio system. This means that the various DIP switches normally need to be set only once. However, as in the receiver,

there is space for experimentation, but note that the measurements given in this article refer to default settings of the DF1704.

The only difference between control via software and hardware is that with the former a digital attenuator can be used independently, providing 256 steps of 0.5 dB each both to the left and to the right.

One of the more important settings is the correct tuning to the format set at the receiver, that is, I²S.

With reference to **Table 1**, the various possible settings are detailed below.

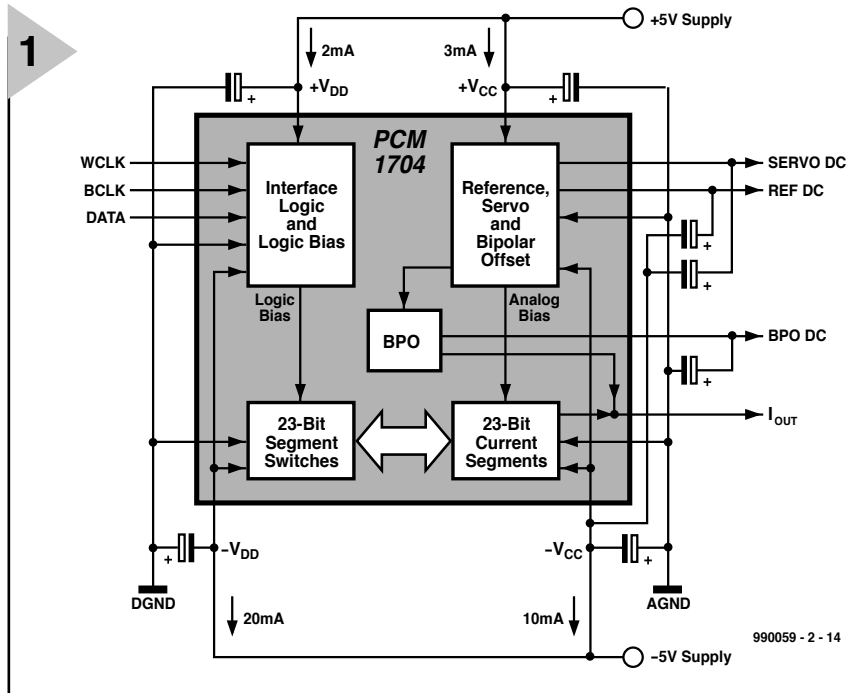


Figure 4. Internal block diagram of the integrated digital-to-analogue converter Type PCM1704.

DIP switch S2 is a quadruple device since pins 11–13 have dual functions. When mode pin 10 is high, these pins form a 3-wire software-control port and are then called MD, MC, and ML, respectively. These names are shown in brackets adjacent to the pin locations on the board. At the other side of the location the hardware mode functions are shown, just as the levels adjacent to ON and OFF. In the present application, this arrangement is not used, but S2 may, if desired, be replaced by an 8-pin board connector (to accept flatable) to, say, link the digital filter to a microcontroller.

Pins 11–13 and mode pin 10 have internal pull-up resistors, so that a closed DIP switch (ON) results in a low level at S2. This means that for the hardware mode, section 1 of S2 must be closed (Mode=low). Pin 13 (RESV – section 4 of S2) is then not used.

Pin 12 (LRIP – section 3 of S2) determines at which level of the L/R clock the data must be considered as belonging to the lefthand channel or to the righthand channel. When section 3 of S2 is off, LRIP is high, whereupon it is assumed that when clock signal LRCIN is high, the data are intended for a lefthand sample. In the I²S mode, LRIP is not used.

Pin 11 (CKO – section 2 of S2) determines whether the CLKO output on pin 9 is equal to the clock at XTI or XTI/2. This pin has no specific function in the Audio DAC and is therefore not used.

It is possible to connect a crystal oscillator to pins XTI and XT0, but this is rather pointless since XTI is provided

by the high-precision master clock (MCK) in IC₁. XTI may have

a number of values: 256F_s, 384F_s, 512F_s, and 768F_s. Its maximum value at 512F_s and a sampling rate of 96 kHz is 49.152 MHz, but the maximum possible frequency of a crystal oscillator is 24.576 MHz. In fact, at 256F_s and a sampling rate of 96 kHz, the manufacturer advises against the use of a crystal oscillator and suggests the use of an external source for XTI. This is the reason that there is no space reserved for a crystal oscillator on the board.

Bit clock BCKIN may be 32F_s, 48F_s, or 64F_s, while LRCIN is, of course, always equal to F_s. The input formats are self-evident and should be compared with the output format of IC₁. When both a CD player and a DVD player with a 24 bit/96 kHz are to be connected to the Audio DAC, the mode should always be 24 bit, which fixes the position of the MSB.

The various input formats are determined by inputs IW0 and IW1, and I²S, that is, sections 3, 4, and 5, of S3 respectively. For clarity's sake, the function of the sections of S3 is shown in tabular form on the board adjacent to K5.

The output format is determined by inputs OW0 and OW1, that is, sections 1 and 2 of S2, XTI, and the 8-times oversampling. The format is always complement 2, MSB first and right justified. DOR contains samples for the righthand channel only, and DOL for the lefthand channel only. The inputs sense whether the data at the output contains 16, 18, 20, or 24 bits per sample.

Output word clock WCKO is, of

course, always 8F_s, irrespective of the system clock. Output bit clock BCKO is determined by the system clock and is 256F_s when XTI is 256F_s or 512F_s, or 192F_s when XTI is 384F_s or 768F_s. In the present application, BCKO is always equal to the master clock (MCK) of IC₁. The outputs are set to 24 bits by setting sections 1 and 2 of S3 to ON.

The slow rolloff filter function ensures reduced ringing in the pass band, but produces more aliasing products. The manufacturer recommends that the filter is not used above 96 kHz. Input SRO (pin 27) determines whether the filter is used; its level is set with section 8 of S3, which is normally OFF.

When the deemphasis control is actuated by the receiver, IC₁, the two remaining inputs, SF0 and SF1 (pin 17 and 18) respectively determine for which sampling rate the deemphasis is valid. This is normally 44.1 kHz, on the assumption that deemphasis is usually required for certain CDs only. All inputs that are controlled via S3 have internal pull-down resistors, which is the reason that S3 is linked to the +5 V line.

Soft mute control input MUTE is switched directly by error output ERF of IC₁ (which is inverted by the GAL). When the level at MUTE is low, the digital filter is in the mute position – the output relay is then deactivated.

The DF1704 has an internal power-on reset as well as a reset input. The internal reset lasts for 1024 system clock periods after the supply voltage has been switched on; all outputs are then low. This is true also after a low-to-high change at the RST pin.

DIGITAL - TO - ANALOGUE CONVERTERS (DAC)

The data from the digital filter is applied to two high-quality digital-to-analogue converters (DACs), IC7 and IC8, whose internal block schematic is shown in Figure 4.

- These devices
- ◆ are suitable for sampling rates of 16–96 kHz;
- ◆ provide 8× oversampling;
- ◆ provide a choice of 20 or 24 bit data;
- ◆ have a dynamic range of 112 dB;
- ◆ provide a signal-to-noise ratio of 120 dB;
- ◆ have a glitch-free output;
- ◆ invert the data.

In contrast to oversampling data converters using, for instance, the delta-sigma architecture, the Burr-Brown devices use a different solution to the bipolar zero transition problem.

Delta-sigma converters have an inherent poor signal-to-noise ratio which makes the use of noise-shaping

circuits to improve that ratio within the audio band essential. Unfortunately, this creates an appreciable increase in noise outside the audio band. If the outputs of the DACs were not filtered correctly, an overall deterioration of performance would ensue.

The PCM1704 uses the traditional DAC structure ($R-2R$) in such a manner as to provide excellent low-frequency performance and yet not lose the outstanding properties of this structure: excellent full-scale performance; high signal-to-noise ratio, and simplicity of design. Burr-Brown designers term this architecture sign-magnitude. Briefly, this means that two 23-bit DACs are combined in a complementary setup which results in a highly linear output so that a 24-bit resolution is assured at the zero crossings.

The two DACs have a common reference and $R-2R$ ladder network. The network uses dual-balanced current segments that ensure correct performance in all kinds of circumstance. Moreover, the discrete bits of the DACs are alternated so that, after laser trimming of the resistors, the DACs are identical for all purposes required by the present application.

The DAC is timed so that only the 24 bit before word clock WCLK goes low causes the data in the serial input register to be transferred to the parallel DAC register. If pin 9 (20-bit mode) is active (linked to the -5 V line), the foregoing also applies to the last 20 bit. Any other bits present will not be accepted, so that the data applied to the DAC must correspond to the mode to which the DAC is set. If this is not so, the data will become mutilated or the level is much too low.

The maximum bit clock is specified as 25 MHz, which is related to the $8\times$ oversampling, a 32-bit frame for the data, and the maximum sampling rate, ($8\times 32\times 96$ kHz = 24.576 MHz). The data can be inverted by linking pin 10 (INVERT) of the PCM1704 to the negative supply line.

Pins 9 and 10 have internal pull-up resistors to digital ground (DGND) and are switched with DIP switch S4. Section 4 of this switch is not connected, so that a 3-section switch would suffice. However, 4-section switches are much more readily available.

The ICs are powered by a symmetrical ± 5 V supply. This is derived via

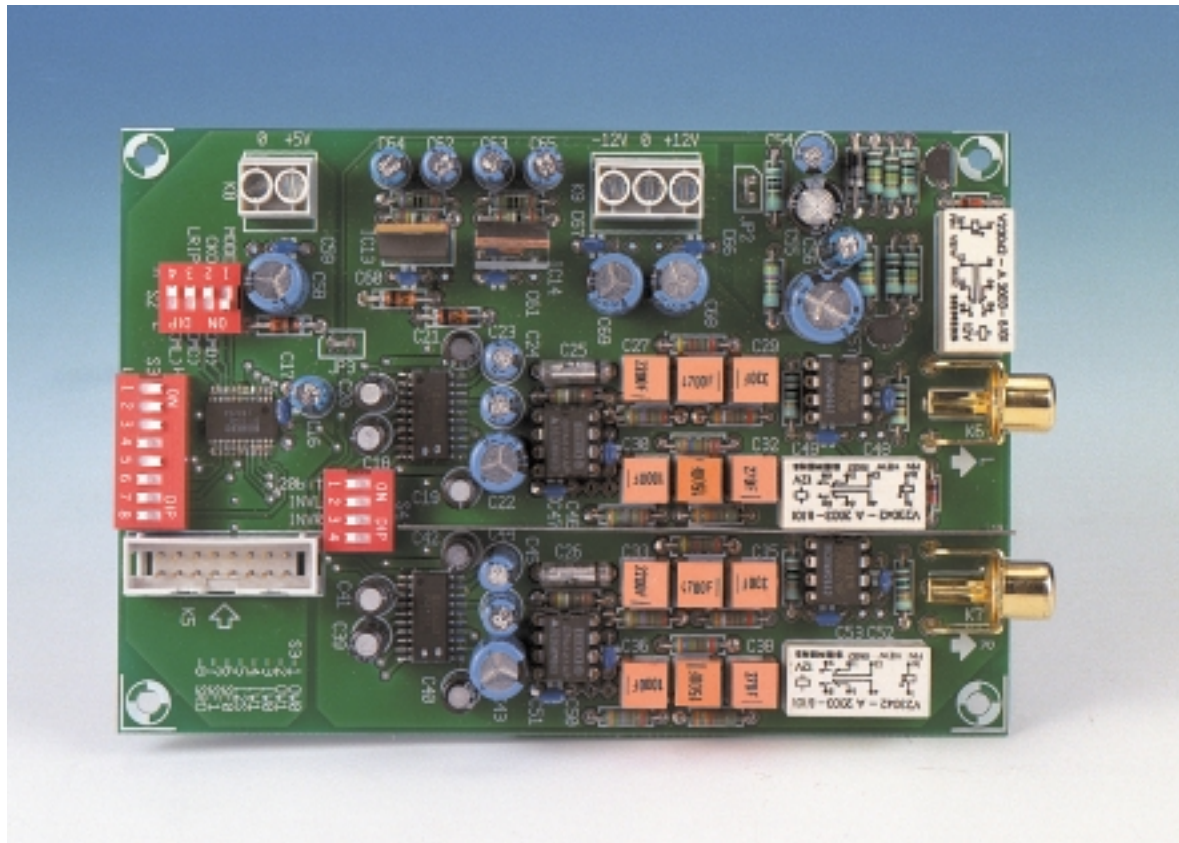
regulators IC13 and IC14 from the analogue ± 12 V line and used only for the DACs. Potential dividers R51-R52 and R53-R54 set the regulators to exactly 5 V. Since there is some residual ripple on the ± 12 V line (which does not affect the op amps), capacitors C64 and C65 provide additional ripple suppression. Zener diodes D5 and D6 protect the DACs against errors such as wrong resistors or defect regulators.

The manufacturer's specification stipulates that the supply lines to the digital and analogue sections must be linked as a single line to an analogue supply. There is no advantage in separating the digital and analogue supplies, but it is essential that they are decoupled to the ground plane as close to the relevant IC pins as possible. This, and that fact that internal voltages SERVO DC, REF DC, and BPO DC

- ◆ a high slew rate to be able to follow the DAC accurately;
- ◆ excellent linearity.

In the Audio DAC the OPA627 is used, which has a bias current of just 10 pA, a slew rate of 55 V μ s $^{-1}$, and a distortion of only 3×10^{-7} (0.00003%).

The inherent input offset of the OPA627 ≤ 0.5 V, which results in overall offset voltages at the output of the prototype ≤ 10 mV and ≤ 20 mV respectively. This is low enough to prevent the use of an output capacitor, particularly since this would inevitably adversely affect the quality of the output signal. It is assumed in any case that there is invariably a coupling capacitor between preamplifier and output amplifier. If nevertheless an output capacitor is desired, a metalized polypropylene (MKP, Siemens)



must be decoupled in a like manner, is the reason that the ICs are surrounded by decoupling capacitors.

The current output of the DAC is specified as 1.2 mA/200 ns (the full range is ± 1.2 mA), which demands certain requirements from the I/U converter as described in the following section.

I/U CONVERTER

Op amps IC9 and IC11 on which the current-to-voltage converters are based must have:

- ◆ a very low bias current to obviate additional offset;

type of about 10 μ F should be used. Resistors R40 and R42 may then be replaced by an external RC network. It should be borne in mind that a 10 μ F MKP capacitor is fairly large.

The one disadvantage of the OPA627 is its low-frequency noise, which in any FET op amp is fairly high. Even so, the specified values of 20 nV/ \sqrt Hz at 10 Hz and 5.6 nV/ \sqrt Hz at 1 kHz are very good indeed.

Since the value of R25 and R26 is retained at 2.49 k Ω , the actual output voltage of 2.1 V_{rms} is slightly higher than the standard 2 V_{rms}.

Capacitors C25 and C26 are needed to filter r.f. components from the signal.

Because of quality considerations, these capacitors should be (axial) polystyrene types.

OUTPUT FILTER

Although the digital interpolation filter attenuates most aliasing frequencies by at least 115 dB, an analogue low-pass filter is still required to remove any residual components plus any spurious products caused by jitter of the system clock.

In fact there are two output filters, which are selected by a relay. The first, R27–R29–C27–C29 is a 3rd order Butterworth type for the more usual sampling rates of 32 kHz, 44.1 kHz, and 48 kHz. The cut-off frequency of this filter is about 27 kHz.

The second filter, R33–R35–C30–C32, is a 3rd order Bessel type for use with sampling rates of 88.2 kHz and 96 kHz. Its cut-off frequency is about 43.7 kHz.

The amplitude characteristics of the two filters are virtually identical over the audio range.

The filters are 3rd order types since the first passive section of this type of filter provides much better r.f. suppression than that of a 2nd order filter. In the latter, r.f. suppression depends on the ratio of the impedance of the filter network and the output impedance of the relevant buffer op amp.

Switching between the two filters is effected in each channel by a relay with parallel-connected double-pole change-over contacts (Re2 and Re3 respectively). The relays are 12 V types that are energized directly by the analogue + 12 V line. The supply to the relays is separately filtered by R57–C57. The board layout is designed so that the return currents are separate up to the 0 terminal.

The relays switch the outputs of the two filters to the input of buffer IC10 (one channel) or IC12 (other channel). Although the non-selected filter loads the relevant I/U converter and output buffer, it does not affect the response of the selected filter.

The relays are energized indirectly by signal DBW from the GAL on the receiver board. Since this signal is a TTL signal (5 V) and the relays need 12 V, voltage conversion is needed, which is provided by darlington transistor T2. The base current of this transistor is low enough not to load the GAL to an unacceptable extent.

The only load is presented by potential divider R47–R49, which is decoupled by capacitor C56. Resistor R49 ensures that T2 is switched off at any residual voltage, which results in a much better defined switching signal for the transistor.

Diode D3 is a freewheeling diode that provides a leakage path for the energy in the circuit when the relay is

PIN NAME	PIN NUMBER	DESCRIPTION																												
RESV	13	Reserved, Not Used																												
LRIP	12	LRCIN Polarity LRIP = H: LRCIN= H = Left Channel, LRCIN= L = Right Channel LRIP = L: LRCIN= L = Left Channel, LRCIN = H = Right Channel																												
CKO	11	CLKO Output Frequency CKO = H: CLKO Frequency = XT1/2 CKO = L: CLKO Frequency = XT1																												
MUTE	15	Soft Mute Control: H = Mute Off, L = Mute On																												
I ² S IWO IW1	3 4 5	Input Data Format Controls <table border="1"> <thead> <tr> <th>I²S</th> <th>IW1</th> <th>IWO</th> <th>INPUT FORMAT</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>L</td> <td>16-Bit, Standard, MSB-First, Right-Justified</td> </tr> <tr> <td>L</td> <td>L</td> <td>H</td> <td>20-Bit, Standard, MSB-First, Right-Justified</td> </tr> <tr> <td>L</td> <td>H</td> <td>L</td> <td>24-Bit, Standard, MSB-First, Right-Justified</td> </tr> <tr> <td>L</td> <td>H</td> <td>H</td> <td>24-Bit, MSB-First, Left-Justified</td> </tr> <tr> <td>H</td> <td>L</td> <td>L</td> <td>16-Bit, I²S</td> </tr> <tr> <td>H</td> <td>L</td> <td>H</td> <td>24-Bit, I²S</td> </tr> </tbody> </table>	I ² S	IW1	IWO	INPUT FORMAT	L	L	L	16-Bit, Standard, MSB-First, Right-Justified	L	L	H	20-Bit, Standard, MSB-First, Right-Justified	L	H	L	24-Bit, Standard, MSB-First, Right-Justified	L	H	H	24-Bit, MSB-First, Left-Justified	H	L	L	16-Bit, I ² S	H	L	H	24-Bit, I ² S
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SRO	27	Digital Filter Roll-Off: H = Slow, L = Sharp																												
OWO OW1	19 20	Output Data Word Length Controls <table border="1"> <thead> <tr> <th>OW1</th> <th>OWO</th> <th>OUTPUT FORMAT</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>16-Bit, MSB-First</td> </tr> <tr> <td>L</td> <td>H</td> <td>18-Bit, MSB-First</td> </tr> <tr> <td>H</td> <td>L</td> <td>20-Bit, MSB-First</td> </tr> <tr> <td>H</td> <td>H</td> <td>24-Bit, MSB-First</td> </tr> </tbody> </table>	OW1	OWO	OUTPUT FORMAT	L	L	16-Bit, MSB-First	L	H	18-Bit, MSB-First	H	L	20-Bit, MSB-First	H	H	24-Bit, MSB-First													
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SF0 SF1	17 18	Sample Rate Selection for the Digital De-Emphasis Control <table border="1"> <thead> <tr> <th>SF1</th> <th>SF0</th> <th>SAMPLING RATE</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>44.1kHz</td> </tr> <tr> <td>L</td> <td>H</td> <td>Reserved, Not Used</td> </tr> <tr> <td>H</td> <td>L</td> <td>48kHz</td> </tr> <tr> <td>H</td> <td>H</td> <td>32kHz</td> </tr> </tbody> </table>	SF1	SF0	SAMPLING RATE	L	L	44.1kHz	L	H	Reserved, Not Used	H	L	48kHz	H	H	32kHz													
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H	H	32kHz																												
DEM	16	Digital De-Emphasis: H = On, L = Off																												

990059 - T1

Table 1. Hardware mode controls of the digital interpolation filter.

deenergized.

Note that T2 switches both relays, since the coils of them are in parallel.

MUTE RELAY

The mute relay, Re1, at the output of the DAC circuit, obviates switch-on clicks and other irregular pulses on the supply lines. It is controlled by a signal from IC1 and switches the digital filter to the mute state when the receiver detects an error.

Since the impedance of both outputs is low, one relay suffices without any risk of deterioration of the channel separation at high frequencies. If there is a drawback, it is that the relay is not fast enough at switch-off, which may cause a loud click.

Like the output filters, the relay is switched by a darlington transistor, T1. When the relay is not energized, the outputs are in the mute state.

When the supply voltage is switched on, or when an error has been remedied, the relay is energized gradually to ensure that all stages have been reset correctly before the relay operates. The delay time is determined by network R43–R44–C54, the time constant of which is 3 seconds in case of a switch-on, but rather shorter after an

error has been remedied.

Capacitor C1 is discharged via diode D1 so that the relay changes state immediately upon the receiver detecting an error, such as the absence of an input signal.

Network R46–C55 decouples the 12 V supply lines to ensure that the switching of the relay contacts does not create pulses on these lines.

Diode D2 is a freewheeling diode that provides a leakage path for the energy in the circuit when the relay is deenergized.

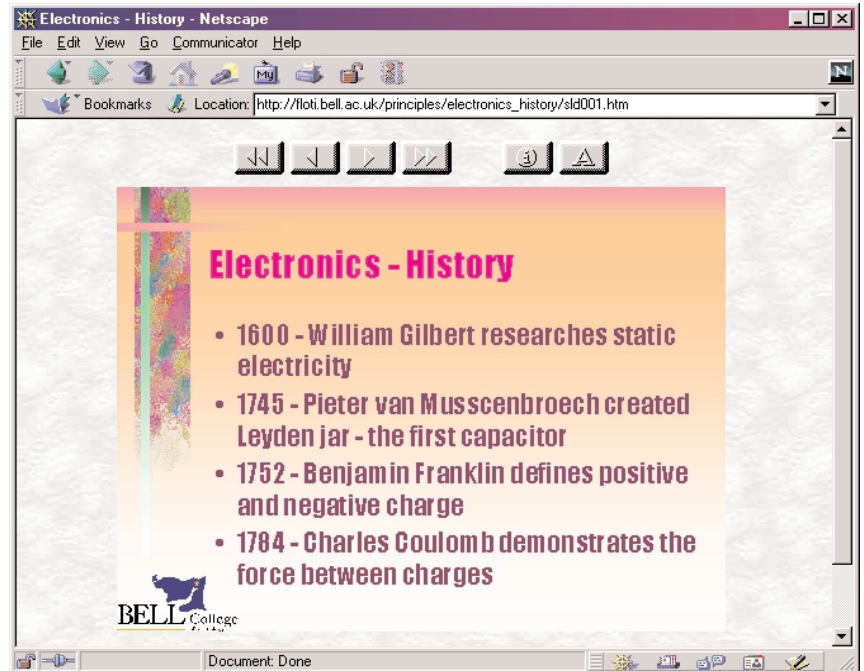
[990059]

The third and last part of this article will deal primarily with the printed circuit boards, the construction, and the test results.

history

looking back... via the Internet

On the verge of the new Millennium, it seems appropriate to reflect and ruminate on this century's tremendous developments in electronics. So what better archive to browse than the largest of them all, the Internet?



If you employ the Internet for a bit of research into the history of electronics, you should be prepared to spend quite some time. Although there are plenty of web sites covering the history of a specific subject, that does not apply to a more general field like electronics. None the less, we came across a respectable number of web addresses with information covering a large part of the (admittedly wide) field called electronics.

A global overview of most important discoveries in the field is available in the form of a short slide show compiled and hosted by **Bill Steele** at (http://floti.bell.ac.uk/principles/electronics_history/index.htm).

A nice looking overview of the people behind major inventions may be found on the pages called 'a **Thumbnail History of Electronics**' by Professor Taylor: (<http://www.ee.umd.edu/~taylor/Electrons.htm>). Prof. Taylor is also a good source for the history of optics.

The history of one of the greatest inventions in electronics, and indeed of all times, may be browsed on the **Lucent Technologies** web site at (<http://www.lucent.com/ideas/heritage/transistor/>).

If you are looking for a concise but

clear chronological overview on the developments in **film, video and audio recording**, we'd recommend visiting the web site at <http://www.soundsite.com/history/history.html>.

Now that we seem to have digressed to specific subjects, we may just as well mention a fine web site for the history of **solar energy** developments: <http://hyperion.advanced.org/17658/sol/solhistoryht.html>.

The history of **radio astronomy** is also extensively covered by various sites. A 'nutshell' version, however, may be found at <http://www.win.net/~radiosky/ra01.html>.

A far-reaching historic overview of developments in **telecommunications** has been compiled by a group of German students at Esslingen Polytechnic (FHTE). Take a look at (<http://www-stall.rz.fht-esslingen.de/telehistory/indexhaupt.html>).

A rather special site we came across should not be left unmentioned as it fits very well in this overview. The pages called 'A **Philatelic History of Radio and Electronics**' found at (<http://www.qsl.net/kf4oad/stamps.htm>) present an overview of a variety of stamps depicting great achievements

in electronics, and inventors, as collected by radio amateur KF4OAD.

Two of this century's greatest inventions are radio and television. 'Surfing the Aether' presents a fine and comprehensive story about developments in radio communications at (www.northwinds.net/bchris/index.htm).

In eleven time periods, these pages examine the greatest achievements and milestones. In case you are only interested in the main facts and dates, you may find the 'History of Radio' pages at (www.vwlowen.demon.co.uk/radio/radhist.htm) more convenient.

The development of the medium we call television is covered by EBU's Jean-Jacques Peters in 'A History of Television' at (http://www.ebu.ch/dvb/dob_articles/dvb_tv-history.htm).

Having visited (and hopefully enjoyed) the web sites mentioned in this article, it would seem fitting to get to know a bit more about the history of the Internet itself. All right then here is our last Internet link for this century and Millennium. It is **Hobbes' Internet Timeline v4.2** at (<http://info.isoc.org/guest/zakon/Internet/History/HIT.html>).

(995094-1)

PCM1704

Integrated circuits
Special Function, AF



DATASHEET 1 2 / 9 9

SPECIFICATIONS

All specifications at $T_A = +25^\circ\text{C}$, $\pm V_{CC} = \pm V_{DD} = \pm 5\text{V}$, $f_S = 768\text{kHz}$ (96kHz \times 8), and 24-bit data, unless otherwise noted.

PARAMETER	CONDITIONS	PCM1704U			UNITS
		MIN	TYP	MAX	
RESOLUTION			24		Bits
DATA FORMAT					
Audio Data Interface Format		20-, 24-Bit, MSB-First			
Audio Data Code		Binary Two's Complement			
Sampling Frequency (f_S)		16		96	kHz
Input Clock Frequency				25	MHz
DIGITAL INPUT/OUTPUT					
Input Logic Level:					
$V_{IH}^{(1)}$		+ 2.0		± 5.0	V
$V_{IL}^{(1)}$		0		+ 0.8	V
$V_{IH}^{(2)}$		-3.0		0	V
$V_{IL}^{(2)}$		-5.0		-4.2	V
Input Logic Current:					
$I_{IH}^{(1)}$	$V_{IH} = +V_{DD}$			± 10	μA
$I_{IL}^{(1)}$	$V_{IL} = 0\text{V}$			± 10	μA
$I_{IH}^{(2)}$	$V_{IH} = 0\text{V}$			± 10	μA
$I_{IL}^{(2)}$	$V_{IL} = -V_{DD}$			-100	μA
DYNAMIC PERFORMANCE⁽³⁾					
THD+ N at $V_O = 0\text{dB}$	PCM1704U		0.0025	0.0030	%
	PCM1704U-J		0.0015	0.0025	%
	PCM1704U-K		0.0008	0.0015	%
THD+ N at $V_O = -20\text{dB}$	PCM1704U		0.008	0.020	%
	PCM1704U-J		0.007	0.015	%
	PCM1704U-K		0.006	0.01	%
Dynamic Range	EIAJ, A-weighted				
	PCM1704U, -U-J	102	110		dB
	PCM1704U-K	106	112		dB
Signal-to-Noise Ratio	EIAJ, A-weighted	112	120		dB
Low Level Linearity	$f = 1002\text{Hz}$ at -90dB		± 0.5		dB
DC ACCURACY					
Gain Error			± 1.0	± 3.0	% of FSR

PCM1704

Integrated circuits
Special Function, AF



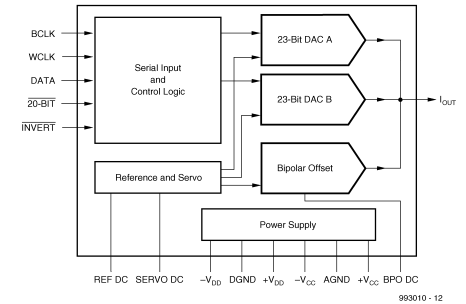
DATASHEET 1 2 / 9 9

PCM1704

Soundplus™ 24-Bit, 96 kHz BICMOS Sign-Magnitude Digital-to-Analog Converter

Manufacturer

Burr-Brown,
PO Box 1140,
Tucson, AZ 85734, U.S.A.
Tel. (520) 746-1111, fax (520) 889-1510.
Internet: <http://www.burr-brown.com/>



PCM1704 Block Diagram

Features

- Sampling frequency (f_S): 16 kHz to 96 kHz
- 8x oversampling at 96 kHz
- Input audio data word: 20-, 24-bit
- High performance:
 - dynamic range: K grade = 112dB typ
 - SNR: 120dB typ
 - THD+ N: K grade = 0.0008% typ
- Fast current output: $\pm 1.2\text{mA}/200\text{ns}$
- Glitch-free output
- Pin-programmable data inversion
- Power supply: $\pm 5\text{V}$
- Small 20-lead so package

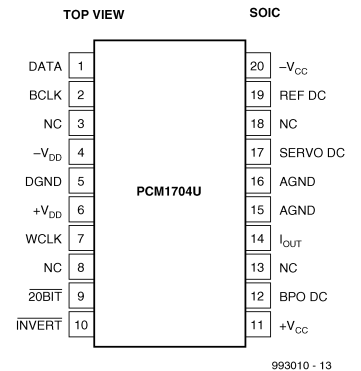
Application Example

Audio DAC2000,
Elektor Electronics November 1999 – January 2000

Description

The PCM1704 is a precision, 24-bit digital-to-analog converter with exceptionally high dynamic performance. The ultra-low distortion and excellent low-level signal performance makes the PCM1704 an ideal candidate for high-end consumer and professional audio applications. When used with a digital interpolation filter, the PCM1704 supports 8x oversampling at 96kHz. The PCM1704 incorporates a BICMOS sign-magnitude architecture that eliminates glitches and other nonlinearities around bipolar zero. The PCM1704 is precision laser-trimmed at the factory to minimize differential linearity and gain errors.

In addition to high-performance audio systems, the PCM1704 is well suited to waveform synthesis applications requiring very low distortion and noise.



Pin configuration, top view, SOIC

Audio Data Interface

Basic Operation

The audio interface of the PCM1704 accepts TTL-compatible input levels. The data format at the DATA input of the PCM1704 is Binary Two's Complement, with the most significant bit (MSB) being first in the serial input bit stream. Table 1 shows the relationship between the audio input data and DAC output for the PCM1704. Any number of bits can precede the 24



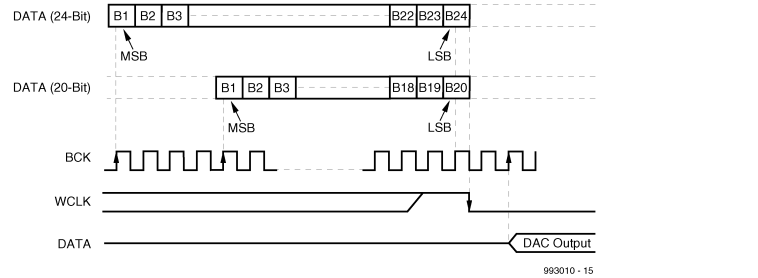


Figure 1. Audio input data format

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bits to be loaded since only the last 24 bits will be transferred to the parallel DAC register after WCLK (pin 7) has gone LOW (logic 0).

BINARY TWO'S COMPLEMENT INPUT DATA (Hex)	DAC OUTPUT
7FFFFF	+ Full Scale
000000	Bipolar Zero
FFFFFF	Bipolar Zero - 1 LSB
800000	- Full Scale

Table I. Digital Input/DAC Output Relationships.

Audio data is supplied to the DATA (pin 1) input. The bit clock is used to shift data into the PCM1704 and is supplied to BCLK (pin 2). All DAC serial input data bits are latched into the serial input register on the rising edge of BCLK. The serial-to-parallel data transfer to the DAC occurs on the falling edge of WCLK.

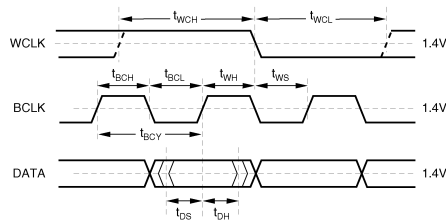


Figure 2. Audio input data timing

BCLK Pulse Cycle Time	t _{BCY}	40ns (min)
BCLK Pulse Width HIGH	t _{BCH}	14ns (min)
BCLK Pulse Width LOW	t _{BCL}	14ns (min)
BCLK Rising Edge to WCLK Falling Edge	t _{WH}	10ns (min)
WCLK Falling Edge to BCLK Rising Edge	t _{WS}	10ns (min)
WCLK Pulse Width HIGH	t _{WCH}	> t _{BCY}
WCLK Pulse Width LOW	t _{WCL}	> t _{BCY}
DATA Set-up Time	t _{DS}	10ns (min)
DATA Hold Time	t _{DH}	10ns (min)

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The change in the output of the DAC occurs at the rising edge of the 2nd BCLK after the falling edge of WCLK. Figure 1 shows the audio data input format. Figure 2 shows the input timing relationships.

Maximum Bit Clock (BCLK) Rate

The maximum BCLK rate is specified as 25MHz. This is derived from the 8x oversampling of the PCM1704. Given a 96kHz sampling rate, an 8x oversampling input and a 32-bit frame length, we get: 96kHz x 8 x 32 = 24.576MHz

'Stopped Clock' Operation

The PCM1704 is normally operated with a continuous BCLK input. If BCLK is stopped between input data words, the last 24 bits shifted in are not actually transferred from the serial register to the parallel DAC register until WCLK goes LOW. WCLK must remain LOW until after the first BCLK cycle of the next data word to insure proper DAC operation. The specified setup and hold times for DATA and WCLK must be observed.

PARAMETER	CONDITIONS	PCM1704U			UNITS
		MIN	TYP	MAX	
Bipolar Zero Error			±0.5	±1.0	% of FSR
Gain Drift	0°C to 70°C		±25		ppm of FSR/°C
Bipolar Zero Error Drift	0°C to 70°C		±5		ppm of FSR/°C
ANALOG OUTPUT					
Output Range			±1.2		mA
Output Impedance			1.0		kΩ
Settling Time	±0.0003% of FSR, ±1.2mA Step		200		ns
POWER SUPPLY REQUIREMENTS					
Voltage Range: +V _{CC} = +V _{DD}		+4.75	+5.0	+5.25	VDC
Voltage Range: -V _{CC} = -V _{DD}		-4.75	-5.0	-5.25	VDC
Combined Supply Current: +I _{CC}	+V _{CC} = +V _{DD} = +5.0V		5	8	mA
Combined Supply Current: -I _{CC}	-V _{CC} = -V _{DD} = -5.0V		30	45	mA
TEMPERATURE RANGE					
Operation		-25		+85	°C
Storage		-55		+125	°C
NOTES: (1) BCLK, WCLK, DATA. (2) 20BIT, INVERT. (3) Dynamic performance data is tested with 5534 I/V amp with 7.5kΩ feedback resistor. THD+ N data is tested by Shibasoku 725C with 30kHz external LPF, 400Hz HPF, average mode. Input signal frequency = 1.1kHz.					

Data format control

Data format is controlled by two pins on the PCM1704—the 20BIT and INVERT inputs. Their functions are described in the following paragraphs and tables.

Input Word Length

20BIT (pin 9) is used to select the input data length. Table II shows the available selections. Pin 9 is internally pulled up to DGND and therefore, defaults to 24-bit data.

Input Data Inversion

INVERT (pin 10) is used to select the phase of the input data presented to the DAC. Table III shows the

20BIT (Pin 9)	DATA WORD LENGTH
20BIT = H (DGND)	24-Bit Data Word
20BIT = L (-VDD)	20-Bit Data Word

Table II. Input Word Length Selection.

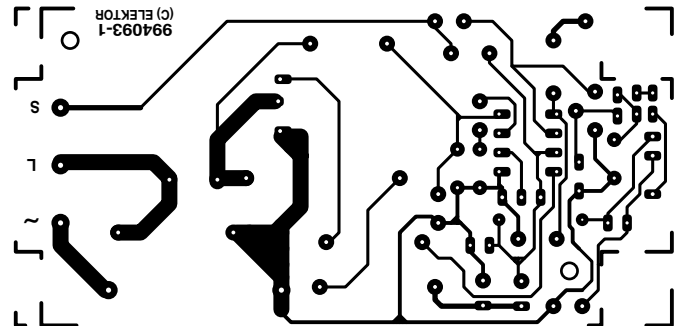
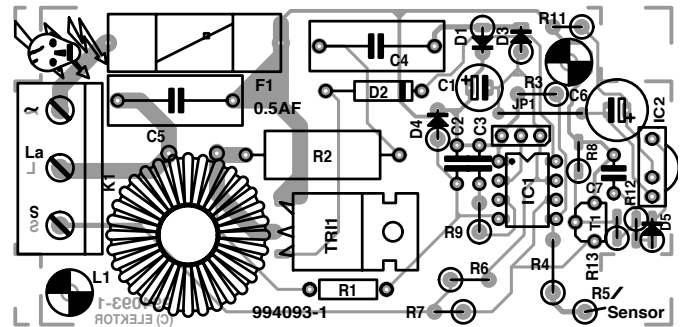
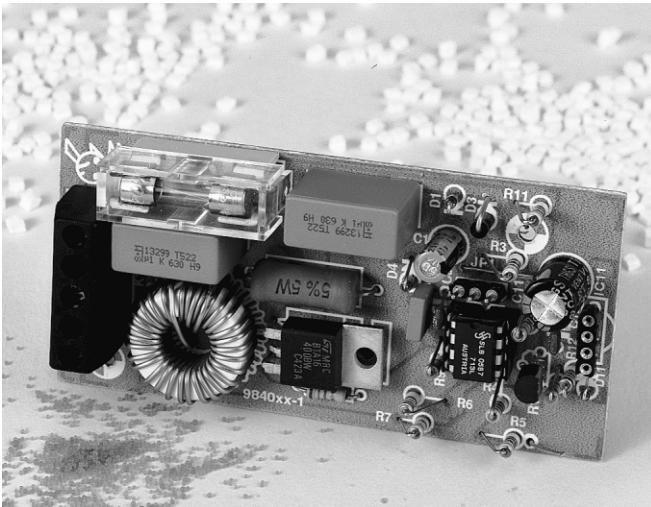
two options. Pin 10 is internally pulled up to DGND, and therefore defaults to normal, or non-inverting data.

INVERT (Pin 10)	PHASE
INVERT = H (DGND)	Normal (non-inverted)
INVERT = L (-VDD)	Inverted

Table III. Input Data Phase Selection.

touch dimmer

001

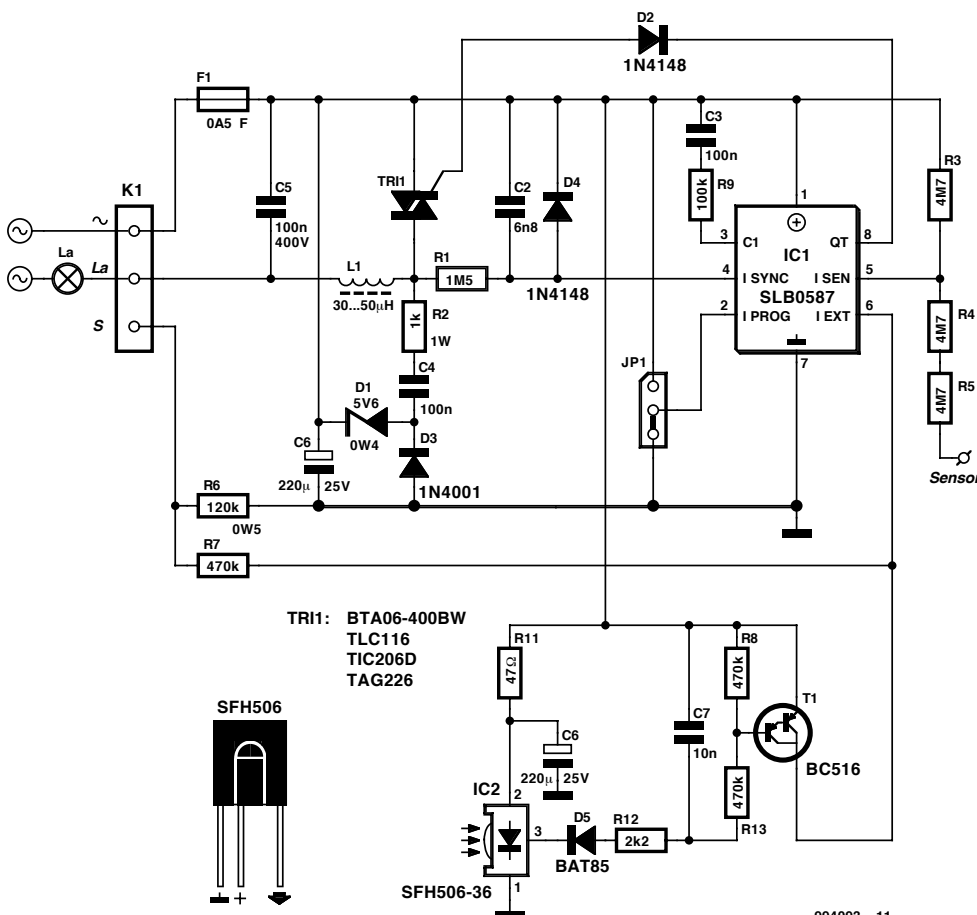


L. Lemmens

The dimmer is suitable not only for normal domestic lighting, but also for dimming halogen lamps (and other inductive loads).

The dimmer is based on a Siemens Type SLB0587, a circuit specially designed for this kind of application, and to which has been added an infra-red remote control. This remote control was published in the July/August 1998 issue of this magazine.

In the circuit diagram, the series network $R_2-C_4-D_1$ provides a direct voltage of 5 V directly from the mains to power IC₁. The IC



is also in sync with the mains voltage via resistor R_1 and capacitor C_2 . The actual phase gating is effected by triac Tri_1 , whose gate is linked to pin 8 (QT) of IC₁ via diode D_2 . The phase-locked loop (PLL) of the IC is synchronized with the mains frequency via capacitor C_3 and resistor R_3 .

The touch sensor that enables a domestic light to be dimmed consists of three 4.7 MΩ resistors, R_3-R_5 . These high resistance values make touching the sensor harmless. The output of the sensor is applied to pin 5 (I_{SEN}) of IC₁. Since in some cases it is handy to control the circuit with a push-button switch, this may be connected between S and La on connector K₁.

The IC also has an input I_{EXT} , which is for use with the optional infra-red remote control that is based on IC₂, a Type SFH506-36. This circuit picks up the signal from the sender and converts it into a control signal for IC₁ via a network that comprises among others, T₁ and R₇. The operation of the

Parts list

Resistors:

$R_1 = 1.5 \text{ M}\Omega$

$R_2 = 1 \text{ k}\Omega, 1 \text{ W}$

$R_3\text{--}R_5 = 4.7 \text{ M}\Omega$

$R_6 = 120 \text{ k}\Omega, 0.5 \text{ W}$

$R_7, R_8, R_{13} = 470 \text{ k}\Omega$

$R_9 = 100 \text{ k}\Omega$

$R_{11} = 47 \Omega$

$R_{12} = 2.2 \text{ k}\Omega$

Capacitors:

$C_1 = 47 \mu\text{F}, 16 \text{ V}, \text{radial}$

$C_2 = 0.0068 \mu\text{F}$

$C_3, C_4 = 0.1 \mu\text{F}, 630 \text{ V}$

$C_5 = 0.1 \mu\text{F}, 400 \text{ V}$

$C_6 = 220 \mu\text{F}, 25 \text{ V}, \text{radial}$

$C_7 = 0.01 \mu\text{F}$

Inductors:

$L_1 = 30\text{--}50 \mu\text{H}, 3 \text{ A}$

Semiconductors:

$D_1 = \text{zener } 5.6 \text{ V}, 400 \text{ mW}$

$D_2, D_4 = 1\text{N}4148$

$D_3 = 1\text{N}4001$

$D_5 = \text{BAT}85$

$T_1 = \text{BC}516$

Integrated circuits:

$\text{IC}_1 = \text{SLB}0587 \text{ (Siemens)}$

$\text{IC}_2 = \text{SFH}506\text{-}36$

Miscellaneous:

$\text{JP}_1 = 3\text{-way jumper}$

$\text{K}_1 = 3\text{-way connecting strip}$
for board mounting, pitch
7.5 mm

$\text{F}_1 = \text{fuse holder with } 0.5 \text{ A}$
(F) fuse

$\text{PC}_1 = \text{PCB pin}$

$\text{Tri}_1 = \text{BTA}06\text{-}400\text{BW}$ or
 $\text{TIC}206\text{D}$ or $\text{TAG}226$

PCB Order no. 994093 (see
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the end of this magazine)

dimmer is determined by jumper JP_1 . When this is left open, the dimmer will always start with the brightness with which it was switched off. Each time the dimmer is started, the direction in which it is controlled is reversed.

When the jumper is placed to connect pin 2 of IC_1 to C_3 , the dimmer always starts at maximum brightness. When the jumper is placed in the position shown in the circuit diagram, the dimmer always starts at minimum brightness.

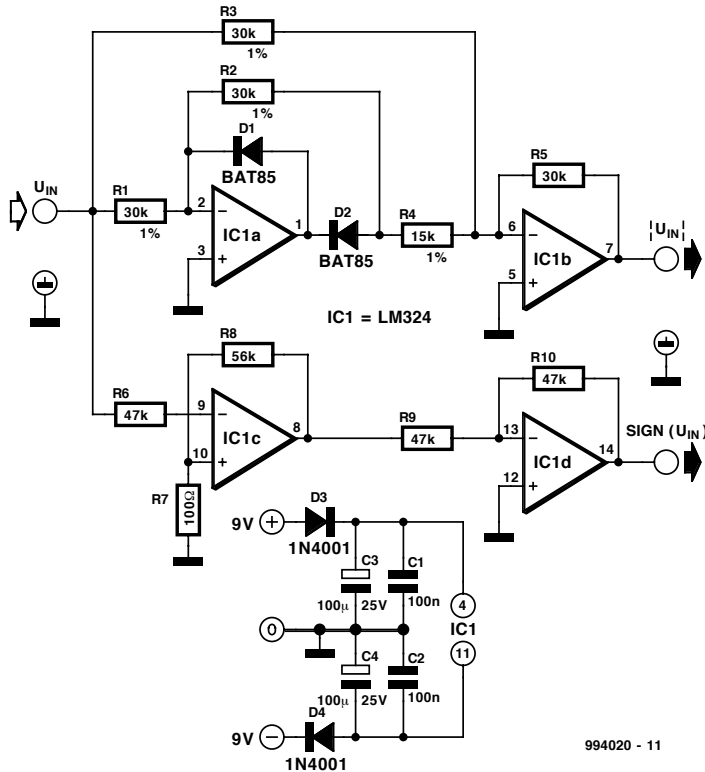
The dimmer is best built on the printed-circuit board shown, which is available through our Readers Services (see towards the end of this magazine).

It cannot be emphasized too strongly to bear in mind that the circuit carries potentially lethal mains voltages. Only connect the dimmer to the mains once it has been completed and built into an insulated or plastic case. If the infra-red remote control is not used, IC_2 and T_1 and associated components, except R_7 , may be omitted.

[994093]

absolute-value meter with polarity detector

002



Design by V. Mitrovic

This circuit breaks an input voltage signal down into its components: (1) the absolute value and (2) the polarity or 'sign' (+ or -). It will handle direct input voltages as well as alternating voltages up to several kHz. With a supply voltage of ± 9 V, the input level should remain below ± 6 V.

The circuit consists of two sections, each having its own function.

Operational amplifiers IC1a and IC1b form a full-wave rectifier, its output terminal supplying the absolute value of the input signal, while operational amplifiers IC1c and IC1d examine the polarity of the input voltage.

For negative input voltages, the output of IC1a goes high. Consequently D2 is reverse-biased so that IC1a has no effect on the rest of the circuit. IC1b then acts as an inverter because its amplification is $(-R5/R3)$ or -1 .

Thus, the output voltage is positive. For positive input voltages, D2 conducts and the amplification of IC1a is -1 . The output voltage is then determined by the sum of currents that flow through R3 and R4. Taking into account the polarities and the value of all resistors, the overall amplification becomes

$$-R5/R3 + (-R5/R4) \Leftrightarrow (-R2/R1) = -1 + 2 = 1$$

This means that the value of the output voltage at the output terminal is the same as the input voltage, but the polarity is always positive. The accuracy of the rectification process is determined by the accuracy of resistors R1-R4; close-tolerance (1%) types are recommended.

At low input voltages (smaller than 20 mV), the input offset voltage of the operational amplifiers may introduce significant errors. If this is the case, use individual operational amplifiers instead of an array of four (TL061, TLC271, AD548, ...), because they have pins for offset voltage compensation. Alternatively, use an operational amplifier with a low offset voltage like the OP07.

In the polarity detector IC1c acts as a comparator, with a certain amount of positive feedback due to R7 and R8. This feedback causes a hysteresis of 20 mV that prevents oscillation when the input voltage changes slowly. IC1d is an ordinary inverter. For input voltages above 10 mV, the SIGN output terminal will swing

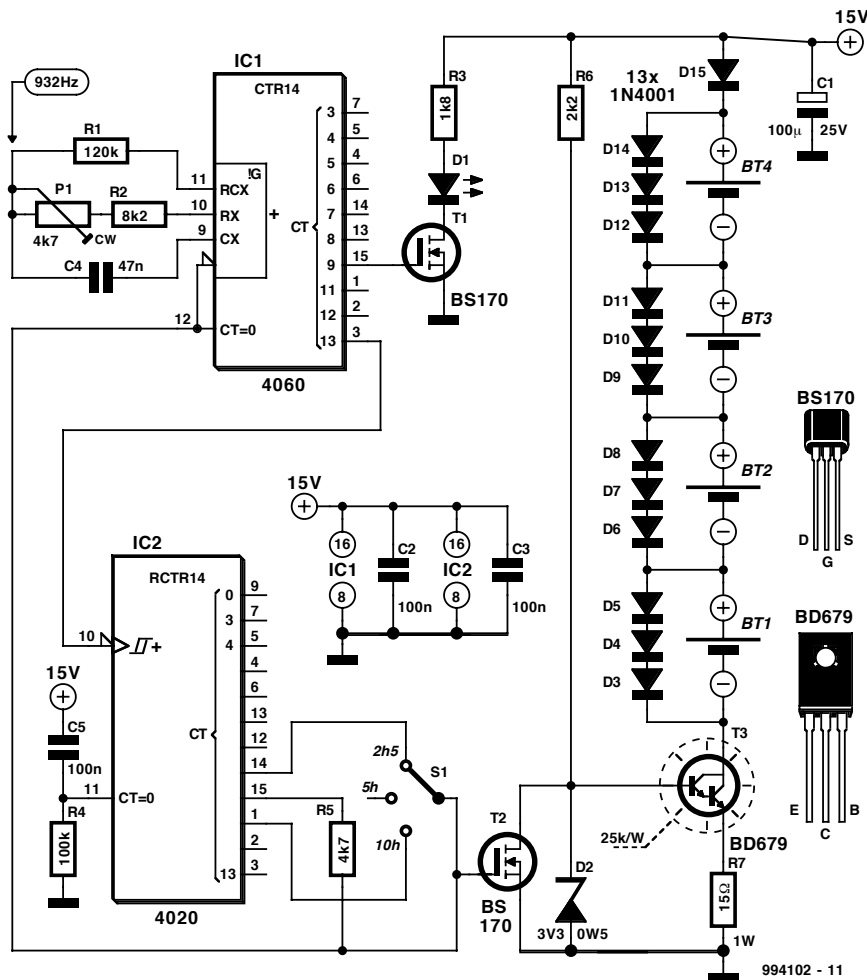
to almost the positive supply. When the input voltage is below -10 mV, the SIGN terminal drops low, almost to the negative supply voltage. For input voltages between these two thresholds, the output voltage is well defined, too, because it stays at its previous level. This circuit is the perfect complement to the '+ /- voltage on bargraph display' circuit discussed elsewhere in this issue (reference number 994012-1). The $|U_{in}|$ and SIGN outputs of the present

circuit may be directly connected to U_{in} and CONTROL IN inputs of the bi-directional bar display. The ± 6 V sign indicator signal may be used as the control voltage for the + /- voltage display as long as the reference voltage remains smaller than 3 V. Although presented as a pair, both circuits may of course be used individually for other purposes.

(994020-1)

general-purpose NiCd battery charger

003



dates batteries or cells Type R6 and R14. Switching off after a period of 2 h 30 m, 5 h, or 10 h is arranged by 3-way switch S_1 . The 2 h 30 m period is for charging Type R6 batteries (1/2 charge), the 5 h period for fully charging Type R6 batteries or half charging Type R14 batteries, and the 10 h period for fully charging Type R14 batteries. Light-emitting diode D_1 lights when charging is taking place. Charging after the set period has elapsed can be continued, if so desired, only by switching the supply off and then on again.

The time periods are determined by counters IC_1 and IC_2 , Type 4060 and 4020 respectively. The 4060 has an integral oscillator, whose frequency is set to 932 Hz with preset P_1 and the aid of a frequency meter.

For various reasons, such as the values of the components used and parasitic elements, the oscillator itself operates at a slightly higher frequency – of the order of 1 kHz. The frequency of the signal at the wiper of P_1 is divided by 2^{14} , so that the frequency of the signal at Q13 of IC_1 is 0.056 Hz, equivalent to a pulse every 17.6 s. The signal at Q13 is applied to the input, pin 10, of IC_2 . When switch S_1 is in position 2 h 5 m

(output Q10 of IC_2), the divisor should be 2^{10} (1024). However, contrary to what these figures indicate, the time period stops at half that at output Q10. To obtain a charging period of 2 h 30 m, that is, 9,000 seconds, which should correspond to half a period at output Q9 of IC_2 , the oscillator period must be $9000 \times 2 / 16.7 \times 10^6 = 1.073$ ms, which corresponds to a frequency of 932 Hz as mentioned earlier.

On power-on, only counter IC_2 is reset, since an error of a few seconds that may arise in IC_1 is of no significance. This arrangement simplifies the design. When the time set has elapsed, that is, charging is finished, diode D_1 goes out.

The charging current is fixed by darlington transistor T_3 , which is a classical design of a current source with negative feedback. The transistor tends to hold its emitter potential at 1.3 V, but this

J. Gonzales

There is a wide variety of NiCd (nickel-cadmium) battery chargers on the market, but there are not many that can work from an in-car 12 V cigar lighter. Such a charger would, for instance, be of interest to campers and caravanners who do not have a 230 V a.c. mains supply available. To satisfy the needs of these users, a charger could be designed for operation from the cigar lighter, but it is, of course, of far greater interest if it could also work from the domestic mains supply. Furthermore, it would also be very useful if a number of cells, say, 1 to 4, of different format could be charged simultaneously. Lastly, another benefit would be if the charger would automatically switch off once the battery or cells have been charged fully.

The charger described in this article does all that: it accommo-

requires the aid of a zener diode, D_2 . In this type of design, the thermal stability is, in fact, totally acceptable, because the temperature of the zener diode, in view of the small current this draws and its consequent low temperature rise, hardly affects the charging current

Transistor T_1 is either on or off and serves to power the on/off indicator LED. It is needed to prevent an overload on the output of counter IC_1 if this would be required to absorb the total current (about 7 mA) drawn by the diode.

Transistor T_2 discontinues the charging when the time set by S_1 has elapsed by earthing the base of darlington T_3 .

Diodes D_3 – D_{14} are connected in threesomes across the terminals of the batteries to be charged: D_3 – D_5 across those of battery Bt_1 , D_6 – D_8 across those of Bt_2 , and so on.

Diode D_{15} prevents the batteries to be charged from being discharged when the supply fails.

When the charger is used in a vehicle, additional precautions should be taken to ensure that any spurious surges on the vehicle power lines do not adversely affect the charger's operation.

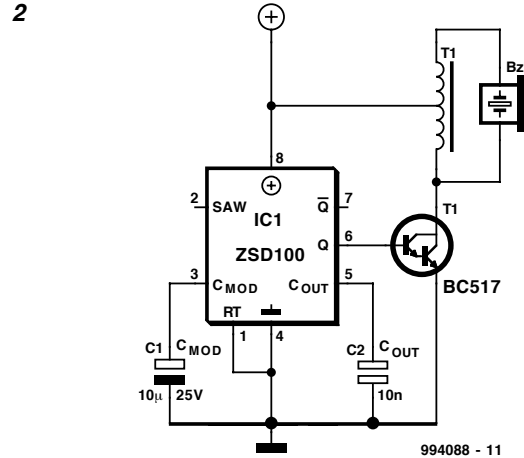
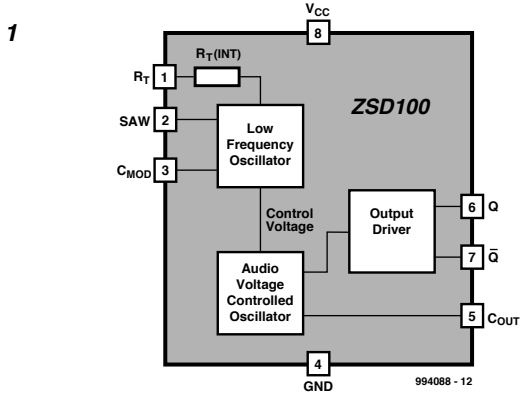
The battery holder should be one that can accommodate four size R6 (AM3; MN1500; SP/HP7; mignon) or R14 AM2; MN1400; SP/HP11; baby) batteries. The length of these batteries, but not their diameter, is the same (about 45 mm).

When the charger is used at home, it may be powered via a suitable 15 V mains adaptor. It draws a current of about 150 mA.

A final word of warning: it is possible for batteries to be connected to the charger with incorrect polarity. This may result in a very large discharge current and even destruction of the battery. It is, therefore, imperative to verify the correct polarity of the battery before inserting it into the holder.

siren driver

004



Pinout of ZSD100

1	R_T	Optional resistor to earth for improved frequency control of the modulation and the output oscillator. The R_T pin may be used to disable the IC by leaving it open or connecting to V_{CC} .
2	SAW	Determines the shape of the modulating signal. When SAW remains open, the signal is triangular; if it is linked to C_{MOD} , a true sawtooth is obtained.
3	C_{MOD}	The capacitor to earth (0.1–100 μF) determines the frequency of the modulating signal.
4	GND	Earth.
5	C_{OUT}	The capacitor to earth (0.001–0.1 μF) determines the centre frequency of the output oscillator.
6	Q	Non-inverting output driver.
7	Q	Inverting output driver.
8	V_{CC}	Supply voltage, 4–18 V

L. Lemmens

Zetex Semiconductors have a siren driver IC Type ZSD100 available that is suitable for use in alarm systems for cars and model craft. With the addition of only a few components as shown in the diagram, the device produces an ear-splitting sound of 120 dB.

The IC contains an a.f. rectangular-wave generator that is driven by a sawtooth generator. The sawtooth sweeps the output frequency range (sweep 2:1) once every second. The frequencies of both oscillators are dependent on an internal 61.5 k Ω resistor and

an external resistor, $R_T = < 1 \text{ M}\Omega$, and capacitors C_{MOD} and C_{OUT} . The output driver has an inverting and a non-inverting output.

The simplest application of the ZSD100 is shown in Figure 2 in which the sound is produced by a piezo buzzer. If a dynamic 6 Ω loudspeaker is used, it is connected in an H-bridge, that is, driven symmetrically. The value of resistor R_T must then be small, or the relevant pin must be strapped to earth.

The IC draws a current of about 25 mA in use, and around 1 μA in the quiescent state. It is suitable for operation over the temperature range of -40°C to $+125^\circ\text{C}$. The output can provide 5 mA at a level of 1.4 V and sink 0.5 mA.

Provided the specified values of resistors and capacitors are maintained, the circuit is ideal for experimentation. The frequencies are given by:

$$f_{MOD} = 2850 / C_{MOD} (61.5 + R_T)$$

and

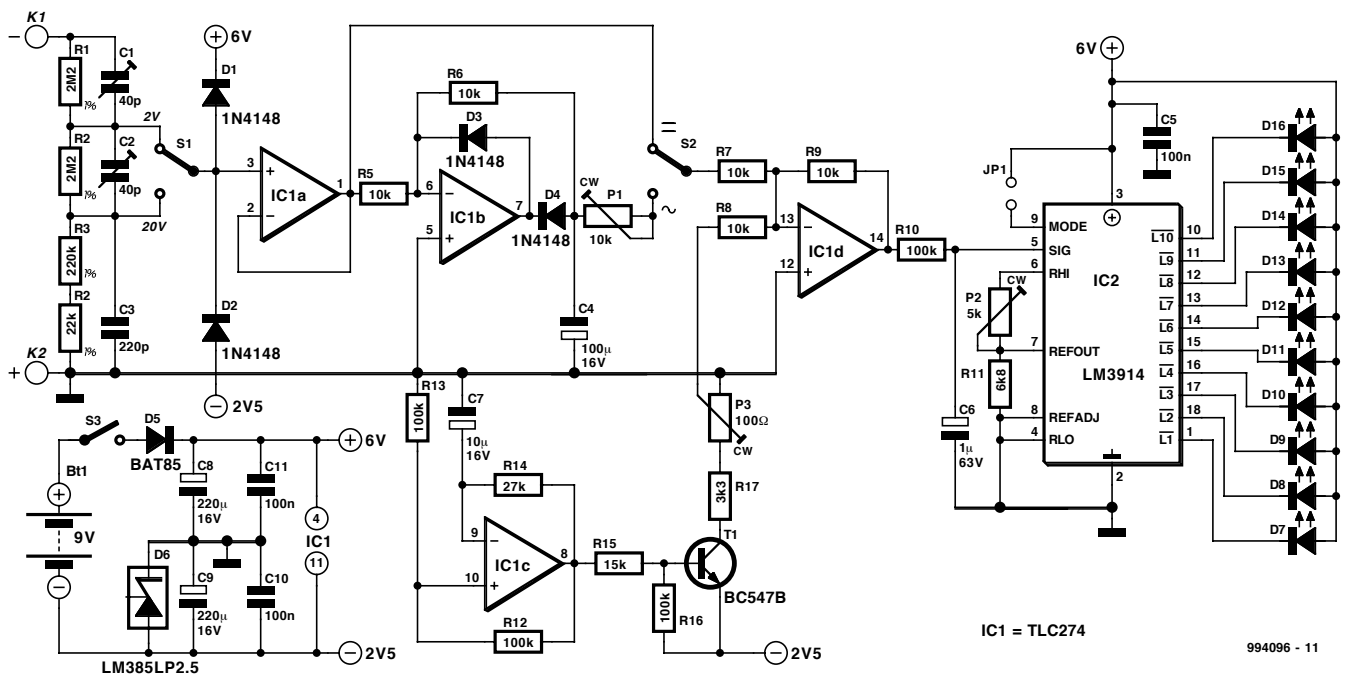
$$f_{OUT} = 1710 / C_{OUT} (61.5 + R_T),$$

where the capacitors are in μF and R_T is in kilohms.

[994088]

high-resolution AC/DC voltmeter with LED display

005



F. Hueber

Voltmeters with LED display are very useful instruments for repair and maintenance work on electronic equipment. Unfortunately, their resolution is normally poor: of the order of ten per cent at the top end of the range. The instrument described in this article has a resolution at least twice as good and also measures audio frequency signals up to 10 kHz with small error.

Almost all such voltmeters use the well-known Type LM3914 LED driver which can control up to ten light-emitting diodes. This means that with a total measuring range of 0–2 V, the voltage difference between two adjacent LEDs is 200 mV. When a rectangular voltage at a level of half this voltage difference is added to the measurand, and the resulting signal exceeds 200 mV, the next higher LED flashes. This arrangement ensures a resolution of about five per cent at the top end of the range.

The diagram shows the circuit of the voltmeter arranged for measuring ranges of 2 V and 20 V. The divider at the input lowers the analogue signal to about 1/20 when the 20 V position of switch S₁ is selected. Capacitors C₁–C₃ provide frequency compensation up to about 10 kHz. Diodes D₁ and D₂ provide protection against overvoltages. Operational amplifier IC_{1a} functions as an impedance inverter.

Alternating voltages are measured with the aid of active rectifier IC_{1b}, which has excellent linearity. During a positive half-wave of the signal the op amp operates as an inverting unity-gain amplifier (R₅ = R₆). Its output is negative, so that diode D₄ conducts, whereupon capacitor C₄ is charged to the peak level of the signal applied pin 6. During a negative half-wave, the output is positive, D₄ is reverse-biased, but the feedback is retained since diode D₃ then conducts. In the case of a direct-voltage input, the rectifier is bypassed by switch S₂.

Circuit IC_{1d} is a summing amplifier that combines the measurand and the 100 mV rectangular voltage. Since this stage inverts, whereas the LED driver requires a positive signal, the signals applied to the inputs of IC_{1d} must be negative with respect to earth. This is the reason for the somewhat unusual polarity of the rectifiers and the input terminals.

The rectangular signal is generated by IC_{1c} which, with com-

Brief technical data

Measurement range	100 mV–2 V, resolution 100 mV (AC/DC) 1–20 V, resolution 1 V (AC/DC)
Frequency range	10 Hz → 10 kHz ± 2 dB about –2 dB at 100 kHz
Input impedance	about 4.6 MΩ//20 pF
Power supply	9 V dry or rechargeable battery
Current drain	5 mA (stand-by) ≤ 6 mA (dot mode) ≤ 20 mA (bar mode)

ponent values as specified, oscillates at 1.6 Hz. This frequency may be altered within a wide range by changing the value of resistor R₁₄ to individual requirements.

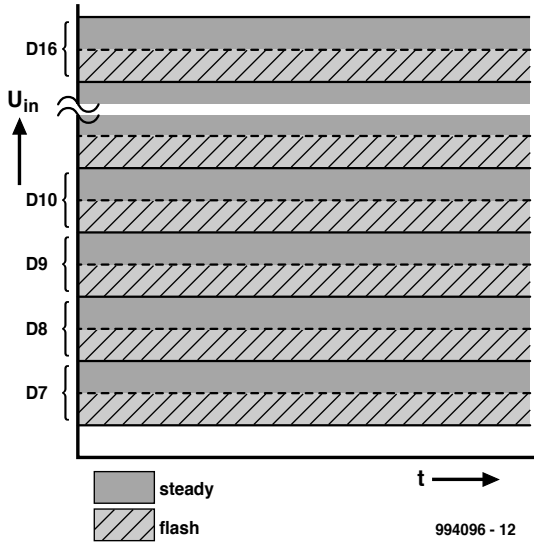
The output of the generator drives transistor switch T₁, which applies the –2.5 V signal periodically to potential divider R₁₇–P₃. The preset enables the exact level of the rectangular voltage to be set, whereupon this is applied via R₈ to pin 13 of IC₁ together with the measurand.

The LED driver, IC₂ is configured in a conventional manner. Its input pin 5 is preceded by filter R₁₀–C₆. The display mode is set with jumper JP₁: when this is left open, a bar display ensues; when it is closed, a dot display results.

The internal reference voltage of 1.25 V, which may be varied with preset P₂, is available at pin 7 (REF_{OUT}) and is used to set the brightness of the display. The current flowing from pin 7 via R₁₁ and P₂ determines the LED current (about 1.7 mA). It is, of course, advantageous to use high-efficiency LEDs.

In the power supply section reference diode D₆ ensures that even with fluctuating currents and falling battery voltage the negative supply line remains a stable –2.5 V with respect to earth. This ensures that the voltage across P₃ is independent of the state of the battery.

Diode D₅ provides protection against polarity reversal and is a Schottky type to minimize voltage losses. The battery voltage may



drop to 5.5 V before the accuracy of the display begins to suffer.

So as to save energy, an on/off indicator is not provided, but where this is wanted, an LED with a 2.2 k Ω series resistor may be added between the output of IC_{1d} and the +6 V line.

Before the voltmeter can be used, it must, of course, be calibrated. This is begun by checking the potential divider at the input by connecting a digital voltmeter (DVM) at the output of IC_{1a} and applying a 2 V direct voltage (+ to earth) across the input terminals. With S₁ in position 2 V, the DVM should indicate about 1 V. When S₁ is then set to position 20 V, the DVM should indicate about 0.1 V.

Next, set S₂ to position = and short-circuit P₃. Apply a voltage of exactly 2 V or 20 V (set S₁ accordingly) to the input terminals and adjust P₂ until D₁₆ just lights. Remove the short-circuit from P₃ and apply a voltage of exactly 10 V (set S₁ to 20 V) across the input terminals. In the dot mode, D₁₁ should light; in the bar mode, D₇–D₁₁ should light. If D₁₂ shows a tendency to flash, turn P₃ slightly towards earth until D₁₂ is out.

Increase the input voltage to 11 V and adjust P₃ until D₁₂ just begins to flash. When the input voltage is raised to 12 V, D₁₂ should be fully on. In the dot mode, only one LED should light, but in practice it will be found that when the input is raised from 10 V to 11 V, D₁₀ lights constantly and D₁₁ begins to flash. When the input is raised slightly more, both diodes light until D₁₀ goes out. A clearer indication is obtained in the bar mode, but this adds to the current drain from the battery.

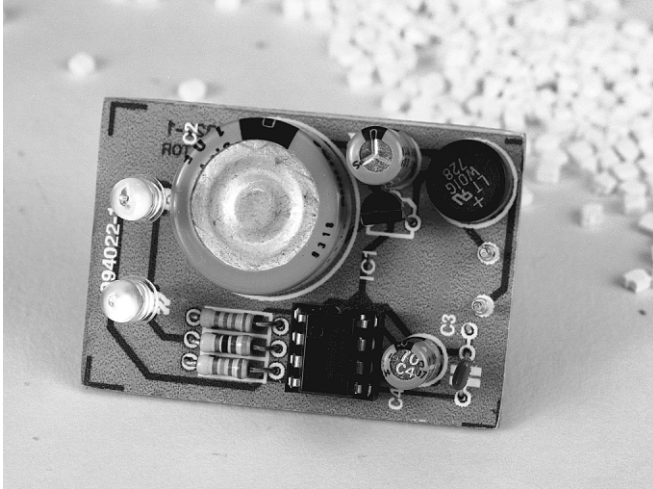
The AC range is calibrated by setting trimmer C₁ to its centre position (use an insulated small screwdriver) and applying a 100 Hz sinusoidal signal to junction R₁–R₂ (earth to K₂). Set S₁ to 20 V. Connect a DVM (10 V d.c. range) across C₄, set S₂ to <> and adjust the generator output until the DVM reads ≤ 1.4 V. Keep the generator output constant, change the frequency to 10 kHz, and adjust trimmer C₂ (insulated screwdriver) until the DVM reading is the same as with 100 Hz.

Next, set S₁ to 2 V and repeat the procedure just described at the same frequencies and adjust C₁ as before. Since the settings of the trimmers influence one another, the calibration of the AC ranges must be repeated a couple of times, setting C₁ with S₁ in the 2 V position and C₂ with S₁ in the 20 V position. A properly calibrated divider is virtually linear up to about 10 kHz.

Finally, to set the sensitivity of the instrument, apply a 100 Hz sinusoidal signal at an accurately known level to the input terminals and adjust P₁ until the LED display shows the r.m.s. value of the input signal.

bicycle rear-light afterglow

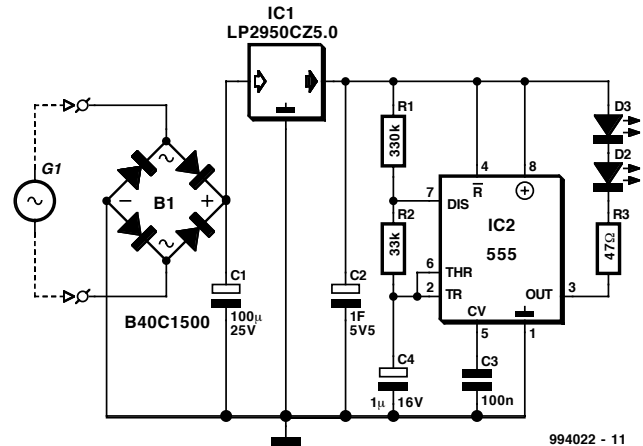
006



(For bicycles with a dynamo)

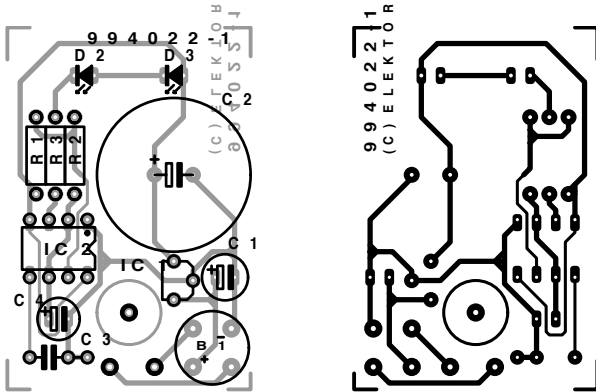
Stefan Knorr

This article is of interest only to readers whose bicycle lights are powered by a dynamo. The laws on bicycle lights in the United Kingdom are stricter than in most other countries and a dynamo is, therefore, a rarity in the UK.



For safety's sake, it is obligatory for cyclists in the UK to have the rear light of their bicycles on even when they are at standstill. Such a rule is, of course, also advisable in other countries, even when it is not mandatory.

In contrast to a similar article in the July/August 1998 issue of this magazine, the super-luminous LEDs are not powered directly by the regulator, IC₁, but via a timer, IC₂. The timer is driven by a pulsating voltage with a duty factor of 10%. This ensures very



low current drain and also that the reservoir capacitor, C_2 , can energize the LEDs for a long time.

Capacitor C_2 is charged when the bicycle, and thus the dynamo if this makes contact with the relevant wheel, is ridden. This happens via bridge rectifier B_1 , and low-drop regulator IC_1 . The output of the regulator is a steady + 5 V.

When the bicycle is in use, but at standstill, for instance, at traffic lights, the potential across C_2 powers an astable multivibrator

Parts list

Resistors:
 $R_1 = 330 \text{ k}\Omega$
 $R_2 = 33 \text{ k}\Omega$
 $R_3 = 47 \text{ }\Omega$

Capacitors:
 $C_1 = 100 \text{ }\mu\text{F}$, 25 V, radial
 $C_2 = 1 \text{ F}$, 5.5 V, Goldcap
 $C_3 = 0.1 \text{ }\mu\text{F}$, ceramic

Semiconductors:
 $B_1 =$ rectifier B40C1500,

round
 $D_2, D_3 =$ high luminosity LED

Integrated circuits:
 $IC_1 =$ LP2950CZ5.0
 $IC_2 =$ TLC555CP

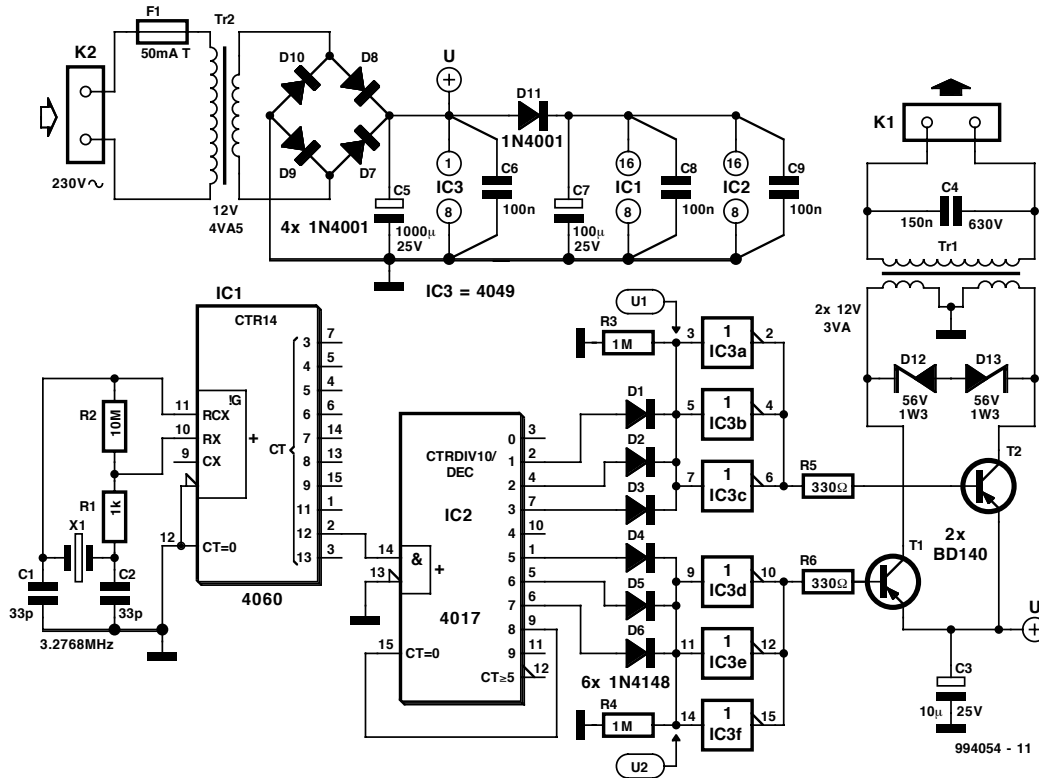
Miscellaneous:
 PCB Order No. 994022 (see Readers Services towards the end of this issue)

(AMV) IC_2 . With component values as specified, the switch-on time is about 0.02 s, but the LEDs are not energized until 0.25 s have elapsed.

The circuit is best built on the printed-circuit board, which is available through our Readers' Services (see towards the end of this issue) under Order. no. 994022.

frequency converter

007



K. Viernickel

The converter enables a mains voltage with unstable frequency to be converted to one with quartz-crystal stability. It may also be used to convert the mains frequency from 50 Hz to 100 Hz or to 25 Hz. It enables low-power equipment that needs an accurate mains voltage frequency to be supplied from an inexpensive 230 V

inverter (driven, say, by a 12 V car battery).

The time base, IC₁, of the converter is a crystal oscillator operating with a 3.2768 Mhz quartz crystal. This frequency is divided internally by 2¹³ to give an output frequency of 400 Hz. The 400 Hz signal is applied to counter/divider IC₂. When the reset of this IC is linked to Q₈ (pin 9), the circuit operates as an :8 divider so that

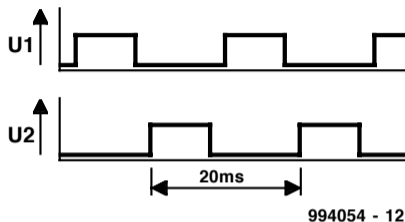
its output is exactly 50 Hz.

The output signals of IC₂ are bundled by wired-OR gates D₁–D₃ and D₄–D₆ into U₁ and U₂ respectively. These signals (shown at the top of Figure 1) are used to control drivers T₁ and T₂ via parallel-connected inverters contained in IC₃, a Type 4049 CMOS circuit. The drivers alternately switch a 12 V transformer winding into circuit, which, because of the constantly changing magnetic flux, results in a stable 230 V alternating voltage across the primary of the transformer.

The drivers are standard Type BD140 p-n-p transistors, so that the inverters in IC₃ draw current when the the relevant driver is on. It is a well-known fact that CMOS elements are far better in drawing current than providing current. The drivers are protected against high-voltage spikes by zener diodes D₁₂ and D₁₃.

Capacitor C₄, in conjunction with the stray inductance of the transformer, forms a bypass for high-frequency components in the primary winding of the transformer.

The frequency of the output voltage may be changed to 100 Hz

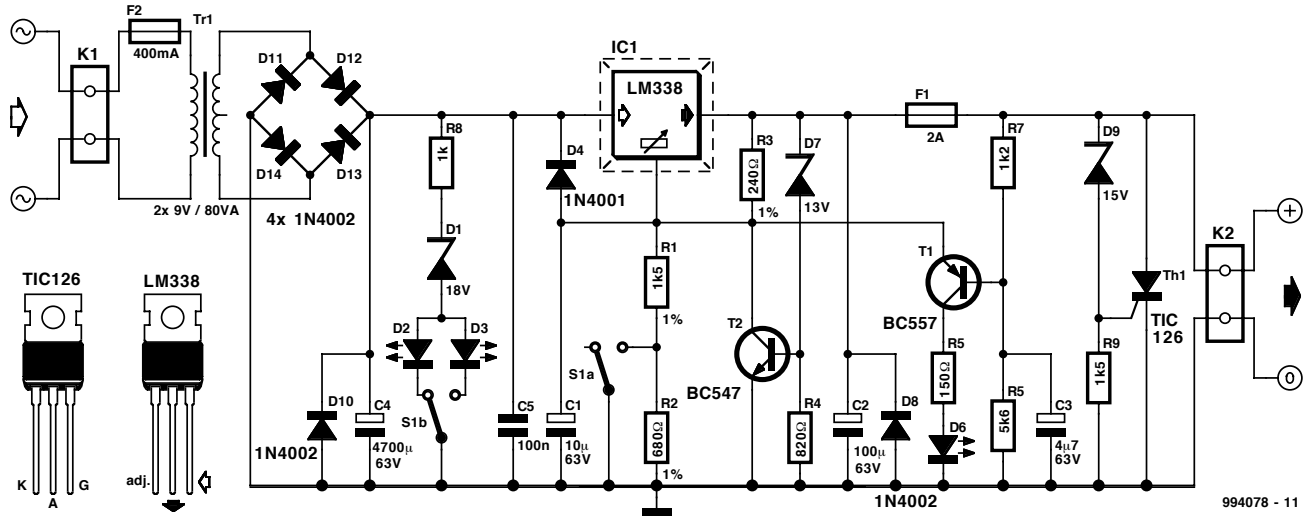


or 25 Hz by linking Q₁₁ (pin 1) or Q₁₃ (pin 3) respectively to the clock input of IC₂.

Note that in the supply circuit at the bottom of the diagram, diode D₁₁ and capacitor C₇ prevent excessive voltage fluctuations caused by the heavy load presented by the drive circuit from adversely affecting the operation of IC₁ and IC₂.

rugged PSU for ham radio transceivers

008



994078 - 11

Design: N.S. Harisankar VU3NSH

This rugged power supply is based on the popular LM338 3-pin voltage regulator. The LM338 is capable of supplying 5 A over an output voltage range of 1.2 V to 32 V with all standard protections like overload, thermal shutdown, overcurrent, internal limit, etc., built in. In this power supply, some extra protections have been added to make it particularly suitable for use with low to medium-power portable and mobile VHF/UHF (ham) and 27 MHz transceivers.

Diodes D4 and D5 provide a discharge path for capacitors C1 and C2. Diode D8 protects the supply against reverse polarity being applied to the output terminals. Capacitor C1 assists in RF decoupling and also increases the ripple rejection from 60 dB to about 86 dB. If junction R1-R2 is not grounded by switch S1A, transistor T2 starts to conduct, causing the regulator to switch to zener diode D7 for its reference voltage (13 V). The PSU output voltage will then be 12.3 V. Normally, T2 will be off, however, and the PSU output voltage is then about 8.8 V. The high/low switch is useful to control the RF power level of modern VHF/UHF handhelds.

Transistor T1, a p-n-p type BC557, acts as a blown-fuse sensor. When fuse F1 melts, T1 starts to conduct, causing LED D6 to light. If, for whatever reason, the PSU output voltage exceeds about 15 V, thyristor TH1 is triggered (typically in less than a microsecond). Such a high-speed 'crowbar' may look like a drastic measure, but remember that this kind of protection is required by digital ICs that will not stand much overvoltage. The crowbar, when actuated, will faithfully destroy fuse F1 rather than allow the PSU to destroy expensive ICs.

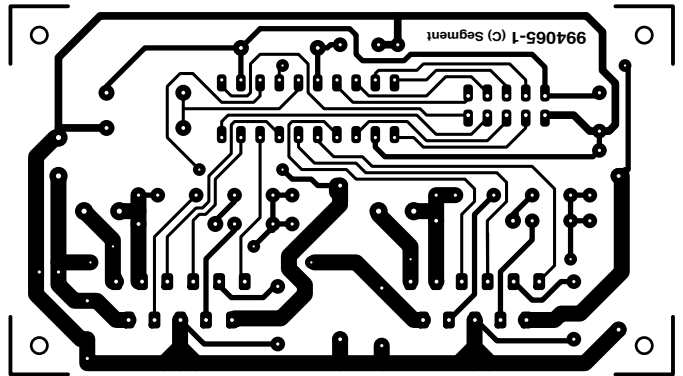
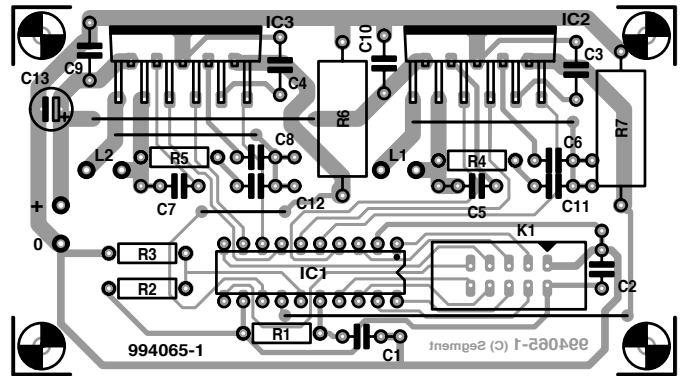
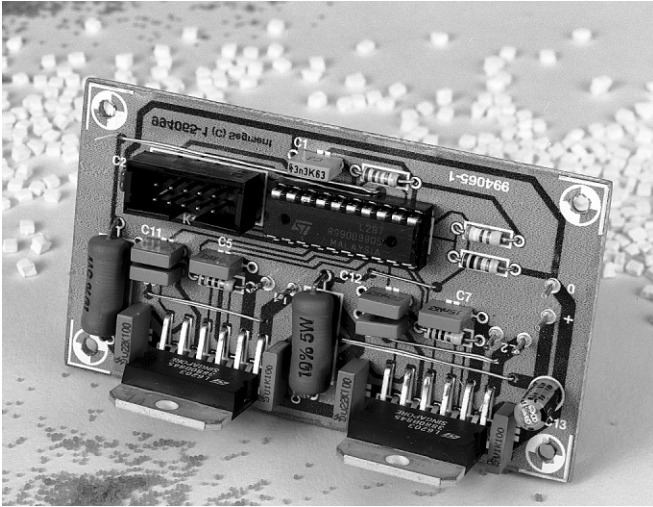
The two LEDs on the S1B contacts not only act as 'high/low' indicators but also as power-on indicators which are turned off when the mains voltage drops below about 160 V.

If you envisage 'heavy-duty' use of the PSU, then voltage regulator IC1 should be mounted on as large a heatsink as you can get. The minimum we'd say is an SK129 heatsink from Fischer (Dau Components).

(994078-1)

ELEKTOR		
240V~	50Hz	
No. 994078		
F = 400 mA		

stepper motor control 009



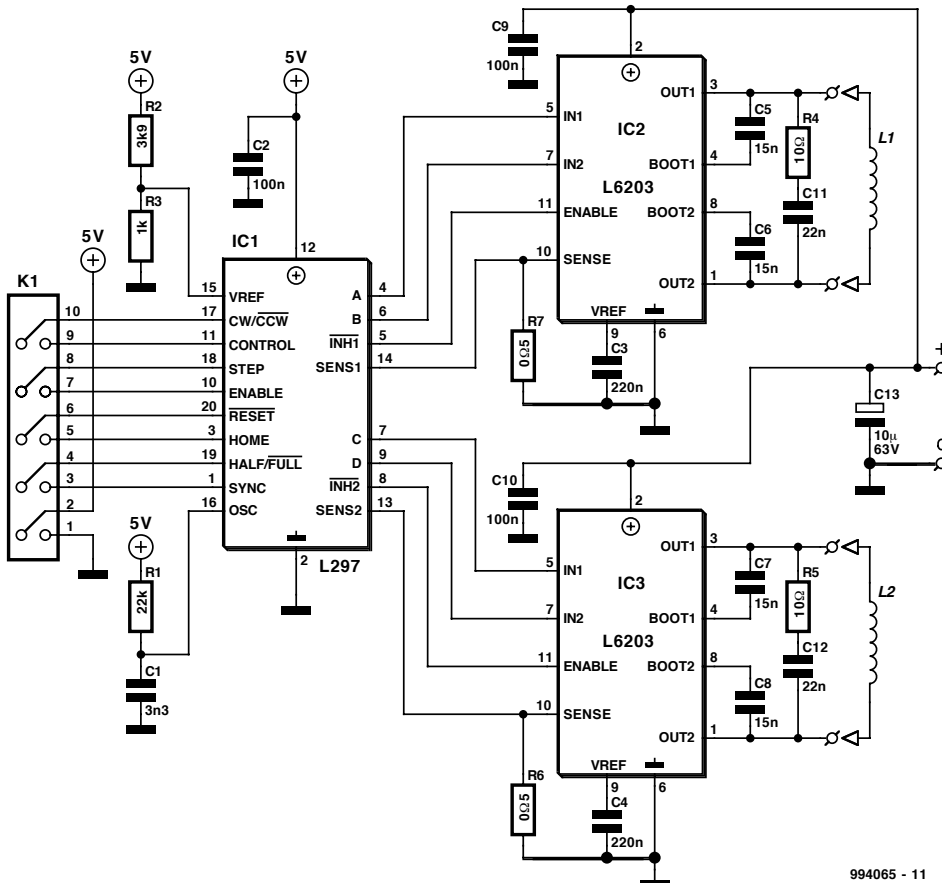
K.S.M. Walraven

The control is a compact design for driving bipolar stepper motors. Driver stages IC₂ and IC₃ are modern types from ST Microelectronics. Because of the combination of CMOS logic with D-MOS power transistors, these devices need few external components. Also, compared with the previous generation of bipolar devices such as the L298, the D-MOS transistors drop lower voltages so that the internal dissipation is smaller.

The input stage, IC₁, enables the motor to proceed one step for each pulse at its input pin 18. The level at pin 17 (CW/CCW)

determines whether the motor rotates clockwise or anticlockwise. The level at pin 19 decides whether the motor moves whole or half steps for each pulse at pin 18. In normal operation, pin 20 (reset), pin 11 (control), and pin 10 (enable) should be linked to the +5 V supply. Pin 1 (sync) is an output used when several L297s are driven in tandem and should be left open in the present design. Pin 3 (home) is an output that indicates when outputs A, B, C, and D, assume the binary code 0101, and is not used in the present design. The other pins are of less importance and will in most cases not be used at all – further information may be obtained from Internet address <http://www.us.st.com>

Since the current through the motor coils must not only be switched on and off, but also be reversed, the driver ICs contain a complete bridge formed by four D-MOSFETs. The upper two need to be driven by a potential that is higher than the supply voltage, and this is obtained with the aid of a boot-



994065 - 11

Parts list

Resistors:

$$R_1 = 22 \text{ k}\Omega$$

$$R_2 = 3.9 \text{ k}\Omega$$

$$R_3 = 1 \text{ k}\Omega$$

$$R_4, R_5 = 10 \text{ }\Omega$$

$$R_6, R_7 = 0.5 \text{ }\Omega, 3 \text{ W (see text)}$$

Capacitors:

$$C_1 = 3.3 \text{ nF}$$

$$C_2, C_9, C_{10} = 100 \text{ nF}$$

$$C_3, C_4 = 220 \text{ nF}$$

$$C_5\text{--}C_8 = 15 \text{ nF}$$

$$C_{11}, C_{12} = 22 \text{ nF}$$

$$C_{13} = 10 \text{ }\mu\text{F}, 63 \text{ V, radial}$$

Semiconductors:

$$IC_1 = \text{L297}$$

(ST Microelectronics)

$$IC_2, IC_3 = \text{L6203}$$

(ST Microelectronics)

Miscellaneous:

$$K_1 = 10\text{-way header}$$

$$PC_1\text{--}PC_6 = \text{PCB pins}$$

$$L_1, L_2 = \text{bipolar stepper motor}$$

$$\text{PCB Order no. 994065-1}$$

strap circuit (C_5, C_6). Network $R_4\text{--}C_{11}$ suppress voltage peaks across the motor terminals. Most of the other capacitors in the dia-

gram are decoupling (bypass) elements.

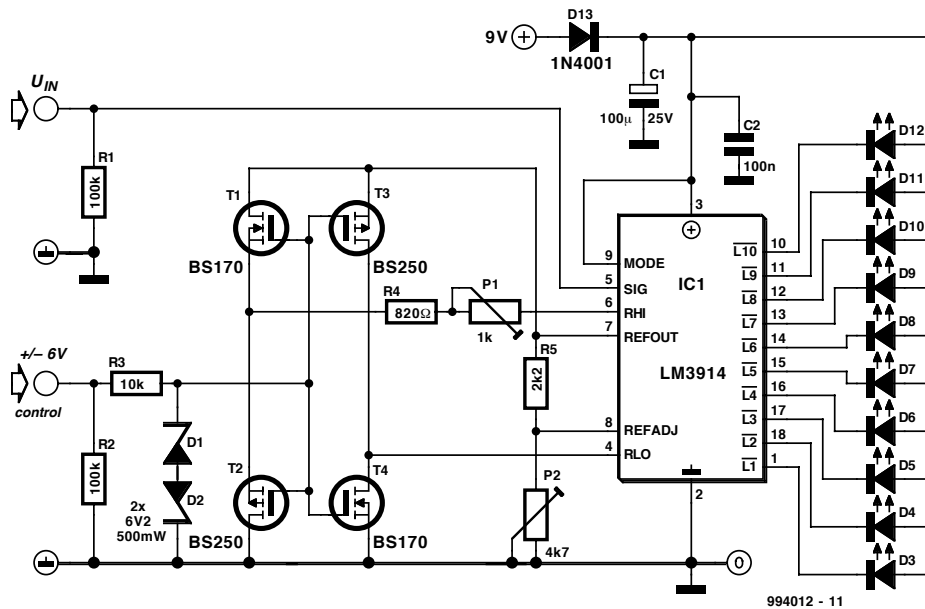
The driver ICs can handle currents of up to 4 A at voltages up to 42 V. For safety's sake, it is better for the voltage to remain well below 42 V; the current is internally limited to 4 A. Any tendency of the current to rise above this level is sensed by resistors R_6 and R_7 , whereupon the IC is disabled. The value, R , of these resistors must, therefore, be in line with I_m , the motor current: $R = 1/I_m$.

The driver ICs are provided with internal thermal protection, but when the dissipation is large, it is advisable to mount them on a suitable heat sink. They do not get damaged by heat, but they do switch off the motor when the temperature rises above the maximum specified temperature.

Finally, it should be noted that IC_1 operates from a +5 V supply (via K_1) from which it draws a current of about 50 mA. The voltage at pins 0 and + is intended for the stepper motor and should be equal to, or a little higher than, the rated motor voltage.

+/- voltage on bargraph display

010



Design by V. Mitrovic

The LM3914 is a truly versatile component. Besides LEDs, only a few other components are needed to make the 'bidirectional' bargraph voltmeter shown here. The circuit is similar to a conventional bar display, but it offers a possibility to change the direction in which the LEDs are switched on. This may be useful, for example, when positive and negative voltages are measured. For a positive input voltage, the LEDs are switched on in the usual manner, that is, from D3 to D12, while for negative voltages, the LEDs are switched on in the opposite direction, from D12 to D3. Obviously, the negative voltage must be 'rectified', i.e. inverted, before the measurement. A suitable circuit for this purpose is presented in the article 'Absolute-value meter with polarity detector' (reference number 994020-1) elsewhere in this issue.

A set of transistor switches (MOSFETs) controls the direction in which the LEDs light. When the control voltage is high (+ 6V, according to the schematics, but any voltage that is at least 3V

higher than reference voltage will do), T1 and T4 are switched on, while the other two MOSFETs are off. In this way, the LM3914 is configured in the usual manner with the top end of the resistor network connected to the internal voltage reference and the low end connected to ground. As the input voltage rises, the comparators inside the LM3914 will cause the indicator LEDs to be switched on one by one, starting with D3.

When the control voltage is lower than about -3V, T2 and T3 are switched on while T1 and T4 are off. Consequently, the ends of the resistor network are connected the other way around: the top end goes to ground and the low end, to the reference voltage. The first

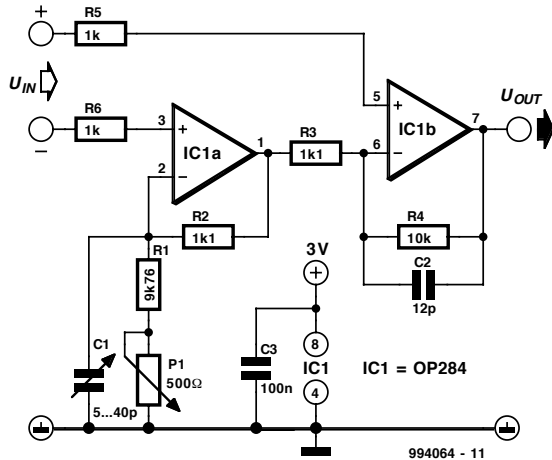
LED to be switched on will then be D12; i.e., the LEDs that forms the bargraph display light in the opposite direction. Although not documented by the manufacturer of the LM3914, this option works well, but only in bar mode (in dot mode, internal logic disables any lower-numbered LEDs when a higher-numbered LED is on, which obviously conflicts with our purposes).

To achieve good symmetry, an adjustable resistor is added to the voltage divider in the LM3914. Using a DVM, adjust the preset until the voltage across P1+ R4 equals 1/11th part of U_{refout} . Sensitivity is determined with the ratio of resistors R5 and P2. If, for example, the reference voltage is set to 2.2 V by means of P2, there will be a voltage drop of 200 mV per resistor in the ladder network (including R4-P1). So, the first LED will switch on when the input voltage exceeds 200 mV, the second, at 400 mV, and so on, and the whole display will be on at 2 V.

The circuit draws about 100 mA when all LEDs are switched on.

(994012-1)

single-supply instrumentation amplifier



An Analog Devices application

The OP284 is a low noise dual op amp with a bandwidth of 4 MHz and rail-to-rail input/output operation. These properties make it ideal for low supply voltage applications such as in a two op amp instrumentation amplifier as shown in the diagram.

The circuit uses the classic two op amp instrumentation topol-

ogy with four resistors to set the gain. The transfer equation of the circuit is identical to that of a non-inverting amplifier.

Resistors R_2 and R_3 should be closely matched to each other as well as to resistors $(R_1 + P_1)$ and R_4 to ensure good common-mode rejection (CMR) performance. It is advisable to use resistor networks for R_2 and R_3 , because these exhibit the necessary relative tolerance matching for good performance. Potentiometer P_1 is used for optimum d.c. CMR adjustment, and capacitor C_1 is used to optimize a.c. CMR.

With circuit values as shown, circuit CMR is better than 80 dB over the frequency range of 20 Hz to 20 kHz. Circuit referred-to-input (RTI) noise in the 0.1 Hz to 10 Hz band is exemplary at $0.45 \mu\text{V}_{\text{pp}}$.

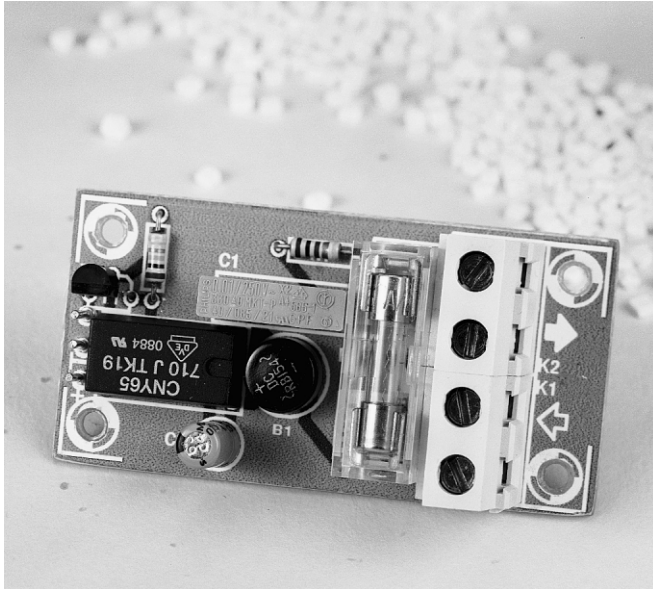
Resistors R_5 and R_6 protect the inputs of the op amps against overvoltages. Capacitor C_2 may be included to limit the bandwidth. Its value should be adjusted depending on the required closed-loop bandwidth of the circuit. The R_4 - C_2 time constant creates a pole at a frequency, $f_{3\text{dB}}$, equal to

$$f_{3\text{dB}} = 1/2\pi R_4 C_2.$$

With a value of C_2 of 12 pF, the bandwidth is about 500 kHz.

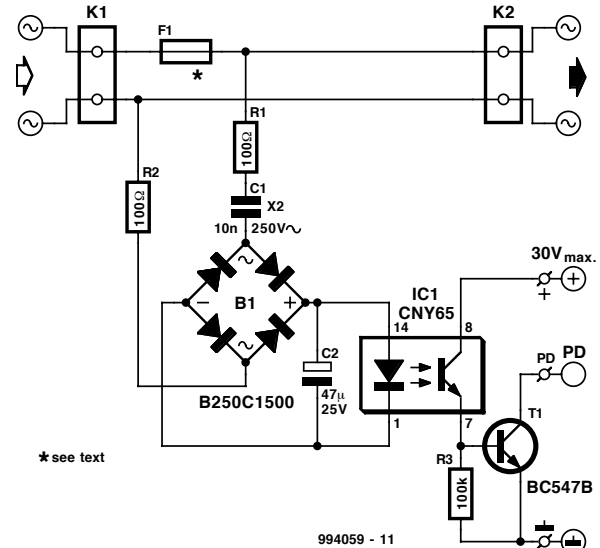
The amplifier draws a current of about 2 mA.

mains voltage detector 012

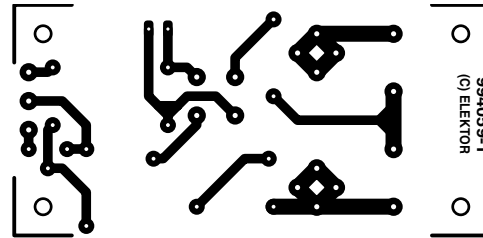
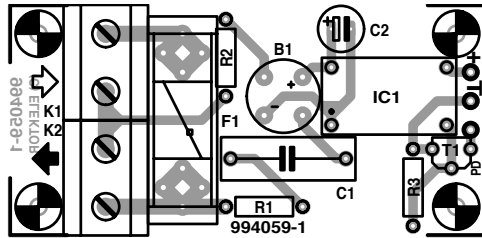


Design by T. Giesberts

The detector is intended to sense and signal to another circuit that an appliance is connected to the mains voltage. For this purpose, an



optocoupler, IC1 in the circuit, is used. The light-emitting diode in this device is connected across the mains voltage rectified by bridge B1. The mains voltage is applied to this bridge via potential divider R1-C1-R2. When the capacitor has a value as specified



in the diagram, the current through the diode is about $700\ \mu\text{A}$ (for a mains voltage of 230 V). This results in sufficient light to make the phototransistor conduct. The drop across the LED is about 1 V. The detector draws a current only when the monitored equipment is switched on. It is intended to be built into the appliance whose mains connection is to be monitored and must, of course, be connected behind the mains on/off switch.

A possible application of the detector is in the preamplifier described in the June 1999 issue of *Elektor Electronics* ('DIY: From vinyl to compact disc'). When it senses that the record player is being switched on, it can be used to link the Line-In input of the soundcard automatically to the preamplifier. Another possible application is its use as a power-on reset circuit in a protection system.

Transistor T1 can switch currents of up to 10 mA; in the prototype, the knee voltage of the transistor was around 200 mV at a current of 20 mA.

The maximum permissible switching voltage of the optocoupler is

COMPONENTS LIST

Resistors:

R1, R2 = $100\ \Omega$
R3 = $100\ \text{k}\Omega$

Capacitors:

C1 = 10nF 250VAC (class X2)
C2 = $47\ \mu\text{F}$ 25V radial

Semiconductors:

B1 = B250C1500
T1 = BC547B
IC1 = CNY65
(Temic/Telefunken)

Miscellaneous:

K1, K2 = 2-way PCB terminal block, pitch 7.5mm
F1 = fuse holder with fuse (rated as required)

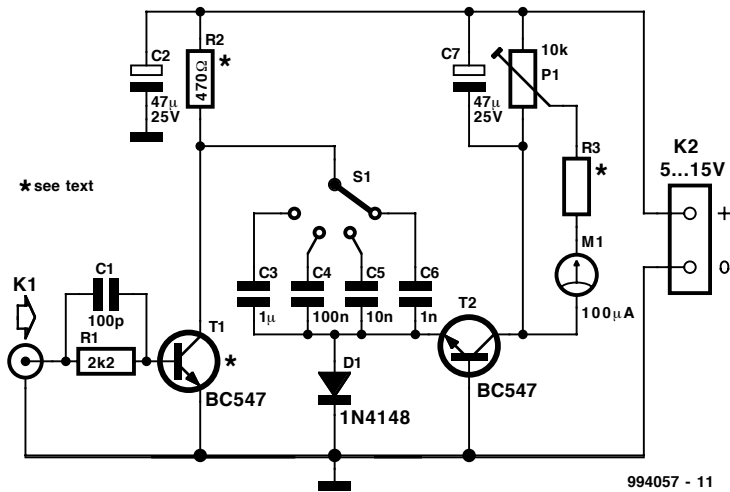
30 V.

Fuse F1 is added to allow a fuse to be omitted on the monitored appliance.

The PCB shown here is not available ready-made through the *Elektor Electronics* Readers Services.

generator scale enhancement

013



994057 - 11

F. Hueber

The set frequency of inexpensive frequency or function generators is often indicated by a simple scale on the tuning knob, which is not normally very accurate. It is possible to improve this by adding a counter discriminator circuit consisting of a small number of standard components as shown in the diagram.

The input should be a square wave at TTL level to drive transistor T_1 which functions as a switch. The RC network in the base circuit improves the switching operation at high frequencies.

One of capacitors C_3 – C_6 , depending on the position of switch S_1 , is charged and discharged via T_1 and R_2 in synchrony with the input signal. Resistor R_2 plays an important role in achieving the wanted accuracy. If its value is high, the relevant capacitor cannot be charged fast enough at high frequencies, with the result that the signal at the collector of T_1 is no longer a true square wave. On the other hand, when T_1 is on, the current through the resistor, and thus the total current drain, is small. If, however, the value of R_2 is small, the relevant capacitor is charged at the correct speed, which improves the accuracy, but the current drain is higher. Clearly, the value of the resistor specified is a compromise between these requirements.

The charging and discharge currents of the relevant capacitor flow through the base-emitter junction of T_2 and diode D_1 . Owing to the reactance of the capacitor, the currents vary linearly with the frequency. The relatively high currents would result in relatively high pulses at the collector of T_2 were it not for capacitor C_7 which integrates the pulses into a smooth direct voltage, whose level also depends on the frequency. The direct voltage is applied to a milliammeter, M_1 , via preset P_1 and resistor R_3 .

The circuit may be used for voltages in the range 5–15 V: the current drain, I_B , at several voltages, U_B , and the requisite value of R_3 for a $100\ \mu\text{A}$ meter are shown in the table. The current level in brackets refers to R_2 having a value of $1\ \text{k}\Omega$, but this results in the measurement error, which is normally about 2%, rising somewhat.

If current drain is of no consequence, the value of R_2 may be lowered until the current through T_1 just does not exceed the maximum permissible level of 100 mA. The minimum values of R_2 for various conditions are shown in the table.

The level of the supply voltage is not critical, but the voltage should be well regulated. If a digital display instead of an analogue meter is used, replace the meter by a 1 k Ω resistor and measure the voltage across this in the 200 mV range. When a liquid-crystal display (LCD) voltmeter is to be used, bear in mind that this needs a discrete supply. To use the total display range of an LCD voltmeter, the ranges may be set to 200 Hz, 2 kHz, 20 kHz, and 200 kHz. It is then necessary to use an r.f. transistor, such as the BSX20, in the T_1 position.

For good accuracy, capacitors C_3 – C_6 must have the same tolerance and their values should be in a ratio of 1:10. Note that the circuit capacitance may have an effect when the switch is in the C_3 position.

To calibrate the circuit, apply in each range a square-wave input signal at a frequency of about 2/3 of the maximum in that range (660 Hz in the 1 kHz range) and adjust preset P_1 to obtain a voltage reading of about 2/3 of the maximum for that range. Without

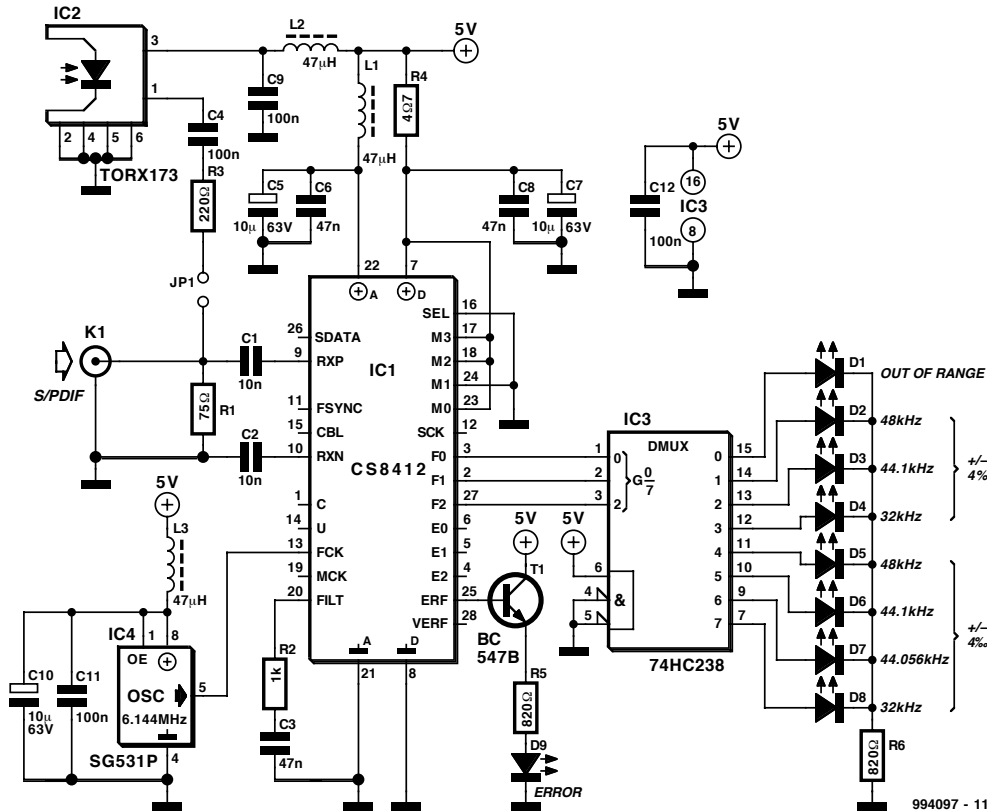
UB V	IB mA	R3 k Ω	R2 min Ω
5	9	15	56
9	15	39	100
12	19 (12)	56	120
15	22 (14)	68	150

altering the setting of P_1 , find the range in which the highest voltage reading is obtained. Adjust P_1 to exactly the input frequency. In the three other ranges, the readings are then slightly too small, but this is rectified by placing small value capacitors in parallel with the range capacitors until the correct frequency is displayed.

If all this is too cumbersome, replace P_1 by a 10 k Ω resistor and solder four parallel-connected presets in series with R_3 . These presets must be switched by a second wafer on S_1 . This arrangement allows each range to be calibrated independently of the others. If, furthermore, a three-wafer switch is used, the third wafer enables the decimal point of an LCD to be switched in.

S/PDIF monitor

014



tor, IC₄, enables the receiver to differentiate incoming signals by means of a frequency comparator – and this is what the present monitor does. When the frequency of an incoming signal differs from a reference value, the difference is indicated in one of three ways: < 400 ppm; < 4%; and out of range (differs more than 4% from the reference value). Clearly, the accuracy of the crystal oscillator determines the precision of these limits (the SG531P crystal from Epson used in the diagram has an accuracy of ± 100 ppm).

The optical input provided by IC₂ is a useful addition. The output of this circuit is applied across R₁ via C₄, R₃ and jumper JP₁. The potential across R₁ may also be used as a digital output, in which case the value of R₃ needs to be adapted as necessary.

The circuit may also be used as a kind of relay station or as a means for reducing jitter. For these purposes, IC₁ is connected in a special mode (mode 13) when M₃ is made 1, and M₀–M₂, 1, 0, and 1, respectively. When these levels are set the received S/PDIF data, including the preamble, is transferred directly to the output. The bit clock, SCK, then has a value twice as high as would be the case with coded data. It is possible to connect a TOSLINK module, or a coaxial output via a buffer (such as a number of parallel-linked 74HC04 inverters), to the

T. Giesberts

The monitor is one of the many applications possible with the digital audio interface receiver Type CS8412 from Crystal. Other applications described in earlier issues of this magazine dealt with the decoding of the S/PDIF (Sony/Philips Digital Interface Format) into data, bit clock and L/R clock in a digital voltmeter or clipping indicator. The addition of an external reference oscilla-

SDATA output.

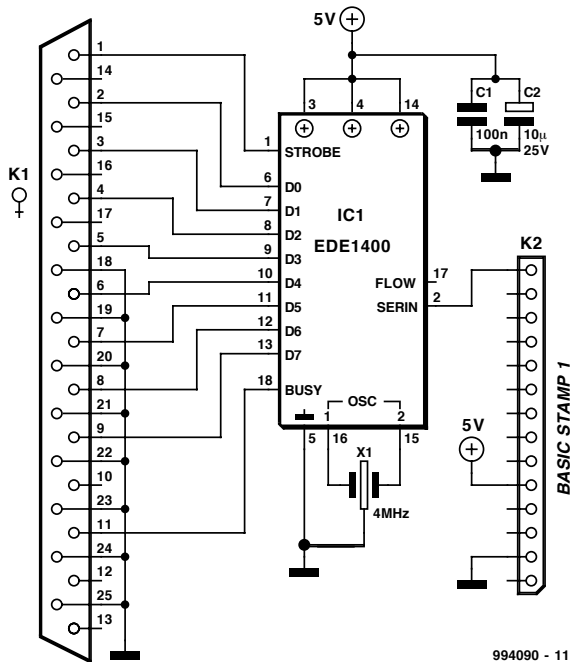
A demultiplexer, that is, 3-to-8 line decoder IC₃, is used to decode the data at F₀–F₂ to eight separate light-emitting diodes.

Diode D₉ indicates whether IC₁ receives no or poor data. The overall circuit draws a current of not more than 35 mA.

[994097]

printer port for BASIC Stamp

015



994090 - 11

Design by L. Lemmens

Users of the BASIC Stamp are generally satisfied with the product, but there are many who wish the device has a parallel printer

port. Such a port is particularly helpful when the BASIC Stamp is used as a data logger.

Fortunately, it is possible to provide the Stamp with a printer port by adding just one IC. The relevant circuit is based on IC1, an EDE1400 from E-Lab Digital Engineering. This chip converts the serial data into a parallel port at TTL level. The IC works from a single +5-V power supply and needs an external 4 MHz crystal for its oscillator. The internal circuits (a programmed PIC!) process the Centronics protocol.

The requirements on the data to be converted are not high: any serial signal at 2400 baud (no parity, eight data bits, and one stop bit) suffices. When the serial data have been received (the design is such that only a signal line and an earth return are needed), the circuit generates the requisite control signals for the printer. The internal watchdog/timer guarantees troublefree operation. A simple test program is shown in the listing.

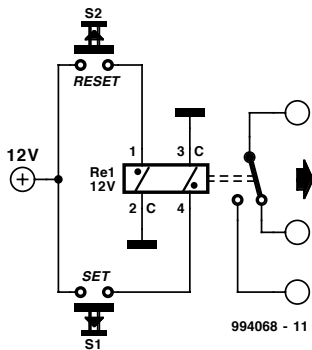
(994090-1)

Testprogramma

```
ser out 7, T2400, (" This text is from the Stamp 1"  
ser out 7, T2400, ( 10) : REM Carriage Return  
ser out 7, T2400, ( 13) : REM Line Feed  
for b7 = 48 to 57 : REM ASCII 0 through 9  
ser out 7, T2400, (b7)  
next b7  
ser out 7, T2400, ( 10) : REM Return
```

bipolar relay with single supply

a



G. Böhme

When a bipolar relay is to operate from a single supply voltage, normally two coils are needed. When, in Figure 1, the push-button RESET switch briefly connects the second terminal of coil 1 with $+U_b$, the relay is in one position. Pressing the SET switch briefly causes the relay to switch over to the other position. The relay can, however, change over only if the currents through the coils flow in opposite directions.

There are bipolar relays available that make operation with a single coil possible, but these are quite expensive. These relays are operated with voltages of opposite polarity or with a voltage whose polarity can be reversed.

An alternative, suggested by Robert Friberg in *Model Railroad Electronics*, 4 ('Adaptor for bipolar switches', p. 81), is shown in

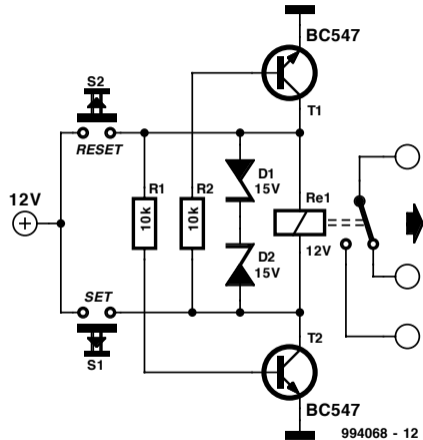
Figure 2. As in the case of a bipolar relay with two coil, the terminals of the solenoid are alternatively linked to the positive supply voltage, U_b . At the same time as one terminal is connected to $+ U_b$, the other is linked to earth by a transistors whose base is connected via a series resistor to the first terminal, that is, $+ U_b$.

Low-power bipolar relays with a coil resistance of 2–5 k Ω may be combined with small-signal transistors, such as the BC547. These transistors need a base resistor of about 10 k Ω . Higher power relays need power transistors and base resistors appropriate to the relay coil resistance.

The transistors should be protected against voltage spikes by free-wheeling zener diodes with a zener voltage slightly higher than the operating voltage.

[994068]

b

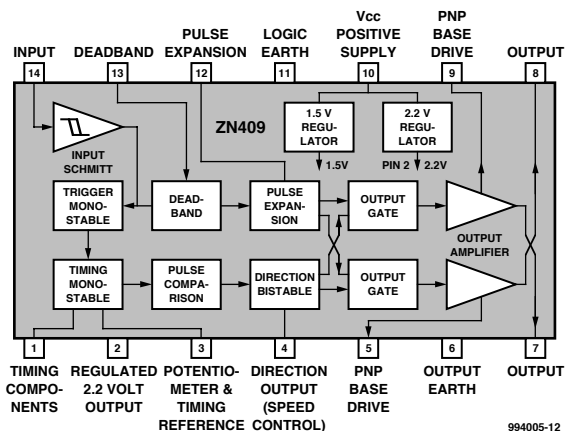
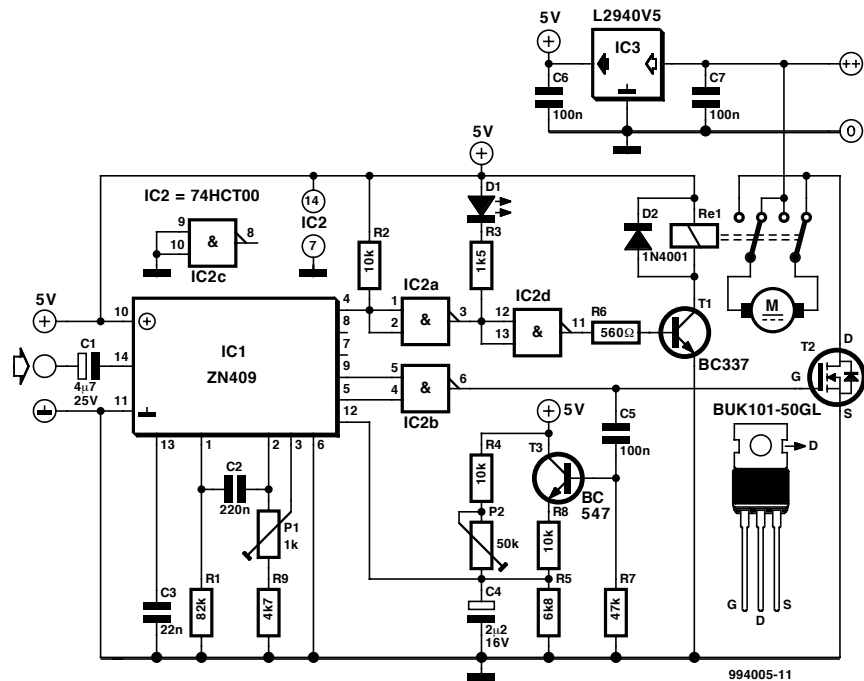


speed controller for model train

J. Schröder

The Type ZN419CE servo control IC from Ferranti is ideal for use in model railway direct-current engines. The internal circuit diagram of this device is shown in **Figure 1**. The IC varies the pulse width of input pulses in direct proportion to the displacement of a potentiometer. It operates with positive-going input pulses which can be coupled directly or via a capacitor to input pin 14. The advantage of a.c. coupling is that should a fault occur which causes the input signal to become a continuous level, the servo will remain in its last quiescent position, whereas with direct coupling the servo output arm will rotate continuously.

The active input is a Schmitt trigger input (pin 14), which allows the servo to operate consistently



with slow input edges and supplies the fast edge required by the trigger monostable independent of input edge speed. The input pulse is compared with the monostable pulse in a comparison circuit and one output is used to enable the correct phase of an on-chip power amplifier. Additionally, a deadband, that is the period during which the motor must not move, is effected by capacitor C₃ between pin 13 and earth.

Any difference between the input and monostable pulses is used to drive the motor in such a direction as to reduce this difference so that the servo takes up a position that corresponds to the position of the potentiometer in the controller.

The relation between the setting of the joystick on the controller and the duty factor of the output signal (0–100%), which determines the speed of the engine, depends on the potential at pin 12. This potential is set with P₂, while the rest position of the joystick and the motor is set with P₁.

The potential at pins 5 and 9 are applied to the inputs of NAND

gate IC_{2b}. The pulse-width modulated (PWM) output of this gate is applied to TTL-compatible power MOSFET T₂, which switches the motor. The PWM signal drives the pulse expansion circuit via C₅ and T₃. In this way, pulses that are only just outside the dead-band are expanded, which improves the control over the motor.

The potential at pin 4, which decides the direction of travel, is applied to relay Re₁ and Re₂ via gates IC_{2a} and IC_{2d}, and buffer T₁. The relays serve to reverse the polarity of the motor. The direction of travel is indicated by diode D₁. When the relays are in the rest position, the direction of travel should be forward, since their rating of 12–16 A applies only to short periods of time.

The supply voltage for the servo is held steady by regulator IC₃. This should be a low-drop type if the input to K₂ ≤ 8 V; with higher

voltages, a standard 7805 may be used. The supply voltage for the motor is, of course, not regulated.

Transistor T₂ can handle currents of up to 25 A. If a higher current is needed, two of these transistors can be connected in parallel. A somewhat less expensive transistor is the BUK100 which can handle currents of up to 13 A.

If a printed-circuit board is used for the construction, it should be capable of working with the high currents mentioned earlier (separation of tracks!).

The motor should be decoupled for noise and interference by ceramic capacitors rated ≥ 50 V: 0.01 μF between casing and earth and 0.01–0.1 μF across the terminals.

programmable amplifier 018

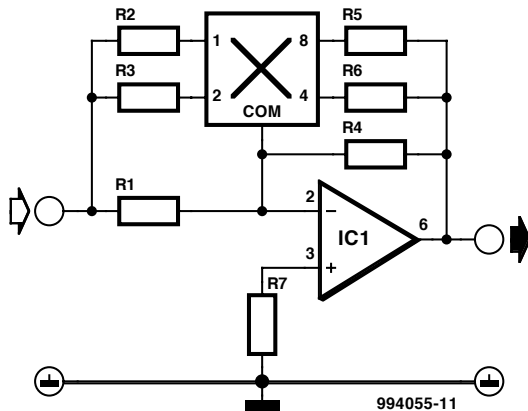


Table 2. Design example

$R_1, R_4, R_6 = 20 \text{ k}\Omega$

$R_2 = 20 \text{ k}\Omega$

$R_3, R_5 = 30 \text{ k}\Omega$

$$A = - (R_4 \parallel R_5 \parallel R_6) / (R_1 \parallel R_2 \parallel R_3)$$

Switch	Amplification
C	-0.25
4	-0.50
E	-0.75
0	-1.00
6	-1.50
5	-2.00
2	-3.00
1	-4.00
3	-6.00

B. Schädler

One way of designing a programmable amplifier is placing a HEX-coding switch in the feedback loop of an operational amplifier

(op amp). A 16-position coding switch has a mother contact, COM, and four binary coded outputs. Depending on the switch position, COM is linked to the relevant output.

Op amp IC₁ is arranged as an inverting amplifier with resistors R₁ and R₄ providing the feedback. These resistors are shunted by one or two resistors, as the case may be, by the coding switch. Each of the 16 ensuing combinations provides an amplification or attenuation factor as shown in Table 2.

The circuit as shown has a slight drawback: a changing input impedance. This means that in certain applications a buffer should precede the input. Bear in mind also that the resistor at the non-inverting input of IC₁ compensates for the input offset current and should therefore have a value that is comparable with that of the parallel combination of R₁, R₂, and R₃.

The switching may be augmented by replacing the coding switch by an analogue switch and operate this via a micro-controller.

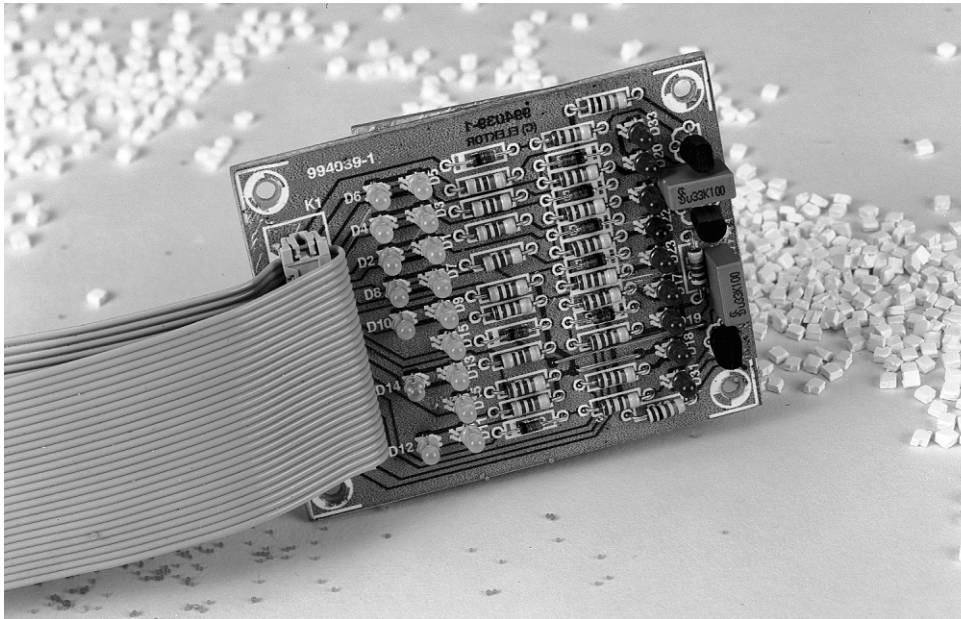
Table 1. Resistor shunting with a hex coding switch.

Switch position	Input resistance			Feedback resistance		
	R1	R2	R3	R4	R5	R6
0	R1			R4		
1	R1	R2		R4		
2	R1		R3	R4		
3	R1	R2	R3	R4		
4	R1			R4	R6	
5	R1	R2		R4	R6	
6	R1		R3	R4	R6	
7	R1	R2	R3	R4	R6	
8	R1			R4		R5
9	R1	R2		R4		R5
A	R1		R3	R4		R5
B	R1	R2	R3	R4		R5
C	R1			R4	R6	R5
D	R1	R2		R4	R6	R5
E	R1		R3	R4	R6	R5
F	R1	R2	R3	R4	R6	R5

[994055]

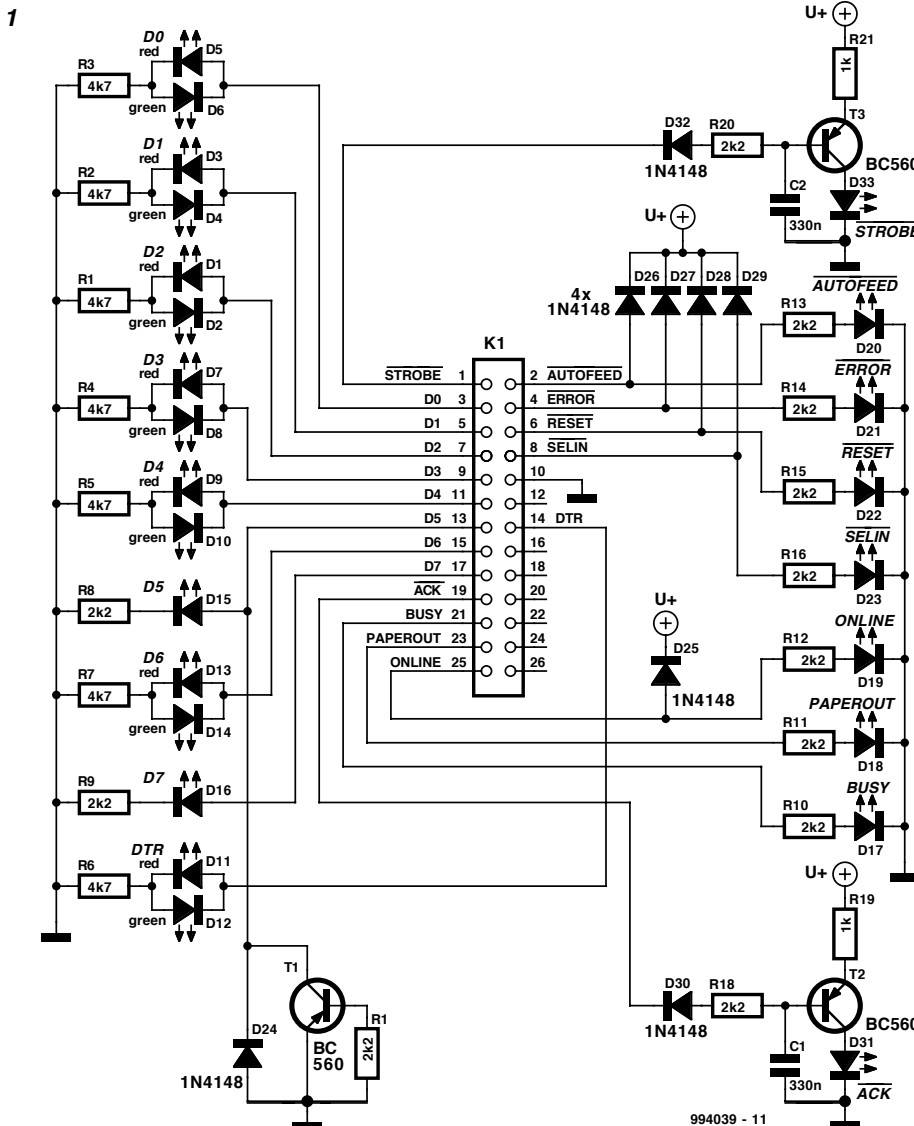
LPT/COM tester

019



W. Foede

Any computer owner/enthusiast who likes to experiment should really have an interface tester. This need not be an expensive, proprietary instrument: in most cases a simple Go/NoGo tester as shown in Figure 1 is perfectly adequate. The circuit may be used for testing the level on serial interface lines (COM) as well as on parallel ones (LPT). As a reminder: parallel interfaces normally work with TTL levels (0–5 V), whereas serial interfaces usually work with levels of ± 12 V to ± 15 V (although interfaces used with laptop and palmtop computers invariably use TTL levels). For both cases a common 26-pin box header with protective shoulder and polarity and positioning lug. The link to the computer is via 25-core flatcable with pressed-on sub-D connectors. Note that pin 26 of the box header is not connected. If the COM interface on the computer has a 9-pin connector, a suitable adaptor must be used. The interconnections between the box header and the interface connectors are shown in the table.

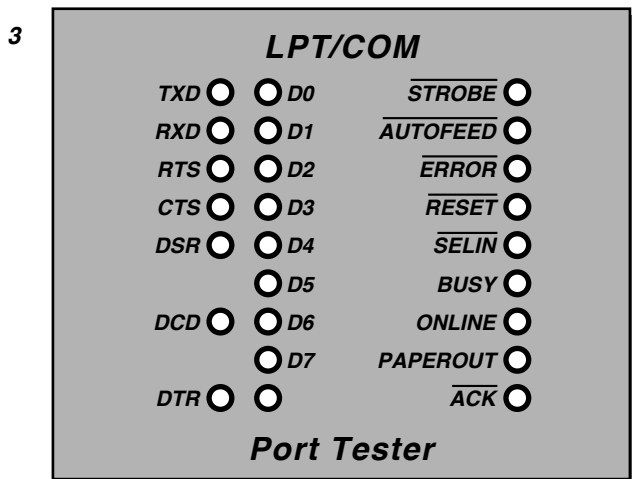
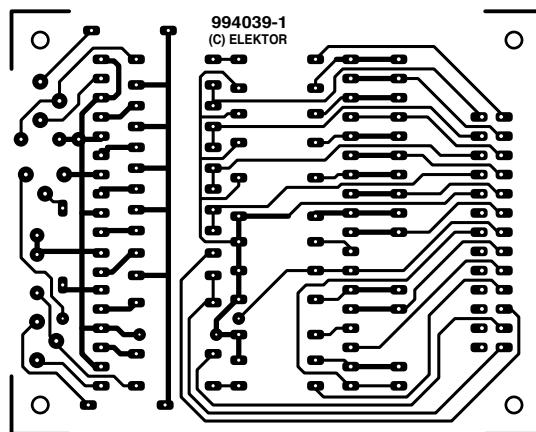
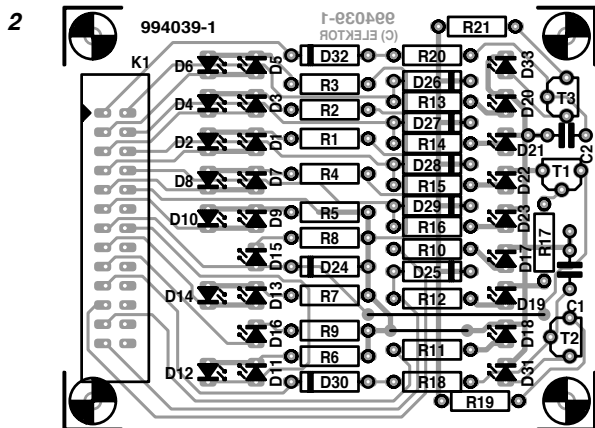


LPT DISPLAY

The display for the parallel interface consists of a red light-emitting diode (LED) and series resistor for each wire linked to earth. If the level on the wire is + 5 V, the diode lights, except in the case of the ACKNOWLEDGE and STROBE lines. On these lines, the LED is connected via an inverter, T₂ and T₃ respectively, so that it lights when the line is active low. The supply voltage is derived from active low lines AUTOFEED, ERROR, RESET, SELECT IN, and ONLINE, via 'OR gates' D₂₅–D₂₉. Network R₁₈–C₁ (R₂₀–C₂) stretches the display time, which can be altered to individual requirements by changing the component values within certain limits.

COM DISPLAY

The level display of the serial interface uses the same LEDs as the LPT display, but, since negative voltages occur on certain lines, green LEDs are connected in antiparallel with the red LEDs where relevant.



994039 - 12

Parts list

- | |
|-----------------------------|
| D15–D23, D31, D33 = LED |
| D24–D30, D32 = 1N4148 |
| T1–T3 = BC560 |
| Resistors: |
| R1–R7 = 4.7 kΩ |
| R8–R18, R20 = 2.2 kΩ |
| R19, R21 = 1 kΩ |
| Semiconductors: |
| D1, D3, D5, D7, D9, D11, |
| D13 = LED, red |
| D2, D4, D6, D8, D10, D12, |
| D14 = LED, green |
| Miscellaneous: |
| K1 = 2×13 polarized box |
| header |
| 25-way sub-D male connec- |
| tor for cable fitting |
| 25-way sub-D female con- |
| connector for cable fitting |
| PCB Order no 994039-1 |

Additionally, there is a DTR line and transistor T₁, which is linked to the (LPT) DATA5 line. In the case of a serial interface, this line is linked to the interface earth, which is passed on as a reference potential via D₂₄ when the levels are positive, and via T₁ when the levels are negative. Note that the transistor operates with reduced current amplification since otherwise the brightness of D₁₅ in the LPT mode would be insufficient.

CONSTRUCTION

The tester is best built on the printed-circuit board shown in Figure 2. The construction is very simple, but do not forget the two wire bridges and make sure that all components, where relevant, are wired in with correct polarity. The cathodes of the LEDs are identified by a short terminal, whereas those of the other diodes are marked by a ring. To ensure that all LEDs are at the same height above the board, first fix the board to the ready drilled lod of the enclosure and only then solder the LEDs in place.

At the left adjacent to K₁ is the COM display (negative levels). In the centre is the common LPT/COM display for positive COM levels as well as LPT levels of data lines DATA0 to DATA7. At the right is the display for the LPT control levels.

The design of a suggested front panel is shown in Figure 3.

[994039]

Pinout of K₁

K ₁	LPT	COM
1	STROBE	
2	AUTOFEED	
3	DATA 0	TxD
4	ERROR	
5	DATA 1	RxD
6	RESET	
7	DATA 2	RTS
8	SELECT IN	
9	DATA 3	CTS
10	GND	
11	DATA 4	DSR
12		
13	DATA 5	GND
14		DTR
15	DATA 6	DCD
16		
17	DATA 7	
18		
19	ACKNOWLEDGE	
20		
21	BUSY	
22		
23	PAPER OUT	
24		
25	ONLINE	
26	n.c.	

12-bit ADC with I²C™ interface

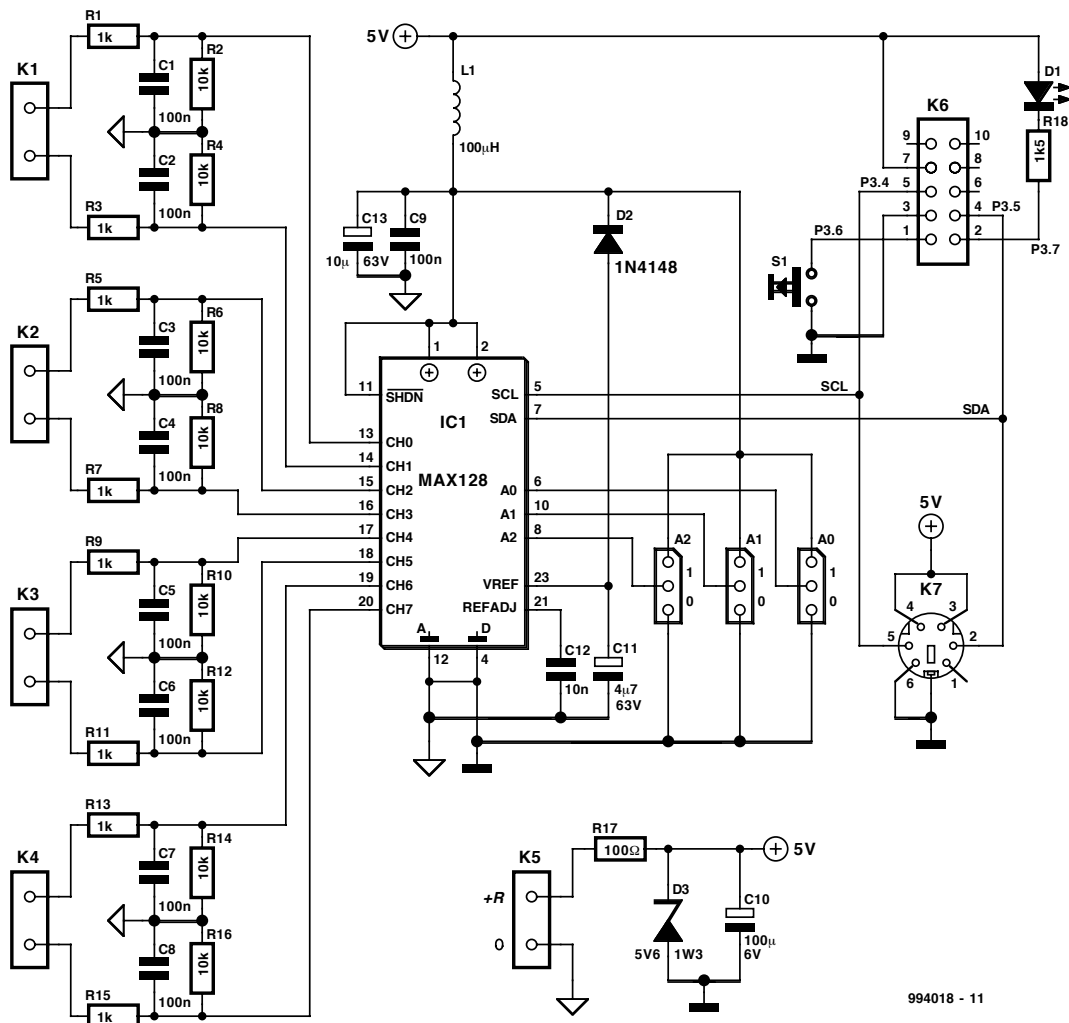
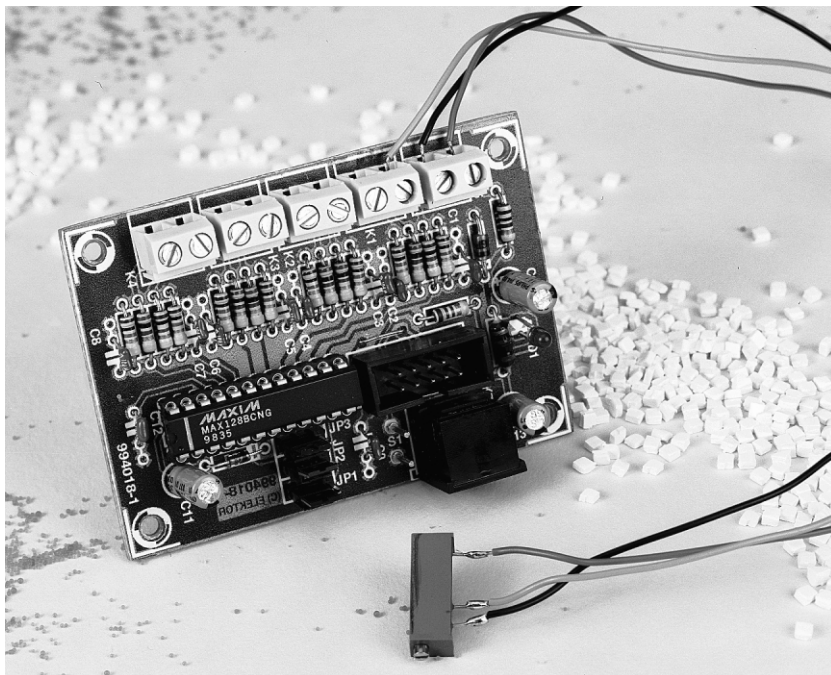
020

K.S.M. Walraven

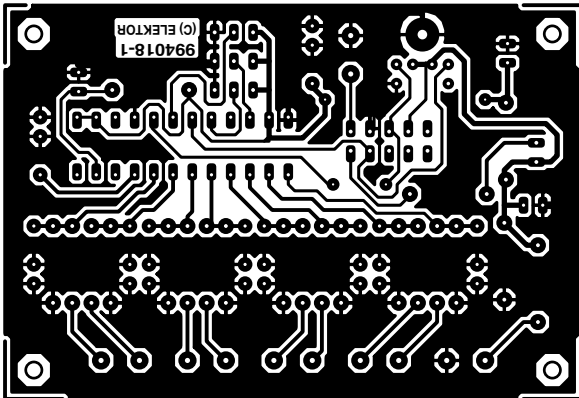
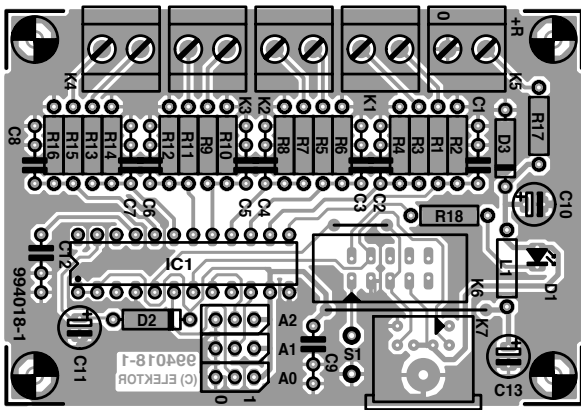
Until not so long ago, only 8-bit analogue-to-digital converters (ADC) offered an I²C™ interface. Unfortunately, a resolution of 256 samples is inadequate for a number of measurements. The 12-bit ADC described in this short article has a resolution $\times 16$ or even $\times 64$ as high. This makes it a lot more convenient to read, say, the usual temperature sensors, such as the LM335, which output $10 \text{ mV } ^\circ\text{C}^{-1}$. With a 12-bit ADC and an internal reference voltage of 4.096 V, the resolution is 1 mV, which means that the sensor reading can be read in $0.1 \text{ } ^\circ\text{C}$. With an 8-bit converter, the resolution would be only $1.6 \text{ } ^\circ\text{C}$.

The program given below is written for the Matchbox computer a book about which, *Matchbox BASIC Computer* (ISBN 0 905705 53 X) is available from Elektor Electronics (Publishing).

When START is enabled, the program arranges for an interrupt per second to be produced, which means that a sample is taken every second. At the same time, the liquid-crystal display (LCD) is initialized. The final line sends the result of the print instruction to the LCD; if this and the penulti-



994018 - 11



Parts list

Resistors:

- R₁, R₃, R₅, R₇, R₉, R₁₁, R₁₃, R₁₅ = 1 kΩ
- R₂, R₄, R₆, R₈, R₁₀, R₁₂, R₁₄, R₁₆ = 10 kΩ but see text
- R₁₇ = 100 Ω
- R₁₈ = 1.5 kΩ

Capacitors:

- C₁–C₉ = 0.1 μF
- C₁₀ = 100 μF, 6 V, radial
- C₁₁ = 4.7 μF, 63 V, radial
- C₁₂ = 10 nF
- C₁₃ = 10 μF, 63 V, radial

Inductors:

- L₁ = 100 μF

Semiconductors:

- D₁ = LED, high efficiency
- D₂ = 1N4148
- D₃ = zener, 5.6 V, 1.3 W

Integrated circuits:

- IC₁ = MAX128BNCG (Maxim)

Miscellaneous:

- JP₁–JP₃ = 3-way jumper
- K₁–K₅ = 2-way terminal block for board mounting
- K₇ = 6-pin mini DIN socket for board mounting
- S₁ = push-button switch, 1 make contact
- PCB Order no. 994018 (see Readers Services towards the end of this issue)

mate line are ignored, the results are automatically passed to the monitor screen.

After initialization under START, the program is in an endless loop waiting for interrupts. When an interrupt arrives, a byte is sent to the ADC, whereupon the result (2 bytes) is read. Note that this means that the result must previously be declared as an array of two bytes. Subsequently, the cursor of the display is set to the correct position and the result is written to the LCD. The interrupt routine is ended with the instruction IRETURN.

There are two types of ADC: the MAX 127 and the MAX128. In the MAX127, the software allows an input range of 0–10, 0–5, ± 10, or ± 5 V, to be selected. In the MAX128, these ranges are 0–V_{REF}, 0–V_{REF}/2, ± V_{REF}, and ± V_{REF}/2.

The analogue-to-digital conversion is started by sending a byte to the converter: base address 50_H. Bit 7 must be 1, bits 6–4 determine which of the eight inputs is selected; bits 3, 2 determine which input range is chosen, and bits 1, 0 differentiate between active mode (current drain about 10 mA) and power down (current drain 700 or 120 μA respectively).

After the first byte has

been sent, the converter may be read by reading two bytes via the I²C. The first received byte is the most significant bit (MSB), and the four highest bits in the second byte contain the lowest significant bit (LSB). The four lowest bits are zero.

Datasheets for the MAX127 and MAX128 may be had via the internet: <http://www.maxim-ic.com>

The interface is best built on the printed-circuit board, which is available ready made (Order no. 994018) via the Readers Services—see towards the end of this issue.

A final note: if the inputs are used for voltages only, resistors R₂, R₄, R₆, R₈, R₁₀, R₁₂, R₁₄, and R₁₆, may be omitted.

[994018]

I²C is a trademark of the Philips Corporation.

Listing

```

; MAX128. MBL
; MAXI M 128 12 BI T A/D TEST
; 08/04/99 BY W

RESOURCE I I C-EEPROM 0100H BYTES @5000H
RESOURCE 8051-I RAM 10H BYTES @70H

BYTE RESULT[ 2] ; Array for I2C
BYTE CNTRL

START:
ON INT GOSUB CONVERSION
TIMER( 0, 0) ; Stop Timer
TIMER( 192, 4800) ; Start Timer 1s interval
SETBITS( INTena, TIMena) ; Enable interrupts and Timer interrupt
LCDSET ; Init LCD
FORMAT( LCD D U LENGTH=5 Z I ) ; Output to LCD, decimal, no sign, 5 digits

LOOP: ; Endless loop
GOTO LOOP

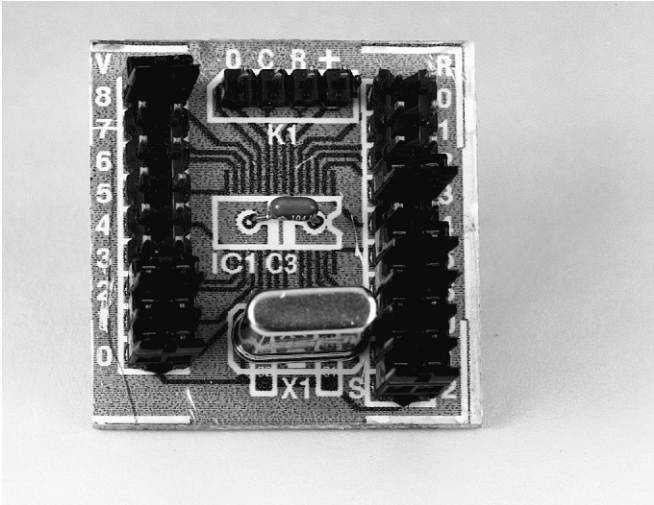
CONVERSION: ; Interrupt routine every 1s
CNTRL:=10001000B ; Start A/D conversion, input 0, 0..Vref
I I CWR( 01010000B, 1, CNTRL) ; Write to A/D
I I CRR( 01010000B, 2, RESULT) ; Read two bytes (msb & lsb)
LCDCOM( 128) ; Position cursor LCD
PRINT( RESULT[ 0] * 16+RESULT[ 1] / 16) ;

CLEARBITS( TIMnt) ; Reset timer interrupt flag.
IRETURN ; Return from timer interrupt

END

```

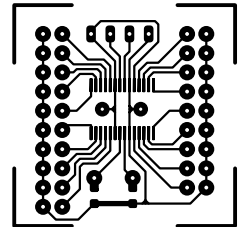
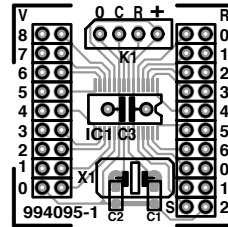
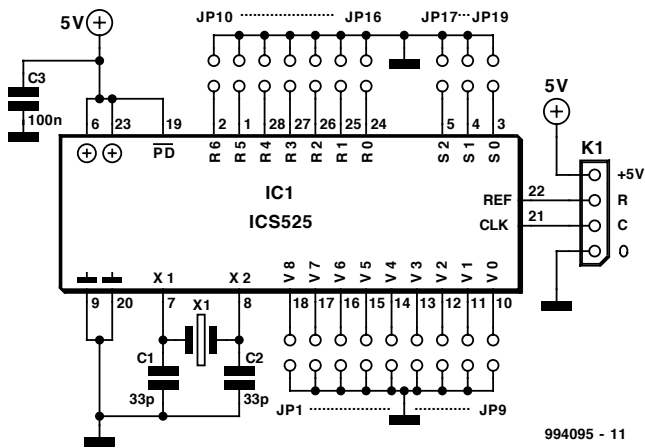

configurable clock generator 021



crystal frequency may be manipulated are set with pins, something that in most other similar ICs has to be done via a serial protocol and the aid of an additional processor.

In the diagram, the manufacturers' numbering of the jumpers given in the datasheets has been retained. The position of the jumpers for various combinations of input and output frequencies may be obtained via the Internet or by fax request. The table shows an example of how a 12 MHz clock may be converted to a 24.576 MHz one with 0 ppm error. Of course, not all combinations of input and output frequencies are error-free. If, for instance, the input for the 25.576 MHz clock is changed to 10 MHz, the error is not less than 34 ppm. Clearly, it pays to try out a number of different crystal frequencies.

The generator is best built on the printed-circuit board shown, but this is not available ready made. The IC and surface-mount technology (SMT) capacitors C_1 and C_2 should be soldered at the track side of the board. Since capacitor C_3 is at the component side



Parts list	Clock)
Capacitors: $C_1, C_2 = 33$ pF SMT ceramic $C_3 = 0.1$ μ F ceramic	Miscellaneous: $X_1 =$ crystal (see text) JP_1 - $JP_{19} =$ 2-way jumper $K_1 =$ 4-way header
Integrated circuits: $IC_1 =$ ICS525-01R (Micro-	

H. Bonekamp

MicroClock have available 28-pin a generator IC Type ICS525, also called OSCaR (acronym for oscillator replacement), which may be used to replace virtually any kind of clock oscillator. The range of operation is wide although extensive hardware and/or software is not needed. The multipliers and divisors with which the

of the board exactly opposite the IC, it is best to mount the capacitor first and then the IC.

The generator draws a current of about 15 mA from its + 5 V supply.

[994095]

INPUT FREQUENCY = 12 MHz														OUTPUT FREQUENCY = 24.576 MHz									
S2	S1	S0	R6	R5	R4	R3	R2	R1	R0	V8	V7	V6	V5	V4	V3	V2	V1	V0					
PIN 5	4	3	2	1	28	27	26	25	24	18	17	16	15	14	13	12	11	10					
1	0	0	0	0	1	0	1	1	1	0	0	1	1	1	1	0	0	0					
ERROR ppm = 0.0																							

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auto switch for toilets 022

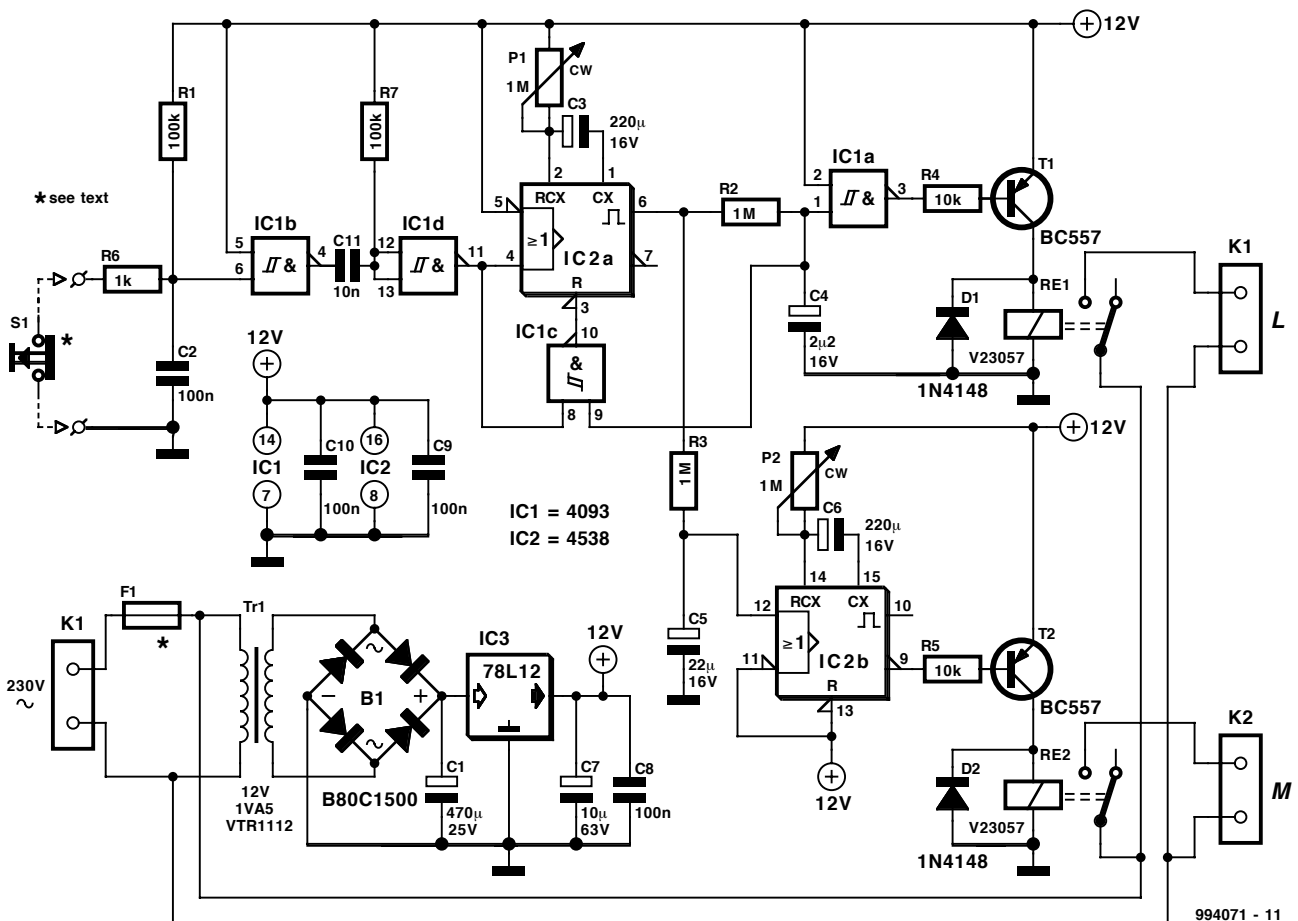


Design by L. Lemmens

The switch controls two relays, one, Re1, for turning the toilet light on and off, and the other, Re2, for turning an extractor fan on and off.

In the diagram, switch S1 is a reed switch fitted in the toilet door. A small magnet, fitted in the door post opposite the switch, ensures that the switch is closed when the door is shut. When the door is opened, the switch is opened also, whereupon the output of gate IC1b changes state (from low to high) so that monostable multivibrator (MMV) IC2a is triggered and inverter IC1d. During the mono time of the MMV, relay Re1 is energised via gate IC1a and transistor T1, whereupon the light is turned on. The maximum on time is set with preset P1.

The output of IC2a triggers a second MMV, IC2b, after a delay equal to the time constant R3-C5 (about 10 seconds). The second MMV energises relay Re2 via transistor T2, causing the extractor fan to be switched on. The mono time of IC2b is set with P2; it is, of course, advisable to make this rather longer than that of IC2a,



994071 - 11

COMPONENTS LIST

Resistors:

R1,R7 = 100k Ω
R2,R3 = 1M Ω
R4,R5 = 10k Ω
R6 = 1k Ω
P1,P2 = 1M Ω preset

Capacitors:

C1 = 470 μ F 25V radial
C2,C8,C9,C10 = 100nF
C3,C6 = 220 μ F 16V radial
C4 = 2.2 μ F 16V radial
C5 = 22 μ F 16V radial
C7 = 10 μ F 16V radial
C11 = 10nF

Semiconductors:

D1,D2 = 1N4148
T1,T2 = BC557
IC1 = 4093

IC2 = 4538
IC3 = 78L12

Miscellaneous:

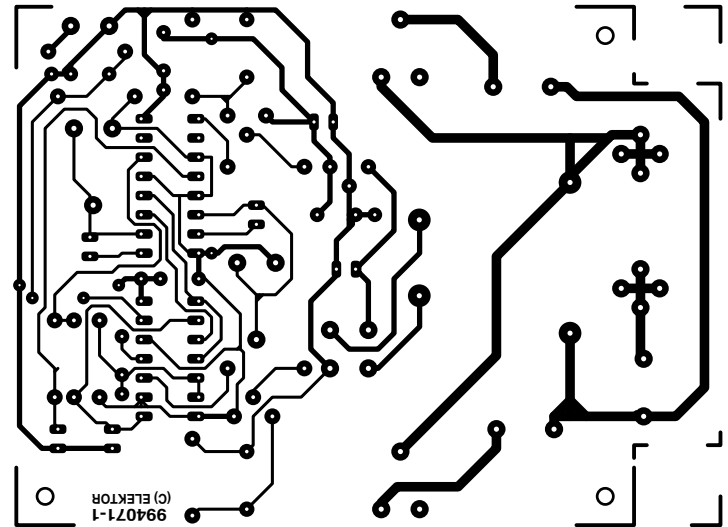
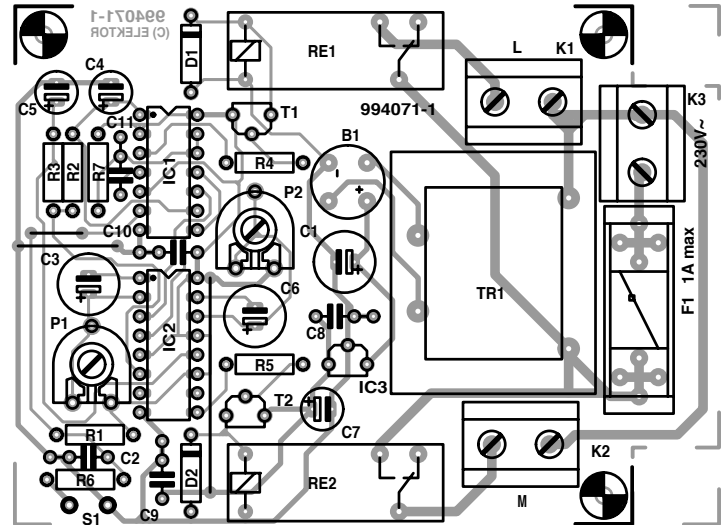
K1,K2,K3 = PCB terminal block, pitch 7.5mm
S1 = reed switch with magnet
B1 = B80C1500, round case
F1 = 1A fuse with PCB mount holder
Tr1 = mains transformer, 12V, 1.5A secondary, e.g. Block VTR1112
Re1,Re2 = 12V relay, 1 change-over contact, e.g., Siemens V23057-B0002-A101.
Enclosure: e.g. Sarel type IP55
PCB, order code 994071-1

to keep the fan working for some time after the light has been turned off.

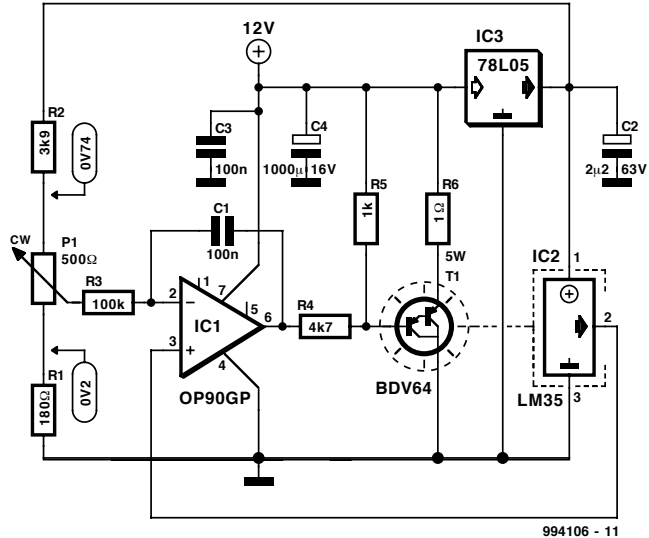
When the toilet door, and thus switch S1, is opened again, IC2a is triggered by a second leading edge and is reset, whereupon the light goes out. Network R2-C4 provides some delay in this, so that the person leaving the toilet is not immediately in darkness before the door is closed.

The control is best built on the PCB which is available ready-made through the Publishers' Readers Services (subject to availability). The completed board is best fitted in a plastic (ABS) case and fitted close to the light fitting in the ceiling or wall, where it may conveniently be linked to the mains via the existing wiring.

(994071-1)



temperature reference 023



H. Bonekamp

It is often difficult to properly calibrate a temperature sensor since there is no suitable aid for doing so available. This article, which describes a temperature reference source, aims at putting this right. Since the source is made variable, the reference temperature may also be used for adjusting thermostats correctly. This may prove useful in the case of the recently published Titan 2000 audio power amplifier.

The diagram shows how a Type BDV64 power transistor, T_1 , is used to provide a regulated-heat source and a calibrated sensor Type LM35 (IC_2) monitors the resulting temperature. The two devices are mounted on a common heat sink. At the same time, good thermal coupling between IC_2 and the sensor to be calibrated is of paramount importance.

Circuit IC_1 functions as an on/off switch and actuates the power transistor (heater) when the temperature drops below the set value. The desired temperature is set with potentiometer P_1 . The better the thermal coupling, the smaller the hysteresis of the system.

The circuit operates as follows. The output of IC_1 controls power transistor T_1 . The specified values of resistors R_4 and R_5

ensure that the current through the transistor is not greater than 0.5 mA. This results in a dissipation of not greater than 6 W.

Sensor IC₂ is powered by a regulated 5 V supply. Its output is a direct voltage of 10 mV °C⁻¹. With component values as specified, the temperature may be set with P₁ between + 20 °C and + 74 °C.

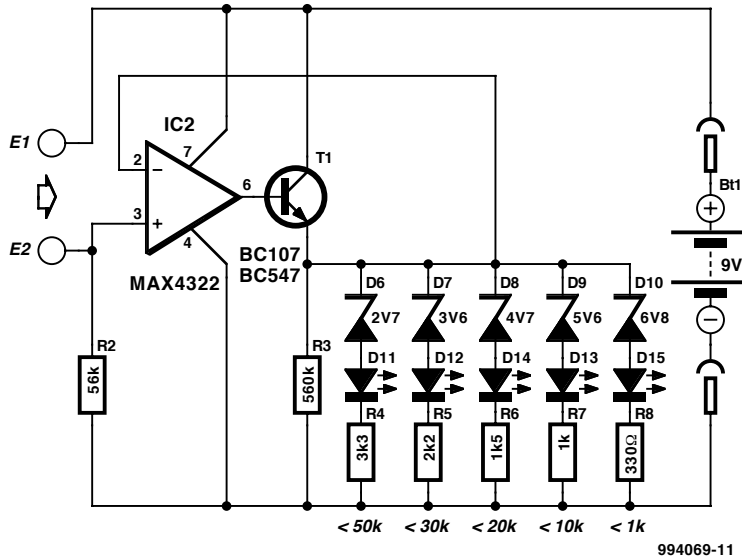
Given these data, it is fairly simple to construct a suitable scale for the potentiometer.

Almost any power transistor in a TO3P case and an amplification factor of ≥ 1000 may be used for T₁.

[994106]

multiple continuity tester

024



number of parallel-connected light-emitting diodes. Each LED is in series with a zener diodes and a resistor. The zener diodes have dissimilar zener voltages as shown in the diagram.

When the drop across R_2 exceeds the sum of base-emitter voltage of T_1 , a zener voltage, and the threshold voltage of the LED in series with that zener diode, the relevant LED lights. The diagram shows at which resistance value of the unit/component on test a particular LED lights. Bear in mind, however, that these values depend to some extent on the type of LED, and also that the zener voltages are subject to tolerances. Serious deviations

may be corrected by the addition of a standard diode or a Schottky diode. It is also possible to add branches to individual requirements, or to use a bar display instead of LEDs.

It is important that the op amp used has a rail-to-rail output since the input voltages as well as the output may rise to the peak supply voltage. This requirement is met by the MAX4322 as used in the prototype.

P. Lay

The continuity tester is a handy adjunct to an ohmmeter. The unit or component whose continuity is to be checked is connected between terminals E_1 and E_2 (which may be probes or croc clips). The test current then flowing through the unit/component on test causes a potential drop across resistor R_2 , which is applied to the non-inverting input of buffer IC₂. The output of the op amp is applied to transistor T_1 , in the emitter circuit of which there are

steep-skirted low-pass filter

025

T. Giesberts

When considering the design of a filter, one is inclined to think of a combination of inductors, resistors, and capacitors, perhaps in association with an active element. The filter in the diagram shows that a different approach is perfectly feasible.

The filter is based on a Type MAX7400CPA from Maxim. This IC, in conjunction with six capacitors, forms an elliptic, eighth order low-pass filter. It operates from a single + 5 V supply from which it draws a current of only 2 mA.

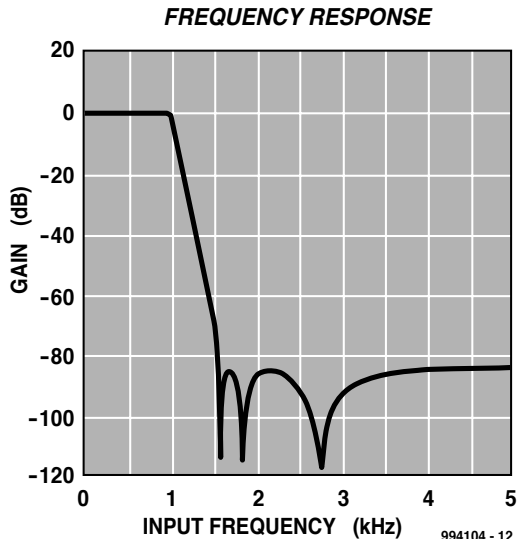
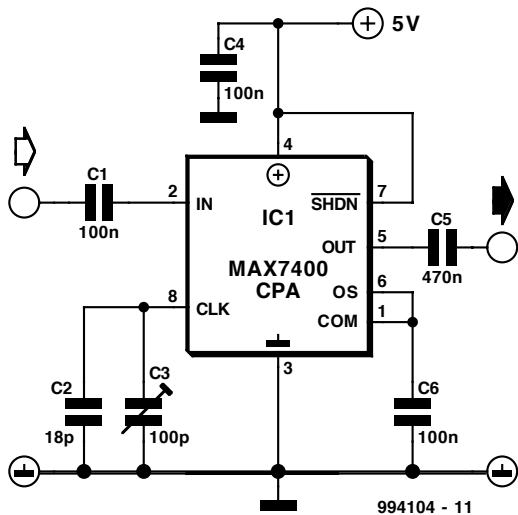
The cut-off frequency may be set between 1 kHz and 10 kHz and depends solely on the clock frequency used. The obtainable attenuation is, of course, of paramount importance. According to

the manufacturers' data sheet this is 82 dB: the frequency response diagram confirms this specification.

The IC may be provided with a clock signal in two different ways. The circuit as shown uses the internal oscillator, whose operating frequency may be adjusted, and cut-off frequency adapted, with trimmer C_3 . With component values as specified, the cut-off frequency may be set between 3 kHz and 10 kHz.

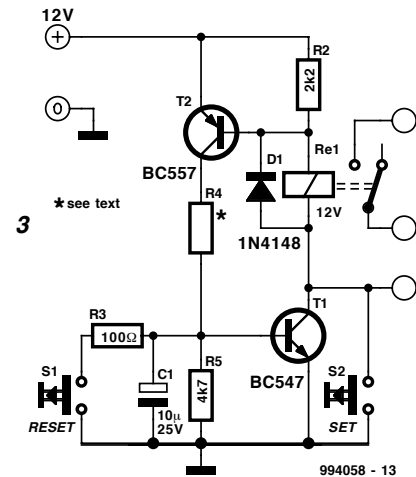
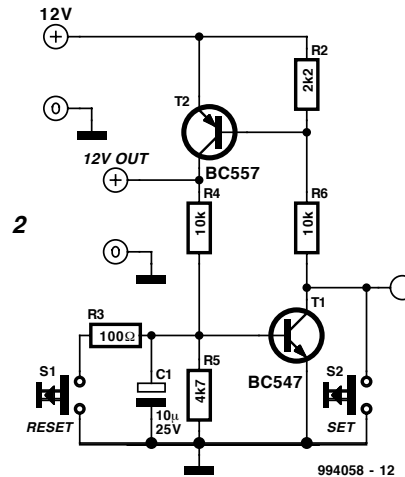
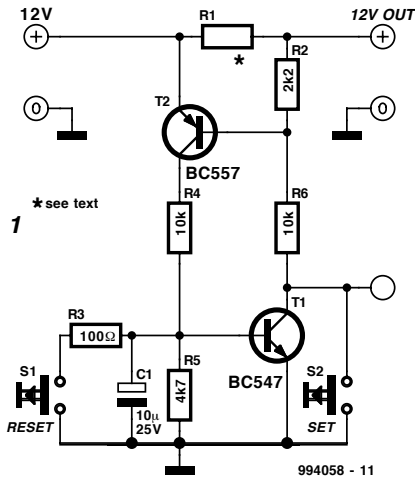
If it is necessary for the cut-off frequency to be set accurately, the IC may be provided with a stabilized clock signal via pin 8. The cut-off frequency is then equal to 1/100 of the clock frequency.

[994104]



transistor bistable

026



G. Böhme

The diagram in Figure 1 shows a well-known bistable circuit that is often used (without the switches) in protection circuits in various equipment. In the quiescent state, the bistable draws no current and is set only when the U_{BE} of T_2 is exceeded. At what level of current this happens is determined by the value of resistor R_1 . Both transistors are then on, so that the collector potential of T_1 goes to U_b , and that of T_2 to earth. The collector of T_2 then connects the control input of a device at output terminals PC₃, PC₄ to earth and thus in fact switches off the direct voltage.

Normally, it is assumed that the load current circuit must be opened before the bistable can be reset after an overcurrent. This is usually effected by a relevant switch contact or electronic device. It is, however, fairly simple to set and reset the bistable without interfering with the load circuit by placing the switch as shown. The switch only carries the control current of the bistable.

When the circuit is reduced to its essentials as shown in Figure 2, it becomes a general-purpose multivibrator that can provide a much greater current than a standard logic IC, provided suit-

able transistors are used. The multivibrator can work from a wide range of operating voltages. Capacitor C_1 ensures that the correct pulse/pause ratio is maintained at switch-on.

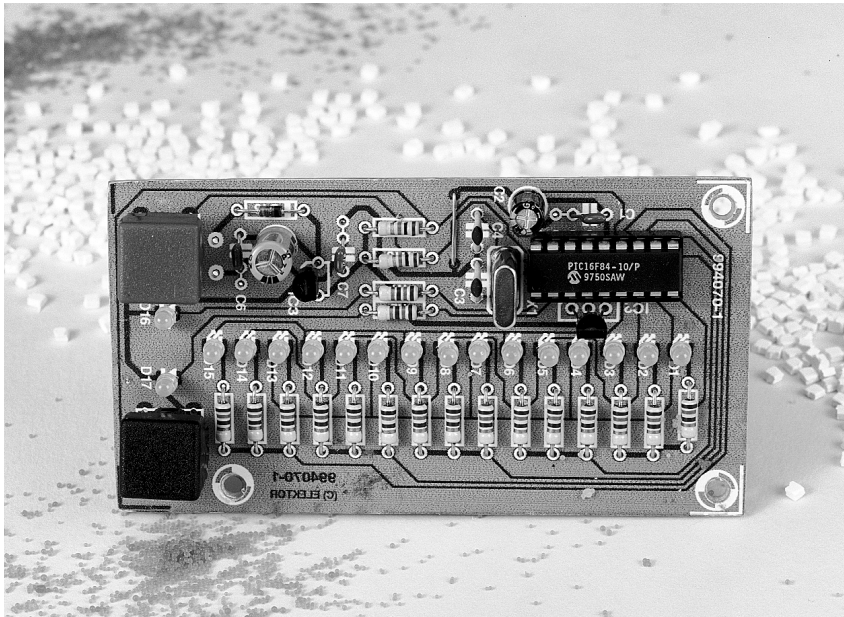
If R_3 is replaced by a relay solenoid, the circuit functions as a bistable relay which, after the circuit has been set with switch S_2 , remains stable until the bistable is switched off with switch S_1 . With other components as specified, the relay should have a high-resistance coil: 900–1000 Ω in the case of 12 V types, and around 3.5 k Ω for 24 V types. The value of R_2 should be of the same order, but it is not particularly critical.

If only a power relay with low-resistance solenoid is available, the transistors and resistors R_1 , R_2 , and R_4 , must be adapted to the current demand of the relay. Freewheeling diode D_1 may be a Type 1N4148 in case of a small relay, but when the relay current is greater than about 100 mA, it is advisable to use a Type 1N4001.

[994058]

minimum/maximum thermometer

027



U. Reiser

Although the diagram shows a simple circuit, the thermometer is capable of measuring temperatures with a resolution of 0.5 °C over a range of 30 °C. It also shows when the temperature measured falls outside the range and retains minimum and maximum measured temperatures. All this is made possible by microcontroller IC₁, a Type PIC16F84, and assembler programme

THER15. The device is available ready programmed from the publishers (Order no. 996514-1 – see Readers Services towards the end of this issue). Readers who wish to program the device themselves can obtain the source code on a diskette.

The temperature sensor is a Type SMT160, available from Smartec (www.hy-line.de/Sensor/), which does not, as is usual, output a voltage commensurate with the temperature, but a pulse-width modulated signal. This makes a separate analogue-to-digital converter unnecessary.

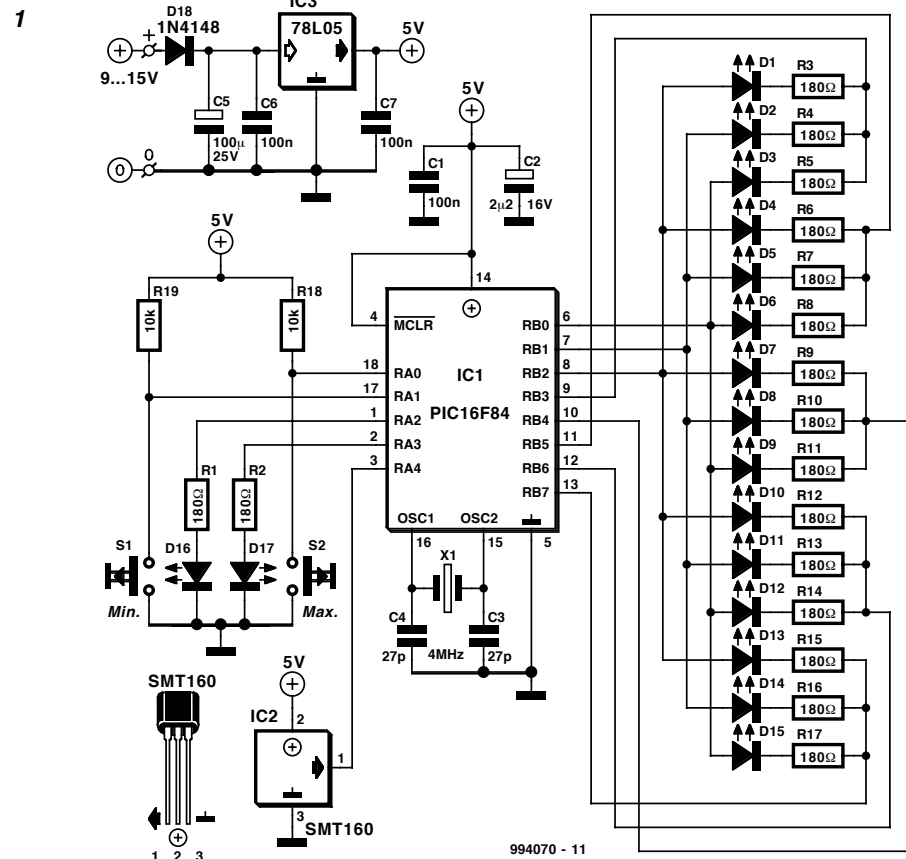
Only a PIC microcontroller with integral EEPROM can be used if minimum and maximum temperatures are to be retained. In the present design, a 15-way LED display, (D₁–D₁₅) is used to show temperatures in the ranges 0–15 °C and 16–30 °C. Which of these ranges is indicated by D₁₆ and D₁₇. The simultaneous lighting of two adjacent LEDs indicates a half degree between their two values.

The LEDs are multiplexed in five groups of three each, so that for the display of the temperatures only one port is needed. The change from one temperature to the next takes place at a frequency of 67 Hz. When a temperature below the range is measured, only D₂ lights; when the temperature is above the range, only D₁ lights.

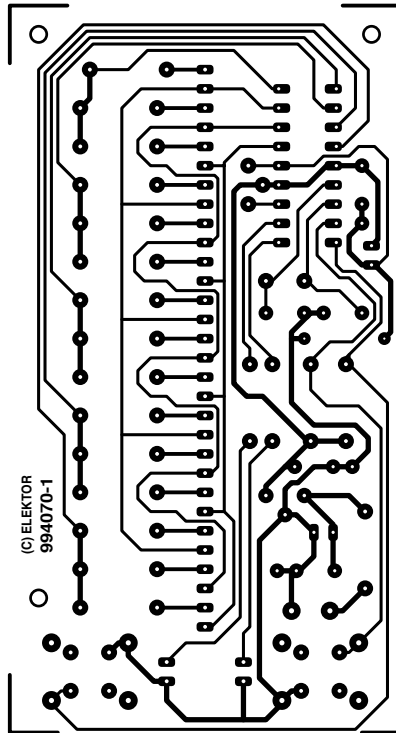
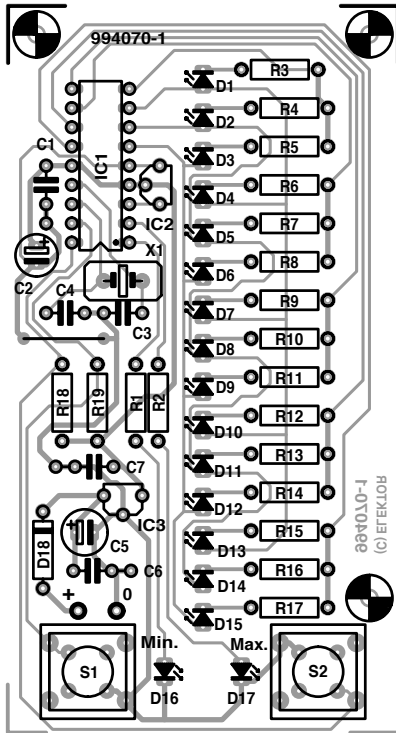
The stored minimum and maximum temperatures are displayed by the relevant LED when push-button switches S₁ and S₂ respectively are pressed. At the same time the relevant range LED lights. The minimum and maximum values can be erased by pressing (and holding) S₁ and then S₂ or S₂ and then S₁ respectively.

The circuit draws a current of not more than 25 mA (in case four LEDs light simultaneously). A 100 mA regulator is therefore perfectly all right. Power may be obtained from a suitable 8–12 V mains adaptor, but if low-current LEDs are used, a 9 V battery may also be considered. Note that the PIC cannot be used in the SLEEP mode since this would disable the minimum and maximum temperature memories.

The construction of the thermometer on the printed-circuit board in Figure 2 is straightforward. When purchasing the LEDs, make sure that their brightnesses are uniform; their colour does not really matter and is to individual taste. It is advisable to solder them in place last when the distance between the lid of the enclosure and the board has been established (since the diodes should just protrude through the lid).



[994070]



Parts list

Resistors:

R_1 – R_{17} = 180 Ω (if standard LEDs are used; value should be adapted when low-current LEDs are used)
 R_{18} , R_{19} = 10 k Ω

Capacitors:

C_1 , C_6 , C_7 = 0.1 μF
 C_2 = 2.2 μF , 16 V
 C_3 , C_4 = 27 pF
 C_5 = 100 μF , 25 V

Semiconductors:

D_1 – D_{17} = LED (see text)
 D_{18} = 1N4148

Integrated circuits:

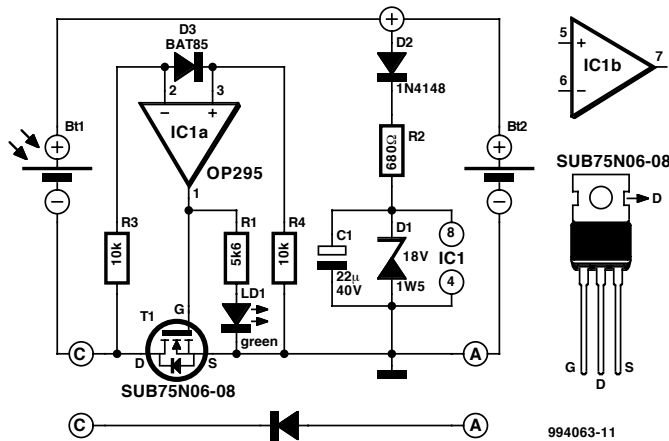
IC_1 = PIC16F84-10P (ready programmed Order no. 996514-1)
 IC_2 = SMT160 (Smartec)
 IC_3 = 7805

Miscellaneous:

S_1 , S_2 = push-button switch with make contact
 X_1 = quartz crystal, 4 MHz
 Diskette with source code, order code 996020-1

power diode for solar power systems

028



K-J Thiesler

Apart from the sun, solar power systems cannot work without a reflow protection diode between the solar panel and the energy store. When current flows into the store, there is a potential drop across the diode which must be written off as a loss in energy. In the case of a Schottky diode, this is not less than 0.28 V at nominal current levels, but will rise with higher ones. It is clear that it is advantageous to keep the energy loss as small as possible and this may be achieved with external circuitry as shown in the diagram.

The circuit is essentially an electronic switch consisting of a high precision operational amplifier, IC_{1a}, a Type OP295 from Analog Devices, and a MOSFET, T₁. This arrangement has the advantages over a Schottky diode that it has a lower threshold voltage and the

lost energy is not dissipated as heat so that only a small heat sink is needed.

When the potential at the non-inverting input of the op amp, which is configured as a comparator, rises above that at the inverting input, the output switches to the operating voltage. The transistor then comes on, whereupon light-emitting diode LD₁ lights. Diode D₃ clamps the inputs of IC_{1a} so that the peak input voltage cannot be greater than half the threshold voltage, provided the values of R₃ and R₄ are equal.

The op amp provides very high small-signal amplification, a small offset voltage, and consequent fast switching. The MOSFET changes from on to off state and vice versa at drain-source voltages in the microvolt range. In the quiescent state, when U_{DS} is 0 V, the transistor is on, so that LD₁ lights.

The operating voltage (C–A) may be between 5 V (the minimum supply for the op amp and the input control potential, U_{GS}, of the transistor) and 36 V (twice the zener voltage of D₁). Zener diode D₁ protects the MOSFET against excessive voltages (greater than ± 20 V). Diode D₃ and resistors R₃ and R₄ halve the potential across the inputs of the op amp. This ensures that operation with reversed or open terminals is harmless.

The substrate diode of the MOSFET is of no consequence since it does not become forward biased as long as the forward voltage, U_{SD}, of the transistor is held very low.

The on-resistance, R_{SD(on)}, of the transistor is only 8 mΩ and the transistor can handle currents of up to 75 A. When the nominal current is 10 A, the drop across the on-resistance is 80 mV, resulting in an energy loss of 0.8 W. This is low enough for a SUB type with a TO263-SMD case to be used without heat sink. When

the current is 50 A, however, it is advisable to use a SUP type with a TO220 case and a heat sink since the transistor is then dissipating 12.5 W. Even then, the voltage drop, $U_{SD} = 0.32$ V is significantly lower than that across a Schottky diode in the same circumstances.

Moreover, owing to the high precision of IC_{1a} , a number of transistors may be used in parallel.

The circuit proper draws a current of $150 \mu A$ when only one of the op amps in the OP295 is used. An even lower current is drawn by the alternative Type MAX478 from Maxim. However, the dif-

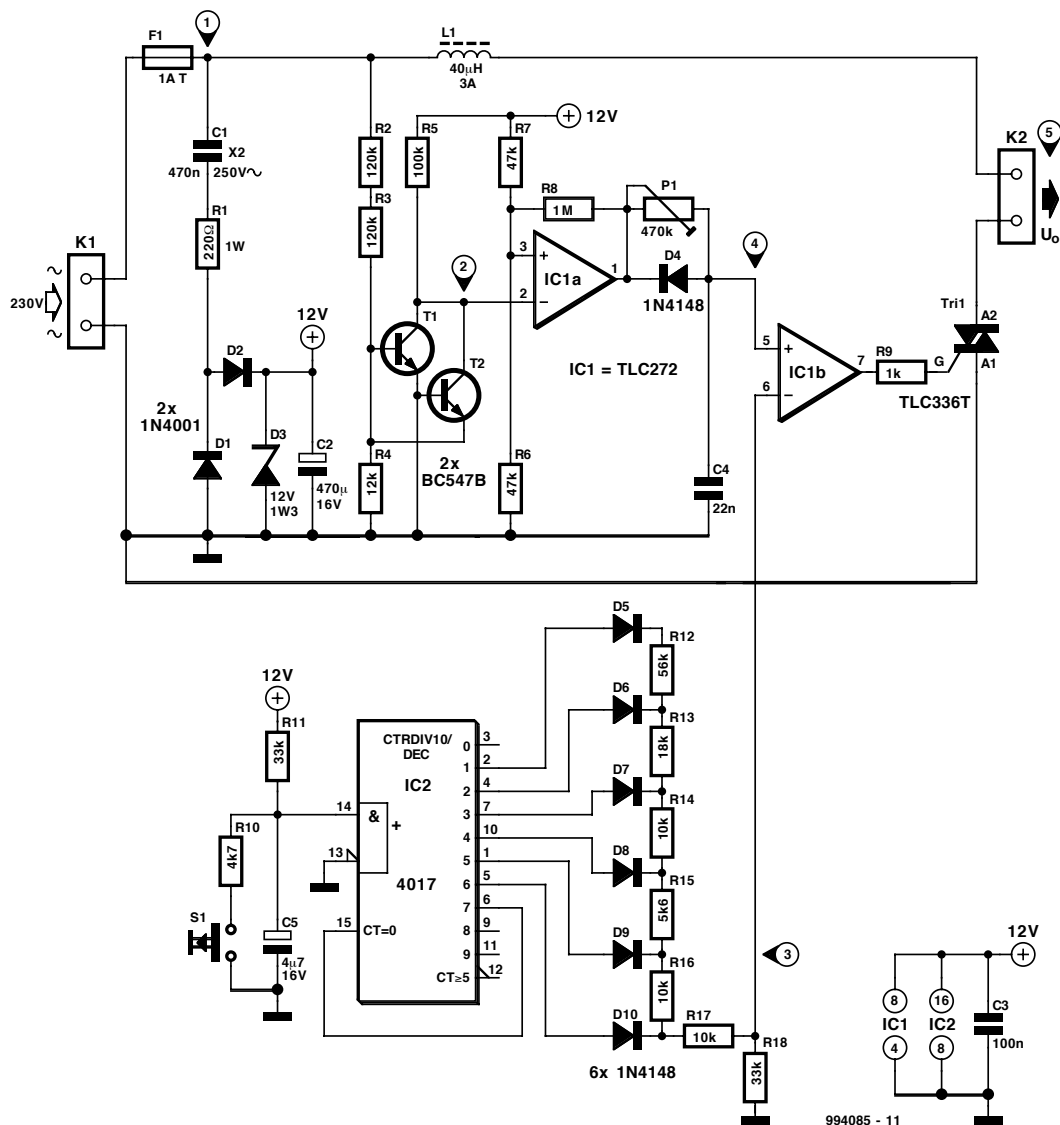
ferences between these two types are only relevant in the low current and voltage ranges. Both have rail-to-rail outputs that set the control voltage accurately even at very low operating voltages. This is important since the switch-on resistance of MOSFETs is not constant: it drops significantly with increasing gate potentials and decreasing temperature.

A experimental circuit may use an LM358 op amp and a Type BUZ10 transistors, but these components do not give the excellent results just described.

push-button dimmer switch

029

1



J. Graßmann

The present dimmer does not make use of the special integrated circuit for this purpose, the Type SLB0586, but, as the diagram shows, only of standard components. It consists of a power supply, a zero-crossing detector, a comparator with triac for phase gating (phase angle control), and a serial analogue-to-digital converter (ADC).

The power supply section does not use a transformer, but a capacitive potential divider, C₁-R₁-D₁, rectifier D₁-D₂, voltage lim-

iter (to 12 V) D₃, and charging cum decoupling capacitors C₂ and C₃. The 12 V direct voltage is used to power the other sections.

The zero crossings are detected by network R₂-R₅-T₁-T₂. Transistor T₁ is off when the level of the positive half wave of the attenuated mains voltage drops to about 12.6 V, that is, just before the zero crossing. Because of this, the potential at the inverting input of IC_{1a} (test point 2) becomes + 12 V, but rapidly returns to its original value when the emitter potential of T₂ becomes negative

with respect to earth. This results in short positive pulses around the zero crossing as shown in the timing diagram in Figure 2.

Additionally, the output pulses from IC_{1a} are inverted. Resistors R₆ and R₇ set the threshold potential to 6 V, while resistor R₈ provides some hysteresis. The inverter charges capacitor C₄ via P₁ after each and every zero crossing. During the zero crossings, the output of the inverter briefly goes low, but long enough for C₄ to become discharged rapidly via diode D₄. This results in the sawtooth-like voltage (waveform 4 in Figure 2) at the non-inverting input of comparator IC_{1b}.

The reference voltage for the comparator is provided by counter IC₂. Each time switch S₁ is pressed, the counter progresses one position. After the first time the switch is pressed, Q₁ is active (high), after the second time, Q₂, after the third, Q₃, and so on, until the seventh time when the counter is reset.

Network R₁₂-R₁₈-D₅-D₁₀ converts the counter position into an analogue output voltage, U_o:

$$U_o = R_{18}(U_b - U_d)/R,$$

where U_b is the supply voltage, U_d is the diode voltage, and R is the sum of all resistors interconnected by the counter output. The resistors have been selected to ensure floating transition between the various stages. For instance, at the fifth pulse,

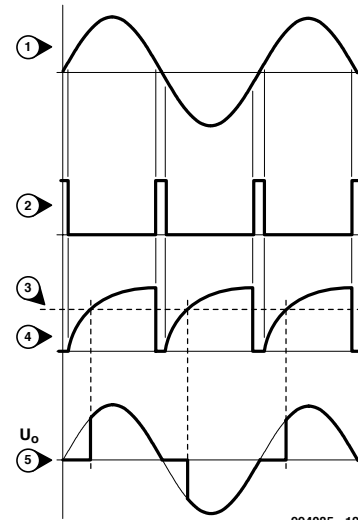
$$U_{o(5)} = R_{18}(U_b - U_d)/(R_{16} + R_{17} + R_{18}) = 7.1 \text{ V},$$

and at the sixth pulse,

$$U_{o(6)} = R_{18}(U_b - U_d)/(R_{17} + R_{18}) = 8.7 \text{ V}.$$

The higher the voltage, the shorter the part of the sawtooth above

2



994085 - 12

the threshold that turns on the triac. At U_{o(6)}, the output of IC_{1b} is low so that the load remains switched off. At U_{o(0)} (reference voltage), there is no phase gating at all. This may be set with P₁. The phase-gated mains voltage at connector K₂ is shown in the lowest waveform in Figure 2 (U_o).

Since there is no isolation of the mains voltage either during use or test, the dimmer must be housed in a well-insulated or plastic enclosure. Switch S₁ must be suitable for carrying mains voltage.

timer

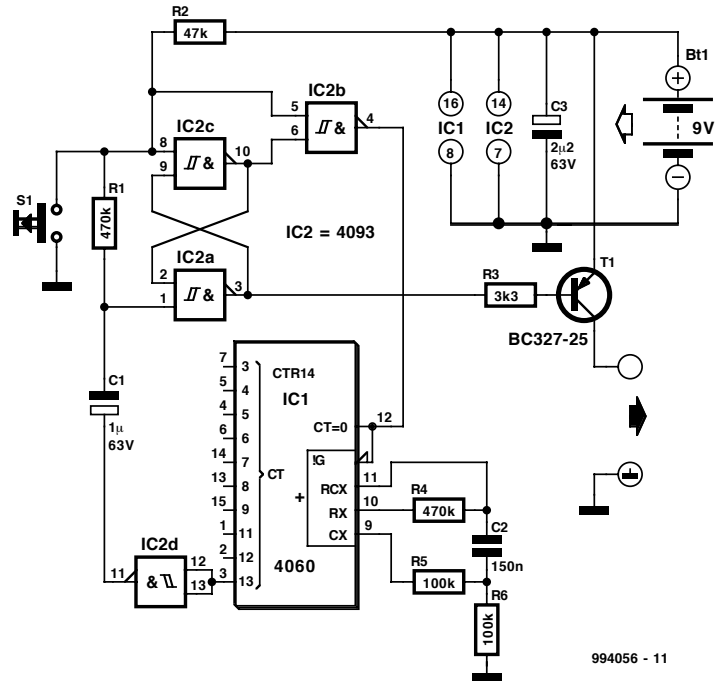
F. Rimatzki

The timer was designed for switching off a battery charger after a predetermined time to avoid overcharging. It may, however, be used for a number of other applications. It may be switched off before the predetermined time has elapsed and may later be retriggered by a simple push-button switch, S_1 . The circuit does not need any special components or parts. In the quiescent state, current drain is negligible.

The timer is switched on by briefly pressing switch S_1 . If the switch is then not touched again, the timer remains on for a period determined by time constant $R_4 \cdot C_2$. If during this period the switch is pressed again briefly, the period is started anew. If, however, the switch is pressed for a time exceeding time constant $R_1 \cdot C_1$ during the predetermined period, the equipment being controlled is switched off. This time constant may be adapted to individual requirements by altering the value of R_1 or C_1 .

The timing period ($R_4 \cdot C_2$) may be changed by altering the value of R_4 and/or C_2 . It must be borne in mind, however, that the value of R_4 must remain greater than that of R_5 and R_6 .

The slightly unorthodox configuration of the oscillator in IC_1 ensures that the polarity of capacitor C_2 does not change, so that an electrolytic type may be used here. With component values as specified, the 'on' time is six seconds per nanofarad of the value of C_2 . This means that when, for example, the value of this capacitor is $10 \mu F$, the 'on'



time is more than 16 hours.

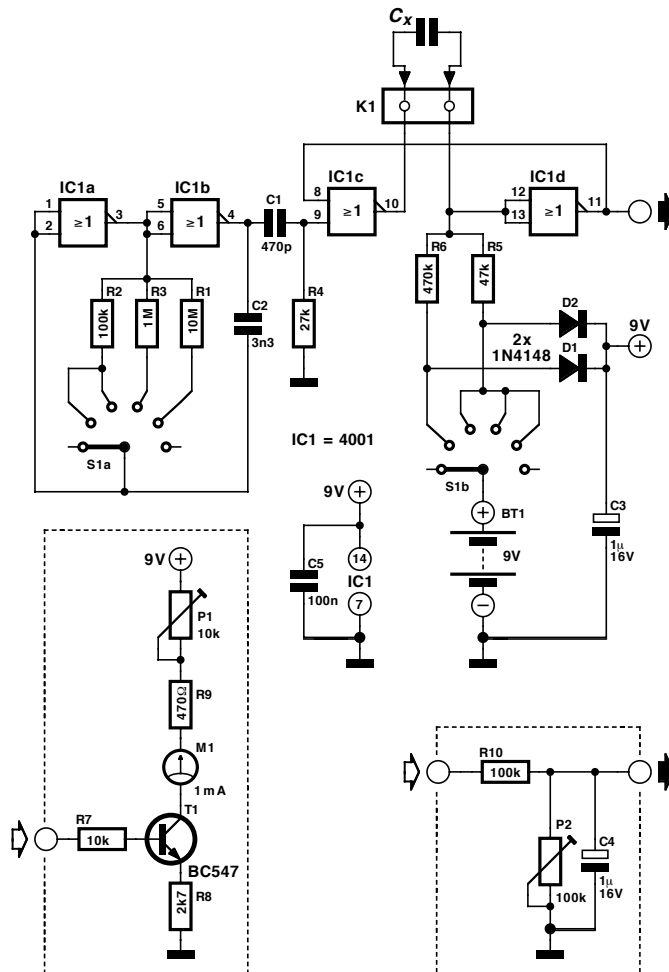
When the supply voltage is 9 V, the base current of output transistor T_1 is around 2.5 mA, which, for a voltage drop of only 0.1 V, results in an output current of up to 100 mA. If this is insufficient for a particular application, a different type of transistor may be used, or the BC327-25 followed by a relay or a MOSFET stage. If the output current is not required to be as large as stated, the value

of base resistor R_3 may be increased.

The supply voltage should be not less than 4 V, since the oscillator stops operating below 3.5 V. At a supply voltage of about 5 V, the base current of T_1 , and thus the output current, is rather smaller than stated. However, lowering the value of R_3 is not advisable, since the output of gate IC_{2a} is high-impedance.

capacitance meter

031



W van der Voet

The capacitance meter, which is attractive and easy to build, has five measurement ranges and allows the test result to be displayed on an analogue or a digital meter.

Gates IC_{1a} and IC_{1b} are arranged as an astable multivibrator (AMV), whose frequency is determined by capacitor C₂ and the resistor, R₁, R₂, or R₃, selected with switch S₁.

The output of the multivibrator is applied to a monostable multivibrator (MMV) formed by IC_{1c} and IC_{1d}. The pulses generated by the AMV appear in integrated form at the output of the MMV for a period of time determined by the capacitor on test, C_x, and the resistor, R₅ or R₆, selected with S₁. It follows that the pulse duration (width) at the output of IC_{1d} is directly proportional to the value of C_x.

The values of resistors R₁–R₆ enable five ranges to be selected with S₁, starting with 0–100 pF in position 1 to 0–1 μF in position 5.

The boxes in the diagram show two ways of displaying the measurement result. A standard BC547 transistor is capable of driving a moving coil meter, M₁, which may be calibrated with the aid of preset P₁. The other way is the use of a variable potential divider and integrator to which a digital voltmeter may be connected.

The meter is calibrated with the aid of a number of capacitors of accurately known value for each of the ranges. Set switch S₁ to range 1, connect one of the test capacitors (of relevant value!) across the test terminals and adjust P₁ or P₂, as the case may be, until the meter reading coincides with the value of the capacitor.

The accuracy of the meter is, of course, dependent on the tolerance of the resistors, which should therefore be 1% in all cases.

Pascal for the MAX512

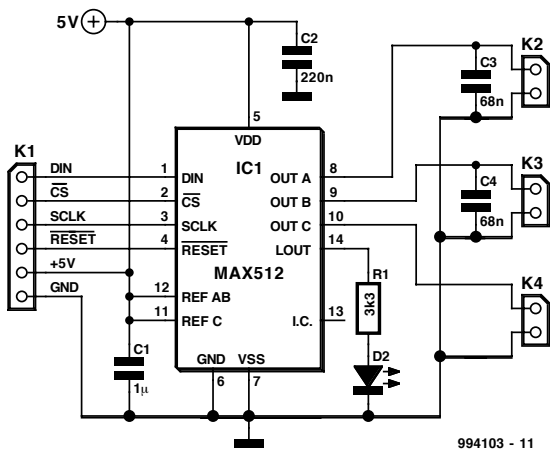
032

B. v. Berg

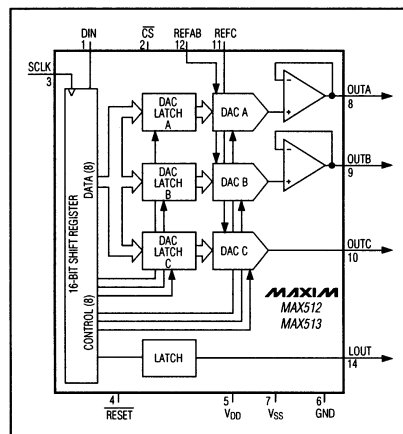
The MAX512 is a simple triple digital-to-analogue converter with a serial interface and a resolution of eight bits. Two of the three converters (DAC A and DAC B) provide a unipolar or bipolar buffered output voltage. Converter A can provide or sink currents of up to 5 mA, and B currents of up to 0.5 mA. Converter C is

intended for accurate applications and therefore has an unbuffered output. The reference voltages are applied separately (in contrast to the diagram) to converters A/B and C. Apart from the converter outputs, the MAX512 also has a digital output (1.6 mA) which, for instance, may be used for directly driving a high-efficiency LED.

The data is applied to the converter via a 3-wire interface. The interface operates with frequencies up to 5 MHz and is compati-



994103 - 11



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ble with standards such as SPI, QSPI, and Microwire.

The serial shift register at the input is 16 bits wide: eight data bits and eight control bits. The latter enable a converter to be selected or switched off. In the shutdown mode, the R2R network of the relevant converter is isolated from the reference source. The DAC registers may be charged at the leading edge of \overline{CS} either independently of one another or simultaneously.

The MAX512 may be operated from a single + 5 V supply or a symmetrical ± 2.5 V supply. It draws a current of about 1 mA and $< 1 \mu A$ in the shutdown mode.

The compact and well-documented Pascal program shows

clearly how one can work with the MAX512. Serial lines D_{IN} , Chip-Select, \overline{CS} , clock signal SCLK, and \overline{RESET} are then to be connected to ports P4.0–P4.3 of an 87537 processor, but other devices may also be used for controlling the process. It may then be necessary to adapt the port addresses at the start of the program.

After the program has been started, all three converters generate a five-step staircase voltage at a frequency of about 5 Hz. By introducing variations in the FOR loop that determines the length of the steps, the voltage steps may be altered. The software is available from the Publishers (Order no. 996022) but it should be noted that the commentary is in German. [994103]

```

(*****)
(*   Program      SERI_DAU.PAS           Ver si on:  1. 0       *)
(*   Aut hor s:   vom Berg / Gr o p p e   Dat e:  13. 04. 99   *)
(*****)

pr ogr am ser i _dau;

const      DI N = $E8;                    (* Serial data line on Port P40 *)
           CS = $E9;                      (* Serial Chip Select line on Port P41 *)
           SCLK = $EA;                    (* Serial Clock line on Port P42 *)
           RESET = $EB;                   (* Reset input of DAU on Port P43 *)

pr ocedur e ini t _dau;                    (* Bus line defaults *)

begi n
  set bi t ( CS );                          (* Off state of serial Bus: *)
  cl ear bi t ( SCLK );                      (* CS\=HIGH, SCLK=LOW, RESET\=HIGH *)
  set bi t ( RESET );                        (* and level of DI N does not matter! *)
end;

pr ocedur e r eset _dau;                    (* D/A converter basic settings *)
                                           (* clear *)

begi n
  cl ear bi t ( RESET );                     (* Pull Reset line to active state, *)
  set bi t ( RESET );                       (* to load all registers with their *)
end;                                        (* default values! *)
pr ocedur e r ausby tes ( cont rol , dat a : by t e ); (* Serial transmission of 2 Bytes, *)
                                           (* always MSB first, LSB last *)

var PEGEL, TEI LER, i : by t e;

begi n
  cl ear bi t ( CS );                         (* Start condition of serial Ds, CS=LOW *)

  Teil er := 128;                            (* Mask, with 1st iteration for MSB *)
  for i := 1 to 8 do                          (* Loop for transmission of *)
    begi n                                    (* first 8 data bits (Contr. Byte) *)
      PEGEL := cont rol and TEI LER;          (* Mask off other 7 Bits *)
      if ( PEGEL >= 1 ) then set bi t ( DI N ) el se cl ear bi t ( DI N );
      set bi t ( SCLK );                      (* Depending on bit level, build data line *)
      cl ear bi t ( SCLK );                  (* and apply clock pulse to clock line *)
      TEI LER := TEI LER di v 2;             (* New mask! *)
    end;
end;

```

```

Teiler := 128;
for i:=1 to 8 do
  begin
    PEGEL:=data and TEILER;
    if (PEGEL>=1) then setbit(DIN) else clearbit(DIN);
    setbit(SCLK);
    clearbit(SCLK);
    TEILER:=TEILER div 2;
  end;

  setbit(CS);
end;

procedure treppe(kanal:byte);
var
  kontrollbyte:byte;
  i:byte;
begin
  case kanal of
    0: kontrollbyte:=%00001111;
    1: kontrollbyte:=%00110001;
    2: kontrollbyte:=%00101010;
    3: kontrollbyte:=%00001100;
  end;
  for i:=0 to 4 do
    rausbytes(kontrollbyte, (i*50));
  end;
begin
  reset_dau;
  init_dau;
  repeat
    treppe(0);
  until false;
end.

```

```

(* Mask, with 1st iteration for MSB *)
(* Loop for transmission of *)
(* second 8 data bits (Data Byte) *)
(* Mask off other 7 Bits *)

```

```

(* Depending on bit level, build data line *)
(* and apply clock pulse to clock line *)
(* New mask! *)

```

```

(* Stop condition of serial Ds, CS=HIGH *)

```

```

(* Generate sawtooth on channel: *)
(* 1->channel A, 2->channel B, 3->channel C or *)
(* 0->on all three channels! *)
(* Aux. variable for channel info *)
(* Loop variable *)

```

```

(* Load all Registers, shut down none *)
(* Load Reg. A only, shut down channel B & C *)
(* Load Reg. B only, shut down channel A & C *)
(* Load Reg. C only, shut down channel A & B *)

```

```

(* Loop var. = 4 -> staircase w. 5 steps *)

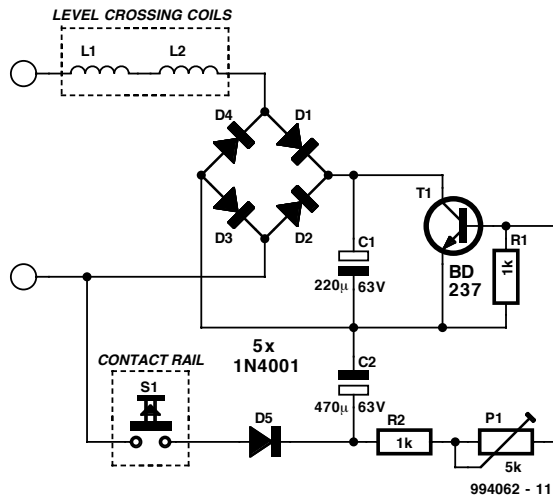
```

```

(* Reset serial D/A converter *)
(* Initialise serial D/A converter *)
(* Endless loop, create periodic staircase voltage *)
(* Show staircase on all three channels *)

```

railway barrier monitor 033



W. Heyn

The rails and wheels of railway carriages are liable to oxidizing no matter how carefully they are maintained. After a while this causes problems when the train moves across a level crossing since the

oxidization causes unreliable contacts of the relevant switches so that correct and timely closing of the barrier (lifting boom or traditional gate) does not take place. As long as the switch contacts are sound, the barrier closes rapidly and timely. This is ensured by the circuit in the diagram, which may be used with a variety of model railway systems.

When track switch S_1 is open, supply voltage for transistor T_1 is provided via rectifiers D_1 – D_4 . The transistor is off, so that no current flows and the barrier is open. When an approaching train closes the track switch, capacitor C_2 is charged slowly via diode D_1 . This results in the base voltage of T_1 rising from 0 V to 0.8 V, so that the transistor begins to conduct. Consequently, a gradually increasing current flows through the barrier solenoids, L_1 , L_2 , whereupon the barrier closes slowly.

When the switch contact is opened briefly, transistor T_1 remains on as long as the charge on, and thus the potential across, capacitor C_2 is sufficient. The barrier then remains closed. The time taken by C_2 to become discharged depends on the setting of P_1 .

When the train has left the relevant section of track switch, S_1 is opened, and capacitor C_2 is discharged via R_1 – P_1 – R_2 . The transistor is then cut off, capacitor C_1 is charged, and the barrier opens.

In the case of direct-voltage systems, diodes D_2 and D_4 are not needed.

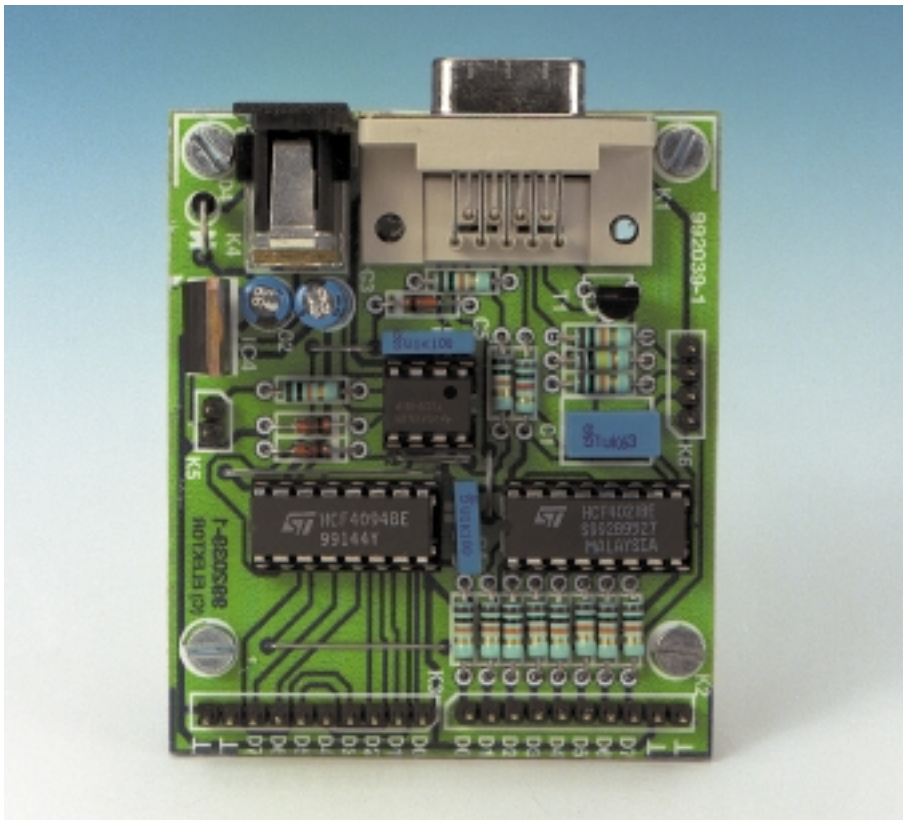
[994062]

An interface between the PC and the external world does not have to be complicated. This general-purpose Windows interface needs only three ICs, and it works directly from the serial interface. In addition to eight digital outputs and eight digital inputs, it has an analogue input and a frequency-measurement input. The project is complete with easy-to-use Windows software.

Design by B. Kainka

universal interface for Windows

making measurements with Uniface & Compact



The universal interface works directly from the PC's serial interface. It does not employ the asynchronous RS232 standard, but is instead operated under direct control of the serial interface lines. Since the COM interface of the PC has only three output and five

input lines, shift registers are used to transfer data serially. A data line and a clock line are necessary for each data transfer channel. Data transfers are not restricted to any given rate, so fast and slow computers can be equally well employed.

The software for the interface was originally written in Turbo Pascal, and could not be directly run under Windows. However, since starting out with the project, the author developed a solution for the Windows platform. The software and the interface described here a Windows 95/98/NTDLL that in principle supports the serial interface, the parallel or printer port, the joystick interface, the sound card and the video card. Here, we concentrate on serial communications.

Input and output shift registers

Figure 1 shows the schematic diagram of the interface. A 4094 CMOS shift register provides eight output lines. The PC can output eight data bits via the RS232 lines TXD (data) and DTR (clock), and then connect these bits to the outputs by applying a pulse to the RTS (strobe) line. The outputs can deliver up to around 5 mA and can directly drive LEDs via series resistors.

The type 4021 shift register makes eight input lines available for reading by the PC. A strobe pulse on the RTS line captures the states of the inputs, which are then read via the DCD line by a series of eight clock pulses applied to the DTR line. The inputs are protected against voltage surges by 10 kΩ series resistors. They have a high input impedance and exhibit random levels when left dis-

connected.

The simple and inexpensive A/D converter IC, type TLC549, is also addressed as a shift register. It provides its data via the DSR line. It provides an analogue input with a measurement range from 0 to +5 V, with eight-bit resolution. The analogue input is also protected against overvoltage by a 10 kΩ resistor.

The frequency-measurement input works via a small buffer amplifier connected to the CTS input line. The PC

COMPONENTS LIST

Resistors:

R1-R5, R8-R15 = 10kΩ
 R6 = 100kΩ
 R7 = 1kΩ

Capacitors:

C1 = 1μF MKT (Siemens)
 C2, C3 = 10μF 63V radial
 C4, C5 = 100nF ceramic

Semiconductors:

D1, D2, D3 = zener diode 4V7, 500mW
 D4 = 1N4001
 T1 = BC547B
 IC1 = TLC549CP or -IP (Texas Instruments)
 IC2 = 4021
 IC3 = 4094
 IC4 = 7805 or LP2950

Miscellaneous:

K1 = 9-way sub-D socket (female), angled pins, PCB mount
 K2, K3 = 10-way SIL pinheader
 K4 = mains adaptor socket, PCB mount
 K5 = 2-way pinheader
 K6 = 4-way (2x2) pinheader
 PCB, order code 992039-1 (see Readers Services page)
 Disk, 'Compact' control software, order code 996034-1 (see Readers Services page)

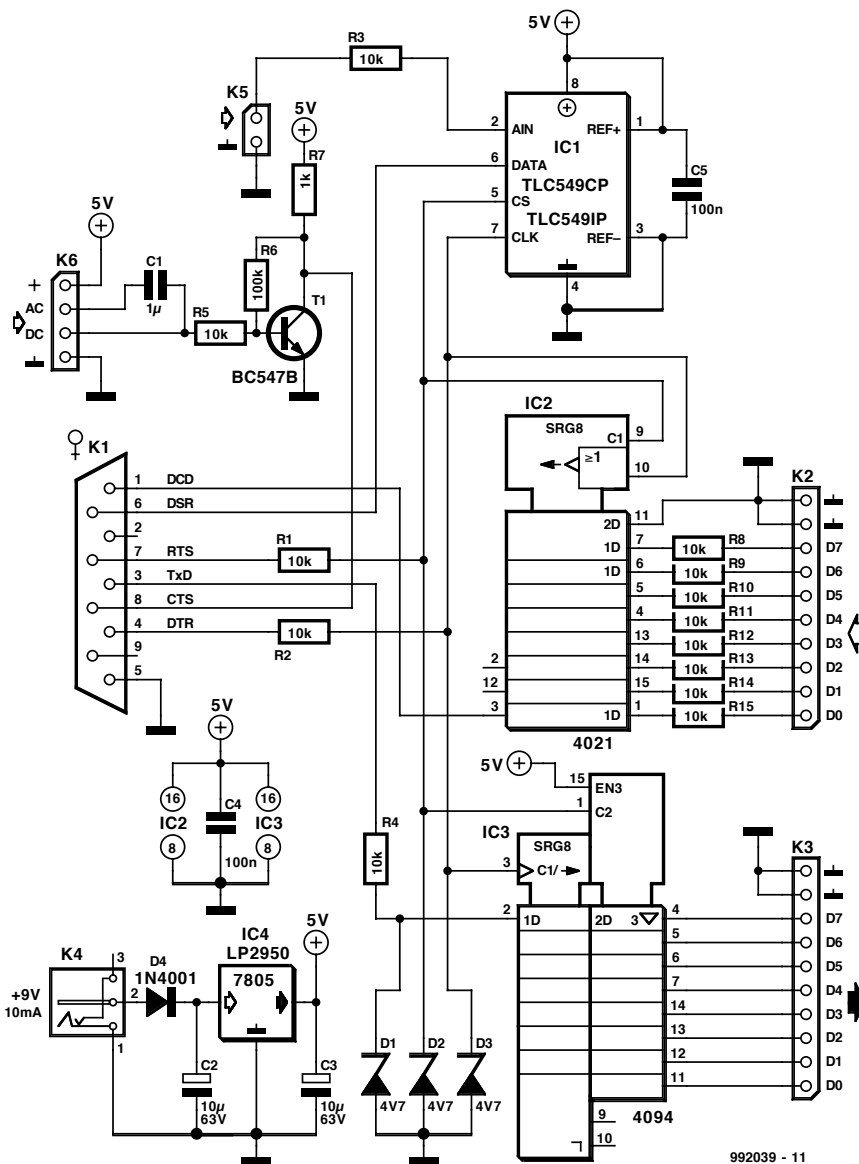


Figure 1. The Windows interface.

can directly read and count pulses. There is a d.c.-coupled input for static signals, pulse-length measurements and low-frequency measurements.

There is also an a.c.-coupled input for frequencies up to around 50 kHz. The highest measurable frequency is strongly dependent on the PC used.

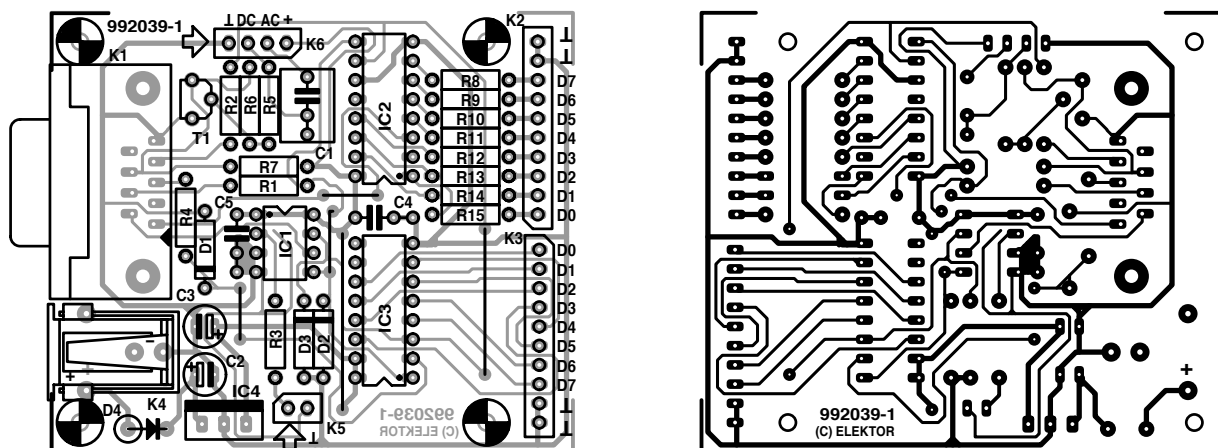


Figure 2. The printed circuit board.

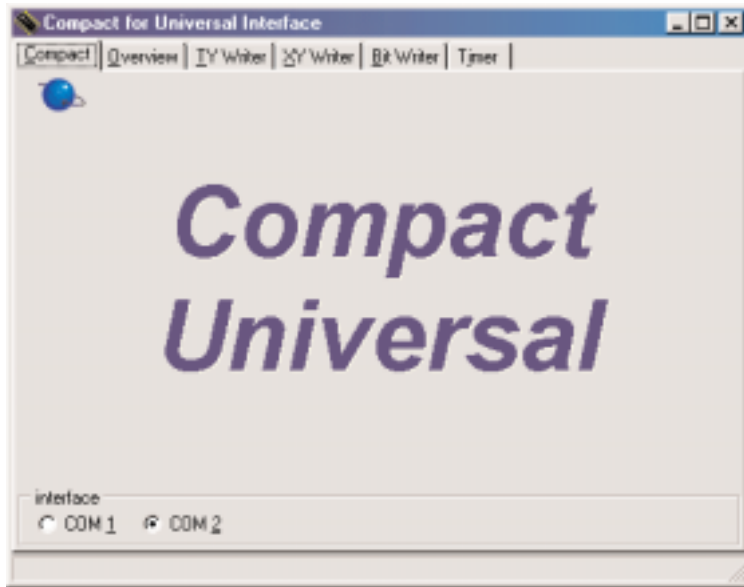


Figure 3. The Compact Universal program.

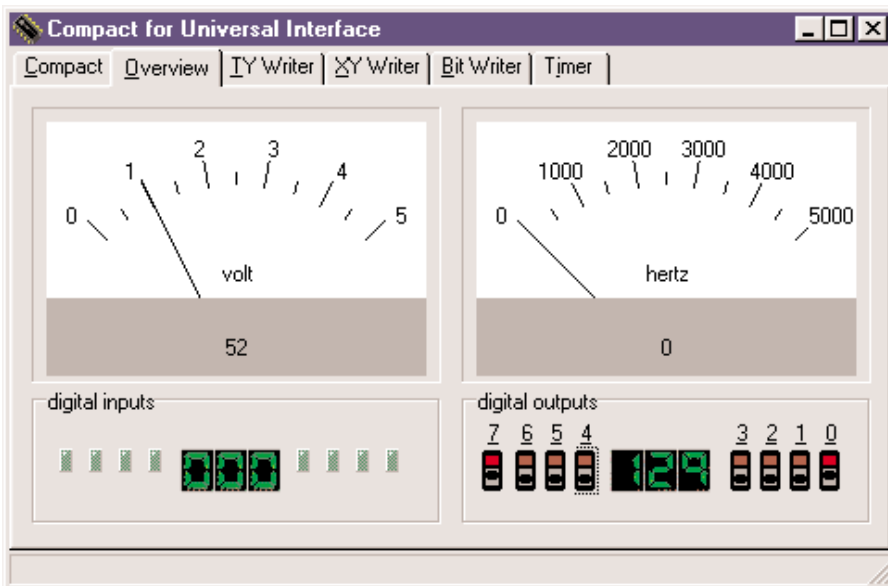


Figure 4. All inputs and outputs displayed directly.

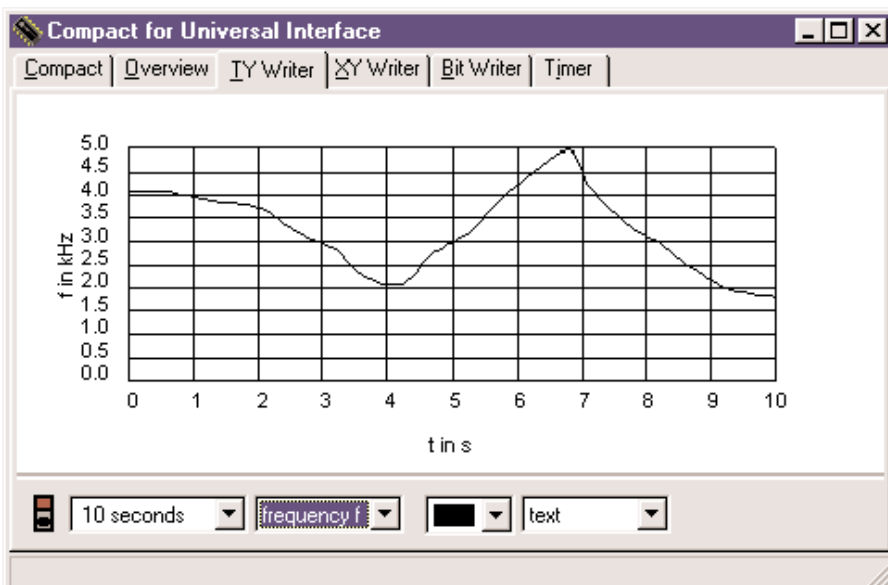


Figure 5. The measured value plotted versus time.

With a 200-MHz Pentium, 5 kHz can be reliably achieved under Windows 95. The program 'Compact' can display frequencies up to 5 kHz. With faster PCs, or if the measurements are made under DOS, significantly higher frequencies are possible.

Power is provided by a simple mains adapter having an output voltage of 9 to 12 V, combined with a 5 V regulator IC on the board. A diode connected to the power input jack protects against reverse-polarity connections. **Figure 2** shows the copper track layout and component mounting plan of the printed circuit board. The construction of the board should not present any difficulties.

Compact: a universal measurement program

A versatile application program, called Compact, has been developed for general use in the electronics lab. It is available in English, German, French and even Dutch-language versions. It drives all inputs and outputs of the interface and allows measurements to be taken in a flexible manner. The user can choose the COM port upon starting the program. The simplest and least expensive way to obtain Compact is undoubtedly by downloading it from Elektor's Internet home page (www.elektor-electronics.co.uk). This will be possible as of 1 December 1999.

After the program is started, a menu with several options appears (see **Figure 4**). The **Overview** function provides the user with direct access to all inputs and outputs. The two analogue inputs, for voltage and frequency, are displayed as pointer instruments. Their values are also displayed digitally, which in the case of the voltage measurement means the value of the data byte provided by the A/D converter. Both instruments can be used directly for experiments and troubleshooting.

In addition to the analogue inputs, the operator has access to the digital inputs and outputs of the universal interface. The eight digital inputs are displayed in the form of virtual LEDs, and also digitally as a byte whose value ranges from 0 to 255. This allows the state of a digital circuit to be directly monitored. The levels of the digital output lines can be altered using virtual slide switches. A digital display shows the state of the combined output bits as a byte value.

The **TY Writer** function plots the magnitude of one or both of the analogue inputs versus time (see **Figure 5**). This simplifies the observation of time-vary-

ing values. The measurement interval can be selected within wide limits, ranging from 1 second to 24 hours. Possible applications include long-term measurements, such as recording the charge and discharge characteristics of battery packs. Weather observations using simple sensors are another possibility.

Measured analogue quantities are frequently mutually dependent. In such cases, the **XY Writer** function can be useful (see **Figure 6**), with which the voltage can be plotted against the frequency. This type of presentation is well suited for displaying frequency-response characteristics. The signal from a function generator is used to drive both the frequency-measurement input of the interface and the input of the circuit under test. The output signal from the circuit under test is passed through a measurement rectifier to the voltage input of the interface. The frequency range of interest can be manually scanned in order to generate the response characteristic. **Figure 7** shows the resonant circuit whose frequency response is displayed in **Figure 6**. It is possible to measure the resonant frequency and the Q factor of the inductor. This procedure is also suitable for indirectly measuring the value of the inductance, and for comparing the Q factors of coils having the same inductance.

The **Bit Writer** function implements a **logic analyzer** that is suitable for purely digital applications (see **Figure 8**). The states of up to eight digital signals can be directly observed over a selectable time interval. This function is helpful in troubleshooting digital circuits, for example. The eight digital inputs can be directly connected to up to eight test points in the circuit.

An additional useful function of the program is the **Timer** function. This provides precise time measurements of a pulse waveform connected to the CTS input. As shown in **Figure 9**, a switch connected to earth, with a pull-up resistor to +5 V, can also be connected to this input to make a manually-operated stop watch. The same circuit can be used to measure frequencies using a reed switch.

Programming

The Compact program is naturally only one of the possible applications of the universal interface. Many readers will surely find it interesting to drive the interface using their own programs. **Listing 1** shows in principle how this can be done. The procedure Swap is written

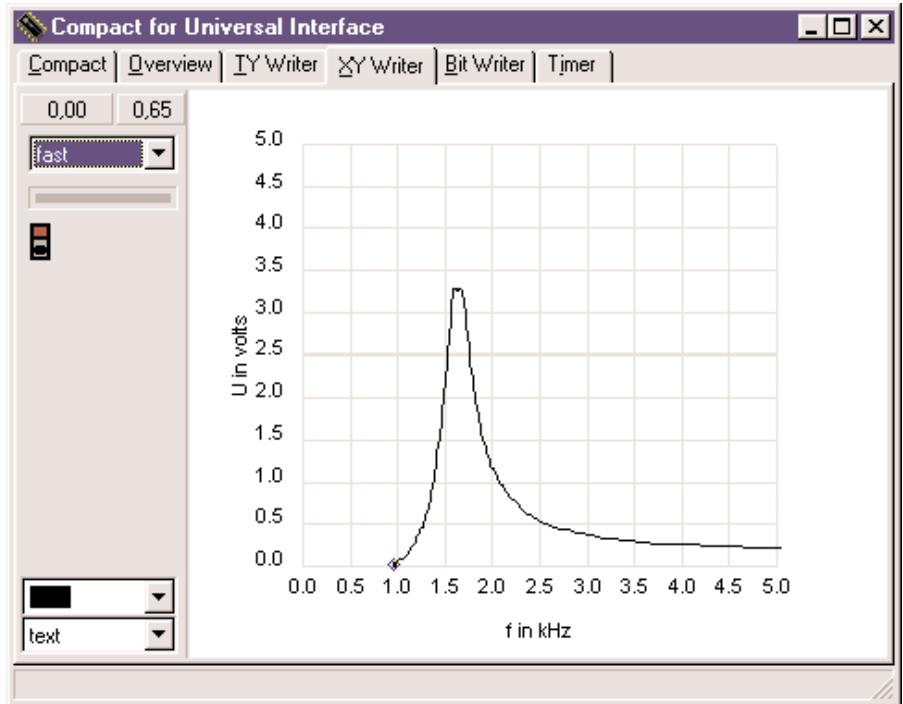


Figure 6. The XY Writer function, and the frequency-response characteristic of a resonant circuit.

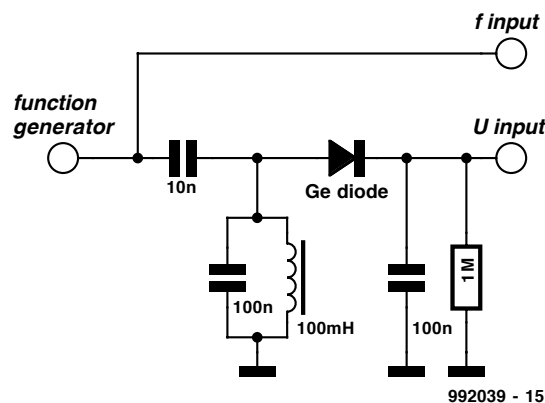


Figure 7. Many parameters of the resonant circuit can be determined using Compact.

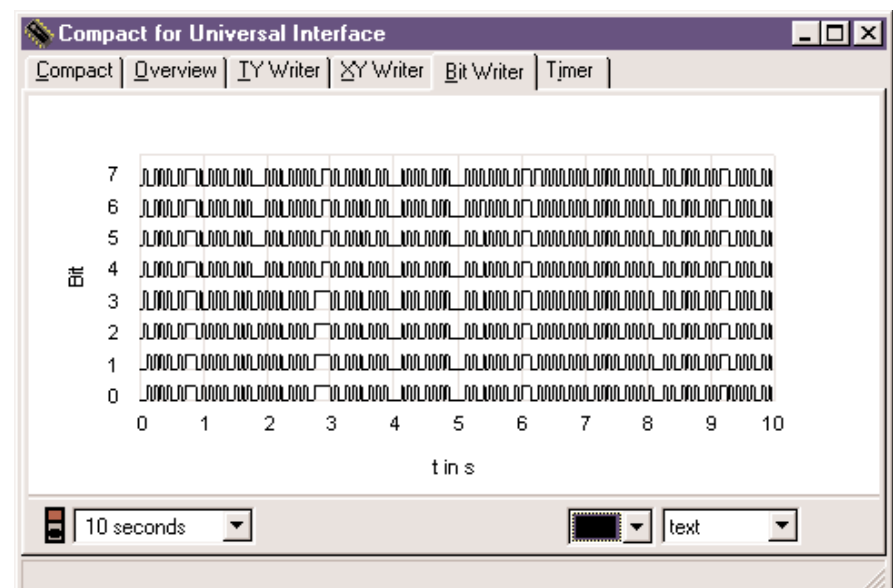


Figure 8. The Bit Writer function can be used as a logic analyzer.

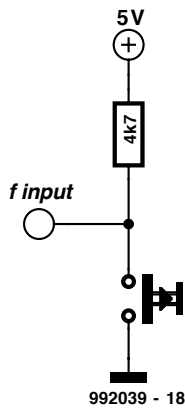


Figure 9. An input switch connected to earth.

in Delphi and services both shift registers and the A/D converter on the circuit board. Data are sent to the output register and read from the input register using the same clock signal. The procedure employs the three global variables Dout (output data for the 4094), Din (input data from the 4021) and Ain (the measurement value from the TLC549).

This program sample also illustrates the application of some important DLL functions to the serial interface. The code for PORTSDLL has been specially written by H. J. Berndt. The procedures TSD, DTR and RTS can be used for data outputs, and the procedures CTS, DSR, FI and DCD for data input. When the program is started, the interface must be opened using the command

```
OpenCom(pchar('com2: 9600, N, 8, 1')).
```

The interface parameters, such as the baud rate, are arbitrary. Nonetheless, OpenCom registers the usage of the interface with the Windows system. Without this, communication with the interface would not be possible.

The universal interface can of course also be operated under DOS. Listing 2 shows a suitable Turbo Pascal procedure. Access to the interface lines occurs here via direct port commands.

Additional applications

The interface can be used not only as a general-purpose laboratory instrument, but also for quite varied applications, including such things as running-light displays, experimental traffic-signal controllers, alarm installations and small weather stations.

The universal interface may also be used in a test system for automatic ver-

```

procedure Swap;
var Stelle, StelleAD, n, m : Integer;
begin
  RTS (1);           { Strobe on }
  Delayus(20);      { Delay }
  RTS (0);           { Strobe off }
  Stelle := 1;
  StelleAD := 128;
  Din := 0;
  Ain := 0;
  for n:=1 to 8 do begin
    if ((Dout AND Stelle) > 0) then
      TXD (1)       { output data }
    else TXD (0);
    if DCD = 1      { read data }
      then Din := Din + Stelle;
    if DSR = 1 then { read A/D }
      Ain := Ain + StelleAD;
    DTR (1);       { Clock on }
    Delayus(20);  { Delay }
    DTR (0);       { Clock off }
    Stelle := Stelle * 2;
    StelleAD := StelleAD div 2;
  end;
  RTS (1);           { Strobe on }
  Delayus(20);      { Delay }
  RTS (0);           { Strobe off }
end;

```

Listing 1. Sample Delphi driver program.

```

procedure Swap;
var Stelle, StelleAD, n, m : Integer;
begin
  Port [BA+4] := 2;           { Strobe on (RTS) }
  for m=1 to 10 do;          { Delay }
  Port [BA+4] := 0;           { Strobe off (RTS) }
  Stelle := 1;
  StelleAD := 128;
  Din := 0;
  Ain := 0;
  for n:=1 to 8 do begin
    if ((Dout AND Stelle) > 0) then
      Port [BA+3] := 64       { Output data (TXD) }
    else Port [BA+3] := 0;
    if (Port[BA+6] AND 128) = 128 { Read data (DCD) }
      then Din := Din + Stelle;
    if (Port[BA+6] AND 32) = 32 then { Read A/D (DSR) }
      Ain := Ain + StelleAD;
    Port [BA+4] := 1;         { Clock on (DTR) }
    Stelle := Stelle * 2;
    StelleAD := StelleAD div 2;
    Port [BA+4] := 0;         { Clock off (DTR) }
  end;
  Port [BA+4] := 2;           { Strobe on (RTS) }
  for m=1 to 10 do;          { Delay }
  Port [BA+4] := 0;           { Strobe off (RTS) }
end;

```

Listing 2. Sample DOS driver, using Turbo Pascal 6.

ification of digital ICs in the 4000 series. A special program generates bit patterns that are applied to the inputs of the IC under test, and also verifies the output states. Tables that describe the correct behaviour could be added automatically for other types of ICs. In

addition to the purely digital functions, the tester would then verify the current consumption to test for insulation faults.

(992039-1)

The fan runs constantly in many PCs, which may not even be necessary. A simple controller circuit can regulate the fan speed according to demand. This not only saves energy, it also reduces irritation from the fan noise.

Design by Joachim Holzhauser

PC fan speed controller

for a low-noise PC

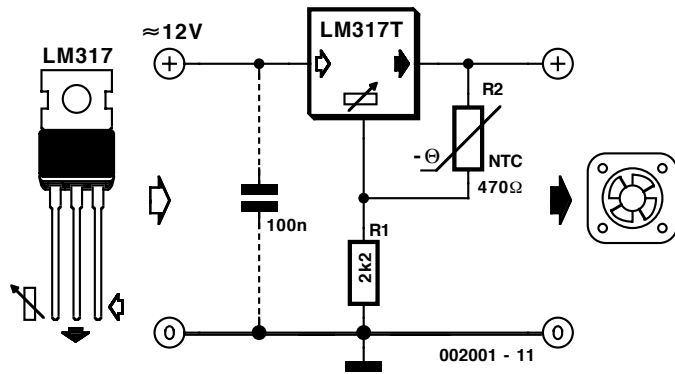
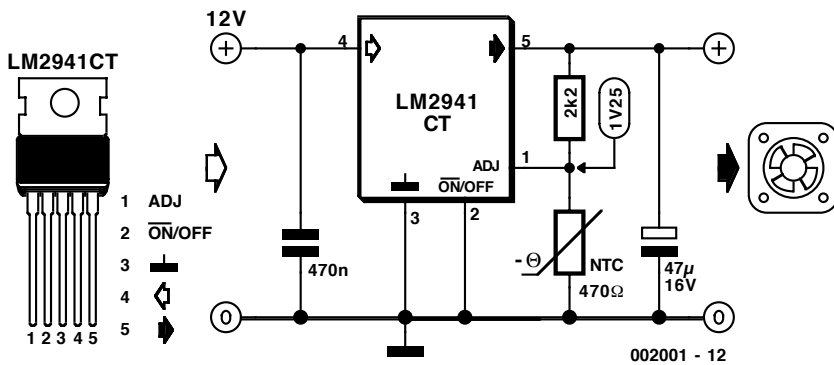


Figure 1. The fan speed controller can be built using a standard voltage regulator ...

Figure 2. ... or a low-drop voltage regulator.



Only three components are needed to allow the fan speed to be controlled according to the actual demand: one adjustable voltage regulator and two resistors that form a voltage divider. One of the resistors is a NTC thermistor (temperature-sensitive resistor), while the other is a normal resistor. If the 12-V power supply is not located close to the regulator, a decoupling capacitor is also required (see **Figure 1**).

The thermistor has a rated value of 470 Ω. It sets the output voltage of the LM317T to approximately 7 V at 25 °C. This should ensure reliable starting of the fan. If the temperature rises to roughly 40°C, the output voltage of the regulator reaches its maximum value and the fan runs at its maximum speed. The voltage drop across the regulator is at least 1.75 V for a motor current of (for example) 300 mA, and in any case 2 V at the maximum current level of 1 A. You thus might want to consider using a low-drop regulator, such as the National Semiconductor LM2941CT. To be sure, this increases the size of the circuit to a full five components, which are arranged as shown in **Figure 2**. However, this approach reduces the voltage drop to 0.2 V at 300 mA or 0.5 V at 1 A. By the way, low-drop voltage regulators are not available in a three-lead package.

The circuit can be constructed as a well-insulated 'free-standing' assembly, or it can be built on a small piece of prototyping board. In either case, it should be fixed to one of the mounting holes of the fan body (via the cooling tab of the TO-220 regulator package for the free-standing construction). The circuit board should be mounted out of the air stream, but the NTC thermistor must extend into the air stream.

(002001-1)

Anyone who overclocks the CPU of a PC lives in constant fear of having the processor fail due to overheating. A permanently-installed temperature monitor can do a lot to ease this fear.

Design by Dipl-Ing K Viemickel

CPU thermometer

overclocking without overheating

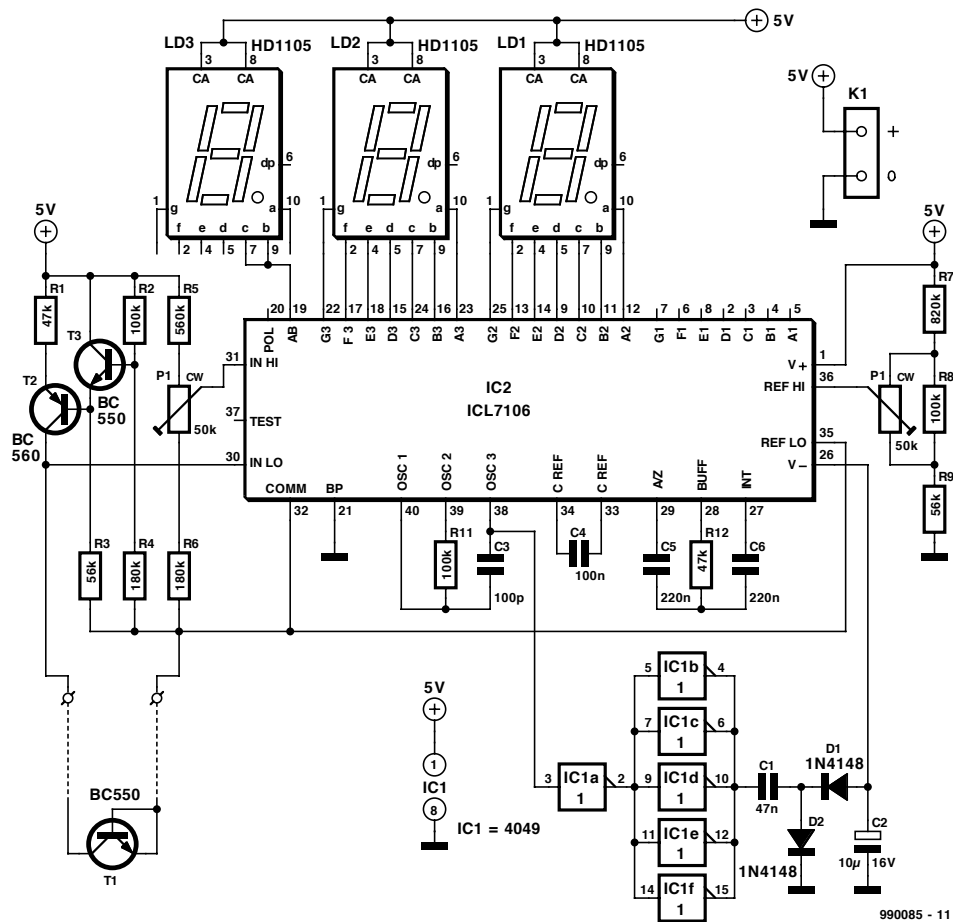


Figure 1. Schematic diagram of the CPU thermometer, showing the DVM IC and the sensor transistor T1.

If you want to coax a bit more speed out of a PC that's starting to show its age, you can try running the CPU and/or the peripheral components at a clock rate higher than that chosen by the manufacturer. This does not require soldering in a new crystal, but simply changing the positions of a few jumpers on the motherboard (typically arranged in two groups). One set of

jumpers selects the system clock rate (50, 55, 60 MHz and so on, for example), which applies to the entire chip set. The other set selects a multiplier (such as 1.5, 2, 2.5 and 3). The CPU clock rate is determined by the product of the system clock rate and the multiplier. The PCI bus can also benefit from such measures, since it operates at half the system clock rate. Since the

various components of the chip set, and PCI devices, are only suited to certain clock rates, you should try to keep the system clock rate 'acceptably' low and the multiplier as high as possible. For a description of how overclocking works and what you should bear in mind, see the article 'CPU overclocking' in the October 1997 issue of *Ektor Electronics*.

Better safe than sorry

A disadvantage of overclocking is that it increases the power dissipation of the CPU, which results in the generation of more heat. In order to maintain stable system operation, additional cooling of the CPU is not just recommended, but actually mandatory. If you go too far with overclocking, you risk thermal failure of the CPU, either immediately or in the (near) future. To avoid this, it is a good idea to monitor the temperature of the CPU IC. This is the task of the circuit described here. It works with a standard digital voltmeter IC (type ICL7107CPL), which can be found in any well-stocked electronics shop. The temperature sensor is the base-emitter junction of a transistor fitted in the CPU socket (Socket 7), directly underneath the processor IC. The schematic diagram in **Figure 1** shows that this transistor is connected between the IN LO and REF LO inputs of the DVM IC. It provides a voltage drop that is inversely proportional to

the junction temperature.

The ICL7107CPL needs a supplementary negative supply voltage for proper operation. This is provided by the combination of D1, D2, C1 and C2. The a.c. signal that this voltage doubler requires as an input is tapped off from the internal clock oscillator of the ICL7107 and buffered by IC1.

Now we come to the main attraction of the circuit. The DVM IC can directly drive an LED display, but it is not necessary to fit a new display into the computer. Instead, you can use the two- or three-digit clock frequency display, which is already present and which in most cases is totally useless. Remove and discard the existing connections to this display, and replace them with those shown in the schematic diagram. Before you do this, check that the LED display is the common-anode type. If it is not, you will have to replace the DVM IC with the pin-compatible version 7106CPL.

Two-point calibration

Before fitting the sensor transistor underneath the CPU IC, you must calibrate the circuit. Two trimpots are provided for setting the upper and lower calibration values. You can do without a calibrated thermometer by using ice water and boiling water as references. Wrap the transistor in plastic foil to prevent it from getting wet, and immerse it first in the ice water (0 °C). Adjust P1 so that the display indicates this value. Then perform the same adjustment with boiling water (100°C) and P2. Once the display is properly calibrated, you can fit the sensor transistor underneath the CPU IC. When the PC is operating with overclocking, the measured CPU temperature should not exceed a value of around 70 °C.

(990085-1)

There are many different ways to protect a computer against virus attacks. The electronic removable disk presented here is an especially reliable approach.

Design by H. Kraus

an electronic removable disk

virus protection using two hard disks

When a computer is used by more than one person, virus protection is doubly difficult. For example, if your offspring frequently install games or programs of obscure origin on your home workstation PC, it shouldn't take too long for viruses to start flexing their muscles in your computer and damaging important system files. Even if you diligently run a virus scanner or employ a boot manager, which allows an alternate

system to be booted from a different partition or drive, you cannot be assured of 100 percent protection. Seemingly, the only truly secure solution would be to use a removable disk. However, even this approach has a serious disadvantage, in that unintentionally switching off or swapping the disk while the system is running will unavoidably result in hardware and software faults.

The switch mechanism

A circuit for switching disks off line is described in the April 1999 issue of *Ektor Electronics*. This can naturally be used to switch between two hard disk drives, so that the computer can be booted from physically separate system disks. This circuit is ideal for older-model drives, but it does not work with new models. These communicate

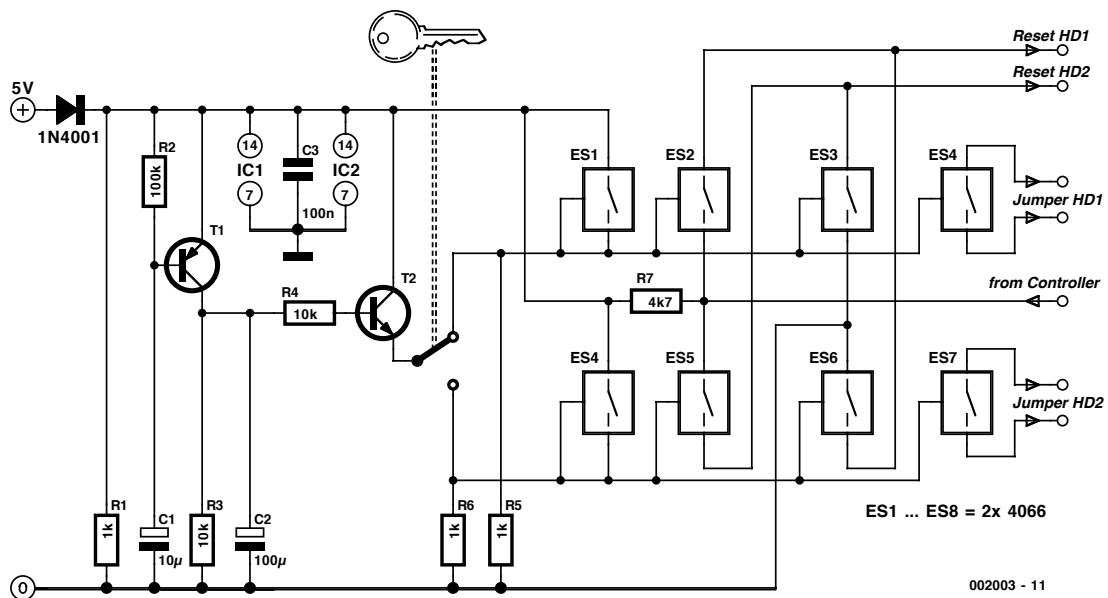


Figure 1. The power-on pulse enables one of the two hard-disk drives, depending on the position of the switch.

with each other via the $\overline{\text{DASP}}$ line, and this can cause the interface to lock up if a drive is switched off line. However, this problem can easily be solved by designating the off-line drive as a slave drive and breaking the $\overline{\text{DASP}}$ line between the drives. This works with all hard disk drives, drive controller boards and operating systems that have been tested by the author.

In addition, you must make sure that it is not possible to accidentally switch over the disks while the system is running, since this would result in a data catastrophe — a total loss of data.

The circuit described here fulfils two functions. The portion around T1 and T2 amounts to a sort of power-on reset circuit. Transistor T1 is normally blocked, since its base is connected to its emitter via R2. However, C1 charges via R2 when power is first applied, and the voltage drop across R2 switches T1 on for a short time. The full supply voltage is thus briefly applied to C2 during the power-up interval. The resulting power-on pulse is available at the emitter of T2, which has a low output impedance. This pulse can be connected to a key switch or an unused turbo switch (for example), as desired. The emitter resistors for T2, R5 and R6, also hold the control inputs of the electronic switches low when the mechanical switch is open.

Now we come to the second part of the circuit. The first two 4066 switches are latching, which means that they hold their states after the power-on pulse has occurred — either open or

closed, depending on the position of the switch. These two switches control the remaining three pairs of switches, which look after enabling and disabling the disk drives. Two pairs of switches enable the selected drive and place the non-selected drive off line, while the remaining pair of switches replaces the master/slave jumpers of the drives. The jumper assignments can usually be determined by examining the component labels on the drive's circuit board; otherwise, you will have to consult the manual.

Since the power-on circuit generates a

pulse only when the power is switched on, nothing will happen if the key switch is turned while the system is running. A disk changeover will only occur following the next hardware reset, or after the computer has been switched off and on again. As a final remark, note that either the two hard disk drives must be the same type and model, or the option 'MODE = AUTO' must be enabled in the BIOS for the primary master drive.

(002003-1)

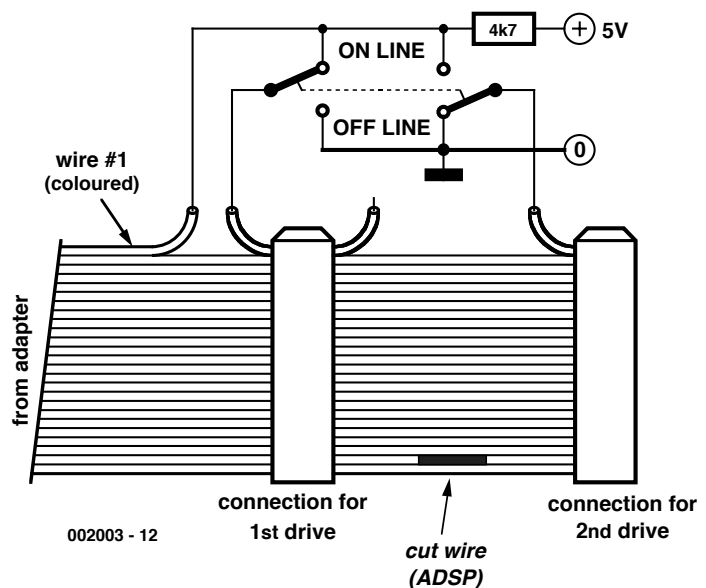


Figure 2. The $\overline{\text{DASP}}$ line must be cut.

Using the program discussed here it is possible to implement a general-purpose delay routine with any length between 26 and 281 processor cycles, at a resolution of one cycle.

By W. Couzijn

adjustable delay for PICs

a small but useful routine

If you want to implement wait cycles as part of a microcontroller programming job involving, for example, a Microchip PIC device, most of us would come up with a simple loop which is executed a predetermined number of times. Using this method you obtain delays whose length is always a multiple of three cycles, a resolution of one cycle being out of the question. By contrast, the routine presented here does offer an accuracy of one cycle within the range 26 to 281 processor cycles.

Tick

This routine will be particularly useful for simulating a USART (serial port) on smaller PIC controllers like the PIC12C508/509/671/672 and the PIC16C505. These devices do not have a built-in USART, although an internal RC oscillator is available. Mind you, the RC are external components! This oscillator comes in handy because it frees up two extra I/O pins while also avoiding the use of an (expensive) external quartz crystal. However, a problem arises if you want to generate a baudrate of, for example, 9600 bits/s because the on-board RC oscillator is subject to a tolerance of about 10%.

Fortunately, there's a simple trick to go round this problem. Let's assume a PC connected to the circuit sends data to the PIC in the application circuit. The bit times (i.e., periods) of the received data are then measured. Next, the results of the measurement are used to 'adjust' one of the delay routines in such a way that the same bit times are also employed for transmitted data. In this way, the PIC calibrates itself.

Structure

Two versions have been developed of

Call from the main program:

```
....  
MOVLW 50 ; Delay =50  
cycles  
CALL WAIT ; This line  
takes 50 cycles  
....
```

Assembly code version 1:

```
WAIT MOVWF BUFFER  
MOVLW 5  
SUBWF BUFFER, F  
WAIT1 SUBWF BUFFER, F  
BTFSF BUFFER, 0  
BTFSF BUFFER, 1  
GOTO WAIT1  
WAIT2 SUBWF BUFFER, F  
INCF STATUS, F  
GOTO WAIT2  
RETURN
```

the general-purpose delay routine. They work as follows.

The desired wait time (delay) is loaded into the working (W) register. Next, the routine called using a CALL instruction. The set delay includes the CALL and RETURN!

Version 1 of the routine is suitable for a delay of between 26 and 281 cycles, with all delays greater than 255 cycles are achieved by setting the desired delay as an 8-bit number. So, '0' for delay of 256 cycles, or '1' for one of 257 cycles, etc.). This routine consists of two loops. In the first loop, the program waits for a multiple of 5 cycles until the delay is divisible by four. Next, the sec-

Source code

Assembly-code version 2:

```
WAIT CLRF BUFFER  
SUBWF BUFFER, F  
MOVLW 12  
ADDWF BUFFER, W  
MOVWF BUFFER  
ANDLW 3  
ADDWF PCL, F  
INCF BUFFER, F  
INCF BUFFER, F  
INCF BUFFER, F  
INCF BUFFER, F  
MOVLW 4  
WAIT1 ADDWF BUFFER, F  
BTFSF STATUS, Z  
GOTO WAIT1  
RETURN
```

ond loop waits a multiple of four cycles. The routine eventually copies a 0 to the working register.

Version 2 offers an even shorter minimum delay, the available range being from 17 to 272 cycles. Here, again, 256 = 0, 257 = 1, etc.). The disadvantage of this version is the use of a calculated jump (ADDWF PCL) which is not executed properly by every PIC processor in every part of the memory. This should be taken into account!

(990086-1)

So far in this series of articles, we have looked at two areas of FPGA usage. Having looked at the design methodologies available to us, and the usage of FPGA design software, we are now in a position to consider the hardware implications of FPGA usage.

By Gordon Paddock



Atmel FPGA design course (3)

We saw in the first article that of the currently popular design methods, text based design entry, and in particular the usage of VHDL, is the most suitable approach for FPGA design. VHDL makes the design of reusable modules an easy and convenient way of handling external peripherals and functional blocks used in several designs, especially where there is a common base across projects.

The FPGA software seen in the previous instalment allows the assigning, or 'locking' of pins early in the design life cycle, with a high degree of confidence that the design will still be routable and able to meet the required timing criteria.

Also, by having timing analysis tools within the software, it is possible to locate critical timing paths and possible problems that would otherwise be impossible to resolve. Finally, with the availability of dynamic probes we can monitor in real time the internal behaviour of the device.

We now know that our designs will be functional when the bit-stream we create reaches the FPGA. But this raises one question: How do we get the bit-stream into the FPGA? And what other hardware implications are there in using an FPGA?

Data-to-FPGA

The FPGA has to be configured every time power is applied to the device from the 'off' state. In the Atmel AT40K family, this can be achieved in several ways.

Firstly, and probably currently the most popular method, is to use a serial EEPROM with an interface optimised for configuring the FPGA. This method requires a minimum number of inter-

connects between the FPGA and the EEPROM, but is the slowest method of configuration. For most applications, however, this is not a problem, as the configuration time is in the same order of time as a microprocessor reset. Serial EEPROMs have the advantage of taking very little board area, and are re-programmable in-system.

When a bitstream becomes exceedingly large, there may be an issue with configuration time. To get around this there are several other modes of configuration. These modes utilise a parallel bus connection between the FPGA and either non-volatile memory or a microprocessor data and address bus. There are both 8 and 16 bit wide modes available to get the maximum data transfer rate the user requires. With a non-volatile memory, either the FPGA or an external device can be the controller for the configuration. The master is the device that provides the address and control signals for the data transfer between the memory and the FPGA.

If we use the microprocessor bus solution, the processor will always be the master. Using this mode, the FPGA can be treated in the same way as a memory device, allowing it to be configured at any time. The Atmel AT40K family of FPGAs has the unique ability to be partially reconfigured whilst not affecting the rest of the FPGA. Indeed, until the reconfiguration is complete, all I/Os and cell outputs remain in their previous state. This allows for the adaptive changing of functions or constants within the FPGA without affecting the performance of the rest of the system.

Typically where an FPGA is used to perform Digital Signal Processing functions, coefficients for the functions can

be changed with an environmental change. One example is in a video movement detection function. This process looks for changes between frames within a datastream. A large number of calculations are performed on an incoming data stream, and comparisons with known results made. In differing lighting conditions known results may vary widely. The ability to adapt the known results with changes in lighting conditions adds added value to the system but no extra hardware for the designer. This approach is best for those systems already utilising a processor alongside one or more FPGAs, and is becoming a common method of configuration.

The other major consideration for FPGA users is that of clocks. Global or Fast Clock signals/buffers should be used wherever possible. This part of the routing resource is designed to minimise the skew between the same clock input at all positions on the FPGA. Also, good quality clock signals, especially with the higher clock frequencies involved, are essential.

FPGA applications

Now we know everything about how to use an FPGA, what can they be used for? The most obvious usage is as a tool to 'mop up' random logic on boards with large amounts of discrete devices. This is probably also the simplest and most trivial use of such a powerful device. The FPGA really comes into its own where complex high level functions are implemented in one device.

Digital audio

We have already seen that the AT40K

devices are particularly good at operations involving mathematical functions. Many applications in the audio and video sphere are based around complex mathematical algorithms. For instance, the latest generations of digital (GSM) mobile telephones perform some form of Digital Signal Processing on both the received and transmitted data to optimise for noise cancellation and filtering of unwanted frequencies. This sort of system could be emulated by using a pair of Analogue to Digital and Digital to Analogue converters as an interface to an audio source and some form of audio output driver. Then, the FPGA could be used as a functional block on which algorithms could be developed to create effects such as filtering and echo cancellation in the digital domain.

User interfaces

For just about every application today, there is a User Interface of one form or another. There are several levels of such an interface, from a simple LED response or a pushbutton right up to a full touch-sensitive colour LCD or Plasma graphic display panel. The FPGA, where the level of usage for this type of device can vary, is an ideal way to control such an interface. One of the beauties of this approach is that the input and output side can have any level of dependency on each other as required by the user.

For example, an LCD display is often controlled by toggling the backplane of the display at 50 Hz, and then toggling the 'On' segments at the same frequency but out of phase with this backplane. The generation of the backplane clock waveform is an ideal function for an FPGA, as is the interfacing or decoding of the data being output to the display driver. With the use of the internal pull-ups and pull-downs for terminating the bus interfaces and for switch inputs, the number of external passive components required can be minimised.

Video

The same approach could be applied to video signals. Here a much higher speed ADC and DAC are required, and the data throughput will be much greater. However, once the data is digitised, the processing is carried out in a similar method, although more care is needed with timings. The possibilities with manipulating video signals are much greater than for audio, with picture-in-picture (PIP) effects using multiple input bitstreams concatenated into the one output stream. Also, time/date data could be added to a video picture.

Microprocessor communication

Another common feature of electronic systems is communication between devices using a serial interface, like I²C or SPI, or via a UART connection onto RS232 for longer distance communications. These serial interfaces are usually based around state machines for both reception and transmission of data. As we have seen earlier, FPGAs are very good at implementing this kind of function, especially with VHDL entry methods. One of the main attractions for a serial bus is the small number of interconnects required by the interface. This kind of interface is commonly used to interface with serial EEPROMs, a form of non-volatile memory most suitable for data storage. Also, there are a large number of slow, high precision ADCs which use an SPI serial interface for data transfer.

In-system programming

We have looked at the configuration of the AT40K family of FPGAs whilst in operation. This can be achieved by using a small, low cost, efficient microcontroller often interfaced to external memory for bit-stream storage. A microcontroller from the Atmel AVR range is ideal, as it boasts In-System Programmable Flash and EEPROM memory for program and data storage. The MegaAVR range boasts a very large internal memory (128Kx8), so a small amount of application code could use the remaining Flash memory as bitstream storage without the need for external non-volatile memory.

On-board microcontrollers

One of the future developments of FPGAs will be the integration of microcontroller cores into programmable devices. There are two approaches to this. The first is to have the VHDL code for a microcontroller core, and use the FPGA itself to integrate the core. This takes a large amount of FPGA resource, and there are definite limits to the speed the microcontroller core can run.

The other approach is to actually integrate the microcontroller core into the FPGA in hardware. This gives the opportunity to still run the microcontroller at full speed and not lose any of the programmable resources available in the FPGA core. For the AT40K range, it also means that the bitstream controller is effectively built into the FPGA for the on the fly partial reconfiguration.

Starter Kit

There are many more things that we can do with an FPGA. But still, one of

the biggest problems is the development of hardware solutions using this technology due to the very nature of the high pin count, fine pitched physical device size.

It is hard for the casual user or hobbyist to create a board that can be used for experimentation for these very reasons, and so the FPGA lays dormant as a device for home use.

To combat this, Atmel have introduced, accompanying this series of articles, an FPGA Starter Kit¹ which gives the user a ready built development environment that includes several FPGA controlled peripherals.

The first of these peripherals is the external circuitry needed to implement three types of Analogue to Digital converter, and two types of Digital to Analogue converter. The first of the ADCs uses a binary successive approximation approach to get an 8-bit conversion in eight clock cycles, allowing high speed conversion, dependent only on the quality of the external components, and the ultimate speed of the FPGA. The second type uses a binary count to achieve the same result, but this approach takes from 1 to 255 clock cycles to get a result. The only advantage is that it is easier to implement. The final type of ADC is a very slow, on-board high-accuracy ADC designed for measurement systems.

The DACs are implemented using an R-2R ladder approach to generate an output voltage very quickly from an 8 bit binary number. The second approach is to use pulse width modulation to generate the output voltage. A pulse train of constant frequency has its mark/space ratio varied to adjust the DC content of the waveform. This is not a quick, high-resolution approach, but is useful as a controller in power supply applications.

The second major on board peripheral, and probably the most obvious one, is the 6-digit, 7-segment LCD display. This is operated as explained earlier on, and provides a high quality display for applications such as timers, instrumentation and even games. There is also a connector for the addition of a graphic LCD panel, not supplied, for more complex graphic displays. In addition there are eight LEDs and eight switches available for more feedback/debugging. In both cases, an LED or a switch is 'on' if the port pin on the FPGA is at a logical '0'.

The board has RS232 drivers for easy connection of a firmware UART to another device, such as a PC for data logging, debug or any other purpose. This ensures the correct voltage levels

```

LIBRARY ieee;

USE ieee.std_logic_1164.all;

ENTITY orgate IS

PORT (
  A : IN    std_logic;
  B : IN    std_logic;

  P : OUT   std_logic
);

END orgate;

ARCHITECTURE behaviour OF orgate IS

BEGIN

  IF      (A == '1')
  THEN   P <= '1';
  ELSEIF (B == '1')
  THEN   P <= '1';
  ELSE   P <= '0';
  END IF;

END behaviour;

```

Figure 12. Build, oops, program your own OR gate.

for direct connection without further buffering.

One of the most convenient features of the Starter Kit is its clock handling. There are four clock generators, one Oscillator and three crystals, and one manual clock input. The clock frequencies are 40 MHz, 10 MHz, 4.1920 MHz and 32.768 kHz. The 4.1920 MHz clock is used as a master BAUD rate generator for the serial interface applications. The 32.768 kHz clock is used for a binary division to get a 1 Hz clock, or other low frequency tick for a real time system operation. The manual clock is a switch that generates a clock edge on each press. Of the eight global clocks, these five clock sources are connected to GCLK1 to GCLK5 on the FPGA. This leaves three other clock signals free for the user to drive.

Another major feature of the development board is the socket for the on-board AVR microcontroller. There are also four sockets for SPI serial EEPROMs for bitstream or data storage as required. This immediately gives the ability to configure the FPGA on the fly under microcontroller control. The AVR section of the board is based on a cut down version of the Atmel STK200 Starter Kit, and employs the same download cable as the FPGA Configurator to program it In-System. This also starts to address the future by integrat-

ing a hardware microcontroller and an FPGA, not on the same piece of silicon, but on the same circuit board. This gives many of the same possibilities as future developments will bring us!

As well as all of the peripheral interfaces on board the Starter Kit, all of the non-dedicated I/Os are tracked to headers for connection to other peripheral blocks. This allows the user to make connections to the Starter Kit from other boards/systems to allow full system prototyping easily and cost effectively.

Build your own OR gate

Now we have seen how to design an FPGA from idea to finished hardware, with cost effective software and hardware in the form of a FPGA Starter Kit, we will quickly look at a simple

VHDL design that can be implemented on the Starter Kit.

We will create an OR gate from first principles as a simple example. The VHDL code for the OR gate is shown in **Figure 12**.

The first two statements include and enable for use a standard VHDL library supplied with all VHDL tools. This library contains the basic constructs for VHDL, as well as architecture specific details.

All VHDL files have an ENTITY declaration. This section defines the inputs and outputs of the design, (in our case, two ins and one out). The ENTITY is a description of the outside of the circuit, and is analogous to a symbol on a schematic.

The ARCHITECTURE description is where we define the logic to be implemented in the design, which is like the circuit diagram within the symbol. In this section we would have a definition of the SIGNALS used to connect several entities together in a more complex design. We would also describe the connections between the entities in this section.

Implementing an OR gate is certainly a simple example, but this series has not intended to teach VHDL in any way. There are many good courses and texts available on VHDL from various sources², and at varying costs. Training companies with good reputations such as Doulos run open courses

to teach VHDL and other design methodologies to take an absolute beginner to a high standard within a few days. Alternatively, several of the best texts take a tutorial approach to aid practical learning of what can be an abstract subject.

Conclusion

We have come a long way since the first article. We started out by discovering what an FPGA is, and what can be done with this type of component. Then we looked at how we design with them and what methods of design entry are suited to such a complex component. Finally in the first article we looked a little at the general architecture of Atmel FPGAs.

In the second part we looked at how a design was taken from raw VHDL in an ASCII text file and converted, via synthesis and device routing, into a file the FPGA can be configured with. This includes an overview of the design tools provided on the free CD-ROM accompanying this series of articles³, which are not restricted in any way.

Finally, in this article we have looked at the hardware aspects of using FPGAs, and how a low cost Starter Kit, such as the one from Atmel can make the use of such complex components easy for the home user. Finally we had a brief look at what a VHDL file looks like in its most basic form.

It is hoped that following this series of articles, the user is tempted to go further and perhaps purchase and enjoy using the FPGA Starter Kit, on special offer in this magazine, and create exciting and innovative FPGA designs that give the user a great deal of self satisfaction.

(990063-3)

Notes:

1. The book and Starter Kit mentioned in this article series are available (at a special discounted price for Eektor readers) from Kanda Systems Ltd, Unit 17-18, Glanrafon Enterprise Park, Aberystwyth, Ceredigion SY23 3JQ. Tel. (01970) 621030, fax (01970) 621040, Email sales@kanda.com
2. Programmable logic: VHDL and other new ways. Eektor Electronics October 1997.
3. Free cover-mounted CD-ROM supplied with November 1999 issue of Eektor Electronics.

switched mains output for ATX

Design by K Walraven

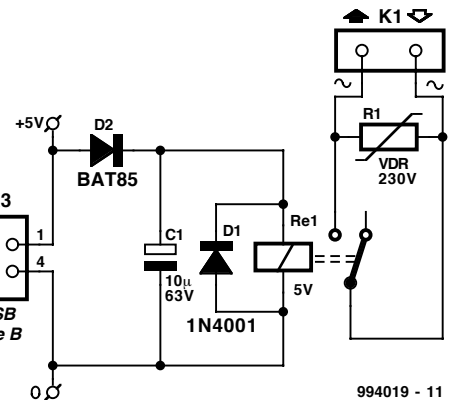
Current personal computers with an ATX motherboard are not provided with a switched mains output socket. It is therefore no longer possible to achieve automatic switching on or off of peripheral units with the computer on/off switch. This is not such a problem when switching on, because it is quickly seen when a peripheral unit is on or not. However, overlooking switching off at the end of the day or working session leads to needless energy consumption and a possible shortening of life of the peripheral unit. It is, fortunately, simple to do something about this.

An ATX motherboard contains all logic circuits for implementing a USB port. Peripheral equipment that may be connected to this bus may draw a current of up to 100 mA from it, and a total of not more than 500 mA for all units together.

This means that the USB port may be used without any difficulties to energise a relay. This relay in turn makes it possible to switch peripheral units on and off in tandem with the computer.

When there is a potential at the USB interface, relay Re1 is energised via diode D2. The relay contact closes and the peripheral units are powered. Capacitor C1 buffers any irregularities on the USB potential so that a brief dip in this does not immediately lead to the relay being de-energised. Diode D1 is a free-wheeling device for the relay coil.

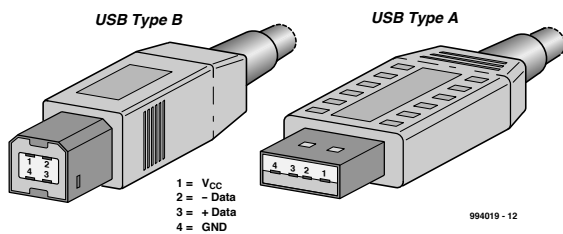
The design of the USB port is well thought out. There are two types of connector around. Downstream, that is, from computer to peripheral unit, a square one (Type A) is used, whereas upstream, that is, from peripheral unit



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to computer, a flat one (Type B) is used. By terminating each cable with a Type A and a Type B connector, connecting errors, such as those frequently encountered with RS-232 and DIN cables, are all but impossible. The cables are always terminated into plugs, whereas the equipment is fitted with sockets.

(994019-1)



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COMPONENTS LIST

Resistor:
R1 = voltage-dependent resistor (VDR), 230/250V

Capacitor:
C1 = 10µF 63V

Semiconductors:
D1 = 1N4001

D2 = BAT85

Miscellaneous:
Re1 = Siemens E-card relay, 5V, PCB mount
K1 = 2-way PCB terminal block, pitch 7.5mm
K3 = USB socket, panel mounting, Type B

