

ELEKTOR
ELECTRONICS

PC TOPICS:

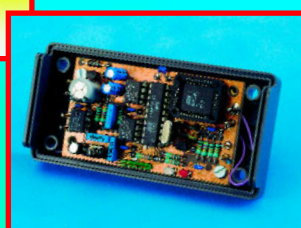
digital audio formats

COM port analyser

printer port extension



microcontrollers' survey



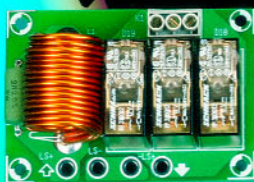
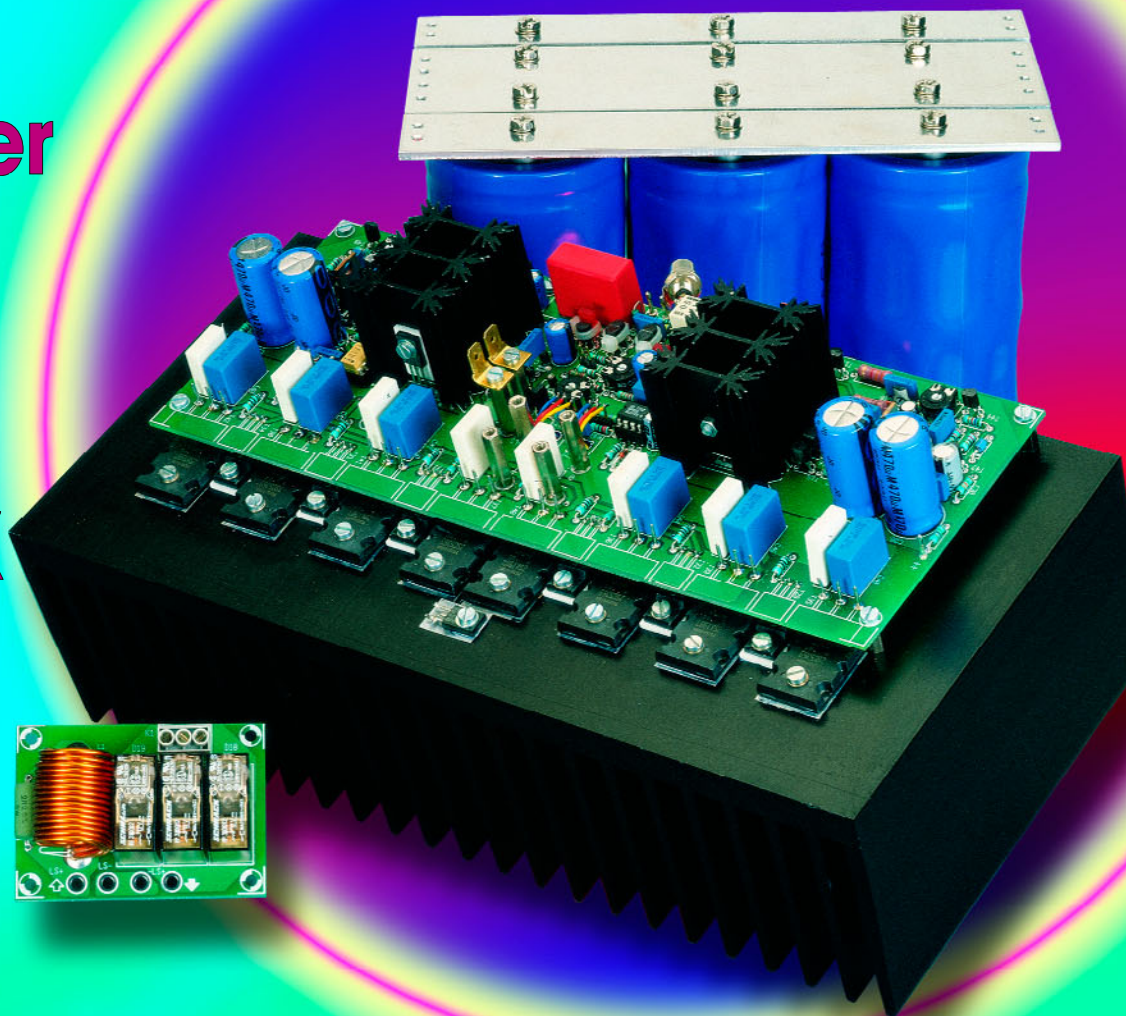
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for DMM**

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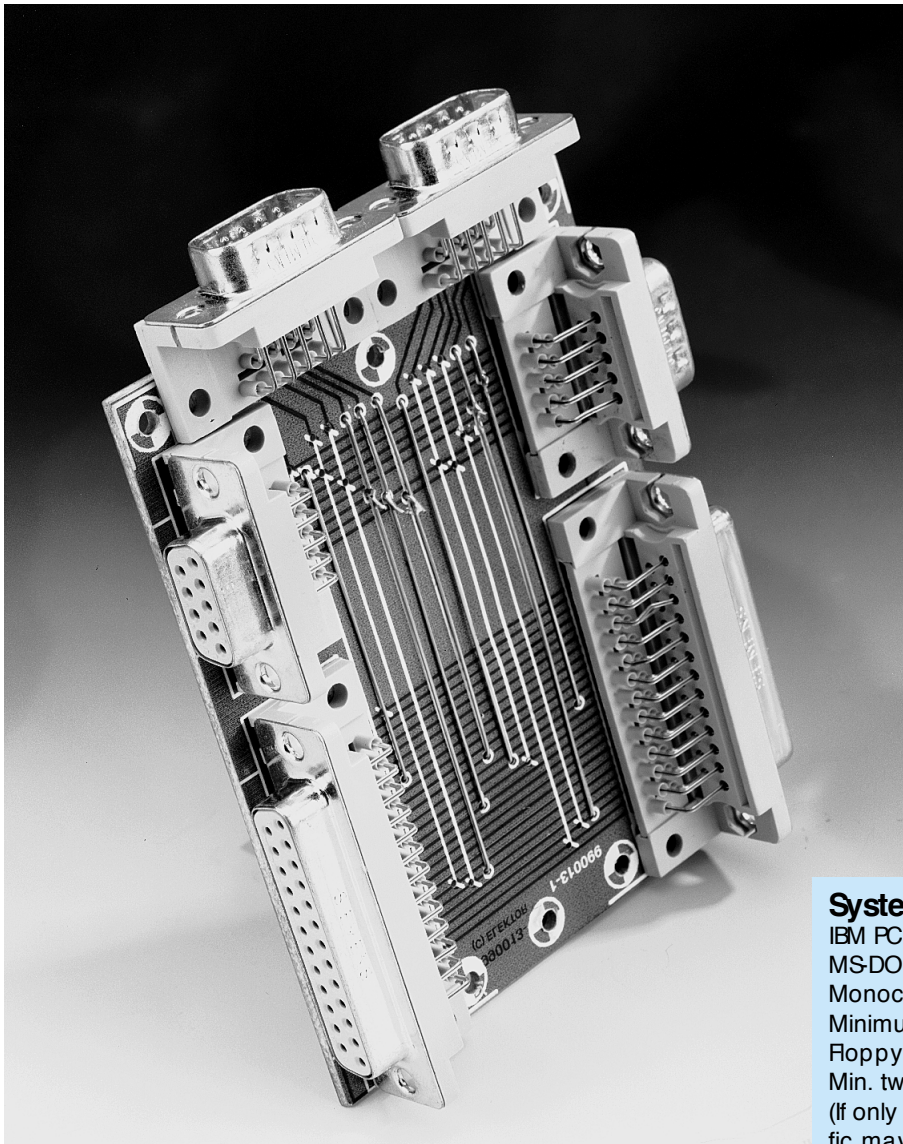
- COM-Watch
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To many computer users, asynchronous serial communication will always remain something of a mystery. Does the link work or not? Do all the peripherals have the same settings, and does the right signal arrive on the right pin? These questions are easily answered by Com-Watch®. The system consists of an advanced DOS program and a simple passive adaptor.

In co-operation with CER International

COM-Watch®

problem sleuth for serial ports



Although the serial port is one of the most frequently used communication gateways in the modern PC, it also calls up the largest number of questions. Modem, mouse, graphics tablet, digital photo camera, personal organiser, you mention it, all this equipment is designed to exchange data with the PC by way of the serial port. The difficulty with this port is the ever-changing number of control signals employed: sometimes three, sometimes five, and then again eight! This should not be a problem, though, if only the transmitter and the receiver use the same communication settings.

The problem is aggravated by the fact that there is a difference between a DTE (data terminal equipment, for example, a PC or a printer), and a DCE (data communication equipment, for example, a modem). As a result, two computers that have to communicate with each other (i.e., two DTEs), have to be connected by a different cable than, say, a computer (DTE) and a modem (DCE).

Note, however, that there are still lots

System requirements

IBM PC XT AT or better
MS-DOS 3.1 or later
Monochrome or colour videocard
Minimum 256 kBytes memory free
Floppy disk drive (3.5 in.)
Min. two free serial ports
(If only one port is available, one-way data traffic may be monitored)

Com-Watch is a registered trademark of CER International b.v.

of pitfalls even if the right hardware (wires and connectors) is used. There is, for instance, the baud rate to take into account, the number of data bits (7 or 8), the number of stop bits and the parity check.

Considering all these potential problems, it is surprising to see that so many serial links work just fine.

The complexity of the matter is evident from the very fact that so many different systems have been developed to analyse serial connections, and resolve conflicts. COM-watch is a system developed by CER international specifically for this purpose. Using very little hardware and a DOS program, all traffic on an RS232 link may be scrutinised in great detail, allowing the user to detect the cause of the communication conflict, and, of course, eliminate the source of the problem.

CER International and *Eektor Electronics* jointly offer the program at a special reduced price. The associated hardware is simple to make, and you'll find it described further on in this article.

The approach

The basic operation of COM-Watch is illustrated in **Figure 1**. In principle, there are two ways of analysing a serial link: actively or passively. Com-Watch supports both, so that the system can really be called versatile.

The first approach that comes to mind is to observe the operation of an existing link. This is shown in **Figure 1a**. The method as shown employs passive analysis. Two apparatus communicate by means of a serial connection. Using a special adaptor (which will be reverted to below), the link is 'tapped'. A PC running the COM-Watch software then analyses the data traffic, and attempts to make sense of any errors that occur. Note that the PC used for fault analysis does not partake in the data traffic: it merely acts as an onlooker, i.e., its role is passive. The PC uses two serial ports (Channel 1 and Channel 2) to monitor the communication process: one for the data traffic from DCE to DTE, and for DTE-to-DCE traffic. Both channels have their own connection on the interface board to be described.

On the PC, serial ports COM1 through COM4 may be used for Channel 1 and Channel 2. For maximum functionality, two physical ports are needed. If only one port is available, then the channel to use for a particular set of signals may be found in **Table 1**. By changing over to another connector on the interface board, the entire

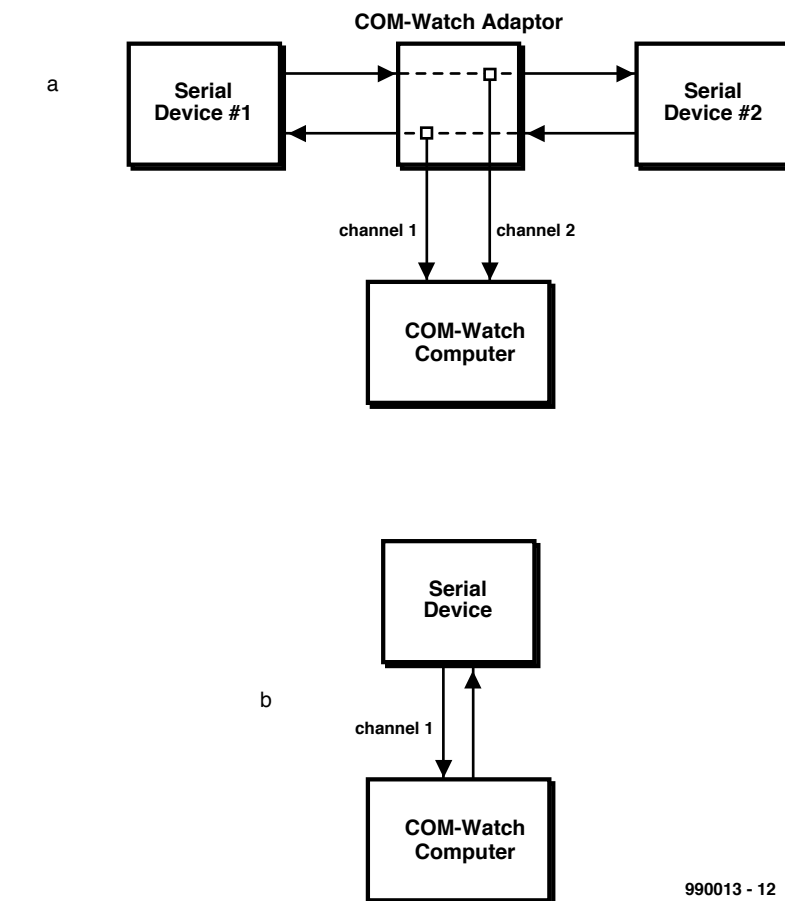


Figure 1. Using COM-Watch, data traffic may be analysed in two ways, passively (a) or actively (b). The passive approach requires a special adaptor.

communication process may be still analysed with just one extra action.

In passive mode, all data traffic is monitored, but not affected in any way. In true Sherlock Holmes tradition, Com-Watch tries to observe what is happening, and detect flaws without any of the 'suspects' noticing. On the display of the PC running the Com-Watch program appears a detailed analysis of the problem situation.

The active alternative

If you are having problems in getting a serial port to work at all, Com-Watch offers an active mode to help you sort it all out. Figure 2b shows how it works. Via its serial port the analysing computer communicates with the peripheral, and so collects as much information as possible. The display shows which data is sent by the PC, and which data is returned. The switching of several control signals is also easy to follow. This measurement method does not require specific hardware.

Data received by the computer is displayed by the software via Channel 1 (remote channel), while that sent by the computer to the peripheral

apparatus may be viewed on Channel 2 (local channel). The latter Channel is only implemented in software, and therefore does not require a physical serial communication port.

On paper, the approach used by Com-Watch may look complex. In practice, the process is self-evident. The internal context-sensitive Help function makes working with the software much easier.

A little hardware

To be able to analyse the connections sketched in Figure 2a, a special adaptor circuit has been developed. As shown in **Figure 2**, this is a very simple circuit. For do-it-yourself construction, a single-sided printed circuit board is available. Few of you will object to the one disadvantage of a single-sided board: having to fit a couple of wire links. The copper track layout and component mounting plan of the PCB are given in **Figure 3**. Actually, 'components' is limited to a few wire links and connectors that enable the serial link to be 'tapped'. So, we think you will agree with us that this is a very simple circuit indeed.

990013 - 12

Script language

COM-Watch has an extensive script language, which allows almost any problem to be pinpointed, even if it occurs sporadically. This overview lists the commands available for making scripts. Script files intended for COM-Watch have the extension .cws.

Syntax

[] means optional

| means 'or'

drive: specifies disk station

path: specifies location

filename: self-evident

string: a series of characters enclosed in brackets

control: specifies the status of control signals the system has to wait for. The following options are available:

CTS= on | off

DSR= on | off

RI= on | off

CD= on | off

BRK= on | off

FE= on | off

PE= on | off

OE= on | off

Description of script commands

CAPTURE= *on | off*

Determines whether or not data from connected equipment has to be stored in a buffer, for later analysis.

CHDIR [*drive:*]*path*

Change current directory

EXIT [*PROGRAM*]

Leave the script program and return to analysis mode. If the parameter *PROGRAM* is added, the program returns to DOS mode.

GOTO *label*

Only the first 8 characters of a label are used to distinguish it from other labels. Up to 100 labels may be used in a script.

KEYBOARD *on | off*

Switch the keyboard on or off. This allows you to simulate a terminal.

MATCHCASE *on | off*

Determine if the script language is case sensitive or not. The default is **MATCHCASE** *off*.

SEND *string*

Transmit a text line to the connected peripheral, for example, a modem initialization string.

SEND FILE [*drive:*]*[path]filename*

Transmit the indicated file to the peripheral.

SETCHAN*n* = COM*m* | *off*

Select a communication port. For parameters *n* and *m* the values 1 through 4 are available. A COM-Watch channel is switched off with *off*.

SETCHAN*n* IDENT= *string*

Defines an identification string for a channel. Parameter *n* is either 1 or 2. Only the first 10 characters of a string are used by the program.

The default identifiers are

CHAN1 IDENT= Channel # 1

CHAN2 IDENT= Channel # 2

SETCOM*m* = *baud* [*,parity*] [*,data*] [*,stop*]] COM*m*

Specifies the COM port, with *m* between 1 and 4.

baud

Specifies the communication speed; available values are 110, 150, 300, 600, 1200, 2400, 4800, 9600, 19200, 38400, 57600 and 115200.

data

Specifies 7 or 8 databits

stop

Specifies the number of stop bits.

The default values are copied from DOS.

SET DISKSTREAMING *on*, [*drive:*]*[path]filename* | *off*

If no extension is given with the filename, the program chooses the extension .cws.

SET FORMAT *mnem* | *ascii* | *hex* | *dec* | *oct* | *ebcdic*

This command changes the current format into the selected format.

SET RINGBUFFER *on | off*

Switch the ring buffer on or off.

SET SENDDELAY *milliseconds*

This is used to set the length of the pause between consecutive characters in the transmission of data. The available range is 0 to 100 ms. The default is no delay.

SET TIMESTAMPING *abs* | *rel* | *date* | *off*

This command is used to select the operation of the time stamping system.

SET VIEW *split* | *mixed* | *channel 1* | *channel 2* | *event* | *active*

This command is used to set the current display mode.

WAITCOUNT_EVENTS *number*

Determines how many events must have occurred before execution of the script is continued. Maximum value: 1000.

WAITDATA_EVENT [*CHAN**n*] *string* [*control*]

Interrupts the execution of a script until the stated data have been received.

[*CHAN**n*]

This may be used to optionally define the channel. If no channel number is indicated, both channels are monitored.

string

Specifies the string to wait for.

control

Specifies the status of the control signals to wait for.

WAITDELAY *hundredths_of_seconds*

Execution of the script is halted and resumed after the specified delay.

WAITKEYSTROKE *string*

Execution of the script is halted and not resumed until the specified text has been entered via the keyboard.

WAITTIME_EVENT [*month-day-year*] *hours:minutes:seconds*

This specifies the date and time when script execution is to resume. Month, day and year are optional.

WHEN DATA_EVENT [*Chan**n*] *string* [*control*] [*,command*]

Indicates which action has to be taken if a specific situation arises.

*CHAN**n*

This command allows you to optionally specify the channel. If no number is supplied, both channels are monitored.

string
This specifies the text to wait for.

control
Specifies the status of the control signals to wait for. This is an optional addition.

command
Defines the action to be taken if a condition is satisfied.

WHEN KEYSTROKE *string[,command]*
This command specifies the action to be taken after a string has been entered.

string
Specifies the text to wait for.

command
Specifies the action to be taken when the condition is satisfied.

WHEN TIME_EVENT [*month-day-year*] *hours:minutes;seconds* [*command*]
This command specifies the action undertaken when a certain time is reached.

month
Specifies the month; valid numbers are 1 through 12.

day
Specifies the day; valid numbers are 1 through 31.

year
Specifies the year; valid numbers are 1980 through 2099.

hours:minutes;seconds
Specifies the exact time at which the script is to be executed.

hours
Specifies hours, valid numbers are 0 through 23.

minutes
Specifies minutes, valid numbers are 0 through 59.

seconds
Specifies minutes, valid numbers are 0 through 59.

Command
This is the command to be executed when the indicated date and time are reached. If no command is entered, COM-Watch will switch off the previously defined WHEN DATA_EVENT with the same string.

The component mounting plan in **Figure 2a** shows the locations of the wire links if the interface is employed for analysing regular serial links (RS232). If you require support for a symmetrical serial bus like RS422, another configuration is in order. The relevant 'constellation' of the wire links is shown in **Figure 2b**. D25 and D9 connectors are fitted at both sides of the PCB. If you do not envisage ever needing one of the two, then simply omit the relevant connectors. If you only use the 9-pin version, the board may be made much smaller by omitting the 25-pin connectors.

The link to the PC (carrying the information employed for Channel 1), is made using two 9-way (male) connectors.

The software

COM-Watch is a program which runs under the DOS operating system. It is suitable for analysis of data traffic between a DTE and DCE. Fortunately, the fact that the DOS environment has been chosen for the program does not preclude its use under the Windows operating system. When the program is started, it simply claims the entire screen, temporarily hiding Windows.

Install the software on drive C: in a directory called ComWatch. If you want to use another drive, say, D:, then type

a: i n s t a l l d:

Any other drive number may be used, provided it exists.

After entering

[drive][path] Comwat ch. exe

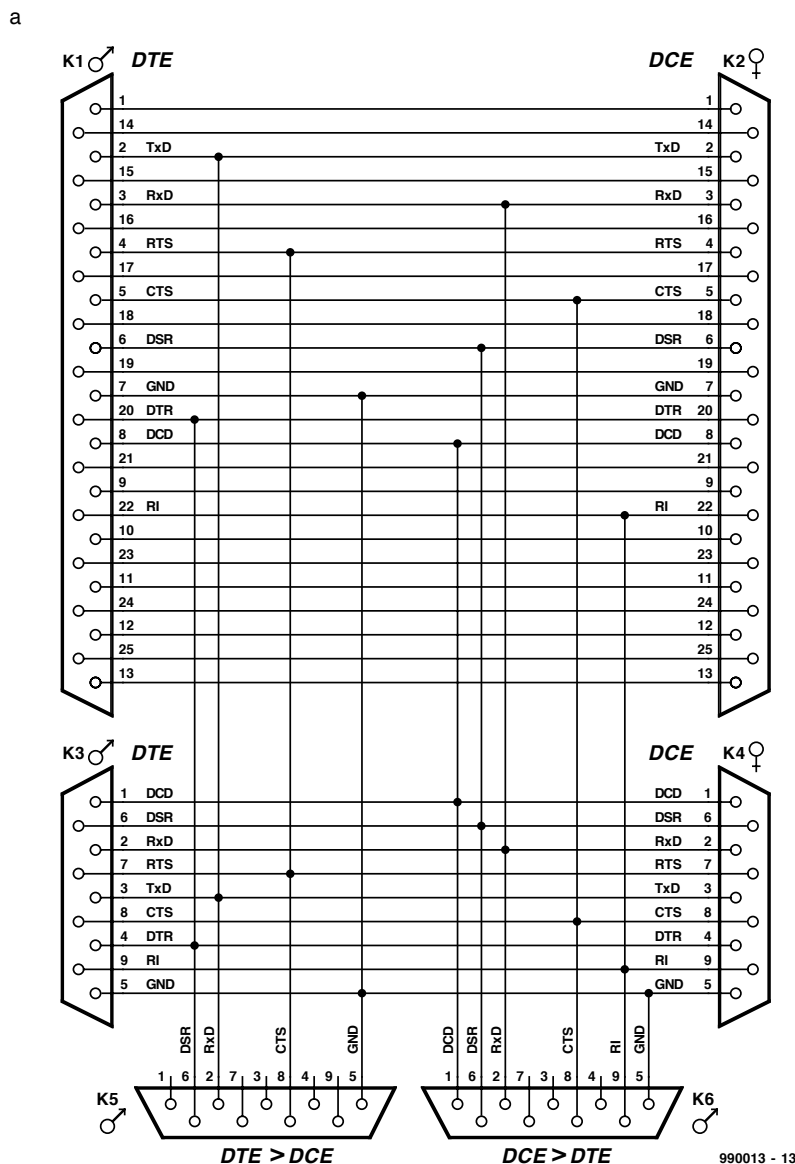


Figure 2a. Circuit diagram of the adaptor used for measurements in passive mode (RS232 version).

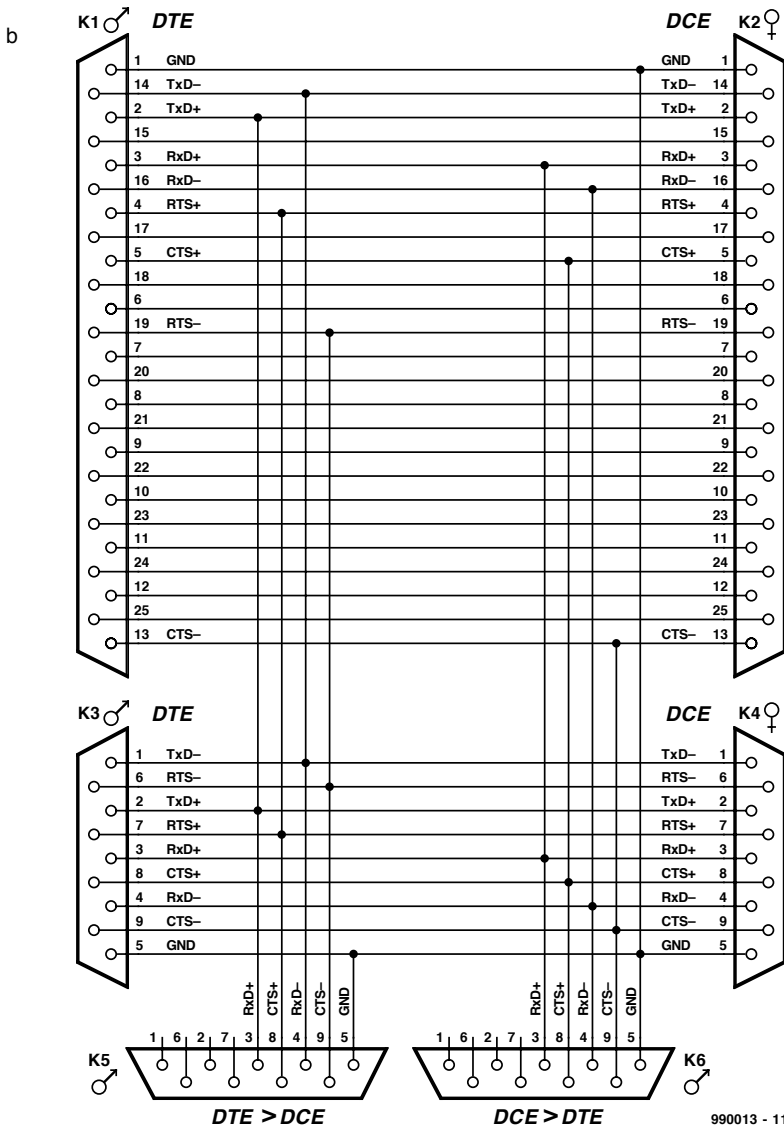
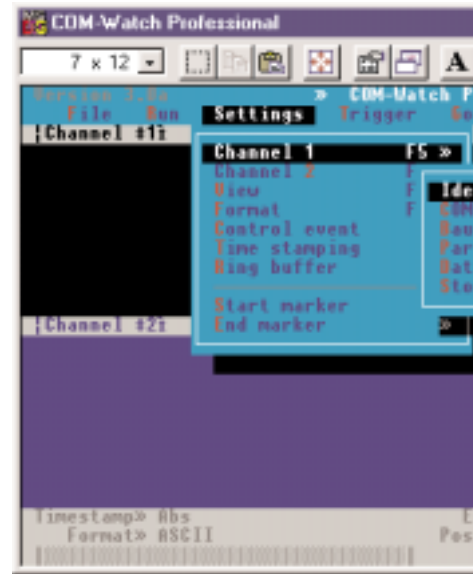


Figure 2b. Circuit diagram of the adaptor used for measurements in passive mode (RS422 version).



the program starts in full-screen mode. If the hardware has been connected up, the measurement session may start.

The screen shows quite a few things. Fortunately an interactive and context-sensitive Help function is available, so that everything will soon be clear. **Table 2** shows the functions assigned to various keys.

After connecting the hardware to the PC, you first have to configure the software. As you can see from the table, this is done with the aid of function keys F5 and F6. Once you have entered the right data, the program is ready for use.

Table 1. Signal allocation on 25-pin and 9-pin RS232 connection.

D-25	D9	description		monitored	DTE-DCE
1		screening			
2	3	transmitted data	TxD	yes (# 1)	DTE →
3	2	received data	RxD	yes (# 2)	← DCE
4	7	request to send	RTS	yes (# 1)	DTE →
5	8	clear to send	CTS	yes (# 2)	← DCE
6	6	data set ready	DSR	yes (# 2)	← DCE
7	5	massa	SGND	-	
8	1	data carrier detect	DCD	yes (# 2)	← DCE
9		reserved			
10		reserved			
11		free			
12		data carrier detect ch. 2		no	← DCE
13		clear to send ch. 2		no	← DCE
14		transmitted data ch. 2		no	DTE →
15		transmitted sign. elem. timing		no	DTE →
16		received data ch. 2		no	← DCE
17		received sig. elem. timing		no	← DCE
18		free			
19		request to send ch. 2		no	DTE →
20	4	data term. ready	DTR	yes (# 1)	DTE →
21		free			
22	9	ring indicator	RI	yes (# 2)	← DTE
23		data rate select		no	DTE →
24		transm. sign. elem. timing		no	DTE →
25					

Note:
signals processed via 1st COM port (# 1) DTE → DCE
signals processed via 2nd COM port (# 2) DTE ← DCE

Table 2. COM-Watch function keys

FKey	Normal	+ Ctrl
F1	Help	Go to position
F2	Save as...	Go to Time location
F3	Open ...	Find...
F4	Calculation	View/Activity
F5	Settings	View/
	Channel 1	Channel 1
F6	Settings	View/
	Channel 2	Channel 2
F7	View	View/Split
F8	Format	Format/
		Mnemonic
F9	Capture	Set Start
	Mode	marker to
		Current position
F10	Analyse mode	Set End marker
		to current
		position



Finally we should mention that a more extensive version of the program is available. More information may be found on the CER Internet website at www.cer.com.

(990013-1)

The PCB is available ready-made from the Publishers as order number **990013-1**.

The COM-Watch program is available on floppy disk (DOS) as order number **986035-1**.

+ Alt	+ Shift
Go to top	Go to Start marker
Go to Bottom	Go to End marker
Next match	Next error
Previous match	Previous error
Com port	Baudrate
Channel 1	Channel 1
Com port	Baudrate
Channel 2	Channel 2
View/Mixed	View/Events
Format/ASCII	Format/
	Hexadecimal
Set Start marker to Top position	Set Start marker to Entered position
Set End marker to bottom position	Set End marker to entered position

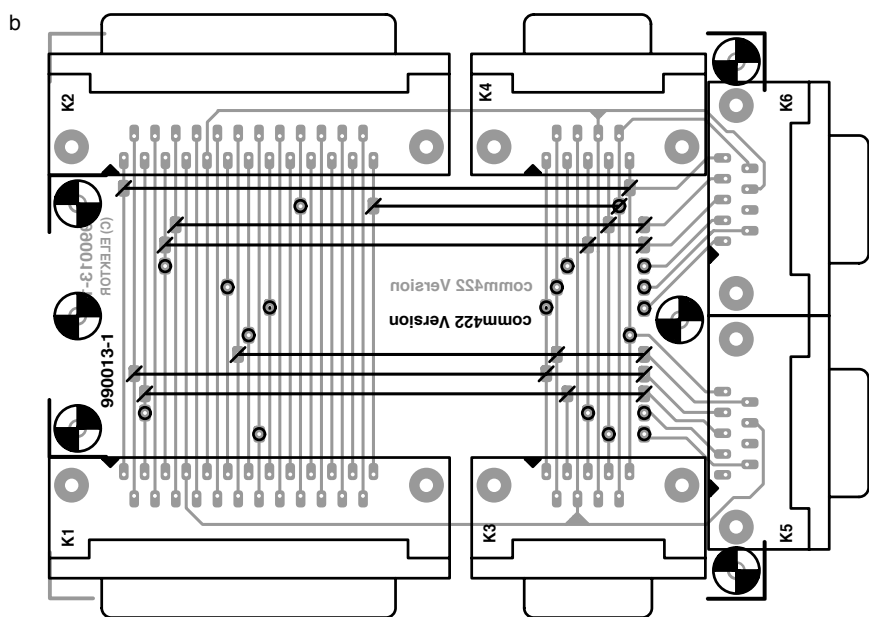
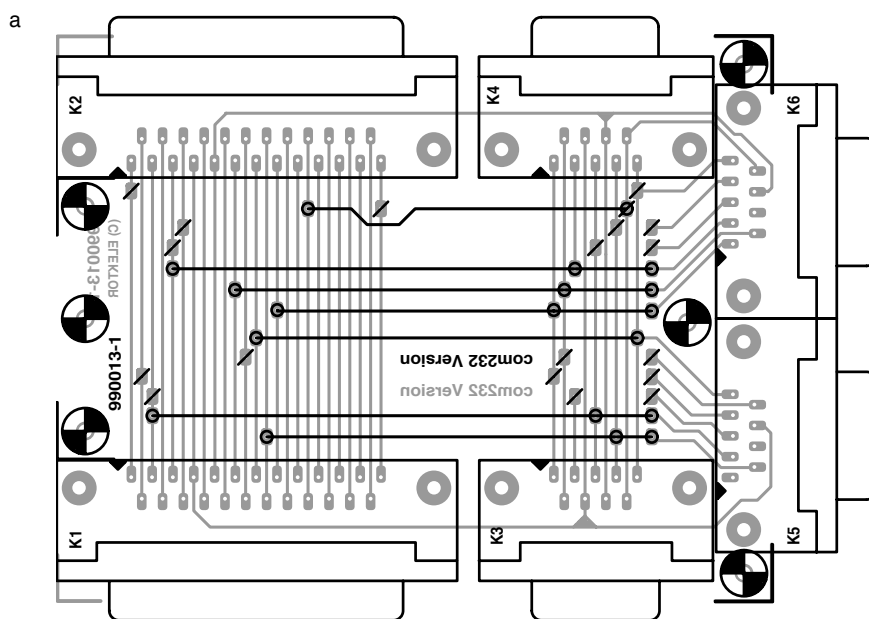
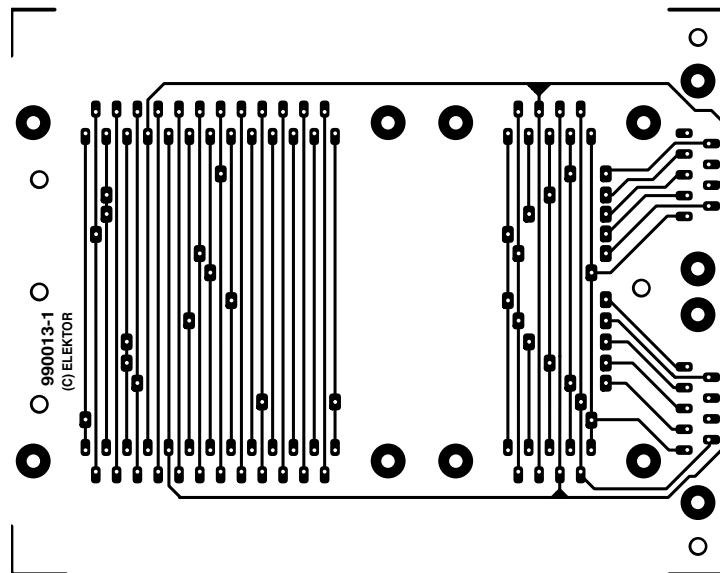


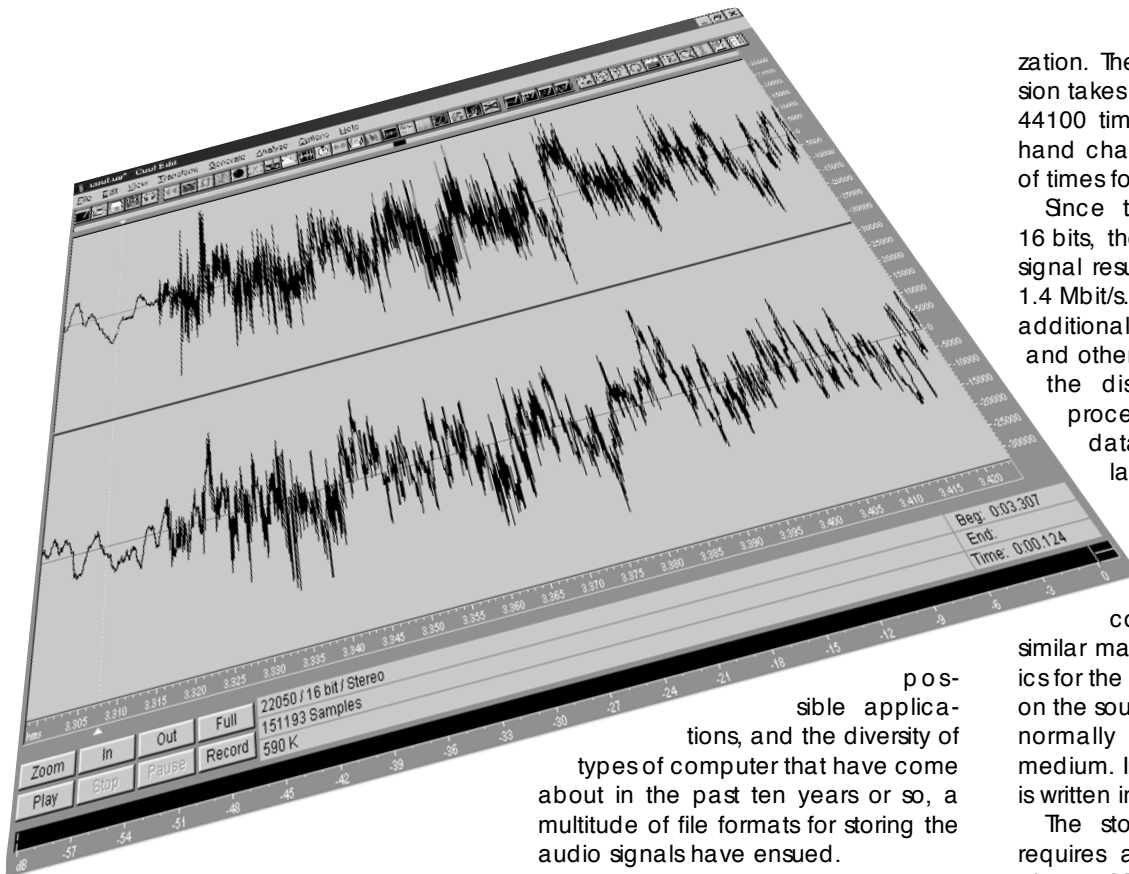
Figure 3. Copper track layout and component mounting plan of the adaptor board used for the passive monitoring system. Figure 4a is for the RS232 version, Figure 4b for the RS422 version.

Over the past few years the computer has changed from a word/graphics processor to an all-round unit that, among others, is suitable for recording and reproducing audio and video signals. Particularly as regards audio reproduction, a number of different formats have come into being. This article describes the more important of these briefly and the currently popular MP3 in some detail.

By our Editorial Staff

digital audio formats

more sounds from your computer



introduction

Today, a computer without sound is a rarity. Whether it concerns a sophisticated computer game or the simple warning beep accompanying various commands, sound is a must. Sound has become important even for Internet users. Nowadays, you can listen to radio broadcasts or download music via the net. Owing to all these

quantization

Thanks to the introduction of the compact disc (CD) almost 20 years ago, many people know what is understood by digital sound. Briefly, for those who do not, the analogue (proportional) audio signal is translated by an analogue-to-digital converter (ADC) to a large number of binary words. This process is called quantization or digiti-

zation. The rate at which the conversion takes place in the case of a CD is 44100 times per second for the left-hand channel and the same number of times for the right-hand channel.

Since the resolution of a CD is 16 bits, the quantization of an audio signal results in a bit stream of about 1.4 Mbit/s. This bit stream, together with additional data for error correction and other information, is recorded on the disc. During playback, the process is simply reversed: the data on the CD are read by a laser and translated by a digital-to-analogue converter (DAC) into analogue signals.

Audio signals in a computer are processed in a similar manner. The requisite electronics for the ADC and DAC is contained on the sound card, while the hard disc normally functions as the storage medium. In a computer, the bit stream is written into a data file.

The storing of the binary words requires a large amount of space: about 1 Mbyte for every six seconds of sound of CD quality. There are several means of limiting this space requirement. One is lowering the sampling frequency from 44.1 kHz to, say, 10 kHz which reduces the bandwidth. Another is recording the signal in mono(phonic) instead of in stereo (phonic) format, which degrades the quality. A third is lowering the resolution from 16 bits to, say, 8 bits, which tends to degrade the signal-to-noise ratio

and increase the distortion. A fourth, widely used, method is compressing the signal during recording and expanding it during playback.

Almost all computer systems (Atari, Unix, Intel, and so on) have their own specific file format, which has resulted in the same confused situation as exists in the case of pixel formats. That is to say, there is a bewildering multiplicity of formats, which does not help the consumer. This situation is not improved by the addition of yet more formats via the Internet.

Table 1 gives an overview of the most frequently encountered formats together with a brief description.

to compress or not to compress

Compressing an audio file is fairly complex because certain similarities between the large number of samples are not easily determined. Consequently, there are only a few lossless compression methods for audio signals. One of these is the ADPCM standard (in Windows) for the popular WAV format.

It is, however, possible to compress audio signals if some loss of detail is acceptable, as in the processing of digital images. In the case of digital images, the compression method is laid down by the Joint Photographic Expert Group (JPEG), a subgroup of the Joint Technical Committee 1 (JCT1) of the ISO (International Standards Organization – consultant to the United Nations) and the IEC (International Electrotechnical Commission). Another sub-group of the JCT1, the Motion Pictures Expert Group or MPEG, has laid down a standard for audio compression: the MPEG format. Currently, MPEG-1 Layer 3 (MP3) is the popular format for Internet users.

real time audio

In the early days of audio in computers, the entire audio file had to be loaded into the computer memory before it could be played back. This is particularly irksome during downloading of files via the Internet.

With the advent of fast modems it has become possible for techniques to be developed that enable sound files to be played back during the downloading. A particularly worthwhile contribution to this has been made by a process called 'AOD' (Audio On Demand), 'real time audio' or 'streaming audio', a product of the company RealAudio.

Table 1.
Overview of the most frequently encountered audio formats

<i>AIF</i>	<i>A format originally developed for the Macintosh. It is quite popular on the Internet and offers many different sampling rates and resolutions. Netscape and Microsoft browsers have no difficulty working with it.</i>
<i>AU</i>	<i>Originates from NeXT and SUN and was popular on the web and is still in use today. There are a number of variants, but normally the data are compressed to an 8-bit format with the u-law standard. Most browsers can work with it.</i>
<i>ES</i>	<i>A streaming audio format from EchoCast. Players are available for Windows and Macintosh.</i>
<i>IFF</i>	<i>An Amiga sound format that handles only 8-bit mono sound; it allows a free choice of the sampling rate.</i>
<i>LCC</i>	<i>A high-compression format (ratios up 1:50 are possible) currently available for Windows only, but other versions are under development.</i>
<i>MID</i>	<i>The MIDI format is not a true audio format, but a standard for exchanging control data between electronic musical instruments. Browsers can handle MIDI via a plug-in.</i>
<i>MOD</i>	<i>An original Amiga format that is reminiscent of MIDI. An MOD file contains a bank with samples and instructions how these samples are to be played. Requires a MOD plug-in.</i>
<i>MP3</i>	<i>The most popular current audio format. Various plug-ins are available.</i>
<i>RA, RAM, RPM</i>	<i>A popular streaming audio format on the Internet from RealAudio. Plug-ins are available for virtually all platforms.</i>
<i>SND</i>	<i>Apple, Amiga and Tandy have used this suffix for sound files. Some variants are compatible with the AU format.</i>
<i>STR</i>	<i>A format for professional sound processing on the Macintosh.</i>
<i>VDO</i>	<i>Another streaming audio format. It requires a plug-in as such as a VDO live player.</i>
<i>VMD</i>	<i>A streaming audio format named Internet Wave. It comes with a free encoder/decoder for Windows.</i>
<i>VOC</i>	<i>The Voice format, which is a development of Creative Labs, maker of the well-known Soundblaster cards.</i>
<i>WAV</i>	<i>The much used wave format has become well known since the introduction of Windows. It offers many different sampling rates, resolutions and compression factors.</i>
<i>XDM</i>	<i>An MPEG format from StreamWorks for streaming audio. There is a special player for Windows.</i>

MP3: good quality with high compression

Currently, MP3 is the most popular of all audio formats. In a very short time, this audio compression protocol has gained a strong position as music compressor. Many modern computers come with MP3 encoding and decoding software installed. Also, large numbers of MP3 files are being disseminated via the Internet and there are already compilation CDs that contain MP3 files. Some manufacturers have started to make available an MP3 Walkman™: a solid-state portable CD player which uses a flash memory as carrier.

developed for DAB

As a contributor to the pan-European Eureka 147 project (to develop a ter-

restrial digital audio broadcasting system – DAB), the German Fraunhofer Institut für Integrierte Schaltungen (Fraunhofer Institute for Integrated Circuits) has developed a codec (coder/decoder) for DAB in which the perception of the listener plays an important role.

The relevant algorithm takes into account certain properties of human hearing and on this basis determines whether a certain aspect of the sound in a piece of music is likely to be perceived by the listener or not. Depending on this likelihood, it further determines whether the relevant data should be included in the bit stream or not. This results in a redundancy compression system that enables a substantial data reduction without degrading the sound

The algorithm has been further

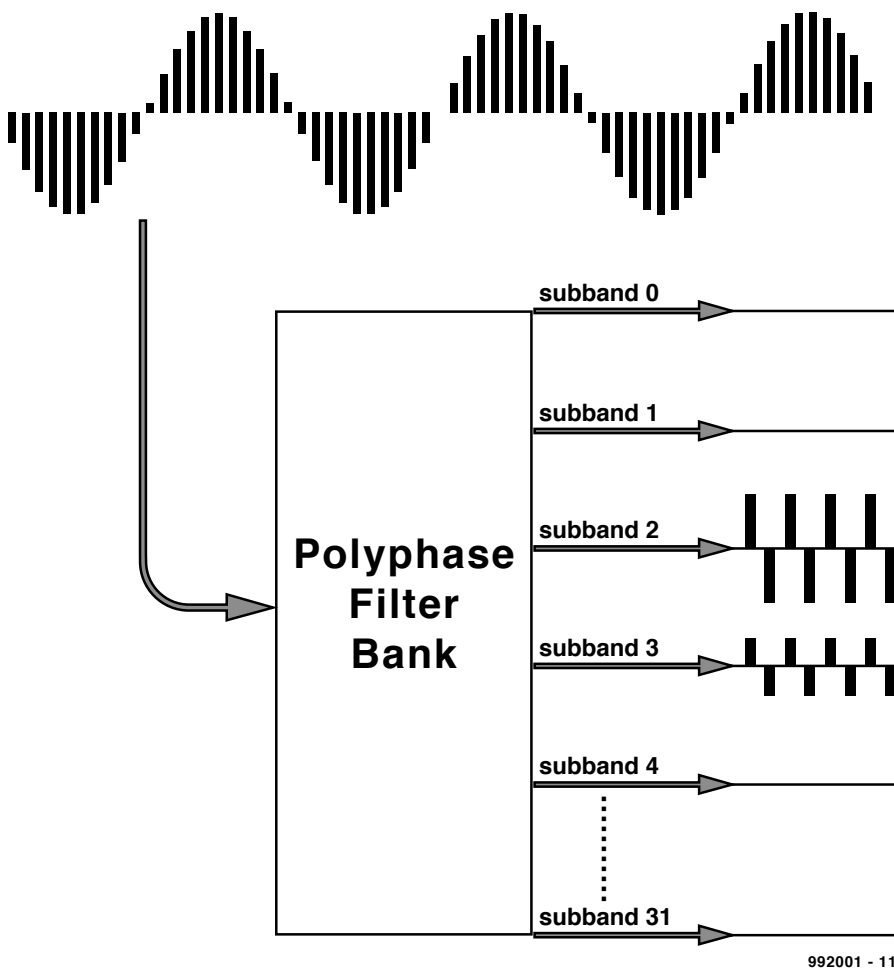


Figure 1. Each MPEG-1 layer makes use of a 32-bit filter bank. Whether the signal becomes masked or not is determined after it has been quantized.

enhanced by IIS in cooperation with the University of Erlangen and has been accepted as ISO MPEG-1 Layer-3 (IS11172-3 and IS13818-3).

layer 1, 2 or 3

Without data reduction, audio signals contain 8-bit or 16-bit wide samples which are taken at a rate that is twice as high as the highest frequency in these signals.

It has already been stated that the digitization of an audio signal results in a bit stream of about 1.4 Mbit/s. A state-of-the-art compression system can compress this by a ratio of 1:12 without an audible degradation of the sound. Reduction ratios of up to 1:24 are possible and still result in a sound quality that is superior to that when the sampling rate or the resolution are reduced to obtain a comparable compression.

The MPEG-1 standard describes three layers of compression: Layer 1, Layer 2, and Layer 3. All three are capable of producing sound of near-

CD quality. Table 2 gives an overview of the characteristics of these layers. The definitions within the norm refer only to the encoder and the data format used. This information enables manufacturers to design a decoder to their own requirements.

If stereophonic reproduction is not used, and if furthermore a restricted bandwidth is acceptable, even higher compression ratios can be used. The highest of these, Layer 3, uses the lowest bit rate and produces the best sound quality.

The three codecs are hierarchically compatible, which means that a decoder for Layer 3 can also be used with Layers 1 and 2. This is, however, not possible the other way around.

The higher the number of the layer, the more complex the encoder becomes and the higher the compression ratio that can be used.

Table 2 also shows the possible compression ratios attainable with Layer 3 and what these can be used for.

Listening tests with mixed audiences

show that the performance of Layer 3 remains excellent with a compression ratio of 1:12 – which is associated with a bit stream of 64 kbit/s per audio channel. If for certain applications the bandwidth can be limited to 10 kHz, good stereo reproduction is possible with a compression ratio of 1:24.

uniform structure

All three layers have the same structure. Their encoding technique is known as perceptual noise shaping or perceptual subband transform coding. The encoder analyses the spectral components of an audio signal with the aid of a filter bank (see Figure 1) and uses a psychoacoustic model to determine the discernible noise levels. Subsequently, the information is quantized and encoded in a manner which ensures that two important conditions are taken into account: the maximum bit stream and the masking effect.

All three layers use the same filter bank with 32 subbands. They all permit sampling rates of 32 kHz, 44.1 kHz, and 48 kHz, and are capable of working with bit streams of 32 kbit/s or higher.

background

To achieve a substantial reduction of the requisite digital bandwidth, MPEG-1 Layer 3 uses several techniques and short-cuts. The most important of these are:

- lower threshold of hearing
- masking effect
- a store of bytes
- joint stereo
- Huffman coding

Lower threshold of hearing

Research has shown that the lower threshold of human hearing is not linear: it peaks between 2 kHz and 5 kHz. Its properties are described by Fletcher and Munson. It is not necessary to encode sound that lies below the threshold since the listener cannot hear it.

Masking effect

Use is made of the fact that human hearing does not perceive weak sounds that are totally or partially masked by (much) stronger ones.

Research shows that owing to the masking certain sounds need not be encoded, which saves quite a lot of space. All MPEG-1 Layer 3 encoders therefore contain a psychoacoustic model in which the properties of

human hearing are incorporated.

Store of bytes

It often happens that a passage of music cannot be encoded with the available bit rate. The quality of the sound must then be adapted temporarily to enable the bit stream to match the capacity of the digital channel. MPEG-1 Layer 3 uses a buffer that provides some additional capacity in such circumstances. The buffer is emptied when sound is encoded at a bit rate lower than that available in the channel.

Joint stereo

Many small stereo hi-fi systems use a common woofer. In spite of this, the listener gets the impression that the sound does not emanate from this loudspeaker, but rather from the satellites. Research shows that below a certain frequency the human ear is not able to judge from which direction the sound comes. Compression techniques can make use of this property by not including stereo information below a certain frequency. This means that below that frequency the signal is encoded in monophonic form only.

Huffman code

The encoding of MPEG-1 Layer 3 uses a classical technique: the Huffman code. This is used after the actual data compression has taken place to encode the digital information. It is, therefore, not a compression system but a very efficient encoding technique. The Huffman algorithm generates a code of variable length and a whole number of bits. Important signals are allocated a short code, less significant ones, a longer code.

Since Huffman codes have a specific header, they can be decoded perfectly in spite of the variable length. Decoding is very fast since use can be made of a table. The technique gives a space saving of some 20 per cent.

The Huffman technique is an ideal complement to the perception-dependent compression. In passages containing many frequencies simultaneously, the perception-dependent encoding provides an appreciable reduction by eliminating masked signals. Since few identical signals occur, the Huffman code has little effect.

During passages with few different sounds, not many masking effects occur. This is when the Huffman code saves considerable space since there is much redundant information. Such passages can, therefore, be represented by short codes.

[992001]

Table 2. The modes of MPEG-1 audio

<i>Compression factor</i>	<i>method</i>	<i>comments</i>
1:4	via Layer 1	stereo signal results in a bit stream of 384 kbit/s
1:6 – 1:8	via Layer 2	stereo signal results in a bit stream of 256–192 kbit/s
1:10 – 1:12	via Layer 3	stereo signal results in a bit stream of 128–112 kbit/s



There is much information and many links at www.mpeg.org.

Table 3. Facilities available with MPEG-1 Layer 3

<i>Sound quality</i> <i>Compression factor</i>	<i>Bandwidth (kHz)</i>	<i>Mode</i>	<i>Bit rate (kbit/s)</i>
Telephone 1:96	2.5	mono	8
Better than shortwave 1:48	4.5	mono	16
Better than medium wave 1:24	7.5	mono	32
FM radio 1:24 – 1:26	11	stereo	56–64
Near-CD 1:16	15	stereo	96
CD 1:12 – 1:14	> 15	stereo	112–128

With a modest number of components, the standard PC printer port can be transformed into an I/O system with up to 256 I/O lines. This article completely describes both the hardware and the necessary BASIC software. The hardware can also easily be controlled using other programming languages.

Design by V. Himpe

printer port extension

up to 256 I/O lines on a standard printer port

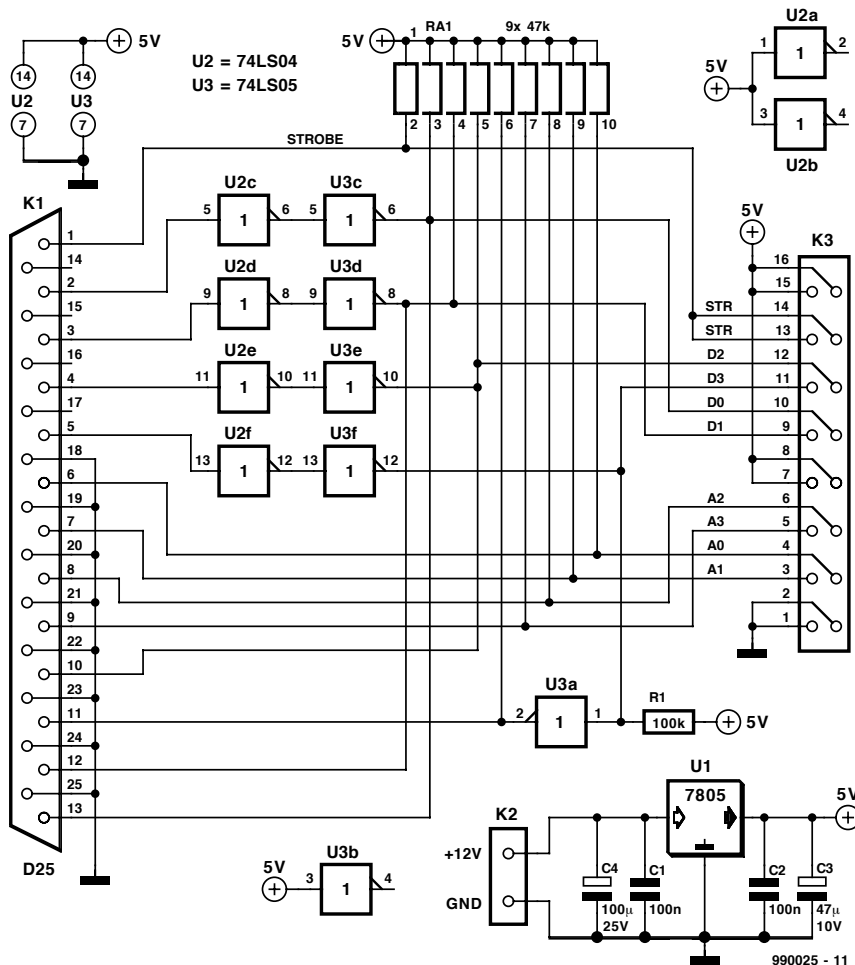


Figure 1. The schematic diagram of the bus unit, which is the heart of the I/O system.

It can hardly be said often enough that the PC was primarily developed to meet the needs of the office environment. This basically means that in the overall design, a lot of attention has been given to connecting standard peripheral equipment, such as printers and modems. Analogue and/or digital inputs and outputs, which would be useful to the user who wants to perform control tasks, are thus simply not present in a standard PC configuration.

The circuit that is presented here, or better said the complete system, was originally named 'Paraport' by its developer, since it is an I/O extension for the parallel port. It provides a large number of digital I/O lines for a normal PC at a modest cost. If you decide on the maximum configuration, this amounts to 256 lines. Although it might seem natural to arrange these as 128 inputs and 128 outputs, you are free to divide the lines between inputs and outputs as you desire.

The inputs work with TTL levels, while the outputs have buffers with open-collector outputs, so that they can directly switch relatively heavy loads. Thanks to the modular nature of the design, you can build exactly the amount of hardware that is needed to satisfy your specific needs. There is thus no need for any unnecessary investment, and the hardware can be kept as compact as possible.

Design approach

As already mentioned, this project is based on a modular design. There are

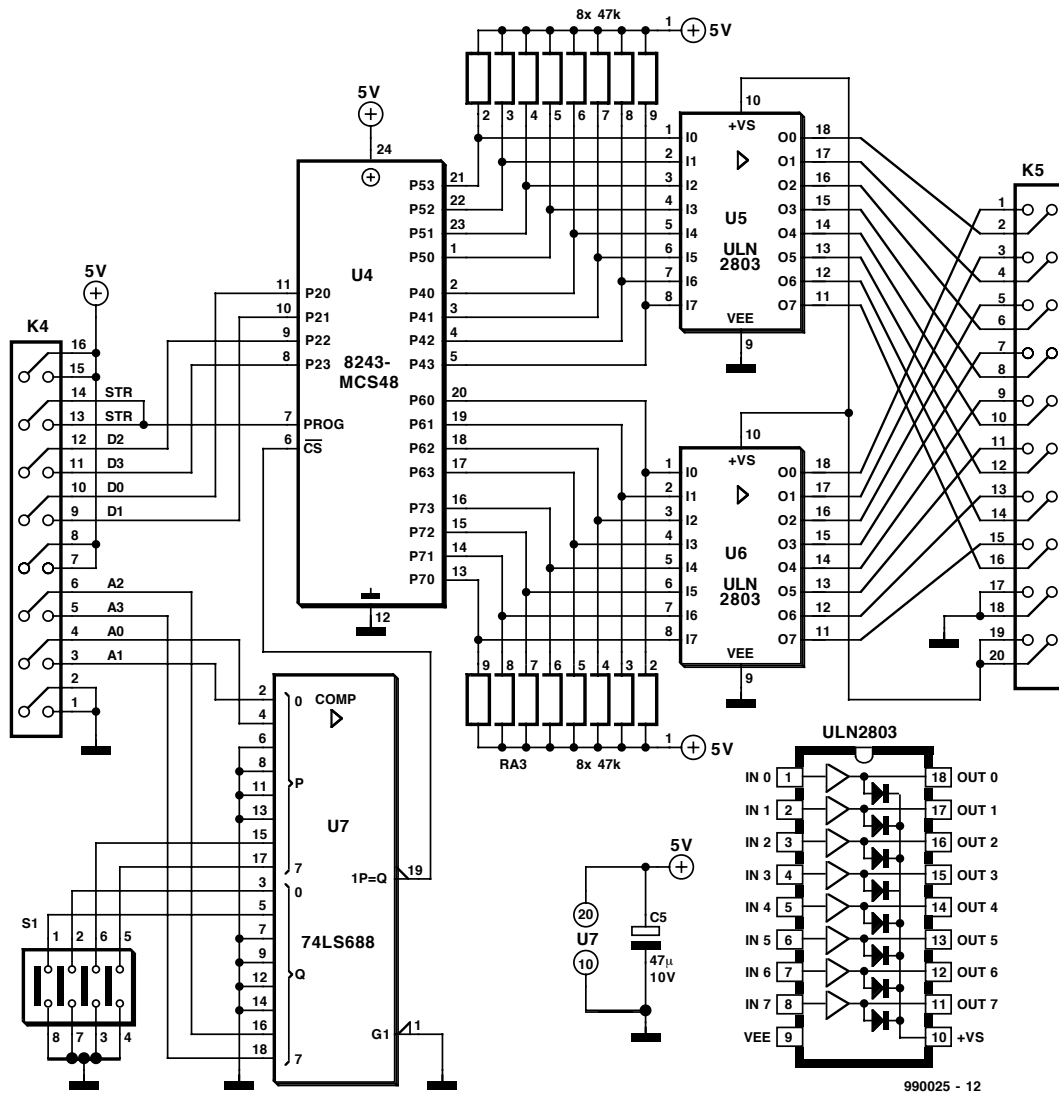


Figure 2. Up to 16 of the I/O units shown here can be connected to the bus unit.

two types of units: an interface to the printer port (the bus unit) and the actual I/O unit. Each I/O unit provides eight TTL-compatible inputs and 8 buffered outputs. Up to 16 I/O units can be connected to the bus unit. In the maximum configuration, a total of 17 circuit boards are thus connected to the printer port.

The hardware

Figure 1 shows the design of the bus unit. This circuit contains a number of inverters that adequately buffer the printer port signals. Since the standard printer port is intended to function primarily as an output port, recourse is made to several control lines of the port for input data. The data lines D0 through D3 from the PC are used for data output, and the control lines Acknowledge, Busy, Paper Empty and Select are used for data input. The remaining four outputs (D4 through D7) are used to address the sixteen I/O modules. Finally, the Strobe signal has

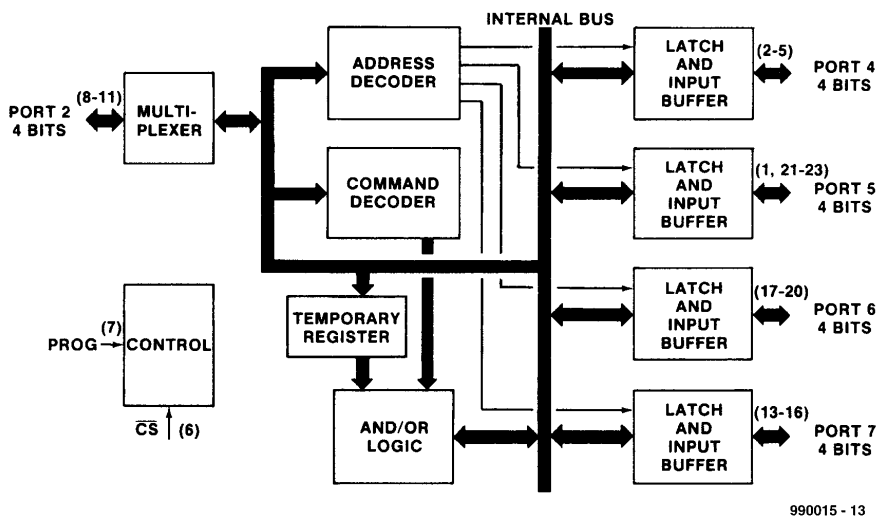


Figure 3. The internal structure of the 82C43, a controller with five 4-bit ports.

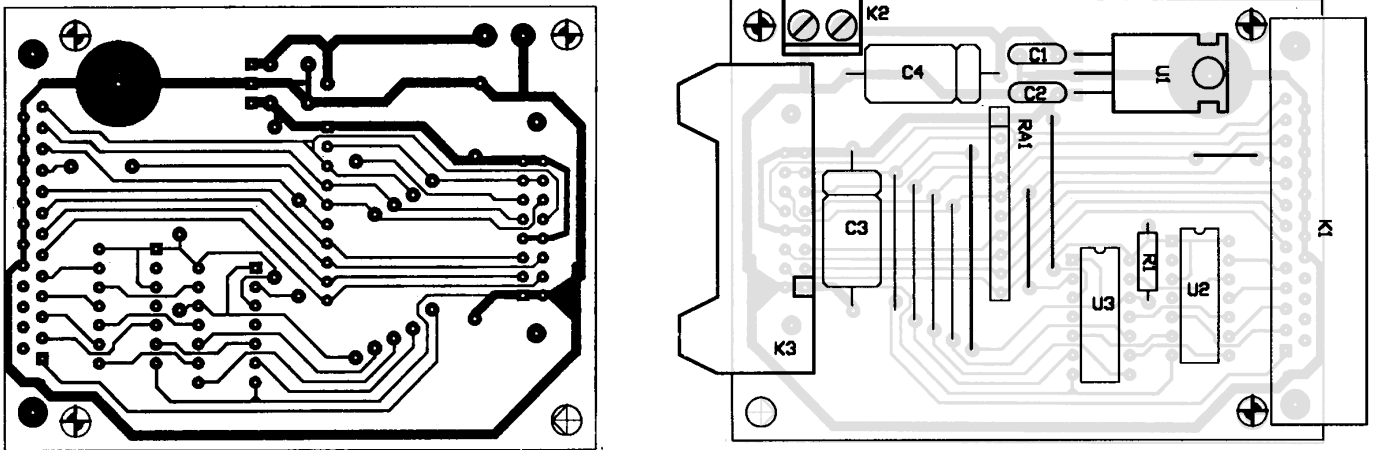


Figure 4. The copper-track layout and component overlay for the bus unit card, as made by the author.

COMPONENTS LIST

bus-unit

Resistors:

R1 = 47k Ω
RA1 = SIL array 9 x 47 k Ω

Capacitors:

C1, C2 = 100nF
C3 = 100 μ F 25V
C4 = 47 μ F 25V

Semiconductors:

U1 = 7805
U2 = 74LS04
U3 = 74LS05

Miscellaneous:

K1 = 25-pin angled sub-D connector, male, PCB mount
K2 = 2-way PCB terminal block
K3 = 16-pin boxheader, angled, with eject levers

also been assigned a function. It ensures that the I/O system reads the data on the D0 through D3 lines at the proper time; these lines are used for both data and commands. Only one such bus unit per printer port is needed for this project.

Modular design

The I/O units are connected to the bus unit. **Figure 2** shows the design of a single I/O unit. The heart of this unit is an 82C43 IC, which is a port expander chip that was specifically developed by Intel to expand the I/O capabilities of its 8048 processor (the predecessor of the 8041/51 processors). For those of you that are not familiar with the operation of the 82C43, a short explanation is in order. The IC is supplied in a 24-pin package and contains five 4-bit bi-directional ports (labelled P2, P4, P5, P6 and P7) and two control inputs (PROG and CS). **Figure 3** shows the internal organization of the 82C43. The

COMPONENTS LIST

I/O-unit (up to 16 off)

Resistors:

RA1, RA2 = SIL array 8 x 47k Ω
U5, U6 = DIL array 8x330 Ω *

Capacitors:

C5 = 10 μ F 25V

Semiconductors:

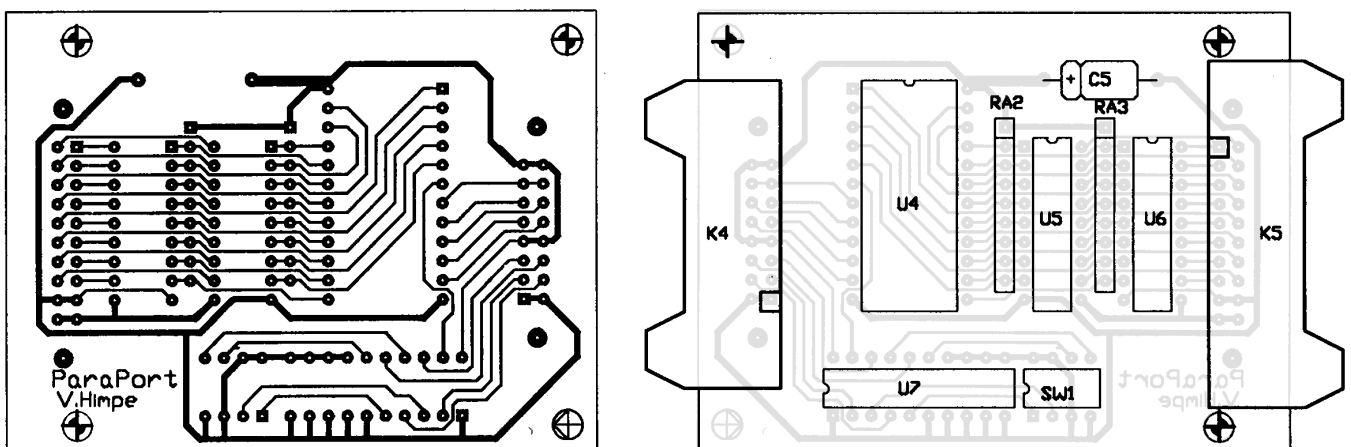
U4 = 82C43 or 8243 (Intel)
U5, U6 = ULN2803*
U7 = 74LS688

Miscellaneous:

K4 = 16-pin boxheader, angled, with eject levers
K5 = 20-pin boxheader, angled, with eject levers
SW1 = 4-way DIL switch

* see text

Figure 5. The copper-track layout and component overlay for the I/O unit.



port numbering may seem to be a bit strange, but this is due to the fact that this IC was intended to be used in combination with an 8048 microcontroller, which already has several ports of its own.

One of the 4-bit ports (P2) is used for communication with the printer port, and is thus connected directly to the printer output lines D0 through D3. This leaves 16 lines free for I/O functions. The Strobe signal from the printer port is connected directly to the PROG input of the 82C43, and thus controls data input. The remaining control input of the 82C43 (CS) is connected to an address decoder based on a 74LS688.

The 74LS688 is an old acquaintance. It is a word comparator that is very often used in address decoders, as in this project. The module address is selected by the 4-pole DIP switch SW1, in the range of 0 through 15. If the address selected by SW1 is equal to the value present on the address bus, the decoder output goes low, which selects the I/O unit in question.

As can be seen from the schematic diagram, every I/O line has the same structure. This means that every line can be used as an input line or an output line, as desired. However, the selection (either input or output) must be made for a set of eight lines at a time, since the buffers used here are packaged eight to a chip.

If a set of lines is to be used as inputs, the associated integrated buffer (ULN2803) must be removed and replaced by an 8-position, 330-Ω resistor array. This array must be housed in a DIL package, so that it can be plugged into the socket provided for the buffer IC. When inserting the resistor array, you must be sure that all inputs are connected to their associated outputs. They are all arranged directly across from each other, so the only thing you need to do is to take care that the resistor array is properly inserted in the socket. When it is correctly placed, pin positions 9 and 10 of the socket will be open. The pull-up resistor array ensures that open inputs are held at a defined logic level. Since the inputs are only suitable for TTL signals, the actual input signals must naturally also conform to this standard.

If a set of lines is to be used as outputs, the associated ULN2803 must be installed. This IC has open-collector outputs. Since the loads connected to the outputs may be inductive, each output has a built-in protection diode. The cathodes of all these diodes are

```
' REM PARAPORT programming example
' Witten by Vincent Himpe

' printer port initialisation
' LPT1= &h378 &h379 &h37A
' LPT2= &h278 &h279 &h27A
' PRN = &h3BC &h3BD &h3BE

' controller instruction set
' read      = 0
' write     = 4
' Write_or  = 8
' Write_and = 12

' ports numbered 0 through 3 :
' this corresponds to chip ports
' 4 through 7 (pin names)

'***** initialisation *****
OUT &h378,255 ' set all to 1
OUT &h37A,0   ' pull strobe high

'***** Write *****

' formula to compute command word:
' (Car address *16)+command+port
' example : write to port 2 on card 1
' (1*16)+ 4 +1 = 21

out &h378,21 ' card address + port address + command
out &h37A,1  ' strobe low

' formula to compute data:
' (Car address*16)+data
' so in this case (1*16)+data
' for testing we make the 2 last bits high HLL = 12
' so the result becomes : (1*16)+12 = 28

out &h378,28 ' prepare data
out &h37A,0  ' strobe high

' data now available on desired port

'***** Read *****
' Command formula: same as with writing, but using diff. command
' (1*16)+0+1 = 17

out &h378,17 ' card address + port address + command
out &h37A,1  ' strobe low
out &h378,255 ' set controller outputs to high-Z

value = inp(&h379) ' read
value = ((value and &hF0)/16) ' extract highest nibble
out &h37A,0 ' strobe high

'***** end *****
```

Figure 6. A BASIC program that can be used to control the I/O system.

connected to the V_p pin. They can thus be connected to the highest-available potential via connector K5. The earth pin is connected to the system earth. Each buffer can switch voltages up to 50 V and currents up to 500 mA, which is more than adequate for most applications.

Compact hardware

Figure 4 shows the copper-track layout and the component overlay of the

printed circuit board for the bus unit, while Figure 5 shows the same for the I/O unit. Both types of circuit boards are single-sided, so that you can easily make them yourself. The price of this approach is that several wire jumpers are needed on the bus unit card. Fortunately, only one of these has to be built, so this is not a particularly onerous disadvantage.

A length of flat cable can be used to connect the I/O units to the bus unit, since headers are used for the con-

nectors on the bus side (K3 and K4). If the I/O cards are mounted one on top of the other using 10-mm spacers, the whole system can be constructed as a compact and sturdy assembly. The desired address for each I/O card must be selected using the associated DIP switch; each unit must have its own (unique) address.

A mains adapter with an 12-V DC output can be used to power the system. The 5-V supply voltage produced in the bus unit is provided to the various I/O units via the bus cable.

A few lines of BASIC

Most hardware also needs some kind of software, and that is true for this project. Before delving into the software, it's necessary to give a little more attention to the 82C43. Since this IC was specifically developed to work with an 8048 controller, a special procedure must be used to write to and read from its registers. This approach, which allows data to be read into or written from the 8048 with a single

Table 1. Port selection.

input/output address code		selected input/output
P21 (D1)	P20 (D0)	
0	0	4
0	1	5
1	0	6
1	1	7

instruction, can also be used to advantage here.

The 4-bit bus can be used for both data and commands. To send a command to the IC, the command bits must be placed on the bus and the level of the Strobe line then switched from high to low. Data can then be transferred by placing the data bits on the bus and switching the Strobe line back to high.

The 82C43 recognizes four basic commands: Read, Write, Write_AND and Write_OR. Logically enough, Read is used to read data and Write to write data, so these commands need no further explanation. With Write_AND, the new data written to the IC are log-

Table 2. Command selection.

Command		Function
P23 (D3)	P22 (D2)	
0	0	Read
0	1	Write
1	0	ORLD
1	1	ANLD

ically ANDed with the data that are already present in the selected port, and the result is retained in the port. With Write_OR a similar process takes place, except that a logical OR is performed instead of a logical AND. The manner in which the various ports are selected and the way that the various functions are activated are described in **Table 1** and **Table 2**, respectively. As can be clearly seen from the program listing in Figure 6, it is not at all difficult to work with this circuit in actual practice. If you study this simple program, you will learn all that you need to know to be able to use all functions of the I/O system.

WHEN ELECTRONICS WAS YOUNG (2)

Birth of the battery

Count Alessandro Giuseppe Anastasio Volta (1745–1827) belonged to an aristocratic family and was Professor of Physics at the universities of Como and Pavia. He became interested in a phenomenon described by Galvani in 1786 to the effect that “an electric spark, or contact with copper and iron, causes a frog’s leg to twitch”. This gave rise to the, fortunately short-termed, belief that animal tissue was necessary for the generation of electricity.

Experiments showed Volta that an electric current could be generated by bringing different metals into contact with each other. There are different versions of which metals he used: some writers claim silver and zinc, others, copper and zinc. In 1799, he succeeded in making a construction of metal discs, alternately silver (or copper) and zinc, with brine-soaked card between them. This ‘voltaic pile’ as it became known was the first man-made source of electricity. Its invention was made known by Volta to Sir Joseph Banks, President of the Royal Society, in a letter in early 1800. In this letter, Volta says that he used 25 mm dia. copper and zinc discs. After his invention was made known, Volta did little further work on the device. His name survives, however, in the SI unit of electric potential difference, the volt.

It is interesting to note that in 1848 Scyffer in his *Geschichtliche Darstellung der Galvanisms* (Historical Notation of Electric Phenomena) states that others besides Volta carried out experiments with dry cells between 1800 and 1812, namely Ludicke, Einhof, Ritter, Hachette, Desornes, Biot, and others. Several physicists of that era, particularly Zamboni, expressed as their opinion that the best performance was not that of Volta but that of De Luc.

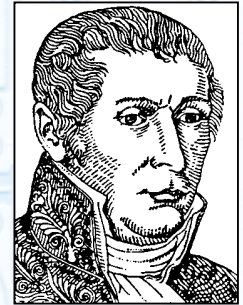
Be that as it may, Volta’s invention transformed the study of electricity and was, therefore, invaluable to men

such as Nicholson, Davy and Faraday. It also put paid to the belief that animal tissue was needed for the generation of electricity.

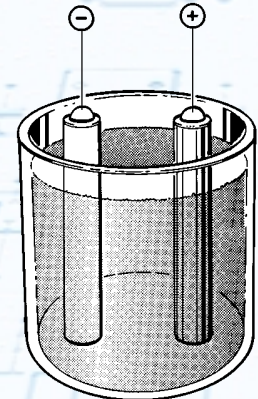
It may be said that all this work in the early part of the 19th century was experimental. The first reliable, practical source of electric current, based on the interactions of carbon and zinc in an electrolyte consisting of, among others, ammonium chloride, manganese dioxide, zinc chloride and water, was described by the French physicist Georges Leclanché in 1868. The Leclanché cell, improved many times since its inception, remains the best known dry or primary cell in common use today.

The secondary battery, invented in 1803 by Johann Wolfgang Ritter (1776–1808) consists of discs of one metal separated by circular pieces of cardboard that are moistened in a liquid that cannot chemically affect the metal. When the extremities of this pile are linked to the poles of a voltaic pile, it becomes electrified and can be substituted for the latter and it will retain the charge.

However, the first practical secondary battery, the lead-acid battery, was produced in 1859 by another French physicist, Gaston Planté (1834–1889). In spite of all sorts of other type of secondary battery, the lead-acid battery remains the most widely used secondary battery in the world today.



Alessandro Volta (1745 ... 1827)



[905016-1]

Volta's cell

electronics on line

CPU coolers and boosters

faster and cooler with just software

Making the computer run faster is probably every user's desire. However, not everyone is prepared to invest in a faster CPU or motherboard upgrade. Fortunately, in some cases the computer may also be given a speed boost by software or hardware tricks.

Features	Waterfall Pro 1.2	Waterfall 1.23	Rain 1.0
System Performance	Best	Very Good	Very Good
Cooling Performance	Very Good	Good	Very Good
Security	Best	Very Good	Good
Memory Requirement	76KB	300KB	300KB
CPU Optimization	Yes	Yes	Yes
File System Optimization	Yes	No	No
Memory Swapping Optimization	Yes	No	No
Plugin Sensor Module	Yes	No	No
CPU Throttling	Yes	No	No
CPU Monitor	Yes	Yes	No

Freeware or Shareware?
 Although we truly believe in the concept of 'freeware', Waterfall Pro was very expensive to develop because of the amount of hardware that we had to purchase (in order to support them with sensor module drivers). Therefore, all that we're doing is trying to cover our expenses, which is only fair.

A computer is always too slow. Especially if you are a power user running the latest software, a few megahertz extra are often more than welcome.

Fortunately, you don't have to buy a new hardware kit to make your computer a bit faster — there are other ways! Overclocking the CPU is still among the most popular alternatives. Essentially, the CPU is given a clock signal that is faster than the one it is officially rated for by the manufacturer, for example, 350 MHz instead of 300 MHz. This works on nearly all Intel CPUs (with a few tricks, though), as well as on those from AMD and IBM/Cyrix. Lots of information on overclocking methods, results and related aspects may be found at www.sysopt.com/overc.html and www.tomshardware.com/overclock.html.

A major problem with overclocking is the extra heat the processor will produce as a result of the higher clock frequency. Increasing the size of the heatsink/fan combination may not always be sufficient. Fortunately, a couple of small programs are available on the Internet that lend a helping hand in preventing early CPU demise as a result of overheating. Basically, these programs insert halt instructions in the program code when the CPU idles. In this way, the CPU temperature can be made to drop by 10-20 degrees. Some programs go one step further, providing extra functions such as guarding

the CPU voltage and temperature. The three best known are:

- Waterfall and Waterfall Pro**
cpu.simplenet.com/leading_wintech/
- Rain**
cpu.simplenet.com/rain10.zip
- CPUidle**
www.stud.uni-hannover.de/~goetz/

There are also ways to make the CPU faster by changing a couple of internal settings. Once a popular method with the earlier CPU generations produced by Cyrix and AMD, it is no longer necessary with the latest CPU types. One program, **CPU booster**, should be mentioned here, however, because it

may be useful to owners of 'older' computers. It may be found at www.geocities.com/SiliconValley/Vista/7532. The maker of this program claims that it speeds up nearly all older processors without having to increase the clock frequency. For the rest, the story is a bit murky. None the less, we did give the program a test spin on a couple of computers in our offices. The results varied widely. No speed increase was noticed on newer PCs, but users of older ones with a 486 or older Pentium at least were under the impression that the machine went faster, so we say it's worth trying.

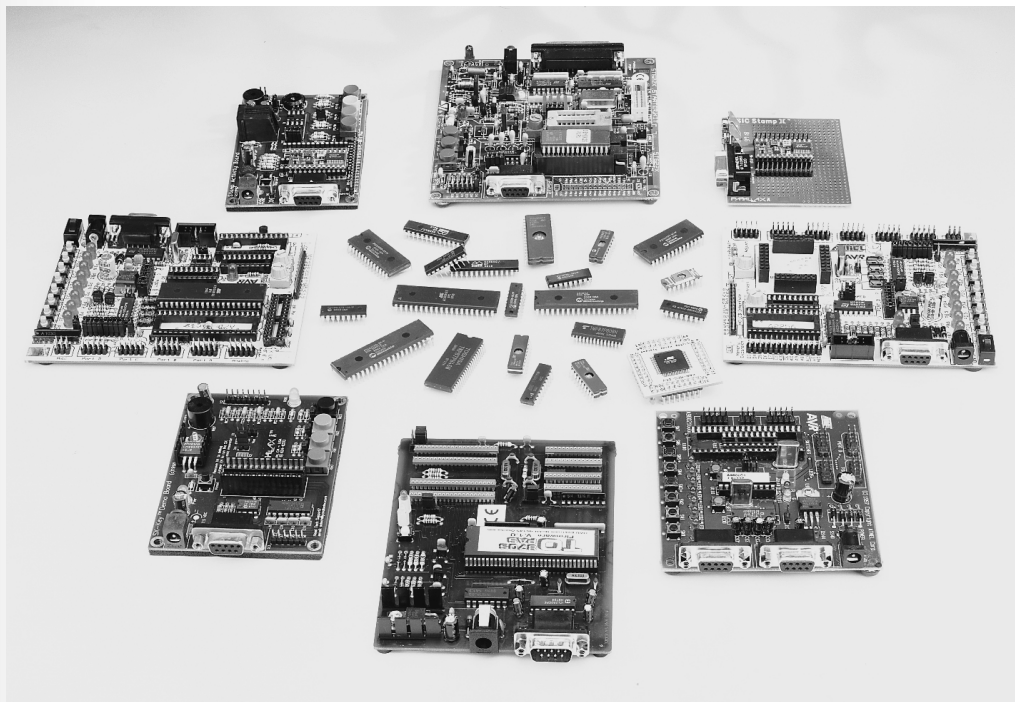
(995013-1)



microcontrollers' survey

news from the world of bit crunchers

These days a perplexing number of microcontroller types are available. Embedded, single-chip, RISC, 8-bit, 16-16, surface-mount, flat-pack, you name it, it's turmoil! The microcontroller world is bustling with activity, and there are new arrivals almost every week. In this article we will look at some of the latest developments in this ever-active field.



Although there is only a small and very slow increase in the number of microcontroller manufacturers, this is in stark contrast with the rocketing number of different versions, types and sub-types of these components. With this in mind, we had to limit ourselves to look at the latest developments only. So, instead of a complete overview of all microcontrollers currently available on the market we will concentrate on those products that can be called 'recent introductions'.

ATMEL

Founded not so long ago (in 1984), Atmel, in just a few years, have become one of the major forces in the microcontroller market. Atmel have always excelled at offering a product range that meets even the most extravagant demands from designers of microcontroller-based systems for a wide variety of applications.

Below are short descriptions of

Atmel's most recent products.

AT90S8535, this one has an 8-kByte ISP Flash program memory, 512 kBytes of ISP (in-system programmable) EEPROM and an identical amount of SRAM for data;

AT90S4434 and **AT90S4433**, both having 4 kBytes of Flash ISP program memory, 256 bytes of ISP EEPROM, and 256 and 128 bytes of SRAM data memory;

ATmega603 with a massive 64 kBytes of ISP Flash program memory, 2 kBytes of ISP EEPROM and 4 kBytes of SRAM for data storage.

Taking the ATmega103 as an example (from which the ATmega603 is a derived version), you are looking at a microcontroller with the computing power of a PC of about 15 years ago (128 kBytes ISP Flash memory, 4 kBytes ISP EEPROM, and 4 kBytes SRAM). The new device has 120 instructions, it can be programmed externally or in-

By our Editorial Staff

system (ISP), its clock rate is 6 MHz, it has 32 input/output lines, three timers, an 8-channel 10-bit converter, a real-time clock (operating at 32 kHz), and a UART, all in a 64-pin TQFP package.

One of the best things about the megaAVR controllers (which, by the way, are 8-bit types), is that they allow the complete 16-bit instruction to be loaded and stored in one operation, using two addresses.

Another novelty is the ATtiny11, which is actually a low-voltage controller. The relevant supply voltages are 3 V for the ATtiny11 and 1.8 V for the ATtiny 11L. Its sole memory element is a 1-kByte Flash memory. This controller has 90 instructions, and is supplied in an 8-pin case!

With the introduction of the AT91 ARM Thumb, finally, Atmel ventures out into 16/32-bit ARM RISC technology.

The most recent model is the AT91M40400, which is also the latest device in a family of standard microcontrollers based on the ARM7TDM1 core. The ARM91M40400 is a fully static component capable of achieving 30 MIPs at a clock speed of 33 MHz and a low supply voltage between 2.7 V and 3.3 V. This device has rather a lot of peripheral circuitry, including data and address buses with a width of 32 bits, 37 registers with the same width, and an in-circuit emulator interface. It contains 4 kBytes of SRAM.

DALLAS SEMICONDUCTOR

As far as its microcontrollers are concerned, Dallas Semiconductors can not be said to have followed an innovative course. Rather, the accent has been on increasing speed and computing power. The series of microcontrollers currently produced by Dallas Semiconductor operates at clock rates up to 33 MHz. However, since they use only 4 clock cycles rather than 12 (for an 8051) to execute an instruction, these microcontrollers appear to run at a speed of 99 MHz.

The latest products from Dallas Semiconductor include:

DS80C130

A high-performance replacement of the 8051, without ROM or XRAM, but having 56 bytes of protected RAM.

DS80C320

Identical to the 80C130 but having an on-chip watchdog and a supply level monitor. The DS80C323 is the 3-V version.

DS87C250

This controller has 16 kBytes of EPROM (OTP), 1 kBytes of SRAM, and various Power Management and EMI Reduction modes. The DS83C520 is a version with masked ROM, and the DS87C530, one with a real-time clock (RTC) and an NV RAM controller.

DS87C530

Integrating a real-time clock, the DS87C530 is compatible with the 8051, although it offers better performance and lower power consumption. The revised core needs only 4 clock cycles to execute an instruction, as opposed to 12 for the 8051. In fact, it offers the same performance as an 8051 running at 99 MHz. This new microcontroller offers 16 kBytes of EEPROM (UV or OTP), 1 kBytes of non-volatile MOVX SRAM, 2 serial ports, a watchdog timer, a supply voltage guard, dual data pointers, and advanced power management techniques. The device is, we believe, ideal for data logger systems.

ISSI (INTEGRATED SILICON SOLUTION, INC.)

The IS89C52 from ISSI is an 8-bit microcontroller with 8 kBytes of reprogrammable Flash memory. Capable of operating at a highest clock speed of 40 MHz the IS89C52 is without doubt one of the fastest microcontrollers in its class. As suggested by the type number, the new microcontroller is functionally compatible with the industry-standard 80C52 device. It offers, among others, 256 bytes of RAM, a serial I/O port suitable for multi-processor communications, and I/O extension circuitry plus a full-duplex UART. Sporting no fewer than 3 timer/counter units, the IS89C52 has four 8-bit input/output ports with a total of 32 input/output lines. Its memory addressing capacity is 64 kBytes of ROM and the same amount of RAM. The device is capable of protecting the program memory using encrypted verification (32 bytes), and lock-out bits (3 bits).

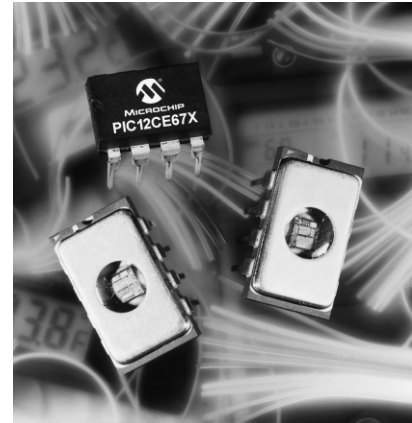
MICROCHIP

Microchip recently released five new microcontrollers on the market. The new PIC16CE62X and PIC12CE67X PICMicro™ families now offer protected EEPROM memory.

These 8-bit one-time programmable (OTP) microcontrollers present unbeatable security. In fact, to gain access to the EEPROM, the memory of the PIC16CE62 and PIC12CE67X has to be reprogrammed, which, in the case of OTP devices, is impossible! The new devices are claimed to be the smallest one-time programmable 8-bit RISC controllers in an 8-pin case. Offering one million write/clear cycles, Microchip's EEPROM technology also guarantees the longest period of data retention: more than 40 years.

The PIC16CE623, 624 and 625 offer 512 to 2048 words of one-time programmable memory, 128 bytes of EEPROM, and 96 up to 128 bytes of static RAM for data storage.

The PIC16CE673 and 674 are the first 8-pin microcontrollers in the world



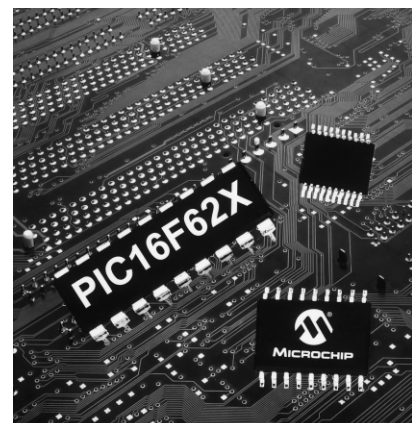
with an on-chip 8-bit analogue-to-digital converter (ADC) as well as an EEPROM. Offering 1024 and 2048 OTP program memory with a word width of 14 bits, these integrated circuits also contain 128 bytes of static RAM and 16 x 8 bytes of EEPROM data memory.

PIC17C7xx (752, 762 and 766)

These microcontrollers take us to the 16-bit limits. Although they are strictly speaking 8-bit OTP microcontrollers, the devices in Microchip's PIC17Cxxx series offer functionality and performance levels that compete with 16-bit devices. These components in 64-pin and 84-pin cases contain 10-bit A-D converters and two high-speed USARTs. These PICs achieve a performance of 8.25 MIPs at a clock rate of 33 MHz, and so even surpass certain competing devices like the Motorola MC68HC11 and Hitachi's H8. Offering up to 16 kwords of 16-bit program memory in OTP EPROM and up to 902 bytes of user RAM, these new circuits comprise a one-cycle (120-ns) hardware 8x8 multiplication unit, and options for high-speed communication on 2 channels (duplex) using a USART with a speed of 8.25 million bits/s.

PIC16CR54C and PIC16C505

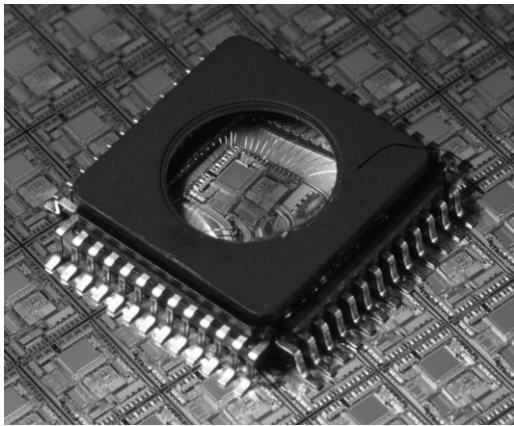
It seems that these devices actually are the most economic 8-bit OTP ROM controllers currently on the market. The PIC16CR54C, a ROM-based controller, and the PIC16C505, a one-time programmable chip, offer a galaxy of functions at a very low price. Packaged in a 14-pin enclosure, it is the first 8-bit



microcontroller to expand the possibilities of 8-pin designs with more I/O capacity, all at a cost of less than 50 dollar cents in volume quantities.

The PIC16C5050 has a memory with a capacity of 1024 words of 12-bits, 72 bytes of user RAM, 12 I/O pins, a wake-up circuit activated on I/O line state changes, and an internal 4-MHz clock oscillator. It is also capable of being programmed in-circuit, which means that the microcontroller does not have to be removed from the printed circuit board to receive a new program.

The ROM-based PIC16R54C is an 18-pin controller with a program memory of 512 words of 12 bits, 25 bytes of user RAM, and 12 I/O pins. These two circuits offer 33 one-word instructions, a programmable watchdog function with an on-chip RC oscillator for no-break operation, an instruction cycle



time of 200 ns at a clock rate of 20 MHz, 7 hardware registers for special functions, a 2-register hardware stack, an 8-bit real-time timer/counter, a wide range for the supply voltage, and, last but not least, low power consumption: 2 mA at a clock rate of 4 MHz and a supply voltage of 5 V.

The following are the latest models announced at the Munich 'Electronics 98' exhibition.

PIC16F877 and PIC16F876

These new microcontrollers contain 8 kwords of 14-bit enhanced Flash memory, and 256 bytes of EEPROM-resident data memory. They offer the widest operating voltage known in the industry, namely between 2.0 V and 5.5 V. These are also the first controllers to employ Microchip's new MM (*Migratable Memory*) technology for the greatest possible system performance and design flexibility (say Microchip). The MM technology effectively ensures pin-for-pin and software compatibility of all microcontrollers, ROM-based, one-time programmable (OTP), or their Flash equivalents, and allows designers to choose the memory technology as a function of the expected application lifetime. It also enables easy migration

to more cost-effective solutions, if necessary. These components contain a 10-bit A-D converter with 5 to 8 channels, a UART with RS485 compatibility for data acquisition applications in multi-channel systems, a computing performance of up to 5 MIPs at a clock speed of 5 MHz, options for I²C bus communication or SPI for system expansion with peripheral circuits, and, finally, two 8-bit and one 16-bit timer.

A number of precision timing interfaces allow quantities to be captured and compared (16 bits) at respective resolutions of 12.5 ns and 200 ns, or PWM (pulsewidth modulation) signals to be generated with frequencies up to 20 kHz and a resolution of 10 bits. The devices allow up to 1,000,000 clear/program cycles, which is the highest number achieved in the industry today.

The PIC16F877 and PIC16F876 are the first 8-bit RISC-type PICmicro® controllers to integrate enhanced Flash memory technology.

PIC16F627 and PIC16F628

These new components comprise an internal 4-MHz clock oscillator, high-precision voltage comparators, a high-speed USART, and a capture/comparison/PWM module. These 18-pin microcontrollers contain 1024 and 2048 of 14-bit wide Flash program memory respectively, besides 224 bytes of RAM and 128 bytes of EEPROM for data storage. The highest clock speed is 40 MHz.

PIC16C733 and PIC16C774

These 8-bit microcontrollers integrate a sophisticated analogue technology for direct, programmable, interfacing to the power supply and for precision control of external systems. These parts, with 28 and 40 pins respectively, provide a complete system solution for mixed-signal environments, considerably reducing the number of discrete logic parts, associated parts and, of course, overall system cost. They integrate a 10-channel 12-bit A-D converter (± 1 LSB) and a precision voltage reference ($\pm 3\%$), a programmable voltage-drop detector, and a programmable low-voltage detector (both with a current drain of 50 μ A and an accuracy of $\pm 3\%$).

With 4 kwords of 14-bit wide OTP memory, the PIC16C773 and PIC16C774 contain an RS485-style UART for multiple-data acquisition purposes, offering a throughput of up to 5 MIPs at a clock speed of 20 MHz, two 8-bit timers, one 16-bit timer, as well as possibilities for industry-standard I²C and SPI communication buses.

MOTOROLA

Motorola recently introduced a new version of its 68HC08, the **68HC908GP20**, which, because of its in-system programmable (ISP) Flash

memory, is said to be completely state-of-the-art. The GP20, as Motorola calls it, has 19,968 bytes of ISP Flash memory, 512 bytes of RAM, and offers a novel option called *Auto Wake-up Out of Stop*. It will faithfully run all instructions of the 68HC08, and allows designers having worked with the 68HC05 to upgrade to a larger model.

Silently, Motorola has also switched over to the use of Flash memory. The product range currently includes the 68F333, 68HC916Y1 and 68HC916X1.

Finally, we should not forget to mention the introduction of Motorola's new **68HC(7)05SB7**, which is basically a new version of the 68HC705. This chip was specifically developed for *Smart Battery* applications.

At the 16-bit microprocessor front, Motorola has three families available, the 68000, 68HC12 (in more than 10 different versions) and the 68HC16 (which comes in 8 different flavours).

NATIONAL SEMICONDUCTOR

National Semiconductor has really just one series of microcontrollers available, the COP8. This is an 8-bit processor which comes in no fewer than 82 different versions. The OTP versions of the COP8 have memory capacities of between 4 and 32 kBytes of OTP EPROM.

Quite recently, National Semiconductor launched a new OTP microprocessor called **COP8SGR7**. Having an EPROM memory of 32 kBytes, its price is remarkably low at less than 5 dollars for 1k+ order volumes.

Another recent arrival, the **COP8SGE7**, comes with 8 kBytes of OTP memory.

With its huge memory capacity, the COP8SGR7 allows designers to drastically reduce development time because there is no longer a need to compact the program code to make it fit in a memory (which is always too small!). Once the program has been tested and debugged, it may be burned into a ROM-based COP8 processor.

The COP8 family was recently extended with five new members: the COP8SGE5 (8 kBytes ROM), COP8SGG5 (16 k), COP8SGH (20 k), COP8SGK5 (24 k) and the COP8SGR5 (32 k).

All members of the COP8SGx family have a full-duplex UART/USART which is software programmable to enable quick implementation of various communication protocols. A pair of analogue comparators is available to detect zero-crossings, or for implementing a regular or 'dual-ramp' A-D converter function. These controllers have either 256 (SGE) or 512 (SGR) bytes of RAM.

The COP8SGR7 and COP8SGE7 guarantee perfect protection of the

intellectual copyrights vested in the firmware code. Once the code has been made secure by means of an optional protection mechanism, the program is virtually impossible to 'hack'.

Finally, we should note that most applications of the COP8 family members are typically industrial.

PHILIPS SEMICONDUCTORS

Philips Semiconductors are obviously in a bid to offer the most extensive range of microcontrollers derived from the 'generic' 80C51.

89C51, 89C52, 89C54 and 80C58

The most recent microcontrollers from Philips Semiconductors are four Flash MTP (Multi Time Programmable) (sic, *Ed.*) Flash types in the extremely popular 80C51 family. These fledglings are called 89C51, 89C52, 89C54 and 80C58. The main point to make about these controllers is that they can be reprogrammed many times, and even in-system (ISP), which equates to a considerable reduction of two infamous factors, *cost* and *time to market*.

These new processors are capable of operating at up to 33 MHz, which makes them among the fastest 80C51 Flash processors currently available.

The difference between the various models is mainly the size of the on-chip Flash memory: 4 kBytes in the 89C51, and 8, 16 or 32 kBytes in the '52, '54 and '58 types respectively. The 89C51 has 128 bytes of RAM available, the other types, double that amount (128 bytes).

SCENIX SX-18, SX-28

Scenix may rightly claim to be the company with the fastest 8-bit microcontrollers currently available on the market. Operating at up to 50 MHz and capable of executing the majority of instructions in just one clock cycle, the 'SX' Flash EEPROM microcontrollers from Scenix are good for up to 50 MIPs, which means that they are 10 to 50 times faster than a traditional 8-bit microcontroller.

The main characteristic of the SX, besides showing new roads towards evolution for all users of 8-bit microcontrollers, is that it enables 'Virtual Peripherals' to be created (the term was obviously coined by Scenix). By virtue of the unmatched performance of the SX, the *Virtual Peripherals* are basically software implementations of functions that would otherwise require costly and dedicated hardware (mainly timers, PWM generators, and other serial ports).

There are actually two types of SX controller: easy to tell apart, really, because their number of pins is indicated by the type designation, 18 for the SX-18 and 28 for the SX-28.

The SX architecture is basically a copy of that used in Microchip's PICs. The SX is compatible with the PIC16C5x, and offers 10 additional instructions. One of the reasons for the technical success of the SX is the speed of its EEPROM program memory (2048 words of 12 bits) and its RAM-based registers (136 bytes) for data storage.

The instructions of the SX have a uniform length (12 bits) and most of them are executed in one clock cycle. Although the internal clock speed of the SX is 'just' 4 MHz, the controller outperforms a number of classic CPUs running at much higher speeds (12 or 33 MHz, for example), mainly because these require several clock cycles to execute a single instruction (12 cycles, for example, for the 8051).

Stop Press: Scenix just announced an addition to its production program: a new version of the SX18/28, called SX18/28AC100. As suggested by its type designation this number cruncher is capable of achieving a processing performance of up to 100 MIPs. Running at up to 100 MHz, the SX18/28AC100 executes one instruction in one clock cycle. At a data throughput of 100 MIPs, the resulting instruction cycle length is 10 ns. These two new versions sport 2 kwords of Flash/EEPROM memory with a width of 12 bits.

SGS-THOMSON MICROELECTRONICS

The ST6 Family

This is probably the best known series of 8-bit microcontrollers from SGS-Thomson. It comprises the following types: ST6200/1/3/8/9, ST6210/15/18, ST6220/25/28, ST6230/32, ST6240/42/46, ST6252/53/55, ST6260/62/63/65 and ST6280/85. Note that not all of these microcontrollers are available in a 28-pin or 40-pin DIL enclosure — a number of them are only supplied in a PQFP flatpack case.

Within this series, SGS-Thomson offers an EPROM, ROM and OTP version of each type. In this way, a good compromise is reached between design flexibility and low cost. The characteristics shared by ST6 family members include a maximum operating frequency of 8 MHz, a program memory with a size between 1 and 8 kBytes, and a RAM and (for some types) EEPROM capacity of 64 to 128 bits. The components that make up this series are specified to last 300,000 programming cycles, they have an on-chip 8-bit A-D converter, an SPI compatible serial interface, a UART, one (or two) 8-bit timers with pulsewidth modulation, and interrupt detection on all inputs.

The ST7 Family

This is the latest family of microcontrollers released by SGS-Thomson

Microelectronics. It is based on an architecture that is still actively employed for the design of microcontrollers for specific applications like PC displays, remote control units, CD players or car radios with RDS.

The members of the ST7 family differ in respect of on-chip memory size, ranging from a modest 4 Kbytes of program memory and 128 bytes of RAM in the ST72101 right up to 32 kBytes of ROM/EPROM, 1024 bytes of RAM and 256 bytes of EEPROM in the ST72331. The IC cases have 28 up to 56 connecting pins.

Among the options for peripheral circuits are an 8-bit multi-channel ADC, SPI interfaces, I²C, USB and CAN bus interfaces, and one or two 16-bit timers.

As far as performance is concerned, the ST72 series is situated about



halfway between the low-cost ST62 family and the ST9 family with 8/16 bit registers.

The ST72 family is expected to be extended shortly with a couple of new members specially developed for applications like controlling LCDs or brushless motors.

The ST9 Family

This series contains a number of microcontrollers which are generally referred to as '8/16-bits'. The best known types are the ST90135 and the ST90R158.

The ST10 Family

This series of 16-bit microcontrollers is often said to combine the advantages of CISC and RISC. It comprises the following integrated circuits: ST10R165, ST10R163, ST10F163, (128 kBytes Flash memory), ST10R166, ST10F166 and ST10F167. To these will be shortly added the ST10R272L and the ST10F168. Clock frequency is rated at up to 20 MHz and the memory is 128 kBytes Flash. These new controllers are compatible with the C16x

family from Siemens.

The ST20 Family

This is the 32-bit family of microcontrollers produced by SGS-Thomson.

SIEMENS

The C500 from Siemens is one of the most interesting microcontroller series. The latest addition is called **C505L**. This 8-bit device is offered as a *single-chip* solution. This processor, a descendant of the generic 8051, is the first to be supplied with an on-chip LCD interface.

The C505L is totally compatible with the industry-standard 80C51 and 80C52. It integrates a 32-kByte OTP memory, 512 bytes of RAM, a synchronous/asynchronous serial interface, and a very accurate 10-bit A-D converter boasting a conversion time of just 6 μ s. The on-chip LCD controller may drive a 128-segment LCD (i.e., 4 lines of 32 characters); it has 36 LCD outputs of which 20 are reserved for display functions. The remaining 16 outputs may be used as conventional I/O lines. At a clock frequency of 20 MHz, the cycle period is about 300 ns. The real-time clock on the chip also supports a *power-down* mode in which the current consumption drops to just 50 μ A (at a supply voltage of 3.3 V and a clock frequency of 32 kHz).

TEMIC

Temic recently launched their **TSC8051i2**, a new 8-bit microcontroller which, according to the manufacturer, integrates a multimaster I²C controller, analogue PWM outputs and a traditional watchdog circuit.

The two-wire I²C bus has become an industry standard mainly because it is so simple and versatile. The TSC8051i2 contains a multimaster I²C controller which presents an economic solution to designers wishing to implement the I²C bus.

As indicated by its type number, the TSC8051i2 is based on the architecture of Intel's 80C51. In addition to the multimaster I²C controller, the Temic micro contains 8 kBytes of OTP/EPROM or ROM, 256 bytes of RAM, 2 timers and a UART. It runs at a clock rate of 24 MHz at 5 V, and will soon be available in a 3-V version capable of running at 16 MHz.

ZILOG

In the wake of the famous Z8 from Zilog are a number of follow-up devices designated 'Z86'. This is quite a large family:

Z86C34/35/36/44/45/46, Z86E34/44, Z86144, Z8E001, Z86E02/C02/L02, Z86E03/06/C03/06/L06/16, Z86E04/C04/L04, Z86E08/C08/L08, Z86E30/31/40, Z86C33/43, Z86C83/84. There also exists a new series of

derived products called **Z8Plus**. The core of these controllers presents a number of advantages over the classic Z8 core. These advantages include higher processing speed resulting from a lower system clock pre-division factor.

When clocked at 10 MHz, controllers based on the Z8Plus core achieve a performance level equal to that of a classic Z8 running at 16 MHz. The first product is the **Z8E001**, an OTP device with 1 kBytes of program memory, a 64-bytes register array, 3 timers (including PWM) and an analogue comparator, all in an 18-pin case.

Z86144

This new product offers 16 bytes of EEPROM space which may be addressed in three different ways: (1) by user code, (2) externally by means of two interface protocols, or (3) in 'EEMODE' which allows programming and access on a byte-by-byte basis.

There are many other manufacturers of microcontrollers, including Analog Devices, Arm, Fujitsu, Harris Semiconductor, Hitachi, IDT, Mitsubishi, NEC, OKI, Samsung, Sharp and Texas Instruments. Because of various reasons their products could not be discussed in this survey.

CONCLUSION

Based on current market tendencies, the outlook is: more computing power, higher speeds. An increasing number of dedicated or application-specific

microcontrollers is noticed. These devices are tailor-made to perform one specific function only, often having very specific circuitry on board, as required by the application for which they were designed.

Note

The editorial staff is grateful to all companies and distributors who kindly responded to our requests by sending technical documentation, illustration material or even complete evaluation kits (Atmel).

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Internet addresses

Analog Devices :	http://www.analog.com
Arm :	http://www.arm.com
Atmel :	http://www.atmel.com
Cypress :	http://www.cypress.com
Dallas Semiconductor :	http://www.dalsemi.com
Fujitsu :	http://www.fujitsu-edc.com
Harris Semiconductor :	http://www.semi.harris.com
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Siemens :	http://www.siemens.de/semiconductor
Temic :	http://www.temic.de/e/index.htm
Texas Instruments :	http://www.ti.com
Zilog :	http://www.zilog.com

BTW an excellent search engine may be found at: <http://www.800go.com>.

general-coverage receiver

part 2 (final): construction and operation

Since publishing the first installment of this article, considerable interest has been expressed in the design by many of our readers. As always, however, the proof of the pudding is in the eating, and actually building the receiver is no mean job. Fortunately, ready-made PCBs are available, and the receiver is easy-going on adjustment.



Before discussing the construction of the general-coverage receiver, we think it is fair to warn that the project should not be attempted by beginners without any experience in building RF circuits. But that is not to say you may not try, assuming that you have considered the following conditions:

- you can rely on a more experienced 'ham' to help you;
- you are capable of working very accurately;
- you are not under the stress of meeting deadlines, say, for completing a school project or GCSE assignment;
- a set of plastic coil adjustment tools is available;
- you are willing and able to obtain all the parts as specified, preferably from a reputed kit supplier.

In the following discussions it is assumed that the constructor has reasonable experience in building RF circuits printed-circuit boards. Also, for terms and abbreviations used here,

you may have to refer back to part 1 of this article.

MAIN RECEIVER BOARD

The design of the main receiver board is shown in **Figure 4**. This is a pretty large board containing many discrete components. It is **double-sided, through-plated** and available ready-made from the Publishers (or through a kit supplier).

As you will not have failed to notice, the top side of the board acts as a ground plane which serves to keep RF interference (both radiated and picked-up) to a minimum.

Start by mounting the lower-profile parts on the board. As usual, check the value and, if necessary, orientation of each component before you mount it. For a change, the low profile parts include the following ICs: IC1 (TCA440), IC5 (MC145156), IC3 (MC3317), and IC4 (MB501L). These ICs are not mounted in sockets to ensure minimum stray capacitance and inductance around their pins.

Some components whose mounting

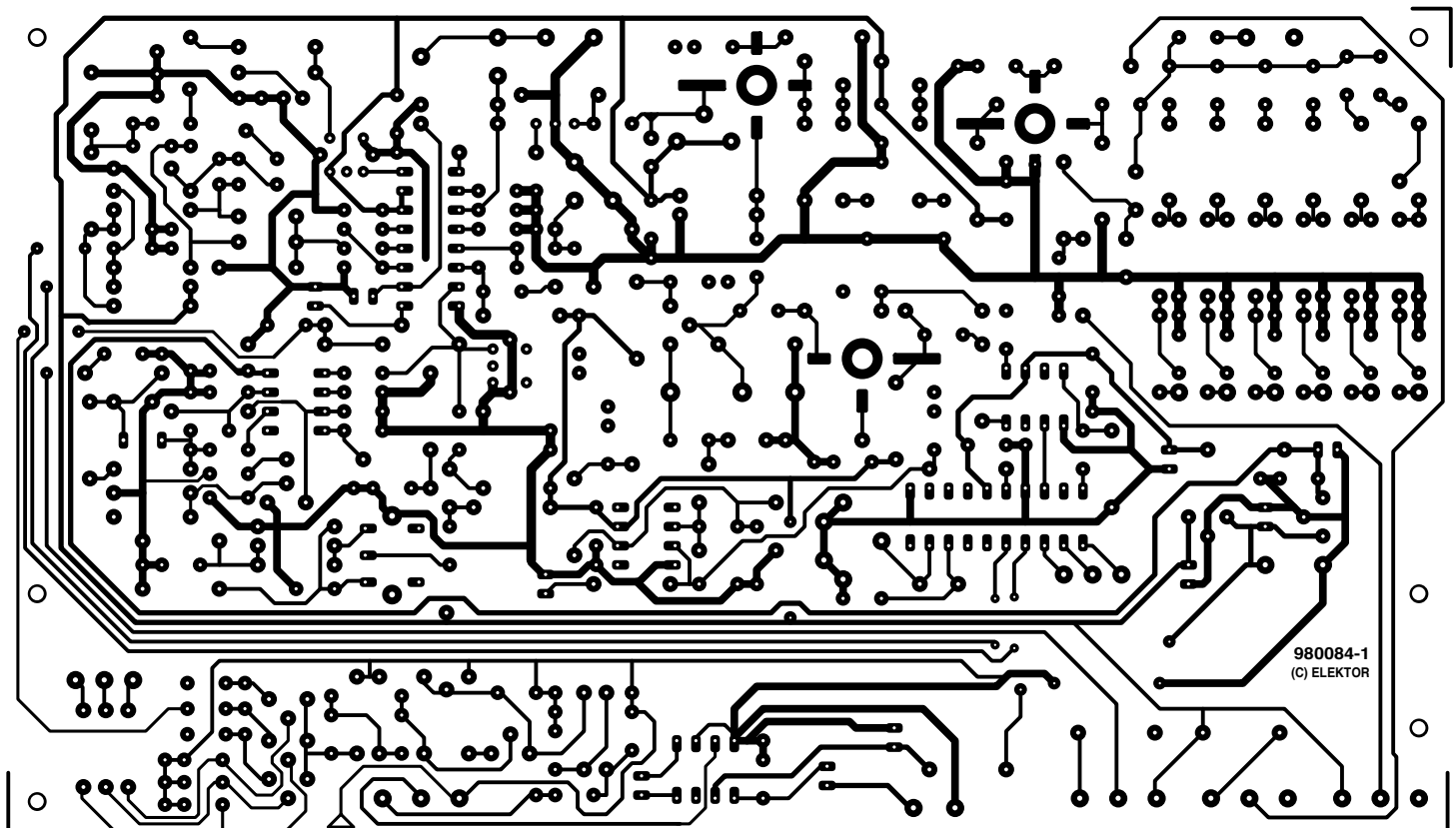
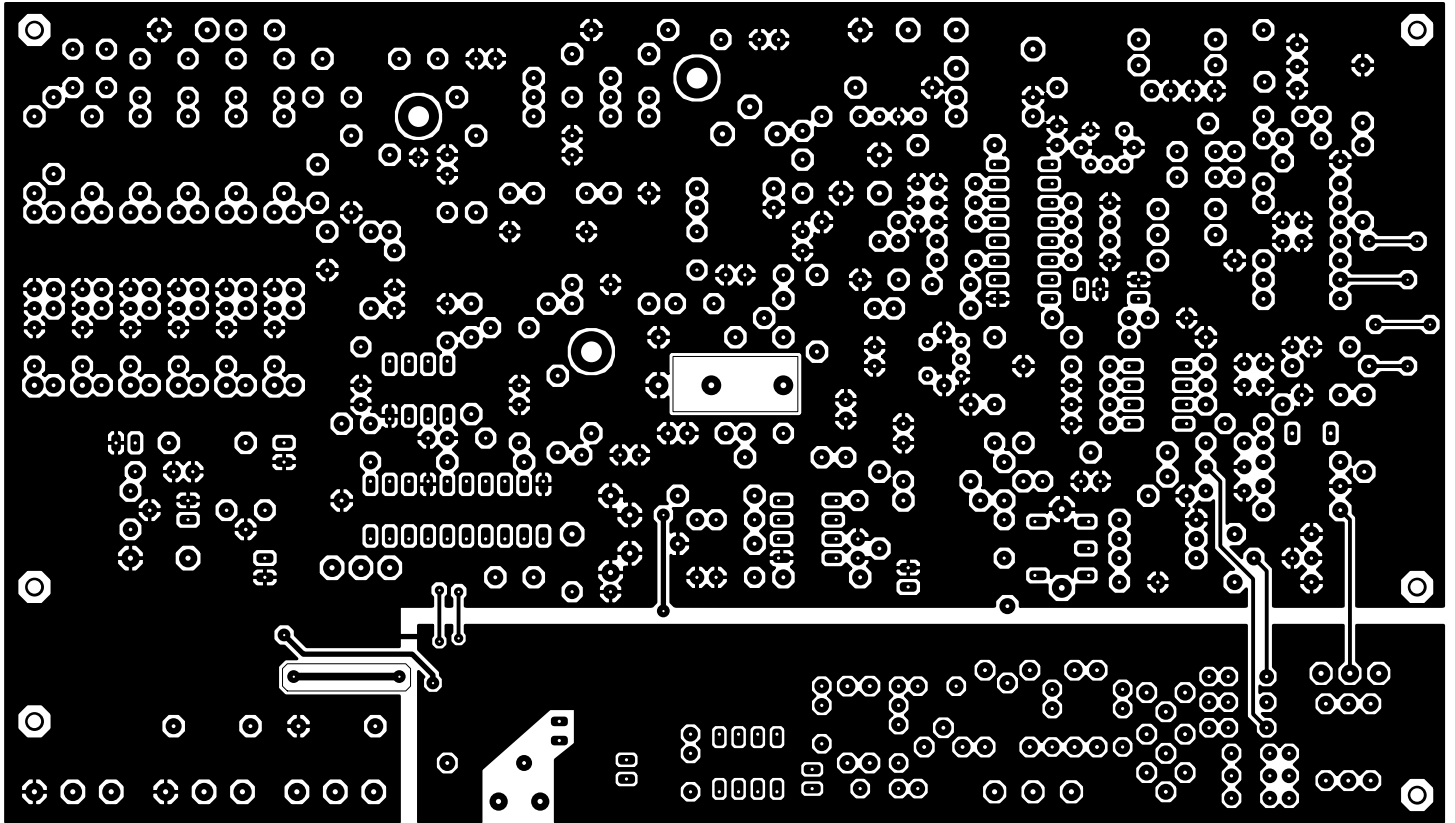


Figure 4. main receiver board layout (solder side and top side). The ready-made board supplied by the Publishers is through-plated.

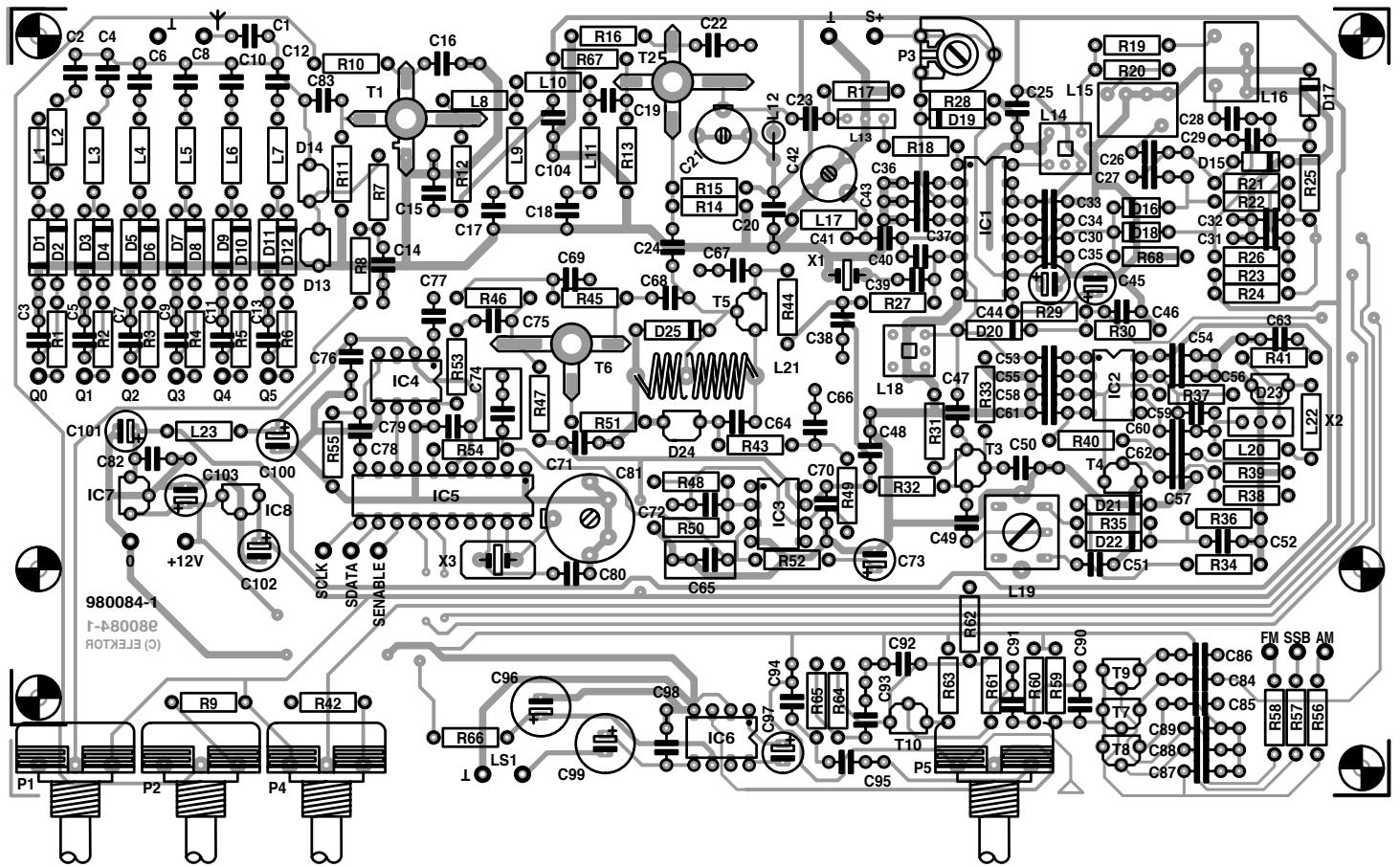
deserves special attention will be discussed below.

Inductor L21

This consists of 7 turns of 0.5-mm dia (SWG26) silver-plated wire. The internal diameter is 6 mm, so the inductor is easily wound on a 5-mm drill bit.

Stretch the turns evenly to make the coil ends reach the holes in the PCB. Then determine the position of the tap, which should be connected at about 3 turns from the cold end. A very short piece of wire installed using tweezers will do the job. A small piece

of foam plastic or similar may be pushed into the coil to reduce microphonic noises due to vibration.



COMPONENTS LIST

Main receiver board

Resistors:

R1-R6 = 330Ω
 R7 = 1MΩ
 R8, R9 = 100kΩ
 R10, R41 = 330kΩ
 R11, R14, R45, R52 = 33kΩ
 R12 = 680Ω
 R13, R40, R46 = 15kΩ
 R15 = 68kΩ
 R16 = 180Ω
 R17, R68 = 3kΩ23
 R18, R63 = 1kΩ
 R19, R20, R32, R33, R55 = 2kΩ2
 R21, R22, R25, R26, R59 = 10kΩ
 R23, R24, R27 = 5kΩ6
 R28 = 8kΩ2
 R29 = 39kΩ
 R30, R49, R64 = 12kΩ
 R31 = 220kΩ
 R34, R35, R54 = 82kΩ
 R36, R43, R48, R50, R56, R57, R58, R60, R65, R67 = 47kΩ
 R37, R38, R39, R42 = 22kΩ
 R44 = 270Ω
 R47 = 560Ω
 R51 = 56Ω
 R53 = 47Ω
 R61 = 560kΩ
 R62 = 3kΩ9
 R66 = 1Ω
 P1, P2, P4 = 50kΩ linear potentiometer, spindle dia. 4mm
 P5 = 50kΩ logarithmic potentiometer, spindle dia. 4mm
 P3 = 10kΩ preset H

Capacitors:

C1 = 6pF8
 C2, C4, C6, C8, C10, C12, C26-
 C30, C50, C60, C69, C72, C92, C95 =
 10nF
 C3, C5, C7, C9, C11, C13-
 C16, C20, C22, C25, C31-
 C38, C43, C48, C54, C55, C57, C58, C63,
 C66, C67, C70, C71, C76, C79, C82, C84-
 C89, C98, C104 = 100nF Sibatic
 (Siemens) or miniature ceramic
 C17, C18, C53 = 10pF
 C19, C83 = 220pF
 C21, C42 = 22pF trimmer
 C23 = 15pF
 C24 = 56pF
 C39, C41, C56, C75, C77, C78, C94 = 1nF
 C40 = 4pF7
 C44 = 4μF7 16V radial
 C45 = 2μF2 16V radial
 C46, C62 = 3nF3
 C47 = 47pF
 C49, C51, C80 = 100pF
 C52 = 2nF2
 C59 = 470pF
 C61, C90 = 22nF
 C64 = 150pF
 C65, C74 = 220nF
 C68 = 5pF6
 C73 = 1μF 16V radial
 C81 = 40pF trimmer
 C91 = 4nF7
 C93 = 3nF9
 C96, C99 = 220μF 16V radial
 C97 = 1μF5 16V radial
 C100-C103 = 10μF 63V radial

Inductors:

L1, L2 = 1mH5
 L3 = 0mH82
 L4 = 120μH
 L5 = 18μH
 L6 = 3μH3
 L7 = 0μH68
 L8, L10 = 4μH7
 L9 = 0μH33
 L11 = 0μH22
 L12, L17 = 0μH56
 L13 = 45M15AU (Murata)
 L14, L18 = LMC4101 (Toko)
 L15 = SFR455J (Murata)
 L16 = A55GGP (Toko) (12kHz)
 L19 = YMCS17105R2 (Toko)
 L20, L22 = 1mH
 L21 = 7 turns of 0.5mm dia (SWG26) sil-
 ver-plated wire, internal dia. 6mm, tap
 at 3 turns from cold end.
 L23 = 100μH

Semiconductors:

D1-D12 = BA479S
 D13, D14 = BB112
 D15-D18 = BA182
 D19-D22 = BAT85
 D23, D24 = BB509
 D25 = BAT82
 T1, T2 = BF961
 T3, T5 = BF245C
 T4, T7, T8, T9 = BS170
 T6 = BFR91
 T10 = BC549C
 IC1 = TCA440 *
 IC2 = NE612AN
 IC3 = MC33171P * (Motorola)
 IC4 = MB501-L * (Fujitsu)

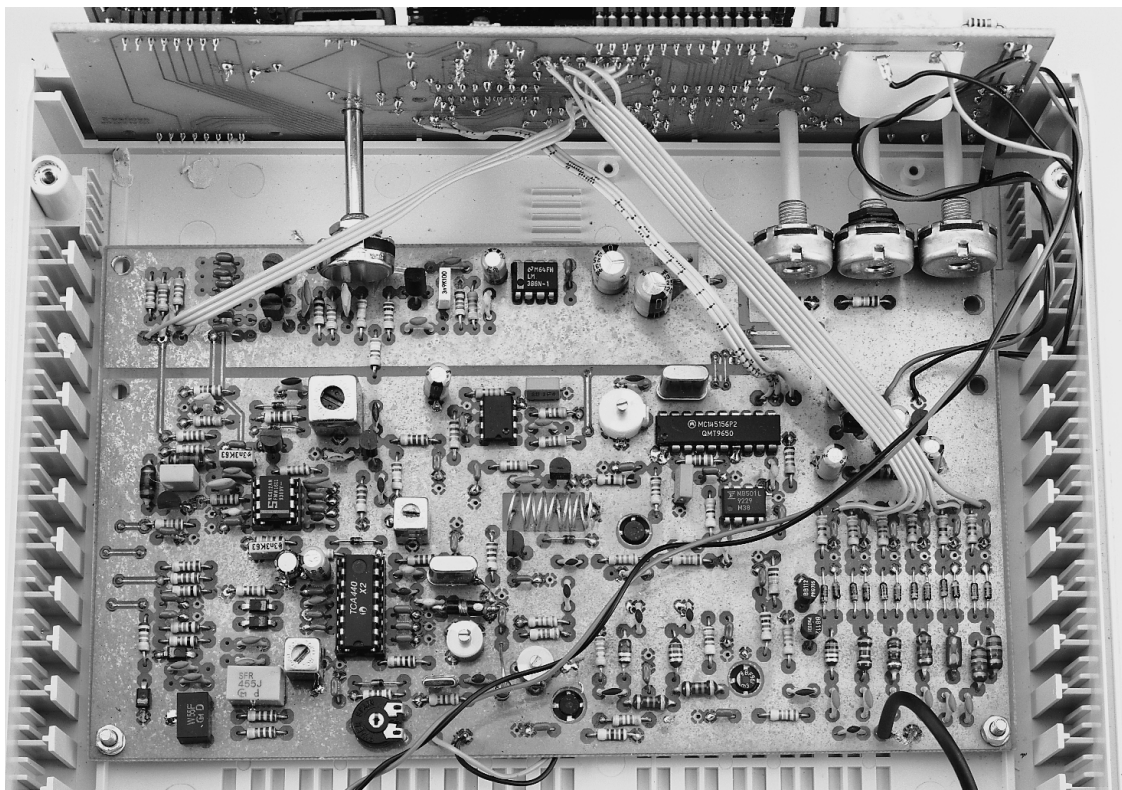


Figure 5. Top view of receiver board, provisionally mounted.

IC5 = MC145156-2 * (Motorola)
 IC6 = LM386N-3
 IC7 = 78L05
 IC8 = 78L09

Miscellaneous:

M1 = moving coil meter, 'S' meter type, fsd 0.1-1.5mA
 Ls1 = 8 ohms, 1 watt
 X1 = 44.545MHz crystal, HC49U case, third overtone, 20pF loading
 X2 = CSB455A resonator
 X3 = 1MHz crystal, HC49U
 Case: Bopla laboratory instrument case, size approx. 223mm (w) x 72mm (h) x 199mm (d), Conrad Electronics order no. 52 33 48-55
 Aluminium front and rear panel, order code 52 33 56-55 (2 off)

* do not use an IC socket

For availability of special RF components used in this project we recommend contacting these suppliers
 Cirkit Distribution Ltd (01992) 441306
 Mainline Electronics (0116) 247 7551
 BEC Component Distribution Ltd (01753) 549502

The prototype was built with components supplied by
 Barend Hendriksen HF Elektronika BV, P.O. Box 66, NL-6970-AB Brummen, The Netherlands. Tel. (+31) 575 561866, fax (+31) 575 565012, email barendh@xs4all.nl

DG MOSFETs and BFR91

The two dual-gate MOSFETs in the circuit, T1, T2, are mounted at the underside of the board. Make sure they are fitted the right way around — the component overlay shows their (different!) orientations. The BF9xx series MOSFETs as supplied these days is no more sensitive to static discharges (ESD) than any common-or-garden CMOS IC, so no special precautions are required in this respect. Unusual as it may be that the type print on a particular MOSFET happens to be illegible from the top side, it is irrelevant! In other words: stick to the component orientation as indicated. In case of doubt refer back the circuit diagram, Figure 2 in part 1.

The BFR91 bipolar transistor is also mounted at the underside of the board. The longest terminal is the collector.

Trimmers

The terminals of the three trimmer capacitors on the board should be soldered as quickly as possible to prevent the heat of the solder bit deforming the plate structure and the internal PTFE material. Note that one trimmer, C21, is at the positive supply voltage. Set all three trimmers to mid-capacitance.

Preselector

No special precautions here, but do make sure you do know the value of each and every miniature choke before you fit it. Also, the PIN diodes must be fitted the right way around!

Quartz crystals

Connect the two quartz crystal cases to the ground plane by means of a

short wires.

Toko inductors

These having two pins at one side and three at the other, they can not be mounted the wrong way around. The lugs at the can sides should also be soldered.

Potentiometers

Note that these are small types with a 4-mm spindle. Do not cut the spindles as yet, their lengths have to be determined accurately later.

RF input

Connect a short length of thin (3-mm dia.) coax cable (like RG174/U) to the RF input.

45M15AU first-IF filter

This metal-encapsulated component has three wires, the centre one being grounded. It can be mounted either way around.

You will notice that the board allows both 5 and 7.5-mm pitch 100-nF ceramic capacitors to be mounted (most are for decoupling). If you can not get hold of the 'Sibatit' capacitors we used in the prototype, they may be replaced with miniature ceramic ones.

Take your time to populate the main receiver board — many mistakes are made as a result of hurrying. **Figure 5** shows one of early prototypes of the receiver board, photographed from above.

CONTROL BOARD

This being a fairly traditional micro-

Figure 6. Copper track layout and component mounting plan of the control board. Unlike the main receiver board, this one is single-sided. Cut off the keyboard section.

COMPONENTS LIST

Control board

Resistors:

R1 = 4k Ω
 R2,R3,R4 = 15k Ω
 R5,R9 = 10k Ω
 R6 = 100 Ω 0.5W
 R7 = 150 Ω
 R8 = 22k Ω
 P1 = 10k Ω preset H

Capacitors:

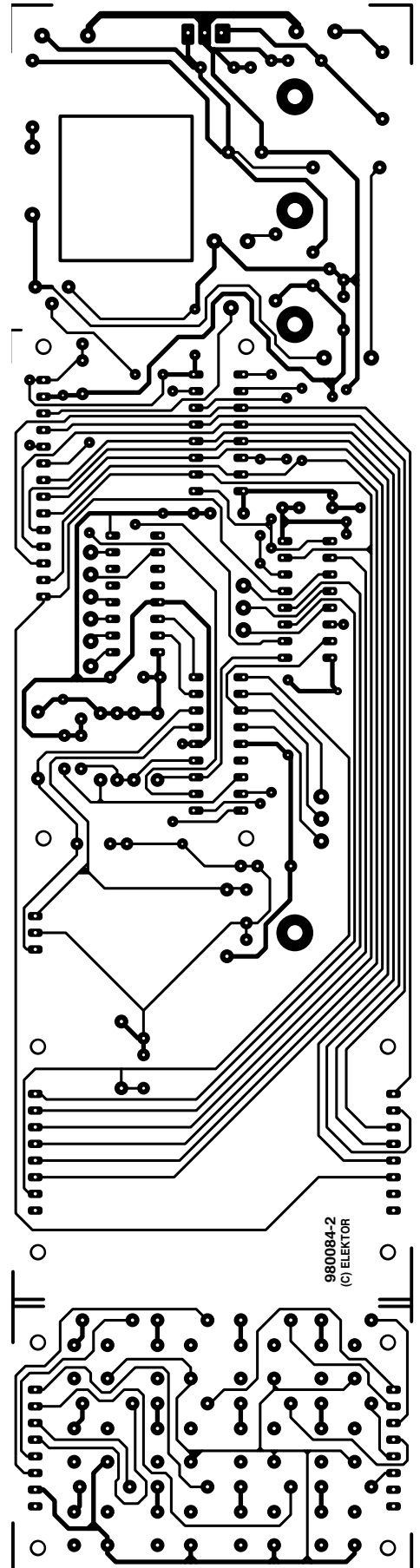
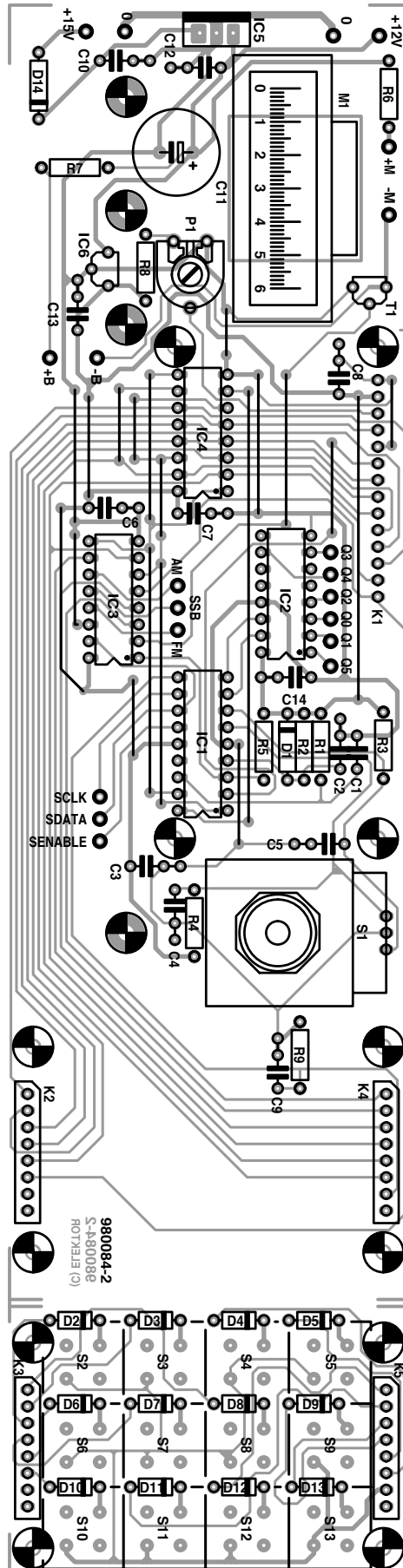
C1 = 27pF
 C2-C8,C10,C12,C13,C14 = 100nF
 C9 = 100pF
 C11 = 470 μ F 25V radial

Semiconductors:

D1-D13 = 1N4148
 D14 = 1N4001
 T1 = BS170
 IC1 = PIC16F84-04/P (order code 986517-1)
 IC2 = 74HCT4017
 IC3,IC4 = 4015
 IC5 = 7812
 IC6 = 78L05

Miscellaneous:

K1 = 14-way SIL socket
 K2, K4 = 8-way SIL socket
 K3, K5 = 8-way SIL pinheader
 S1 = ECW1J-B24-AC0024 (Burr Brown) (supplier: Eurodis)
 S2-S13 = pushbutton, 1 make contact, type D6-R-RD, plus cap type D6Q-RD-CAP (ITC) (supplier: Eurodis)
 LC display, 1 line, 16 characters, type LM161556 (Sharp) (no backlight) or type M16417DY (Seiko) (with backlight) (supplier: Eurodis)
 PCB, order code 980084-2



processor board it is probably easier to build up than the receiver board. The board is single-sided. The design is shown in **Figure 6**, and our finished

prototype, in **Figure 7**.

Like the main receiver board, the control board is available ready-made from the Publishers. If you buy the

complete project from a kit supplier, the PCBs and/or the programmed PIC may or may not be included, so do make sure you know what you get!

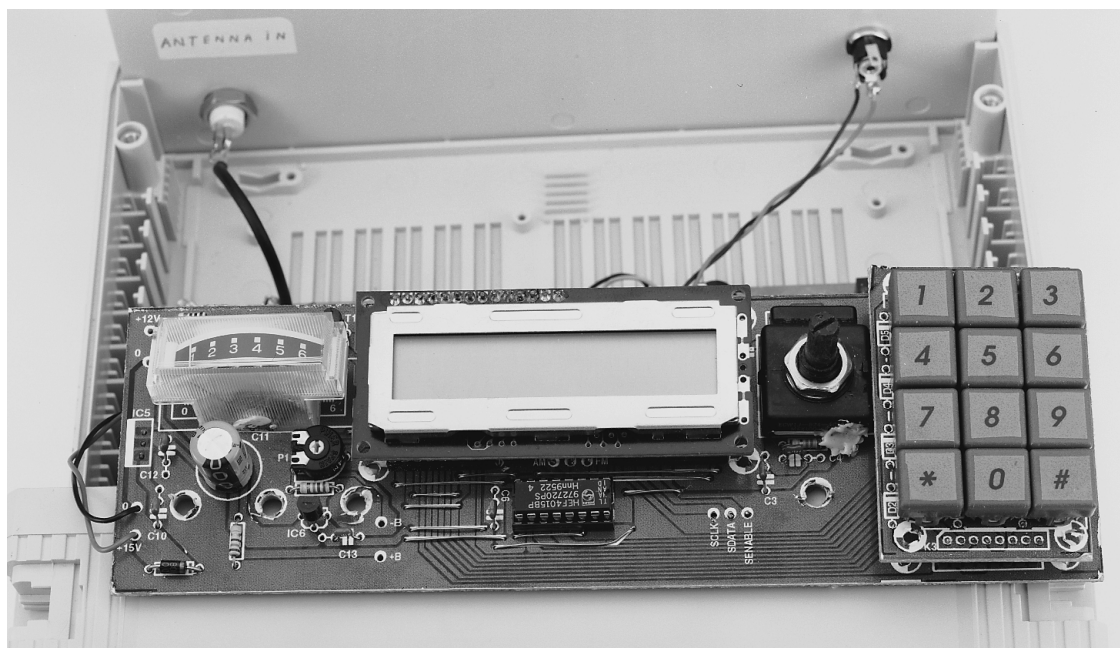


Figure 7. Built up control board.

The keypad section has to be cut from the main control board.

The main point to note about this board is that all components on it must be mounted at the lowest possible height to enable the board to be properly fitted against the inside of the front panel later. If necessary, components IC5 and C11 are mounted at the solder side of the board. For the rest, the control board is conventionally populated, i.e., you use IC sockets and simply follow the parts list and the component overlay. There are, however, a number of wire links which we recommend you fit first.

An important note we should make about building this board is that the switches, the LCD and the S-meter are mounted at such a height that the S meter is flush with the front panel, the LCD is just behind it, and the switches just protrude. This may sound complex, but it is in fact fairly easy to achieve by inserting the control board in the small vertical slots inside the case. These slots are specially made to hold vertically mounted boards, and govern the mounting height of the previously mentioned elements. In our prototype, the LCD was mounted on a SIL pin strip (K1) at about 12 mm above the control board surface. The keypad sub-board was mounted at a height of about 10 mm on two 8-way SIL pinheaders and mating sockets (K2 and K4). By 'nudging' the pinheaders in the sockets, the keytops can be made to protrude about 1 mm from the front panel.

The S meter sits in a square clearance cut in the controller board. Once its final position is known, it may be secured to the board with a few drops of glue.

WIRING

The wire connections between the main receiver board and the control board are made in short lengths of flatcable. A 6-way cable is used for the 'preselector' cable (Q0-Q5), and 3-way cables for the serial bus (SCLCK, SDATA and SENABLE) and the mode selection (FM, AM, SSB). Solder these cables at the receiver board first, and then find the corresponding points on the control board. **Connect the wires at the solder side of the control board.** This is not necessary for the LCD backlight connections, if used.

The controller board has the 12-V voltage regulator on it, so it is connected to the mains adaptor output. The regulated 12-V supply voltage is connected to the receiver board. A mains adaptor with a current rating of 12 V at about 1 A will be fine for the receiver. Note that although an input voltage of 15 V is required, most mains adaptors actually supply at least 15 V when set to 12 V.

The S meter is directly connected to the receiver board (wires to S+ and ground). If the meter has internal lighting, then run two wires from the lamp connections to the terminals + M and -M on the control board. The same for the LCD backlight (if available), which is connected to terminals + B and -B, also on the control board.

A loudspeaker may be mounted inside the case, or a socket may be fitted on the rear panel for connecting an external loudspeaker (often to be preferred).

FRONT PANEL

The layout of the front panel is shown in **Figure 8**. As always you can use this drawing as a template and a master for transferring onto a transparency.

The layout also provides the size of all holes and rectangular clearances to be cut. Unfortunately, a ready-made front panel foil is not available from the Publishers.

The rear panel only holds the RF input socket (a BNC or SO239 type), an external loudspeaker (or headphones) socket and the mains adaptor socket.

ADJUSTMENT

The receiver is designed such that it should be able to receive strong stations with all trimmers and inductor cores set to mid-travel.

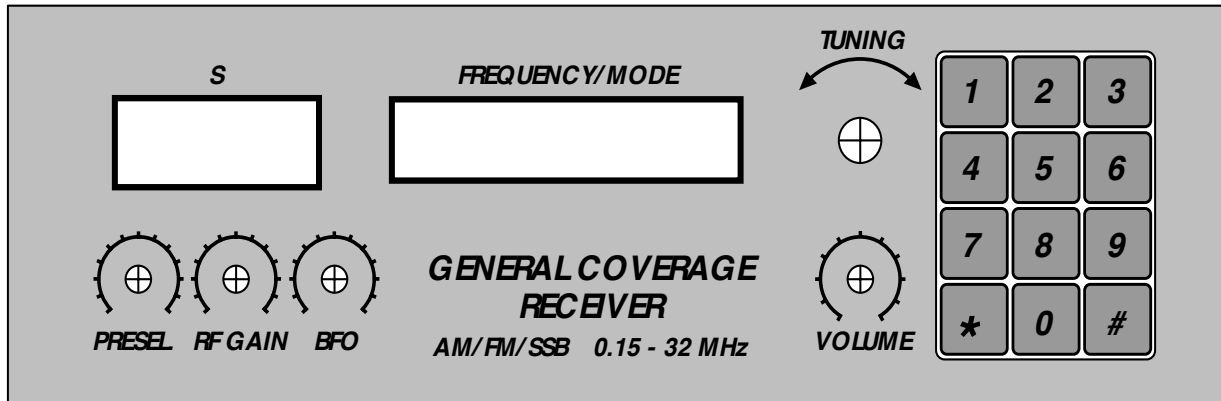
To be able to adjust the receiver, you have to have the two PCBs temporarily connected to each other. Likewise, a power supply, and an antenna and a loudspeaker are provisionally connected up. Turn the volume control way down.

Once you have ascertained the level and the polarity of the 15-V DC supply voltage, connect it to the control board and switch on.

Start by adjusting the LCD contrast using P1. Typically this preset has to be turned almost fully ccw.

The first time you switch on the receiver, memory 0 will contain data that makes no sense and, worse, makes manual tuning impossible. So, first program memory 0 with meaningful information (see below under Operation).

Initially, we recommend tuning to a strong medium-wave (MW) band broadcast station, say BBC Radio 1. Type the frequency into the display, confirm with #, and adjust the 1-MHz reference oscillator (C81) for highest S meter indication. Next, carefully adjust the cores in L14 and L18 for best reception, **using a plastic trimmer tool** (if you don't have this, file down a plastic egg spoon or a matchstick for ovens).



980084 - F

Figure 8. Front panel layout shown at 75% of true size.

If the signal gets very strong, change to a foreign broadcast or a national one which you know you can only receive marginally. Now peak the other two trimmers, C21 and C42, for the highest S meter reading, if necessary reducing the RF gain. The remaining inductor in the receiver, L19, is adjusted for best audio quality of an FM CB station in the 27-MHz band. Failing an off-air FM signal you can also adjust it for minimum audio output when receiving an AM station.

OPERATION

The program developed by the author and burnt into the PIC microcontroller (Publisher's order code 986517-1) provides easy operation of the receiver by driving the LCD and scanning the keyboard. The keyboard allows you to enter the frequency you want, as well as the associated bandwidth (3 or 12 kHz) and mode (AM, FM or SSB). The LCD presents the following readout:

```
mmmb p      ffff kHz
where
mm(m) = AM/FM/SSB (receiver mode)
b=     n/w     narrow or wide band-
        width
p =     1-6    preselector band
ffff = 150-32000 receive frequency in
        kHz
```

The keyboard functions are as follows:

```
ffff#      enter frequency in kHz
01         select AM mode
02         select SSB mode
03         select FM mode
04         select narrow-bandwidth (3 kHz)
05         select wide bandwidth (12 kHz)
00         LCD backlight on/off (if available)
*mm#      store frequency at memory location
           mm
#mm#      load frequency from memory loca-
           tion mm
```

```
where
mm = 00-20; defaults to 00 when the receiver
      is switched on
ffff = 150-32000 (kHz)
```

PRACTICAL RESULTS

Obviously this receiver can not be expected to perform like the latest £1k+ JRC communications receiver. Overall performance is quite good, however, provided you give some thought to the antenna. Even with a simple telescopic antenna, stations at distances of hundreds of miles could be received. The amount of digital interference caused by the microcontroller was found to be so low as to present no problems at all. No wonder, the PIC is asleep most of the time!

Radio amateurs in the 20, 40 and 80-metres bands usually employ SSB for voice communication. With the BFO control on the receiver set to about mid-travel a BFO frequency of about 455 kHz is obtained. Turning it clockwise and anti-clockwise over about 90 degrees then provides the right setting for USB and LSB respectively. Because of the widespread use of synthesizer-

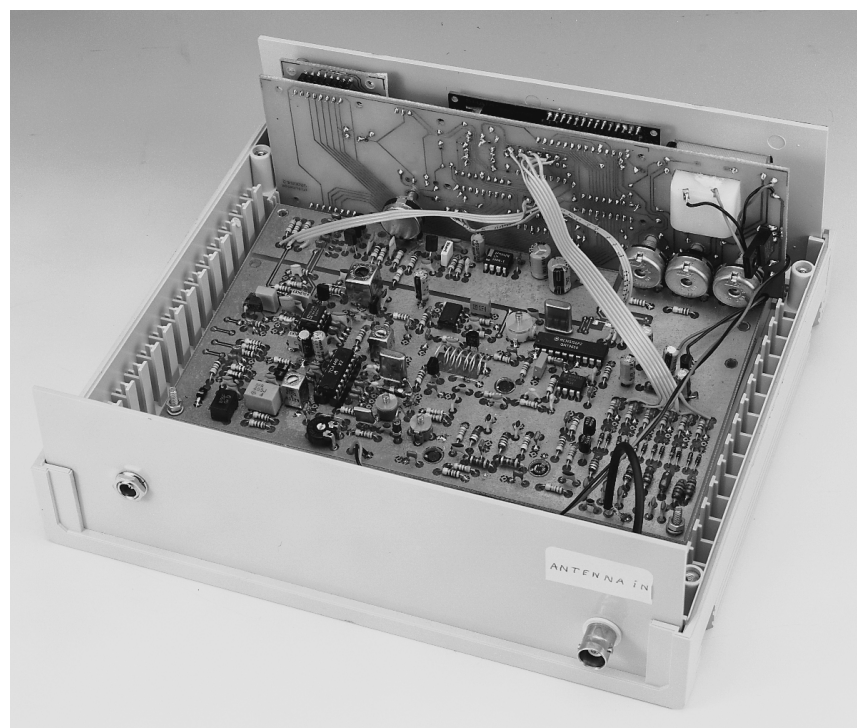
controlled transceivers, many hams use a 1-kHz raster. Even if this is not the case, reception is possible by turning the BFO so that a frequency shift of about 500 Hz is obtained.

Because most radio amateurs use relatively low power levels (as compared to broadcast stations), it pays to use a relatively long wire antenna. The author found that a wire with a length of about 5 m, hung between two houses, gave reasonable results already.

The prototype of the receiver was also successfully tested with the superb Omega-2 and Omega-3 magnetic loop antennas described in the September 1998 issue of *Elektor Electronics*.

Finally, the author welcomes any feedback you may want to provide on building and using the general-coverage receiver described here. His email address is G.Baarst@hotmail.nl

(980084-2)



Eye pattern meter
PC Topics Supplement,
March 1999, p. 13. (992002)
 The moving coil meter shown in Figure 3 should have a sensitivity of 100-200 μ A f.s.d.

Electronics Freeware
May 1999, PC Topics Supplement, p. 4 (990011-1)
 The correct url for Digital Works is

<http://www-scm.tees.ac.uk/users/d.j.barker/digital/digital.htm>

Battery capacity measurement by PC
PC Topics Supplement,
December 1998, p. 14-16. (982093)
 With reference to the circuit diagram, a number of logic

gates in IC4 have been transposed to improve the PCB layout. Functionally, this is of no consequence. However, one track on the board is missing: that between pin 2 and pin 8 of IC1 (ADC0804). If this link is added, C1 is effectively connected and the circuit will work as described.

Sealed lead-acid battery charger
May 1999, p. 26-31. (990037-1)
 In Table 2 (Component Values), the two formulas for R6 should read

$0.45 / I$ [ohms].

D9 is missing from the parts list. As indicated in the circuit diagram, this diode is a type

1N5401. If the charger always supplies currents smaller than about 1 A, diode D9 may also be an 1N4001 or similar.

General Coverage Receiver
January & February 1999 (980084).

In the preselector section, the upper varicap diode, D14, has no dc path. A suggested method of improving the behaviour of the varicap (without modifying the PCB) is to replace capacitor C83 (220pF) with a wire link.

Flash Designs – address information
April 1999, New Products, p. 73.

In the New Products section, the address and telephone number of Flash Designs

should be changed to read

Flash Designs, Ltd.,
 North Parade House,
 North Parade,
 Bath BA2 4AL
 Tel. (01225) 448630.

We extend our apologies to Flash Designs and our readers for any inconvenience caused by the incorrect address information.

Electronic Spirit-Level
July/August 1998, p. 36 (984038).

In the circuit diagram, all LEDs (D2 through D10) should be reversed. The PCB layout is all right.

precision current gauges

with low-loss sense element and PWM output

The LM3812/LM3813 current gauges from National Semiconductor are suitable for application as battery charge/discharge gauge, motion control diagnostics, power supply load monitoring and management, and resettable smart fuse.

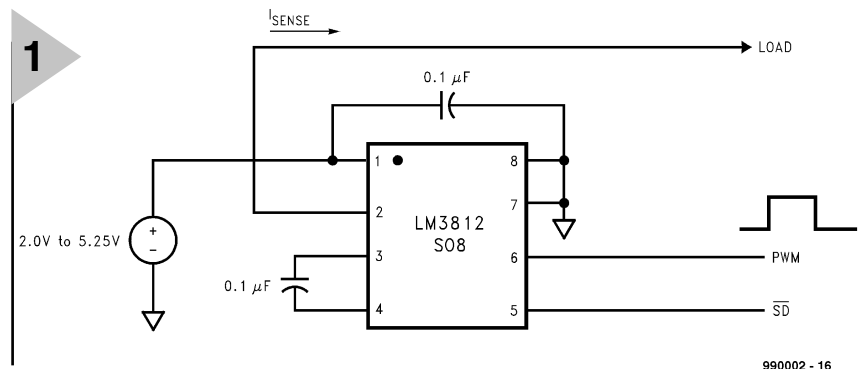


Figure 1. Typical application circuit of an LM3812 (high sense). That of an LM3813 (low sense) is equally straightforward.

INTRODUCTION

The LM3812/LM3813 current gauges provide easy-to-use precision current measurement with virtually zero insertion loss (typically 0.004Ω ; tempera-

ture coefficient $2600 \text{ ppm } ^\circ\text{C}^{-1}$).

A Delta Sigma analogue-to-digital converter is incorporated to precisely measure the current and to provide a current averaging function. Current is

Main parameters

- ⇒ Ultra low insertion loss (typically 0.004Ω)
- ⇒ 2–2.5 V supply range
- ⇒ $\pm 2\%$ accuracy at room temperature (includes accuracy of the internal sense element) (LM3812-1.0, LM3813-1.0)
- ⇒ Low quiescent current in shutdown mode (typically $2.5 \mu\text{A}$)
- ⇒ 50 ms sampling interval
- ⇒ No external sense element required
- ⇒ PWM output indicates the current magnitude and direction
- ⇒ PWM output can be interfaced with microprocessors
- ⇒ Precision delta-sigma current-sense technique
- ⇒ Low temperature sensitivity
- ⇒ Internal filtering rejects false trips
- ⇒ Internal power-on reset (POR)

averaged over 50 ms time periods to provide immunity to current spikes.

The devices have a pulse-width modulated (PWM) output which indicates the current magnitude and direction. The accuracy, including the accuracy of the internal sense element, is better than $\pm 2\%$ at room temperature.

The shutdown pin may be used to inhibit false triggering during start-up or to enter a low quiescent current mode.

The LM3812 is used for high-side sensing, and the LM3813 for low-side sensing. The diagram of the LM3812 in **Figure 1** shows that the only external components needed are two capacitors. The application diagram of the LM3813 is equally straightforward.

Both ICs operate from a supply voltage of 2–5.25 V. They are factory-set in two different current options. The sense range is -1 A to $+1\text{ A}$ or -7 A to $+7\text{ A}$. The sampling interval is 50 ms. If faster sampling is desired, reference should be made to the LM3814 and LM3815.

The devices are available in eight different versions in an SO8 package. In the type coding LM381aXc-d, M indicates that the part is available in surface mount package; a indicates high-side (= 2) or low-side (= 3); X indicates that the part is available in multiples of 2500 on tape or reel; c indicates the sampling time ($c=P=50\text{ ms}$; $c=F=6\text{ ms}$), and d indicates the sense range ($d=1.0$ for $\pm 1\text{ A}$; $d=7.0$ for $\pm 7\text{ A}$).

OPERATION

The current is sampled by a delta-sigma modulator as shown in **Figure 2**. The pulse density output of the modulator is digitally filtered. The digital output is then compared to the output of a digital ramp generator, which produces a PWM output.

The duty cycle of the PWM is proportional to the level of current flowing. A duty cycle of 50% indicates zero current. If the current is flowing into a positive direction, the duty cycle $> 50\%$; if it is flowing into a negative direction, the duty cycle $< 50\%$.

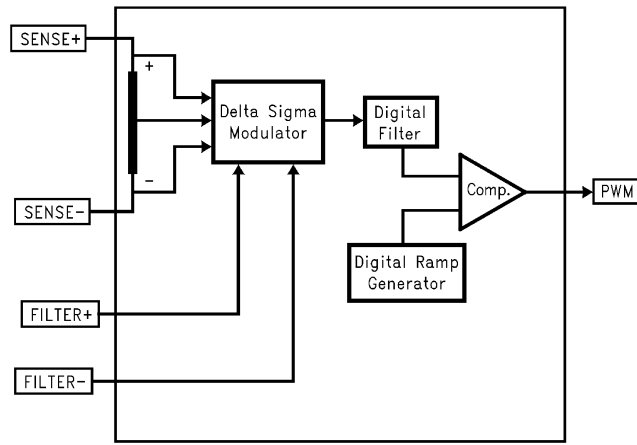
A duty cycle of 95.5% (4.5%) indicates the current is at I_{\max} ($-I_{\max}$). The IC can sense current from $-I_{\max}$ to $+I_{\max}$. Options for I_{\max} are 1 A or 10 A. A typical timing diagram for a mostly positive current is given in **Figure 3**. The sense current is given by

$$I_{\text{sense}} = 2.2(D - 0.5)(I_{\max})$$

where D is the duty cycle of the PWM signal and I_{\max} is the full-scale current (1 A or 10 A). Similarly, the duty cycle is given by

$$D = (I_{\text{sense}} / 2.2I_{\max}) + 0.5.$$

2



990002 - 11

Figure 2. Functional block diagram of the LM3812/LM3813.

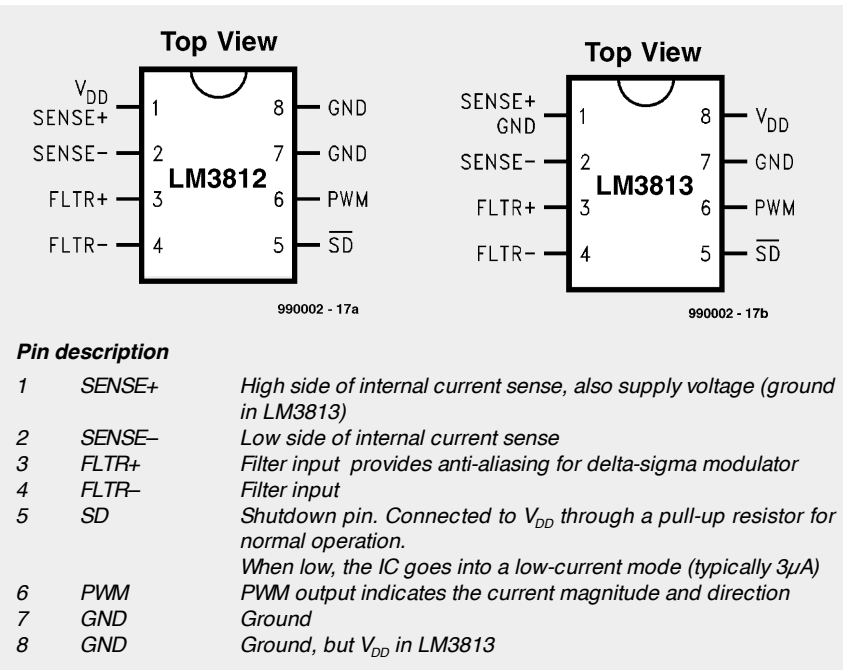
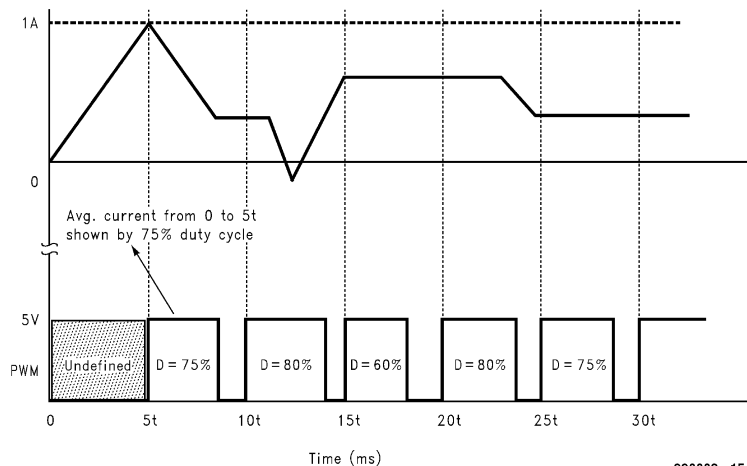


Figure 3. Typical timing diagram for mostly positive current. The duty cycle of the PWM signal during any sampling interval indicates the current magnitude (average) and direction during the previous sampling interval.

3



990002 - 15

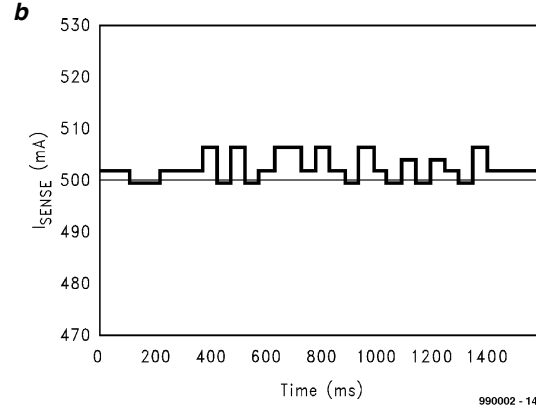
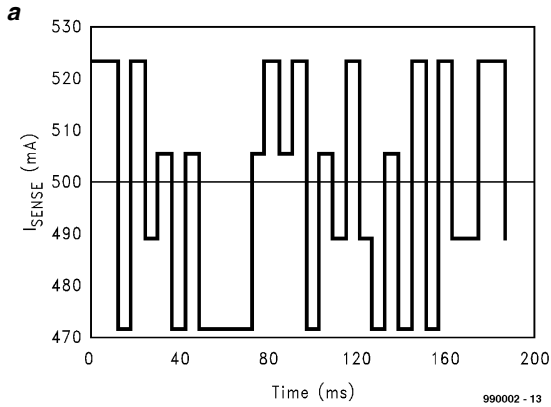


Figure 4. Typical response of an LM3812-1.0/LM3813-1.0 P version (a) and F version (b).

Note that although the LM3812-7.0 and LM3813-7.0 will read 10 A full scale, they are rated for 10 A operation for a duration of no more than 200 ms, and 7 A operation continuously.

OFFSET

The PWM output is quantized to 1024 levels, which means that the duty cycle can change in increments of 1/1024 only.

There is a one-half quantization cycle delay in the output of the PWM circuitry. That is to say that instead of a duty cycle of $n/1024$, the duty cycle actually is $(n + 0.5)/1024$.

The quantization error can be corrected if a more precise result is desired. To correct for this error, simply subtract 1/2048 from the measured duty cycle.

The extra half cycle delay will show up as a d.c. offset of 0.5 bit if it is not corrected for. This is about 1.1 mA for 1 A ICs, and 11 mA for 7 A devices.

ACCURACY VS NOISE

The graph shown in **Figure 4** illustrates the typical response of ± 1 A current gauges. In this graph, the horizontal (x) axis indicates time, and the vertical (y) axis, the measured current (the PWM duty cycle has been converted to current). The graph shown was generated for an actual current of 500 mA.

The difference between successive readings manifests itself as jitter in the PWM output or noise in the current measurement (when the duty cycle of the PWM output is converted into current).

The accuracy of the measurement depends on the noise in the current waveform. The accuracy can be improved by averaging several outputs. Although there is variation in successive readings, a very accurate measurement can be obtained by averaging the readings. For example, on averaging the readings shown in this

example, the average current measurement is 502.3 mA. This value is very close to the actual value of 500 mA. Moreover, the accuracy depends on the number of readings that are averaged.

[990002]

Source: Data sheet 'LM3812/LM3813 Precision Current Gauge IC with Ultra Low Loss Sense Element and PWM' (National Semiconductor) (www.natsemi.com/)

Electrical characteristics ($V_{DD} = 5.0$ V, Supply bypass capacitor is 1 μ F and filter capacitor is 0.1 μ F)						
Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
I_{ACC}	Average current accuracy	LM381aPM-1.0	0.882/0.864	0.9	0.918/0.936	A
		LM381aFM-1.0	0.868/0.850	0.9	0.932/0.950	A
		LM381aPM-7.0	2.400/2.350	2.5	2.600/2.650	A
		LM381aFM-7.0	2.350/2.288	2.5	2.650/2.712	A
e_n	Effective output noise	LM381aPM-1.0		2		mA
		LM381aFM-1.0		12		mA
		LM381aPM-7.0		20		mA
		LM381aFM-7.0		120		mA
I_{Q1}	Quiescent current	Normal Mode		100	160	μ A
		Shutdown Mode		2.5	10	μ A
D_{RES}	PWM resolution	Precision Mode		0.1		%
		Fast Mode		0.8		%
t_s	Sampling time	Precision Mode	40	52	80	ms
		Fast Mode	4	6	10	ms
f_p	Frequency of PWM signal	Precision Mode	12.5	20	25	Hz
		Fast Mode	100	160	250	Hz
V_{QH}	Logic high level for PWM	Load current = 1 mA	$V_{DD} - 0.2$	$V_{DD} - 0.05$		V
V_{QL}	Logic low level for PWM	$2V \leq V_{DD} \leq 5.25V$		0.04	0.2	V
P_I	Insertion loss	$I_{SENSE} = 1$ A		0.004		Ω

Notes: Specifications in standard type face are for a junction temperature $T_j = 25 \pm 0.5^\circ\text{C}$ and those in bold type face apply over the full junction temperature range of -40°C to $+125^\circ\text{C}$.

datalogger for DMM

for Metex & Voltcraft DMMs

As you may know, the combination of a PC and a Metex or Voltcraft DMM sporting a serial interface may be used as a recording oscilloscope provided you leave the PC switched on and connected all the time. Because that is not always possible or desirable, we present a datalogger system that can make do without the PC.



Features

- ⇨ Simple to operate
- ⇨ High accuracy
- ⇨ Supports all DMM measurement ranges
- ⇨ Compatible with Voltcraft and Metex DMMs
- ⇨ Data readout on internal LCD
- ⇨ Simple construction, low cost

Technical data

Supply voltage	
Mains adaptor	9-12 V
Battery	9 VPP3
Average current drain	6.5 mA
Serial protocol (PC link)	1200/8/n/2 9600/8/n/2

Design by R. Lock

Some of the latest digital multimeters (DMMs) have an extremely useful function: a serial interface. By linking this to a PC, you get a recording oscilloscope for slow signals. On the down side, the PC then has to be present at the measurement location, and left running all the time. Besides, the DMM occupies the serial port during the entire measurement (which may take several days to complete). These disadvantages considerably complicate the use of the DMM as described, and limit its functionality.

The datalogger described here avoids these problems. It automatically captures the discrete measurement values supplied by the DMM, puts them in permanent

storage, and, if desired, displays them on an LCD. Relatively large data volumes may still be transferred to a PC, for processing later using 'big gun' spreadsheet/statistics software like Excel.

Another marked advantage of the system as described is that the use of a multimeter ensures that all measurement ranges of the instrument in question are available with the relevant accuracy. Multimeters with special measurement options like temperature, power and so on further add to the versatility and appeal of the datalogger.

HARDWARE

As you can see from the circuit diagram in **Figure 1**, the datalogger is basically a 'stand-alone' microcontroller system based on the 80C31. The control program is stored in a type 27C256

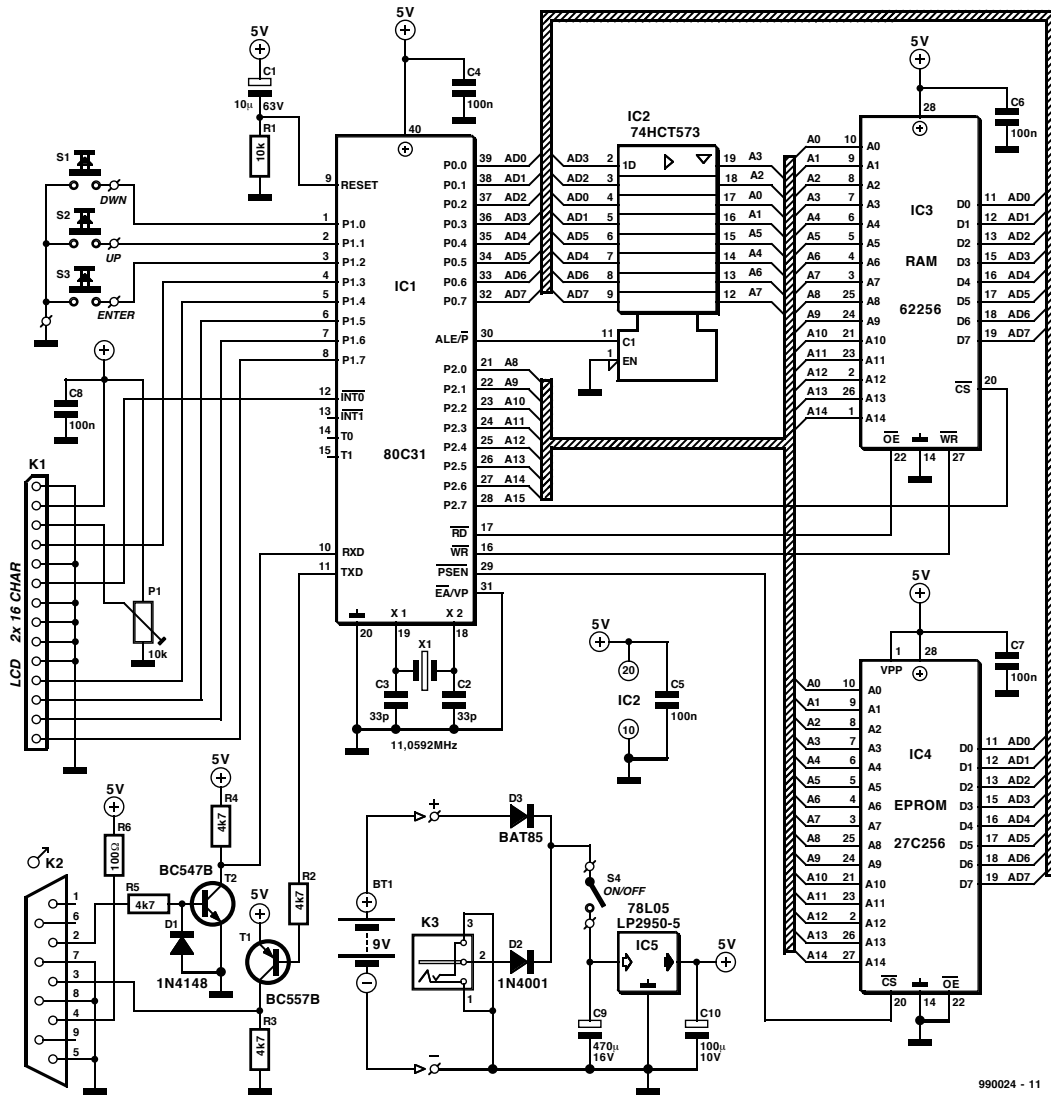


Figure 1. The datalogger consists of an 80C31 microcontroller system with RS232 and LCD interfaces.

EPROM with a size of 32 kBytes. A 62256 RAM with the same size is employed for storage of the measurement data. The microcontroller is clocked by an 11.0592 MHz quartz crystal. This frequency may seem odd, but it does allow standard baudrates to be derived easily. Network R1-C1 provides the power-up reset signal. The alphanumeric display is controlled in 4-bit mode via serial port 1.

The RS232 interface in the datalogger is a minimum-hardware design consisting of a transistor buffer/inverter on the TxD line and a level converter/inverter, also transistorised, on the RxD line.

The supply circuit allows the datalogger to be powered by a conventional mains adaptor. By means of diodes D2 and D3, an external battery is 'OR-ed' into the circuit, in parallel with the mains adaptor. When the output voltage from the mains adaptor fails, the battery takes over as the power supply. In this way, a no-break power supply is created, and no further mea-

asures are required to safeguard the RAM data against corruption by power disruptions. The low-drop voltage regulator type LP2950-5 can be relied upon to completely drain the battery to the last microampere-hour. In case the datalogger is to be powered by the mains adaptor only, a more conventional fixed-voltage regulator like the 78L05 may be used. In the inactive state, the circuit draws a quiescent current of about 6.5 mA. With battery life in mind, it is fortunate that the average current drain of the datalogger is not much higher. When a measurement takes place, the current drain briefly rises to approximately 20 mA.

OPERATION

The first thing to do after switching on the circuit is adjust preset P1 until the text on the LCD is clearly legible. The first text to appear will be **DNDLE12**. The datalogger is operated with the arrow keys and the Enter key. The latter selects between the various menus, and confirms the selection of the menu

options you can point to with the arrow keys.

To perform a measurement, connect-up the supply voltage, switch off the DMM, connect the datalogger to the DMM, and then switch the DMM on again. After starting the datalogger, you will see the menu options

```

MAIN MENU
>Data retrieval
>Measuring

```

Having selected the option **Measuring** and having pressed the Enter key the following information appears on the display:

```

Sampling P 00:02
Enter minutes

```

You are prompted to enter the measurement interval (P); the highest value allowed is 99 minutes and 99 seconds. (99:99). Use the arrow keys to select the minutes value, then press Enter. This menu appears:

```

Sampling P 00:02
Enter seconds

```

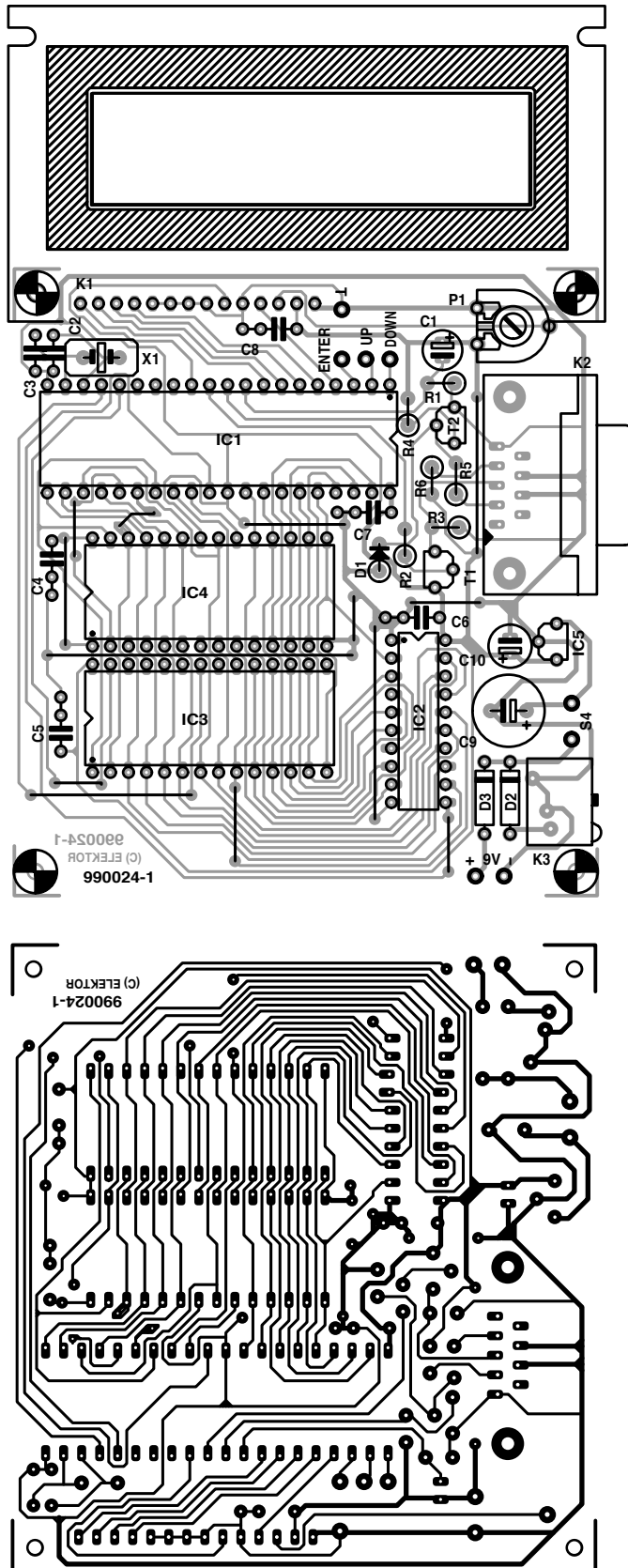


Figure 2. The printed circuit board is easily mounted in a case with a display window.

Enter the desired no. of seconds of the measurement (sampling) interval, and press Enter again. The next prompt appears:

```
START          y
MEASUREMENT? n
```

Press 'y' to continue. The first line of

COMPONENTS LIST

Resistors:

R1 = 10k Ω
 R2-R5 = 4k Ω 7
 R6 = 100 Ω
 P1 = 10k Ω preset

Capacitors:

C1 = 10 μ F 63V radial
 C2, C3 = 33pF
 C4-C8 = 100nF
 C9 = 470 μ F 16V radial
 C10 = 100 μ F 10V radial

Semiconductors:

D1 = 1N4148
 D2 = 1N4001
 D3 = BAT85
 T1 = BC557B
 T2 = BC547B
 IC1 = 80C31, 80C51 or 87C51 (40-pin DIL case)
 IC2 = 74HCT573
 IC3 = 62256 (e.g. UMC62256E-70LL)
 IC4 = 27256 (order code 986522-1)
 IC5 = 78L05 or LP2950-5 (see text)

Miscellaneous:

K1 = 14-way IDC connector for flat-cable
 K2 = 9-way sub-D pinheader, angled pins, PCB mount
 K3 = mains adaptor socket
 S1 = pushbutton, 1 make contact, CTL3 (Multimec)
 S4 = Slide switch, 1 x on
 X1 = 11.0592MHz quartz crystal
 Plastic case, approx. size 145 x 90 x 28 mm (Pactec type HP)
 LC display, 2 lines of 16 characters, e.g., LTN 211 R-10 (Philips) or LM16A211 (Sharp)
 PCB, order code 990024-1

the display will then show the previously captured set of data, with the current measurement time on the second line, for example,

```
DC      00.00 V
        00:00:08
```

The clock continues to tick and is updated every second. The measurement value in the upper line is updated depending on the previously set sampling interval. The longest measurement period is 100 hours less one second.

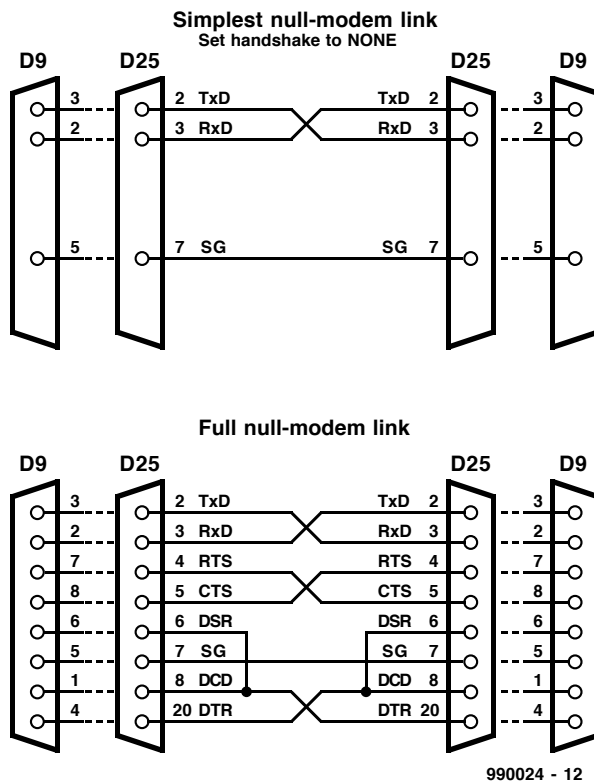
If no multimeter is connected, the microprocessor will 'hang'. To start a measurement anyway, you press the Enter key.

A measurement may be ended by keeping the Enter key pressed for more than 1 s. Cancelling is confirmed when the display indicates

STOP

The last data set and the associated time mark are then 'frozen'. By pressing the Enter key again you are returned to the main menu.

Transferring measurement data



from the datalogger to the PC is even simpler. In the main menu you select **Data retrieval**. By pressing the up/down arrow keys you call up the following options:

- >> Display
- >> PC numerical
- >> PC alphanumeric

Selecting the first option causes the measurement values to be shown on the datalogger LCD, with the arrow keys available to scroll through the data sets.

The other two options cause the data sets to be sent to the PC, either in numerical or alphanumeric format. Before that can be done however, you have to select the data speed in this menu

- >>> BAUDRATE
- >>> 1200 baud
- >>> 9600 baud

Once that has been done, you may launch the data upload operation by confirming the option

Out put - -> PC

CONSTRUCTION

The design of the printed circuit board shown in **Figure 2** is pretty spacious, so constructing the datalogger and fitting it in a 'windowed' plastic case should not present undue difficulties.

All ICs may be fitted in sockets. Do not forget the 13 wire links on the single-sided board, and make sure all parts are mounted the right way around. With everything in place, give the board a thorough visual check, looking for cold joints and solder splashes.

CONNECTING - UP

The DMM and the PC are hooked up to one and the same the 9-way sub-D connector on the datalogger board, but not simultaneously, of course. Like the serial port connector on a PC, this connector is a plug, so that the DMM is easy to connect. Connecting the PC however requires a special cable: it should have sockets at both ends, as well as crossed TxD, RxD and hand-

shaking lines. The construction of this so-called *null-modem* (or *zero-modem*) cable is illustrated in **Figure 3**.

DMMs with an RS232 interface are designed for direct connection to a PC. The serial interface on the PC may have a 9-pin or a 25-pin connector. In the first case, pin 3 is the output, and pin 2, the input. The pin numbers are reversed on the 25-way connector! This is taken into account in the serial cable for the multimeter, no matter if a 9-pin or 25-pin connector is used.

Basically there is only one-way data traffic between the PC and the datalogger. The DTR signal on pin 4 (DB25: pin 20) of the PC connector indicates that the PC is ready to receive new data. The same applies to the RTS signal on pin 7 (DB25: pin 4), which is activated by the PC to indicate that it wants to send data. Because many digital multimeters require these two signals to be able to upload logged data to a PC, pin 4 of K2 on the datalogger is started to +5 V, while pin 7 is connected to ground.

At the PC side, you may use just about any communications program, including the popular HyperTerminal utility which comes with Windows 95. Select the COM port and the following communication parameters:

1200 bits/s or 9600 bits/s, 8 databits, no parity, 2 stop bits and *hardware* protocol. A zero-modem cable with no more than the two data lines and ground will also work. The datalogger does not employ handshaking, so you select *none* for the protocol. Incidentally, the data exchange between the datalogger and the DMM employs a different communications protocol: 7 databits, no parity, and 2 stop bits.

The author used the datalogger in combination with a Metex M-3610-D and a Volcraft VC 506. The prototype circuit built in the *Elektor Electronics* design lab was successfully tested with a Metex M-3650-CR. Other DMMs of the same two brands can be expected to support the same protocol.

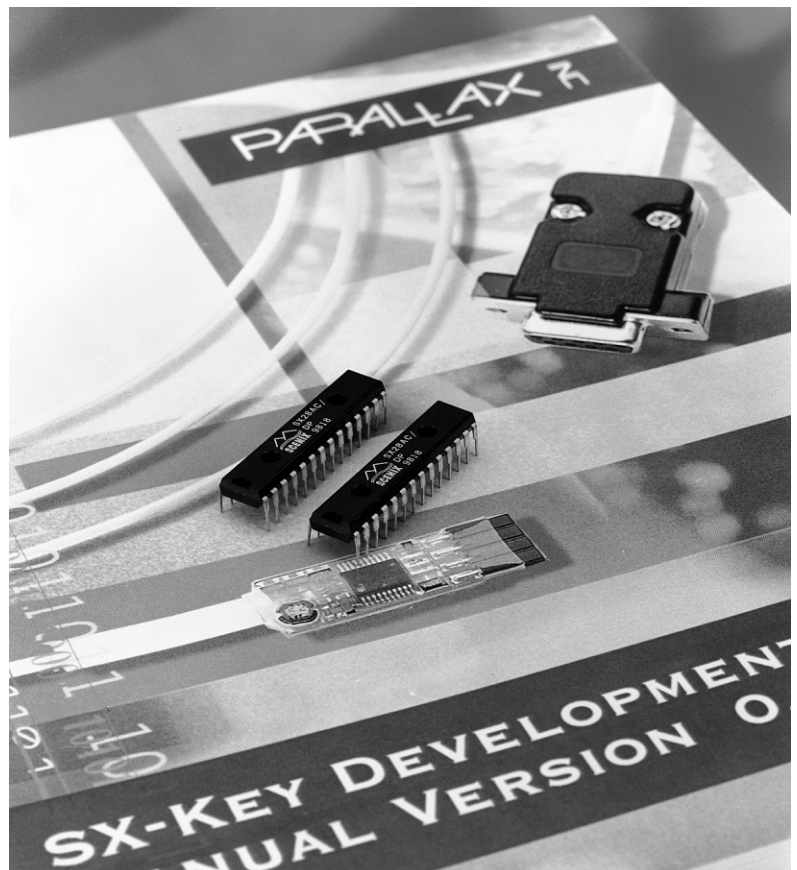
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Figure 3. All about zero-modem cables.

SX-microcontroller evaluation system (1)

part 1: introducing the Scenix SX micro

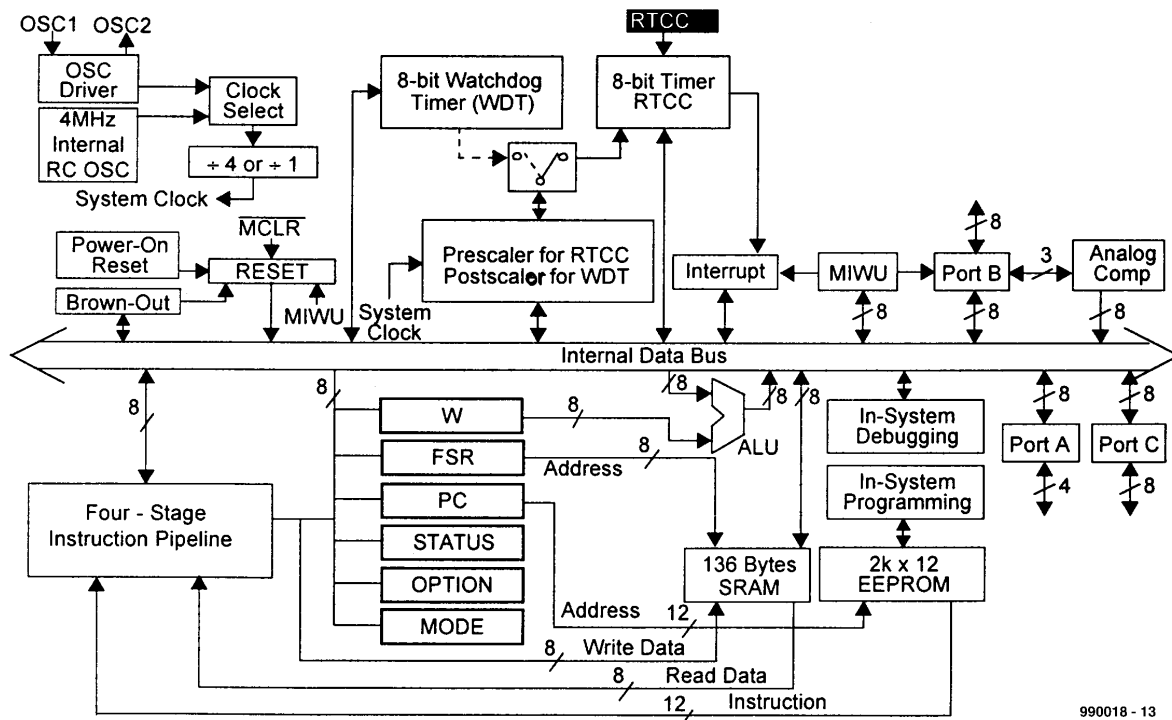
Design by Dr. M. Ohsmann



With a PC-like RISC architecture and offering clock frequencies up to 100 MHz, the new SX

processors from Scenix are currently the fastest 8-bit microcontrollers around. Unfortunately, the cost of the development kit supplied by Parallax is on the high side to say the least, and that is why we present an alternative for home construction. The system consists of a programming adaptor, an assembler, two demonstration boards and a variety of example programs.

1



990018 - 13

Figure 1. SX microcontroller architecture.

Scenix recently released the first devices from of a new series of 8-bit microcontrollers. Although these early products are still flawed by the odd bug, they allow designers to get cracking. As far as raw speed is concerned, the new Scenix products are currently the fastest 8-bit microcontrollers you can buy. At a clock frequency of 50 MHz, the standard version rockets along at a speed of 50 MIPs (million instructions per second). Meanwhile, the first samples of 75-MHz versions have arrived, and a 100-MHz version is in the pipeline.

The price, too, is right at less than 4 US dollars per unit for volume quantities. On the down side, development kits, assemblers and programming adaptors for the SX series are priced well over 250 US dollars. As you can see from **Table 1**, The development system we have in mind is far less costly, and comprises just about anything you need for a head start with the extremely fast 'SX' microcontroller.

Datasheets of the SX processors may be downloaded from the Scenix web site at www.scenix.com. There you will also find the errata sheets for the earliest chips. This information was obviously taken into account while the present development system was designed.

THE SX PROCESSOR FAMILY

As we write this, the SX series consists of just two members, which differ in respect of the number of ports. The smaller version does not have port C bonded out to pins. It is available 18-pin cases (Type SX18AC/SO = small

outline; Type SX18AC/DP = DIL case), or in a 20-pin SSOP case (Type SX20AC/SS).

The larger brother has port C available on pins. It comes in three different 28-pin cases (SX28AC/SO = small outline; SX28AC/DP = DIL case, SX28AC/SS = small scale). The 75-MHz and 100-MHz versions have the respective type designations SX28AC75/DP and SX28AC100/DP.

The internal architecture of these processors is shown in **Figure 1**. The processor has several clock oscillators, which will be discussed in detail further on in the series.

An internal low-power oscillator may be used, or an external quartz crystal or RC network may be connected. Next, we have a ÷4 prescaler. If this is bypassed, the so-called Turbo Mode is selected, which guarantees the fastest program execution. The instruc-

Table 1 SX Evaluation System Hardware and software overview

PICKALOCK	Programming adaptor for in-system serial programming (ISP) of Scenix SX controllers
PICKLOC1.DOC	Documentation of the PC/PICKALOCK interface
SXDemoboard 1	Demonstration board for the SX28AC controller
SXDemoboard 2	Demonstration board for the SX18AC controller
SXASM.PAS	Assembler for SX controllers; source code (Pascal 5.0)
SXASM.EXE	Assembler for SX controllers (executable program)
SXASM.DOC	Documentation with assembler
SXPRO.PAS	PC shell for SX-PICKALOCK; source code
SXPRO.EXE	PC shell for SX-PICKALOCK
SXPRO.DOC	Operation manual
TIPS.DOC	Tips for faultfinding
LED1.SRC	Example program: LED flasher using 16-MHz crystal
IRC1.SRC	LED flasher using internal RC oscillator
RC1.SRC	LED flasher using external RC oscillator
SERIO1.SRC	Serial hexadecimal I/O for test purposes
SERPWM1.SRC	PWM/ADC and LED control
SINGEN1.SRC	Sine wave generator, 1 kHz, PWM
SINGEN2.SRC	Sine wave generator, 455 kHz, using R-2R DAC
MIW1.SRC	Multi-wakeup test

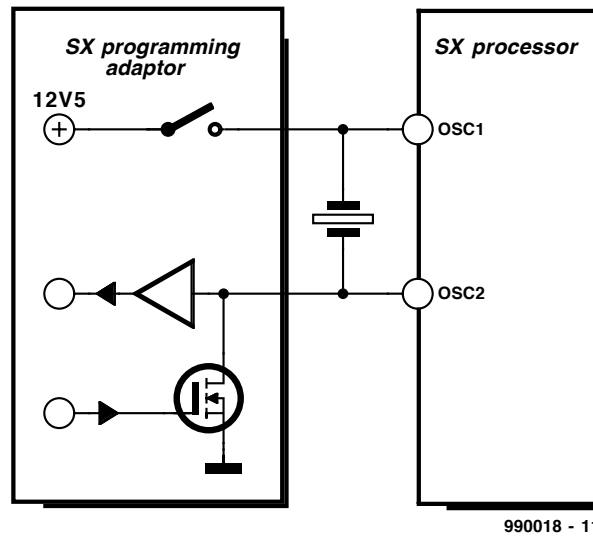


Figure 2. Principle of in-circuit serial programming (ISP) of the SX controller by way of the two oscillator pins on the chip.

tions have a width of 12 bits and arrive by way of a 4-stage Pipeline. That is why branch (jump) instructions take more than one clock cycle to execute, after all, the pipeline contents has to be handled first.

There is an internal, independent watchdog circuit which is useful if not essential for no-break systems. An 8-bit timer is available with somewhat limited possibilities, although that is easily compensated by the high processing speed of the SX. The interrupt unit is triggered by this timer or the wake-up unit in Port B. In this way, level changes on the 8-bit Port B may be sued to request interrupt servicing. A welcome extra in this arrangement is the constant latency of 60 ns at a 50 MHz clock rate, which guarantees jitter-free interrupt servicing. This useful feature is found on very few processors indeed.

A number of registers is available, including W, FSR, PC and STATUS, which serve to select options — they may be used as register pointers or auxiliary registers for the arithmetic logic unit (ALU). The arithmetic unit is capable of performing 8-bit subtraction and addition. Special attention should be given to the 'carry' bit. By means of an option you choose during programming, the carry bit is either taken into account or ignored. This will take some getting used to, and requires strict discipline, particularly with program parts you have not written yourself.

The regular logic combination options are all available. A hardware multiply unit is, however, not found in the SX.

The instruction set contains a large number of instructions for bit testing and setting, so that bit manipulation and logic interrogations are easily implemented. Most transfers and oper-

ations are performed with the aid of the W register. To add two values loaded from

memory, you normally need two instructions. That is the hallmark of the RISC instruction set — complex operations are simply implemented by calling in the help of several RISC instructions.

The processor core employs an internal 136-byte RAM, whose contents may be addressed by means of RISC bank-switching commands. This procedure should be familiar from PIC programming as described by Microchip. Those of you who 'grew up' with the 8051 may find this a little unusual, though. The program is contained in a 2-kword (12-bit wide) EEPROM, which may be accessed externally by way of the ISP interface. More real-world connections are available through ports A, B and C, whose inputs can be set up as Schmitt-triggers or made to respond to different levels. The output lines offer even more options and should be suitable for a vast number of applications. Any indi-

vidual output line is capable of supplying up to 30 mA for 'high' as well as 'low' levels. This enables LEDs to be driven directly. The chip architecture also comprises an analogue comparator. This sub-circuit may be interrogated via port B, and should enable efficient communication with analogue peripherals to be set up quite easily.

THE KEY TO THE SX

For your first experiments with a new processor you obviously need a programmer, an evaluation board (preferably several) and software (assembler and the like). Although the SX starter kit from Parallax (www.parallaxinc.com) also offers debugging tools and a development system, it is far more expensive than comparable starter kits for other modern microcontrollers. The Parallax starter kit contains the so-called SX-key, which is basically a programming interface that enables programs to be downloaded into the processor. Unfortunately, the SX-key is not supplied separately. The fairly high cost of getting started with the SX micro prompted the author to design his own programming adaptor called SX-PICKALOCK. Although it does not include a program debugging facility (the Scenix debug interface is proprietary), the system as described here does allow you to get started and apply debugging techniques you may already know. So how is the SX chip programmed?

IN-CIRCUIT SX PROGRAMMING

Scenix have designed an ingenious protocol that enables the SX processor to be programmed via the two pins normally connected to the quartz crystal! Using suitably designed circuitry it is even possible to apply the protocol without removing the crystal from the circuit. In other words, in-circuit serial programming (ISP) is a reality with the SX.

Table 2

Bits	Command	
C3 - C0 hex		
1111 = 0F	NOP	(idle)
0000 = 00	ERASE	clear all EEPROM cells
0001 = 01	READ-DEV	read device word
0010 = 02	READ-FUSEX	read FUSEX word
0011 = 03	PROG-FUSEX	program FUSEX word with LOAD-REG
0100 = 04	LOAD	copy data into LOAD-REGISTER
0101 = 05	PROG	store data from LOAD-REG into current address
0110 = 06	READ	read data from current address
0111 = 07	INC	increment current address

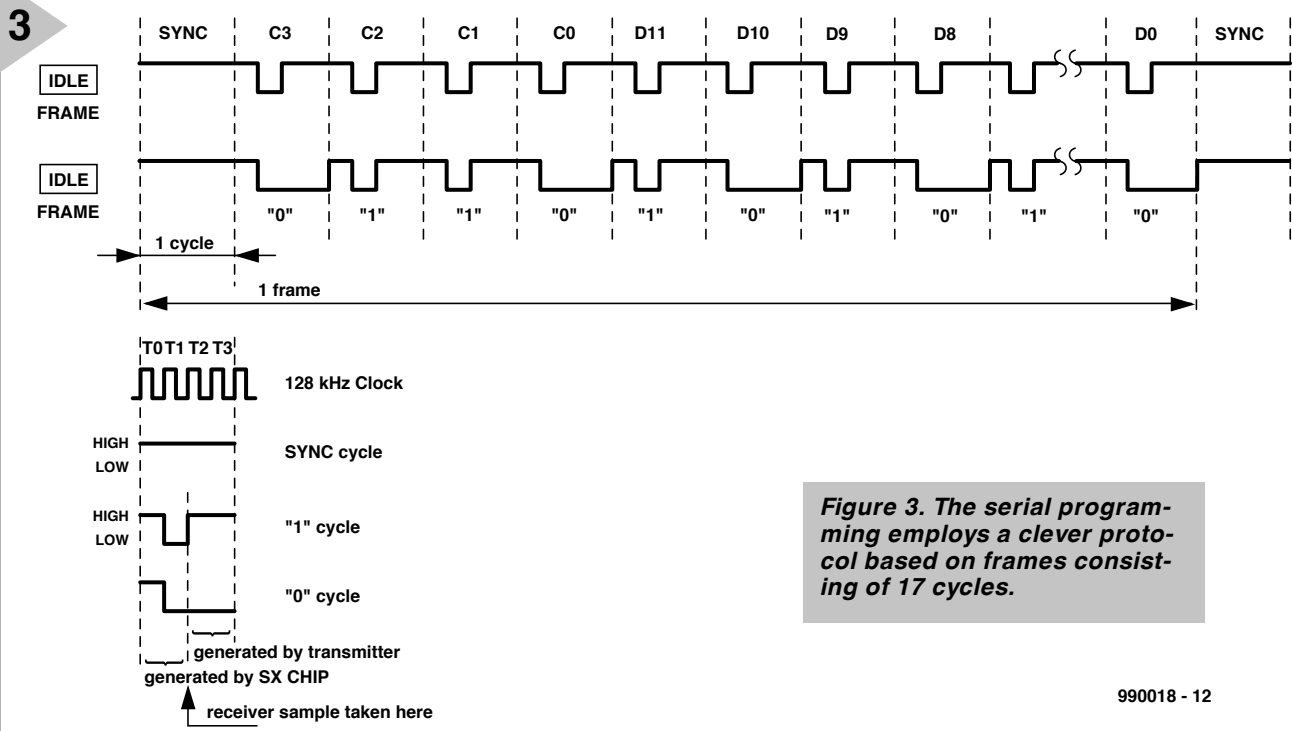


Figure 2 shows the basic circuit that gives the PICKALOCK access to the SX processor. To switch the SX chip to ISP mode, the voltage at the OSC1 pin has to be raised to 12.5 V. First, however, the internal SX oscillator has to be disabled as described in the ISP specification which may be found in the documentation supplied by Scenix.

Once in ISP mode, the SX processor starts an internal oscillator which controls the complete timing of the programming sequence. Data is then exchanged via the OSC2 pin, which acts as a kind of open-drain bus together with the OSC2 connection of the SX-PICKALOCK and an internal pull-up resistor inside the SX chip.

TWO-WAY DATA TRAFFIC

The serial protocol is based on frames consisting of 16 data bits. A frame is divided in 17 cycles, the first one acting as a synchronisation aid. The remaining 16 cycles provide the actual data transfer. The system is illustrated in Figure 3.

Every individual cycle consists of four equally long parts, T0 through T3. There are three types of cycle. In a sync cycle, the OSC2 signal is high all the time. In a '1' cycle, the OSC2 signal is

high in the parts called T0, T2 and T3, and low in the part called T1. In a '0' cycle, the OSC2 signal is high during the T0 part, and low in the T1, T2 and T3 parts. The currently active transmitter defines the state during the T2 and T3 parts. The receiver interrogates the level at the OSC2 input on the transition from T2 to T3. When the SX-PICKALOCK idles, i.e., does not execute commands, and the SX chip is in programming mode, the latter always transmits frames consisting of a sync cycle and 16 '1' cycles (IDLE frame in Figure 3).

This frame allows the SX-PICKALOCK to find out when the frames start. Once frame synchronisation has been achieved, the SX chip and the SX-PICKALOCK are ready to start exchanging data and commands. Each frame always 'moves' 12 bits of data, and 4 bits of command information. The first four bits (C3 through C0) in a frame are the command bits (MSB-first). These are always transmitted by the SX-PICKALOCK. Depending on the command, the next 12 bits then travel from the SX chip to the PICKALOCK, or the other way around. The available commands are listed in Table 2. Figure 3 indicates a READ frame with the following bit levels: C3-

C0 = 0110, D11-D0 = 10101...0.

TRANSMISSION SPEED

The documentation supplied by Scenix via their web site states that each interval of T0 to T3 equals a 128-kHz clock. In other words, a cycle has a length of $4/128,000$ seconds or 31.25 ns. On a couple of early processors (data code 9818) a clock rate of about 105 kHz was measured. Apparently the internal oscillator which creates the clock signal was a bit too slow. A similar point was found in the Errata sheets about the internal RC oscillator which may be used to clock the oscillator. According to Scenix, 3.2 MHz was reached instead of 4 MHz, and doing the sums, $128 \text{ kHz} \times 3.2/4 = 102 \text{ kHz}$, provides a good explanation of the actually measured clock rate. The upshot was that the PICKALOCK had to be designed such that it would be able to handle different bit rates. The current version accepts bit rates between 95 kHz and 140 kHz, which should be sufficient for most, if not all, practical purposes.

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In next month's instalment we will describe the construction and practical use of the SX-PICKALOCK, and the demo boards will also be described.

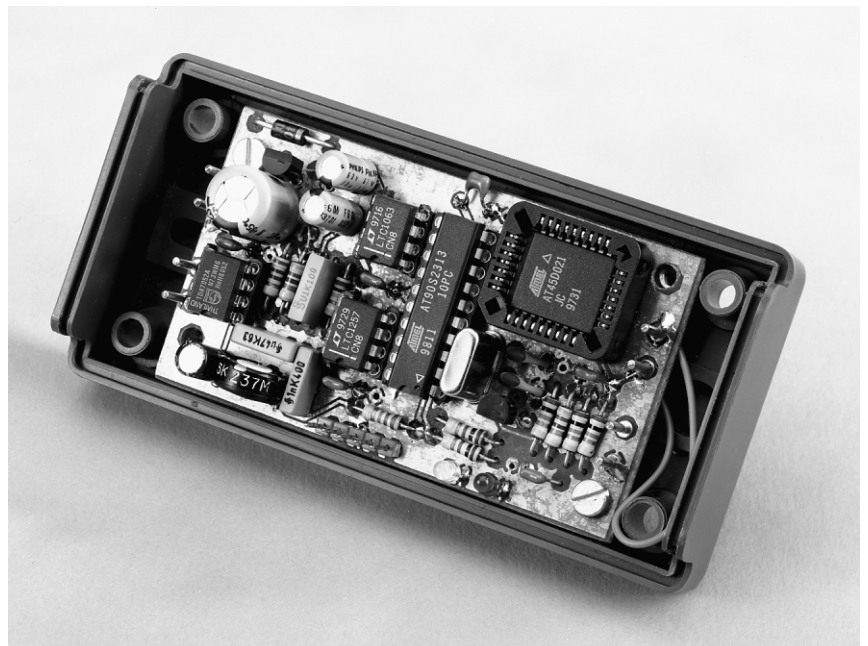
wave file player

a music box that you can program with your PC

Specifications

Controller:	Atmel AT90S2313
Memory:	2 Mbit flash ROM
D/A converter:	12-bit
Filter:	5th-order switched-capacitor
Serial interface:	RS232
Serial format:	57k6, 8N1 *
Sampling frequencies:	6, 8, 11.025 & 22.05 kHz
Playback:	monophonic
Word size:	8 or 16 bits
Playing time:	8 to 43 seconds
Amplifier:	1 watt bridge

* see text



The wave file player is yet another circuit that offers the prospect of several hours of enjoyable tinkering. The PC and the soldering iron work as partners on this project. You have to admit that this is an Elektor project in its best form. The result is a compact circuit that, on command, plays back a sound file that has been previously downloaded via the PC. The wave player can be used as a programmable doorbell, but it can also be used for model railroading or to amuse your children. Depending on the desired sampling frequency and resolution, it can store up to 43 seconds' worth of sound.

Using modern electronic components, it is possible to pack a lot of functions onto a relatively small circuit board. The circuit is also based on existing standards. In practice, this means that the controller works with 'wav' (wave) files. These are familiar to every PC user. Another important factor is that the configuration of the player is automatically derived from data in the sound files, so that the best possible sound quality is always guaranteed.

BASIC ASSUMPTIONS

A number of considerations played a role in the development of the wave file player. We wanted it to be compact, utilize industry standards and be flexible in use.

The interface with the PC allows all the 'tunes' that the player has to reproduce to be generated conveniently and 'made to measure'. Depending on the capabilities of the PC used, sound fragments can be taken from a CD (but

watch out for copyright restrictions) or sampled via a sound card. You can use a sound editing program for this (such as the shareware program Cool Edit). Also, thanks to the 'universal' approach used in the design, a Windows environment is not essential. The only thing that you need is a program that can generate and edit wav files. The resulting file must be transferred to the player as a data file, via an RS232 interface. Standard terminal programs can be used for this, as long as they support RAW ASCII. In addition, there is a specially-prepared downloader program available for Windows users.

A CLOSER LOOK AT THE HARDWARE

The block diagram of the hardware design is shown in **Figure 1**. The heart of the circuit is an AT90S2313 IC, which can be connected to a PC via an RS232 interface. On the analogue side we find a D/A converter, a configurable low-pass filter and an adjustable output amplifier. The data are stored in a flash memory. All that's left is the power supply: from a 9 V input, it provides the circuit with 8.4 V and 5 V working voltages. The user interface consists of one switch ('play') and two LEDs ('recording' and 'playing').

Thanks to the power of the controller used here, the entire hardware design needs only five integrated circuits. **Figure 2** shows the full schematic diagram. The serial interface consists of no more than a single transistor and three resistors. The hardware around the CPU can be quickly described. The

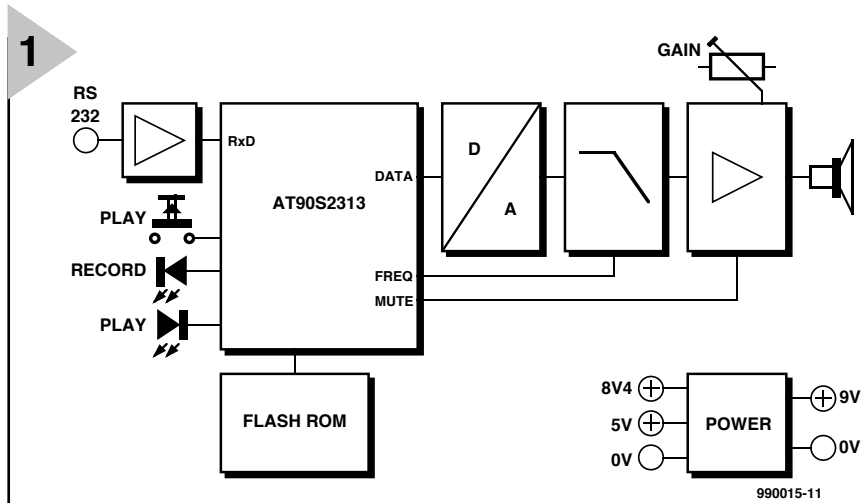


Figure 1. Block diagram of the wave file player.

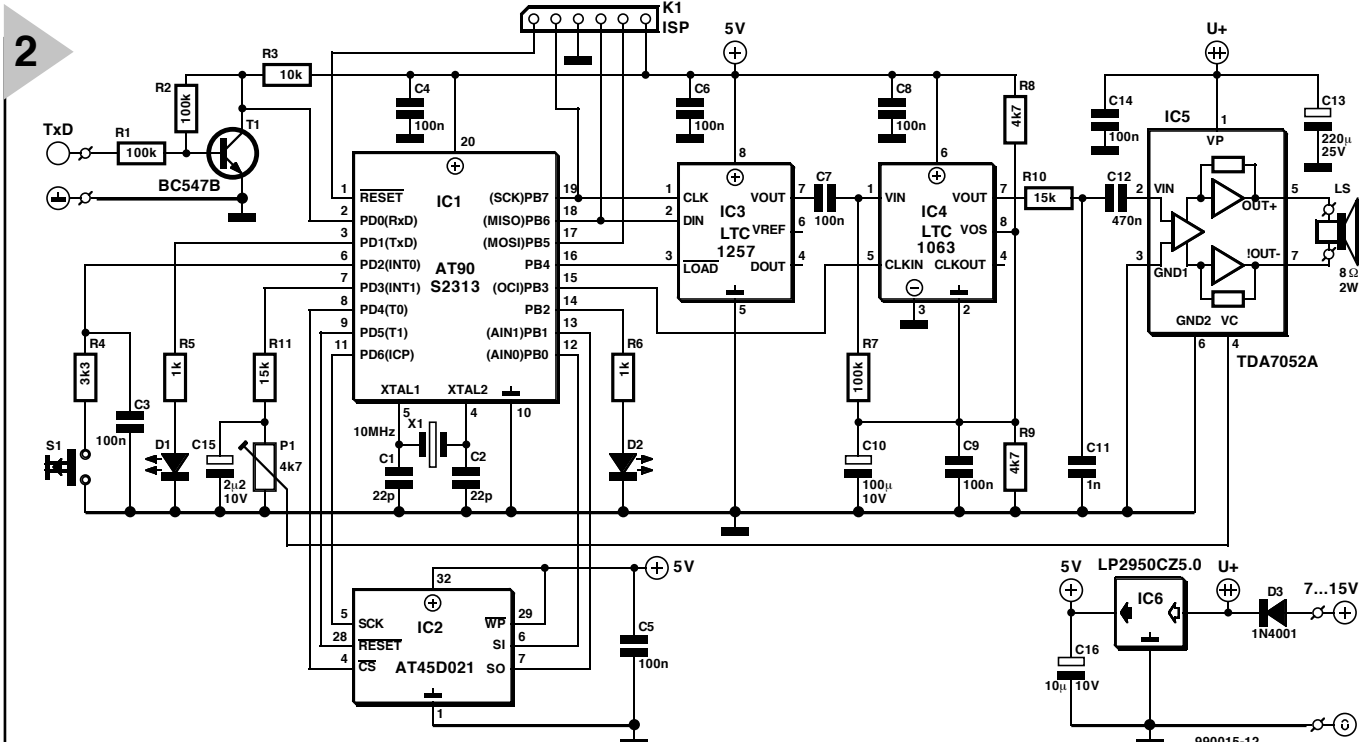
oscillator components are X1, C1 and C2. The 'play' switch is debounced in software, and resistor R4 protects the IC against electrostatic discharges. Capacitor C3 suppresses any coupled-in high-frequency signals. LEDs D1 and D2 are connected to one of the controller's I/O ports via series resistors. The 2-Mbit flash memory, IC2, is organized as 1024 pages each holding 264 bytes. Since it takes 64 clock cycles to read out one page, it is not possible to simply transfer data directly from the flash memory to the D/A converter. A 64-byte circular buffer in RAM is used to deal with this problem. Data are read from the circular buffer while a page

address is being sent to the flash memory. In addition, the data are organized so that the least possible amount of time is lost in reading the data.

The D/A converter is connected to the CPU via three signal lines (CLK, DIN and LOAD). Its output signal (V_{out}) is capacitively coupled to the input of the low-pass filter (IC4). The LTC1063 chip used here is a switched-capacitor device, which filters the analogue signal under control of the CPU. A circuit trick is used to set the input level to the filter to 2.5 V. The necessary

Figure 2. From theory to practice: the complete circuit requires only five integrated circuits.

supplementary voltage is provided by R8 and R9. Resistor R7 provides a relatively high-



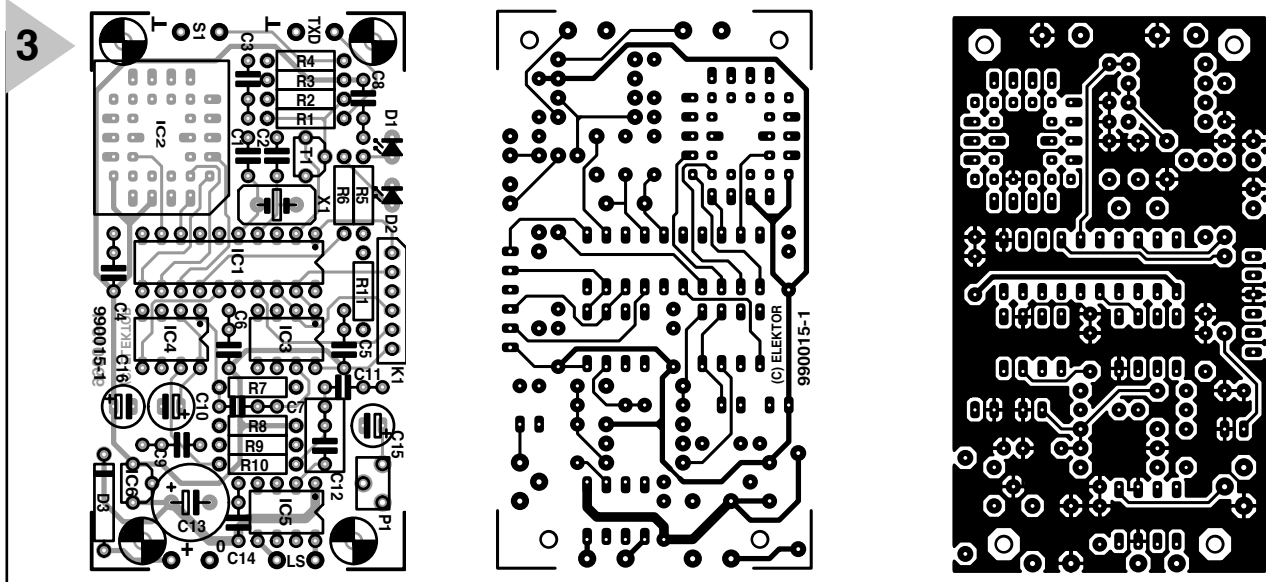


Figure 3. The copper-track layout and component overlay show the compactness of the player. It can easily be fitted into a small enclosure.

impedance path for this voltage to the input of IC4. The filter characteristics can be adjusted by varying the frequency of its clock signal.

The final part of the circuit is the output amplifier IC5. The TDA7052A IC is wired as a bridge amplifier and provides an output power of 1 watt. The volume level can be adjusted via P1. The PD3 output of the processor controls the mute function. The output amplifier is muted after the wave file has finished playing.

Readers who have carefully studied the schematic may well wonder about the function of K1. The answer is that this connector allows the processor to be programmed directly in the circuit. This is a handy option for anyone who wants to modify the microcontroller program to suit his own wishes. The source code of the program, which was developed in the Elektor labs, is readily available from our Readers Services (order number 996006-1).

Construction should not present any problems. A compact printed circuit board, whose copper track layout and component overlay are shown in **Figure 3**, forms the basis. If you use sockets for the ICs, almost nothing can go wrong. For this reason we can quickly shift our attention to the software, which is the key to the whole show.

WORKING WITH COOL EDIT

Wave files to be played back by this circuit must first be made to fit, and for this you will need a sound editor for the PC. One possibility is the Windows program Cool Edit, which is preferable

to various other programs since it provides good facilities for resampling sound files. This is an important task, which in large measure determines the quality of the sound.

A shareware version of Cool Edit can be found at the website <http://www.syntrillium.com>. This program has several functions that are particularly well suited to our objectives, including altering the sampling frequency, selecting a particular passage and optimizing the amplitude. In addition, it is easy to make a mono file from a stereo file. This is essential for the wave player, since it makes the file smaller. Finally, the resolution can be selected to be 8 bits (256 levels maximum) or 16 bits.

As can be seen from **Table 1**, the playing time is strongly dependent on the sampling frequency. A high sampling frequency is recommended for music (up to 22 kHz with this circuit), but a lower frequency can be used for speech. By and large, a sampling rate of 8 kHz yields a signal whose sound quality is equal to that of a good telephone connection.

The difference between 8-bit and 16-bit resolution can be seen in the signal-to-noise ratio. The lower the resolution, the larger the steps. With 8 bits, only 256 signal levels are possible. A larger step size results in a greater difference between the actual value and the desired amplitude, which increases the noise and distortion levels. For the best quality, 16-bit resolution should be used. Note also that the player circuit reduces this to 12 bits, since the D/A converter has its own limitations. With these 12 bits we achieve an optimum

COMPONENTS LIST

Resistors:

R1,R2,R7 = 100kO
 R3 = 10kO
 R4 = 3kO3
 R5,R6 = 1kO
 R8,R9 = 4kO7
 R10,R11 = 15kO
 P1 = 4kO7, preset V

Capacitors:

C1,C2 = 22 pF, ceramic
 C3...C6,C8,C9,C14 = 100nF, ceramic
 C7 = 100nF, MKT
 C10 = 100µF 16V, radial
 C11 = 1nF, MKT
 C12 = 470nF, MKT
 C13 = 220µF 25V, radial
 C15 = 2µF2 10V, radial
 C16 = 10µF 10V, radial

Semiconductors:

D1 = LED, high eff. red
 D2 = LED, high eff. green
 D3 = 1N4001
 T1 = BC547B
 IC1 = AT90S2313 10PC (order code 996505-1)
 IC2 = AT45D021JC
 IC3 = LTC1257 CN8
 IC4 = LTC1063 CN8
 IC5 = TDA7052A
 IC6 = LP2950CZ5.0

Miscellaneous:

32-way PLCC socket for IC2
 S1 = pushbutton 1 make contact
 LS = 8Ω 2W
 K1 = 6-pin SIL pinheader
 X1 = quartz crystal, 10 MHz
 Case: Bopla type E410
 PCB, order code 990015-1
 Programmed controller: order code 996505-1
 3.5"-floppy disk with Windows-software and source code file of controller program: order code 996006-1.

compromise between the signal-to-noise ratio and the memory capacity. The best possible sound quality can be achieved by using the sound-editing program to adjust the amplitude of the signal so that the full dynamic range is utilized.

Since the wave file player simply cuts off the sound at the end of the available playing time, it is also necessary to modify the sound file so that it starts and ends softly. A bit of experimenting will quickly teach you how everything works.

Once the file is ready, it must be transferred to the wave file player via the serial port. A terminal program can be used for this, as long as it supports the RAW ASCII option. This is the only way to be sure that the data will not be corrupted on its way to the player. For Windows users, we have developed a utility program that drastically simplifies file downloading.

This program ensures that the complete wave file is quickly and reliably transferred to the player's memory. Proper configuration of Cool Edit is important, since the controller software checks the structure of the wave file. When the file is received, it is checked to see that:

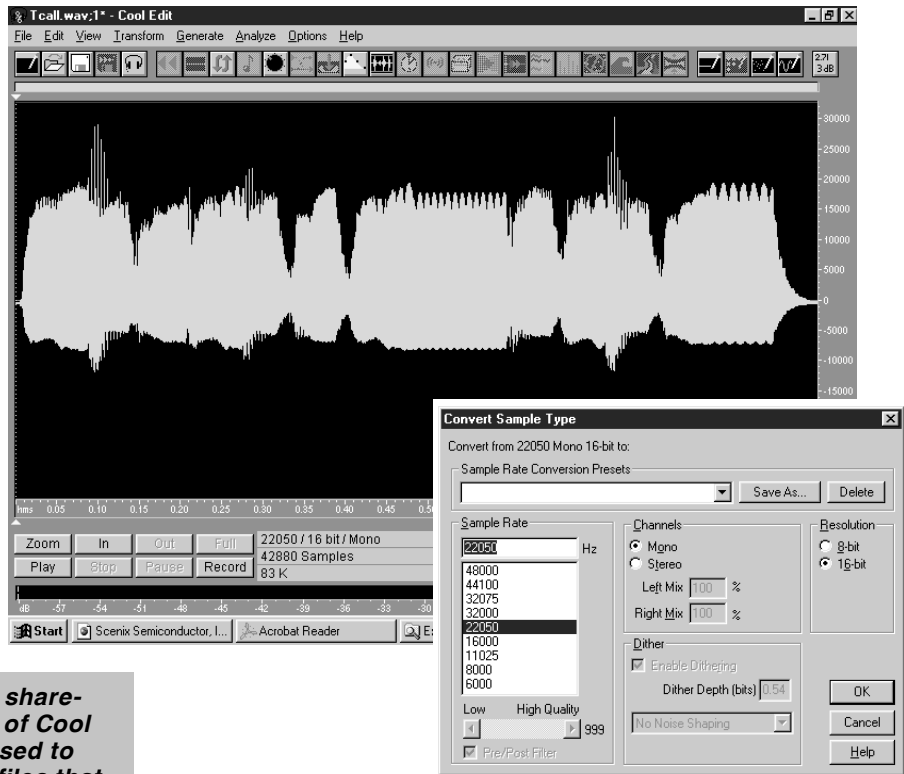
- it is a wav file,
- the sampling frequency is equal to one of the predefined values;
- the signal is monophonic;
- PCM coding is used and
- the word size is 8 or 16 bits.

If all these conditions are satisfied, then the file can be properly read in. If an error is detected, the red LED is immediately lit.

There is in practice a problem when Windows 3.1 is used. With this software the maximum speed of the serial interface is considerably less than 57.6 kbps, which is used here. It is thus necessary to drop back to a lower speed. If switch S1 is held depressed while the power is switched on, a serial data rate of 9600 baud is selected. All other settings remain unaltered.

The red LED (D1) flashes while data are being downloaded. As soon as the flash ROM is full, it stays on continuously. If no more data are sent to the controller for an interval of 500 ms, the

Figure 4. The shareware version of Cool Edit can be used to make sound files that are suitable for the wave file player.



LED is extinguished.

The green LED (D2) is lit when power is applied to the circuit. It flashes while a stored wave file is being played back (in response to pressing S1).

If the player is used as a doorbell, a mains adapter can be used to supply it with power. The doorbell switch then functions as S1. You can welcome your guests on special occasions (such as

Christmas or a birthday) by loading an appropriate tune in the ROM. You could also consider programming the sound of barking dogs for your vacation time. This should confuse would-be thieves who try to see if anyone is at home by ringing the doorbell!

(990015-1)

Table 1. Files, formats and playing times.

Sampling rate	word size	file size	playing time
22.05 kHz	8	256 k	11.92 s
	16/12	341 k	7.94 s
11.025 kHz	8	256 k	23.83 s
	16/12	341 k	15.89 s
8 kHz	8	256 k	32.77 s
	16/12	341 k	21.85 s
6 kHz	8	256 k	43.69 s
	16/12	341 k	29.13 s

Titan 2000

High-power hi-fi and public-address amplifier

It could be argued that most of the output amplifiers published in this magazine lack power.

Although this is a debatable point, it was felt that a true heavyweight output amplifier would make a welcome change for many constructors. The Titan 2000 can produce 300 watts into 8 Ω , 500 watts into 4 Ω , and 800 watts into 2 Ω . For those who believe that music power is a reputable quantity, the amplifier can deliver 2000 watts of this magical power into 4 Ω .



Brief parameters

<i>Sine-wave power output</i>	300 W into 8 Ω ; 500 W into 4 Ω ; 800 W into 2 Ω
<i>Music power*</i>	2000 W into 4 Ω
<i>Harmonic distortion</i>	< 0.005%
<i>Slew limiting</i>	85 V μ s ⁻¹
<i>Open-loop bandwidth</i>	55 kHz
<i>Power bandwidth</i>	1.5 Hz – 220 kHz

* See text about the validity of this meaningless quantity.

INTRODUCTION

Amplifier output has been a cause of argument for as long as there have been audio power amplifiers. For domestic use, a power rating of $2 \times 50 \text{ W}$ is more than sufficient. With the volume control at maximum and the use of correctly matched good-quality loudspeakers, this will provide

'PROGRAMMABLE' POWER OUTPUT

The amplifier has been designed in such a manner that its output is 'programmable' as it were. With a sine wave input, it delivers an average power of 300 W into an 8Ω load, which should meet the requirements of all but the power drunk. Compared

age across the loudspeaker and the r.m.s. current flowing into the speaker. The term music power is generally meaningless, because to some manufacturers it means the product of the peak voltage and peak current; to others it means merely double the true power; and to yet others, even more disreputable, it means quadrupling the true power).

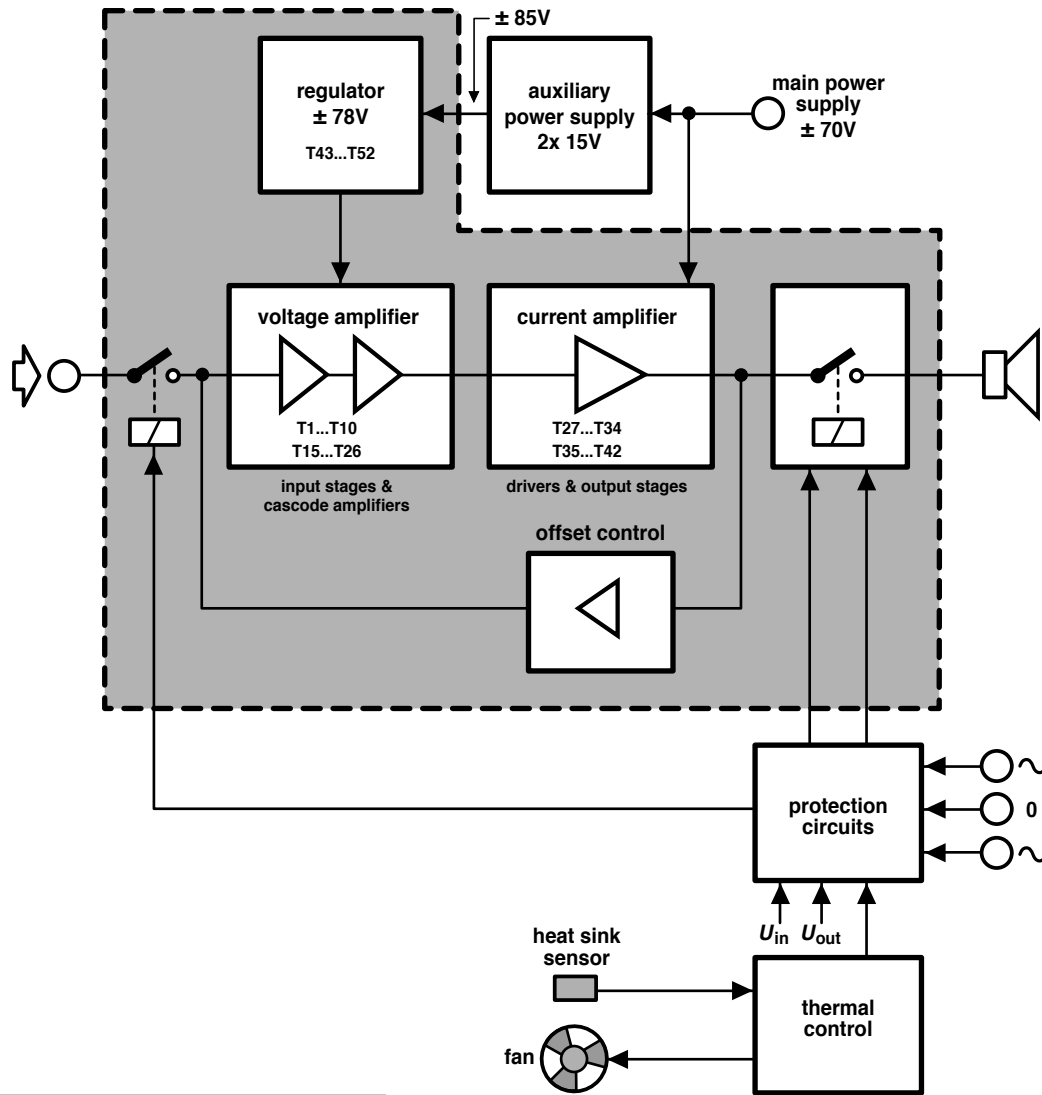


Figure 1. Simplified block diagram of the Titan 2000. The auxiliary power supply, protection networks and thermal control are discrete circuits built on discrete PCBs.

a sound pressure level (SPL) equivalent to that of a grand piano being played forte in the same room.

However, not all amplifiers are intended for domestic use: many are destined for discos, small music halls and other large rooms. But even here, what power is really required? Since doubling the amplifier output increases the SPL by a barely audible 3 dB, it was felt that 300 watts sine wave power into 8Ω would appeal to many.

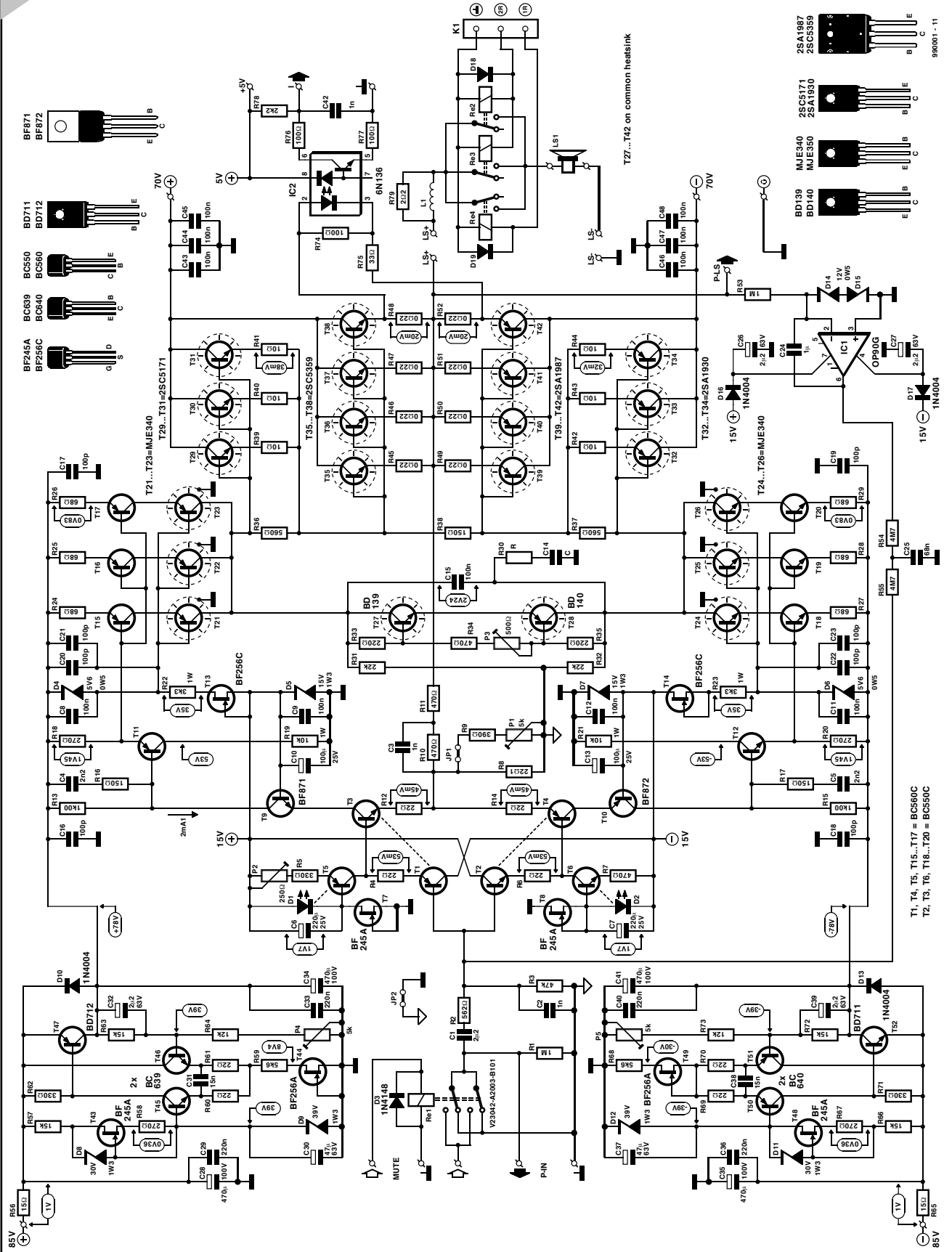
with the output of 50 W from a domestic audio amplifier, this gives an increase in SPL of 7.5 dB. If even higher outputs are needed, the load impedance may be lowered to 4Ω , which will give an increase in SPL of 10 dB compared with a 50 W output.

Although music power is a deprecatory term, since it does not really give the true power rating of an amplifier, readers may note that the Titan 2000 can deliver 2 kW of this magical power into 4Ω . (True power is average power, that is, the product of the r.m.s. volt-

However, power is not the only criterion of an amplifier. Low distortion, good slew limiting, and an extended power bandwidth, as possessed by the Titan 2000, are also hallmarks of a good amplifier.

Power bandwidth denotes the frequency range over which the power falls to not less than half its maximum value. This is much more telling than the frequency response, which is usually measured at a much lower output level.

Slew limiting is the maximum input voltage change that can occur in one

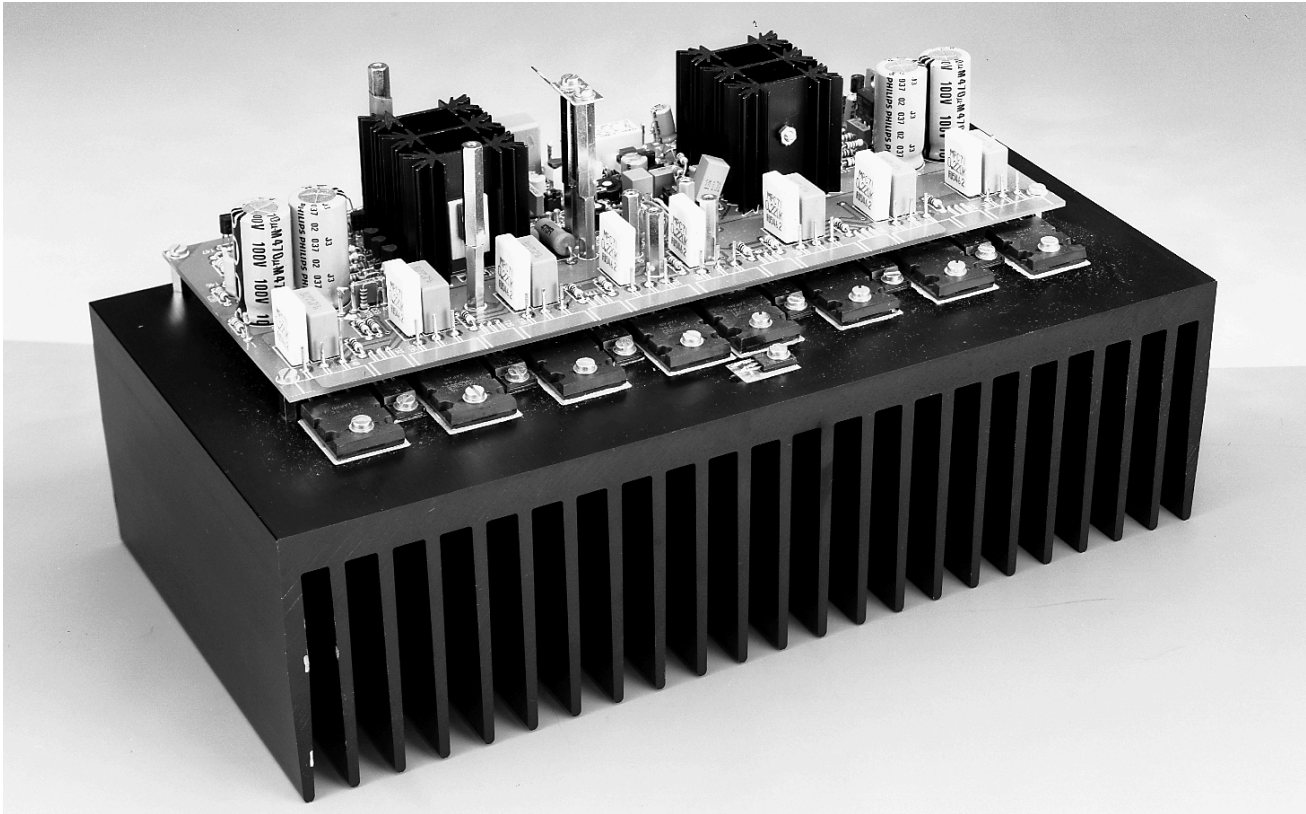


- BF245A
- BC639
- BC640
- BC580
- BD711
- BD712
- BF871
- BF872
- T21...T23=MJE340
- T29...T31=2SC5171
- T35...T38=2SC5359
- T39...T42=2SA1987
- T24...T26=MJE340
- T1, T4, T5, T15...T17 = BC60C
- T2, T3, T6, T18...T20 = BC50C

- 2SA1987
- 2SC5359
- MJE340
- MJE350
- BD139
- BD140
- 2SC5171
- 2SA1930

990001 - 11

Figure 2. Although the circuit diagram gives the impression of a highly complex design, the amplifier is, in essence, fairly straightforward.



microsecond, and to which the amplifier can respond.

DESIGN CONSIDERATIONS

The Titan 2000 is based on the 'compact power amplifier' published in the May 1997 issue of this magazine. That was a typical domestic amplifier with a power output of 50 W into 8 Ω or 85 W into 4 Ω . The special property of this fully balanced design was the use of current feedback instead of voltage feedback, which resulted in a fast-responding amplifier with a large open-loop bandwidth. The amplifier performed well both as regards instrument test and measurements and listening tests. However, to serve as a basis for the Titan 2000, its output current and drive voltage range had to be increased substantially.

For a start, the supply voltage has to be more than doubled, which means that transistors with a higher power rating have to be used in the power supply. The higher supply voltage also results in larger potential drops across a number of components, and this means that dissipation problems may arise.

The large output current required for the Titan 2000 makes a complete redesign of the current amplifier used in the 'compact power amplifier' unavoidable, since that uses insulated-gate bipolar transistors (IGBTs). Although these are excellent devices, the large spread of their gate-emitter voltage makes their use in parallel net-

works next to impossible. To obtain the requisite output power, the use of parallel networks of symmetrical pairs of transistors is inevitable.

In view of the foregoing, bipolar transistors are used in the current amplifier of the Titan 2000. However, these cannot be driven as readily as IGBTs, which means that current drive instead of voltage drive is used. This entails a substantial upgrading of the driver stages and the preceding cascode amplifiers (which also consist of a couple of parallel-connected transistors). The good news is that the power transistors in the Titan 2000 are considerably less expensive than IGBTs: an important factor when eight of these devices are used.

Finally, the protection circuits have been enhanced in view of the higher voltages and currents. The circuits protecting against direct voltages and short-circuits are supplemented by networks protecting against overload and (too) high temperatures. The latter is coupled to a proportional fan control.

In short, a large part of the Titan 2000 is a virtually new design rather than a modified one.

BRIEF DESCRIPTION

The block diagram of the Titan 2000 is shown in **Figure 1**. The voltage amplifier consists of input stages T_1 - T_{10} , and cascode amplifiers/pre-drivers T_{15} - T_{26} . The current amplifier is formed by driver transistors T_{27} - T_{34} , and output

transistors T_{35} - T_{42} .

The offset control stage prevents any direct voltage appearing at the output of the amplifier.

The loudspeaker is linked to the amplifier by three heavy-duty relays.

The current amplifier operates from a ± 70 V supply, which is provided by two 50 V mains transformers. To enable the voltage amplifier to drive the current amplifier to its full extent, it needs a slightly higher supply voltage to compensate for the inevitable losses caused by inevitable voltage drops. This is accomplished by superimposing a ± 15 V potential from an external auxiliary supply on to the main ± 70 V supply and dropping the resulting voltage to ± 78 V with the aid of regulator T_{43} - T_{52} .

The combined protection circuits constantly compare the input and output voltage of the amplifier: any deviation from the nominal values leads to the output relays disconnecting the loudspeaker and the input relay decoupling the input signal.

The thermal protection circuit monitors the temperature of the heat sink and, if necessary, switches on a fan. If, with the fan operating, the temperature approaches the maximum permissible limit, the output relays are deenergized and disconnect the loudspeaker.

CIRCUIT DESCRIPTION

The circuit diagram of the Titan 2000 is shown in **Figure 2**. In spite of the large number of components, the basic cir-

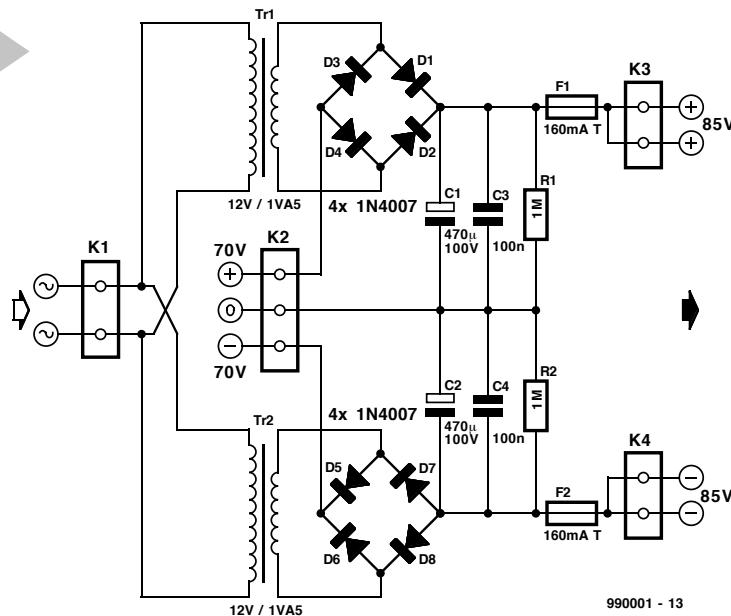


Figure 3. Circuit diagram of the requisite auxiliary power supply.

cuit is straightforward.

As already noted in the previous paragraph, transistors T_1 – T_{10} form the input amplifier, T_{11} and T_{12} are buffers, T_{13} and T_{14} are current sources, T_{15} – T_{26} form the cascode amplifier/pre-driver stage, T_{27} – T_{34} are the driver transistors in the current amplifier, T_{35} – T_{42} are the output transistors, and T_{43} – T_{52} form a sophisticated supply voltage regulator.

Input amplifier

Strictly speaking, the input amplifier is formed by transistors T_3 – T_4 . Cascode stages T_9 – T_{10} serve merely to enable the input section handling the high voltages. These voltages are limited by zener diodes D_5 and D_7 , which are part of the potential divider that also sets the operating points of T_{21} – T_{26} . In view of the requisite stability, the current through the zener diodes is held constant by current sources T_{13} and T_{14} . Resistors R_{22} and R_{23} limit the potential across, and thus the dissipation in, these field-effect transistors.

Otherwise, the input section is virtually identical to that of the 'compact power amplifier'. The drop across the emitter resistors of buffers T_1 and T_2 determines the drop across the emitter resistors of T_3 and T_4 , and consequently the setting of the operating point of the overall input section. To eliminate the influence of temperature variations, T_1 is thermally coupled to T_3 and T_2 to T_4 .

Since the operating point of buffers T_1 and T_2 is critical, current sources T_5 and T_6 have been added. The reference for these current sources is provided by light-emitting diodes (LEDs) D_1 and D_2 . The current through these diodes is determined by current sources T_7

and T_8 . In view of the requisite stability, diode D_1 is thermally coupled to T_5 and D_2 to T_6 .

Any imbalance of the input stages is compensated by making the current through T_5 equal to that through T_6 with potentiometer P_2 .

Cascode amplifiers/pre-drivers

The large output current of the Titan 2000 necessitates a proportionally large pre-drive voltage, which is provided by three parallel-connected cascode amplifiers, T_{15} – T_{26} . The current through these amplifiers is arranged at 10–15 mA, but the current feedback used may cause this level to be appreciably higher. This is the reason that the transistors used in the T_{21} – T_{26} positions are types that can handle currents of up to 50 mA when their collector-emitter voltage is 150 V.

The input section is linked to the cascode amplifiers by buffers T_{11} and T_{12} , which results in a lowering of the input impedance. The arrangement also enables an increase in the values of R_{13} and R_{15} , which results in a 3 dB increase in amplification of the input section.

The function of resistors R_{19} and R_{21} is threefold: they limit the dissipation of the buffers; they obviate the need of an additional voltage to set the operating point of the buffers; they limit the maximum current through the buffers, and thus the cascode amplifiers, to a safe value.

The open-loop amplification of the Titan 2000 is determined solely by those of the input section and cascode amplifiers. The amplification of the input section depends on the ratios $R_{13}:(R_{12}+R_8)$ and $R_{15}:(R_{14}+R_8)$ and, with values as specified is $\times 10$ (i.e., a

gain of 20 dB).

The amplification of the cascode amplifiers is determined largely by the ratio of parallel-connected resistors R_{31} and R_{32} and the parallel network of R_{24} – R_{26} . With values as specified, the amplification is about $\times 850$ (remember, this is a push-pull design), so that the overall amplification of input section plus cascode amplifiers is $\times 8500$ (a gain of close to 80 dB).

Current amplifier

Since one of the design requirements is that the amplifier is to work with loads down to 1.5Ω , the output stages consist of four parallel-connected pairs of transistors, T_{35} – T_{38} and T_{39} – T_{42} . These transistors have a highly linear transfer characteristic and provide a direct-current amplification that remains virtually constant for currents up to 7 A.

Like the output transistors, the driver stages need to remain within their safe operating area (SOA), which necessitates a threefold parallel network. The transistors used in the driver stages are fast types ($f_T = 200 \text{ MHz}$).

Setting the bias voltage for the requisite quiescent current is accomplished by balanced transistors T_{27} and T_{28} . These transistors are mounted on the same heat sink as the output transistors and driver transistors to ensure good thermal coupling and current control. Of course, the current rises during full drive conditions, but drops again to its nominal level when the amplifier cools off. The quiescent current is set to 200 mA with potentiometer P_3 .

Owing to the large output current, the connection between amplifier output and loudspeaker is not arranged via a single relay, but via three. Two of these, Re_3 – Re_4 , are controlled in synchrony by the protection circuits. When they are deenergized, their disabling action is delayed slightly to give the contacts of the third relay, Re_2 , time to open, which is of importance in a fault situation.

Input relay Re_1 is switched off in synchrony with Re_2 to ensure that there is no input signal by the time Re_3 and Re_4 are deenergized.

Optoisolator IC_2 serves as sensor for the current protection circuits. The light-emitting diode in it monitors the voltage across R_{48} – R_{52} via potential divider R_{74} – R_{75} , so that the positive as well as the negative output currents are guarded. The use of an optoisolator prevents earth loops and obviates compensation of the $\pm 70 \text{ V}$ common-mode voltage. The $+5 \text{ V}$ supply for the optoisolator is derived from the protection circuits.

Feedback

The feedback loop runs from the out-

put of the power stages to the junction of T_3 and T_4 via resistors R_{10} and R_{11} . This is current feedback because the current through T_3 and T_4 depends on the potential across R_8 , which is determined largely by the current through R_{10} and R_{11} . The overall voltage amplification of the output amplifier is determined by the ratio $R_8:(R_{10}+R_{11})$.

Compensation

Capacitors C_3 – C_5 and resistors R_{16} , R_{17} form part of the compensation network required for stable operation.

Low-pass filter R_2 – C_2 at the input is essential to prevent fast, that is, high-frequency, signals causing distortion. This filter is also indispensable for stability's sake.

Coupling capacitor C_1 is needed because the available offset compensation network merely redresses the bias current of the input buffers and is not intended to block any direct voltages at the input.

Relay Re_1 at the input enables the input signal to be 'switched off'. It forms part of the overall protection and in particular safeguards the input section against overdrive. The overall protection circuit will be discussed in detail next month.

Network R_9 – P_1 is intended specifically for adjusting the common-mode suppression when two amplifiers are used in a bridge arrangement. It is needed for only one of these amplifiers, and may be interconnected or disabled by jumper JP_1 as needed.

Offset compensation is provided by integrator IC_1 , which ensures that if there is any direct voltage at the output of the amplifier, the operating point of T_1 – T_2 is shifted as needed to keep the output at earth potential. The operational amplifier (op amp) used draws only a tiny current ($20 \mu A$) and has a very small input offset ($450 \mu V$).

Supply voltage for IC_1 is taken from the $\pm 15 V$ line for the input section via diodes D_{16} and D_{17} . This arrangement ensures that the supply to the IC is retained for a short while after the main supply is switched off so that any interference is smoothed out.

Diodes D_{14} and D_{15} safeguard the input of IC_1 against (too) high input voltages in fault conditions.

The values of resistors R_{54} and R_{55} arrange the level of the compensating current at not more than $1 \mu A$, which is sufficient to nullify the difference between the base currents of T_1 and T_2 .

Regulation

Although current feedback has many advantages, it also has a serious drawback: poor supply voltage suppression. This makes it essential for the supply voltage for the voltage amplifier to be regulated. In view of the requisite high symmetrical potential and the fact that the unregulated voltage that serves as input voltage can vary substantially under the influence of the amplifier load, two discrete low-drop regulators, T_{43} – T_{47} and T_{48} – T_{52} are used.

As mentioned before, owing to

inevitable losses through potential drops, the supply voltage for the input section and cascode amplifiers needs to be higher than the main $\pm 70 V$ line. Furthermore, the input voltage to the regulators must be higher than the wanted output voltage to ensure effective regulation.

Fortunately, the current drawn by the voltage amplifier is fairly low (about $70 mA$) so that the input voltage to the regulators can be increased with a simple auxiliary supply as shown in **Figure 3**. This consists of two small mains transformers, two bridge rectifiers, D_1 – D_4 and D_5 – D_8 , and the necessary reservoir and buffer capacitors.

The $\pm 15 V$ output is linked in series with the $\pm 70 V$ line to give an unregulated voltage of $\pm 85 V$.

The $39 V$ reference is provided by zener diode D_9 . This means that the regulator needs to amplify the reference voltage $\times 2$ to obtain the requisite output voltage.

The zener diode is powered by current source T_{43} , to ensure a stable reference, which is additionally buffered by C_{30} .

Differential amplifier T_{45} – T_{46} , whose operating point is set by current source T_{44} , compares the output voltage with the reference via potential divider R_{63} – R_{64} – P_4 . This shows that the output voltage level can be set with P_4 .

Transistor T_{47} is the output stage of the regulator. The output voltage remains stable down to $0.2 V$ below the input voltage.

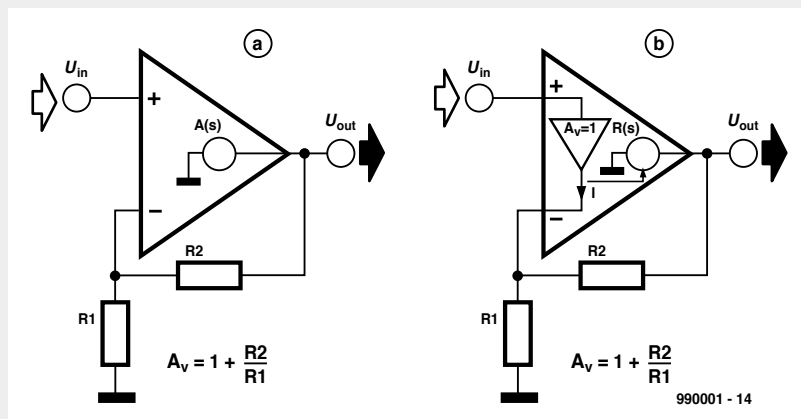
Current-feedback

In an amplifier using voltage feedback (Figure a), the differential voltage at its inputs is multiplied by the open-loop amplification. The feedback loop forces the output voltage to a level that, divided by network R_1 – R_2 , is equal to the input voltage.

Whereas an amplifier with voltage feedback has high-impedance inputs, an amplifier with current feedback (Figure b) has an high-impedance and a low-impedance input. Its input stage consists of a buffer with unitary gain between the inverting and non-inverting inputs. Essentially, the inverting input is the low-impedance input. The buffer is followed by an impedance matching stage that converts the output current of the buffer into a directly proportional output voltage.

The current feedback loop operates as follows. When the potential at the non-inverting input rises, the inverting input will also rise, resulting in the buffer current flowing through resistor R_1 . This current, magnified by the impedance matching stage, will cause the output voltage of the amplifier to rise until the output current flowing through resistor R_2 is equal to the buffer current through R_1 . The correct quiescent output voltage can be sustained by a very small buffer current. The closed-loop amplification of the circuit is determined by the ratio $(1+R_2):R_1$.

An interesting property of an amplifier with current feedback is that the closed-loop bandwidth is all but independent of the closed-loop amplification, whereas that of an amplifier with voltage feedback becomes smaller in inverse proportion to the closed-loop amplification – a relation known as the gain-bandwidth product.



Resistor R_{57} and diode D_8 protect T_{43} against high voltage during switch-on, while D_{10} prevents current flowing through the regulator in the wrong direction.

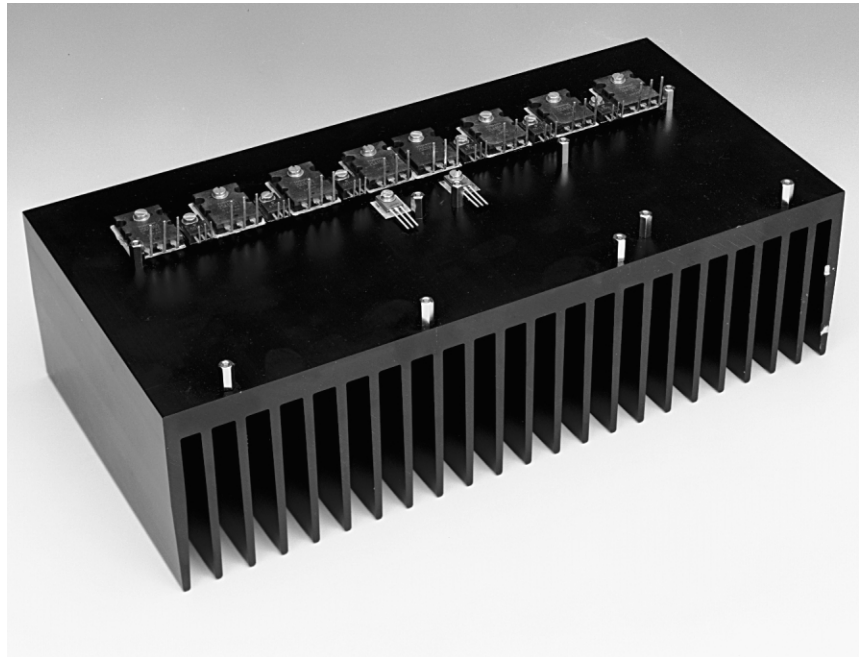
Capacitors C_{31} and C_{32} enhance the rate of operation of the regulator.

Network $R_{56}-C_{28}-C_{29}$ provides additional smoothing and r.f. decoupling of the ± 85 V lines.

NEXT MONTH

Next month's second and concluding instalment of this article will describe details of the protection circuits, the fan control, and the construction of the amplifier. The instalment will also include detailed specifications and performance characteristics.

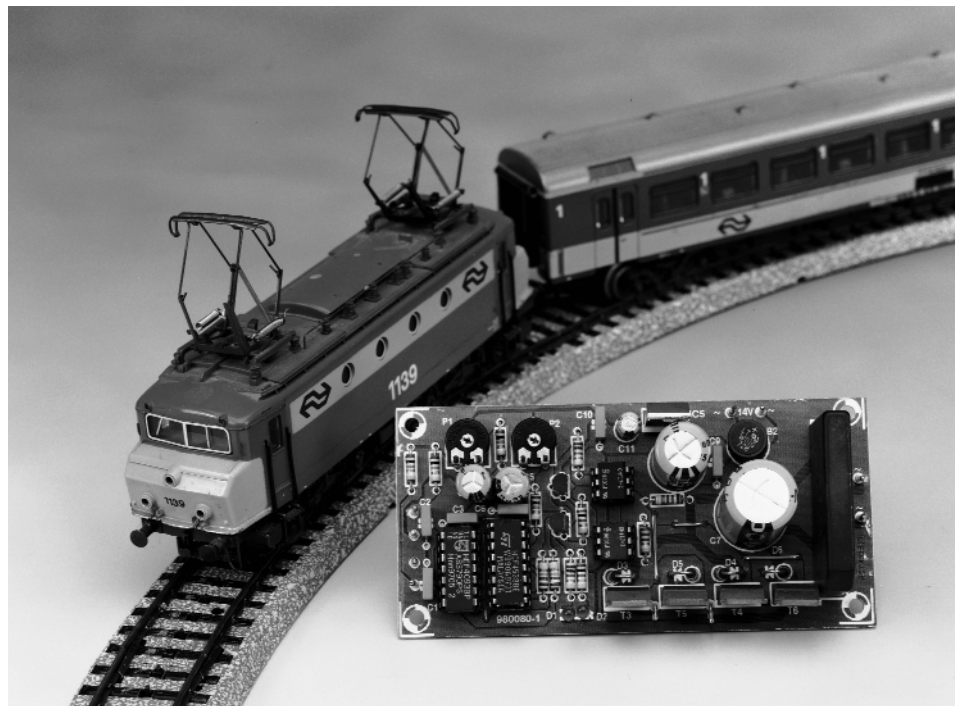
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auto shuttle service for model railway

From A to B and back

The service provided by the circuit described in this article is known as a shuttle service (as for instance through the Channel tunnel between England and France – named Le Shuttle). It enables a train to travel to and fro between two stations without the necessity for a manual instruction. Compared with a number of other types of shuttle service, the present one has several interesting advantages.



An important advantage of the present circuit is that it does not require a change-over track or platform. The point in time when the polarity of the drive voltage of the train should be reversed is determined by two reed

switches or relays in the track. This means that small magnets for operating these devices must be fitted (glued) to the underside of the locomotives used for shuttling between stations A and B.

Features:

- ✓ the distance between the two stations may be quite long
- ✓ the duration of the stop-over at each of the stations can be preset
- ✓ no run round loop required
- ✓ power lines of shuttle circuit and train are isolated
- ✓ wearfree electronic change-over of direction of travel
- ✓ standard, inexpensive components are used

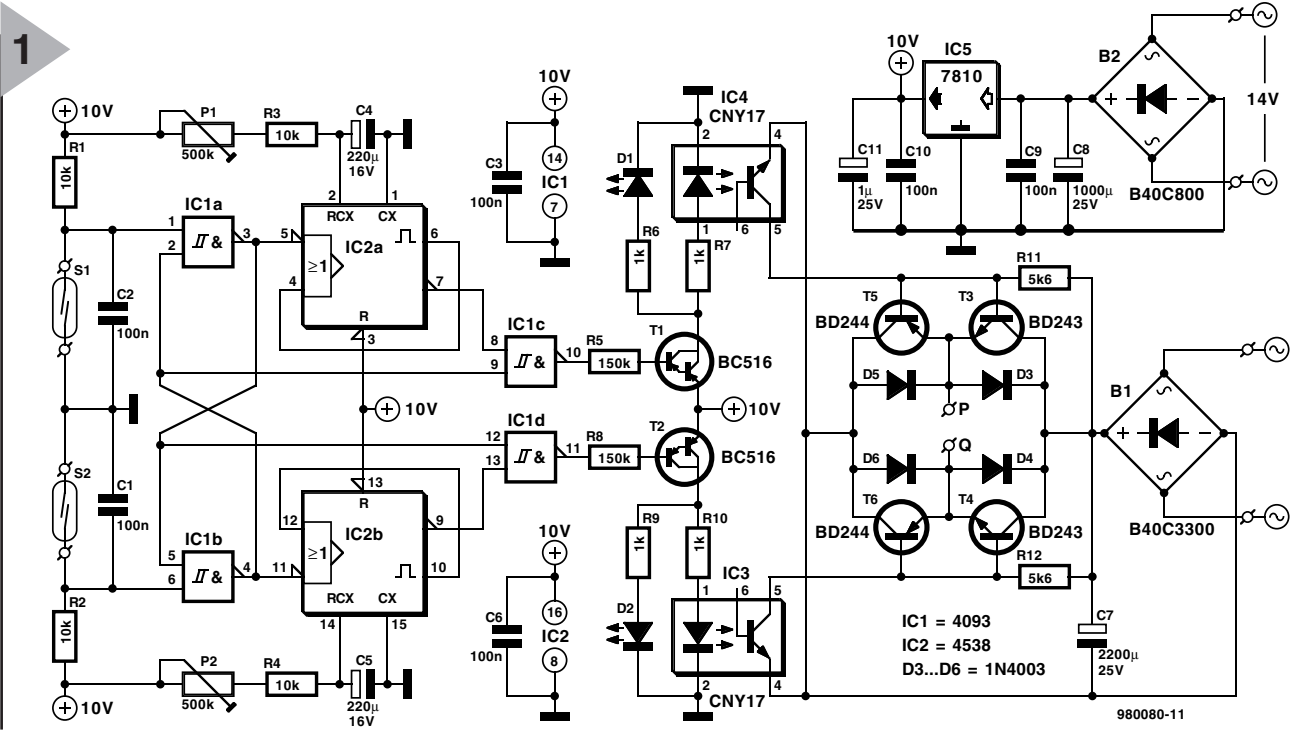


Figure 1. Circuit diagram of the shuttle track control. The direction of travel is reversed by power transistors T₃-T₆. The time the train remains at station A or B is set with P₁ and P₂ respectively.

CIRCUIT DESCRIPTION

To understand the function of the shuttle service circuit, imagine a train travelling from A to B. The train can move only when neither of timers IC_{2a} and IC_{2b} is set (see Figure 1). This is always so when the train is at a standstill at station A or B. Pin 3 of the bistable (flip-flop) formed by IC_{1a} and IC_{1b} is then logic low (0), whereas pin 4 is logic high (1). Pins 6 and 10 of IC₂ are also low, while pins 7 and 9 of IC₂ are high. The inputs of NAND gate IC₁ are high, but its output is low. This means that T₁ conducts whereupon the LED in optoisolator IC₄ lights. Power transistors T₄ and T₅ conduct and link the drive voltage to the rail track. The train is then able to leave station A and travel to station B.

When station B is approached, reed switch B closes when the locomotive passes over it. This causes bistable IC₁ to change state, whereupon pin 3 of IC₁ goes high, and pin 4, low. This results in the input (pin 11) of IC₂ being triggered, so that its normal output (pin 10) goes high at once and the inverted output (pin 9), low. The output of the NAND gate remains high, however, for as long as the timer is set. During this time, darlingtonts T₂ and T₂, as well as the power circuit, T₃-T₆, remain cut off so that the train cannot leave station B.

When the time set by IC_{2b} has elapsed, pin 9 of the timer goes high again, whereupon the inputs of NAND

gate IC_{1d} become high also, the output of the gate goes low, and T₂ conducts so that the LED in optoisolator IC₃ lights. Power transistors T₃ and T₆ then come on and connect the drive voltage with reverse polarity to the rail track. The train is then able to leave station B and travel to station A.

When station A is approached, reed switch A closes when the locomotive passes over it. This causes bistable IC₁ to change state again, whereupon a similar process as described for station B ensues. Now, however, timer IC_{2a}, which determines how long the train stops at station A, is triggered.

In this manner, the train travels continuously between the two stations (provided the power is switched on). Diodes D₁ and D₂ indicate which of the two optoisolators is enabled and therefore in which direction the train is travelling. When the train is at either of the two stations, both LEDs are out.

Because the inverse trigger inputs (pins 5 and 11) of IC₂ are used, timers IC_{1a} and IC_{1b} are triggered by the negative edges at pins 3 and 4 of IC₁. Since the timers change state after the set time has elapsed, even when the trigger inputs are low, operational errors are prevented. This is particularly important to avoid a fast moving locomotive closing the same reed switch twice in succession or a slow train stopping with the locomotive above the reed switch/relay and so keeping this closed.

The track voltage is derived from the normal railway power supply set as required for the track speed. The bridge rectifier, B₁, ensures that the supply to power transistors T₃-T₆ is of correct polarity at all times. Capacitor C₇ smooths the track voltage and short-circuits any spikes on it.

The supply voltage for the control circuit is derived from the normal railway lighting supply (14 V a.c.) via bridge rectifier B₂ and regulator IC₅.

CONSTRUCTION

The control circuit is best built on the printed-circuit board shown in Figure 2. Experienced constructors will have no problems in completing the board. Those with less experience should pay particular attention to the polarity of electrolytic capacitors, diodes, ICs, bridge rectifiers, and so on. Wire bridges also need close attention: make sure that these are soldered in place before any components are fitted.

Although, strictly speaking, power transistors T₃-T₆ do not need a heat sink during normal operation, it is wise to fit them on one to allow for any unforeseen events.

Circuit IC₁ should preferably be a Type 4093, which has high immunity to interference, but a Type 4011 (pin compatible with a 4093) may also be used.

When the power is switched on for the first time to the track and the con-

Parts list

Resistors:

R_1 – R_4 = 10 k Ω
 R_5 , R_8 = 150 k Ω
 R_6 , R_7 , R_9 , R_{10} = 1 k Ω
 R_{11} , R_{12} = 5.6 k Ω
 P_1 , P_2 = 500 k Ω preset

Capacitors:

C_1 – C_3 , C_6 , C_9 , C_{10} = 0.1 μ F
 C_4 , C_5 = 220 μ F, 16 V, radial
 C_7 = 2200 μ F, 25 V, radial
 C_8 = 1000 μ F, 2 V, radial
 C_{11} = 1 μ F, 25 V, radial

Semiconductors:

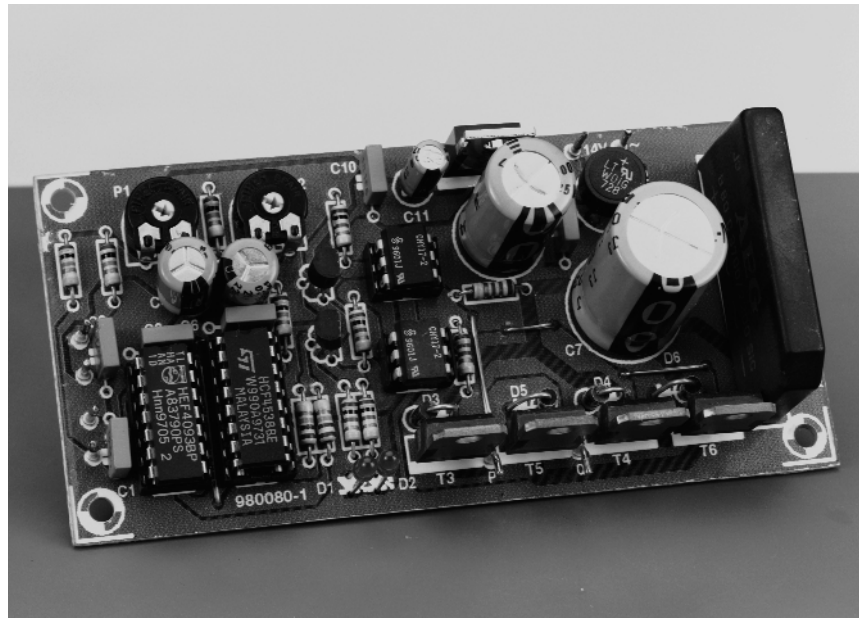
B_1 = B40C3000 bridge rectifier
 B_2 = B40C800 bridge rectifier
 D_1 , D_2 = LED, high efficiency
 D_3 – D_6 = 1N4003
 T_1 , T_2 = BC516
 T_3 , T_4 = BD243
 T_5 , T_6 = BD244

Integrated circuits:

IC_1 = 4093 or 4011 – see text
 IC_2 = 4538
 IC_3 , IC_4 = CNY17-2
 IC_5 = 7810

Miscellaneous:

S_1 , S_2 = reed switch or reed relay
 PC_1 – PC_{10} = solder pins
 PCB Order no. 980080 (see Readers services towards the end of this issue)



trol circuit, the timers are set by the negative edge at their inverse trigger inputs. Therefore, the train will not move until the relevant time has elapsed; at the first switch-on, this may take a little while.

If the train, on first switch-on, moves in the wrong direction and its passing over a reed switch has no effect, the polarity of the track voltage must be reversed.

Because the circuit is controlled via two reed switches or relays as opposed

to via an isolating track, small magnets may be fitted (glued) underneath the last carriage instead of the locomotive. This enables the train to be fairly long while retaining the same distance between the front or rear of the train and the terminals of the shuttle track.

[980080]

See also 'Shuttle Track' in the July/August 1996 issue of this magazine.

2

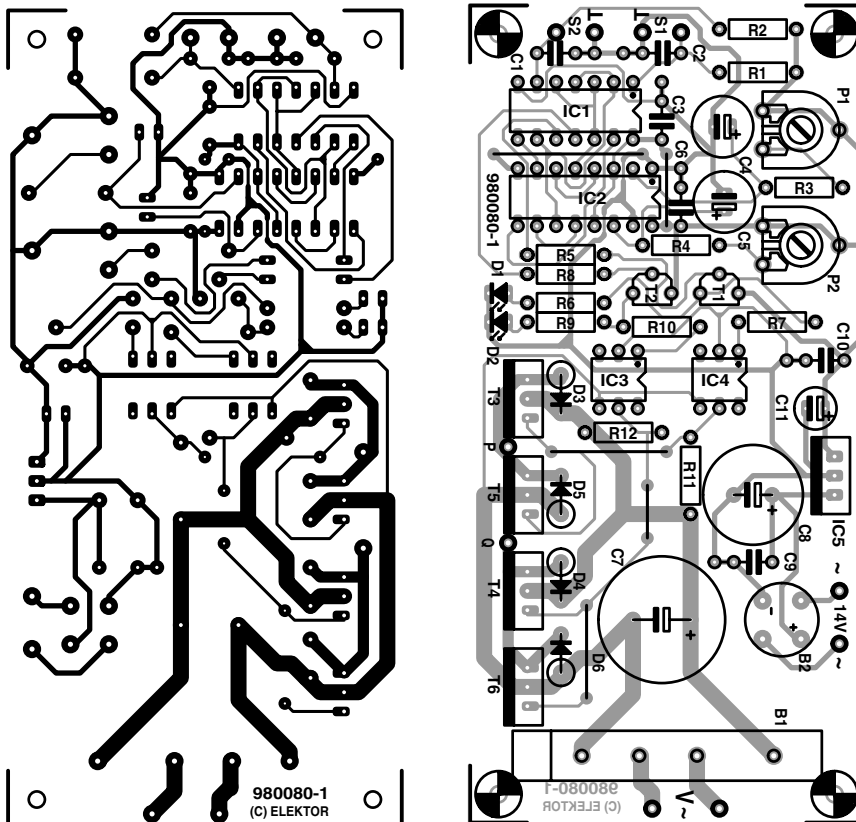


Figure 2. The printed-circuit board for the shuttle track control.

2SC5359

Transistors
AF, high-power

ELEKTOR ELECTRONICS

DATASHEET 2 / 9 9

2SC5359
Silicon NPN Triple Diffused Power Transistor

Manufacturer
Toshiba

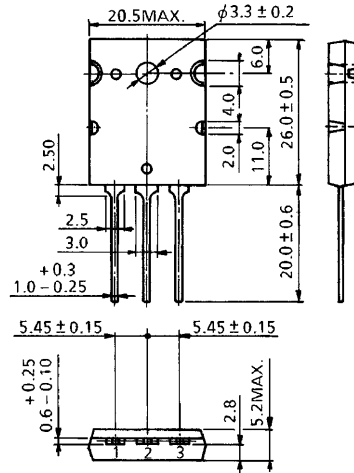
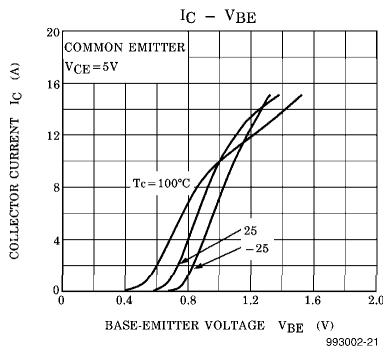
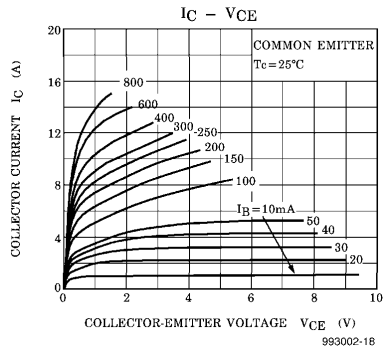
Features

- High Collector Voltage: $V_{CEO} = 230V$ (Min.)
- Complementary to 2SA1987
- Recommended for 100W High Fidelity Audio Frequency Amplifier Output Stage

Application Example

High-Power AF Amplifier,
Elektor Electronics February & March 1999.

MAXIMUM RATINGS (Ta = 25°C)			
CHARACTERISTIC	SYMBOL	RATING	UNIT
Collector-Base Voltage	V_{CBO}	230	V
Collector-Emitter Voltage	V_{CEO}	230	V
Emitter-Base Voltage	V_{EBO}	5	V
Collector Current	I_C	15	A
Base Current	I_B	1.5	A
Collector Power Dissipation (Tc = 25°C)	P_C	180	W
Junction Temperature	T_j	150	°C
Storage Temperature Range	T_{stg}	-55 to + 150	°C



1. BASE
2. COLLECTOR (HEAT SINK)
3. EMITTER

993002-17

2SA1987

Transistors
AF, high-power

ELEKTOR ELECTRONICS

DATASHEET 2 / 9 9

2SA1987
Silicon PNP Triple Diffused Power Transistor

Manufacturer
Toshiba

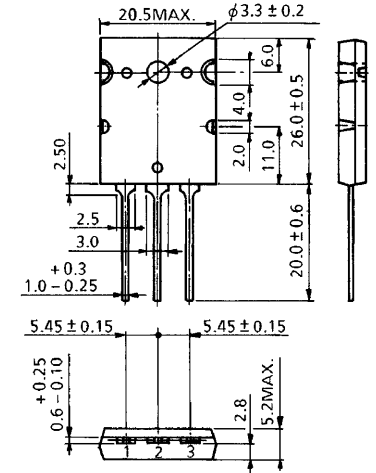
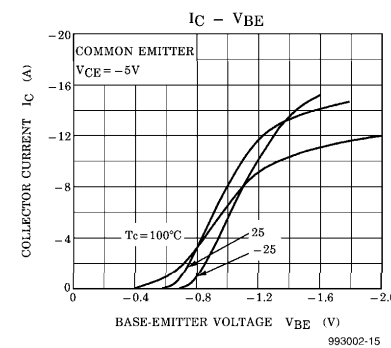
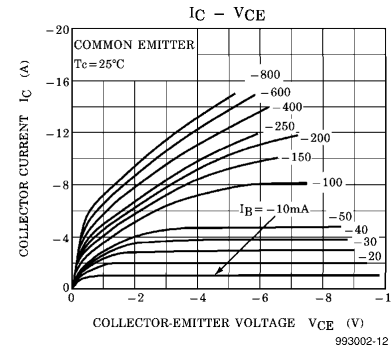
Features

- High Collector Voltage: $V_{CEO} = -230V$ (Min.)
- Complementary to 2SC5359
- Recommended for 100W High Fidelity Audio Frequency Amplifier Output Stage

Application Example

High-Power AF Amplifier,
Elektor Electronics February & March 1999.

MAXIMUM RATINGS (Ta = 25°C)			
CHARACTERISTIC	SYMBOL	RATING	UNIT
Collector-Base Voltage	V_{CBO}	-230	V
Collector-Emitter Voltage	V_{CEO}	-230	V
Emitter-Base Voltage	V_{EBO}	-5	V
Collector Current	I_C	-15	A
Base Current	I_B	-1.5	A
Collector Power Dissipation (Tc = 25°C)	P_C	180	W
Junction Temperature	T_j	150	°C
Storage Temperature Range	T_{stg}	-55 to + 150	°C



1. BASE
2. COLLECTOR (HEAT SINK)
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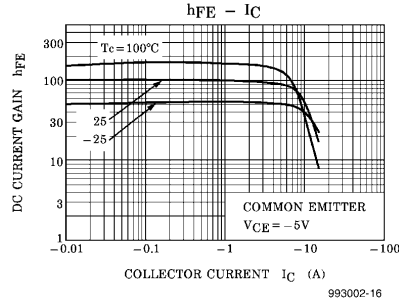
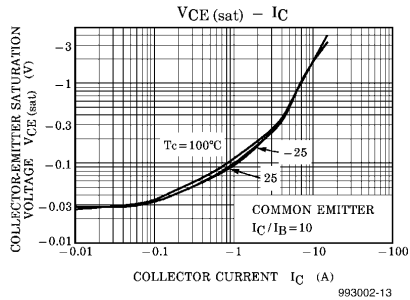
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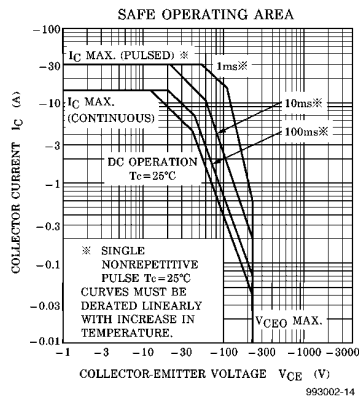
DATASHEET 2 / 9 9



ELECTRICAL CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Collector Cut-off Current	I_{CBO}	$V_{CB} = -230V, I_E = 0$	—	—	-5.0	μA
Emitter Cut-off Current	I_{EBO}	$V_{EB} = -5V, I_C = 0$	—	—	-5.0	μA
Collector-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = -50mA, I_B = 0$	-230	—	—	V
DC Current Gain	$h_{FE(1)}$ (Note)	$V_{CE} = -5V, I_C = -1A$	55	—	160	—
	$h_{FE(2)}$	$V_{CE} = -5V, I_C = -7A$	35	70	—	—
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = -8A, I_B = -0.8A$	—	-1.5	-3.0	V
Base-Emitter Voltage	V_{BE}	$V_{CE} = -5V, I_C = -7A$	—	-1.0	-1.5	V
Transition Frequency	f_T	$V_{CE} = -5V, I_C = -1A$	—	30	—	MHz
Collector Output Capacitance	C_{ob}	$V_{CB} = -10V, I_E = 0, f = 1MHz$	—	360	—	pF

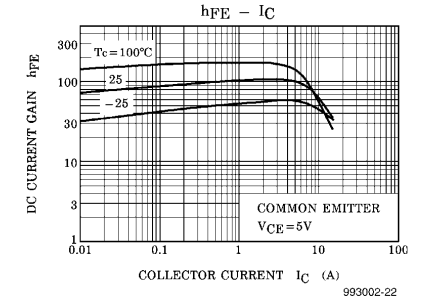
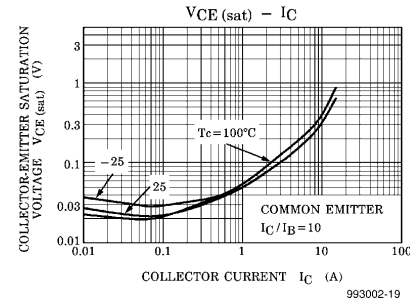
(Note) $h_{FE(1)}$ Classification: R= 55-110; O= 80-160



2SC5359

Transistors
AF, high-power

DATASHEET 2 / 9 9



ELECTRICAL CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Collector Cut-off Current	I_{CBO}	$V_{CB} = 230V, I_E = 0$	—	—	5.0	μA
Emitter Cut-off Current	I_{EBO}	$V_{EB} = 5V, I_C = 0$	—	—	5.0	μA
Collector-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 50mA, I_B = 0$	230	—	—	V
DC Current Gain	$h_{FE(1)}$ (Note)	$V_{CE} = 5V, I_C = 1A$	55	—	160	—
	$h_{FE(2)}$	$V_{CE} = 5V, I_C = 7A$	35	87	—	—
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = 8A, I_B = 0.8A$	—	0.4	3.0	V
Base-Emitter Voltage	V_{BE}	$V_{CE} = 5V, I_C = 7A$	—	1.0	1.5	V
Transition Frequency	f_T	$V_{CE} = 5V, I_C = 1A$	—	30	—	MHz
Collector Output Capacitance	C_{ob}	$V_{CB} = 10V, I_E = 0, f = 1MHz$	—	200	—	pF

(Note) $h_{FE(1)}$ Classification: R= 55-110; O= 80-160

