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PC Topics:

RS232 switch IRQ & DMA usage IR commands via PC

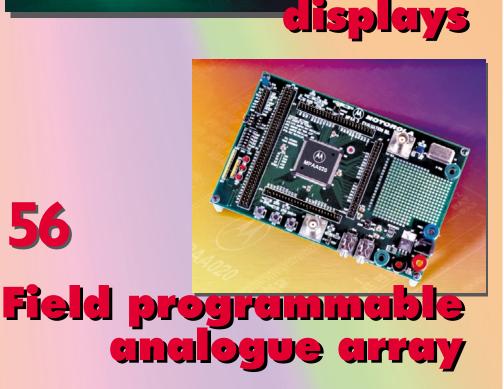
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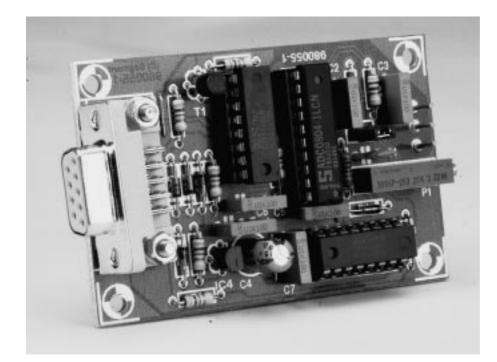
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Using this simple circuit, it is possible to measure analogue signals via the serial port of a PC. The chosen approach allows even a 'cast-off' PC to be used for measuring analogue quantities.

Design by J. F. Verrij

a simple A-D converter works with the serial port of any PC



| Technical data | |
|----------------------|-----------------|
| measurement range: | 0 to 5 V |
| resolution: | 8 bits |
| step size: | 20 mV |
| measurement error: | ±1 bit |
| conversion time: | 150 <i>µ</i> s |
| supply voltage: | 5 V |
| current consumption: | 5 mA |
| interface: | RS232 |
| software: QBASIC | C (for example) |

It is by no means always necessary to use a super-accurate, fast A-D converter to measure analogue signals. If reasonable resolution (such as 256 steps covering a range of 5 volts) and conversion speed are adequate for a given application, then there is no need to make things more difficult for ourselves than they need to be. The circuit presented here is a typical example of a simple, inexpensive design which is nonetheless quite useful. It has a resolution of 20 mV, is easily controlled by a BASIC program (for example), and does not make any extraordinary demands on the computer. In addition, it does not consume very much power (5 mA at 5 V), so that it can be powered directly from the serial interface. A separate power supply is thus not necessary. The accuracy is also satisfactory; the measurement error is limited to ± 1 bit, which represents ± 20 mV.

To the point

The A-D converter presented in this article shows that it is possible to build something nice using only a small number of components. An integrated A-D converter (National Semiconductor type ADC0804, a low-cost 'thoroughbred' which has been available for many years) and a few 4000-series buffers are basically all that is needed to allow analogue voltages to be measured via the serial port. The parallel-toserial conversion of the output data is implemented in the hardware in a simple manner by making clever use of the serial port's handshaking signals. The digital values are read in two steps via the port's control lines. This means that only a pair of inexpensive logic ICs are needed in addition to the A-D converter chip.

The schematic

Figure 1 depicts the schematic diagram of the circuit. The serial port signals are shown at the right-hand side of the figure, and the analogue input is at the left-hand side. A 5-V supply voltage is produced from the RS232 signals by means of three diodes, a capacitor and an integrated voltage regulator. The reference voltage for IC1 is derived from the supply voltage using a simple voltage divider (P1). The RC network consisting of R2 and C3 is added to filter out HF noise. The required supplydecoupling capacitors are also pro-



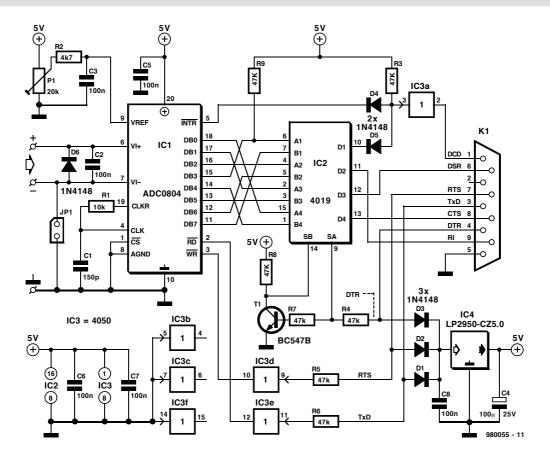


Figure 1. Schematic diagram of the simple A-D converter. The serial interface is used here as a sort of simple parallel port.

vided. For this approach to work, it is necessary that the software ensures that a high-level voltage (+ 12 V) is always present on the TxD, RTS or DTR line.

The built-in clock generator of the A-D converter uses an external RC timing network consisting of R1 and C1. With the chosen component values, the clock frequency is on the order of 400 kHz. The resulting conversion time is approximately 150 μ s.

The analogue signal which is to be measured is applied to the terminals marked 'PC1 (+) and PC2 (–). The circuit works by default with an asymmetric input, but this can be converted to a symmetric input by simply removing jumper JP1. The input voltage may range from –0.3 V to V_{CC} + 0.3 V Diode D6 prevents damage to the input of IC1 if the input voltage is connected with the wrong polarity, and C2 effectively suppresses HF noise.

The remainder of the circuit consists of the interface logic. As already noted, the result of the conversion is read out in two steps. The eight-bit conversion code is made up of two nibbles. Data0-Data3 are contained in the first nibble, and Data $4 \lor Data7$ in the second nibble. The unusual feature of this design is that the individual bits are read in via the CTS, DSR, RI and DCD lines, which

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2

are four control lines of the RS232 port. In this way, the serial port is adapted to act as a sort of parallel port. In addition, the /WR and /RD lines of the

A-D converter, and the selection lines SA and SB of the multiplexer IC, are also

controlled via the serial port. Transistor T1 forms a discrete inverter, which makes either SA or SB active depending on the level present on the DTR line. RTS and TxD are used to control /WR and /RD respectively.

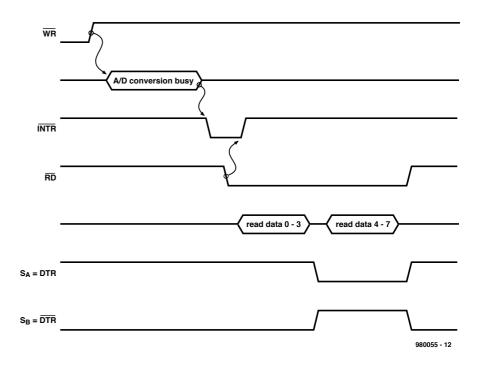


Figure 2. The timing diagram shows the relationships of the various control and data signals.

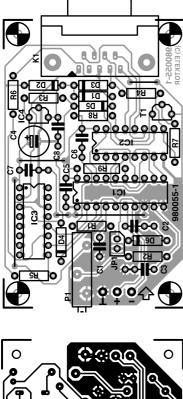


Figure 3. The copper layout and component layout of the printed circuit board for this project. Unfortunately, this board is not available ready-made from the Publishers.

Diodes D4 and D5, together with R3, form an ORgate. The data outputs of IC1 are undefined during the conversion process. Since the A1 input of IC2 is constantly held at a defined level by resistor R9, the D1 output of IC2 will be logic high during the conversion process, assuming that SA is active. The level on the DCD line is thus the same as the level on the /INTR output of the ADC0804. The conversion process is started by pulling the /WR input of the A-D converter logic high. The rising edge of the signal applied to the /WR input initiates the conversion, which takes approximately 150 μ s to com-

COMPONENTS LIST

Resistors: R1 = $10k\Omega$ R2 = $4k\Omega7$ R3-R9 = $47k\Omega$ P1 = $20k\Omega$ multiturn preset

Capacitors: C1 = 150pF C2,C3,C5-C8 = 100nF Semiconductors: D1-D6 = 1N4148 T1 = BC547B IC1 = ADC0804LJN IC2 = 4019 IC3 = 4050 IC4 = LP2950-CZ5.0

Miscellaneous: JP1 = jumper K1 = 9-way sub-D socket (female), PCB mount

plete. As soon as the DCD line goes low, the computer knows that the conversion has been completed. A read command must then be issued (by making /RD low), which causes the A-D converter to place the result of the con-

```
COMadres = &H3F8
LCOP1:
'First switch on power supply by making DTR and TxD high
'read (TxD) not active, write (RTS) active
OUT COMadres + 4, INP(COMadres + 4) OR 1 'DTR=SA=H, SB=L
OUT COMadres + 4, INP(COMadres + 4) AND & HFD 'RTS=WRnot=L
OUT COMadres + 3, INP(COMadres + 3) OR 64 'TxD=RDnot=H
'Wait 50 ms until circuit is stable before starting a conversion
Start = TIMER
DO
TIME = TIMER
LOOP UNTIL TIME >= Start + .05
'Start conversion by making Write not active
OUT COMadres + 4, INP(COMadres + 4) OR 2 'RTS=WPnot=H
'Wait for interrupt (DCD), signalling end of conversion
DO
intr = INP(COWadres + 6) AND 128
LOOP UNTIL intr = 0 'wait until DCD=L
'Reset interrupt by making read active
OUT COMadres + 3, INP(COMadres + 3) AND 0 'TxD=RDnot=L
'Now the result can be read in 2 nibbles
READDATAL:
Datalow = (INP(COWadres + 6)) AND 240 'read low nibble
'Switch multiplexer input
OUT COMadres + 4, I NP(COMadres + 4) AND & HFE 'DTR=SA=L, SB=H
READDATAH:
Datahigh = (INP(COMadres + 6)) AND 240 'read high nibble
'Optimize power supply and return circuit to standby
'by making DTR and TxD high
OUT COMadres + 3, INP(COMadres + 3) OR 64 'TxD=RDnot=H
OUT COMadres + 4, INP(COMadres + 4) OR 1 'DTR=SA=H, SB=L
'Now the two nibbles are combined into the original byte
DATAHL = Datahigh + Datalow / 16
'Convert the result to the measured input voltage
Range = 4.998
Voltage = Range * DATAHL / 255
'Rounding the result to 3 digits
Voltage = INT(Voltage * 1000 + .5) / 1000
'Display the result
PRINT counter; "Voltage="; Voltage; "Volt"
Counter = Counter + 1
GOTO LOOP1:
FND
```

Figure 4. This QBASC program listing shows how easily the converter circuit can be controlled.



version on its outputs (DB0-DB7). In addition, the /INTR output is also automatically set logic high again. In case this all sounds a bit complicated, have a look at **Figure 2**, which clarifies the whole process in the form of a timing diagram.

Before you ask: yes, it's true that buffers IC3d and IC3e are driven directly by RS232 signal levels (±12 V), even though they are specified to handle signals which switch between 0 V and + 12 V, and then only if the supply voltage is also 12 V. This is possible (and the circuit works under these conditions) because the internal input protection diodes are utilized, in combination with the 47 k Ω current-limiting resistors, to convert excessive input voltages into small currents which are diverted via the protection diodes. Under normal conditions the internal protection networks can safely handle currents of up to 10 mA, which is much more than the currents encountered in this circuit.

A small circuit board

Figure 3 shows the layout of the printed circuit board for the converter. Mount the four wire jumpers first. Although

sockets can be used for the ICs, experienced constructors will prefer to solder them directly to the board. Naturally, the remaining components are soldered directly to the board. Take care that the electrolytic capacitor (C4) and the diodes are installed with the correct polarization.

The analogue input uses three circuitboard pins. If only the asymmetric input is used (which is recommended), then the pin marked '–' can be omitted. Of course, jumper JP1 must then be installed.

The connection to the PC is made via a D9 connector. To avoid placing too much mechanical stress on the solder joints when attaching or removing the connector, it must be fastened to the circuit board using two screws. Firmly fasten the connector to the board with the screws before soldering its 9 pins to the board, since otherwise the solder joints will probably be subjected to excessive strains.

On the software side

No matter how clever the hardware may be, there's not much that can be done with it without software. We thus need some software as well with this project. Fortunately, the circuit can be controlled using a relatively small number of BASIC instructions, so that it can be easily integrated into your own particular applications.

Figure 4 presents a listing of a sample QBASIC program for controlling the converter circuit. Between the comments and the descriptions of the register functions of the serial port, you should have no difficulty understanding how to use the program and the converter. Specific descriptions of the register structure of the 8250 IC can be found in the *DataSheets* section of this issue (an 8250 or compatible controller is the standard device used in a PC for the serial port).

Calibrating the circuit is easy: connect a known voltage source to its input (such as a fresh button cell) and start the control software, so that the measured value is calculated and displayed. Now adjust P1 until the measured value agrees as closely as possible (± 20 mV) with the actual input voltage.

(980055-1)

PC software competition

circuit design
 communications

As in the past two years, this magazine will publish a design competition in the July/August issue (on sale 18 June), for which a number of advertiser sponsors have made available some glittering prizes.

Since more and more readers are interested and/or engaged not only in electronics, but also in computers (although this is just a branch of electronics), this year's competition will link the two as the subtitle suggests: the design of PC software for use in test and measurement, circuit design, or communications

The aim of the competition should be seen in its broadest sense. Competitors may well devise a program to test or measure a physi-

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PC

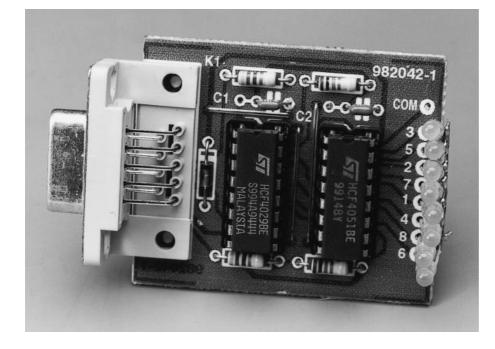
cal quantity with the aid of a PC, but which also needs some additional hardware. Others may create software for testing logic circuits, or a small circuit design system that is driven by a PC, or a program to decode the output of weather reporting stations. The main thing is that the PC plays an active role in the design.

Full details of the competition and the prizes will be published in next month's issue of this magazine. Don't miss it! [980060] The circuit presented in this article enables you to build a software-controlled 8-channel analogue switching unit that will be hard to beat as far as simplicity is concerned. The software for controlling the switch is written in Visual BASIC, and available on disk.

Hardware design and software by B. Oehlerking

RS232-controlled 8-channel switch

Using CMOS logic and Visual Basic



Using a PC to control 'real-world' loads like lamps, relays and so on is an everpopular subject, and various designs of PC-controlled switching units have appeared in this magazine over the past few years. However, many at you may have hesitations about building such complex circuits, which, in the worst case, are insertion cards. Unless you are into industrial control systems and have lots of PCs to play around with, it is best to opt for a switching system which is connected to the PC as an external unit, and controlled by way of one of the PC's ports (FS232 or parallel).

The good news is that the present design is cheap, open to experiments, totally external, RS232-driven, and it does not even require a power supply! What's more, we have available the software to control the switch in a userfriendly-way using an attractive userinterface which appears on the screen.

The hardware

Pemarkably, there are only two integrated circuits in this design, as evidenced by the circuit diagram shown in **Figure 1**. What's more, the 4029 and 4051 ICs are traditional CMOS devices which anyone should be able to obtain at a very small outlay.

The circuit is powered by the + 10 V voltage tapped from the PC's RS232 port via the DTR (data terminal ready) line. Because the DTR line can also drop down to -10V, a diode, D1, is inserted in the supply line to the circuit to protect it against the harmful nega-

tive voltage.

The type 4029 counter is automatically reset at power-on by C3-P5. The counter operates in BCD (binary coded decimal) mode, and responds to rising pulse edges at its clock input, pin 15. This pulse transition is supplied to the circuit by the PC sending the word '0' (0000 0000 binary) over the TxD (transmitted data) line. Potential divider R1-R4 and the internal clamping diodes protect the clock input of the 4029 against harmful voltage levels.

Binary outputs Q1, Q2 and Q3 (pins 6, 11 and 14) of the 4029 are connected to the corresponding inputs of a type 4051 bilateral 8-way analogue multiplexer, IC2. Depending on the channel selection code received at its control inputs, the 4051 switches the voltage at pin 3 (COM) to one of the eight outputs marked 0 through 7. In this way, the 4051 acts as a digitally controlled rotary switch. A 'high' (+ 10 V) voltage level on the RTS line disables the 4051 via pin 6, causing all channels to be disconnected simultaneously. Here, again, a resistordiode combination is used to ward off the risk of negative voltages on the RTS line damaging the 4051.

The 4051 is by no means a 'power switch', and capable of switching currents up to about 1 mA only, while the voltage level should be between 0 V and 9 V. If you want the circuit to control much heavier loads, say, a relay or a lamp, then we suggest adding a BUZ10 MOSFET current booster as shown in **Figure 2**. Note that the + 10 V control voltage arriving by way of the 4051 is again 'stolen' from the DTR line, and that the load (obviously!) has to be powered by an external supply

TOPICS

capable of providing the necessary current.

The carry bit supplied by pin 7 of the 4029 counter is read by the PC via the CTS (clear to send) line, for reasons we will discuss further on.

That more or less wraps up the discussion of the hardware. The circuit is connected to a free COM port on the PC via a 9-way sub-D PCB-style socket, K1, and a standard serial interface cable.

Construction

The 8-channel switch is built on a small printed-circuit board of which the artwork (copper track layout and component mounting plan) is shown in Figure 3. This board is unfortunately not available ready-made from the Publishers.

Construction should not cause undue difficulty even to (relative) beginners to the noble art of soldering. It is recommended to use IC sockets for the 4029 and the 4051. Watch their polarity and also that of the diode!

Control software

The program for controlling the switch was written in Visual BASIC 3.0. Its flowchart is shown in Figure 4. First all channels are switched off by pulling

COMPONENTS LIST Resistors: $R1,R2 = 10k\Omega$ $R5 = 100 k\Omega$ Capacitors: C1.C2.C3 = 100nF

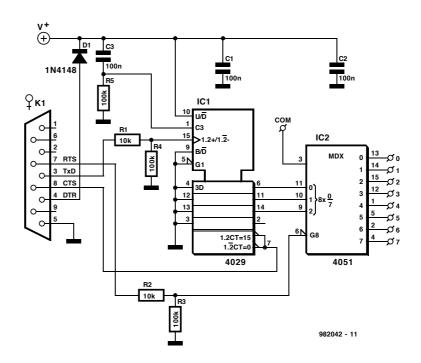
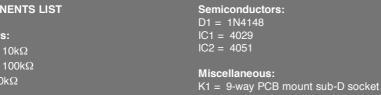


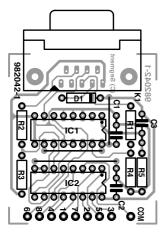
Figure 1. Circuit diagram of the RS-232 controlled 8-way switching unit.

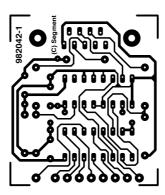
RTS high. Next, the value '0' is repeatedly written (via TxD) until CTS drops low. Next, the user can click on the 'Switch' button in the user interface box to step through the channels. Each mouse click causes a further '0', that is, a clock pulse, to be sent to the 4029, which is incremented in this way. Once channel 7 is reached, the next



(female), angled pins. Control software on disk, order code 986015-1, see Readers Services page

Figure 3. Copper track layout and component mounting plan of the PCB designed for the switching unit (board not available ready-made).





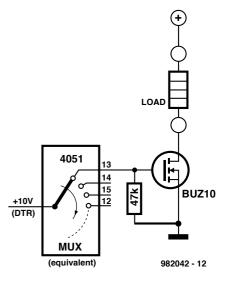


Figure 2. Optional power driver extension (up to eight required) to enable 'real' loads to be controlled.

mouse click causes the program to send the number of pulses needed to make Q1=Q2=Q3=0 again, i.e., channel 0 is selected again (assuming that all channels have been disabled using the button 'On/Off Ch's', i.e., RTS).

The user interface will tell you which channel has been selected, as well as the status of the supply voltage applied to the circuit (DTR on/off), and the status of the 'channel disable/enable' control (On/Off Ch's). Pressing the 'Auto' button causes the program to automatically step through all eight channels at the indicated interval (here, 1 s). The available range of the auto-step interval is approximately 0.1 s to 1 s. The complete executable program and its project code file (written in Visual BASC 3.0) are available from the Publishers on a floppy disk with

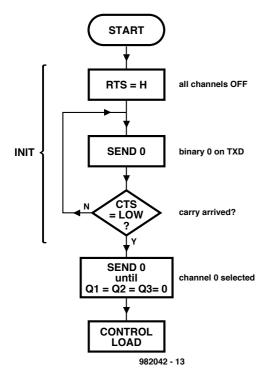


Figure 4. Flowchart of the VB3 program developed for the project.



Figure 5. The user interface is a window with buttons offering full control over the eight switched devices, as well as useful status information indicators.

order code **986015-1**. No need to mention that VB fans among you may edit and enhance the program to their hearts content.

Applications

As already mentioned, the switch is suitable for control-

ling (dc-operated) loads if you extend it with the power buffers shown in Figure 2. However, the 4051 containing bilateral analogue switches, it also is possible to use the circuit to collect, say, analogue voltages from eight sources, and feed these, one at a time, to an ADC (analogue/digital converter) via pin 3 of the 4051.

(982042-1)



8 - 6/98 Eektor Eectronics EXTRA

The IRQ and DMA lines are used to manage communications between the computer and all other components, extension cards and peripheral devices. It is important that these lines are correctly allocated and applied, since otherwise the PC will not work properly with the various devices which are connected to it. In this article we explain the functions of these lines and the possibilities which modem PCs offer for resolving possible problems and conflicts relating to their use.

By our editorial staff

IRQ and DMA usage right-of-way rules for the PC

The computer's processor must perform a large variety of tasks. It must execute programs, look after memory management, maintain communications with various system components (ranging from the real-time clock IC to the hard-disk drive) and much more. Good communications between the various elements of the system, and a certain amount of hierarchical structure, are needed for this to all work smoothly and efficiently. The interrupt lines and DMA channels of the PC were developed to aid in this process. Every device which is either located inside the computer or connected to the computer (such as a joystick port or a sound card) first has one or more I/O (Input/Output) addresses assigned to it for transferring data between the processor and the device. A special I/O address region is set aside for this purpose. In addition, there are two additional types of signal lines present to support fast interactions between a system component and the CPU or between two system components: IRQ and DMA.

IRQ

IRQ stands for 'Interrupt Request'. A system component sends such a request to the CPU to indicate that the processor must temporarily suspend its current activities and communicate as quickly as possible with the component in question. After this communication is completed, the CPU continues with whatever it was doing at the time that it received the interrupt request.

The interrupts are all handled by an interrupt-controller IC. The original XT machines had 8 interrupt lines, while in later models two controllers are arranged in series to provide a total of 15 available IRQ lines.

Unfortunately, several IRQs are claimed by internal components such as the timer IC, the keyboard driver and the coprocessor, so that relatively few free IRQs are left for use with ISA and PCI expansion cards. **Table 1** summarizes the available IRQs and the devices to which they are assigned.

PC users are frequently confused by lines 2 and 9. IRQ9 from the second IC actually replaces IRQ2 from the first IC, so that both of these lines have the same function. In certain cases, problems can occur with a component using IRQ2 or IRQ9. As a rule, the software will recognize one of these IRQ lines but not both of them. If the component in question does not work properly with IRQ2, try it with IRQ9 (or vice versa). One of these two settings will usually work okay.

The order of precedence (or priority) of the IRQ lines is also clearly defined. In principle it runs from low to high (IRQ0 thus takes precedence over IRQ1), but in practice the fact that two interrupt controller ICs are connected together causes certain deviations from this rule, as indicated in Table 1.

Not all of the IRQ lines are available for expansion cards. Some are only present on the motherboard, and the higher-numbered lines are only available with 16-bit ISA slots (which is of course not a problem with relatively modern computers). All available IRQ lines are present on the PCI connectors.

As can be seen from Table 1, there is not all that much room for expansion. IRQ5, 9, 10, 11 and 12 are the only free interrupt lines. When you consider that a sound card often takes two IRQs and that a graphics card also demands an interrupt line, you can see that there is very little left over. We will return to this subject later on.

DMA

DMA (Direct Memory Access) is a radical technique which allows one system component lay claim to other system components. In contrast to IRQ, in which a component signals the CPU that it must give its attention that component, with DMA a component can exchange data directly with another component without the intervention of the CPU. The CPU can thus continue to perform its own regular tasks. In order to properly manage the DMA traffic, a special DMA controller IC is provided to execute the necessary tasks. Using



DMA, a sound card can for example write digitized audio signals directly to the memory, with the aid of the DMA controller. In this case the DMA controller temporarily takes over the entire system bus, coordinates the desired data transfer and then releases the system bus.

There are several DMA channels that can be assigned to specific system components. Originally (with the XT) there were only four DMA channels; this was extended to 8 with the AT. As with the IRQ lines, certain DMA channels are normally allocated to certain system components. Fortunately, DMA channels are only needed for devices that must transfer a large amount of data in a short time, and there are not that many. There is thus less demand for DMA lines than for IRQ lines. The higher-numbered channels, as with the IRQ lines, are not available with 8-bit ISA slots.

Solving problems

If two components in the PC use the same IRQ or DMA line, a conflict situation is produced which can have serious consequences for the stability of the system. There are several ways to see which components use which IRQ and DMA lines. Under Windows 95 you can simply have a look at the system configuration under 'Settings - Control Panel - System - Device Manager - Properties'. If you are still using Windows 3.1 or DOS, you can use the program MSD (which is normally provided along with Windows or DOS).

Figure 1 illustrates a situation in which the computer is pretty well filled with expansion cards. Based on this example, let's have a look at the possible problems and their solutions.

Serial ports

A modern PC normally has two RS232 connectors which use IRQ4 (COM1) and IRQ3 (COM2). COM1 is usually reserved for the mouse. If a modem is added, it can always be connected to COM2. An internal modem can be configured to be COM3 or COM4. You should choose COM4, since COM3 shares an interrupt line with COM1 and COM2 shares an interrupt line with COM4; COM1 and COM3 can thus not be used at the same time. If you want to also connect a drawing tablet or an IR remote control, then it is a good idea to use the special PS/2 connector for the mouse (this connector is found on the motherboard of most Pentium PCs) but first make sure that the mouse can be used with a PS/2 interface! IRQ12 is normally reserved for a PS/2 mouse. If you do not use the PS/2 bus, then the IRQ assignment can usually be dis-

PC TOPICS ---

Computer Properties ? X View Resources | Reserve Resources | Interrupt request (IRQ) Direct memory access (DMA) O Input/output (I/O) O Memory Setting Hardware using the setting 💻 00 System timer 8801 Standard 101/102-Key or Microsoft Natural Keyboard 🔍 02 Programmable interrupt controller <u>)</u> 03 Communications Port (COM4) Communications Port (COM2) 904 Communications Port (COM1) **14** 05 Creative AWE64 16-bit Audio (SB16 compatible) **a** 06 Standard Floppy Disk Controller **9**07 ECP Printer Port (LPT1) 🔍 08 System CMOS/real time clock 10 Hauppauge WinCast/TV 🔍 10 IRQ Holder for PCI Steering 911 Matrox MGA Mystique PowerDesk **I** 11 IRQ Holder for PCI Steering . 12 Cordless4 (PS/2) 🛄 13. Numeric data processor ₿14 Intel 82371SB PCI Bus Master IDE Controller 📾 14. Primary IDE controller (dual fifo) 🖶 15 Intel 82371SB PCI Bus Master IDE Controller 🗃 15 Secondary IDE controller (dual fifo) ٠

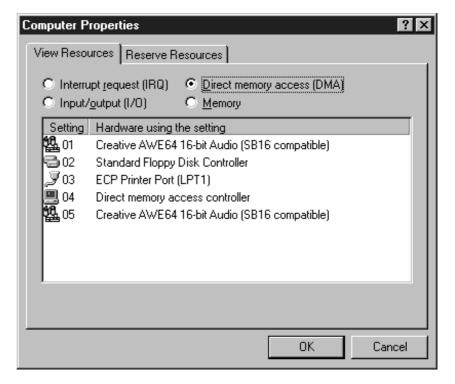


Figure 1. An example of IRQ and DMA utilization in a Windows-95 PC.

ΠK.

Cancel

Table 1. The PC's IRQ lines, showing the order of priority and the devices having fixed assignments.

| IRQ | Priority | Location | I/O addresses | Device |
|-----|----------|-----------------|--------------------|------------------------------|
| 0 | 0 | motherboard | 040 - 043 | system timer |
| 1 | 1 | motherboard | 060 - 064 | keyboard |
| 2 | 2 | motherboard | | diverted to IRQ 10 - 15 |
| 3 | 9 | 8-bit ISA slot | 2F8 - 2FF/2E8 - 2E | = serial ports COM2 and COM4 |
| 4 | 10 | 8-bit ISA slot | 3F8 - 3FF/3E8 - 3E | serial ports COM1 and COM3 |
| 5 | 11 | 8-bit ISA slot | (278 - 27F) | free (printer port LPT2) |
| 6 | 12 | 8-bit ISA slot | 3F0 - 3F7 | floppy-disk controller |
| 7 | 13 | 8-bit ISA slot | 378 - 37F | printer port LPT1 |
| 8 | 14 | motherboard | 070 - 07F | real-time clock |
| 9 | 2 | 8-bit ISA slot | | replacement for IRQ2 |
| 10 | 3 | 16-bit ISA slot | | free |
| 11 | 4 | 16-bit ISA slot | | free |
| 12 | 5 | 16-bit ISA slot | | free (PS/2-bus mouse) |
| 13 | 6 | motherboard | 0F0 - 0FF | coprocessor |
| 14 | 7 | 16-bit ISA slot | 1F0 - 1F7 | first IDE controller |
| 15 | 8 | 16-bit ISA slot | (170 - 177) | free (second IDE controller) |

(priority: 0 = highest, 14 = lowest)

Table 2. The PC's DMA channels, showing the standard assignments.

| DMA | location | device |
|-----|-----------------|--|
| 0 | 16-bit ISA slot | free |
| 1 | 8-bit ISA slot | free (sound card) |
| 2 | 8-bit ISA slot | floppy-disk controller |
| 3 | 8-bit ISA slot | free (ECP printer port or sound card) |
| 4 | motherboard | link between first and second DMA controller |
| 5 | 16-bit ISA slot | free (sound card) |
| 6 | 16-bit ISA slot | free |
| 7 | 16-bit ISA slot | free |
| | | |

abled by a jumper on the motherboard. However, Windows often has problems with releasing IRQ12 for general use, so don't just take it for granted that you can use it for some other application.

Printer port

The parallel printer port normally uses one interrupt line (usually IRQ7). This applies to the standard EPP printer port. If you select an ECP port in the BIOS setup, then a DMA channel is also used (channel 3). If you add a second printer port, it usually uses IRQ5.

Graphics card

Actually, a basic graphics card does not need an interrupt line or a DMA channel. However, modern cards with their extended functions normally do demand an interrupt line. Older-model cards which use an S3 chip are notorious for insisting on using IRQ11, which in many cases leads to annoying conflicts. Modern graphics cards are generally more flexible and can choose from several different interrupt lines (this happens when the computer is booted up). The graphics card usually uses one of IRQ9, 10 or 11.

Sound card

Sound cards are frequently a source of conflicts, since they use a relatively large number of interrupts and DMA channels. traditional The 8-bit SoundBlaster card normally used IRQ5 and DMA0 or DMA1, under the assumption that the second printer port either would not always be used or was not present (a single IRQ line can be assigned to two different devices as long as they are not both used at the same time). The modern-day 16-bit Soundblaster (as well as higher-performance models, such as the AWE64) still uses only one interrupt, but it needs two DMA channels (such as 1 and 5) since it must transfer 16-bit data. Other types of sound cards almost always need two IRQ lines in addition to the two DMA channels.

Network adapters and SCSI cards

Since these types of cards must process a lot of data, they normally use

one interrupt line (chosen from 9, 10, 11 and 12, for example) and one DMA channel (usually a 16-bit channel).

Special cards

If you connect some kind of special device to your computer, it usually comes with a separate plug-in card which also requires an interrupt line. There are also certain cards which only need an I/O address and which handle all communications with the processor via polling. This is somewhat slower, but it can work quite well.

Modern TV-tuner cards write their data directly to the memory of the graphics card via the PCI bus. They need both an interrupt line and a DMA channel to make this possible.

You can see that once a few expansion cards are installed in the computer, the competition for the available interrupt lines becomes rather fierce. Fortunately, we do not have to resolve this all by ourselves. With a modern motherboard and modern plug-in cards, the card themselves check to see which interrupt lines are available when the computer is switched on, and they can each choose from three or four possibilities. With older-model ISA cards this is not possible, which means that they must be configured manually. An additional feature of PCI cards is that they allow interrupt lines to be shared. Two cards can share a single interrupt line, as long as the software is smart enough to be able to recognize which card has generated the interrupt.

BIOS settings

The peripheral devices integrated on the motherboard use interrupt lines and DMA channels which can be configured via the BIOS. It is possible to choose among several I/O addresses and (sometimes) several IRQ lines for the COM ports. This is a handy way to exchange COM numbers; you can (for example) assign COM4 to an internal modem even though it is physically configured as COM3. The printer port(s) can also be set up in the same manner: it is thus possible to select one of two DMA channels and one of two or three IRQ lines in the ECP mode. If the second IDE controller on the motherboard is not used, you can disable it in the BIOS, so that IRQ15 can be made available for some other application.

- **PC**

(982051-1)

TOPICS



This article covers two projects. The first demonstrates how to use a PC to decode RC5-style infrared remote control signals, while the second project concentrates on using a remote control unit to transmit PC keyboard commands.

With contributions by E Saccasijn and KH.A. Duesman

projects for PC & infrared remote-control

The two projects described in this article were awarded Dutch national prizes in the 1996/1997 International Software competition, and have in common that they cover the use of infrared (IR) remote controls in combination with a personal computer (PC) of the IBM/DOS type.

Infrared remote controls for TV sets, CD players and VCPs often go by the dozen in electronic surplus stores, but they are also seen at rallies and flea markets. The type of control to use for the present projects should be **RC5 compatible**, which usually means that it has a Philips, Mullard or Aristona logo. Some Sony types are also suitable, but it is difficult to say exactly which ones as there are some many around.

RC5 remote control analyser/decoder

General

This program, written by Mr. Eric Saccasijn of Belgium, enables a PC to analyse any infrared command emitted by an RC5 (compatible) remote control unit. A simple IR receiver/demodulator is used to feed received pulse trains to BUSY line on the PC's printer port.

Next, the software takes over. Initially, a reference measurement is performed to determine the average bit length of the received pulses. This measurement is necessary to prevent different results on computers operating at different speeds. Based on the reference data, the commands may then be analysed. The signal analysis and decoder program, **RECO.COM**, displays blocks of eight received bytes on the screen, together with the system and function codes. These bytes are used by the second program, **RC5.COM**, which actually uses the RC5 function codes for software-controlled actions. The program to do so you have to write yourself.

RC5 pulse structure

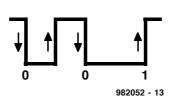


Figure 1. RC5 IR remote control signals are bi-phase encoded.

The RC5 remote control system is based on the biphase modulation principle, whereby a falling (negativegoing) pulse edge represents a logic 0, and a rising (positive-going) pulse edge, a logic 1. In this system, no state change occurs when two identical bits are transmitted successively. Consequently, two different periods can be observed in an RC5 signal: a 'long' period as a result of two identical bits, and a 'short' period as a result of two different bits. The 'long' period is exactly two times as long as the 'short' period. The basic structure is illustrated in Figure 1.

A complete RC5 code word consists of 14 bits: first come two *start bits*, the

first is always a '1', the second, a '1' (standard command follows) or a '0' (command from extended set follows). Next comes the *control bit*, which changes only when commands are separated by pauses. In other words, this bit does not change when you hold a key depressed for some time. The control bit is followed by the 5-bit *system code* and then the 6-bit *function code*. An overview of system codes and function codes will be printed on the Datasheets in the September 1998 issue of *Elektor Electronics*.

In the PC, a software counter is used to establish minimum and maximum values of the 'short' and 'long' periods, taking into account the clock speed of the computer. In this way, the length of the start bit can be measured and used as a reference (see RECO.COM). Once the values are known, they can be used at any time (on the same computer) without the need for a new reference measurement.

Hardware

A simple interface is needed to make the signals emitted by an IR remote control suitable for processing by a PC. The interface shown in **Figure 2** consists of a Semens SH506-36 IR receiver/demodulator, three wires, a 10-k Ω pull-up resistor and a 25-pin sub-D connector for the link to the PC's printer port. The IC and the resistor may be fitted on a small piece of veroboard connected to the sub-D connector via a short length of screened stereo cable. A mini jack socket was installed on the sub-D connector to



enable the interface to be powered by a 5-volt mains adaptor.

RECO.COM

As already mentioned, the main function of PECO.COM is to establish a PCrelated reference for the length of the pulses received from the RC5 IR remote control. It also displays a block of eight bytes, which hold essential information for the decoder program, RC5.COM. Each command comprises its system code, function code and the value of the control bit.

After launching the program, you are prompted to press a key on the remote control. The received signal is used to determine the length of the start bit, on the assumption that a normal RC5 command is transmitted (i.e., not one from the 'extended set', so to begin with don't press any 'special function' buttons on the remote control). Using the measured values, four limits are computed; the minimum and maximum 'short' time, and the minimum and maximum 'long' time. The program employs these limits to decide whether or not a command is valid. The four extreme values are stored in buffers as well as displayed on the screen in the form of eight bytes (two per extreme value). You may want to make a note of the values for use later as a patch for RC5.COM.

After the reference measurement the program waits for a key press to enter a loop in which received commands are decoded, and their system and function codes displayed separately. You may quit the program by pressing the Escape key.

RC5.COM

PC

This MS-DOS program waits for an IR command received by way of the interface described above. Once a command is received, it returns the system to MS-DOS, having supplied the RC5 function code as a return code. Used in a batch file, RC5.COM enables a function selection to be set up with the aid of, for example, the ERRORLEVEL instruction.

This program can not work without the eight 'reference-info' bytes supplied by RECO.COM discussed above. These eight bytes have to be patched into RC5.COM at hex addresses 462 through 469.

RC5.COM may be launched with an RC5 system code appended as an argument. Although the program does decode all bits, it only returns the *function code* as a DOS 'errorlevel' code. By supplying the system code beforehand, you can 'selectively listen' to one

TOPICS

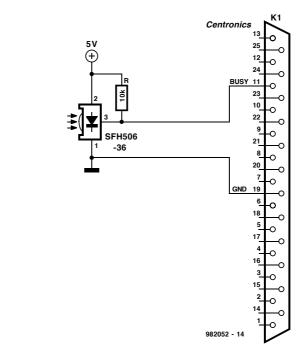


Figure 2. Circuit diagram of the simple IR receiver interface for use with the RECO and RC5 programs.

particular remote control. In that case, the program returns errorlevel code 128 if a wrong system code is received. If no argument is appended, then the system code is ignored, and the program returns the function code

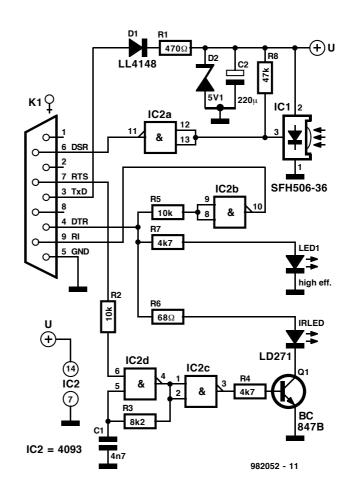


Figure 3. Circuit diagram of the transmit/receive interface for the PCPemote project. Note that this interface is connected to the PC's serial (RS232) port.

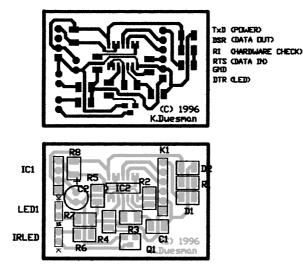


Figure 4. Copper track layout and component mounting plan for the PCRemote interface (shown at 200%).



Figure 5. Prototype of the PCRemote interface.

emitted by any RC5 remote control.

Two small batch programs are provided to get you going. **R.BAT** is an example of RC5.COM being launched without a system-code argument, while **R5.BAT** passes system-code '5' as a filter to RC5.COM, forcing the decoder software to return function codes from 'VCR1' remote controls only. All other remote controls then return '128' as the errorlevel code. Noise and nonsense signals produce errorlevel code '255'. The program may be left by pressing the Escape key.

PCRemote

Mr. K. Duesman from the Netherlands produced the second mini project we present in this article. The project is comprised of a program for MSDOS and a miniature infrared receiver/interface for connecting to the PC's RS232 port. The combination of the hardware and software enables just about any infrared remote control to supply PC keyboard codes. The program even supports different brands of IR remote control. By linking keystroke combinations on the PC keyboard to a certain key on the remote control, PCRemote may be 'taught' to put certain code strings into the PC's keyboard buffer. The interface required for this purpose is of the *KISS*type (Keep It Smple Stupid).

Hardware

Figure 3 shows the circuit diagram of the infrared interface. As in the previous project, an SFH506-36 from Semens is used to receive and demodulate the infra-red signals. The interface also comprises an IR trans-

COMPONENTS LIST

Resistors: (all SMA) R1 = 470Ω R2,R5 = $10k\Omega$ R3 = $8k\Omega 2$

 $R4,R7 = 4k\Omega7$ $R6 = 68\Omega$

Capacitors: C1 = 4nF7 SMA $C2 = 220\mu F$, 16V, radial

Semiconductors:

Miscellaneous:

K1 = 9-way sub-D socket (female) cable mount

mitter which is used for test purposes (together with the utility TestFreq.com). The supply voltage for the parts on the interface board is 'stolen' from the RS232 port.

The board is built using the artwork shown in **Figure 4**. To make for miniature size, many parts are surfacemount assembly (SMA) types. The printed circuit board is not available ready-made from the Publishers. The board is connected to the PC via a standard 9-way RS232 cable.

Softwa re

In true experimenter's spirit, Mr. Duesman has supplied a number of files for this project, including executables, PCB designs in HPGL format and documentation. The following are the *main* files you will require:

| PCHemote.com | ariver | | | |
|--------------|----------|------|----------|--------|
| PCRemote.dat | sample | e d | ata file | Э |
| Manage.exe | learn | & | edit | key- |
| | stroke | СС | mbina | ations |
| | (shell p | orog | gram) | |
| Turnoff.com | a help | uti | lity | |
| Testfreq.com | a help | uti | lity | |
| | | | | |

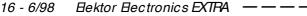
Obtaining the software

All programs and files discussed in this article may be found on a CD-ROM entitled **Software Competition 1996/97**, available through the Publisher's Readers Services as order code **976003-1**.

RC5 decoder project: look in subdirectory NI/10/.

PCRemote project: look in subdirectory NL/7.

(982052-1)

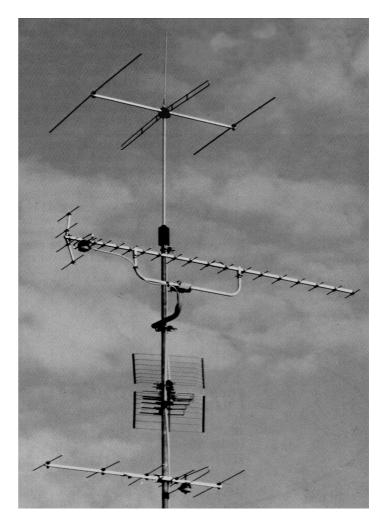




co-channel interference suppression using stacked antennas

a clever solution for VHF/UHF radio and TV

If you want to receive a distant or even overseas TV station that happens to use the same frequency as a strong local transmitter, the received signals will be weak and always suffer from ghost effects, moiré and other interference. In some cases. reception will be totally impossible because of the much greater signal strength of the station around the corner. This article describes an interference reduction method that may be used for UHF TV as well as VHF radio (including amateurs).



Because of the plethora of satellite TV broadcast stations currently crammed into the available bandwidth of cable-TV networks, terrestrial (foreign) programmes are often neglected. Unfortunately, most of these programmes (like Belgian, Dutch or Irish ones) are not on satellite, so interested viewers in coastal regions of the UK mainland are forced to use 'ordinary' TV antennas to receive these programs at justabout-acceptable quality.

Whenever these signals are weak and almost blotted out by interference, you should always remember that there is really no reason to complain. After all, the radiated power, antenna height and radiation pattern of the relevant TV transmitter are such that its designated target area is reliably covered. Any signal that spills outside the normal coverage area, by special propagation conditions or otherwise, is simply good fortune. Many viewers of foreign terrestrial TV stations can live with that, were it not for the fact that reception often suffers from a national TV transmitter or relay that uses the same,

Design by W. Fischer, DD0RQ

or almost the same, frequency. Although there is some international co-ordination between TV transmitter operators as regards channel allocations of high-power TV transmitters, in general no responsibility is assumed for interference inflicted by a national transmitter on the reception of a foreign one.

Similar problems often occur with VHF radio reception and amateur radio (for example, beacons using the same frequency).

Interference readily occurs under favourable propagation conditions. Particularly with ordinary (AM) TV on UHF, even the weakest station on the same channel can cause very annoying interference patterns in the normally crisp and clear picture from a strong nearby station.

Co-channel interference may be suppressed to a considerable extent by using a pair of stacked yagi antennas rather than a single one. Although they are directed at the 'weak' station, the two antennas are not stacked to increase their total gain (by 3 dB in theory as a result of increased directivity). Rather, this is done to cancel out the signal picked up from the strong station that is the source of the interference.

STACKED ANTENNAS

The underlying principle is illustrated in **Figure 1**. Two *identical* antennas are mounted at a distance 'd', and their signals are taken to a power combiner by way of two coax cables *having the same length*.

As the antenna array is aimed at the desired ('weak') station, the received signals will arrive in-phase at the inputs of the power coupler. If the antennas are spaced by the so-called *optimum stacking distance*, the gain so obtained is 3 dB in theory. However, this distance is not used here, because we aim at cancelling interference, and not increasing the antenna gain or sharpening the antenna pattern!

A signal picked up from an interfering station at an angle α will arrive with different phase angles at each of the two antennas (actually, just the dipoles). In fact, the signal arriving at antenna A2 covers an extra distance, *s*, of

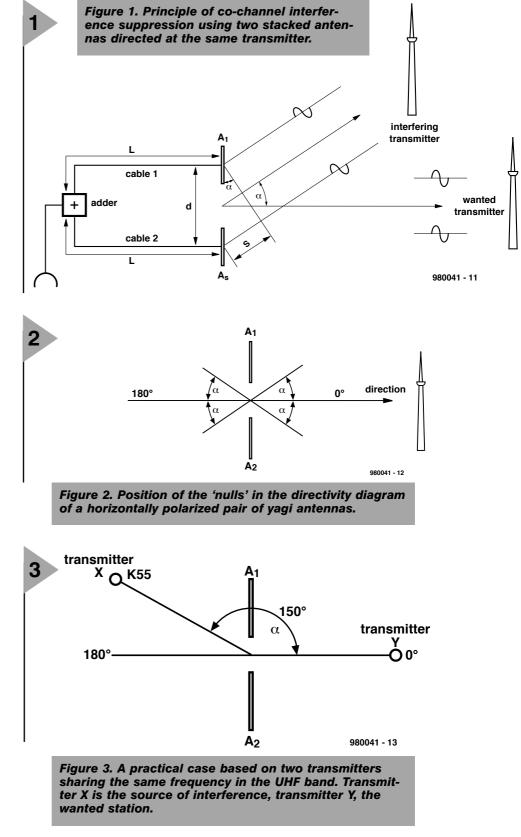
 $s = d \sin \alpha$

The phase shift, φ , incurred underway equals

 $\varphi = 360 \, s/\lambda$

where λ is the wavelength of the signal.

For total eradication of the signal received from this direction, the received signal voltages have to be



equal and exactly 180 degrees out of phase.

As shown in **Figure 2**, the stacked antennas have four so-called 'nulls' in their directivity pattern. These nulls occur at mirror-image positions with respect to the main axis of reception.

COMPUTING THE

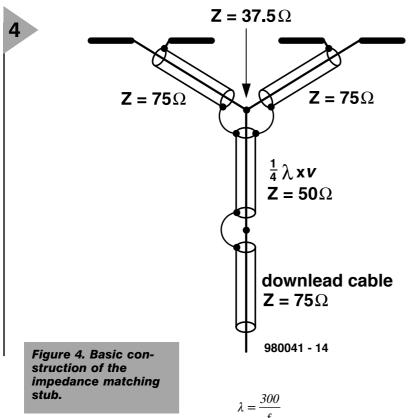
STACKING DISTANCE The distance *d* between the two yagi antennas is computed from

$$d = \frac{\lambda/2 + n \cdot \lambda}{\sin \alpha}$$

In case the calculated distance d is so small as to cause the antenna reflector elements to touch each other, the constant n may be made 1, 2, etc. (integer value required).

Unfortunately, a phase shift of 180 degrees can not be obtained from two antennas stacked as described here,

15



because in that case the wanted signal would be cancelled, too.

Using careful construction, however, co-channel interference may be suppressed by at least 25 dB.

EXAMPLE

The author lives in Southern Germany, and wants to receive an Austrian TV station situated just across the border. The situation is illustrated in **Figure 3**. Both station X and station Y use channel 55 (picture carrier at 743.25 MHz). In this example, the desired station uses transmitter Y, whose reception is to be freed from constant interference caused by high-power station X.

Well, these transmitters actually exist, as well as the receiver location:

X = ARD (German regional TV), location Cham, transmitter power approx. 100 kW.

Y = ORF 2 (Austrian national TV), location Zug peak, transmitter power approx. 2 kW.

A = receiver location, Vohburg/Donau.

Using the above equations, the distance between the identical UHF yagi antennas is calculated as follows: $\lambda = \frac{300}{\text{f}}$ $\lambda = \frac{300}{743.25 \text{ MHz}} = 0.403 \text{ m}$ $d = \frac{\lambda/2 + \text{n} \cdot \lambda}{\sin \alpha} = \frac{0.403/2 + 0.0.403}{\sin 150^{\circ}}$ d = 0.403 m

d = 1.2096 m

Because it is not possible to mount the antennas at a distance of just 40 cm (result of the first calculation), the next higher distance is calculated using n=1. The result is a distance, d, of 1.2096 m, which was actually implemented by the author to build the stacked antenna array.

PRACTICAL REALISA-TION

The two antennas are connected up using a coax coupler device obtained from an antenna installer. The author used a Reichelt coupler type RW021-DC. This simple and inexpensive solution does have a drawback, however: its insertion loss of about 4 dB nullifies any extra gain obtained from stacking the antennas. With weak antenna signals, a different method of coupling the antenna signals is recommended. The alternative is the quarter-wavelength impedance transformer (stub) whose construction is illustrated **in Figure 4**. For clarity's sake, the antenna dipoles are sketched only.

The two antennas are electrically connected in parallel by two pieces of 75-ohm coax cable *having the same length.* The impedance at the junction of the cables is then 75/2=37.5 ohms. A piece of 50-ohm coax cable (for example, the ubiquitous RG58) is then used to step up the 37.5 ohms source impedance to 75 ohms as required for the download cable. The impedance of the matching stub is calculated from

$$Z_{\rm L} = \sqrt{Z_{\rm source}} \cdot Z_{\rm downl}$$

The 50-ohm impedance of our 'realworld' RG58 cable is sufficiently close to the theoretical value of 53 ohms produced by the equation.

The simple equation you will need to calculate the length of the matching stub is given in Figure 4.

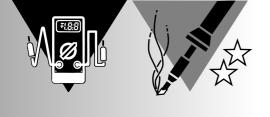
The factor v in the equations is the so-called *velocity factor*, a material constant specified for coax cable by its manufacturer. For RG58 cable as used here, v is stated as 0.66 in the datasheets. Using this constant, the length of the 50-ohm matching stub for the example in Figure 3 is calculated as follows:

f = 743.25 MHzCable = RG58CU; v = 0.66.

$$\lambda = \frac{30000}{\text{f}} \left[\text{cm} \right]$$
$$1 = \frac{\lambda}{4} \cdot \text{v} \left[\text{cm} \right]$$
$$1 = 6.66 \text{cm}$$

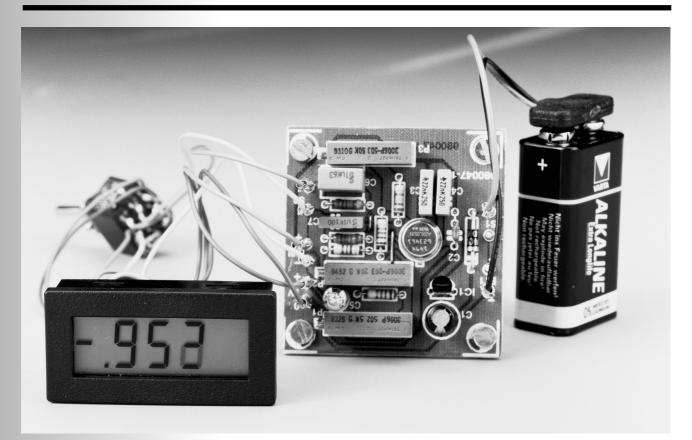
Provided you carefully assemble the stacked antenna array, the signal coupler and impedance matching stub, the method described in this article should enable a previously interference-ridden TV signal to be received much better.

(960041-1)



electronic accelerometer

measure acceleration, deceleration, shock, tilt and vibration



Just over a year ago we published an Application Note covering the type ADXL05 accelerometer chip from Analog Devices. Now it's time to actually use this interesting device in a project for home construction.

From your physics lessons you may recall that acceleration is normally measured in metres per second squared. Acceleration due to the earth's gravity force is, however, usually expressed as a factor of *g*, where *g* is the internationally adopted value 9.80665 m/s². Any forces considerably greater than 1 *g* can produce complex sensations in humans beings: jetfighter pilots, and astronauts can tell you all about them. For your very own experience, do some travelling up and down in a fast elevator system in a tower flat!

Back to electronics, now. For those of you who missed the above-mentioned article, here's a quick rundown on the main component in the present project, the ADXL05.

As illustrated in Figure 1a, the

accelerometer is contained in a 10-pin TO100 metal case, and consists of a sensor, an oscillator, a demodulator, preamplifier, voltage reference and a buffer amplifier. The device will measure accelerations with full-scale ranges of ± 5 g to ± 1 g or less. Its typical noise floor is 500 μ g/Hz, allowing signals below 5 mg to be measured. The ADXL05 can measure uniform acceleration, such as that due to gravity, as well as variable accelerations, such as vibration.

Since acceleration is a vector quantity, the device has three axes: a sensitive axis (X) which is defined as illustrated in **Figure 1b**, a transverse axis (Y), which is perpendicular to the axis of sensitivity in the plane of the package circle, and a transverse axis (Z), which

From an idea by J. Wilkes

is perpendicular to both X and Y. The transverse sensitivity is virtually nil.

CIRCUIT DESCRIPTION

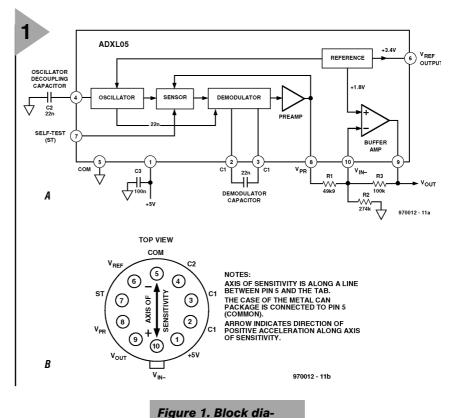
As shown by the circuit diagram in Figure 2, the accelerometer is batterypowered, and equipped with a digital readout in the form of an LC (liquid crystal) display.

At an acceleration of 0 *g*, the sensor output supplies a *nominal* 1.8 V. Two things have to be said about this value. First, it is subject to a tolerance of ± 0.3 V. Second, this value allows positive as well as negative *g* values to be measured. To make sure the DVM indicates 0 *g* at a sensor output of 1.8 V, we need to raise its negative input (–) with respect to ground, in other words, add an offset of 1.8 V. This is done with the aid of the 3.4-V reference voltage supplied by the ADXL05, R1, R2 and preset P1.

Preset P3 and resistor R6 allow any deviation from the nominal 1.8-V (0-*g*) output level supplied by the ADXL05 to be corrected.

Although the use of a DVM module with a full-scale readout of 200 mV does make for a compact and state-of the-art circuit, it does cause some apparently contradicting requirements, for which comprises have to be found. To fully exploit the meter's sensitivity and accuracy, it has to be matched to the typical sensitivity of about 200 mV/g of the sensor. That is not too difficult: simply design for a buffer gain of 0.5 and so create a range of 2 g which corresponds to a full-scale read-

out of 200 mV. On the other hand, the full drive margin the sensor is then not exploited because the device has a range of 5 g. By choosing a gain of 1/20 (0.05), 5 g then produces a readout of just



gram (a) and axes of

sensitivity (b) of the

ADXL05.

50 mV, which, admittedly, is not favourable in respect of DVM accuracy. There you are, however, with two

switch-selectable ranges of ± 2 -g and ± 5 -g ranges as trade-offs between display accuracy and sensor accuracy.

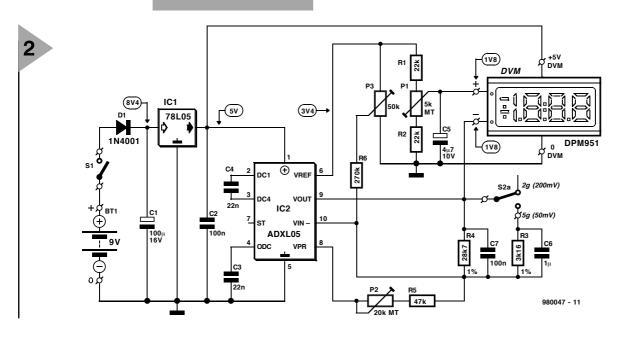
Because the sensor sensitivity is also subject to a tolerance of $\pm 25 \text{ mV/}g$, the buffer gain is made adjustable with preset P2.

The accelerometer is powered by a 9-volt PP3 battery whose output voltage is stepped down to 5 V by an 78L05 regulator in position IC1. Current consumption will be about 15 mA, of which 2 mA goes on account of the DVM module. Finally, the circuit contains a number

of decoupling capacitors at critical locations.

CONSTRUCTION

The accelerometer is easy to build on the printed circuit board whose artwork (copper track layout and component mounting plan) is shown in **Figure 3**. The only point to note here is that the sensor has to be soldered directly on to the board (do not use an IC socket). This is essential because the sensor has to be level when the board is level. The external components (on/off switch, battery, range selector



6/98

Figure 2. Circuit dia-

count is achieved

module.

gram of the accelerom-

eter. A low component

thanks to the use of an

integrated sensor and

a ready-made voltmeter

Visit our Web site at http://ourworld.compuserve.com/homepages/elektor_uk

COMPONENT LIST Resistors: $R1.R2 = 22k\Omega$ R3 = $3k\Omega 16$ 1% (Philips MRS25 series) R4 = 28k7 1% (Philips MRS25 series) $R5 = 47 k\Omega$ $R6 = 270 k\Omega$ P1 = $5k\Omega$ multiturn 10 turn horizontal P2 = $20k\Omega$ multiturn 10 turn horizontal P3 = $50k\Omega$ multiturn 10 turn horizontal **Capacitors:** $C1 = 100 \mu F 16V$ radial C2 = 100nF Sibatit (Siemens) C3,C4 = 22nF MKT (Siemens) $C5 = 4\mu F7 \ 10V \ radial$ $C6 = 1\mu F MKT$ (Siemens) C7 = 100nF MKT (Siemens) Semiconductors: D1 = 1N4001IC1 = 78L05 IC2 = ADXL05JH (Analog Devices) Miscellaneous: BT1 = 9V battery PP3 block S1 = rocker switch, 1 make contact S2 = rocker switch, 1 c/o contact, or 3x c/o contact for decimal point on dvm DVM = DPM951 DVM module (Conrad)

and DVM) are wired up as illustrated in **Figure 4**. Do not yet connect the DVM module, however, because the accelerometer has to be adjusted first.

ADJUSTMENT

1. Connect a digital multimeter to the circuit ground and –DVM terminal, and adjust P1 for a reading

of 1.80 V. Next, connect the multimeter between ground and +DVM. Make sure the board is

Figure 4. Suggested wiring diagram. The decimal point on the DVM module is switched with two sections of S2.

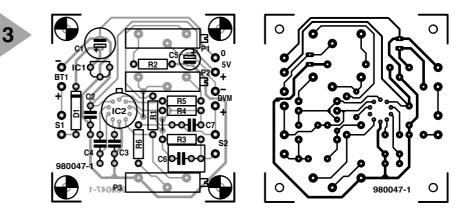


Figure 3. Copper track layout and component

mounting plan (board not available ready-made).

level (0 *g*), and adjust P3 for 1.80 V again. Now con-

nect the DVM module to the accelerometer board.

- 2. Change back and forth between the two ranges. The indicated value should remain the same. If not, adjust P3. Next, adjust P1 again until the module indicates 0 g. Repeat these adjustments until a reasonable optimum is achieved.
- 3. Select the ± 2 -*g* range, and hold the board perpendicular with pin 10 of IC1 pointing upwards. Adjust P2 for a reading of 1.000 (1 *g*). Now turn the board so that pin 10 of IC1 points downwards. The DVM should then indicate -1.000. If not, adjust P2 until the deviation for +1 g equals that for -1 g. This deviation is caused by the above-mentioned (small) transverse sensitivity of the ADXL05.

That completes the adjustment of the instrument. Having 'boxed' the project,

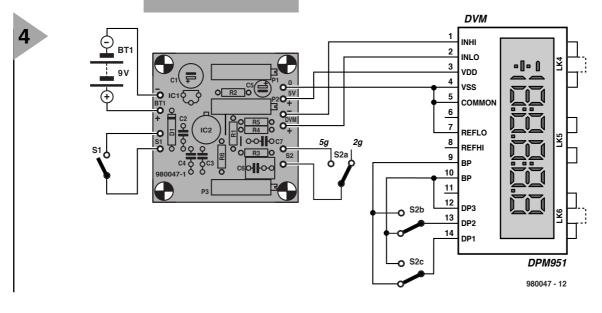
you should be ready to do some real-world *g* testing in a fast elevator or one of those stomachchurning machines you see at funfairs.

Finally a few words about the DVM module used in this project. This module has an option for 'floating' measurements, which allows the circuit to be powered by a single battery. The accelerometer board has a 5-volt connection for powering the DVM module. It should be noted that the negative connection of the DVM module represents a low resistance. Consequently it can not be connected to the negative terminal of the accelerometer board. So it is connected to the (buffered) positive terminal instead. The only difference it makes is the orientation of the sensor (simply turn the accelerometer board 180 degrees). By using a triple changeover switch in position S2, the decimal point on the DVM module can be switched according to the range selected.

(980047-1)

Reference:

Accelerometer Type ADXL05, Application Note, *Elektor Electronics* April 1997.



electronics on-line PICs on the Internet

Microchip's family of PIC devices comprises a small galaxy of single-chip microcomputers, which achieved tremendous popularity mainly because they are so easy to program. We rummaged around on the Internet for a bit and stumbled on an overwhelming amount of information relating to PICs. Some of the more essential sites are discussed here.

The number of sites (on the Internet) covering PIC-related subject reflects the widespread interest in these controllers. The contents of these sites ranges from simple exchanges of information to commercial pages offering ready-built circuits for sale. Many doit-yourself (DIY) enthusiasts, including many readers of this magazine, will be interested mainly in construction projects and free PIC software.

As a matter of course we should start by mentioning the site run by the manufacturer, Microchip: www.microchip.com

Here, all elementary information may be found. Then there's Parallax Inc., who supply the famous BASIC Stamp, a miniature board containing a PIC running a BASIC interpreter. Parallax can be found at

www.parallaxinc. com/home/htm

There are many more companies supplying hardware and/or software employing PIC devices. For example, ITU Technologies from Cincinnati: www.itutech.com

The PIP02 software for the Mini PIC Programmer described our June 1997 issue is available from Silicon Studio at *www.sistudio.com*

PROGRAMMERS

Designs for PIC programmers and the associated software may usually be obtained from sites run by enthusiasts publishing their 'thinkware' via the Internet. A PIC programmer for the PC parallel port (P16PRO), complete with printed circuit board design and Windows software may be found on the Maribor University server (in Slovenia) at *www.uni-mb.si/* ~*uel205e7b/* (our thanks are due to Mr. E. Dekker for supplying this URL).



Another programmer for the Centronics port goes by the name of TOPIC. It may be found at *www.man.ac.uk/~mbhstdj/topic.html* However, if you want to keep things as simple as possible, you are well advised to look for a PIC programmer for the serial port. One definitely *KISS* (Keep It Simple Stupid) and yet welltried design is, for example, COM84. All details on this ultra-simple design are available on

warthog.eece.maine.edu/segee/prog84.html Finally, we should mention the Pro-

grammer 2 design at

www.gbar.dtu.dk/~c888600/newpic.htm

The above mentioned programmers are just a few of dozens of designs that may be found on the Internet.

LINKS

Because of the sheer volume of information available on PICs via the Internet, it's a good idea to have a look at pages maintained by people who have done research work. Eric's PIC page is very extensive an offers, among others, PIC projects, tips and tricks, FAQs and a plethora of links to other PIC sources and suppliers. Go to

www.brouhaha.com/~eric/pic/

Dave Tait, who is also responsible for the TOPIC programmer, runs a page called 'Links to Internet Resources', which contains hundreds of links to books, commercial products, application areas, and other people experimenting with PICs:

www.man.ac.uk/mbhstdj/piclinks.html

The South African PIC Microcontroller Zone at *www.ip.co.za/people/kalle/pic/default.htm* has a nice collection of assorted PIC

and mail lists.

Finally, if you think you need even more information, visit the PIClist Archive Website at

www.iversoft.com/piclist/

which can be browsed by subject, date or author.

(985045-1)





PIC & AVR programmer

Hardware and software to program PIC and AVR microcontrollers



The hardware and Windows 95 software discussed in this article enables you to program Microchip's highly successful 16C84 and 16F84 microcon-

trollers, as well as Atmel's 'AVR' types AT90S1200, AT90S2313, AT90S4414 and AT90S8515. All of these RISC 'beasts' are incircuit programmable, and offer internal Flash/EEPROM program memory, static RAM, various input/output lines and another EEPROM for the microcontroller to write to.

It's almost impossible to think of modern electronics without microcontroller applications. Microcontrollers have a vast number of application areas, ranging from the PC mouse to process control units, not only in industrial systems but also the latest washing machines. Admittedly, very few of you will be interested in developing their own washing machine. However, applications that do come to mind for home development may include a timer-controlled window shutter, an infrared controlled garage door, a sound-to-light unit, or a

Design by W. Schroeder

Visit our Web site at http://ourworld.compuserve.com/homepages/elektor_uk

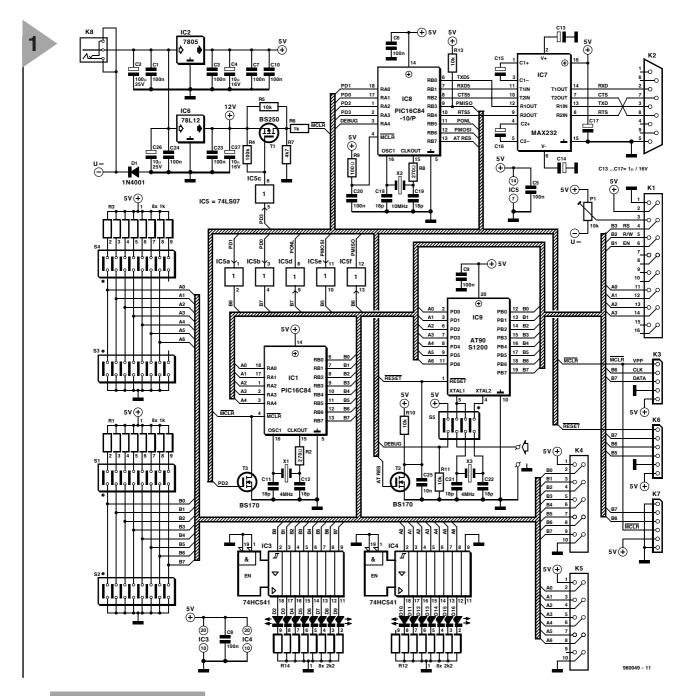


Figure 1. Circuit diagram of the programmer and programming socket adaptor IC9.

digitally controlled laboratory power supply. In these examples, processor controls using more or less powerful microcontrollers are a great option.

The PIC controllers type 16C(F)84

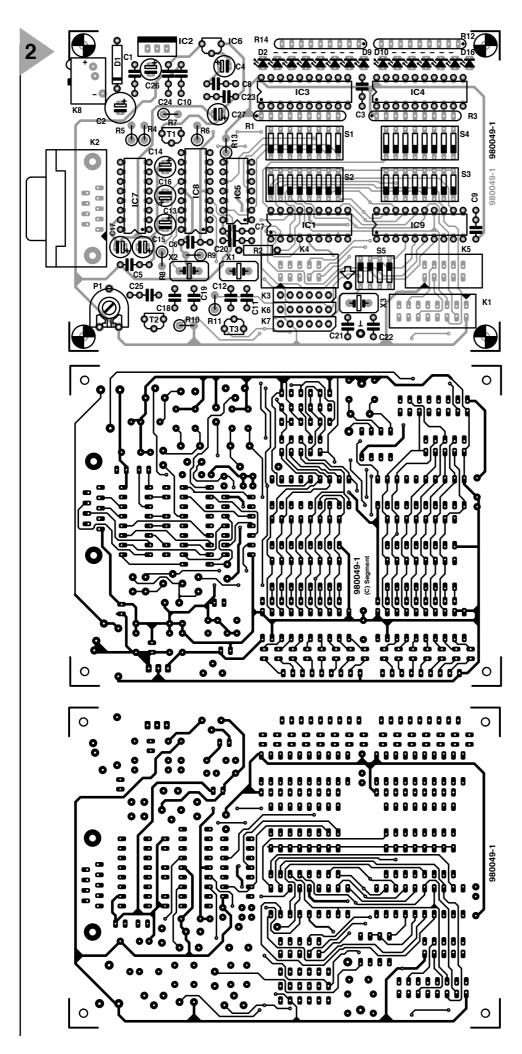
belong in the class of less powerful but also less expensive devices. These RISC controllers have an instruction set of just over 30 instructions (hence *reduced instruction set*). They can be operated at a clock frequency of up to 10 MHz, and then offer a command cycle time of 400 ns, which equals 1/4th the clock frequency.

When more computing power is required, or more I/O pins, you should

opt for Atmel's AVR controllers. The smallest of these, the AT90S1200, was already the subject of a project for home construction (Ref. 1,2), and it may be compared, as far as computing power is concerned, with the PIC devices. The larger AVR controllers offer additional features like an integrated RS232 interface, a serial SPI interface, pulse width modulation, two timers, up to 120 instructions, and so

| Controller | Clock | RAM | Progr.Flash | EEPROM | I/O | TIMER | RS232 | SPI | PWM |
|---------------|--------|----------|-----------------|--------|-----|-------|-------|-----|-----|
| PIC 16C(F)84 | 10 MHz | 36 B | 1024 W | 64 B | 13 | 1 | - | - | - |
| AVR AT90S1200 | 16 MHz | 0 B* | 512 W | 64 B | 15 | 1 | - | - | - |
| AVR AT90S2313 | 20 MHz | 128 B* | 1024 W | 128 B | 15 | 2 | Х | - | X |
| AVR AT90S4414 | 20 MHz | 256 B* | 2048 W | 256 B | 32 | 2 | Х | Х | X |
| AVR AT90S8515 | 20 MHz | 512 B* | 4096 W | 512 B | 32 | 2 | Х | Х | X |
| | | * + 32 × | 8 Bit Registers | | | | | | |





on. The fact that these devices process instructions at the full clock rate makes them four times as fast as a PIC, assuming the same clock rate is used.

For comparison purposes, **Table 1** lists the main features of the individual microcontrollers. Currently, the best available microcontrollers are the PIC16F84, AT90S1200 and AT90S8515 (max. 8 MHz).

HARDWARE DESCRIPTION AND

CONSTRUCTION The hardware and software presented in this article allows you to program Microchip's PIC16C84/16F84 as well as all currently available (early 1998) Atmel AVR microcontrollers (AT90S1200, AT90S2313, AT90S4414, AT90S8515). All RISC microcontrollers supported by the present design are in-circuit programmable using a 'shell' called PICAVR32 which runs under Windows 95. These controllers offer an internal Flash/EEP-ROM program memory, SRAM, a plethora of input/output lines and an EEPROM to which the microcontroller has direct access.

Building the hardware should not present difficulties if you work carefully and take your time. With the possible exception of the ready-programmed PIC in the circuit, only commonly available parts are used. The firmware-code PIC, by the way, is available ready-programmed, either directly from the Publishers or through kit suppliers advertising in this magazine.

The hardware is designed in such as way that PICs as well as the DIL-style AT90S1200 and AT90S2313

> Figure 2. Everything fits on this double-sided through-plated board (available ready-made through the Publishers).

COMPONENTS LIST

Items available from the Publishers: PCB, programmed PIC and disk, order code 980049-C. Firmware PIC only, order code 986509-1. Project disk only, order code 986019-1.

Resistors:

R1,R3 = SIL-Array 8 x 1k Ω $R2.R8 = 270\Omega$ $R4 = 100k\Omega$ $R5,R10,R11,R13 = 10k\Omega$ $R6 = 1k\Omega$ $R7 = 4k\Omega7$ $R9 = 100\Omega$ R12,R14 = SIL array 8 x $2k\Omega 2$ $P1 = 10k\Omega$

Capacitors:

C1,C3,C5-C10,C20,C23,C24 = 100nF $C2 = 100\mu F 25V$ radial C4,C27 = 10μ F 16V radial C11,C12,C18,C19,C21,C22 = 18pF C13-C17 = 1μ F 16V radial C25 = 10nF $C26 = 10\mu F 25V$ radial

Semiconductors:

D1 = 1N4001D2-D16 = LED, low current T1 = BS250T2 T3 = BS170IC1 = PIC16C84/F84 to be programmed IC2 = 7805IC3,IC4 = 74HC541 IC5 = 74LS07 IC6 = 78L12

chips may be programmed and tested by inserting them in a DIL socket on the programmer board. Mind you, these are the chips you want to program, not the PIC mentioned above (containing the firmware code).

In addition, all microcontrollers may be programmed in-circuit via connectors K6 (AVR) and K3 (PIC), which is particularly useful for the AT90S4414 and AT90S8515 which come in a PLCC case.

The programmer board is powered by a mains-adaptor (15 V, 500 mA) connected to K8. When only AVR chips are programmed, a 9-volt adaptor is sufficient because AVR devices do not require an additional programming voltage. The supply voltage is stabilized by a 7805 voltage regulator (IC2) and its satellite decoupling capacitors C1-C4 for smoothing and decoupling. A 78L12 regulator (IC6) is responsible for the extra 12-V PIC programming voltage.

The heart of the PICAVR32 programmer is PIC IC8, which contains the firmware code and arranges all communication with two parties: at one side, the PC, and at the other side, the microcontroller to be read or programmed. The link with the PC is established using an ordinary 9-way 1to-1 sub-D extension cable (socket & plug). The well-known level converter type MAX232 (IC7) on the programmer board changes RS232 voltage levels (±12 V) into TTL/CMOS compatible signals (5-V), and feeds them directly to the corresponding I/O pins of the

firmware PIC, IC8. This chip responds by forwarding control commands set up by the PC software either to the PIC or the AVR to be programmed (positions IC1 and IC9 respectively). In the present programmer both microcontroller types are programmed serially by way of an SP interface. For this the AVR chips employ I/O pins 5, 6 and 7 on Port B (MOSI, MISO, SCK)). The PICs are programmed via I/O pins 6 and 7 of Port B (CLK, DATA). To these programming signals should be added the supply voltage (GND, VCC) and the /RESET or /MCLR signals, all of which are also needed during programming. All relevant signals are taken into account in the pinning of the in-circuit programming connectors mentioned above. When designing your own (application) circuits in which this type of programming is to be employed, you should make sure that 'collisions' between the programmer hardware and the target system hardware are avoided! In particular, be sure to provide series resistors on the signal lines used during programming.

To prevent the risk of your own circuits under test causing damage to the programmer hardware, the latter contains an open-collector driver type 74LS07 (IC5) as well as transistors T2 and T3, which buffer all lines of the firmware PIC, IC8. The use of opencollector drivers does, however, necessitate the switching on of the DIP switches for the pull-up resistors. For the AVR chips, the Port-B lines are pulled up (S1.6, S1.7, S1.8), while for

IC7 = MAX232 IC8 = PIC16C84-10/P (ready-programmed, order code 986509-1) IC9 = AT90S1200 to be programmed Miscellaneous: S1-S4 = 8-way DIP switch block S5 = 4-way DIP switch block X1,X3 = 4MHz quartz crystal X2 = 10MHz quartz crystal K1 = 16-way boxheader K2 = 9-way sub-D socket (female), angled, PCB mount K3,K6,K7 = 6-way SIL pinheader K4,K5 = 10-way boxheader K8 = mains adaptor socket, PCB mount Diskette containing PICAVR32 program, order code 986019-1.

the PIC chips S1.7 and S1.8 are switched on. The other switches in S1 and all switches in S4 should be 'on'. All switches in S2 and S3 should be set to 'off'.

The /RESET line of an AVR chip is controlled via transistor T2. The falling pulse edge at the /RESET pin is essential to initiate a programming sequence on an AVR chip. Because the /MCLR pin on PIC chips has to be at 12 V during programming, T1 is required in addition to T3 which arranges the actual resetting of the PIC. Normally, T1 and T3 are both switched off. The junction R5-R7 supplies a voltage of about 4 V, which arrives at the /MCLR input of the PIC to be programmed, via resistor R6. To reset the PIC, the /MCLR pin is pulled to ground via T3. The programming voltage is applied by switching on the p-channel MOS-FET. When the MOSFET conducts, it short-circuits R5, so that 12 V is applied to R6.

PICs to be programmed are clocked at 4 MHz – other clock frequencies are also possible. For AVR chips a quartz crystal is available, and, as an alternative, a complete crystal-controlled oscillator.

The DIP switches provide assistance with the testing of input/output operations of the two microcontrollers. Switches S1 and S4 connect 1-kQ pullup resistors to all port lines, while S2 and S3 allow port input lines to be held logic low. Users should take care not to use the input switched on port lines declared as outputs! Doing so (by acci-

29

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dent) may cause damage to the relevant port of the PIC or AVR chip to be programmed.

Low-current LEDs D2 through D12 indicate the port-line states. They are controlled via IC3 and IC4.

The hardware when finished is tested with the aid of a couple of specially written test utilities. First, however, let's have a look at the control software running on the PC.

WINDOWS 95 CONTROL SOFTWARE

The software developed for the PIC & AVR Programmer also enables assembly code for PICs and AVRs to be developed, programmed and read. For this purpose, the program as well as the EEPROM memory may be read and written. You can get started with the programmer once it is connected up to the PC's serial port (via a 9-way sub-D cable with no crossed wires), and connected to its power supply. To begin with, you should burn a PIC with the file TESTPIC.ASM, or an AVR chip with the file TESTAVR.ASM. In addition to a controller test, all LED outputs are checked with the aid of a running light. Follow this procedure.

Launch PICAVR32

The PICAVR32 shell first looks for the programmer hardware. When the hardware does not report back, a message reading **No COM Port Selected** is indicated near the bottom of the screen.

Select RS232 port

Select a free RS232 port using the menu OPTIONSI COM PORT. When the programmer hardware is found, the status line reads PICAVR32 (*PIC Version x.x.*) ready. The menu option CONTROLLER is then accessible.

Load assembly-code file

Under Filel Open, load the above mentioned assembler source code file. Alternatively, use the **FILE LOAD** option to fetch a finished Hex(adecimal) file.

Assemble file

Use **FILE START ASSEMBLER** to launch the assembly-code to object-code translation.

Download object code

Next, the menu option CON-TROLLERI DOWNLOAD PROGRAM is used to actually program your PIC or AVR chip. Provided no errors occur during programming, the relevant

> Figure 3. Some screenshots showing PICAVR32 in action.

controller is started, and the LEDs on the programmer board act as a (slightly mixed-up) running lights.

OPTIONS

The software offers various optional functions in addition to the straightforward 'load-file-and-program-away' sequence outlined above. Help with the individual menu options can be summoned up by pressing the F1 key. The menus **FILE**, **EDIT** and **HELP** should be self-explanatory, so they are not discussed here.

Under **OPTIONSI CONTROLLER** you can select the controller to be programmed. If the controller type is included in the first line of the assembly-code file, behind the semicolon, then it is automatically selected when the assembly-code file is loaded.

The **OPTIONSI EDITOR** menu entry allows you to select editor cosmetics like font, colour and type, as well as background colour.

OPTIONSI ASSEMBLER OPTIONS serves to 'adjust' the assembler and the parameter required for calling the assembler. For PIC devices you should use *Microchip Assembler Release 1.4*. For AVR devices, use *AVRASM Version 1.1*. Be sure to obtain the *DOS* versions of these programs, which are **not** included on diskette 986019-1. They are, however, available free of charge from the Microchip and Atmel Internet sites.

OPTIONSI AUTODOWNLOAD, when enabled, automatically launches a program download operation, following successful source code assembly.

OPTIONSI PIC DIFF DOWNLOAD enables a difference-file download for PICs. It is particularly useful if only certain parameters of a program are to be modified, or just a couple of bytes. This option is only available for PICs because AVR chips have to be completely erased before any programming of the program memory.

OPTIONSI SLOW PC should be switched on when using a sluggish PC not having a serial FIFO for the RS232 interface. Use this option if errors occur frequently when downloading programs.

OPTIONSI DEBUG MONITOR launches a Debugging monitor that alows hex values to be produced using a test-output routine. The Debugging procedure and the relevant routines are discussed in greater detail in the PICAVR32 Help file.

By selecting **OPTIONSI SHOW ERRORS** you enable the program to display the assembler's error report file. The Error-Viewer is also opened automatically whenever the assembler writes an error entry in the Error file.

All functions found under the menu option CONTROLLER cover the downloading/uploading of programs, EEPROM and the internal configurations of the individual microcontrollers. The individual functions are, of course, dependent on the selected microcontroller type.

CONTROLLERI DOWNLOAD writes a currently loaded hex file or the object code (resulting from a previously compiled assembly-code file) into the controller. PICAVR32 has an internal buffer for the object code to be written into the microcontroller. A hexadecimal file loaded using the **FILEI LOAD INTEL-HEXFILE32** option is also transferred to this buffer, which has no graphics display in PICAVR32.

FILE SAVE HEX enables a controller to be read, and its contents to be written into a hex file.

CONTROLLER/UPLOAD reads the program memory in the microcontroller, and provides a window displaying the contents word by word in hexadecimal notation. If a microcontroller is read-protected an 'empty' program memory is displayed (FFFFh for AVRs, and 3FFFh for PICs). Output is in the form of words, because each of the two controller families has its own memory organisation. With PICs, the word length is 14 bits, with AVRs, 16 bits.

CONTROLLERI WRITE TO EEP-ROM enables you to modify individual bytes in the EEPROM range of the microcontroller. The EEPROMs in the PIC and the AVR are organised bytewise.

CONTROLLERI UPLOAD EEPROM enables the complete EEPROM to be read, and the contents to be displayed bytewise in hexadecimal notation. Under **CONTROLLERI CONFIGURE**

CONTROLLER you can define the basic configuration data of the relevant microcontroller. With the AVR chip, the

settings are very simple, because they only cover the Flash program protection option. With PICs, the settings not only control the program memory and EEPROM protection, but also the configuration of the oscillator and the power-up and watchdog timers.

CONTROLLERI ERASE CON-**TROLLER** enables microcontrollers to be cleared (erased). This option is useful if you want to reprogram a read-protected PIC.

CONTROLLER START CON-TROLLER performs a hardware reset of the microcontroller.

PROGRAMMING THE MICROCONTROLLERS

A discussion of the programming protocols for the two rival microcontroller families is, unfortunately, beyond the scope of this article. Those of you interested in these matters are referred to the following publications:

- Atmel AVR Enhanced RISC Microcontroller Data Book

- Microchip Datasheets DS30430A and DS30189D.

These publications not only contain extensive descriptions of the programming algorithms and procedures recommended by the respective chip manufacturers, but also provide discussions on the controller structures and explanations of all assembly-code instructions.

Finally, excellent support for the Atmel AVR series of microcontrollers is available from our advertiser Equinox Technologies.

(980049-1)

References:

 Electronic Handyman, *Elektor Electronics* December 1997.
 Programmer for

Handyman/AT90S1200, Elektor Electronics December 1997.

flat-panel displays

current & new technologies

Flat-panel displays have been in use in television receivers and computer monitors since the early 1980s. Strictly speaking, all electronic display devices, except the cathode ray tube (CRT) can be classified as flat panel types. But Sony introduced



a flat CRT television (Trinitron[™]) as early as 1982. What the world is waiting for now is the thin flat-panel display, which can be hung on a wall like a picture. However, in spite of early optimism after its introduction some years ago, lowering the cost of materials for the monolithic types and, more particularly, the assembly costs of hybrid devices have posed far greater problems in practical applications than originally expected.

By our editorial staff

6/98

Elektor Electronics

Electronic display devices can be divided into emissive and non-emissive types. The former include:

CRT (cathode ray tube); PDP (plasma display panel); ELD (electroluminescent display); VFD (vacuum fluorescent display); LED (light-emitting diode);

and the latter,

LCD (liquid crystal display); ECD (electrochemical display); EPID (electrophoretic image display); SPD (suspended particle display); TBD (twisting ball display); PLZT (transparent ceramics display).

The CRT was invented in 1897 in Germany (Braun); LCD watches were put on the market in 1972 in the USA; an ECD clock was introduced in 1982 in Japan (Seiko); an experimental PDP TV was shown in 1978 in Japan (NHK); the light-emitting diode (laser) was invented in 1962 in the USA (Nathan) and the first trial LED TV was shown in 1979 in Japan (Sanyo).

Undoubtedly, the bulk of the development work on flat-panel displays has been, and still is, carried out in the USA.

THE MARKET

The CRT display, which has the longest history (101 years), is still the leading type both economically and for display quality: it has almost 85 per cent of the world market. In 1997, hundreds of factories all over the world produced 68 million CRTs, and this is expected to grow to 85 million by

the year 2001. Number two is the LCD, which has about 10 per cent of the world market. In 1997, this type of display was manufactured in about 30 factories worldwide. The size of aperture (diagonal) of most of these displays varies from 10 in to 12 in (9 in to 11 in viewable). Larger sizes are possible, but they are only made in small numbers because these displays require new machinery, which is costly. Coupled with the fact that, owing to the explosion in the notebook market, the demand far outstrips the production capacity, manufacturers are loath to spend vast sums of money on new machinery while this situation continues. In 1997, the market demand for these displays was 6.9 million, whereas production capacity was only 4.3 million.

Nevertheless, some manufacturers are busy modifying existing factories or building new ones to start produc-

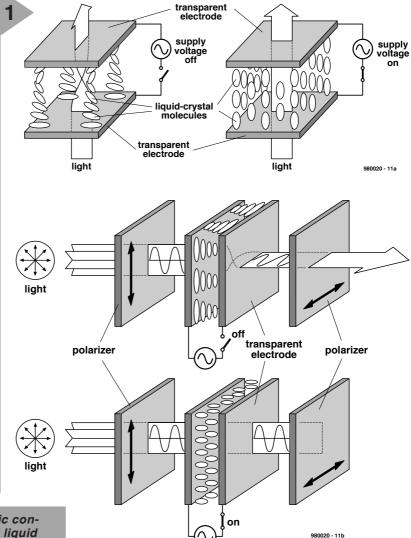


Figure 1. Basic construction of a liquid crystal display (LCD). Liquid crystal is sandwiched between two glass substrates and the construction is completed by an airtight sealing material around the periphery.

tion of 14 in (13 in viewable) displays within the next year or so. It is, however, unlikely that these

developments will bring down prices, particularly since many manufacturers of LCDs also produce CRT displays.

LCD VS CRT

From the point of view of the user, the LCD technology has advanced to the point where an LCD can replace a traditional CRT, at least as far as the smaller apertures are concerned. Technical developments have made possible better resolution, (relatively) larger apertures and higher frequency (currently up to 240 MHz). However, LCDs still suffer from a limited viewing angle, a limited contrast range, and a higher price than comparable CRTs.

PRINCIPLE OF LCD

In a liquid crystal display, the application of a voltage changes the molecular orientation of the liquid crystal, and the resulting change in optical characteristics, such as double refraction, optical rotation, dichroism, or optical scattering caused by the reorientation, is converted into a visible change.

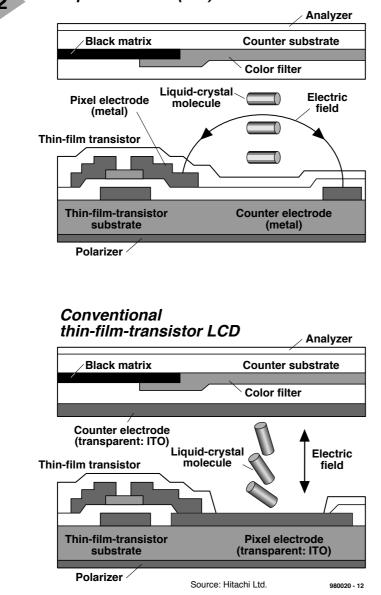
The most widely used types of LCD are the thin-film transistor (TFT) and the super twisted nematic (STN). Basically, each of these is a passive display that uses the modulation of light within a liquid crystal cell. This cell consists of a layer of liquid crystal about $10 \,\mu m$ thick sandwiched between two glass substrates on which are formed transparent electrodes. Grooves are etched in the surface of the electrode to impart a fixed orientation to the liquid crystal molecules. The grooves on each of the electrodes all point in the same direction and are used to direct the molecules mechanically, that is, the long molecules follow the grooves. See Figures 1a and 1b.

Owing to inter-molecular forces between the crystals, there is no, or



^{*} Nematic = having molecules or atoms oriented in parallel lines.

Super TFT LCD (IPS)



hardly any, random movement of the molecules which all adopt the same orientation.

The direction of the grooves on one electrode is, normally, at right angles to that of the grooves on the other electrode. In the

STN type, the molecular axis of the liquid crystal rotates continuously through 90° between the two substrates. Since the pitch of the twist is sufficiently large compared with the wavelength of visible light, the direction of polarization of linearly polarized light incident vertically on one of the electrode substrates is rotated through 90° by the twist of the liquid crystal molecules as it passes through the cell. Therefore, the nematic cell shuts off light when placed between two parallel polarizers and transmits light when placed between two

Figure 2. In an In-Plane Switching-mode (IPS) or Super Thin Film Transistor (TFT) LCD, the twisting of the crystal molecules is arranged with two electrodes positioned at the same side of the device.

orthogonal polarizers. When a voltage is applied to a twisted nematic cell, from a certain threshold voltage, $U_{\rm th}$, the molecule axes begin to align themselves with the electric filed. When the applied voltage is about $2U_{\rm th}$,

the majority of molecules have their axes realigned in the direction of the electric field, so that the 90° optical rotary power is eliminated. In this case, in completely the opposite fashion to the case when there is no voltage applied, between parallel polarizers, light is transmitted and between orthogonal polarizers, light will be shut off.

The basic operation as just described is illustrated in **Figure 1b**. It is based on the electrooptic effect when a twisted nematic cell is placed between two orthogonal polarizers. In this case, light is transmitted when there is no voltage applied, and light is blocked when a voltage is applied. Between parallel polarizers, however, the relationship between transmission and blocking of light is reversed. So, twisted nematic LCDs provide a black display on a white background or a white display on a black background.

A colour LCD contains in addition a colour filter for each pixel. Each of these pixels consists of three tiny dots (red, green and blue). This means that a colour display has three times as many pixels as might be expected on the basis of the graphic resolution.

The background of an LCD is a diffuse source of light, usually fluorescent, placed behind or at the side of the display. A diffusor ensures that the light falls uniformly over the display.

A serious drawback of an LCD is that relatively little light is transmitted: in practice only 3–5 per cent. This poor efficiency is caused partly by the polarizers (50%), and partly by the other transparent layers, particularly the black matrix (30%).

Manufacturers are constantly seeking to improve the efficiency, which is particularly important for users of notebook computers. In such computers, the life of the battery is already a matter of concern so that any improvement in efficiency will be more than welcome.

The company 3M has developed a special foil on which millions of small prisms are deposited. These prisms ensure that as much of the light as possible is incident at right angles. Because of the bundling effect of the prisms, the power of the light source can be halved.

ACTIVE OR PASSIVE

Liquid crystal displays come in two main types: the inexpensive passive types (STN = super twisted nematic), and the more expensive active type (TFT = thin film transistor).

In the STN device, the liquid crystal is controlled by a two-dimensional matrix of conductors. These indium tin oxide conductors are deposited on to the glass substrate. A potential applied to the crossing of two conductors changes the orientation of the crystal, which results in a pixel. Since the matrix is driven by the scan principle, this method is relatively slow. Moreover, variations in the electric field during fast image changes (as when text is being scrolled or a cursor is repositioned) cause annoying shadows. The contrast and the number of colours to be reproduced are limited.

In a TFT device, each pixel has its own transistor cell (whence its name). Transistor are deposited on one of the two glass substrates and can be controlled accurately and rapidly. This



type of display is therefore very suitable for use with a large colour spectrum and rapidly changing images. Owing to the amplification of the transistor, the strength of the electric field across the cell is greater than attainable with passive displays. This, in turn, results in a better range of contrasts.

VIEWING ANGLE

One of the more serious drawbacks of LCDs is their limited viewing angle of 15–40°. The larger the angle the display is viewed at, the more restricted the contrast. This is particularly disturbing in the case of a colour display. To solve this problem, a number of manufac-

turers have introduced a new technique, called variously In Plane Switching-mode (IPS) or Super TFT. This enlarges the viewing angle to almost 140° (depending on the manufacturer).

The new technique has the additional benefit of simplifying the production process. The two electrodes that switch a pixel are deposited on to the glass substrate together with the transistor cell. This means that there is no longer a potential across the whole LCD, but only across the pixel. The arrangement is shown in **Figure 2**.

In the quiescent state, when there is no voltage across the pixel, the molecules are in parallel with the grooves in the electrodes. Twisting of the molecules within the liquid crystal, as in Figure 1, does therefore not occur. The polariz-

ers, which are at right angles to one another, ensure that light is blocked over a large viewing angle, that is, the display is black.

When a voltage is applied, the molecules direct themselves according to the electric field, which is at right angles with the orientation of the molecules in the quiescent state. The stronger the electric field, the greater the rotation in the crystal, and the more light is transmitted.

PDP & FED

Two other important flat-panel displays are the plasma display panel, PDP, and the field emission display (FED).

The **plasma display panel** was first introduced in a paper in the USA in 1954 (Skellet). The first trial colour PDP TV was exhibited in 1978 by NHK in Japan. More recently, Fujitsu of Japan and Philips of the Netherlands have collaborated in the development of a

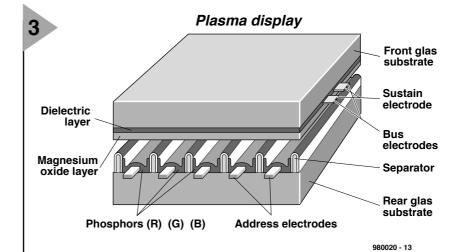


Figure 3. A plasma display panel (PDP) is a good alternative to the LCD, but it will take some time before this kind of display will become commercially affordable.

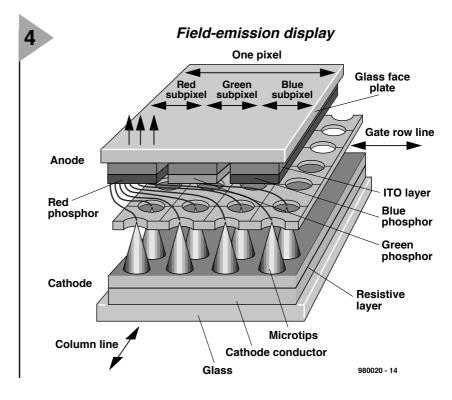
> 41 in wide TV screen. At present, the price of PDP displays is much too high for commercial exploitation, but it is expected that it will come down appreciably within the next few years. At the same time, there are still some fundamental problems to be resolved

Figure 4. In field emission displays, high electric fields strip electrons from the tips of the cathode (whereas in a cathode ray tube thermionic emission is used). The field-emitted electrons excite phosphors that may be identical to those used in CRTs, thus producing a CRT-like image in a flat, thin package. as well.

The basic layout of a PDP is shown in **Figure 3**. In current models, a potential of some 100 V is applied to the electrodes. It is expected that in near-future models this voltage may be lowered to about 60 V and in later models to about 10 V.

The life of a PDP is reckoned to be some 10,000 hours, comparable to the life a typical television receiver. Although the picture on a current PDP is good, it is not good enough. Annoying grey ghosting appears frequently with moving images.

Field emission displays combine the technology of the CRT with that of an LCD. This results in the excellent picture obtainable from a CRT reproduced on a flat panel display. The basic layout of an FED is shown in **Figure 4**.



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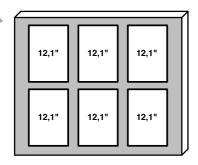


Figure 5. In the manufacture of LCDs, use is made on the production line of material of fixed dimensions. The use of other dimensions results in lower efficiency (profit!) and it may, therefore, be some time before larger aperture displays will become available.

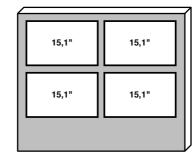
In principle, use is made of phosphors that are ignited by an electron beam.

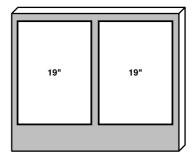
The cathode consists of a strip of conducting material on to which tiny cones (some 10,000 per pixel) are deposited. The cathode in this type of display fulfils the same function as the electron gun in a CRT. A potential of 200–800 V applied between the cathode and anode ensures that the phosphor is ignited to generate light.

The FED technology is new. Preproduction models are available to designers with aperture diagonals of 5–6 in.

THE CRT FIGHTS BACK So as to ensure their ruggedness (remember that there is a high vacuum inside), cathode ray tubes are curved at the front. This curvature causes some distortion in the picture and results in increased sensitivity to reflections in the glass.

Flat panel type CRTs have been around for some time, but only with small apertures. However, Sony's Trinitron[™], RCA's beam-guide CRT, and Mitsubishi's Diamondtron[™] that are now available in aperture diagonals of up to 50 in (full colour) are to all intents and purposes large size, flat panel CRTs. Moreover, the recently introduced Wega FD Trinitron[™] from Sony is a true flat panel CRT. Because of the frontal flatness of these CRTs, the picture can be seen at large viewing angles without loss of contrast or colour resolution. Moreover, the CRTs do not suffer from annoying reflections They have been available for





980020 - 15

Any size you want, as long as it is standard

In 1997, there were in the whole world only three factories producing the latest generation of glass substrates for liquid crystal displays (LCDs) in sizes 550×650 mm. As shown by Figure 5, this size substrate is ideal for the production of LCDs with an aperture of 12 in. The production of different (more particularly, larger) size substrates is not economically viable.

some time for use in good-quality television sets and computer monitors.

The development of the flat panel CRT over the past twenty-odd years has been one of overcoming a great many technical difficulties. One of these was the design of a rugged, mechanical construction able to withstand the large forces resulting from the high vacuum inside the tube. Such a large, heavy tube is difficult to manufacture, but is now produced from glass that is also used for automobile windscreens.

Another difficulty was the use by most manufacturers of a shadow mask or aperture grill that ensures correct division of the electron beam for the three primary colours.

Sony's Trinitron[™] uses a single electron gun with three cathodes aligned horizontally, an aperture grille, and vertically striped phosphors. The cathodes are tilted towards the centre so that the electron beams intersect twice, once within the electron lens focusing system and once at the aperture grille. This type of tube is therefore much lighter and cheaper to produce than three-gun tubes.

The accuracy with which the electron gun can focus the electron beam is of vital importance for the quality of the picture. New technologies have made it possible to modify the electron gun to such an extent that focusing is improved greatly. This means that the tube need not be made deeper. Moreover, the deflectors have been made larger, which further increases the accuracy of the beam. Other, smaller modifications ensure that the electron gun gives a sharp picture at the edges an in the corners of the tube, and minimizes any distortion resulting from spreading of the electrons in the corners.

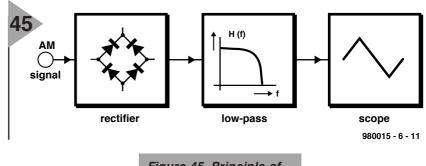
Other firms, such as Hitachi, Panasonic, LG, Mitsubishi and Samsung have also developed flat panel CRTs which will shortly be used in 17 in and 19 in computer monitors (and, of course, in smaller TV sets).

[980020]

introduction to digital signal processing

Part 6 – Modulation and demodulation

This sixth and final instalment deals with the subject of modulation and demodulation.



envelope demodulation.

Figure 45. Principle of



Before using the

programs on the ESPRESSO disk, copy the entire for der from the CD-ROM to the disk: th programs can then be run the hard disk. This procedure is explained in the README file on the -ROM

When copying a file or folder under Windows, its read-only setting is also copied. With many ESPRESSO programs, the read-only attribute causes an error report to appear, or graphics to disappear. This problem is solved by using the Explorer, selecting all files in the ESPRESSO folder on the hard disk, and clicking on file 'Properties'. Remove the check in the read-only box by clicking on it. Close by pressing OK, whereupon everything should function normally.

By Dr. Ing. M. Ohsmann

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ENVELOPE **DEMODULATION**

Amplitude modulated (AM) signals are most conveniently demodulated when their envelope is constructed, which is done by rectification of the signal and its subsequent filtering in a low-pass section - see Figure 45. For the demodulation of the AM signal introduced in Part 5, we use experiment file XDE-MOD3.SPP. The result is shown in Figure 46. The low-pass filtering is necessary to suppress any unwanted spectral components of the signal.

BBC REVISITED

The envelope detector may be used to demodulate the 198 kHz BBC signal (file BBC188. WAV) with a local oscillator (LO) frequency of 188 kHz, which results in an intermediate frequency (IF) of 10 kHz. This is done with file XDEMOD3.SPP, and the result is heard with the use of file TMP4.WAV. When we study the spectrum of file BBC188.WAV (experiment XDEMOD2B), we will note a peak at 10 kHz, which is the converted carrier (IF) of the signal, and a less pronounced peak at 5 kHz.

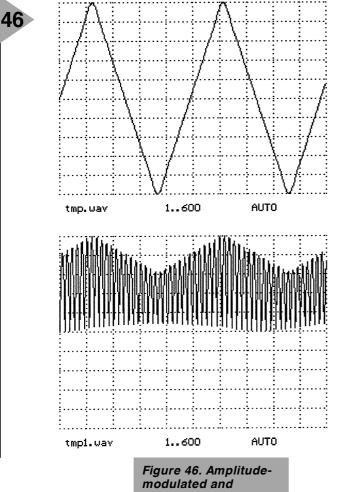
The weak spurious IF of 5 kHz results from the mixing of the LO signal with the carrier of Europa 1 (transmitting at 183 kHz). And, indeed, when file BBC188.WAV is demodulated

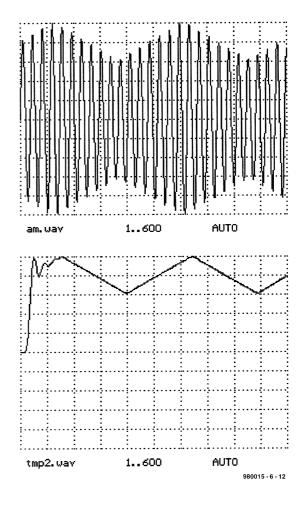
with a LO frequency that results in an IF of 5 kHz, Europa 1 will be heard (in French). A LO frequency that results in an IF of 19 kHz will also result in the reception of a broadcast transmitter at 207 kHz.

SYNCHRONOUS DEMODULATION

There are other means of demodulating an AM signal. In the discussion about amplitude modulation, it was seen that when a signal is multiplied with the sinusoidal output of a local oscillator (LO), the spectrum is shifted by the frequency of the LO. It is, therefore, possible to restore the original spectrum by a second multiplication. The corresponding experiment, XDE-MOD5.SPP is shown in Figure 47, and the result in Figure 48. If the LO signal is exactly the same as that used to modulate the original signal, that signal can be regained by multiplication and low-pass filtering (Figure 3 and Figure 4 top).

Should the phase of the LO signal be 90° out of phase with the carrier of the received signal, there would be no signal left after the low-pass filtering. It is, therefore, essential that the LO is in phase with the carrier of the AM signal. This is called synchronous or coherent demodulation. When the two frequen-





-demodulated signals.

cies are shifted in phase with respect to one

another, the 'in-phase' and '90° phase shift' states alternate in the rhythm of the frequency difference, resulting in a fluctuation of the volume of the audio signal. For that reason, when a coherent detector is used, the receiver requires a circuit, for instance, a phaselocked loop (PLL), to ensure that the frequency and phase of the LO signal are correct at all times. Although synchronous detection of amplitude modulated signals is complicated, it provides optimum results.

HIGH-RESOLUTION SPECTRUM ANALYSER

We have already seen that with the aid of an AM signal generator or by means of multiplication with a sinusoidal frequency the spectrum of a signal may be shifted. This principle is used in modern receivers to convert the input signal into an intermediate frequency (IF) signal. In a similar manner, it is possible to enhance the resolution of our spectrum analyser programme

carrier.

6/98

SPEC1. When the original signal is scanned at a rate of 22050 samples per second, using a DFT of 4096 samples, the result is an interval of 5.3833 Hz between adjacent samples. To be

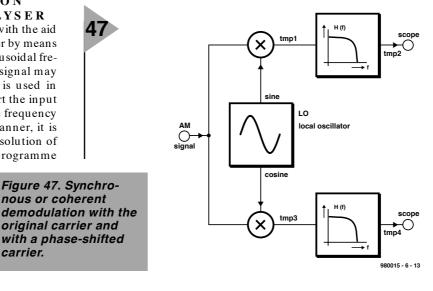
able to view a spectrum range more precisely, it

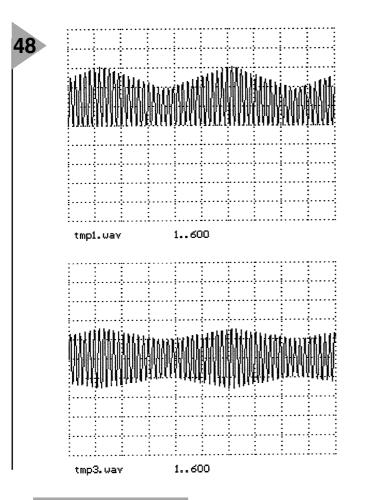
is possible to shift it into the low-frequency region and subject it to lowpass filtering and downsampling.

In practice, this will be be done in the following manner. To resolve signal WD1L.WAV at about 5 kHz, that is, to obtain a resolution of about 0.5 Hz with a DFT of 4096 samples, it is necessary to reduce the sampling rate of 22050 by a factor 10. At 2205 samples/s, it becomes possible to display signals at frequencies of up to 1.1 kHz. The 5 kHz signal from WD1L.WAV can be

shifted into this range when it is reduced to 300 Hz by mixing it with a frequency of 5.3 kHz.

If we start with 40960 samples, 4096 remain, and these resolve file XSPEC.SPP: the result is in Figure 49. The carrier and the two signals at its left and right (originally 57 kHz) are easily recognized. The signal at a distance of 125 Hz is the ARI signal which is switched on when there is travel news. The other signal, at 34.93 Hz from the carrier is the station identification signal that indicates in which region the transmitter whose signal has





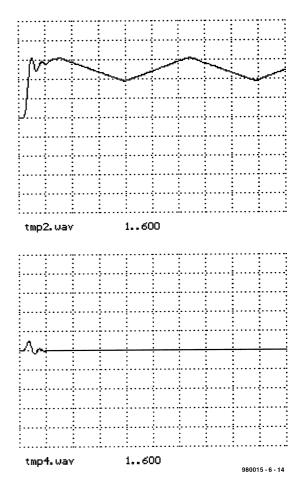


Figure 48. Top: coherent demodulation; bottom: synchronous demodulation with the local oscillator frequency shifted by 90°.

Figure 49. High defini-

tion spectrum of the

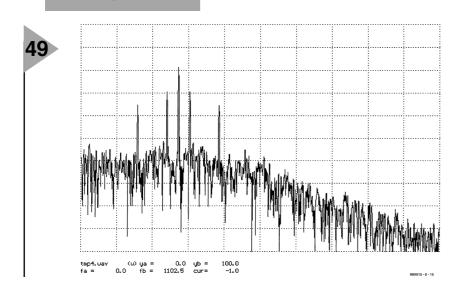
57 kHz subcarrier for

the ARI signal.

just been received is situated. By the way, when the first portion of the file WD1L.WAV is viewed, that is, when the message is not yet coming through, the 125 Hz peak will not be found, since the message recognition modulation is then not yet actuated.

QUADRATURE MODULATION AND DEMODULATION

The discussion on coherent demodulation showed that the phase of the local oscillator signal must be equal to that of the carrier frequency, and that if there is a phase shift between the



42

two, there is no output. This phenomenon may be made use of when an AM signal with sinusoidal carrier and a second carrier of the same frequency but cosine shaped are used. It is then possible to convey both signals via the same channel (Figure 50) and to demodulate them with suitable LO frequencies into their original shape. This is simulated in experiment XDEMOD4. SPP. In this, the first signal is a triangular one and the second, a sinusoidal one. Modulating processes that use sinusoidal and cosinusoidal carriers simultaneously are called quadrature processes. The main carrier and its constituents are normally identified by the letter I (In-phase) and the other with the letter Q (Quadrature).

RDS DETECTION

A practical application of quadrature demodulation is found in VHF and UHF radio. A car radio, for instance, is switched on or off when travel news is broadcast on a 57 kHz subcarrier. This is amplitude-modulated with an audio frequency of, say, 125 Hz when travel news is being broadcast. This is the I constituent.

Today, the same channel is used for the radio data system (RDS). To prevent the ARI and RDS signals affecting one another, the subcarrier for the RDS is 90° out of phase with the main carrier. This means that the RDS data are conveyed in the Q constituent. ExperiFigure 50. Composition

of a system for quadra-

ture modulation.

ment XRDS2.SPP simulates the ARI and RDS demodulator in **Figure 51**. The phase of the LO signal is normally controlled by a phase-locked loop (PLL) to ensure that it is correct with reference to the carrier. The demodulated signals may be seen in **Figure 52**. The upper signal represents the sinusoidal station identification signal (34.93 Hz, while the lower one shows the RDS signal.

F R E Q U E N C Y M O D U L A T I O N

In amplitude modulation, the modulating signal is shifted in the frequency band by the carrier. In frequency modulation, however, the modulating signal, s(t), modifies the frequency of the carrier. The transmitted signal is

 $\mathbf{y}(t) = \cos[2\pi f_{\rm C} t + \mu \mathbf{s}(t)].$

Strictly speaking, this treats frequency modulation as a variation of phase modulation. There is then no longer a simple connection for calculating the spectrum of the transmitted signal. Even with a sinusoidal signal, the spectrum soon becomes fairly complex:

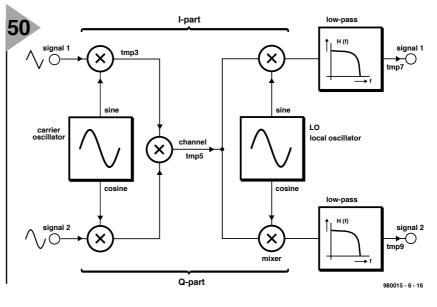
$$\mathbf{y}(t) = \cos[2\pi f_{\rm C} t + \mu \cos(2\pi f_{\rm M} t)].$$

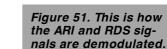
Figure 53 shows the spectra when the carrier frequency, $f_{\rm C} = 2000 \, \text{Hz}$, the modulating frequency, $f_{\rm M} = 100 \, \text{Hz}$ or 200 Hz, and $\mu = 2.4048$ or 4.0. It will be noted that single spectral frequencies occur at a distance $f_{\rm M}$ from the carrier. The carrier itself must not be present in the signal. The magnitude of the single frequencies may be calculated with Bessel functions. Note that the FM spectrum of a transmitted signal is wider than that of the modulating frequency. Although the audio bandwidth is only 15 kHz, the FM spectrum extends up to 150 kHz from the carrier. It is this aspect that makes an FM signal less vulnerable to interference, since the narrow-band interference affects only a small part of the FM spectrum. The requisite Carson bandwidth is calculated from the bandwidth and the energy of the modulating signal.

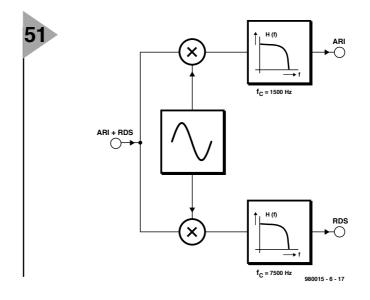
WARBLE SIGNAL

The CD-ROM accompanying the course contains an example of a simple FM signal with sinusoidal modulation. In Germany, ARD (Arbeitsgemeinschaft der öffentlich-rechtligen Rundfunkanstalten der Bundesrepublik Deutschland or, simply, Germany I) transmits a special signal to indicate the onset of travel news. This consists of a 2350 Hz carrier that is frequency modulated at 123 Hz with a modulation index of 1. See **Figure 54**.

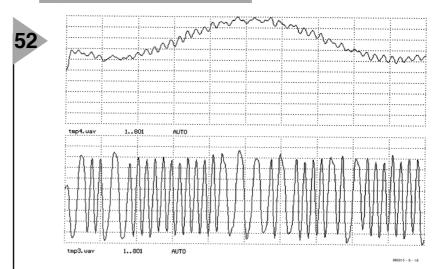
[This is, of course, of no interest to readers in the UK, where the BBC and Independent Radio Stations provide a

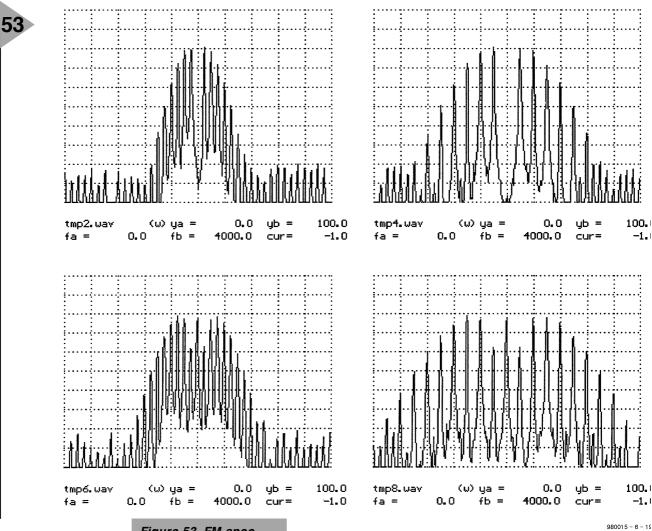












travel service under TP/TA and EON. When the traffic mode

is selected on a receiver, it will switch over to the local station when Travel

News is broadcast. Cassette or CD listening will also be interrupted, and typically the voluem of the set Figure 53. FM spectrum when the modulating signal is sinusoidal.

Figure 54. FM spec-

trum of the special

mitted in Germany

(warble) signal trans-

draw the driver's attention to the bulletin.When used in conjunction with EON, the TA/TP mode allows lis-

> tening to BBC National stations to be interrupted with travel reports for the area from BBC Local stations.

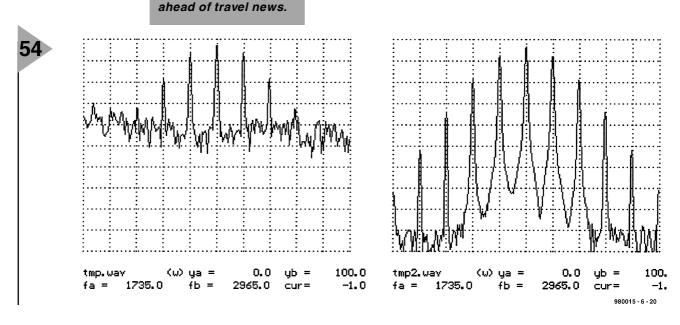
will increase a little to

EON – Enhanced Other Networks – provides a cross reference to other stations for the Travel Service, and other features.

Editor]

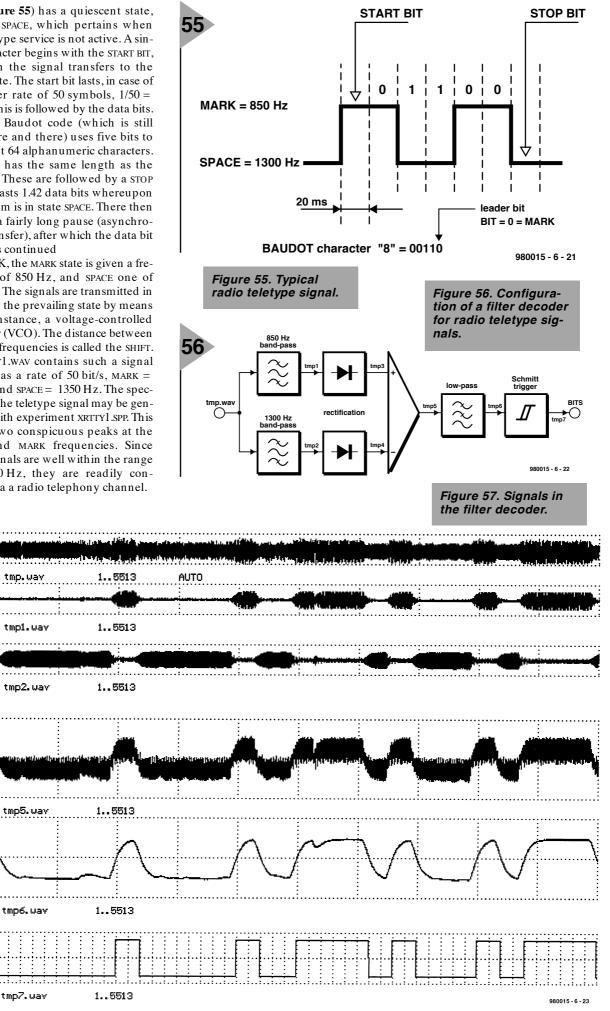
RADIO TELETYPE

The radio teletype service invariably uses frequency shift keying (FSK) to convey teletype signals. Such a signal

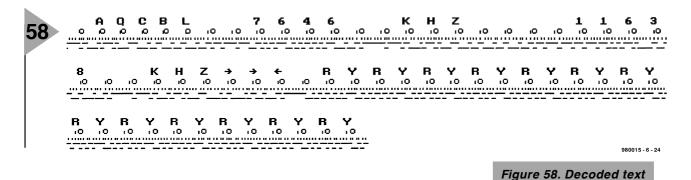


(see Figure 55) has a quiescent state, marked SPACE, which pertains when the teletype service is not active. A single character begins with the START BIT, at which the signal transfers to the MARK state. The start bit lasts, in case of a transfer rate of 50 symbols, 1/50 =20 ms. This is followed by the data bits. The old Baudot code (which is still used here and there) uses five bits to represent 64 alphanumeric characters. Each bit has the same length as the start bit. These are followed by a STOP BIT that lasts 1.42 data bits whereupon the system is in state SPACE. There then follows a fairly long pause (asynchronous transfer), after which the data bit stream is continued

In FSK, the MARK state is given a frequency of 850 Hz, and SPACE one of 1350 Hz. The signals are transmitted in line with the prevailing state by means of, for instance, a voltage-controlled oscillator (VCO). The distance between the two frequencies is called the SHIFT. File RTTY1.WAV contains such a signal which has a rate of 50 bit/s, MARK = 850 Hz and SPACE = 1350 Hz. The spectrum of the teletype signal may be generated with experiment XRTTY1.SPP. This shows two conspicuous peaks at the SPACE and MARK frequencies. Since these signals are well within the range 300-3400 Hz, they are readily conveyed via a radio telephony channel.







RADIO TELETYPE DECODING

An FSK-modulated signal may be decoded by a traditional filter decoder as shown in **Figure 56**; it has been done so in Experiment XRTTY6.SPP. The resulting waveforms are shown in **Figure 57**, while the decoded text is given in **Figure 58**. The preferred test text is the character string RYRYRYR since this contains the fastest bit conversion (XRTTY5.SPP).

FINALLY

Although this is the end of the six-part course, there are a number of aspects that, owing to shortage of space, have not been discussed. Experiments relevant to some of these are listed in the box and contained on the CD-ROM accompanying the course. The title of the disk (see Readers Services towards the end of this issue) is ESPRESSO, an acronym for *E*lektor Electronics Signal *PR*ocessing *Experiments* and *Simula*tion *SO*ftware. With the knowledge gained by the course, readers will be able to conduct these experiments without further discussion. Nevertheless, a small help programme is contained in file EXPS.DOC.

[980015-6]

Additional experiments on the CD-ROM Single-sideband generation Filter method and phase method Single-sideband demodulation

of a radio teletype sig-

nal.

Phase modulation AMDS BBC Terrestrial meteorological broadcasts Satellite meteorological broadcasts Time signal broadcasts DTMF (dual tone multiple frequency)

Elektor Electronics

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discharge circuit

for 1.2 V sintered NiCd batteries

Developments in the world of rechargeable batteries, and the new models that have appeared in recent years, such as the metal hydride battery and the lithium-ion battery, are mainly of interest in the electronics industry. Many experimenters, hobbyists and other amateurs have stuck to NiCd cells and batteries, which have now been with us since the 1950s. The main reason for this popularity is probably their user-friendly behaviour (which is



exceeded only by sealed lead-acid batteries). Another factor in favour of the NiCd battery is its low internal resistance (at least as far as sintered types are concerned), which enables it to provide fairly large currents (but not as high as lead-acid batteries).

> The nickel-cadmium battery is mechanically rugged and long-lived. It has excellent low-temperature characteristics and can be hermetically sealed. Cost, however, is higher than for the lead-acid or nickel-zinc battery. In many applications, the use of a sealed lead-acid battery is to be preferred over the other two types.

> A slight drawback of a sintered NiCd battery is its so-called memory effect, which is fortunately completely reversible. It should be noted that mass plate nickel-cadmium cells and batteries do not develop the memory effect in

any circumstances. The present circuit is, therefore, primarily intended for use with sintered NiCd 1.2 V cells.

LOW INTERNAL RESISTANCE

The ability of NiCd batteries to provide fairly large currents (because of their low internal resistance – at least as far as sintered types are concerned) is an important factor for the amateur fraternity, since many home-made model units draw fairly large currents. As a comparison, the d.c. resistance of three types of fully charged 1 Ah, 1.2 V

Design by K Walraven

sealed cell is

```
Standard110 \text{ m}\Omega/\text{cell}Heavy duty50 \text{ m}\Omega/\text{cell}Sintered19 \text{ m}\Omega/\text{cell}
```

E N V I R O N M E N T A L E F F E C T S

One of the most serious drawbacks of NiCd batteries is their effect on the environment. This type of battery contains cadmium which is toxic. In most countries, discarded NiCd batteries are dumped on the rubbish heap where they remain toxic for a very long time. It is true, of course, that their life of some 500–800 charge/discharge cycles does not cause millions of them to be disposed of on the rubbish heap. Nevertheless, this was a very important factor in the decision of manufacturers in general to discontinue the use of NiCd batteries in most consumer products.

MEMORY EFFECT

Another disadvantage of sintered (not mass plate) NiCd batteries is, as already mentioned, their memory effect. This manifests itself in the cell retaining the characteristics of previous cycling. That is, after repeated shallowdepth discharges the cell will fail to provide a satisfactory full-depth discharge. Note, however, that Eveready cylindrical nickel-cadmium cells are particularly noted for their lack of memory effect.

The memory effect is a nuisance, because it means that a battery with a nominal capacity of, say, 600 mAh, after a number of charge/discharge cycles has a useful capacity of only 300 or 400 mAh. This has nothing to do with the life of the battery: even a new battery if charged as stated will soon lose part of its capacity.

Fortunately, this reduction in capacity can be prevented fairly simply. Moreover, batteries that already suffer from the memory effect can be restored to their nominal capacity. The cure is simply to ensure that a battery is occasionally fully discharged before it is recharged. Occasionally means before every third or so recharge. Note that there are chargers on the market that have the discharge facility built in, but this will certainly not be the case in the less expensive types.

C O R R E C T D I S C H A R G I N G

There is no need for extensive circuitry to discharge a battery: a simple resistor or light bulb will accomplish it readily. It is, however, necessary to keep an eye on the discharge time, because otherwise there is the risk that the battery is discharged beyond a certain voltage. When this happens, it may cause polarity reversal in the cells comprising the battery.

Correct discharging can only take place via a circuit that arranges for the battery to be discharged to a certain level and then disconnects it from the discharge circuit.

The diagram of such a circuit – see **Figure 1** – is pretty straightforward. Nevertheless, such a discharge circuit does the job correctly. It causes a battery to be discharged to a level of 650 mV. This level ensures that the battery is correctly discharged without the risk of polarity reversal. The battery is not discharged at a constant current, but in short bursts. This allows the battery to 'recover' during the intervals, which, in practice, has been found to extend its useful life.

During the discharge, an LED lights to show that the process is continuing. Since the diode cannot work from a voltage of 0.65–1.2 V, the voltage has to be raised. To this end, the astable multivibrator formed by T_1 and T_2 oscillates at a rate of 25 kHz. When T_2 is on, current flows through inductor L_1 , so that energy is stored in the magnetic field. When T_2 is off, the inductor is 'discharged' via the LED, whereupon this lights.

Diode D_1 prevents the energy stored in the inductor from leaking away via the base of T_1 . This might happen because the capacitors in the circuit have fairly high values, whereas the resistors have low ones. The chosen values ensure that the discharge current is sufficiently high. When the battery voltage is 1.2 V, the discharge current is some 200 mA; at 0.8 V, it has dropped to about 100 mA, and at 0.65 V to around 50 mA. When the battery voltage drops to 0.65 V, the discharge process is discontinued.

CONSTRUCTION

The tiny circuit is best built on the printed-circuit board shown in **Figure 2**, but this is not available ready made. However, a small prototyping board will do very nicely as well.

Inductor L_1 is a small choke which should be readily available from most electronics retailers.

The LED should be a high-efficiency type, while, because of the threshold discharge voltage, D_1 must be a Schottky type.

USAGE

There is not much that can be said about using the discharge unit. It is simply a matter of connecting the 1.2 V battery with correct polarity, checking that the LED lights, and disconnecting the battery when the LED goes (or is) out.

In general, the discharge period will normally be three to four hours. As mentioned before, the battery does not need to be discharged fully before it is recharged: before every third recharge

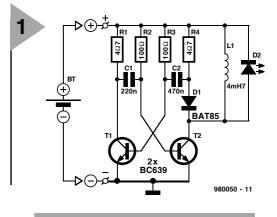


Figure 1. The circuit is basically an astable multivibrator oscillating at a rate of 25 kHz.

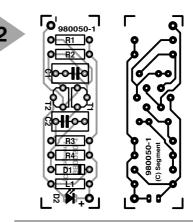


Figure 2. The discharge circuit is intended for 1.2 V batteries. If several of these, or a 9 V rechargeable NiCd battery, have to be discharged, an appropriate number of PCBs are needed.

Parts list

 $\begin{array}{l} \textbf{Resistors:} \\ \textbf{R}_1, \, \textbf{R}_4 = 4.7 \; \Omega \\ \textbf{R}_2, \, \textbf{R}_3 = 100 \; \Omega \end{array}$

Capacitors: $C_1 = 0.22 \,\mu\text{F}$

 $C_2 = 0.47 \,\mu\text{F}$

Inductors:

 $L_1 = choke, 4.7 mH$

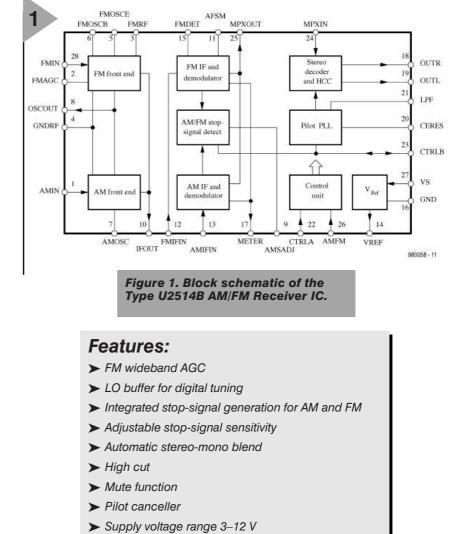
 $\begin{array}{l} \textbf{Semiconductors:}\\ \textbf{D}_1 = BAT85\\ \textbf{D}_2 = LED, \text{red, high efficiency}\\ \textbf{T}_1, \textbf{T}_2 = BC63 \end{array}$

will be fine.

If a battery is suspected of suffering from the memory effect, discharge and recharge it two or three times in succession. This action will in almost all cases restore the capacity of the battery completely (commensurate with its life, of course).

AM/FM Receiver IC

for digital tuning



PIN DESCRIPTION

The FM preamplifier input, FMIN (pin 28) – see the block diagram in **Figure 1** – consists of a transistor grounded-base circuit that provides excellent noise performance and large signal behaviour. It is recommended to connect a source impedance of 100 Ω to achieve optimal performance. The direct current through the amplifying transistor is reduced by the internal automatic gain control (AGC). This means that in the case of large input

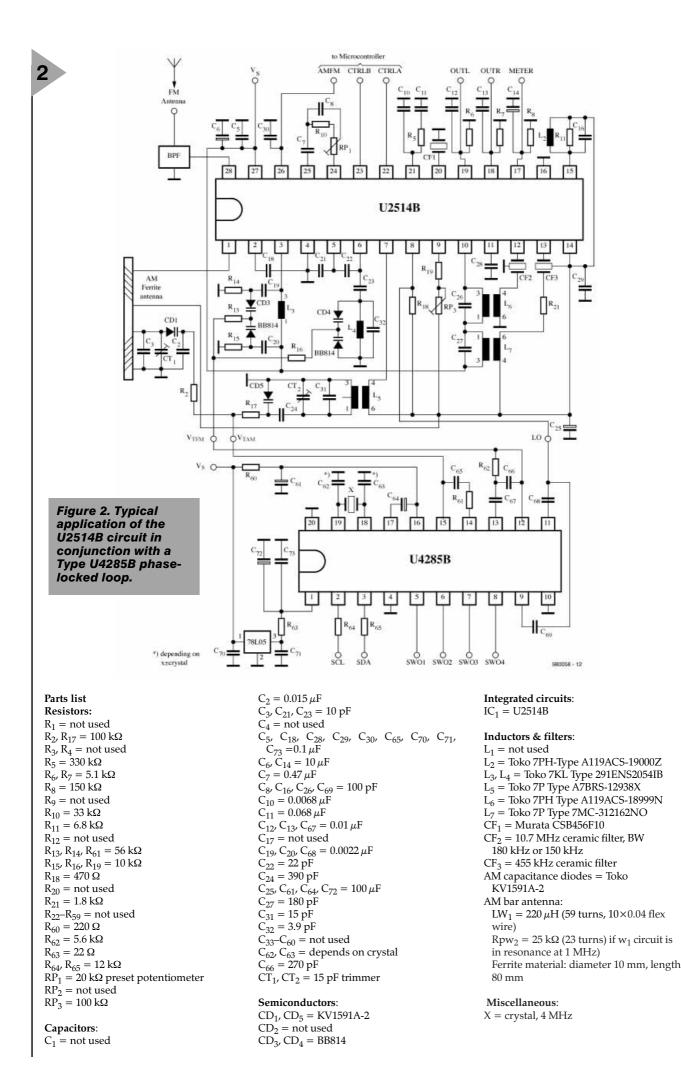
signals the input alternating current is bypassed via the wideband AGC transistor. A capacitor (C_{18} in **Fig-ure 2**), is connected between pins 2 (FMAGC) and 4 (GNDRF) to smooth the AGC voltage and to shorten the transistor base to ground (pin 4). A tuned r.f. (radio frequency) circuit is connected between pins 3 (FMRF) and 27 (vs). The amplified r.f. signal is fed internally to the mixer input.

The FM local oscillator consists of a transistor in a grounded-collector con-

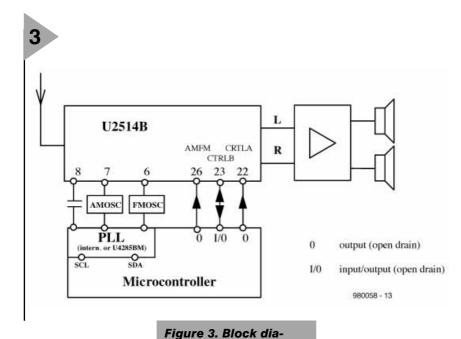
The content of this note is based on information received from manufacturers in the electrical and electronics industries or their representatives and does not imply practical experience by Elector Electronics or its consultants.

The U2514B is an integrated bipolar radio circuit suitable for digital tuning systems. It contains an FM front end with preamplifier and FM stereo decoder as well as a complete AM receiver and demodulator. Stopsignal generation is implemented for FM and AM mode. The circuit is designed for use in small radios, power packs and multimedia applications.

> A Telefunken Semiconductors Application



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gram showing the

a microcontroller.

figuration. The negative resistance at the base of the transistor is

generated by an external capacitor (C_{21} in Fig-ure 2) between pins 5 (FMOSCE) and 4 (GNDRF). Another external capacitor (C_{22} in Figure 2) is connected between pins 6 (FMOSCB) and 5 (FMOSCE) to increase the resistance at the emitter and to lead to a higher oscillator swing. The negative resistance at pin 6 is about 250 Ω . Consequently, the resonant LO (local oscillator) tank resistance of about $5 k\Omega$, which depends on the Q(uality) factor of the coil, is transformed to this magnitude via a capacitor.

A resistor (R8 in Fig. 2) is connected between pins 8 (OSCOUT) and 14 (VREF) which determines the amplitude of the oscillator voltage that is fed to the PLL (phase-locked loop) circuit. The Telefunken U428xBM family of PLL circuits is recommended as members of this family offer a high signal-to-noise ratio and low current drain.

The AM antenna coil is connected between pins 1 (AMIN) and 14 (VREF). To ensure that the AGC operates correctly, a coil impedance of about $25 \text{ k}\Omega$ is required. The AM oscillator must be loaded by an external tank referred to VREF

The IF output (IFOUT - pin 10) of both the AM and the FM mixer has to be loaded into external IF tank circuits referred to VREF. The Q-factor of the IF coils must be not lower than 50 Ω .

The ceramic resonator of the stereo decoder PLL circuit is used as a stop-signal detector for AM signals. For this purpose, the parallel resonance frequency of the resonator, which, unloaded, is about 456 kHz, is reduced by an internal load capacitor to 455 kHz. It is important that the AM IF is 455 kHz. The internal loading capacitor is defined by the current through pin 9

U2514B interfaced with (AMSADJ) to ground. An external resistor

(R₁₉-RP₃ in Fig. 2) between pins 9 (AMSADJ) and 14 VREF) permits the alignment of the stop-signal centre frequency. The width of the stop window is typically 1.2 kHz. If AM search mode is not actuated, the pin is pulled to ground internally.

The input impedance of the AM IF amplifier is $3.3 \text{ k}\Omega$ in accordance with to the required impedance of most ceramic filter. The input refers to VREF (pin 14).

The input impedance of the FM IF amplifier is 330 Ω in line with the required impedance of most FM ceramic filters. The input refers to GND (pin 16).

A tank circuit (L₂-R₁₁-C₁₆ in Figure 2) is connected between pins 15 (FMDET) and 14 (VREF). The discriminator coil must be adjusted so that the voltage at pin 11 (AFSM) is 1.2 V at 10.7 MHz to ensure that the FM stop signal is generated correctly.

A capacitor (C₂₈ in Figure 2) is connected between pins 11 (AFSM) and GND for smoothing the FM audio output. As the deviation of the FM signal (max. 75 kHz) might be greater than the stop-signal window (42 kHz), FM audio output smoothing is necessary to generate a modulation-independent stop signal. In AM search mode, C₂₈ smoothes the FM demodulated AM IF signal.

The METER pin (17) is driven by a current that corresponds to the level of the FM IF or AM IF signal. The required external load consists of parallel network R_8 - C_{14} (see Figure 2). The voltage at this pin controls the high cut and mono/stereo blend function in the reception mode. These functions may be modified by the designer by choosing different values of the load resistor.

The reception mode, search mode,

mute function, and search sensitivity, are selected by applying a control voltage to pin 22 (CTRLA). If this voltage is higher than 800 mV, the receiver circuit is in the reception mode, otherwise in the search mode. When the voltage is between 800 mV and 1.3 V, the audio frequency (AF) level at pins 18 and 19 (OUTR and OUTL respectively) is reduced (mute function). In the search mode (0-700 mV), the voltage level determines the degree of the search sensitivity.

The signal at pin 23 (CTRLB) indicates stereo or mono reception: stereo if the voltage is higher than 1.2 V, otherwise mono. Furthermore, it is possible to force the receiver circuit to mono by applying an external voltage <800 mV to pin 23. If the search mode is selected, the low active stop signal appears at pin 23. If output CTRLB is applied directly to the I/O port of a microcontroller, its high level must be adapted by linking pin 23 to ground via a suitable resistor.

An internal voltage regulator generates a stable reference voltage of 2.4 V, which is needed for all function blocks of the IC. An external capacitor $(C_{29} \text{ in Figure 2})$ must link pin 14 to ground in order to achieve stability and noise suppression.

When pin 26 (AMFM) is linked to ground, the receiver circuit is switched to the AM mode; if the pin is open, the FM mode is selected. Switching between these two states may be performed by a microcontroller with open-drain I/O ports. A capacitor (C₃₀ in Figure 2) must be connected between AMFM and ground for FM mode operation. It serves for smoothing the control voltage of the pilot canceller.

A ceramic resonator of 456 kHz parallel resonance frequency (at 30 pF onchip load capacitance) is connected between pin 20 (CERES) and ground (necessary for the pilot regeneration). It should be mounted very close to pin 20 to avoid spurious radiation. In AM $(V_{AMFM} < 1.1 V)$ search (V_{CTRLA}<800 mV) mode, the resonator is used for stop-signal generation. The parallel resonance frequency is then reduced to 455 kHz by adjusting the current into pin 9.

A phase-locked loop (PLL) circuit is used for the pilot regeneration of the stereo decoder. Therefore, a loop filter formed by network R5-C10-C11 is connected between pin 21 (LPF) and ground.

The multiplexed signal is applied to pin 24 (MPXIN) and thence fed to the stereo decoder. The input resistance at this pin is about 10 k Ω . It is recommended to align the channel separation by an RC network between MPXIN and MPXOUT (pin 25) owing to tolerances in the group delay of the IF filter.

| Pin | Symbol | Function | AM | FM |
|-----|--------|--|--|------------------------------------|
| 1 | AMIN | AM antenna input | V _{Ref} | High impedance |
| 2 | FMAGC | FM AGC time constant | V _{Ref} | V _{Ref} – 80 mV |
| 3 | FMRF | FM RF tank | High impedance | V _S / 0 to 1 mA |
| 4 | GNDRF | Ground RF | GND | GND |
| 5 | FMOSCE | FM oscillator emitter | $V_{Ref} - 2 \times V_{BE} / 0 A$ | 0.95 V |
| 6 | FMOSCB | FM oscillator base | V _{Ref} – V _{BE} / 0 A | 1.7 V |
| 7 | AMOSC | AM oscillator | V _{Ref} /0.3 mA | High impedance |
| 8 | OSCOUT | Buffered AM/FM oscillator output | V _{Ref} /0.3 mA | V _{Ref} /0.7 mA |
| 9 | AMSADJ | Current input for AM stop-signal adjustment | AMsearch=V _{BE} , AM=0.1 V | 0.1 V |
| 10 | IFOUT | AM/FM IF output | V _S /in 50 μ A | V _S /in 0.4 mA |
| 11 | AFSM | AF smoothing | 0.8 to 1.2 V | 1.2 V |
| 12 | FMIFIN | FM IF amplifier input | V _{BE} to GND/ 0 A | V _{BE} to GND |
| 13 | AMIFIN | AM IF amplifier input | 3.3 kΩ to V _{Ref} | 3.3 k Ω to V _{Ref} |
| 14 | VREF | Reference voltage input | $V_{Ref} = 2.4 V$ | $V_{\text{Ref}} = 2.4 \text{ V}$ |
| 15 | FMDET | FM discriminator | V _{Ref} /1 µA | V _{Ref} /0 A |
| 16 | GND | Ground | GND | GND |
| 17 | METER | Field-strength output | 0 to 2,3 V | 0 to 2 V |
| 18 | OUTR | AF output right | 0 to 2.3 V/0.15 mA | 0 to 2.3 V/0.15 mA |
| 19 | OUTL | AF output left | 0 to 2.3 V/0.15 mA | 0 to 2.3 V/0.15 mA |
| 20 | CERES | Ceramic resonator 456 kHz for AM search and for pilot-PLL in FM mode | 0,1 to 2.3 V | 0.1 to 2.3 V |
| 21 | LPF | Low-pass filter for pilot-PLL AM | 0.2 V | - |
| 21 | | Low-pass filter for pilot-PLL AM search and FM | 0.5 to 2 V | 0.5 to 2 V |
| 22 | CTRLA | Control input for mute, search mode and search sensitivity | 0 to V _{Ref} | 0 to V _{Ref} |
| 23 | CTRLB | Control input for forced mono, Control output for stop function, Mono/stereo information | 0.1 V to V_S ,30 k Ω | 0.1 V to V_S, 30 k Ω |
| 24 | MPXIN | Stereo decoder MPX input | 0.8 V | 0.8 V |
| 25 | MPXOUT | AM/FM MPX output | 0.8 to 1,2 V | 1.2 V |
| 26 | AMFM | AM/FM switch and pilot canceller time constant | GND | 1.54 V |
| 27 | VS | Supply-voltage input | 3 to 12 V/in 5 mA | 3 to 12 V/in 9 mA |
| 28 | FMIN | FM antenna input | V _{Ref} – V _{BE} /0 A | 1.5 V |

To drive both the compensation network to pin 24 and an optional RDS (radio data service), the output impedance at pin 25 (MPXOUT) is low. The direct voltage is 1.2 V in FM mode (depending on the discriminator coil alignment) and 0.8–1.2 V in the AM mode (depending on the signal level).

The open-collector output at pins 18 and 19 (OUTR and OUTL respectively) requires and external resistor to ground (R_7 and R_6 in Figure 2 respectively). The deemphasis may be achieved by an additional parallel capacitor (C_{13} and C_{12} respectively).

FUNCTIONAL DESCRIPTION

In the FM mode, the antenna signal is fed via a tuned r.f. circuit to the integrated pre-stage, which consists of a transistor grounded-base circuit. To protect the pre-stage against overload, an automatic gain control (AGC) is included on the chip.

A tuned r.f. circuit on the collector is necessary for amplifying and filtering the FM signal, which is fed internally to the mixer. It consists of a double-balanced Gilbert Cell.

The local oscillator (LO) signal is generated by an integrated oscillator. The buffered LO signal is used to drive a PLL. THE IF signal (10.7 MHz) is coupled out at the mixer's output and fed via a ceramic filter to the demodulator. The demodulated audio signal is available at pin 25 (MPXOUT)

In the AM mode, the signal is fed directly to the mixer. The antenna impedance must be higher than $25 \text{ k}\Omega$ to ensure correct operation of the level control in case of large signals. The LO signal is generated by an integrated oscillator. The buffered LO signal is used to drive the PLL. If the AM search mode is required, the IF must be 455 kHz. The IF output is fed via a ceramic filter to the demodulator. The demodulated audio signal is available at pin 25 (MPXOUT).

When a control voltage is applied to pin 22 (CTRLA), the mode of the receiver may be selected.

The search mode is selected when the control voltage is <800 mV.

The search sensitivity may be selected by varying the control voltage in the range 100–800 mV. When the control voltage is 100 mV, the highest sensitivity is achieved.

In the reception mode, muting is possible by varying the control voltage in the range 0.8–1.4 V. When the control voltage is 0.8 V, the highest mute depth is achieved.

The output at pin 23 (CTRLB) indicates whether the receiver is operating in the stereo or mono mode. When the control voltage applied to pin 23 <1.1 V, the receiver is forced to mono.

In the search mode (V_{CTRLA} < 0.8 V), the internally generated stop signal is available at pin 23 as a low active signal.

If both conditions

for AM: V_{METER}>V_{CTRLA}

for FM: V_{METER} (90/R₈) > V_{CTRLA}

and

 $1.1 \text{ V} < \text{V}_{\text{AFSM}} < 1.3 \text{ V}$

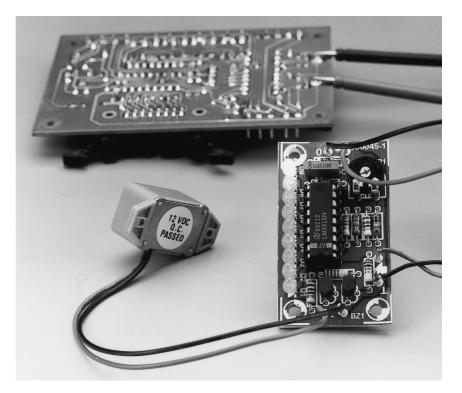
- for AM: current adjust into pin 9 for $f_{pin 20} = 455 \text{ kHz}$
- for FM: detector coil adjust to $V_{pin 11} = 1.2 V$ for 10.7 MHz

are fulfilled, a stop signal is generated. [980058]



conductance tester

with buzzer or LED indication



Arguably, one of the most useful gadgets in a small workshop is a continuity tester which enables the rapid checking of whether a conductor or circuit is open-circuited or short-circuited. It normally uses a buzzer to indicate a short-circuit (that is, a continuity in the conductor or circuit). Such a device is improved considerably if it is given a means of showing the order of resistance between the two probes when the buzzer remains quiet. This quickly solves the question of 'is it a bad contact?' or 'is it a break in a cable?', and so on. The simple indication provided in the present tester shows at a glance the relative magnitude of the resistance between the two probes.

INDICATOR

For a rough indication of a measured value of resistance (or its reciprocal, conductance) a liquid-crystal display (LCD) or other fairly expensive indicator is not necessary, and in the present tester the indicator is formed by a number of light-emitting diodes

(LEDs). These are driven by the wellknown display driver IC Type LM3915. This circuit is designed specifically to display the value of an analogue voltage via a row of LEDs.

The LM3915 contains a reference voltage source and an accurate decadic potential divider. The voltages at the taps of this divider are applied to a series of comparators. These comparators are driven sequentially in line with a rising input to the IC. The comparator outputs can drive an LED directly. The row of LEDs may be set to the dot or bar mode. The brightness of the diodes can also be adjusted in accordance with individual needs.

One of the attractions of the LM3915 is that it requires relatively few external components (other than the LEDs). The high-impedance input circuit of the IC accepts signals at levels from 0 V to 1.5 V below the supply voltage. Provided that the input signals do not exceed $\pm 35 \text{ V}$, there is no need for an external protection circuit. The input voltage is indicated in 3 dB steps.

The conductance tester goes one step further than the usual continuity tester found in so many workshops. It contains a buzzer to indicate a very low resistance between two points along a conductor or circuit and an LED display to show the order of resistance between these points when the buzzer does not sound.

Design by L. Koch

R E S I S T A N C E M E A S U R E M E N T

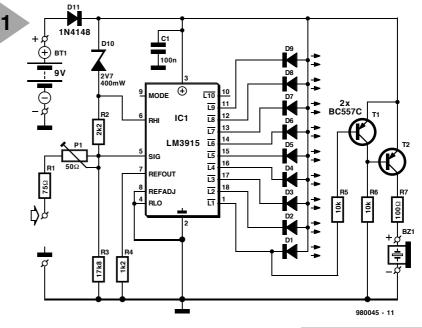
Since the LM3915 is designed for indicating voltages, and the present circuit is intended for measuring conductance (or its reciprocal, resistance), a means has to be devised to convert voltage into ohms or siemens. In the present circuit, this is done by placing an additional potential divider at the input of the LM3915 and ensuring that the division ratio is influenced by the magnitude of the resistance between the test probes.

In the circuit diagram of the tester in **Figure 1**, the external potential divider at the input of IC₁ is formed by D_1 , R_2 and R_3 . The resistance, if any, between the test probes is connected in parallel with R_3 via resistor R_1 and preset P_1 . This means that this resistance affects the division ratio of the divider, and thus the signal applied to pin 5 of IC₁.

The design arranges for resistance values of 10Ω to $7.5 \text{ k}\Omega$ to be indicated in seven 3 dB steps by the sequential lighting of D₂–D₉. The first diode, D₁, lights when the resistance is lower than 10Ω ; this level may be preset to 0Ω (that is, full conduction) with P₁.

Transistors T_1 and T_2 in parallel with D_1 ensure that in case of very low resistance between the test probes only D_1 lights and that the buzzer, Bz_1 , is energized.

The diagram in Figure 1 shows IC_1 configured for the dot mode, which keeps the current drain low. This is



effected by leaving pin 9 (MODE) of the IC open. If the bar mode is wanted, pin 9 must be linked to pin 3.

CONSTRUCTION

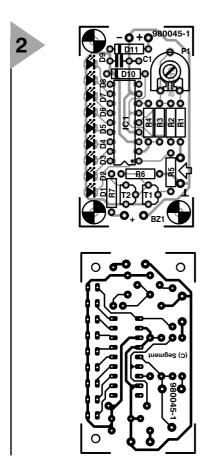
The tester must, of course, be as compact as possible so that it can be carried about in one's pocket. Consequently, the printed-circuit board for it (see **Figure 2**) is small. Building the tester on this board is simplicity itself, as is wiring it up. There are only three connections to be made: two for the probes (arrows), two for the b u z z e r (Bz_1) , and two for the power supply.

Figure 1. The circuit diagram of the conductance tester is an example of simplicity.

The tester is best powered by a 9 V battery. Since the current drain of the circuit is at most 30 mA (with buzzer sounding), an alkaline-manganese battery should last about a year in normal use.

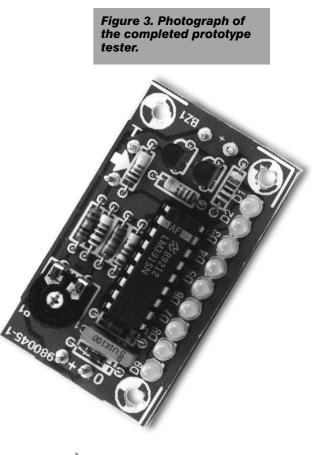
The tester, complete with battery, is best housed in a small plastic case.

[980045]



Parts list **Resistors:** $R_1 = 75 \Omega$ $R_2 = 2.2 k\Omega$ $R_3 = 17.8 \text{ k}\Omega$ $R_4 = 1.2 \text{ k}\Omega$ $R_5, R_6 = 10 \text{ k}\Omega$ = 100 Ω $P_1 = 47 \text{ k}\Omega$ preset potentiometer Capacitors: $C_1 = 0.1 \, \mu F$ Semiconductors: $D_1 - D_9 = LED, 3 mm$ D_{10} = zener diode 2.7 V, 400 mW $D_{11} = 1N4148$ $T_1, T_2 = BC557C$ Integrated circuits: Bz₁ = buzzer, 12 V $Bt_1 = 9 V$ battery with connecting clip 2 off test probes

> Figure 2. The printed-circuit board for the conductance tester is not available ready made.



Field Programmable Analogue Array

MPAA020 from Motorola

The MPAA series of **Field Programmable** Analog Arrays from Motorola is a new family of products that have programmable analogue building blocks that can be configured to create circuit functions that solve real-world signal processing problems. When used with supporting CAD tools and macro library functions, these products allow the user to address analogue circuit design problems with low risk and minimum analogue expertise.

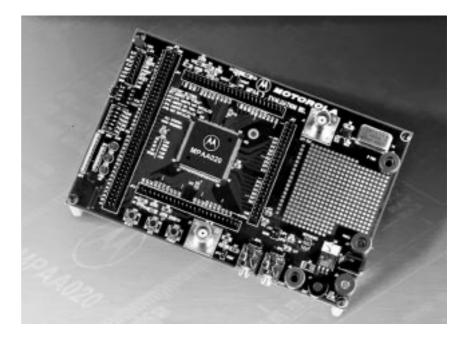
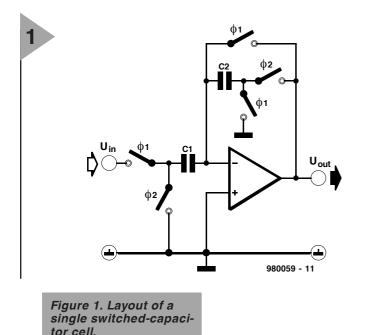


Table 1. Performance specifications of the MPAA020

| Specification | Typical Value |
|---|------------------------------|
| System Master Clock Frequency (clock) Internal Sampling Clock Pate | TBD 1 MHz (max.) |
| Maximum Signal Frequency Recommende Maximum Signal Frequency Nyquist | 200 kHz 500 kHz |
| Input Signal Range | 0.5 V to (Vdd – 0.5V) |
| Analog Output Drive | 100 pF (max.) 1 kΩ (min.) |
| DC Offset | < 10 mV |
| Harmonic Distortion 1 kHz Harmonic Distortion 200 kHz | < 0.1 % < 0.5 % |
| Differential Non-Linearity | < 0.15 LSB |
| Integral Non-Linearity | < 0.24 LSB |
| Slew Rate | 10 V/ms |
| Signal to Noise Ratio (SNR) | > 60 dB |
| Power Supply Rejection Ration (PSRR) | TBD |
| Power Dissipation (max.) Each cell individually selectable | 200 mW (10 mW/cell) |
| Operating Temperature Range | -40 to + 85 °C |

Topology: (1) study of geometrical properties and spatial relations unaffected by continuous deformation, such as twisting or stretching. Mathematical approaches employing topology are of great importance in modern theories of the four fundamental interactions (gravitational, electromagnetic, weak and strong); (2) in electronics: generic circuit structure or collection of working structures.

By M Kupfner



The first available Field Programmable Analog Array, the MPAA020, is an 'electronic breadboard' that provides an ideal medium for quickly designing, debugging, and implementing a wide array of analogue circuits, thereby

reducing development cycle times. Additionally, the analogue arrays, when used with Motorola's MPA series of field programmable gate arrays (FPGA), allow the user to implement field programmable mixed-signal designs, using the products and software from each of the individual FPGA technologies. This mixed-signal design capability extends the user's flexibility even further by providing the capability to simultaneously design, debug, and implement, both the analogue and digital aspects of a system topology.

APPLICATIONS

Motorola's field programmable arrays can be used in a wide variety of applications. The first analogue array products are aimed at industrial motion, process, and power control applications. Additional applications to which the analogue arrays are suited include communications (low to medium frequency applications), process control (temperature, heating and cooling systems, pressure control, and so on), automotive, and medical instrumentation, and measurement systems.

A N A L O G U E T E C H N O L O G Y

The technology for Motorola's field programmable analogue array is based on switched capacitor (SC) technology. The MPAA020's switched capacitor circuit topology (see box) is designed to be insensitive to parasitic capacitances; consequently, arbitrary signal routeing is possible with minimal loss in signal integrity caused by these parasitics.. Also, since the capacitors are integrated on silicon, the capacitance ratios are tightly matched, allowing precise ana-

logue signal processing without the need for calibration or feedback. Analogue resources in the MPAA020 are contained in configurable analogue blocks (CABs) that incorporate a switched-capacitor CMOS op amp, comparator, capacitor arrays, CMOS switches, and SRAM (static RAM). Data stored in SRAM control the switches that program various capacitance values (static and dynamic) in the input and feedback signal paths of the op amp. Analogue functions such as programmable gain stages, adders, subtractors, rectifiers, sample&hold circuits, and first-order filters can be implemented in a single cell (CAB). Higher level functions, such as biquad filters, PLLs (phase-locked loops), level detectors, and so on, can be implemented using two or more cells.

SC TECHNOLOGY IN THE MPAA020

Switched-capacitor cells are invariably implemented in quantity in an integrated circuit. The layout of a single cell is shown in **Figure 1** (which, by the way, is a macro contained in the EasyAnalogTM software).

The clock (switching) phases of the cell are designated Φ_1 and Φ_2 , and the capacitors C_1 and C_2 . The amplification, α , of the cell is, as in a standard configuration, $\alpha = C_1/C_2$.

In accordance with Shannon's theorem, the clock frequency, $f_{\rm clk}$, must be at least twice the highest frequency occurring in the signal, $f_{\rm sig}$. If this condition is not met, aliasing effects will occur. In the MPAA020, the clock frequency is 1 MHz max, which means that the signal frequency must not exceed 500 kHz – in practice, 200 kHz.

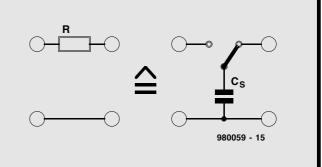
ARCHITECTURE

The MPAA020 contains 41 op amps, 100 programmable capacitors, and 6864 switches. The switches control circuit connectivity, capacitor values, and other selectable features. The array is

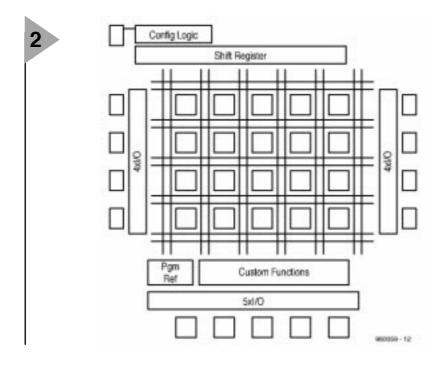
switched-capacitor basics

In switched-capacitor (SC) technology, a resistance is replaced by a switched capacitance. The current through a resistance, and thus through a switched capacitor, is directly proportional to the voltage, U, applied across the resistance.

If, in the diagram, the switch is as shown, the capacitor, C_s , is charged to a charge $Q = UC_s$. When the switch is in the other position, the capacitor is discharged. The process of the capacitor being charged and discharged continuously results in an average current $I = UC_s/T_s$, where T_s is one charge/discharge cycle, that is, $1/f_s$ (f_s is the switching frequency). Substituting f_s for $1/T_s$ gives $I = UC_s f_s$. In analogy to Ohm's law, I = U/R, it follows that $R = 1/C_s f_s$. In other words, the 'resistance' is inversely proportional to the switching frequency and the capacitance of the capacitor. Because of its easy programmability, switched-capacitor devices find application in adaptive filtering, anti-aliasing, phase-locked loops, and digital signal processing (DSP).







structured in a grid that contains 20 CABs arranged in a 4×5 matrix (see Figure 2).

The programmable CABs rely on the configuration logic in the upper portion of the chip to control the connectivity within the array and functionality in each CAB. Two buses move data from the shift register to the CABs; the data control bus retrieves and moves the data from the shift register and the transfer control bus latches the data into local SRAM.

Custom functions can be added to the chip to meet customer specific applications. An 8-bit programmable bandgap voltage reference is available to each CAB.

Op amps are provided on the chip periphery that can be configured for unity gain buffering or filtering—for instance, anti-aliasing or smoothing filters (external resistors and capacitors are then required).

Configuring an analogue design within the array is performed by downloading 6 kbits of data via RS232 communications from a PC or EPROM. The data stream contains information to configure the individual cell, the cell interconnections, internal bandgap voltage reference, and I/Os. During this configuration download process, all cells are placed in a power down mode. Figure 2. Block diagram of the Type MPAA020 field programmable analog array.

SINGLE CAB

The diagram of a single configurable analogue block is shown in **Figure 3**. Each capacitor array consists of 255 statically switched capacitors, which means that the array can be programmed in 255 stepped values.

The static switches, which can be set only once during the programming, are also used to control the routeing resources.

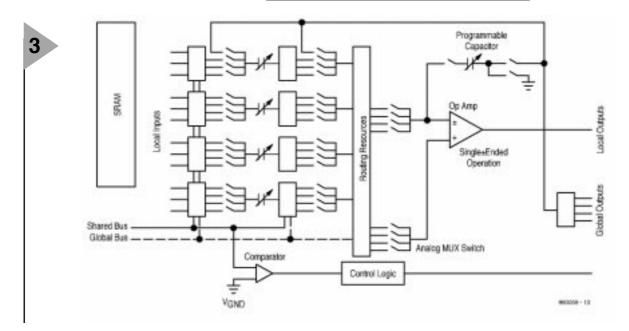
The 'resistance' (switched-capacitor effect) is obtained by dynamic switches, which also affect the phase of the input signal.

Additional switches enable the number and kind of limited local connections between two adjacent CABs. There are, however, also global lines to enable non-adjacent CABs to be interconnected.

20-CELL VERSION

The MPAA020 is a field programmable analogue array based on a general purpose analogue cell that may be configured, either alone or in combinations, as any of a wide range of analogue functions from simple comparators to complex filters. These cells are arranged in a 4×5 array with supporting circuitry to provide input/output

Figure 3. Diagram of one of the Configurable Analogue Blocks on which the MPAA020 is based.



signal buffering, programmable reference voltage, cell to cell interconnections, and so on.

Each cell's function may be programmed to connect with any of the other cells in the array. Unused cells are powered down individually to minimize power dissipation.

Digital interface circuitry is provided to write the analogue circuit configurations data to on-chip SRAM in the same manner as Motorola's digital FPGAs (serial and parallel PROM, and microprocessor mode).

Analogue circuit design is simplified with EasyAnalog[™] design software, which handles bit level circuit configuration details, allowing the user to do analogue design using functional macros in an easy to use point-andclick graphical environment.

E A S YA N A L O G TM P R O G R A M

The EasyAnalog[™] program may be compared with a circuit editor. After the desired function has been selected, it is placed on one or more free CABs, and the input and outputs connected as needed. Freeware EasyAnalog[™] runs under Windows 95 or NT and may be downloaded from the Internet http://sps.motorola.com/fpaa

The available functions are listed in Table 2.

PERFORMANCE

A summary of the MPAA020's performance features is listed in Table 1. The MPAA020's circuit topology provides advantages relative to chip area, pin count, and rail-to-rail voltage swing with improvements being made to the signal-to-noise ratio and signal bandwidth in arrays that will be introduced later this year. One of these, the MPAA132, has a signal-to-noise ratio

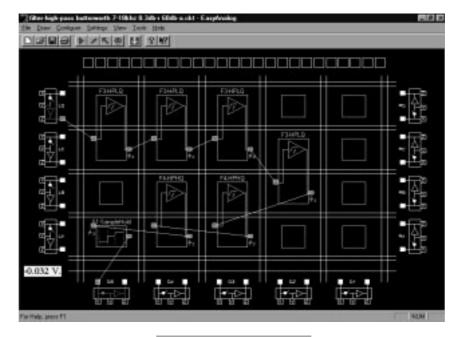


Figure 4. Example of a configuration possible with EasyAnalog ™ software.

(> 80 dB), a bandwidth of 1 MHz, internal feedback facilities, for instance, for automatic gain control (AGC), and a multiplier. A higher voltage family is also planned which will operate in applications with voltages greater than 10 V.

FINALLY

Use of the array may initially be problematic since it is housed in a 160-pin Quadratic Flat Pack (QPF) with a pin pitch of 0.25 mm. This makes manual soldering a little difficult.

[980059]

Table 2. Partial macro library – analogue functions

Single cell macro functions

Gain stages (max= 20' min= 1/20) Sum & diff. amps (3 weight inputs) Sample&hold Track&hold Integrator N-path integrator Differentiator Half-wave rectifier Full-wave rectifier LPF rectifier Cosine filter Decimator Bi-linear filter

Multi-cell macro functions

Low Q biquad filter (high- or low-pass); 2 cells Low Q biquad filter (notch, band-pass); 3 cells High Q biquad filter (high- or low-pass); 2 cells High Q biquad filter (notch, band-pass); 3 cells Maximum corner frequency = T/10 Minimum corner frequency = T/100 Limiter Interpolator Schmidt trigger Voltage-controlled oscillator Sine-wave oscillator Square-wave oscillator Triangle-wave oscillator



an original application for the ST62T20

Measuring liquid levels is a subject which never fails to cause heated debates. Does a technique exist which makes it possible to provide not only a 'tank empty' alarm, but also a continuous indication of the tank contents? The circuit described here operates in one of two modes: stand-alone or remote (using RS-232 communication). Once you've built the circuit, the fuel level in the tank of a heating system, or the water level in the gardening tank, is no longer a secret.

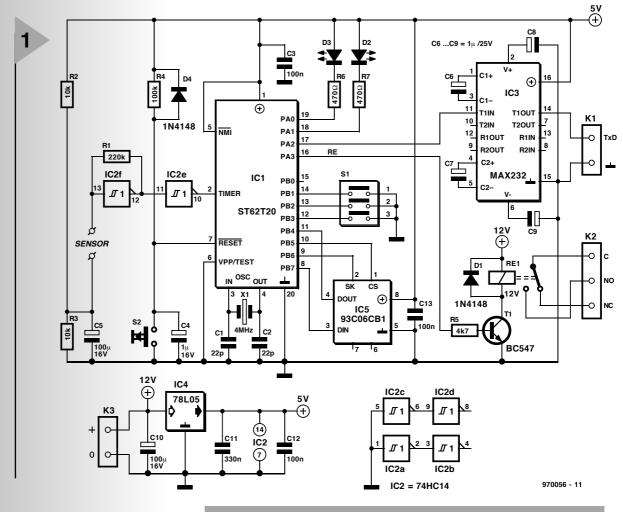


Figure 1. The liquid-level gauge consist of a handful of parts only; most of the work is done by IC1, a pre-programmed ST62T20 microcontroller.

Design by M. Vacher

60

Looking at the increasing number of circuits based on a microcontroller, one may start to wonder how it was possible, only a few years ago, to design electronics worthy of interest. If the microcontroller has changed the face of electronics for home construction, we have to recognise, though, that the appearance of this type of component has also caused a considerable reduction in comprehensibility of circuits based on a microcontroller. On the plus side, the use of a 'micro' presents a number of indisputable advantages, including a much simpler circuit diagram, and cost reductions due to fewer components and a smaller board.

THE ELECTRONICS

A look at the circuit diagram given in **Figure 1** allows you to discover that the electronics are reduced to a few elements only. IC1, A microcontroller type ST62T10 from SGS-Thomson is at the heart of the circuit. One external part the controller can't do without is an EEPROM, IC5. The third elementary component is the ubiquitous MAX232 which looks after the previously mentioned RS232 compatibility of the circuit.

The reasons for choosing an ST6 controller for this application are mainly that the 62T20 version is affordable (approx. £5), and that various entry-level development systems are available, for example, the ST6 Starter Kit, or the ST6 Programmer described in *Elektor Electronics* November 1996. The latter allows you to write your own programs an also 'burn' ST6 controllers.

When S2 is pressed, the ST6 is reset. Components R4 and C4 then briefly pull the reset input of the CPU logic low, and so cause the microcontroller to be re-initialised.

A number of lines from port B, PB4 to PB7, connect the processor to the EEPROM (electrically erasable programmable read-only memory), a type 93C06B1. The EEPROM has a serial communication channel, and offers a capacity of 256 bits organised as 16 words of 16 bits each (default mode used here), or 32 words of 16 bits each.

The on-chip oscillator uses a 4-MHz quartz crystal and the usual pair of satellite-capacitors, C1 and C2. The crystal is connected between the OSCIN and OSCOUT pins of the microcontroller.

The 3-way DIP switch block, S1, has a function in the calibration of the circuit. It will be discussed further on.

The component at the right-hand side of the circuit is a MAX232. There's practically no way to avoid this component because it provides everything you need to convert TTL levels (as supplied by the microcontroller) into RS232 levels (as used by the PC port with the same name), and vice versa. Here, the MAX232 sends data supplied by the processor to the serial interface of the PC, which uses them for further processing.

In the lower left corner of the circuit diagram you can see the electronics required for stand-alone operation of the liquid-level gauge: we're talking about the relay which is directly actuated by the PA3 line of port A (pin 16). Actually, the port line controls the relay via a switching transistor, T1. The relay contacts are connected to PCB terminal block K2. Depending on the way an external circuit, pump, valve or actuator can be controlled, the contacts have to be normally-open (NO) or normally-closed (NC) types.

The power supply is entirely conventional, being based on a three-pin voltage regulator type 78L05 (IC4).

HOW IT WORKS

Schmitt-trigger gate IC2f acts as an RC oscillator in which R1 is the resistive element. The 'capacitor' you would normally expect to see in the oscillator is formed by the two probes immersed in the liquid. As the capacitance is a function of the liquid level, so is the frequency produced by the Schmitttrigger oscillator. This frequency is measured by the microprocessor, and then translated into a corresponding level of the liquid in the tank. The previously mentioned display enables the necessary values to be stored in nonvolatile memory (EEPROM 9306). This principle applies to different liquids. The author tried it with water and heating fuel (light oil). As illustrated in the following table, the frequency variation obtained with the immersion probes depends on the liquid in the tank.

| Liquid | | max. level (250 mm) | resolution | | |
|--------|---------|------------------------|------------|--|--|
| Water | 280 kHz | 70 kHz | 0.07 mm | | |
| Fuel | 280 kHz | 230 kHz | 1 mm | | |

Let's look at the level calculation in greater detail. The signal supplied by the oscillator is applied to the TIMER input of the microcontroller, which measures the total duration of 32,768 cycles of the signal. In this way we get a 16-bit number which is proportional with the liquid level. Next, the ST6 micro performs the following calculation:

Level (mm) = 250 $(x-N_{low}) / (N_{high}-N_{low})$

where *x* is the measured value, N_{low} the 'low' calibration level stored in EEPROM, ($N_{\text{high}}-N_{\text{low}}$) the difference frequency stored in EEPROM and rep-

resenting a liquid level of 250 mm. Any other value is possible provided you modify the relevant parameter in the source code file before assembling the program. The **source code file** is available on a disk, the order code is **976015-1**.

As already mentioned, this circuit can be used in one of two modes:

stand-alone: the system operates independently, the relay being actuated when a programmed level is reached (for instance, to switch on a pump).

remote (RS232): the measured level is periodically sent to a serial link (running at 9,600 baud). The information is then processed by another system (a microcontroller or an alarm system). The liquid-level is directly supplied in millimetres. The syntax of the ASCII messages is

=00xxx < CR > < LF >

where xxx is the measured liquid-level in millimetres.

CONSTRUCTION

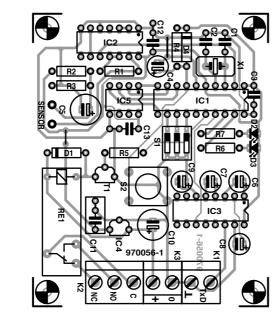
The artwork for the printed circuit board designed for this project is given in **Figure 2**. The circuit board is singlesided and, unfortunately, not available through our Readers Services. Although fitting all the parts is straightforward soldering work, you should observe the orientation of polarised components like integrated circuits (including the voltage regulator), electrolytic capacitors, LEDs, diodes and transistors.

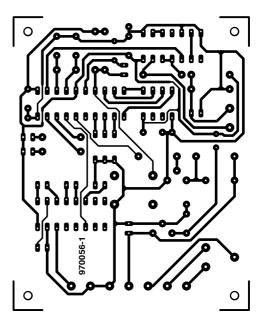
The microcontroller should, of course, contain the right program. Fortunately, you can obtain it **ready-programmed** through our Readers Services (order code **976515-1**), or as part of a kit from a kit supplier.

The integrated circuits are mounted in sockets. There is only one wire link on the board. Since the LEDs are only used during the calibration procedure, they may be fitted close to the PCB surface. Be sure not to fit DIL switch S1 the wrong way around. The contact marked '1' should be close to resistors R7 and R6. When the switches are in the 'on' position, the levers should be moved towards the ST6.

Measuring just 80×62 mm, the circuit board should not be too difficult to mount in a plastic (ABS) case of your choice. The two immersion probes may be made from plastic-covered curtain rods with a diameter of 4 mm. Their length will obviously depend on the depth of the tank. The probes should be fitted at a centre-tocentre distance of about 10 mm. The rods should pass through four holes in the case (two additional holes at the

2





COMPONENTS LIST

Resistors:

 $\begin{array}{l} {\sf R1} = 220 k \Omega \\ {\sf R2}, {\sf R3} = 10 k \Omega \\ {\sf R4} = 100 k \Omega \\ {\sf R5} = 4 k \Omega 7 \\ {\sf R6}, {\sf R7} = 470 \Omega \end{array}$

Capacitors:

C1,C2 = 22pF C3,C12,C13 = 100nF C4 = 1μ F 16V radial C5,C10 = 100μ F 16V radial C6-C9 = 1μ F 25V radial C11 = 330nF

Semiconductors:

Miscellaneous:

K1,K3 = 2-way PCB terminal block, raster 5mm
K2 = 3-way PCB terminal block, raster 5mm
S2 = presskey, Multimec CTL3
S1 = 3-way DIP-switch
X1 = 1 MHz quartz crystal
Re1 = relay, 12V, PCB-mount (e.g., Siemens V23057-B0002-A201)
Optional: floppy disk with microcontroller source code, order code
976015-1 (see Readers Services page).

rear side to keep them in place). Inside the case, the plastic covering is removed locally for the connection to the two oscillator inputs marked SEN-SOR. The four holes are sealed with two-component glue or a potting compound to make the enclosure watertight. In spite of this measure, the case must also be mounted well out of reach of the liquid in the tank. The power supply is a bit more rustic. The supply voltage is furnished by a mains adaptor with an output capacity of 12 V/40 mA. This output voltage need not be regulated, because it only powers the relay coil. The rest of the electronics draws its supply current from the 78L05 three-pin voltage regulator on the board. The 93C06 (or 93C46) EEPROM memory works in 16bit mode ('ORG', pin 6 not connected), which allows circuits of the old generation to be used.

SETTING UP

Once all components are in place on the board, you are ready to proceed with the calibration of the circuit. This procedure consists of two phases:

1. 'Low' level calibration, probes not immersed.

The switches in S1 should be set as follows: SW1-1 on, SW1-2 off, SW1-3 off. After switching on the supply voltage, or after a reset, followed by a stabilisation period of about 2 seconds, the system launches the frequency measurement. The value assigned to N_{low} is written into EEPROM. The end of the process is signalled by one of the two LEDs coming on (the green one, D3, for 'okay', or the red one, D2, for 'error').

2. 'High' level calibration, probes immersed in liquid with a column height of 250 mm.

Set the switch contacts as follows: SW1-1 on, SW1-2 off, SW1-3 on. Again, after switching on the supply voltage, or after a reset, followed by a stabilisation period of about 2 seconds, the system launches the frequency measurement. The value assigned to N_{high} as well as the result of ($N_{high}-N_{low}$) are written into EEPROM. The end of the process is signalled by one of the two LEDs coming on (the green one, D3, for 'okay', or the red one, D2, for 'error').

Figure 2. Copper track layout and component mounting plan of the single-sided printed circuit board designed for the project (board not available ready-made).

Programming the levels at which the relay is actuated.

This procedure is similar to the one for the calibration, only switch SW1-2 is set to the 'on' position. The relay is energised when the liquid tops the 'high' level, and is switched off when the liquid drops below the 'low' level (hysteresis).

Note that the three switch contacts in S1 should be returned to the 'off' position for normal use of the liquidlevel gauge.

OPTIONS

This circuit may be used with or without a serial RS232 link. If the computer system (or microcontroller) you want to use for the processing of liquid-level data accepts TTL levels, then the MAX232 may be omitted. As it is not required in the present application, the RxD line is not implemented in the serial link. If you plan to extend the program with additional functions, you may connect pin 15 (PB0) of the microcontroller to the R1OUT pin. This allows the RxD signal to be applied to the R1IN pin. It is then also worthwhile to replace K1 with a 3-pin header whose contacts may be connected to wires to implement the above mentioned function.

(970056-1)

Warning. This circuit is not designed or approved for use in tanks containing highly flammable, explosive, aggressive or corrosive liquids.

V23057 Card Relay E

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Passive Components Relavs

V23057 Card Relay E

Upright mounting, immersion cleanable. For PCB mounting, pin arrangement suits 2.5 mm and 0.1-in. grid in accordance with DIN 40801 and DIN 40803, **fine**.

V23057-B0*** with creep distances and clearances > 4mm^{*}.

1 changeover contact, single or bifurcated, or 1 make contact, single.

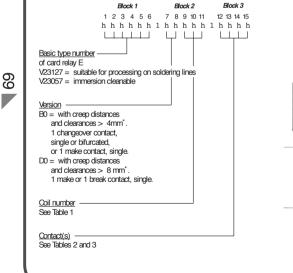
V23057-D0*** with creep distances and clearances > 8 mm^{*}. 1 make or 1 break contact, single.

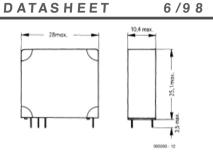
^{*} between winding and contact.

Manufacturer

Siemens. Siemens plc, Siemens House, Windmill Poad, Sunbury-on-Thames, tel. (0932) 752677, fax (0932) 752671. UK distributor: ElectroValue.

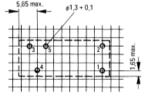
Ordering Code





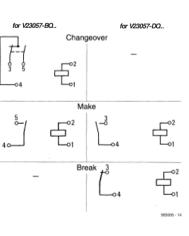
<u>ELLEIKTOR</u>

FIFCTRONICS



Mounting hole layout View onto the terminals

983005 - 13



UM8250A

UM8250A

Manufacturer

(01296) 395 635.

General Description

Integrated Circuits Microprocessor, Interfacing

Asynchronous Communication Element (ACE)

United Microelectronics Corp (UMC), No 3, Li-Hsin

Internet: www.umc.com.tw/. UK Distributors: Future

Road II, Science-Based Industrial Park, Hsin-chu

Oty, Taiwan, R.O.C. Fax: (+ 886) 3-577-4767.

Electronics (01753) 76 3000; Ambar Cascom

The UM8250A is a programmable Asynchronous

Communication Element (ACE) chip fabricated using

the S-Gate NMOS process. It performs serial-to-par-

allel conversion on data characters received from a

peripheral device or a modern, and parallel-to-serial

conversion on data characters received from a CPU.

ELECTRONICS

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The CPU can read the complete status of the ACE at any time during the functional operation. It also includes a programmable baud rate generator capable of dividing the timing reference clock input by divisors of 1 to $(2^{16}-1)$, and producing a 16x clock for driving the internal transmitter logic.

Application

Analogue-to-Digital Converter, *Bektor Bectronics* June 1998 Supplement The following tables of ACE register functions are offered as a help to program the above converter.

Interrupt Identification Register (IIR)

The ACE has an on-chip interrupt capability that allows for flexibility in interfacing popular microprocessor presently available. In order to provide minimum software overhead during data character transfers, the ACE prioritizes interrupts into four levels. When addressed during chip-select time the IIR freezes the highest priority interrupt pending, and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU.

| Interrupt I | dentificatio | n Register | Interrupt Set and Reset Functions | | | | | |
|----------------|--------------|----------------|-----------------------------------|---------------------------------------|--|---|--|--|
| Bit2 Bit1 Bit0 | | Priority Level | Interrupt Type | Interrupt Source | Interrupt Reset Control | | | |
| 0 | 0 | 1 | _ | None | None | _ | | |
| 1 | 1 | 0 | Highest | Receiver Line Sta- tus | Overrun Error or Parity Error or Framing Error or Break Interrupt | Reading the Line Status Register | | |
| 1 | -0 | 0 | Second | Received Data Available | Receiver Data Avail- able | Reading the Receiver Buffer Register | | |
| 0 | 1 | 0 | Third | Transmitter Holding Register Empty | Transmitter Holding Register Empty | Reading the IIR Register (if source of interrupt) or Writing to the Transmitte Holding Register | | |
| 0 | 0 | 0 | Fourth | MODEM Status | Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Detect | Reading the MCDBM Status Register | | |

UM8250A



Integrated Circuits Microprocessor, Interfacing

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| | | 0 DLAB= 1 | Divisor Latch (MS) | DLM | Bt 8 | Bt 9 | Bt 10 | Bt 11 | Bt 12 | Bt 13 | Bt 14 | Bt 15 | |
|---|------------------|-----------|--|-----|--|---|---|---|-------------------------|---|-----------------------------|---------------------------------------|--|
| | | 0 dlab= 1 | Divisor Latch (LS) | DLL | o Xa | 포 - | B <u>t</u> 2 | ъ В | Bţ 4 | E E | В. В | Bit 7 | |
| | | 7 | Scratch Register | SCR | Bto | Bt 1 | Bt 2 | Bt 3 | Bt 4 | Bt 5 | Bt 6 | Bit 7 | |
| | | 9 | MODEM Sta- tus Register | MSR | Delta Clear to Send (DCTS) | Detta Data Set Ready (DDSR) | Trailing Edge Ring Indicator (TERI) | Delta Data Car- rier Detect (DDOD) | Clear to Send (CTS) | Data Set Ready (DSR) | Ring Indicator (RI) | Data Carrier Detect (DOD) | |
| | | 5 | Line Status Register | ISR | Data Ready (DR) | Overrun Error (CR) | Parity Error (PB) | Framing Error (円) | Break Interrupt (Bl) | Transmitter Holding Regis- ter (THRB) | Transmitter Empty (TEMI) | 0 | |
| | Register address | 4 | Modern Con- trol Register | MCR | Data Terminal Ready (DTR) | Request To Send (RTS) | Out 1 | Out 2 | фо | 0 | 0 | 0 | |
| | æ | 3 | Line Control Register | LCR | Word Length Select Bt 0 (WLS0) | Word Length Select Et 1 (MLS1) | Number of Stop Efts (STB) | Parity Erable (PEN) | Even Parity Select | Stick Parity | Set Break (TXD) | Divisor Latch Access Bit (DLAB) | 7 |
| | | 2 | Interrupt Ident. Regis- ter (Read Only) | IIR | '0' if Interrupt Pending | Interrupt ID Bit (0) | Interrupt ID Bit (1) | 0 | 0 | 0 | 0 | 0 | smitted or receive |
| | | 1 dlabe 0 | Interrupt Enable Register) | Œ | Enable Received Data Available Interrupt (ITB H) | Erable Transmitter Holding Register Empty Interrupt (ETBB) | Erable Receiver Line Satus Inter- rupt (ELSI) | Erable MODEM Status Interrupt (DESSI) | o | o | o | o | * Bit 0 is the least significant bit. It is the first bit serially transmitted or received |
| | | 0 DLAB= 0 | Transmitter Holding Reg- ister (Write Only) | ΗR | Data Bt 0 | Data Bt 1 | Data Bt 2 | Data Bt 3 | Data Bt 4 | Data Bt 5 | Data Bt 6 | Data Bt 7 | ficant bit. It is th |
| | | 0 DLAB= 0 | Receiver Buffer Reg- ister (Read Only) | RBR | Data Bit 0* | Data Bit 1 | Data Bit 2 | Data Bit 3 | Data Bit 4 | Data Bit 5 | Data Bit 6 | Data Bit 7 | s the least signi |
| | | | Bit 10 | | 0 | - | 2 | e | 4 | 2 | 9 | ~ | * Bit O i |
| 1 | | | | | | | | • | • | | | • | |

V23057 Card Relay E



Passive Components Relays

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| | | | | Ta | able 1 Coil vol | tages | | | | |
|---|-----------------------------------|-------------|---------------------------------|--|--|---|-----------------------------|--------------------------|----------------------|--|
| | Coil number | Nominal vo | oltage | q | perating voltage | | Resistance at 20 °C | | | |
| | Order Code, | VDC | | Minimum voltage U _l V DC | | Maximum voltage U _{II} V DC | | Ω | | |
| | Block 2 V DC | | | | | | | | | |
| | 001 | 6 | 6 | | 4.2 | | 6 | 80 ± 8 | | |
| | 002 | 12 | | 8 | .3 | 21. | 5 | 330 ± 3 | 3 | |
| | 006 | 24 | | 16 | 5.8 | 40 |) | 1200 ± 180 4700 ± 700 | | |
| | 013 | 48 | | 30 | 3.6 | 79 |) | | | |
| | 023 | 60 | | 4 | 2 | 98 | 3 | 7200 ± 10 | 080 | |
| Table | 2 Contact spe | cifications | V2312 | 7-A0*** and | V23057-A0** | */-B0*** with | single conta | icts | | |
| | ng Code, block 3 | | | A101 | A201 | A401 | A102 | A202 | A402 | |
| Contact material | | | | silver, gold- flashed | silver nickel | silver-cadmium oxide | silver, gold- flashed | silver nickel | silver-cadi oxide | |
| Contac | ts (see also base | terminals) | | double, change-over single, make | | | | 1 | | |
| | witching voltage a 110 group C | is per | V DC V AC | 300 250 | | | | | | |
| Max. s | witching current | | А | 5/15 ¹ | /15 ¹ 8/15 ¹ 5/15 ¹ | | | 8/15 ¹ | | |
| Max. power rating ² , DC voltage W W W W | | | 50330 (voltage dependent) | up to 24 V: 100 30 V: 80 200 V: 30 250 V: 50 | 35330 (voltage dependent) | 50330 (voltage dependent) | 30 V: 80 200 V: 30 (volt | | | |
| AC voltage VA | | | | 1250 2000 1250 2000 | | | | | 000 | |
| Max. c | ontinuous current | | Α | 8 | | | | | | |
| | nical life | | Ops. | approx. 2 x 10 ⁷ | | | | | | |

Table 3. Contact specifications V23127-A0*** and V23057-A0***/-B0*** with bifurcated contacts Ordering code, block 3 B101 B601 Contact material silver, gold-flashed gold F Contacts (see also base terminals) double, change-over V DC Max. switching voltage as per 300 36 VDE 0110 group C V AC 250 30 4/10¹ Max. switching current Α 0.2 Max. power rating W DC voltage voltage-dependent 5 AC voltage VA 500 _ 2 Max. continuous current 6 Α Mechanical life Ops. approx. 2 x 107 ¹ higher current may flow for a maximum of 4 seconds for up to 10% of on time.

70