ELEKTOR ELECTRONICS
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FREE SUPPLEMENT
PC TOPICS

FASTER ACCESS TO THE INTERNET VIA CABLE AND SATELLITE

MONITOR RADIATION? USE OUR E-METER!

PARKING-DISTANCE MONITOR

20-METRE RECEIVER

ELEKTOR ELECTRONICS

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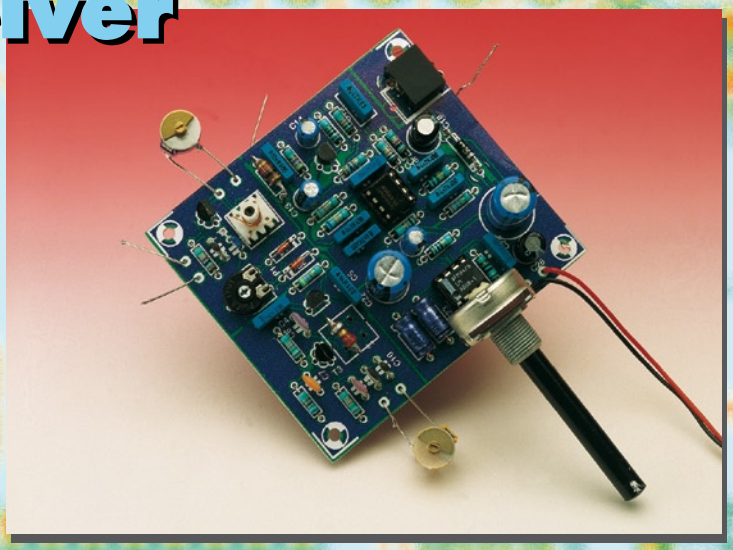

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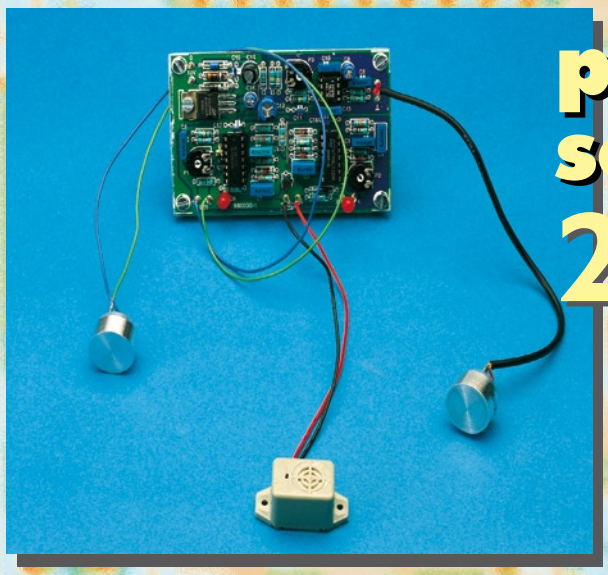

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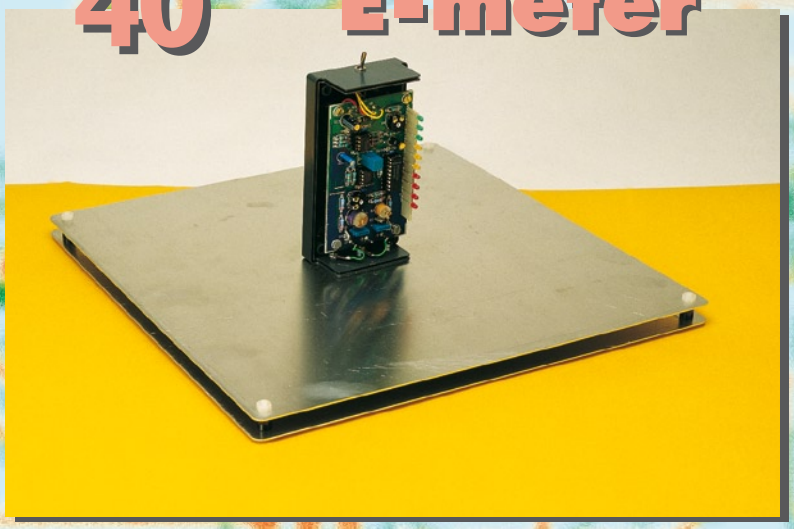

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Many of you will recall the days when a new, and then very fast, modem meant euphoria. “From now on, communication with the Internet will be faster, better, etc.” is what many computers owners must have thought at that time. Alas, speed is a relative notion in computer land. Meanwhile, new communication technologies have been designed to speed up Internet access. This article provides a glimpse of what the future has in store for Internet users.

Faster access to the Internet

by cable and satellite

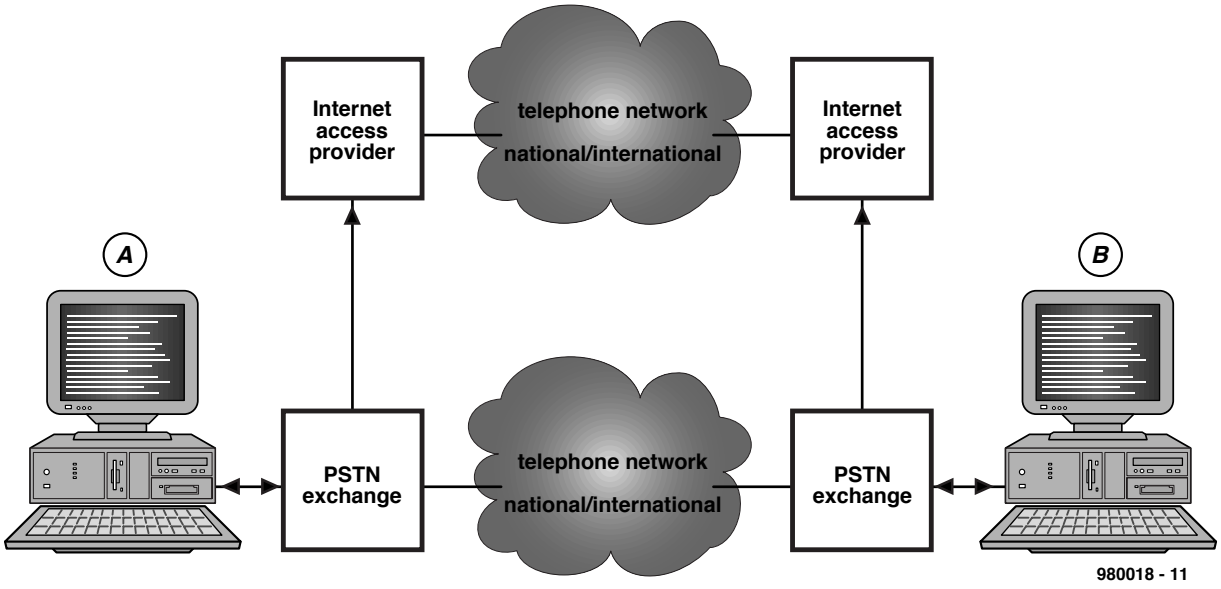


Figure 1. Traditionally, part of an Internet link is by way of the plain old telephone system (POTS).

Internet connections make ever-heavier demands on the bandwidth of a communication channel. Because of the increased information density (these days nearly all web pages have graphic elements, and they support sound and exhibit photographs), a pretty fast data line has to be available to enable the web pages to be built at reasonable speed. Moreover, work on new, 'heavier' services like distributing digital video via the Internet is underway. Consequently, a 14k4 modem is just to slow to surf the Internet, while a 33k6 modem gives reasonable results, and an ISDN connection using a bandwidth of 64 kbits/s is a good alternative these days (though overpriced in the UK). ISDN even allows you to aggregate two channels, enabling a bandwidth of 128 kbits/s to be achieved. Looking at the current trend in technological developments, you may safely assume that even that kind of speed will not be sufficient some time in the near future.
The speed of a modem is, incidentally, only one aspect of the case—the internal capacity (bandwidth) of the Internet and the provider's connection to the Net must not be bottlenecks either. In more cases than you would care to think of, the datastream between provider and end-user is ultimately much slower than the theoretical capacity offered by the modem.
Let's return to the communication between the end-user and the service provider. So far, two systems are in use to realise the communication between the Internet and you, the end-user. The vast majority of individual users will faithfully connect to their ISPs by way of the public switched telephone network (PSTN), also jokingly referred to as POTS (plain old telephone system). Corporate (business) users may resort to leased datalines, which are much faster. In fact, leased lines may supply a bandwidth that matches the exact requirements of the (corporate) user, so that a perfect, seamless link may be made with the corporate network. This type of connection is far too expensive for individual users, hobbyists and other occasional users, who are more or less forced to opt for a modem-PSTN connection. Typically, the available bandwidth will then depend on the quality of the telephone line and the modem technology used. With analogue connections, that is, connections using a standard telephone dial-up connection, the highest available speed is currently offered by the asymmetrical 56 kbits/s standard.
With the increased demand for fast datalinks and the rapidly growing number of Internet users in mind, new service providers seem to pop up almost every day. The coming years will no doubt bring us a fierce and interesting battle between cable-TV companies, electricity boards, telephone companies and other suppliers of information services. Each of these will attempt to induce individual Internet users to go for their offerings of fast Internet services.

Telephone at the hub

The drawing in **Figure 1** illustrates how today's Internet connections are built up. The end-user relies on his/her telephone line to dial the Internet Service provider (ISP). In this way, the end-user causes a digital connection to be established using this (analogue) telephone line. Using a modem bank and a network server, the provider arranges for the actual connection to the Internet to be established. Depending on the final 'destination', a Web site being visited, or an e-mail message to be delivered, a second telephone line is employed at the 'far' side. Actually, the Internet 'bypasses' a piece of the telephone network whenever it allows two end-users to communicate with each other. Ultimately, digital data from one computer is delivered, unmodified, to another, which may be at the other side of the globe! Once you get this point, it is easily understood why telephone companies are striving to find a solution that enables end-users to be connected directly to the Internet. The telephone exchange then has to create the link with the Internet. In a number of cases, the service provider is then no longer required. This option is currently under investigation, and there are already encouraging signs from a manufacturer claiming to have found the solution.
Internet providers, afraid of being abandoned by their millions of users, will of course try to counter this development by offering services that reduce the role of the traditional telephone companies.
In this context, it is interesting to see that the European Commission recently decided that Internet 'phone links need not be subject to special regulations. This decision may be revised, however, when we enter the year 2000 and the EEC will look into the problems again. Until that time, Internet providers are in

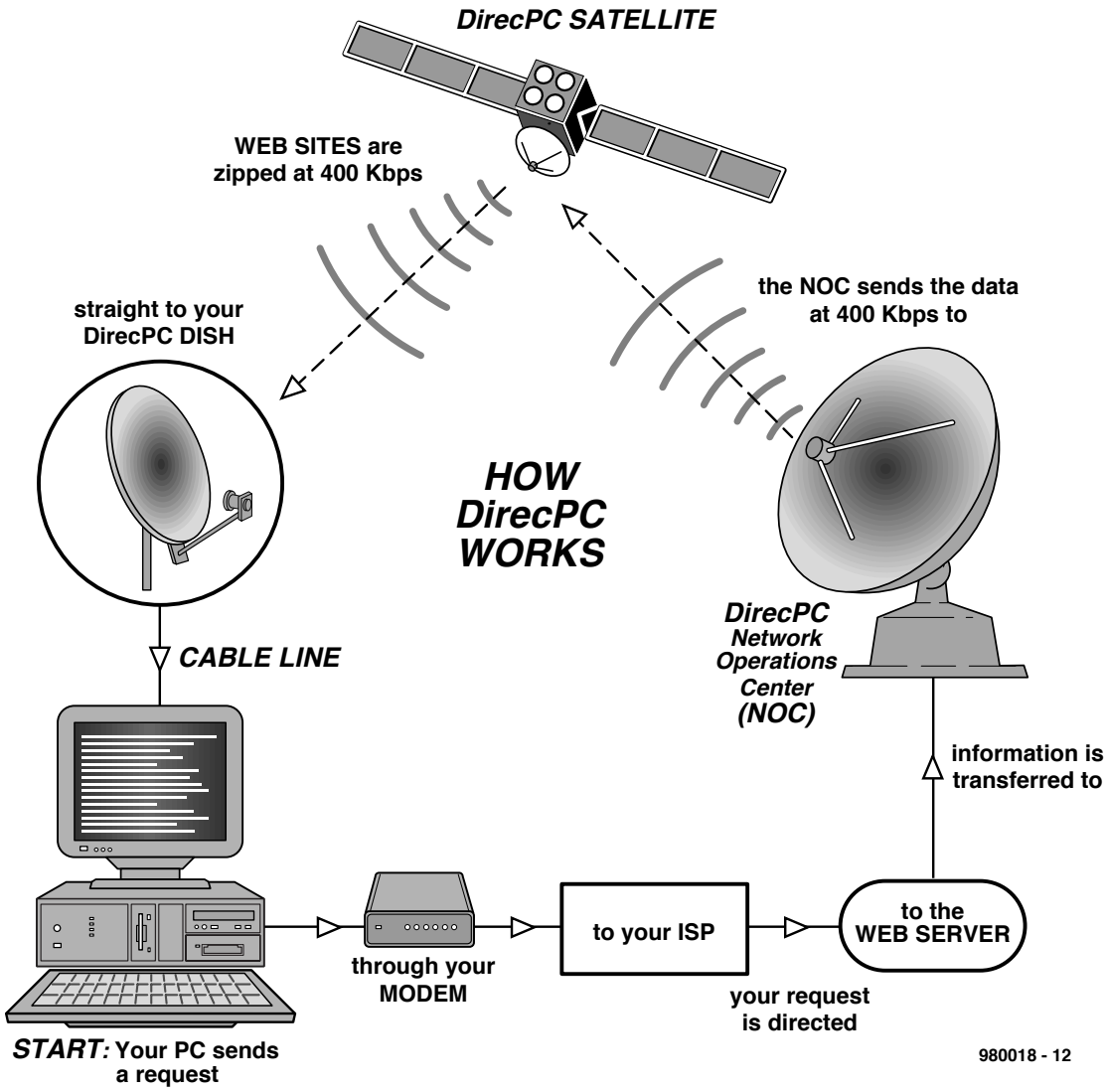
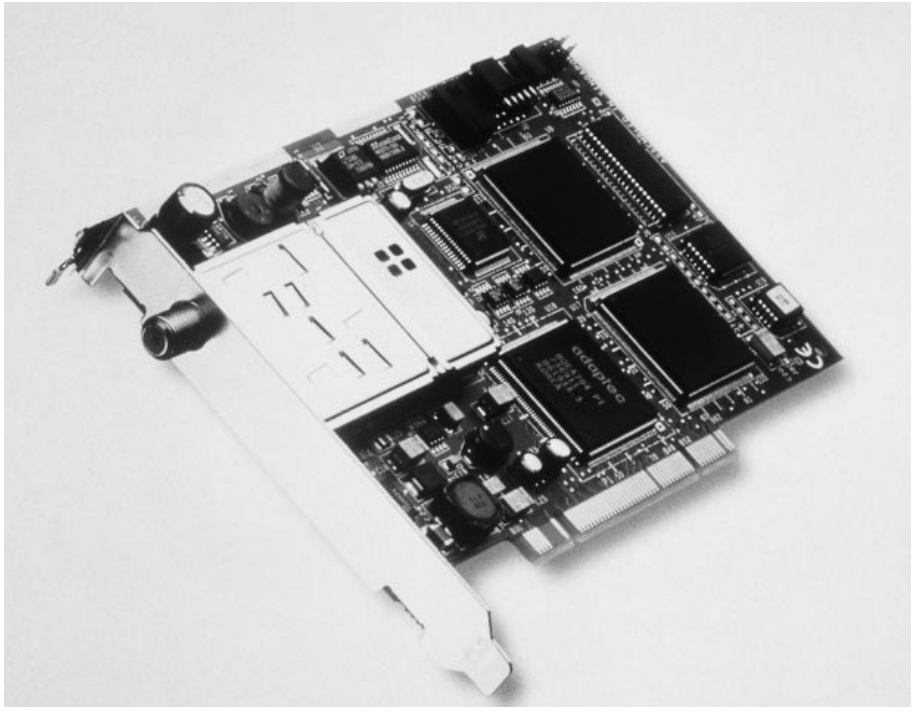


Figure 2. Using DirecPC the end-user employs a modem and a telephone line to dial into the server of his ISP, sending a request for information. The requested information is returned over the air by means of a fast satellite link.

a position to offer national and international telephone services to their customers. True, these services have their limitations. What counts, however, is that they are always cheaper than *any* overseas call. Consequently, telephone companies have rushed to promote the development of this new Internet application.
The EEC reached this decision because the prevailing opinion is that Internet telephony is not a separate service aimed at making a profit, but rather an extension of Internet services already available to the public.



Analogue modems

A number of modem types are currently available for connecting to a regular telephone line. The theoretical speeds achieved by these modems range from 14k4, 28k8 and 33k6, up to 56k. The first three rely on symmetrical

connections with the same speeds being available for the upstream and downstream data. The latter modem type, generally referred to as '56k', employs an asymmetrical connection. Moreover, because of its special technology, a 56k modem may only be used if the Internet provider supports the relevant protocol, and a suitable telephone line is available.
It is generally assumed that 56k modems are pushing the limits of what can be achieved in terms of bandwidth on ordinary (copper) telephone lines. No doubt, new technologies will be developed that allow service providers to offer higher bandwidth and thus more speed to their customers.

ISDN, a fast alternative

In the UK, ISDN is currently the fastest and affordable way available to small business users to jump the Internet bandwagon, and be assured of reasonable speed. Unfortunately, British Telecom, unlike some of its Continental counterparts like Deutsche Telekom and PTT Netherlands, for some reason maintains ISDN price levels which are ludicrous, and way beyond the reach of private individuals.
A standard ISDN connection (BRI, Basic Rate Interface) offers two channels (B channels) of 64 kbits/s each, which may be aggregated (bundled) to give a single channel with a capacity of 128 kbits/s. Doing so (in theory) creates a bandwidth that is four times larger than can be achieved with a 33k6 modem.
A third channel (D channel) with a bandwidth of 16 kbits/s is reserved for special control and signalling functions within ISDN. Although there are a few telephone companies that put this extra bandwidth at the user's disposal for a permanent link to the Internet, the bandwidth is generally of no use to customers. Although this channel offers only a small bandwidth, it is perfect for transmitting information with modest speed requirements. For example, email messaging and Stock Exchange data. While you make a telephone call, data is automatically retrieved from the Internet.
However, a real breakthrough with a promise of much higher data rates calls for a totally different approach. It is therefore not surprising to note the arrival of service providers that are not telephone companies at all. These newcomers look poised to modify their own infrastructures in such a way that it is capable of carrying high-speed data traffic.

By cable TV network

A growing number of cable-TV network operators are beginning to realise that existing infrastructures can handle a lot more than just two dozen or so TV programmes. Using a cable modem and a hefty investment in the layout of existing cable networks and their infrastructures, it should be possible, in principle, to realise two-way high-speed data communication. As far as speed is concerned, the cable modem (if available privately) is then likely to become the fastest link to the Internet. Because the standard behind these modems has not yet been finalised, it is not yet possible to give exact figures as regards the speeds achieved by this new technology. An educated guess, however, is 2 to 10 million bits per seconds, which is far more than the 128 kbits/s and 33.6 kbits/s (theoretical) maximum rates offered by ISDN and plain telephone lines respectively.
When talking about cable modems, a distinction is made between symmetrical and asymmetrical connections. An asymmetrical link means that the path between the user and the service provider is slower than the path in the opposite direction. This situation may be compared to that of the 56k modem. None the less, the speed of this 'slow' upstream channel is still 500 kbits/s, which is impressive when compared with what is normally feasible using the standard telephone network.

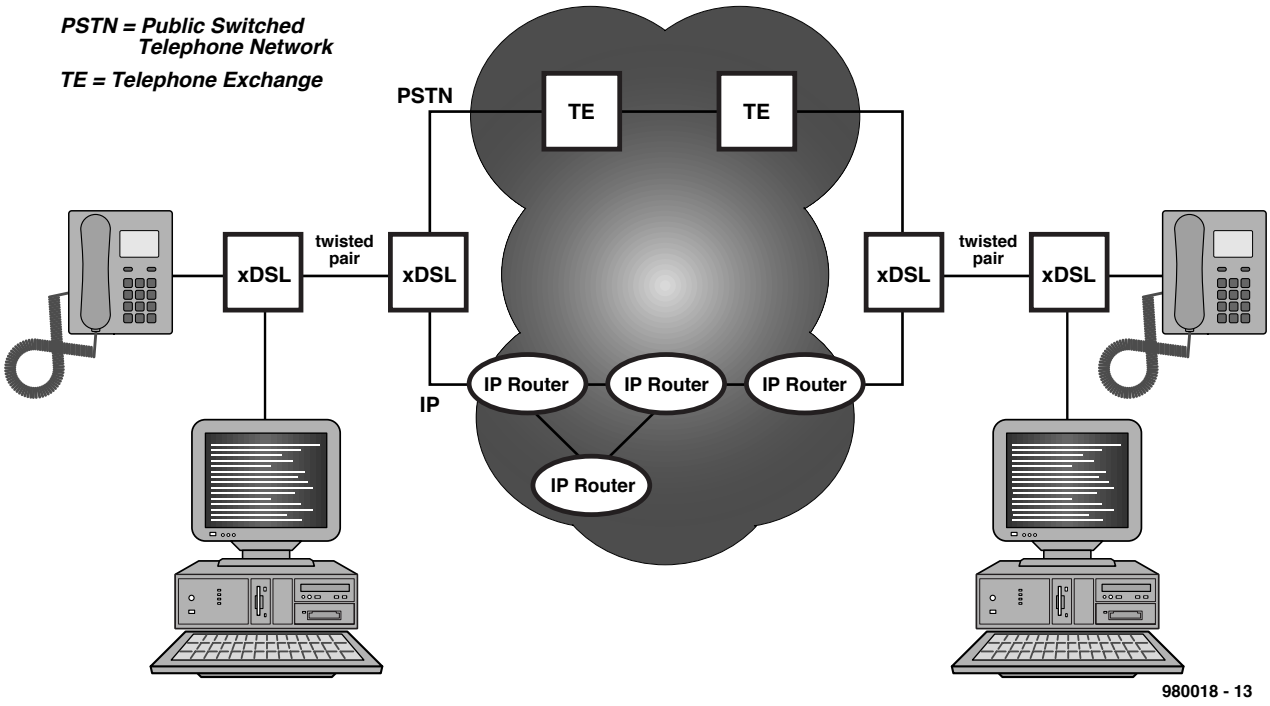


Figure 3. With XDSL modem techniques (i.e., ADSL and VHDSL), high-speed data is sent down twisted-pair copper cables, along with ordinary telephone traffic (PSTN or ISDN). At the local telephone exchange, the data traffic is sent to an IP router. Next, the traffic is arranged via the Internet.

Internet service providers also use proxy servers to make access to popular web sites as fast as possible. A proxy server holds instantly available copies of these sites. Being 'closer' to the end-user, popular web pages can be loaded much faster from a proxy server than from the server operated by the original site builders. A dedicated proxy server prevents users from going under in the very busy traffic on the Internet proper.
Cable modems are equipped with an Ethernet connection, and are incorporated in a small network using a PC-hosted Ethernet interface. The main advantage of this set-up is that the modem connection with the Internet is always available, which means that no time is lost on dialling in and logging on. Moreover, the 'bottleneck' effect of a slow serial port is eradicated. Because the PC communicates with the cable modem by means of the TCP/IP protocol, special software is not required.
To the computer user, the application of an Ethernet interface means that data may always be found rapidly, but also that he/she has to pay attention to files that have been marked as 'shared'. If these files can be accessed without a password, other Internet users may get at them.
As we write this article, the use of cable modems is limited to a couple of experiments only. Clearly, it will take some time for cable companies to get used to the idea of seeing their infrastructure carry two-way data traffic. Consequently, all cable distribution amplifiers have to be adapted, and large parts of the network have to be replaced by fibre optic cables. Once this has been done, the cable modem is probably the fastest way to cruise the Internet. However, cable penetration being modest in the UK as compared with, say, Germany and The Netherlands, the cable modem may be a non-starter in this country.

By satellite

The advantage of a wireless data link, for example, by satellite, is that additional infrastructure is (in principle) not required. In the USA and Germany, it is currently possible to use a satellite dish to receive information from the Internet. This new, wireless, link guarantees fast traffic even under adverse conditions. The first service provider to make Internet access by satellite a reality is a US company called DirecPC, a subsidiary of DirecTV. The company specialises in television services by satellite.
The highest data speed that may be achieved using a satellite dish is about 400 kbits/s, which is more than three times as fast as an ISDN connection. The new technology has a snag, however. The dish only allows the reception of data (downstream) — upstream data is still sent by ordinary telephone lines. So, there's still a telephone bill to pay in addition to the monthly charges raised by the Internet service provider.
In case the user needs to obtain information via the Internet, he/she has to dial into the ISP's server (by telephone) and send the relevant request. The ISP has a fast link to the Internet, and will respond to the call by uploading the relevant data to the satellite. The satellite, in turn, arranges the transmission of the requested data to the user's dish. This rather cumbersome approach, which causes an enormous detour for the data, is of particular interest whenever large amounts of data are needed. None the less, when compared with competitive systems, Internet by satellite supplies only average results at pretty high cost. This makes the system a non-starter for private users, at least, for the time being.

ADSL: phone lines go digital

As communication lines used for the telephone network become more powerful, it seems that there is an increasing danger of the link between the user and the local telephone becomming a bottleneck. In practice, the 2-wire twisted-pair copper cable that brings the telephone network to your home is not very long, and it lends itself to creating faster links provided new modem technologies are employed.
ADSL (asymmetric digital subscriber line) is a new digital network technology capable of employing copper wire pairs as used in the telephone network. On average, a bandwidth of 1.5 Mbits/s is available if you download data over an ADSL line. The uploading speed is 64 Kbits/s. This asymmetric structure lends itself very well to Internet use because the typical user will send far less data to the server than he/she receives from the server. This digital bandwidth is available besides a regular telephone service, and is suitable for combining with ADSL in the near future.
The new ADSL system is in popular use in a number of areas. In Canada, more than 30% of the telephone companies support this protocol. In other countries, ADSL is the subject of extensive experiments.

Still faster

Although ADSL allows an Internet connection to be established that is pretty fast by today's standards, VHDSL (very high-speed digital subscriber line) makes it possible to convey datastreams of about 10 Mbits/s over twisted-pair copper wires. A disadvantage of this protocol is, however, that the largest distance that may be covered using copper wires is even shorter than the 3 to 5 km achieved by ADSL. However, the distance that may be covered using fibre optics and VHDL is, in principle, infinite. Considering the innovations currently implemented in the many parts of the telephone network, the fibre optic cable is rapidly approaching your doorstep. In other words, those copper wires are getting shorter all the time.
Obviously, the coming years will deliver many changes in fast digital connections to our doorstep. As a result, there are fantastic opportunities for advanced digital services like per-per-view and video on demand.

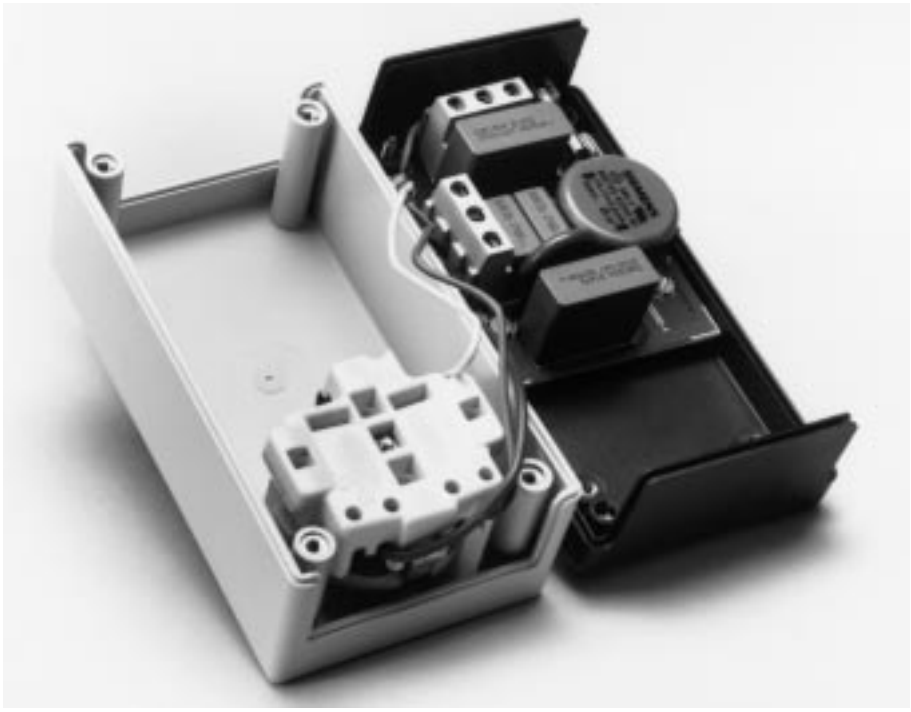
(980018)

This filter fulfils three functions: it acts as a in-phase filter for common-mode noise and as an antiphase filter for differential-mode noise, and it also protects the connected circuit against overvoltages and transients on the mains lines.

Design by H. Bonekamp

Mains filter with overvoltage protection

increases the noise immunity of sensitive circuits



In the last few years, electromagnetic compatibility (EMC) has become an important consideration in the design of electronic circuits. The designer has an obligation to achieve a low level of emissions and a high degree of immunity to external noise, not only for circuits that specifically work at high frequencies but also for most computer, microcontroller and audio circuits. In order to meet this objective at an appropriate cost, passive and active EMC measures must be taken in all stages of the development process. In principle, one can say that the later that such measures are introduced in the course of development, the more difficult and expensive they are to implement.

Designing a circuit with no regard to its EMC behaviour, and then making it compliant by packaging it in a metal enclosure with a mains filter, will in most cases turn out to be an (expensively) mistaken approach. Adding a mains filter to a circuit which has proven to be overly susceptible to external noise, in spite of the use of all other countermeasures, can only be regarded as a desperate solution. Mains filters are thus required even for DIY projects, prototypes and laboratory models. With commercial mains filters, the designer's usual problem is first to select a suitable filter from the profusion of types available, and then to employ it in a manner which more or less meets the conditions stated on the manufacturer's datasheet. It is thus quite reasonable to present a design for a universally usable mains filter whose parameters and operating principles are at least fairly well known.

In-phase operation

You can find a good theoretical introduction to the subject of mains noise in the article "Mains-noise suppression" in the June 1997 issue of *Elektor Electronics*. In the present article, we concentrate on common-mode and differential-mode noise. The difference between these can be explained with reference to **Figure 1**.

If the noise current flows from the source of the disturbance through both mains leads L (live) and N (neutral) to the noise 'recipient', and then returns via the protective earth lead, PE, and the earth, this is called *common-mode* or 'asymmetrical' noise. If on the other hand the noise current flows through one mains lead to the noise recipient and then returns via the other mains lead (but not via the earth), this is called *differential-mode* or 'symmetrical' noise. As a rule, most differential-mode noise lies under 500 kHz and most common-mode noise above 500 kHz.

Technical data

Voltage:	230 V~
Maximum current:	2 A
Common-mode noise suppression:	
(-3dB at 18 KHz):	50 dB
Differential-mode noise suppression:	
(-3dB at 35 KHz):	50 dB

The mains filter consists of nine carefully chosen components. The most noteworthy is the *current-balanced choke* L, which has two identical windings wound in the *same* direction on a toroidal core. The effect of this choke is different for common-mode and differential-mode noise. A current flowing through a winding generates a magnetic flux in the core. With common-mode noise, the noise currents flow through both windings in the same direction, so that the two magnetic fields add to each other. A common-mode noise current thus sees the full inductance of the choke.

The combination of the inductor and the two capacitors C_y acts as a low-pass filter for common-mode noise. In order to quantify the attenuation characteristics of this filter, we can consider **Figure 2**, which depicts the filter elements for one mains lead together with the parasitic components that are most significant for common-mode currents, namely the parallel capacitance of the choke and the series inductance of the capacitor. This filter

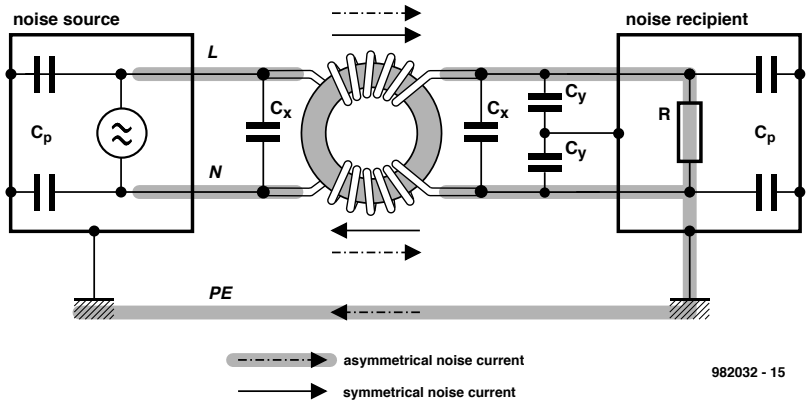


Figure 1. Basic operation of a simple filter between a noise source and a noise recipient. Note the different paths for asymmetric (common-mode) and symmetric (differential-mode) noise currents.

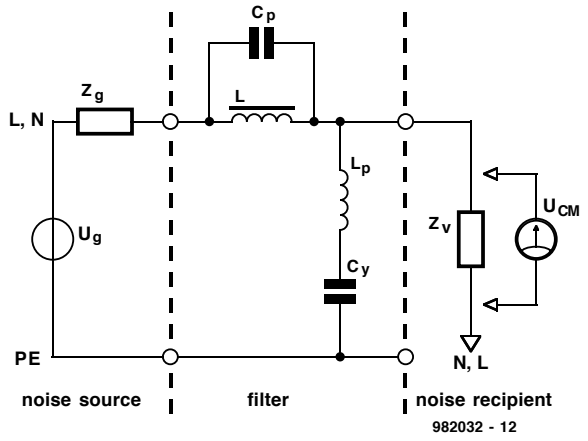


Figure 2. Equivalent circuit for common-mode noise. Only one lead (L or N) is shown.

has an attenuation characteristic with three regions, as shown by the dashed line in **Figure 3**. (Most commercially available mains filters have a similar characteristic.) The low-frequency passband region is dominated by the low-pass LC combination ($f_{res} = 1/2\pi\sqrt{LC_y}$) and has a slope of 12 dB/octave; the effect of the parasitic components is negligible in this region. In the high-frequency region the situation is exactly the opposite: the parasitic components form a 12-dB high-pass filter ($f_{res} = 1/2\pi\sqrt{L_pC_p}$) which allows very-high-frequency common-mode noise to pass with almost no attenuation. The two points of maximum attenuation, between which the attenuation is relatively uniform, are due to two LC networks with resonance frequencies $f_{CM1} = 1/2\pi\sqrt{LC_p}$ and $f_{CM2} = 1/2\pi\sqrt{L_pC_y}$.

In order to achieve the maximum possible attenuation, it is preferable to use a toroidal core with a high relative permeability (μ_r) since this results in a current-balanced choke with high inductance. However, non-linear effects due to the saturation of the core are undesirable; in other words, the peak noise currents should not exceed a certain value — although it is precisely these unpredictable noise peaks which the filter is supposed to render harmless. The capacitors can be relatively small, due to the high inductance of the choke windings. This is fortunate, since otherwise the leakage currents through the capacitors to PE could become large enough to trip the earth-leakage current breaker (ELCB). In addition, suitable capacitors that are approved for use in such filters are only available with relatively small values. Specifically, only so-called EMI-suppression capacitors meeting the EN132400 standard can be used; these are Y2-class capacitors with superior mechanical and electrical safety characteristics. Y-class capacitors are constructed such that no mains voltage can reach the safety earth lead under any circumstances (including destructive failure). The Siemens Y-class capacitors used here are only available in values up to 33 nF. Although selecting a set of component values for the common-mode filter may appear to be as difficult as squaring the circle, it has turned out to be quite easy.

The values of the parasitic components depend not only on the construction of the actual components used, but also on the capacitive coupling of the filter with its surroundings and the inductive coupling between the input and output leads. For this reason, (multistage) filters intended to achieve very high attenuation are always housed in well-screened tinned-metal enclosures. Such enclo-

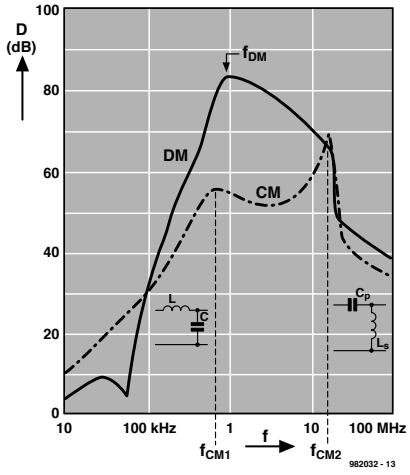


Figure 3. Attenuation characteristics for common-mode noise (dashed line) and differential-mode noise (solid line).

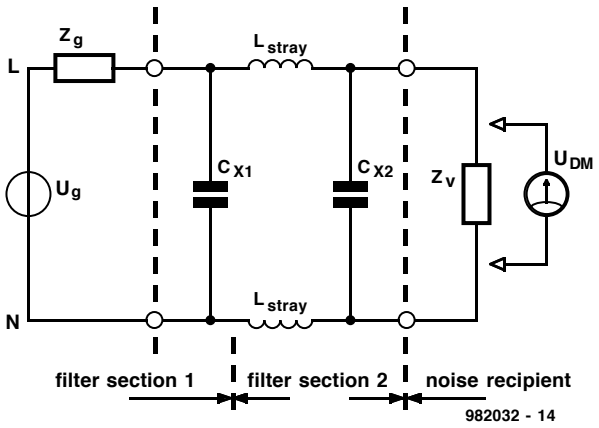


Figure 4. Equivalent circuit for differential-mode noise. The source impedance and input capacitor form the first filter stage.

sures are divided into several isolated compartments for the individual filter sections.

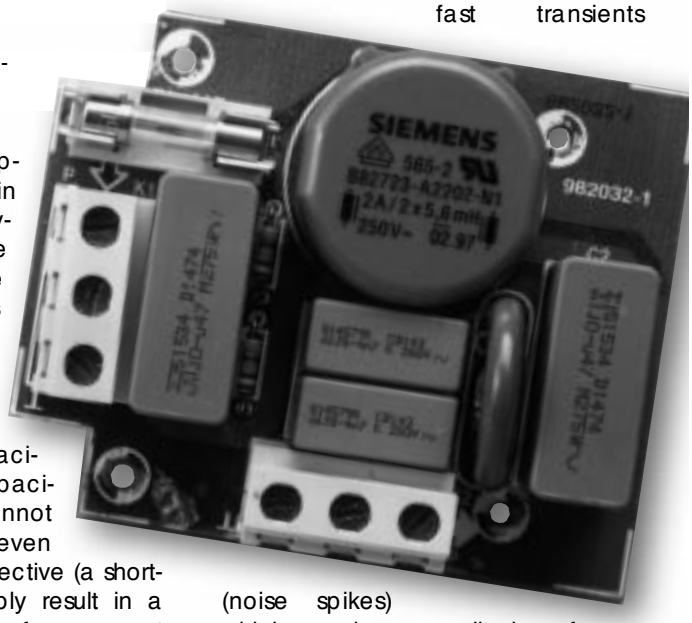
Antiphase operation

The impedance of the mains network is negligibly small at low frequencies. For higher-frequency differential-mode noise the source impedance can reach values of more than 100 Ω, which makes it a significant factor with regard to the mains filter. As shown in **Figure 4**, the combination of the source impedance Z_g and the capacitor C_{x1} forms a 6-dB low-pass filter with a relatively high corner frequency ($f_{-3dB} = 1/2\pi Z_g C_{x1}$). For differential-mode noise the current flows in opposite directions through the two windings of the choke, so that the opposing magnetic fields cancel each other out. Differential-mode noise currents thus see only the small stray inductance of the windings (L_{stray}), which results from imperfect coupling and amounts to roughly 1% of the nominal inductance. The value of C_{x2} is chosen to be a factor of 100 times that of C_y in order to shift the attenuation curve for differential-mode noise to the same frequency range as that for common-mode noise. EMI-suppression capacitors in the X class (MKT or polyester) meeting the EN132400 standard are available with values up to 2.2 µF in the series which is used here. Significantly smaller demands are placed on X-class capacitors than on Y-class capacitors, since they cannot cause much damage even with when they are defective (a shorted capacitor will simply result in a blown fuse). With this set of component values, the effect of the relatively small C_y in parallel with C_x is not significant. The reactive current is of course rather large due to the large value of C_x, but this does not have much effect on the ELCB.

Safety measures

The mains filter presented here, whose complete schematic is shown in **Figure 5**, includes certain components which assure additional safety. The first of these is the fuse F1, which limits the current to the allowable nominal value for the balanced choke (2 A). The two resistors R1 and R2 serve to quickly discharge C1 and C2 when the mains plug is pulled. **Be sure to use two series-connected resistors as indicated**, since a single (470-kΩ) resistor is normally not suitable for connection across the mains voltage.

We now come to the last of the three functions of the filter: *overvoltage protection*. As can be seen from the attenuation characteristics, the filter has practically no effect on high-frequency noise. This also applies to fast transients (noise spikes) which can have amplitudes of up to several kilovolts and durations of 0.1 µs to 1 ms. In order to tame such disturbances it is fully adequate to connect a varistor (a voltage-depen-



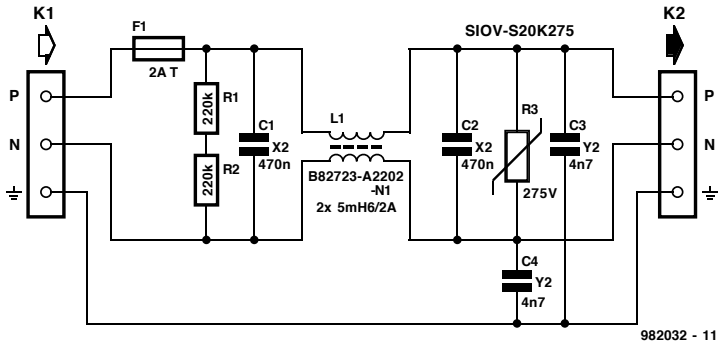


Figure 5. The complete schematic diagram of the mains filter with its nine components.

COMPONENTS LIST

Resistors:

R1,R2 = 220 kΩ
R3 = 275V SIOV-S20k275 (Siemens)

Capacitors:

C1,C2 = 470nF 250VAC class X2, Siemens B81133-D1474M000
C3,C4 = 4nF7 250VAC class Y2, Siemens B81121-CB143

Inductor:

L1 = 2 x 5.6mH/2A 250VAC, Siemens B82723-A2202-N1

Miscellaneous:

F1 = fuse, 2A slow, with PCB mount holder.
K1,K2 = 3-way PCB terminal block, pitch 7.5mm.
Case: Bopla SE432DE.
PCB, order code 982032-1, see Readers Services page.

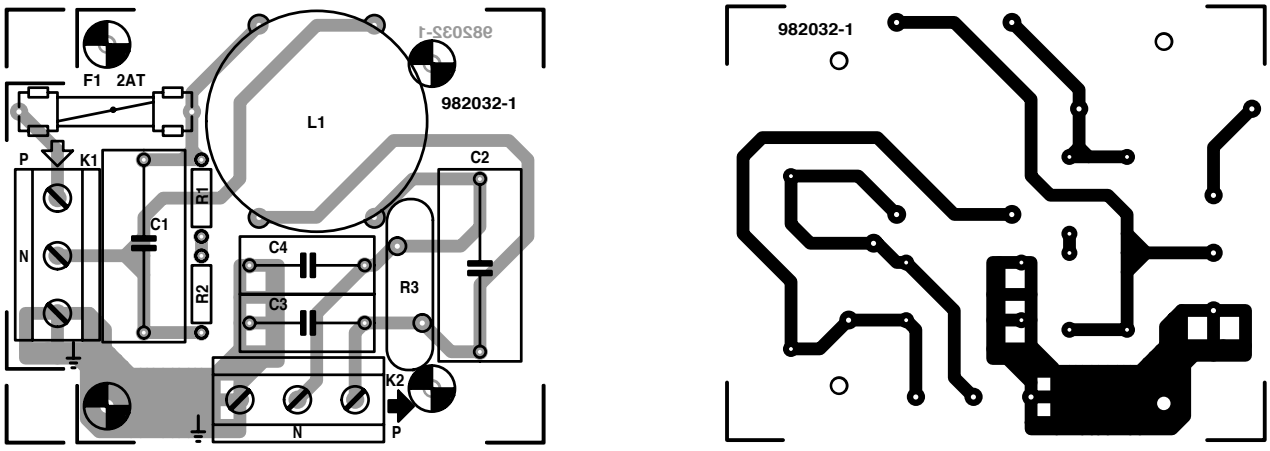


Figure 6. The circuit-board layout guarantees a safe construction in a mains-plug enclosure.

dent resistor) across the mains lines. Such a component has a very high resistance for voltages lower than its rated voltage, and a very low resistance for voltages above this value. Considering the allowed tolerance for the mains voltage (and for the varistor characteristics) a nominal varistor voltage of 275 volts appears to be appropriate. For the varistor to do its job properly, a series resistance is necessary to 'absorb' the excess voltage. The source impedance of the mains network, which rises with increasing frequency, comes into play here. In the frequency range in question (10 MHz and above), the source resistance Z_g is greater than 150 Ω, which is more than enough for proper operation of the varistor.

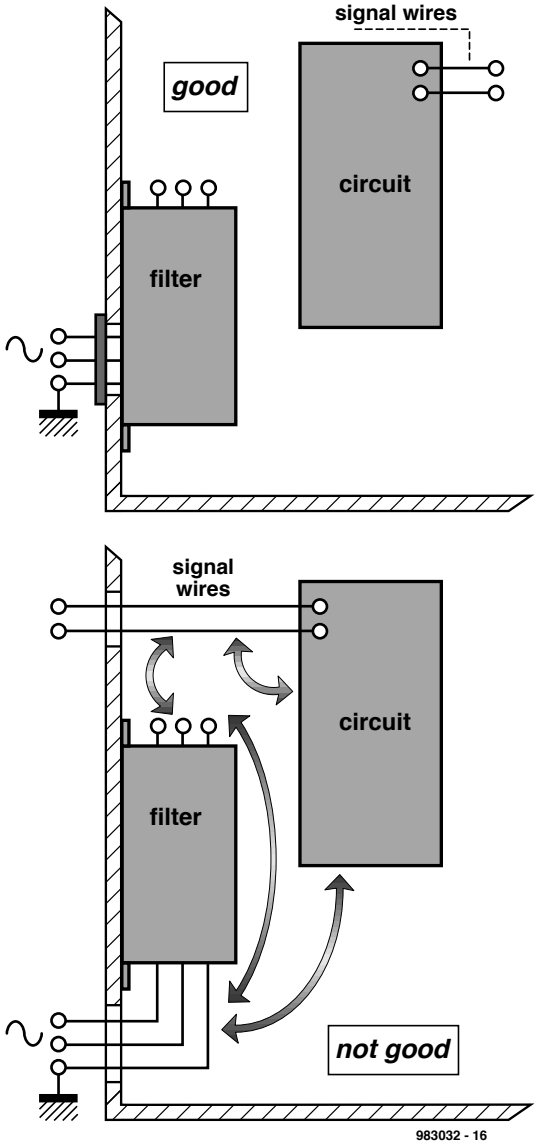


Figure 7. Good and bad ways of mounting of a fully screened mains filter in an equipment enclosure.

Construction and use

We have developed a circuit board for the mains filter (**Figure 6**) with a layout which meets all applicable safety regulations. Mounting the individual components is no problem, but the following must again be emphasised:

Use only the components which are specified in the components list. Only these components (as opposed to 'standard' types) meet the rather strict safety requirements for this project!

The circuit board for the filter should be built into a enclosure with a mains plug and socket in such a way that the plug and socket do not sit directly across from each other. The mounting holes of the circuit board do no allow this with the specified enclosure. In order to keep the crosstalk between the input and output as small as possible and meet the specified attenuation values, the input and output leads should be kept well away from each other. The attenuation factors of commercial mains filters cannot be achieved with a plastic enclosure. One should therefore consider using a tinned-metal enclosure if the filter is to be permanently integrated into a piece of equipment. The manner in which the filter is mounted is then critical. Refer to **Figure 7**, which shows what can go wrong and how to do it right.

(982032)

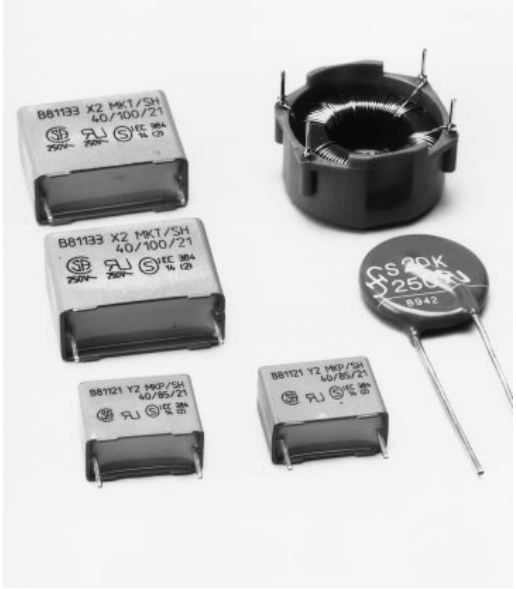
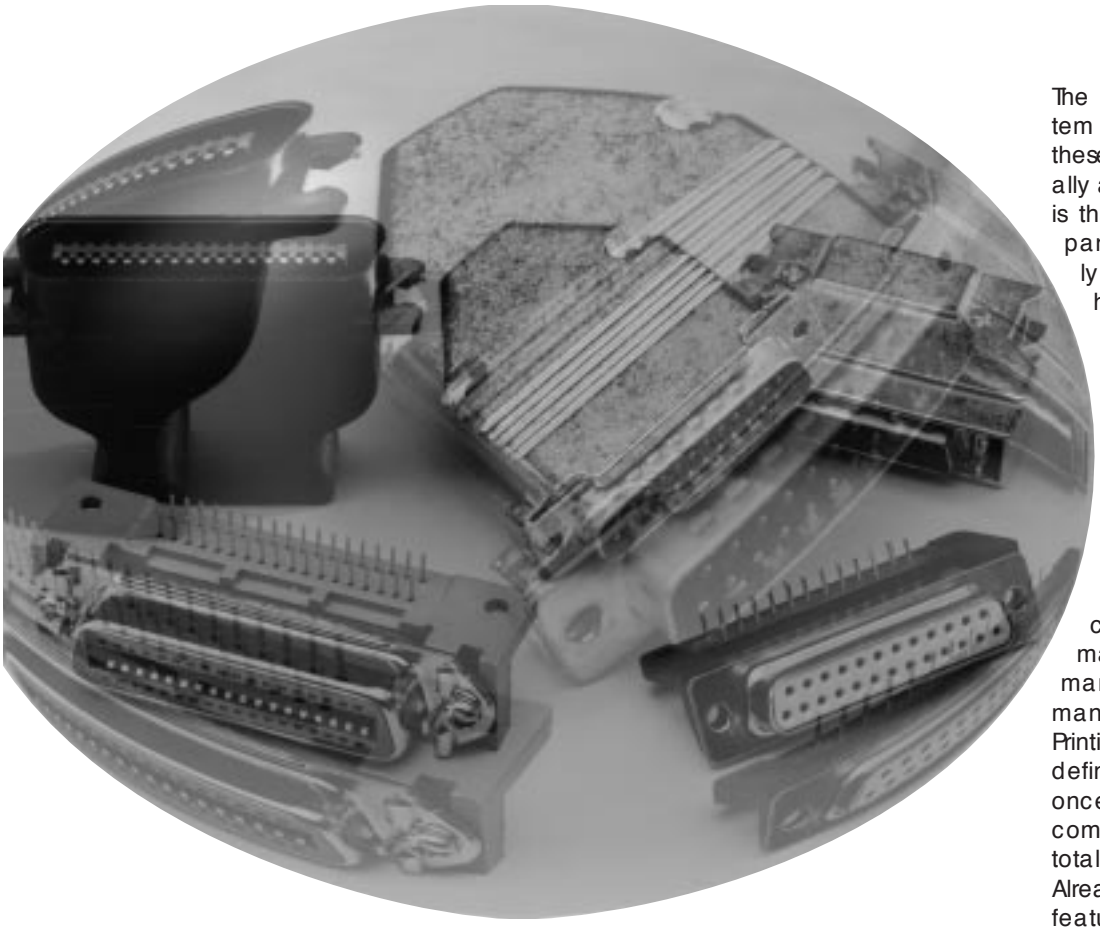


Figure 8. Only these special components may be used in the construction of the mains filter!

Every modern computer has an advanced IEEE 1284 parallel port. Thanks to this interface, the printer port can be used for more than just driving a printer. In some respects, the performance of this interface comes close to that of an 8-bit SCSI interface.

The modern printer port

IEEE 1284 is quickly gaining ground



The standards for the modern bi-directional printer port are laid down in the document "IEEE Std. 1284-1994, Standard Signalling Method for a Bi-directional Parallel Peripheral Interface for Personal Computers". This standard is a conceptual description of a very fast bi-directional parallel connection which with regard to data communication is 50 to 100 times faster than the original parallel port. Yet the new port is still compatible with the older parallel port and the printers which can be connected to it. Before looking at the principles of IEEE 1284, it's a good idea to re-examine the standard parallel interface.

IBM chooses

When IBM introduced the PC in 1981, they opted for a fast 8-bit parallel interface for driving the printer. This approach was preferred to a serial interface (RS232), which was very popular at that time.

At the time of the PC's introduction the printer was the most important 'client' for the parallel port. In the meantime there have been many technological developments, and the parallel port is now used to connect the PC to scanners, CD-ROM players, portable disk drives, tape streamers and other PCs, as well as to printers.

The problems which have faced system designers in the development of these new applications can be generally attributed to three factors. The first is that the performance level of the parallel port has been stuck at roughly 150 kbytes per second, while PCs have become increasingly powerful. The second is that there is no standard for the electrical interface, which results in compatibility problems between various platforms. Finally, due to the lack of standards the maximum practical cable length is limited to about 1.5 metre.

In 1991, printer manufacturers got together and started discussing a new standard. These manufacturers, which included Lexmark, IBM, Texas Instruments and many others, created the Network Printing Alliance (NPA). The NPA in turn defined a number of features which, once they were implemented in the computer and the printer, would allow total control over the printer.

Already during the definition of these features it became clear that this objective could only be realized if a high-performance parallel port was built into the PC. The standard parallel port could not be used for this purpose.

In response to an invitation from the IEEE, the NPA ultimately developed a new standard for a high-speed bi-directional printer port. The preconditions were that the new port must be hardware- and software-compatible with the existing port and that it must be able to achieve a data transfer rate of at least 1 Mbyte/s in each direction. The working group was assigned the name "IEEE 1284" and the resulting standard, IEEE 1284, was established in March of 1994.

The parallel port

The parallel port of a PC utilizes 17 signal lines and 8 earth lines. The signal lines are divided into four control signals, five status signals and eight data signals.
In the basic concept, the control lines serve for driving the printer and providing the 'handshaking'. The status lines also play a role in the handshaking, and in addition they provide the 'Busy' signal and indicate error conditions in the interface or peripheral device. Finally, the data lines are used to transfer data from the PC to the printer. Some time after its introduction, the port was slightly improved to allow bi-directional data transfers.
The first column of Table 1 lists the signals which are used with the Standard Parallel Port (SPP). The port itself receives an address in the PC's I/O space, where it utilizes three locations. The base addresses of these ports, which are often referred to as LPT addresses, are $3BC_H$, 378_H and 278_H respectively. Newer implementations of the parallel port, which support the advanced-mode features of the IEEE 1284 standard, use 8 to 16 locations starting at I/O address 378_H or 278_H. The addresses may also be adaptable, as for example with a 'Plug and Play'-compatible parallel adapter card.

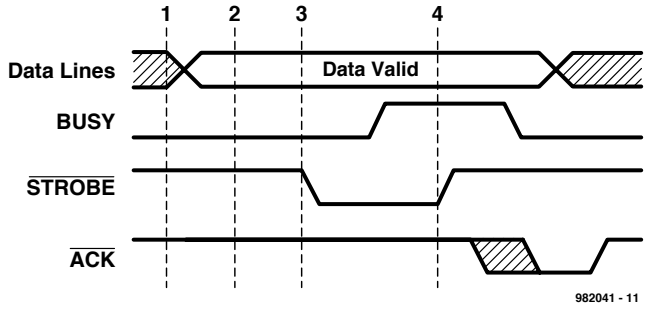


Figure 1. The timing of the standard parallel port (SPP).

Table 1. Signal definitions.

SPP-Signaal	Nibble Mode	Byte Mode	EPP Mode	ECP Mode	Pin (DB25)	In/Out
Strobe\	Strobe\	HostClk	Write\	HostClk	1	Out
AutoFeed\	HostBusy	HostBusy	DataStb\	HostAck	14	Out
SelectIn\	1284Active	1284Active	AddrStb\	1284Active	17	Out
Init\	Init\	Init\	Reset\	ReverseRequest\	16	Out
Ack\	PtrClk	PtrClk	Intr\	PeriphClk	10	In
Busy	PtrBusy	PtrBusy	Wait\	PeriphAck	11	In
PE	AckDataReq	AckDataReq	UserDefined	AckReverse\	12	In
Select	Xflag	Xflag	UserDefined	Xflag	13	In
Error\	DataAvail\	DataAvail\	UserDefined	PeriphRequest\	15	In
Data[8:1]	NotUsed	Data[8:1]	AD[8:1]	Data[8:1]	2-9	

\ = actief laag niveau

IEEE 1284: the approach

Several different communication modes are defined in the IEEE 1284 standard. For example, the Compatible and Nibble modes can be realized with any existing parallel port. They allow data to be exchanged in two directions. The Compatibility and Byte modes allow a bi-directional data channel to be opened, but a prerequisite is that the ports used must support the Byte mode. In practice this means that it must be possible to read a data byte from the external data lines. This is usually implemented by incorporating a direction bit in the control register. Ports which provide this support are commonly called 'bi-directional' parallel ports. The EPP and ECP modes support two-way communications, since this is part of their protocol. However, these modes require that the hardware includes arrangements for automatically generating the handshaking signals which are necessary for high-speed data transmissions.
Finally, it should be noted that with the exception of the Compatibility mode, each mode renames the status lines to correspond to the functions which they have within that mode.

Five modes

If we look more closely at the IEEE 1284 standard, we see that there are five modes which are defined in the standard. Each of these has its own communications possibilities. For communication from the PC to the printer the Compatibility mode is available, and communication from the outside world toward the computer is possible with the Nibble mode (4-bit data, compatible with Hewlett-Packard Bi-tronics) and the Byte mode (8-bit data). Two-way traffic is possible with the EPP and ECP modes.
The EPP (Enhanced Parallel Port) mode is intended to be used in combination with devices other than printers, such

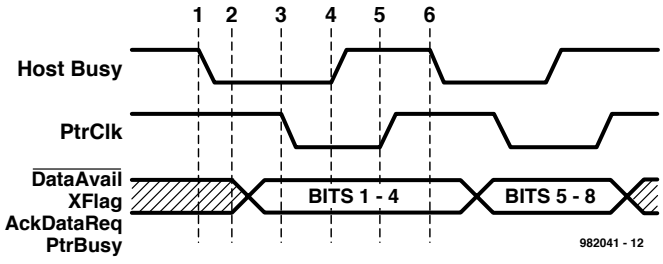


Figure 2. Nibble-mode data transfers. Two cycles are necessary to send a single 8-bit byte.

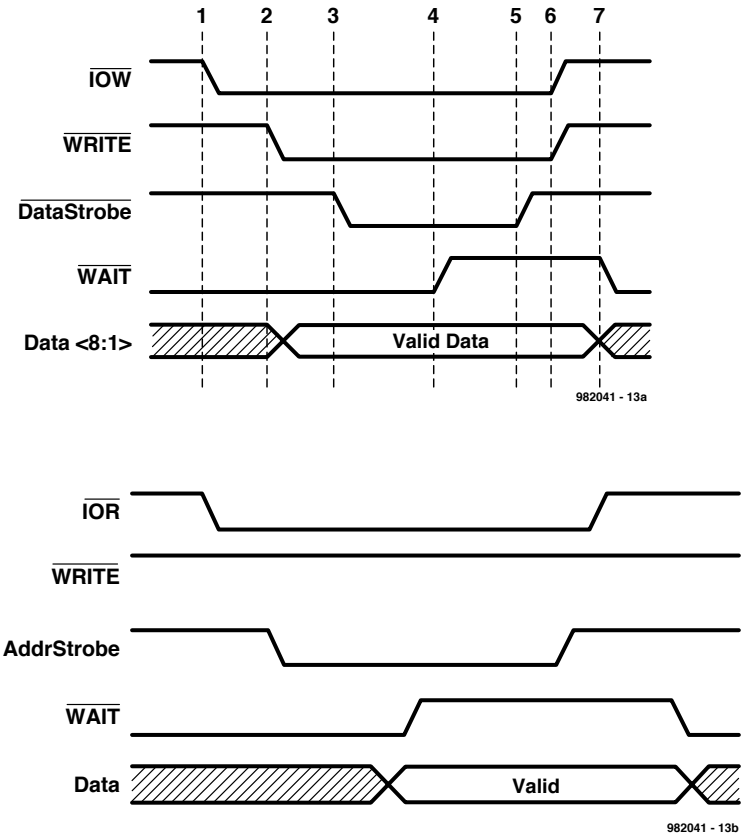


Figure 3. Timing of Data_Write and Address_Write cycles in the EPP mode

as (for example) CD-ROM drives, tape streamers, hard-disk drives, networks and so on. The ECP (Extended Capability Port) mode is an improved printer port which can be used with a new generation of printers and scanners.
The most important difference between the Compatibility, Nibble and Byte modes on the one hand and the EPP and ECP modes on the other hand is that with the first group the software is responsible for handling the complete communications protocol, while with the second group the handling of data communications is in many cases almost completely implemented in hardware (in the form of 'super-I/O' chips). Thus with EPP mode a simple OUT instruction is all that is needed to dispatch data to a peripheral device.

Compatibility mode

This mode defines a protocol which the PC can use to send data to the printer. This protocol is commonly known as the 'Centronics interface', named after the manufacturer which originally developed the interface. In this mode, data are first placed on the data lines and then the status lines are checked to see whether the Busy line is active or the printer has reported an error. After this, a strobe pulse is issued. Figure 1 depicts the timing of the Compatibility mode. In practice, the maximum speed which can be achieved with this interface is 150 kbyte/s.
Many of the integrated-circuit 1284 controllers use a FIFO to manage the data handling in the Compatibility mode. This arrangement is often described as 'fast Centronics' or 'parallel port FIFO mode'. If this feature is available, then the hardware takes care of generating the strobe pulses and manages the complete handshaking process. In this way it is possible to achieve data transfer rates of 500 kbyte/s. However, you must keep in mind that this feature is not part of the IEEE 1284 standard.

Nibble mode

The Nibble mode is the method which is most commonly used when data must be sent from the outside world to the PC. It is often combined with the Compatibility mode in order to realize a bi-directional channel. Five lines of the standard parallel port are used to transfer data from a peripheral device to the PC. The peripheral device uses these lines to send each data byte (8 bits) as two successive 4-bit nibbles. **Figure 2** shows the timing diagram of Nibble mode. Since the ACK line is normally used to allow the peripheral device to communicate with the PC, the bits which are packed into each nibble are recovered from the status register, but they are not arranged here in a 'logical' order. The software thus has to do quite a bit of translation in order to rearrange the bits in the correct sequence. The second column of **Table 1** shows how the SPP signal lines are used in the Nibble mode.
The Nibble mode is the most 'compute-intensive' with respect to the software. For this reason the data transfer rate is rather low: at most roughly 50 kbyte/s. Such a low data rate is a problem for fast peripheral devices such as LAN adapters and CD-ROM drives. The most important advantage of this mode is that it can be used on every PC (old and new).

Byte mode

In later versions of the parallel port, the manufacturers switched over to chips which made it possible to use the printer port in both directions. With such an interface, a peripheral device can send data to the PC eight bits at a time. Splitting each byte into two successive transfers, as in the Nibble mode, is thus no longer necessary.
The rate at which the PC can read in data with this mode is comparable to the rate at which it can write data to a peripheral device in the Compatibility mode. Column 3 of **Table 1** shows how the SPP signal lines are used in the Byte mode.

EPP mode

The Enhanced Parallel Port (EPP) mode was originally developed by Intel, Xircom and Zenith Data Systems as a parallel port which is compatible with the standard printer port but which has a higher level of performance. Intel built the protocol which is used for this mode into the 386SX chip set (82360 I/O chip). This development occurred before IEEE 1284 was initiated.
The EPP protocol had many advantages, and was quickly adopted by many manufacturers. A group of 80 manufacturers ultimately took the initiative to extend and promote the protocol. Subsequently, care was taken to see that this protocol was adopted by the IEEE 1284 group and incorporated into the standard as one

Table 2. EPP register definitions.

PortName	Offset	Mode	Read/Write
SPP Data	+0	SPP/EPP	W
SPP Status	+1	SPP/EPP	R
SPP Control	+2	SPP/EPP	W
EPP Address	+3	EPP	R/W
EPP Data	+4	EPP	R/W
Not Defined	+5...+7	EPP	

Table 3. ECP register definitions.

Offset	Name	Read/Write	ECP Mode	Function
000	Data	R/W	000-001	Data Register
000	ecpAfifo	R/W	011	ECP Address FIFO
001	dsr	R/W	all	Status Register
002	dcr	R/W	all	Control Register
400	cFifo	R/W	010	Parallel Port Data FIFO
400	ecpDfifo	R/W	011	ECP Data FIFO
400	tfifo	R/W	110	Test FIFO
400	cnfgA	R	111	Conf. Register A
401	cnfgB	R/W	111	Conf. Register B
402	ecr	R/W	all	Extended Control Register

Table 4. ECP register modes.

Mode	Description
000	SPP mode
001	Bi-directional mode
010	Fast Centronics
011	ECP Parallel Port mode
100	EPP Parallel Port mode
101	(reserved)
110	Test mode
111	Configuration mode

of the improved modes.
There four ways in which data can be sent in the EPP mode:
1 Data_Write cycle,
2 Data_Read cycle,
3 Address_Write cycle,
4 Address_Read cycle.
The purpose of the data cycles is to exchange data between the computer and a peripheral device. The address cycles are used either for address, channel or control information or for commands. **Table 1** also shows (in column 4) how the signal lines are used in EPP mode. **Figure 3** shows the timing diagrams for an EPP Data_Write cycle and an EPP Address_Read cycle.
One of the most important advantages of this type of port is that the whole data transmission can be handled by a *single* ISA I/O cycle. The transmission rate can thus range up to a maximum of 2 Mbyte/s. In this way the printer port can achieve a speed which is comparable to that of an interface on an ISA card.

ECP mode

The most powerful mode used with the parallel port is the Extended Capability Port (ECP) mode. The protocol for this comes from Microsoft and Hewlett-Packard. It is intended to be a very advanced communication option between a PC and peripheral devices such as printers and scanners. The ECP mode allows high-speed bi-directional communication between the PC and the peripheral equipment. There are two types of cycles in the ECP protocol:

1 data cycle,
2 command cycle.

The command cycle can be further divided into two types: Run Length Count and Channel Address. Let's now see what these mean in practice.
In contrast to the situation with EPP, a standard register arrangement was proposed as part of the ECP protocol. This arrangement is described in the document "The IEEE 1284 Extended Capabilities Port Protocol and ISA Interface Standard", which was published by Microsoft. This document describes supplementary features and functions which fall outside the scope of the IEEE 1284 standard. In this regard it is worth mentioning the following: Run Length Encoding (RLE) data compression for computers, FIFOs for data channels in both directions, and DMA and programmed I/O for the computer.
With the aid of RLE, a data compression factor of 64:1 can be achieved. This is ideal for scanning and printing applications in which large blocks of identical information can occur in data files.
Channel Addressing is conceptually an extension of the addressing scheme used in EPP. This technique is used to allow multiple functions to be housed in a single physical enclosure. For example, consider the combination of a printer, fax and modem. Connecting a *single* piece of equipment to a *single* parallel port then effectively results in having three separate functional devices available: a printer, a fax and a modem. Thanks to the channel protocol, data can be received from the modem at the same time that the printer is busy printing out a document.
In the ECP mode a number of new functions are assigned to the signal lines of the SPP interface. **Table 3** shows the new register structures that are used in the ECP mode.
The Microsoft specification defines a number of common registers for IEEE

Figure 4. The three types of connectors which are allowed by the IEEE 1294 standard.

1284 adapters connected via the ISA bus and also support ECP. It additionally specifies a number of modes that the adapter must support. These are summarized in **Table 4**.

The ECP register model is comparable to that of a standard parallel port, but it also makes use of an important feature of the ISA interface. In the standard IBM architecture only the first 1024 register or I/O addresses are used. This is the address space starting at $0x000_H$ and ending at $03FF_H$. Ten address bits (AD0:9) are required to address this region.

In order to keep costs down, the hardware of older-model ISA cards uses signals from the ISA bus to help in decoding the address. This 'automatically' limits the number of addressable registers to 1024. PCs that are more modern decode more address bits and thus have a larger I/O address space available. A consequence of this is that locations in the first 1K block of the address space can be doubly addressed, since the limited address-decoding logic of older-model ISA cards generates 'mirror' addresses in this block from higher-level addresses. Software can address the new register banks by adding 1024 ($0x400_H$) to the base address which is used. The new addresses thus lie outside of the original 1K address region, but in fact they are 'mirrored' back into this region. For example, selecting addresses $0x378_H$ and $0x778_H$ with newer types of ISA cards gives access to two different registers located in two different banks, while with older-model cards these two addresses will both access the same register.

The advantage of this technique (which is called *aliasing*) is that new cards can have 'invisible' registers and thus can increase the maximum number of available registers. With this approach, other I/O registers located on other cards will never be disturbed. In this way the new cards remain compatible with the older cards, which can only decode 10 address bits.

The ECP register model makes use of the aliasing technique. It defines six registers that use only three I/O addresses (see **Table 3**). Two registers located at addresses $0x000_H$ and $0x400_H$, respectively, have somewhat different names and functions depending on the ECP mode in which they are used, as can be seen from the table. The fourth and fifth columns of **Table 3** list the various ECP modes and identify the functions these registers have for each mode. The actual mode must always be selected in advance by writing one of the mode codes to register $0x402_H$.

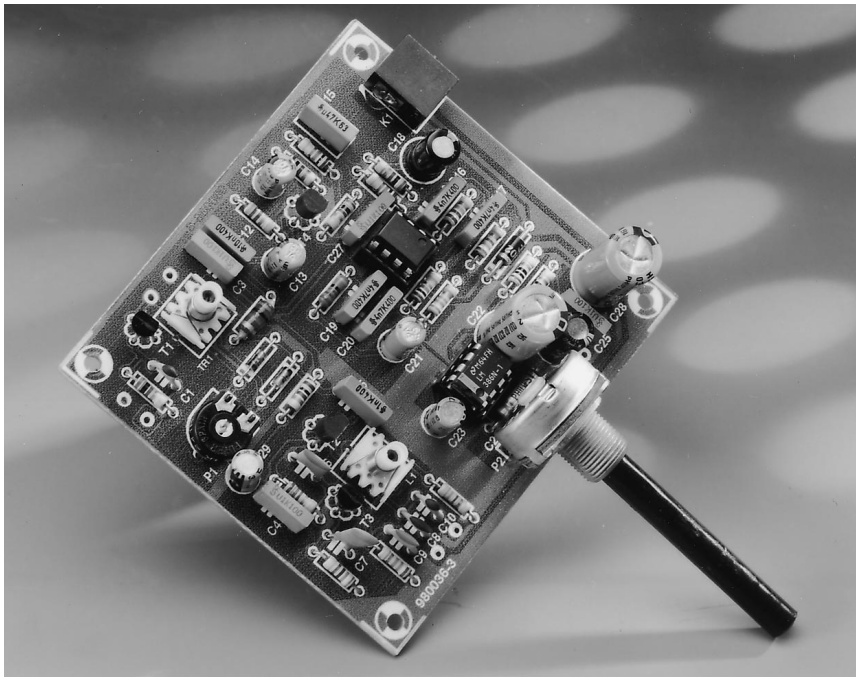
Connectors

The IEEE 1284 standard does not limit itself to defining the structures of the ports and the electrical signals to be used. The mechanical specifications of the connectors to be used are also included in the standard.

Three different types of connectors (types A, B and C) are proposed in the standard. Type A is a 25-pin sub-D connector, which is long since a familiar feature of the PC. Type B is the well-known 36-position Centronics connector, which can be found on many printers. Type C, a miniature 36-pin connector with retaining clips, is especially intended for use in new designs. This last type of connector takes up less space on the circuit board, and it is easily attached and removed thanks to the retaining clips. An additional important advantage of this connector is that with it two additional signals are added to the interface: Peripheral Logic High and Host Logic High. These signals can be used to ascertain whether the equipment at the other end of the cable is powered on. In this way a certain degree of power management is made possible by the IEEE 1284 standard. (982041)

20-metre SSB/CW receiver

a budget receiver based on direct conversion



The receiver described here is of the Direct Conversion type and is designed for the 20-metre band or, in new money, 14 MHz. The components used are readily available from the junk box or can be modified from standard components. The whole idea of building simple radio projects is that they can be constructed from the bits and pieces found in the shack (a shack is a radio amateur's shed).

By Eric Edwards GW8LJJ

The 20-metre amateur radio band (14 MHz to 14.350 MHz in IARU Region 1) is great for daytime DXing. During periods of increased sunspot activity, the band is 'open' all the time, and the 20-m band is buzzing with activity. When there is little or no solar-flare activity, the band is still usable for medium-distance communication during daytime hours and at sunrise and sunset. Because the so-called MUF (maximum usable frequency) only exceeds 14 MHz around noon during the winter months, a fairly large skip zone has to be taken into account. Unfortunately, discussions on the intricacies of radio wave propagation and the impact of the solar cycle on radio communication are beyond the scope of this article. The good news, however, is that there are excellent books available on these subjects.

CIRCUIT DESCRIPTION

The circuit diagram shown in **Figure 1** may appear to be rather complicated at first blush. There are four sub-circuits.

The RF part is concerned with the receiving of the signal. It consists of two sub-circuits: **RF amplifier and filter**, T1-L3-C2, and a **VFO** (variable-frequency oscillator) T3-L1-C11. The **band-pass filter** around IC1 serves to clean up the received signal and make it much better to listen to. The fourth essential building block is the LM386 **audio amplifier**, which raises the cleaned signal to loudspeaker level.

Inductors L1 and L3 are home made and the two tuning capacitors in the receiver are preferably made from tuning capacitors having larger capacitance values — more about this further on.

The received signal from the aerial is fed into the source of a FET-based RF amplifier, T1, configured in grounded-gate mode to present a low impedance to the aerial. The amplified signal is tuned to the desired frequency by means of inductor L3 and variable capacitor C2. This selected output is taken to a pair of diodes wired as a balanced mixer. The other signal used for

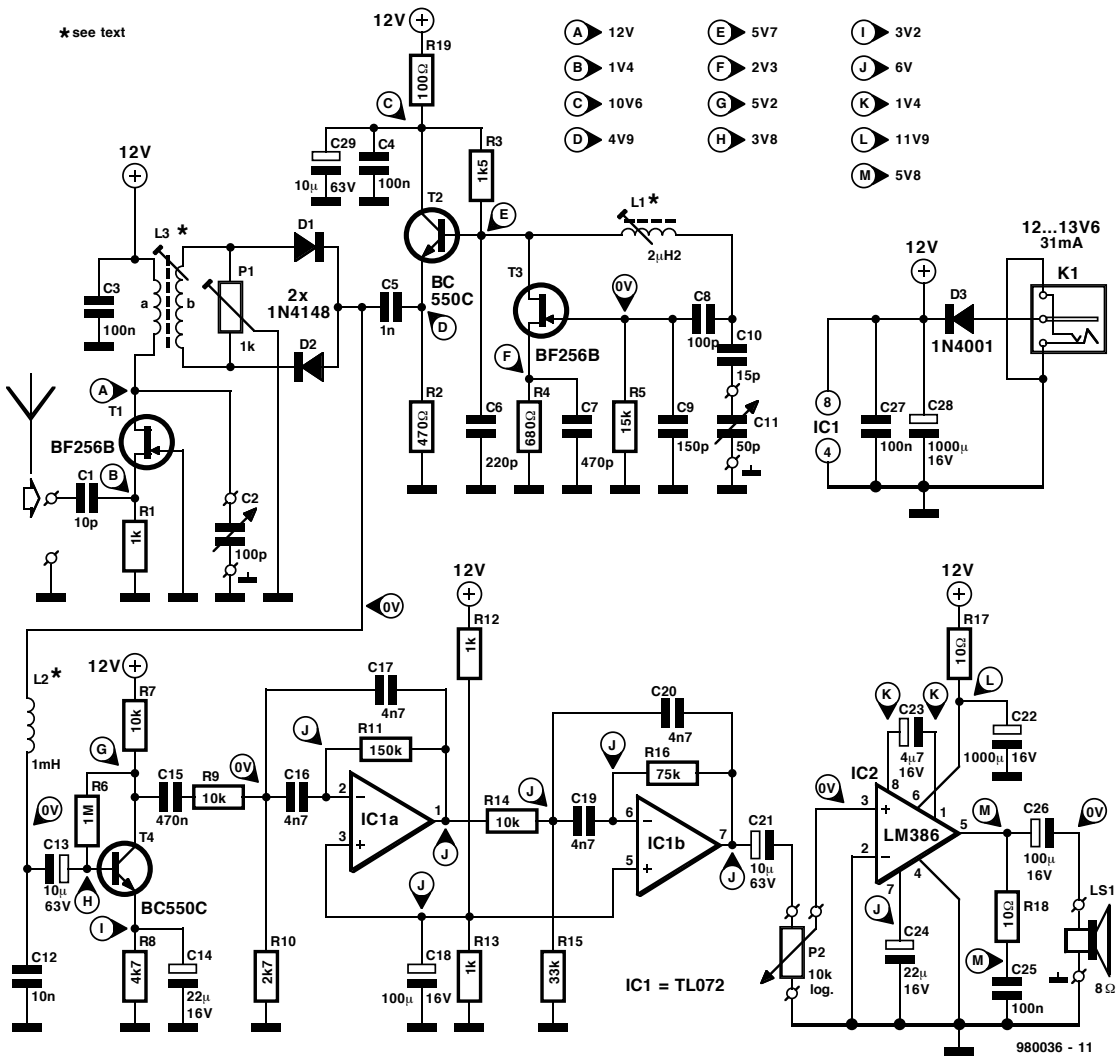


Figure 1. Circuit diagram of the direct-conversion receiver for the 20-metre amateur radio band.

mixing comes from the oscillator tuned by L1 and C11. This signal is tuned to very nearly the same frequency as the RF input signal. The difference is, in fact, the resultant audio output after suitable filtering. The output of the FET oscillator is buffered by a BC550C emitter follower and then fed to the diodes to be mixed with the incoming signal.

The output from the mixer diodes, D1 and D2, is first applied to an RF choke, L2, to remove the RF component from the mixer output signal, allowing the audio to pass through to the band-pass filter.

Across L3b is a preset control, P1, which may also be a good quality potentiometer fitted to the front panel still using stiff wire. It is there to suppress AM stations. Without this control, breakthrough of unwanted commercial stations will render the receiver useless. This receiver is for the reception of SSB (single sideband) and CW (continuous wave; also called Morse code), although I have also used it to receive amateur fax and slow-scan television (SSTV; very popular in the 20-m band).

The band-pass filter (BPF) built around opamps IC1a and IC1b is tuned to a centre frequency of about 2 kHz with a bandwidth of 900 Hz. It is a Butterworth 4-pole type. Basically, the filter will allow a 2-kHz signal to go down a path 900 Hz wide to get to the audio amplifier. In this process of filtering, all the unwanted stuff is removed, including high-pitched whistles (which only your dog could hear), and low frequency hum that is only good for the older valve radio (or wireless). It also ensures all the remaining RF is removed. The filter provides the gain that is so essential to this type of receiver. The older passive type of filters using coils and capacitors introduces losses, so this design was chosen because of its advantages and easily available cheap components.

The filtered output signal goes to the top end of the volume control, P2. The wiper is taken to pin 3 of the LM386 audio output amplifier. An R-C supply decoupling network, R17-C22, provides the LM386 with a clean supply voltage.

BUILDING THE RECEIVER

The 100-pF variable tuning capacitor, C2, may either be obtained from a Radio Rally (there are quite a few of these all over the country all year round), or one can be specially purchased (although the price would be pretty high). Alternatively, get hold of a 250-pF variable capacitor as used in old radios, signal generators etc. or obtain one from a Rally if you cannot get a 100-pF at a sensible price. The vanes of these capacitors are usually crimped onto the main spindle. With a good pair of pliers, grip one of the inside vanes and tug at it until it pulls free. If whilst tugging away at one of these vanes you start to look like someone entering G-force, give up as it is probably welded (I haven't come across any that were). Remove every other until you only have half the number of vanes left. If your capacitor is of the gang type, i.e., it has more than one set of tuning vanes then you need only remove vanes from one of these sections. If you have a capacitance meter, you can at this stage check your capacitor value. It does not have to be exact because the iron dust core in the coil will adjust allowing for this. Carry out the same procedure for C11, the VFO variable capacitor, only removing more vanes to reduce the capacitor value

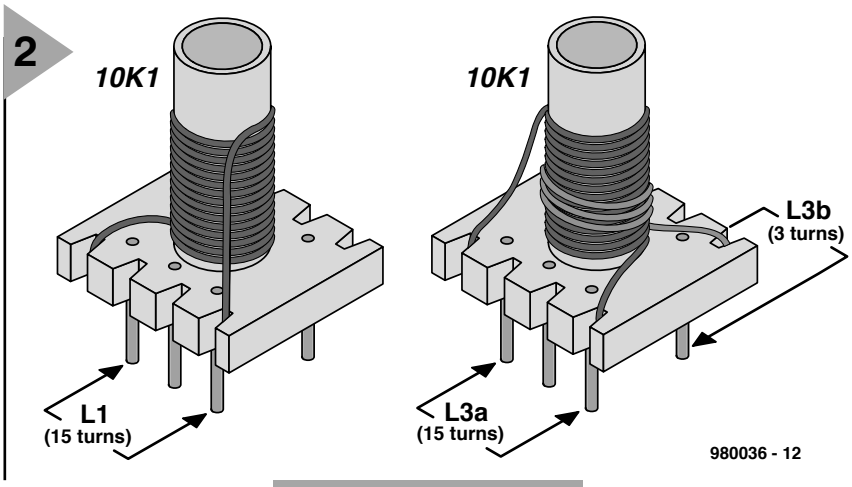


Figure 2. Illustrating the construction of the two home-made inductors in the receiver.

even further. C2 could be of the trimmer type providing it has a spindle to attach a control knob. Actually, the same could apply for C11 as well, providing it will allow the fitting of a slow-motion dial control. After you have removed the vanes, check for short circuits caused by bent vanes. The tuning capacitors should be connected to the board using the shortest possible wires.

Inductors L1 and L3 are made from

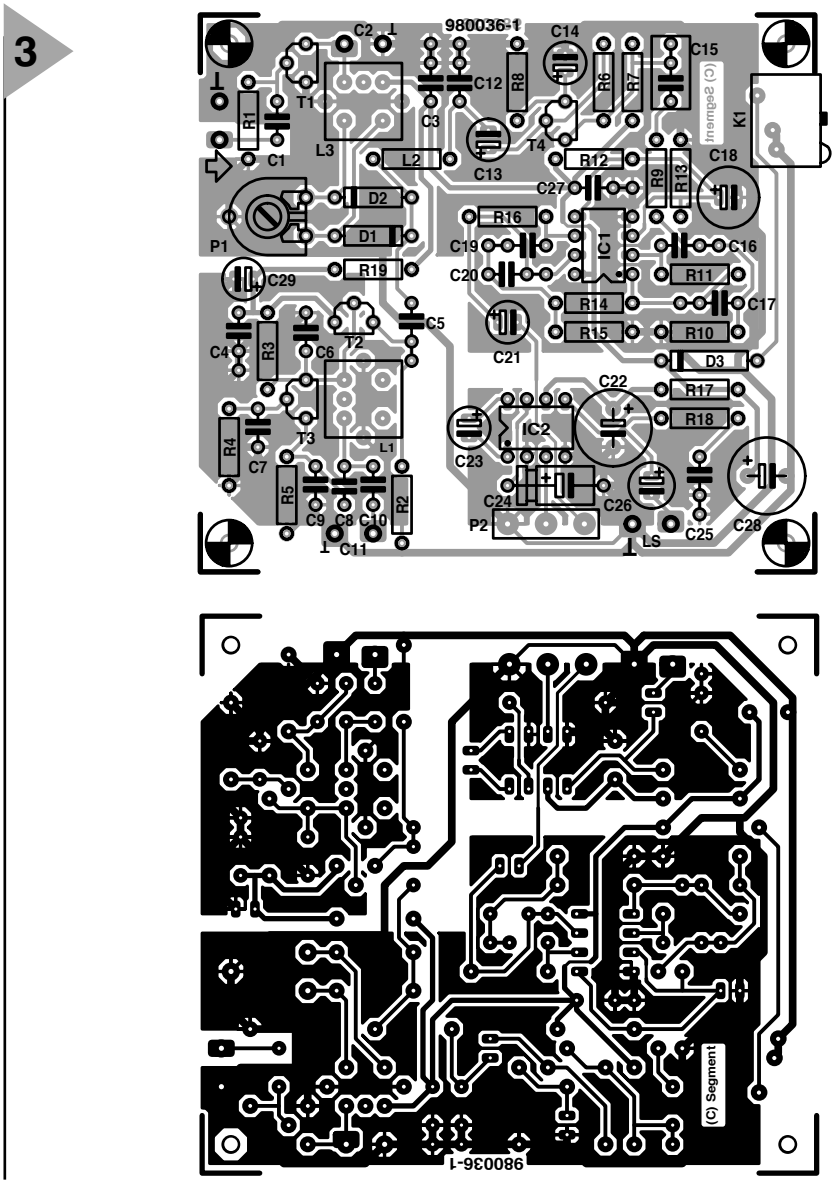


Figure 3. Artwork for the (single-sided) printed circuit board (board available ready-made, see Readers Services page).

COMPONENTS LIST

Resistors:
R1,R12,R13 = 1kΩ
R2 = 470Ω
R3 = 1kΩ5
R4 = 680Ω
R5 = 15kΩ
R6 = 1MΩ
R7,R9,R14 = 10kΩ
R8 = 4kΩ7
R10 = 2kΩ7
R11 = 150kΩ
R15 = 33kΩ
R16 = 75kΩ
R17,R18 = 10Ω
R19 = 1kΩ preset H
P2 = 10kΩ logarithmic potentiometer

Capacitors:
C1 = 10pF
C2 = 100pF variable capacitor or trimmer (see text)
C3,C4,C25,C27 = 100nF
C5 = 1nF
C6 = 220pF
C7 = 470pF
C8 = 100pF
C9 = 150pF
C10 = 15pF
C11 = 50pF variable capacitor or trimmer (see text)
C12 = 10nF
C13,C21,C29 = 10µF 63V radial
C14 = 22µF 16V radial
C15 = 470nF
C16,C17,C19,C20 = 4nF7
C18,C26 = 100µF 16V radial
C22,C28 = 1000µF 16V radial
C23 = 4µF7 16V radial
C24 = 22µF 16V

Inductors:
L1 = 15 turns, 36 SWG (0.2 mm dia) enamelled copper wire on Neosid 10K1 coil assembly (purple core). Alternatives; 10T1 (yellow core), 10F1 (blue core).
L2 = 1mH choke (see text)
L3 = primary 15 turns; secondary 3 turns, 36 SWG (0.2 mm dia.) enamelled copper wire on Neosid 10K1 coil assembly. Alternatives: 10F1 and 10T1.

Semiconductors:
D1,D2 = 1N4148
D3 = 1N4001
T1,T3 = BF256B
T2,T4 = BC550C
IC1 = TL072CP
IC2 = LM386N-1

Miscellaneous:
K1 = mains adaptor socket, PCB mount
Printed circuit board, order code 980036-1, see Readers Services page.
Loudspeaker, 8 Ω, 1 watt

36 SWG (0.2 or 0.25 mm dia.) enamelled copper wire wound on Neosid type 10K1, 10F1 or 10T1 formers. The RF input tuning coil, L3, consists of 15 turns (L3a, primary winding) and 3 turns (secondary winding, L3b). Both are close-wound and connected to the pins of the 10K1 base as illustrated in **Figure 2**. An idea may be to secure the main winding, L3a, with candle wax or super-glue. When set, wind L3b in the same direction on top of and in the centre of L3a. Secure this winding and remove insulation for soldering to the base pins of the plastic former. Check the continuity of the coils at the base pins, and make sure that the screening cans may be fitted later without causing short-circuits with excess solder blobs at the pins.

The RF choke, L2, is a ready-made miniature type. It should be noted, though, that it probably gives inferior performance when compared with a real RF choke removed from some old equipment, probably because of the relatively low Q (quality) factors of those modern miniature chokes. Radio rallies and amateur radio suppliers will have these older (physically larger) types.

The audio amplifier is of a well-proven design with a chip that is economic to buy.

The printed circuit board designed for the receiver has large copper areas at the solder side to reduce stray radiation, and to enable all component leads to be kept as short as possible, which is essential to keep the circuit stable. Use a slow motion dial for the main tuning, and ensure all wiring is rigid, with the receiver built on a solid chassis or framework. Do not use a front panel that bends as you tune or you will never be able to track anyone down. Good rigid construction with neat short wiring is the secret to this good performer.

IN USE

Set the tuning capacitors about half mesh (mid-way) and the coil cores half way down the former, adjusting with a non-metallic tool, otherwise you will be left with iron dust but no core. With the aerial and the all-important earth connected, turn the volume to about half way.

If a signal generator is available, set it to 14.20 MHz. This is centre of the 20-metre band. The output of the generator is connected to the aerial socket of the receiver, and is adjusted so that the signal is heard but not too strong. If no signal is heard and providing all is okay with your construction, tune the main tuning capacitor to bring in the signal. If still nothing is heard, you may be too much off frequency; this is easily detected by swinging the signal generator until a signal is heard. A rewind of the VFO coil may be necessary to solve the problem. In general, however, you should not have trouble in finding the centre of the band. Right you now have the signal from the signal generator, which should be modulated to help resolve it. Reduce the size of the signal until it is just audible, adjust L3 for the strongest signal. You are now ready to try the receiver on air. Remove the signal generator and switch it off. Also switch off your computer because those things generate so much noise you will think your receiver is hyperactive. Hopefully by now you would have picked up a signal off air. Adjust C2 and C11 for the most comfortable reception together with adjustment of the volume control. If AM (Amplitude Modulation) is breaking through, carefully adjust preset P1 (across the diodes) for maximum attenuation. It works!

Throughout the preparation of this article I have been constantly listening to many DX (long-distant) amateur stations in SSB and CW, and have received some very good SSTV pictures from distant stations.

If a signal generator is not available for calibration, a general coverage or ham radio receiver could be used. Place the aerial lead of the commercial receiver near the oscillator circuit of your home-brew receiver, but not too close as to pull the oscillator of your home-brew. This is not as accurate as the signal generator but will give you an idea where you are. Once you are receiving off-air stations, these can be compared with those on the commercial receiver providing that receiver is good enough! The main tuning control does exactly what it states and the RF tune control peaks the signal to maximum. You may have to back this off for those stronger (S9+) signals…

START LISTENING!

Enjoy building and using this little receiver, I think you will be surprised with the results.

One thing to bear in mind whether you are listening on a home-brew or commercial short wave receiver is that the reception is very much affected by the time of day/night and also the time of year. Weather and atmospheric pressure will also affect the reception. Radio amateurs use different frequency bands at different times of the year, day and night.

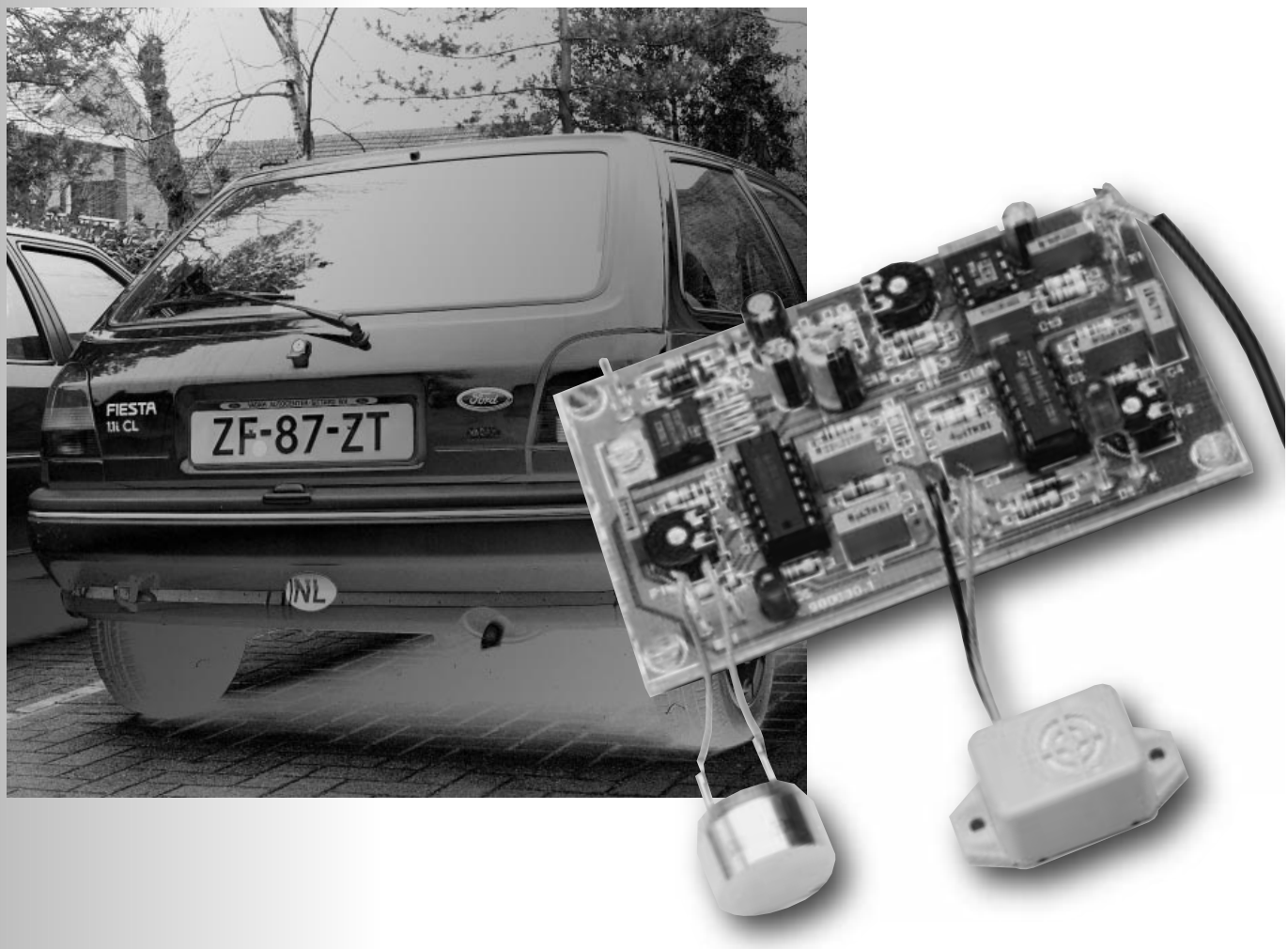
Finally, a directional aerial is much better than a long untuned wire, although you will receive many DX stations with a long wire aerial.

73's and good DX.

(980036-1)

parking sonar

range monitor to make parking safer



Parking in crowded streets often causes one's car to bump into another one. Even though this normally happens at very low speeds, it should be avoided. The range monitor is an aid to 'keeping an eye' on the distance between the bumper of your car and that of the one behind you. It is a compact device that may prevent angry faces.

Design by H Bonekamp

At some time or another, we all have to park our car in a crowded street or car park. Now, parking is something that many of us never master well and consequently tends to make us nervous. The fear is that we will bump our car into the one behind the space we have selected. An aid to warn us when we get too close to that vehicle is, therefore, very welcome.

The circuit described in this article is a fairly straightforward design that actuates an alarm when there is an obstacle at a preset distance of 30–300 cm from the bumper of a vehicle in which it is fitted. Such a distance is fine in all practical conditions. It takes over from a human 'aid' who indicates by means of hand signals how far you can reverse your car.

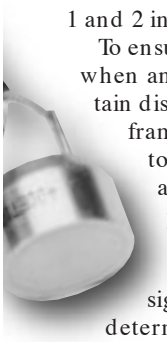
THE DESIGN

The range monitor is based on ultrasonic transducers: a sender and a receiver. It makes use of the natural property that sound travels through air at a virtually constant speed of 340 m s^{-1}. Any obstacle will reflect the sound emitted by the transmitter, which is then intercepted by the receiver. A measurement of the interval between the time the sound is sent and the time the echo is received enables the distance to be computed.

The block diagram of the monitor is shown in **Figure 1**. The frame generator produces rectangular pulses in a fixed rhythm. The width of the pulses determines the duration of the frame. The intervals between the pulses are long enough to prevent signal echoes from interfering with the frames.

The frames are 'modulated' by a 40 kHz signal produced by a second generator. The modulated pulses are then applied to the transmit module. The frequency of 40 kHz is not chosen randomly, but is equal to the resonance frequency of the transducer.

The timing diagram in **Figure 2** clarifies the process. The output of the frame generator and the signal applied to the transmit module are waveforms 1 and 2 in this diagram.



To ensure that an alarm is actuated when an obstacle is present at a certain distance, say, 50 cm, the receive frame must have some relation to the transmit frame. This is arranged by passing the output of the frame generator through a delay line and converting the consequent signal to a pulse whose width determines the window. See signals 3 and 4 in the timing diagram. Note that only signals that fit within the window can be intercepted.

The reflected signal (or echo) is intercepted by the receiver and applied to an amplifier., which not only raises the level of the signal but also functions as band-pass filter. The resulting signal is compared with a fixed voltage: the output of the comparator is signal 5 in the timing diagram. Note that this is identical to signal 2 but shifted in time.

The detector eliminates as many spurious inputs as possible by checking the number of received 40 kHz pulses. Each receive frame should contain at least five of these pulses. If this is not so, the detector treats them as noise, whereupon a new cycle is started at the arrival of the next pulse from the frame generator. Only when at least five 40 kHz pulses are detected will the output of the detector become active. The lighting of an LED and/or the sounding of a buzzer then indicate that the minimum set distance has been reached and that the driver should stop.

1

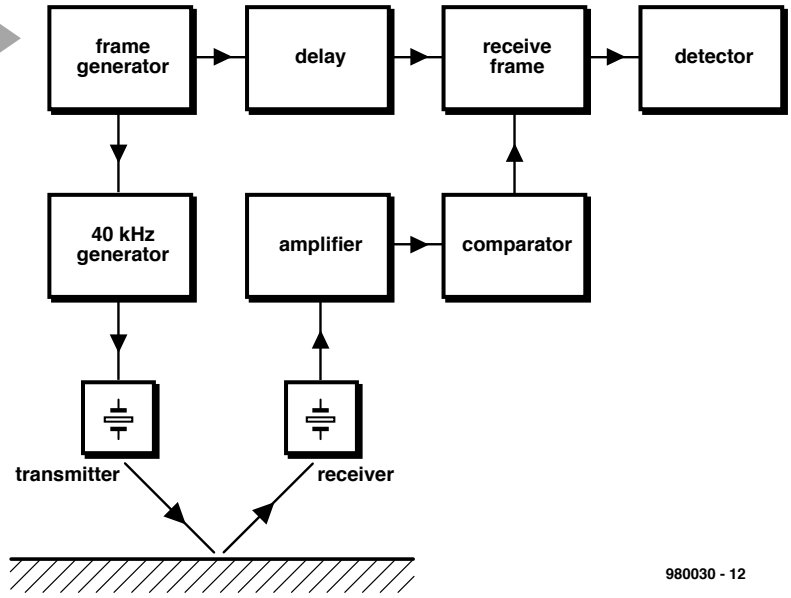


Figure 1. Block diagram of the parking sonar. The distance is computed from the time delay between the transmitted and received pulses.

2

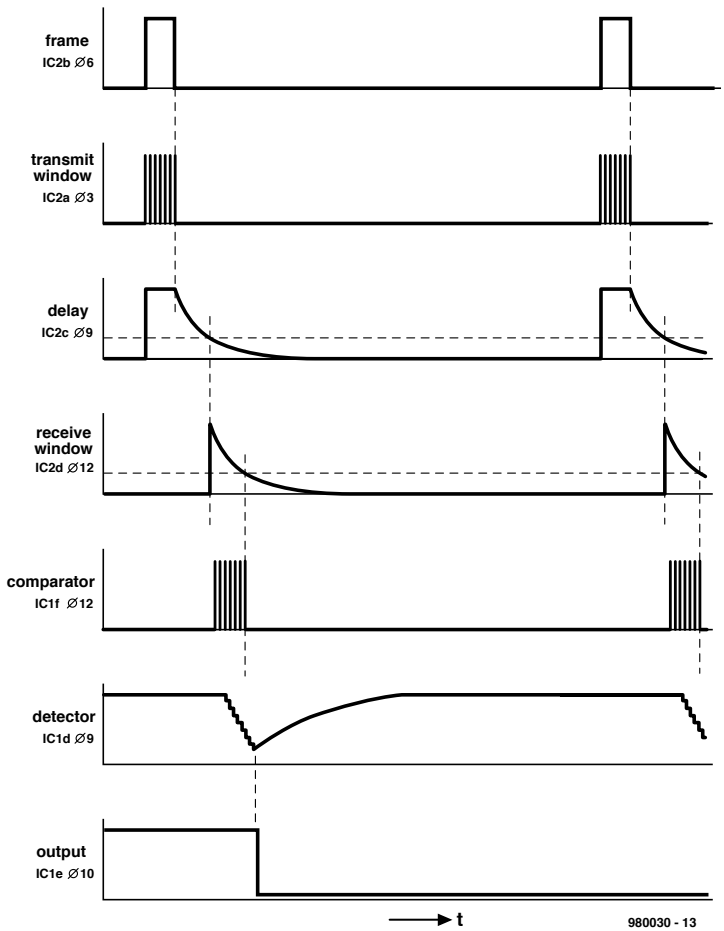


Figure 2. Timing diagram of the parking sonar.

3

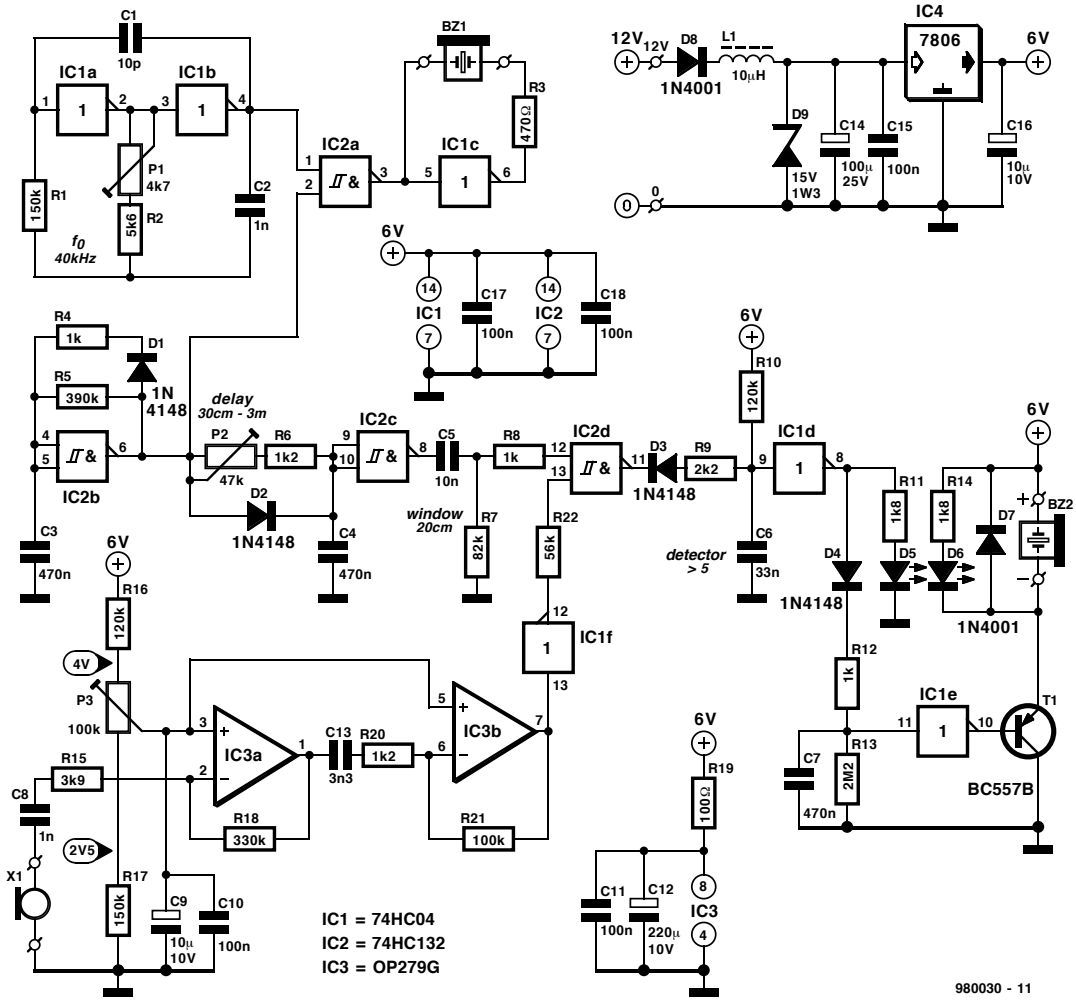


Figure 3. Complete circuit diagram of the parking sonar. The transducers are X_1 and Bz_1, while Bz_2 and D_6 are the indicator elements.

4

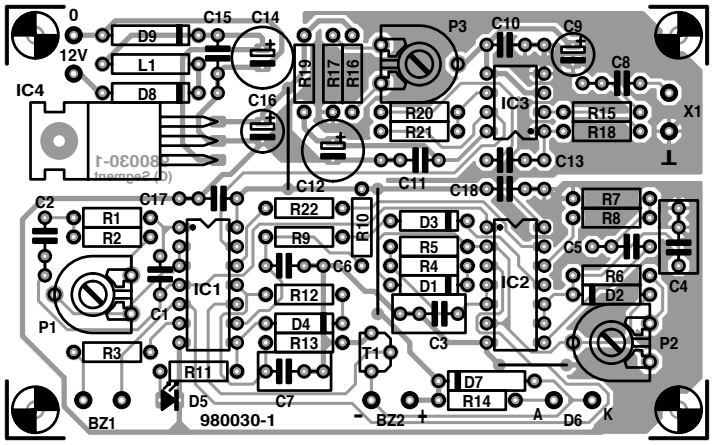
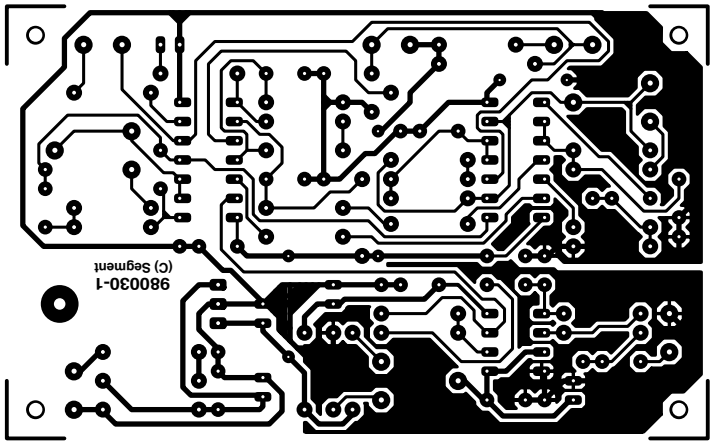


Figure 4. Printed-circuit board for the parking sonar.



Parts list

Resistors:
R_1, R_{17} = 150 kΩ
R_2 = 5.6 kΩ
R_3 = 470 Ω
R_4, R_8, R_{12} = 1 kΩ
R_5 = 390 kΩ
R_6, R_{20} = 1.2 kΩ
R_7 = 82 kΩ
R_9 = 2.2 kΩ
R_{10}, R_{16} = 120 kΩ
R_{11}, R_{14} = 1.8 kΩ
R_{13} = 2.2 MΩ
R_{15} = 3.9 kΩ

CIRCUIT DESCRIPTION

The circuit diagram of the range monitor is shown in **Figure 3**.

The frame generator is based on gate IC_{2b}. It is a simple oscillator that produces pulses at a frequency of about 10 Hz. Network R_4-C_3 determines the width of the pulses and thus of the transmit frame. The pulse interval is determined by network R_5-C_3. The duration of each frame is equal to a period of the frame generator output.

The stability of the 40 kHz oscillator is rather better than that of the frame generator, which is why it is based on two op amps, IC_{1a} and IC_{1b}, and the frequency can be fine-tuned with P_1.

The outputs of the two generators are combined by IC_{2a}, which ensures that the transmit frame is modulated ('filled') with ultrasonic pulses. The resulting signal is applied to the transmit module, Bz_1, via IC_{1c} in a sort of bridge circuit.

The delay line, consisting of IC_{2c}, P_2, R_6 and C_4, is essential for the correct functioning of the monitor. The distance between transmitter and obstacle is set to between 30 cm and 3 metres with P_2.

The output signal of gate IC_{2c} is differentiated by network R_7-C_5, whereupon, in conjunction with the hysteresis of gate IC_{2d}, it determines the width of the receive frame.

Resistor R_8 limits the current through IC_2.

The receiver module is indicated in the circuit diagram by X_1. It is followed by two amplifier cum band-pass filter combinations, based on IC_{3a} and IC_{3b}. These op amps are arranged to give an amplification of ×50 each at 40 kHz.

Variable potential divider R_{16}-P_3-R_{17} enables setting IC_{3a} and IC_{3b} to a reference voltage that ensures that inverter IC_{1f}, which operates as a comparator, obtains the correct bias voltage. In this way, P_3 sets the sensitivity of the circuit. Resistor R_{22} and the input capacitance of IC_{2d}, form a low-pass filter for the comparator output.

To prevent false alarms, the output of detector IC_{1d} can change state only when the receive frame contains at least five 40 kHz pulses. This is effected by applying the signal to network D_3-R_9-R_{10}-C_6 after it has passed through the receive frame. This ensures that the input voltage of IC_{1d} will be sufficiently low to cause its output to change state only after five pulses have been received (penultimate signal in the timing diagram).

When a suitable signal is received that fits in the receive frame, a short positive pulse appears at the output of IC_{1d}. At the same time D_5 lights briefly. The function of this diode is limited,

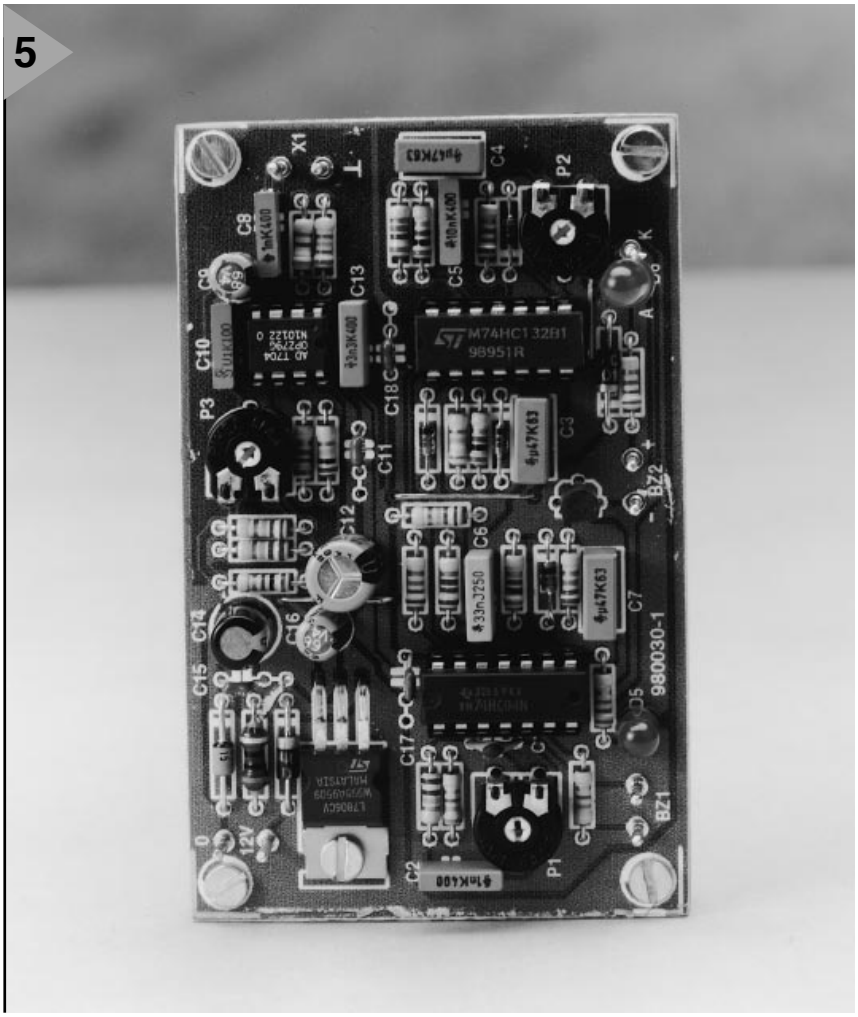


Figure 5. Photograph of the completed prototype. Because of the small current drain, regulator IC_4 does not need a heat sink.

R_{18} = 330 kΩ
R_{19} = 100 Ω
R_{21} = 100 kΩ
R_{22} = 56 kΩ
P_1 = 4.7 kΩ preset potentiometer
P_2 = 47 kΩ preset potentiometer
P_3 = 100 kΩ preset potentiometer

Capacitors:
C_1 = 10 pF
C_2, C_8 = 0.001 µF*
C_3, C_4, C_7 = 0.47 µF*
C_5 = 0.01 µF*
C_6 = 0.033 µF*
C_9, C_{16} = 10 µF, 10 V, radial
C_{10} = 0.1 µF*
C_{11}, C_{15}, C_{17}, C_{18} = 0.1 µF high stability
C_{12} = 220 µF, 10 V, radial
C_{13} = 0.0033 µF*
C_{14} = 100 µF, 25 V, radial

* metallized polyester (MKT)

Semiconductors:
D_1–D_4 = 1N4148
D_5, D_6 = LED, red, low current
D_7, D_8 = 1N4001
D_9 = zener diode, 15 V, 1.3 W
T_1 = BC557B

Integrated circuits:
IC_1 = 74HC04
IC_2 = 74HC132 (SGS Thomson – see text)
IC_3 = OP279G
IC_4 = 7806

Miscellaneous:
L_1 = choke, 10 µH
Bz_1 = 400ET180 (Mercator)
X_1 = 400ER180 (Mercator)
Bz_2 = active buzzer, 5 V, < 100 mA

however, to the calibration. To obtain a clear indication that a proper signal has been intercepted, the output pulse needs to be stretched and this is done by R_{12}-C_7-R_{13}. The stretched pulse is inverted by IC_{1e} (last signal in the timing diagram), whereupon an audible and/or an optical indication (by Bz_2 and D_6 respectively) are actuated.

Note that the receive frame can be widened or narrowed by adapting the value of R_7 as appropriate. For most situations, however, a width of 20 cm, as in the present design, is a good practical value.

The regulator circuit based on IC_4 ensures a stable 6-V power supply. Inductor L_1 and diode D_9 protect the supply lines against interference and overvoltage peaks.

Diode D_8 provides protection against wrong polarity of the 12-V lines. Note that these lines are best taken from the reversing lights.

CONSTRUCTION

The monitor is best built on the printed-circuit board in **Figure 4**, which is, however, not available ready-made. Populating the board should not cause any undue difficulties. Note that it is advisable to use a 74HC132 (IC_2) from SGS-Thomson since other makes may have a different hysteresis.

With the exception of the transducers, the indicator diode and the buzzer, all components are housed on the board.

To minimize any interference, it is essential that the monitor is housed in a properly earthed metal enclosure. The transmit and receive modules should be mounted at some distance from each other, preferably in or near the rear bumper or, in older cars, the rear spoiler. They must, of course, point in a direction immediately behind the vehicle. The transducers must be linked to the monitor (terminals X_1 and Bz_1) via lengths of screened cable (twin-core in case of the transmitter). The screens must be connected to the supply line earth.

It is advisable to keep the lines to the transmit module as far away as possible from the input amplifier to prevent transmit pulses being injected directly into the receiver.

Note that the case of the transmit module is connected internally to one of the terminals; it is, therefore, essential that the module is isolated from the monitor enclosure and/or the car chassis.

The transducers specified in the part list are both watertight.

The indicator diode and/or buzzer should, of course, be placed near the driver, for instance, in or near the instrument panel.

CALIBRATION

When the monitor is switched on, it will be active for about a second, which is the time needed by C_9 to get fully charged. No attempt has been made to eradicate this power-on indication since it tells the driver that the monitor is operating.

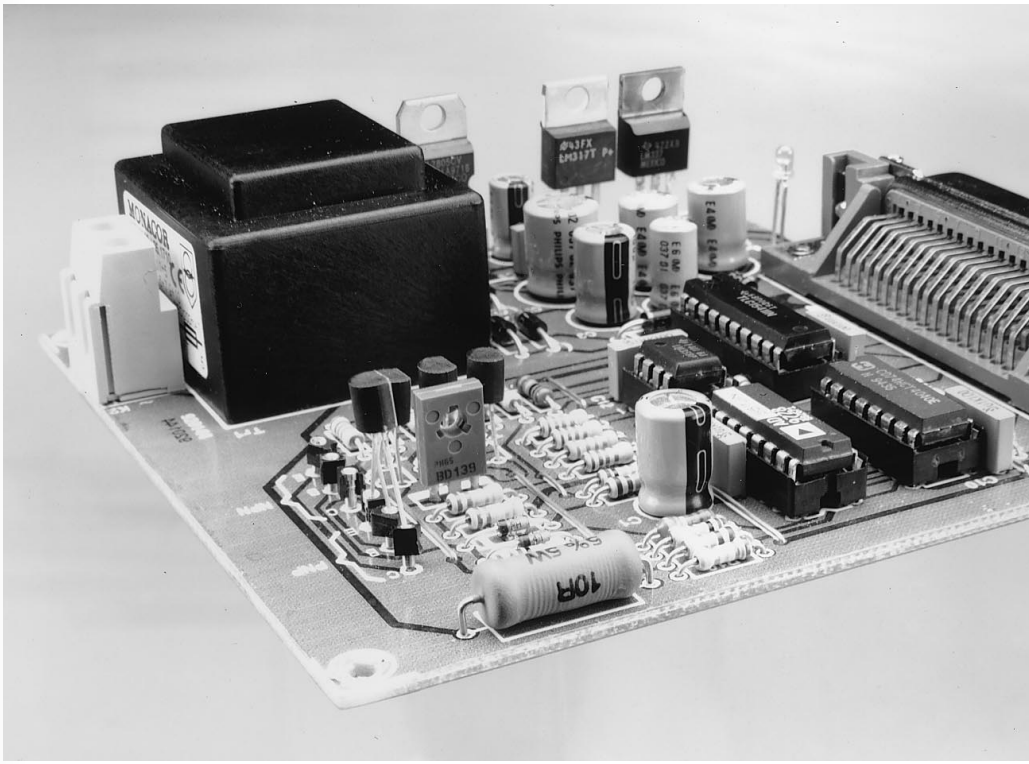
The three preset potentiometers are adjusted with the aid of a good multimeter.

1. Set the multimeter to an appropriate alternating voltage range and connect it across R_3. Short-circuit C_3 with a length of circuit wire. Turn P_1 until the meter reading is a maximum. Seal the preset with some nail varnish and remove the short-circuit from C_3.
2. Short-circuit terminals X_1 and turn P_3 until diode D_5 just goes out.
3. Place an obstacle at the desired distance from the rear bumper and adjust P_2 until diode D_5 begins to flash.

[980030]

PC-aided BJT tester revisited

now with Windows software



The tester presented in this article is an update of the design published in our September 1993 issue. The ZN425 then used for the digital-to-analogue converter (DAC) is replaced by the currently more easily available AD557. Also, the 1993 DOS-version of the software has been replaced by a 32-bit program that runs only under Windows 95 or Windows 3.1 with a Win32S extension.

Features

- *Suitable for n-p-n and p-n-p bipolar junction transistors (BJTs)*
- *To be connected to parallel printer port of a PC*
- *Graphic display of transistor characteristics (on PC monitor)*
- *Integral power supply*
- *Windows software**
- *Test range of U_{CE} = 0–9 V*
- *I_C measured at seven base currents varying from 0 µA to 175 µA*
- *Maximum measurable h_{FE} = 570*

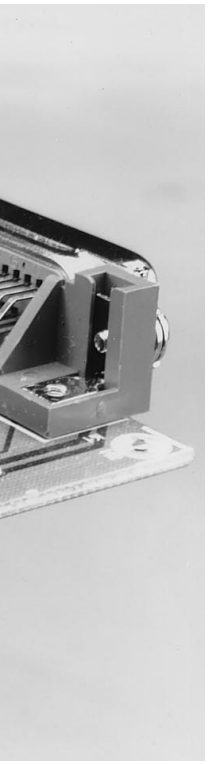
** Suitable for Windows 95 or Windows 3.1 with Win32S extension. The earlier DOS version of the software is also still available.*

Design by S. Aaltonen

Measuring the direct-current gain h_{FE} or β, of a bipolar junction transistor (BJT), p-n-p as well as n-p-n, is, in principle, fairly simple. It is done by passing an accurately known direct current, I_B, through the base-emitter junction and measuring the collector current, I_C. The ratio of the two is the current gain, that is, $I_C/I_B = h_{FE} = \beta$. It is important to note that h_{FE} depends on the collector current, the collector-to-emitter voltage, U_{CE}, and the temperature. This means that a small base current is associated with a smaller h_{FE} than a large base current. This is the reason that a transistor is usually accompanied by a set of gain characteristics. It is clear that to obtain a good idea of the operation of a BJT, a number of base currents should be used in the tests. The circuit described in this article uses seven different base currents, varying from 25 μA to 175 μA. For each of these currents, U_{CE} varies from 0 V to 9 V in 256 steps.

THE DESIGN

The block diagram of the tester is shown in **Figure 1**. The Centronics interface in the diagram is linked to the printer port of the computer. Six data lines of this port are used for controlling the counter and the ADC, while a handshake line (input) is used to read back the serial data from the ADC. Clearly, the data transfer between tester and computer is the same as that between a computer and a printer; moreover, any type of printer port may be used: standard Centronics, Enhanced Parellel Port (EPP) or Extended Capabilities Port (ECP).



The tester is based on an 11-bit counter, IC_1. This chip, which itself is driven by two lines from the printer port, controls a large part of the circuit. During a complete test cycle, it counts from 0 to 2047. The first eight bits (LSBs) are used to drive IC_2, a DAC which generates the collector-emitter voltage, U_{CE}. The remaining three bits (MSBs) set the base current in steps of 25 μA between 0 μA and 175 μA. During the test, the U_{CE} rises from 0 V to 9 V in 256 steps.

To display the transistor characteristics on the monitor screen, I_C and U_{CE} need to be measured, and this is done with the earlier mentioned ADC. Note that only the first quadrant is used since this gives all the necessary information for most applications.

A close look at the block diagram reveals that in case of an n-p-n BJT the emitter current, I_E, is measured, and in an p-n-p transistor, the collector current, I_C. However, this is easily corrected (automatically by the software), since $I_C = I_E - I_B$.

CIRCUIT DESCRIPTION

The circuit in **Figure 3** is largely identical to that of the 1993 tester: the only real change is the substitution of an AD557 for a ZN425 in the IC_2 position.

The U_{CE} for the transistor on test is generated by digital-to-analogue converter IC_2, amplifier IC_{3a} and driver T_1.

The DACs generating the various base currents are discrete designs. The base currents for the n-p-n transistor on test are produced in a simple manner: resistors R_8–R_{11} convert the logic level (5 V) of the three MSBs output by the 11-bit counter directly into a base current. Diodes D_1–D_3 ensure that a low-level output bit cannot draw current from the base current.

In case of a p-n-p transistor on test, matters are slightly more complex, because the emitter is not at ground level, but follows U_{CE}. To make certain that the transistor can switch on at low U_{CE} (about 0 V), it needs to be possible to pull the base to a negative potential. This is why a negative supply line is created with R_{12}–R_{20} and T_2–T_4. The transistors and relevant resistors form current sources that are switched via the three MSBs output by the counter. In a p-n-p transistor, the base current is equal to the sum of the currents produced by the sources.

The resistance across which I_C (in case of an n-p-n transistor, I_E) is measured is R_{23}. To minimize the effect of this component on the test setup, its

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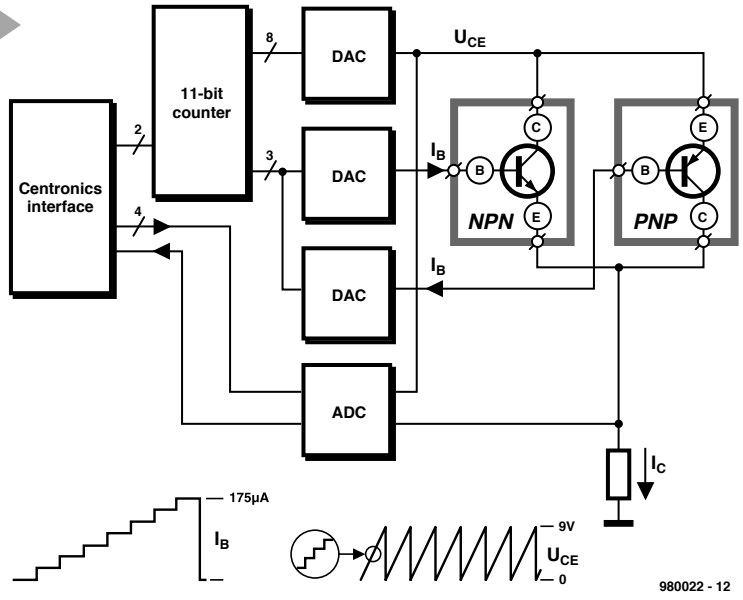
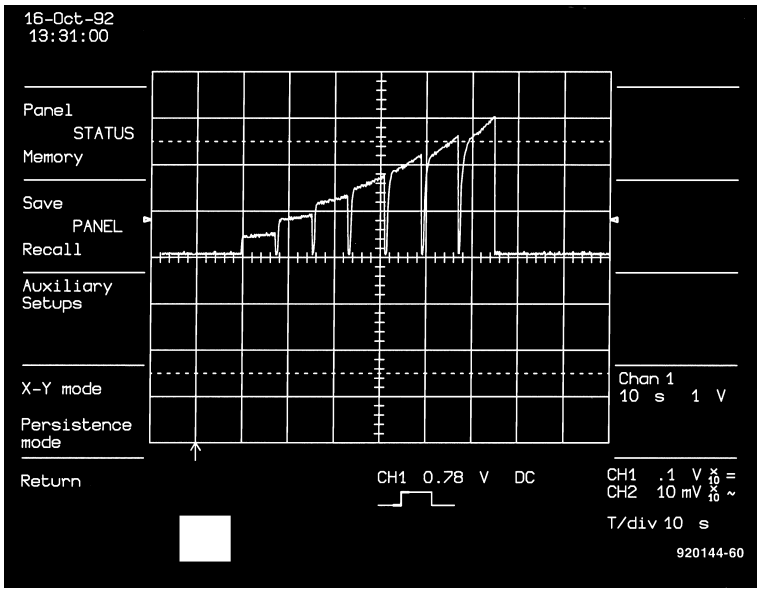


Figure 1. Block diagram of the BJT tester. Apart from the interface and counter, the tester comprises three DACs and one ADC.

Figure 2. This oscillogram shows which signal at input A_0 is applied to the ADC. Each pulse represents a different base current. The slanting side at the top shows the effect of a varying U_{CE}.

2



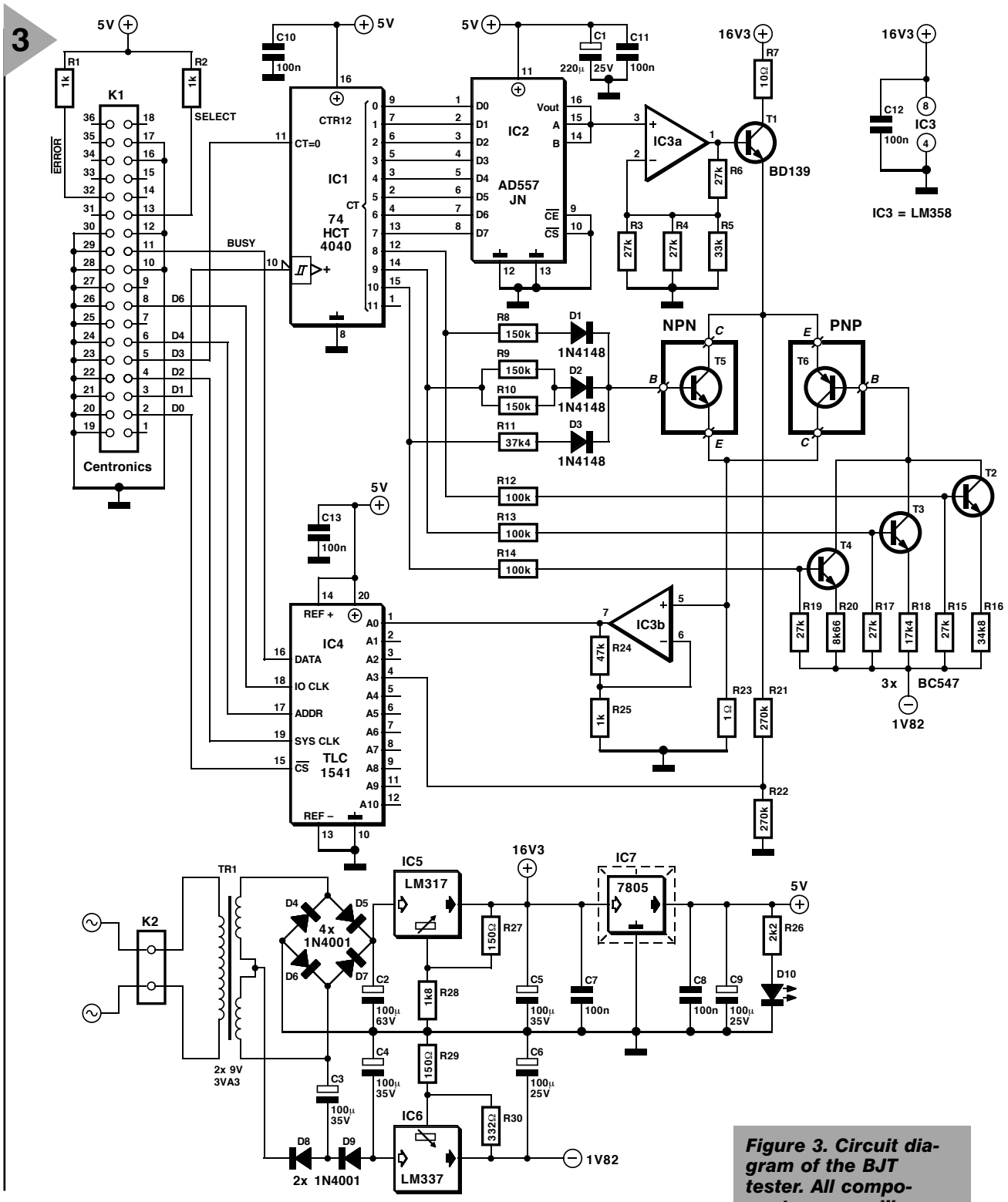


Figure 3. Circuit diagram of the BJT tester. All components are readily available types.

value is low. This has the drawback, however, that the drop across it, that is, the test voltage, is very small. It is therefore raised ×48 by IC_{3b}, before it is applied to digital-to-analogue converter IC_4.

The resulting signal to input A_0 of the ADC is shown in **Figure 2**. This indicates that with seven base currents a voltage proportional to I_C (in of an n-p-n device, I_E) is measured. The reason that the current rises in the course of time, although the base current is stable, is that U_{CE} is increased from 0 V to 9 V in 256 steps during the test period. This shows the effect of U_{CE} on the current gain.

The test value is limited because the measurement range of the ADC is only 5 V. Given a voltage amplification of ×48 and a test resistance of 1 Ω, it is clear that I_C (or I_E) cannot exceed 104.2 mA. Since the base current is 175 µA maximum, the current gain cannot be higher than ×595.

In practice, the measured U_{CE} lies between 0 V and 9 V. This value is brought to the requisite level by attenuator R_{21}-R_{22}. The resulting signal is applied to input A_3 of the ADC.

The power supply is straightforward based on a traditional design. Only the auxiliary negative line is a little out of the ordinary. An alternating current flows through C_3: one half cycle via D_8 and the other half via D_9. Each of the half cycles charges C_4; the resulting potential across this capacitor is held at a level of –1.8 V by IC_{6d}.

Parts list

Resistors:
R_1, R_2, R_{25} = 1 kΩ
R_3, R_4, R_6, R_{15}, R_{17}, R_{19} = 27 kΩ
R_5 = 33 kΩ
R_7 = 10 Ω, 5 W
R_8–R_{10} = 150 kΩ
R_{11} = 37.4 kΩ, 1%
R_{12}–R_{14} = 100 kΩ
R_{16} = 34.8 kΩ, 1%
R_{18} = 17.4 kΩ, 1%
R_{20} = 8.66 kΩ, 1%
R_{21}, R_{22} = 270 kΩ
R_{23} = 1.00 Ω, 1%
R_{24} = 47 kΩ
R_{26} = 2.2 kΩ
R_{27}, R_{29} = 150 Ω
R_{28} = 1.8 kΩ
R_{30} = 332 Ω, 1%

Capacitors:
C_1 = 220 µF, 25 V, radial
C_2 = 100 µF, 63 V, radial
C_3–C_5 = 100 µF, 35 V, radial
C_6, C_9 = 100 µF, 25 V, radial
C_7, C_8, C_{10}–C_{13} = 0.1 µF

Semiconductors:
D_1–D_3 = 1N4148
D_4–D_9 = 1N4001
D_{10} = LED, high efficiency
T_1 = BD139
T_2–T_4 = BC547B
T_5 = n-p-n transistor on test
T_6 = p-n-p transistor on test

Integrated Circuits:
IC_1 = 74HCT4040
IC_2 = AD557JN
IC_3 = LM358
IC_4 = TLC1541IN
IC_5 = LM317 (SOT220)
IC_6 = LM337 (SOT220)
IC_7 = 7805

Miscellaneous:
K_1 = 36-way Centronics socket, right-angled, for board mounting
K_2 = 2-way terminal block for board mounting, pitch 7.5 mm
Mains socket with integral fuse holder and fuse (200 mA slow blow)
2 off 2 mm banana socket, blue (c)
2 off 2 mm banana socket, black (b)
2 off 2 mm banana socket, red (e)
DPDT mains on/off switch
Mains transformer 2×9 V, 3.3 VA, e.g., Monacor/Monarch VTR3209
Enclosure 115×50×135 mm (4.53"×2"×5.32"), e.g., ESM EB11/05)
PCB Order no 980022*
Software Order No. 986005-1* (The DOS version of the software is still available under Order no. 920144)
* These items are available as a single item under Order no. 980022-C

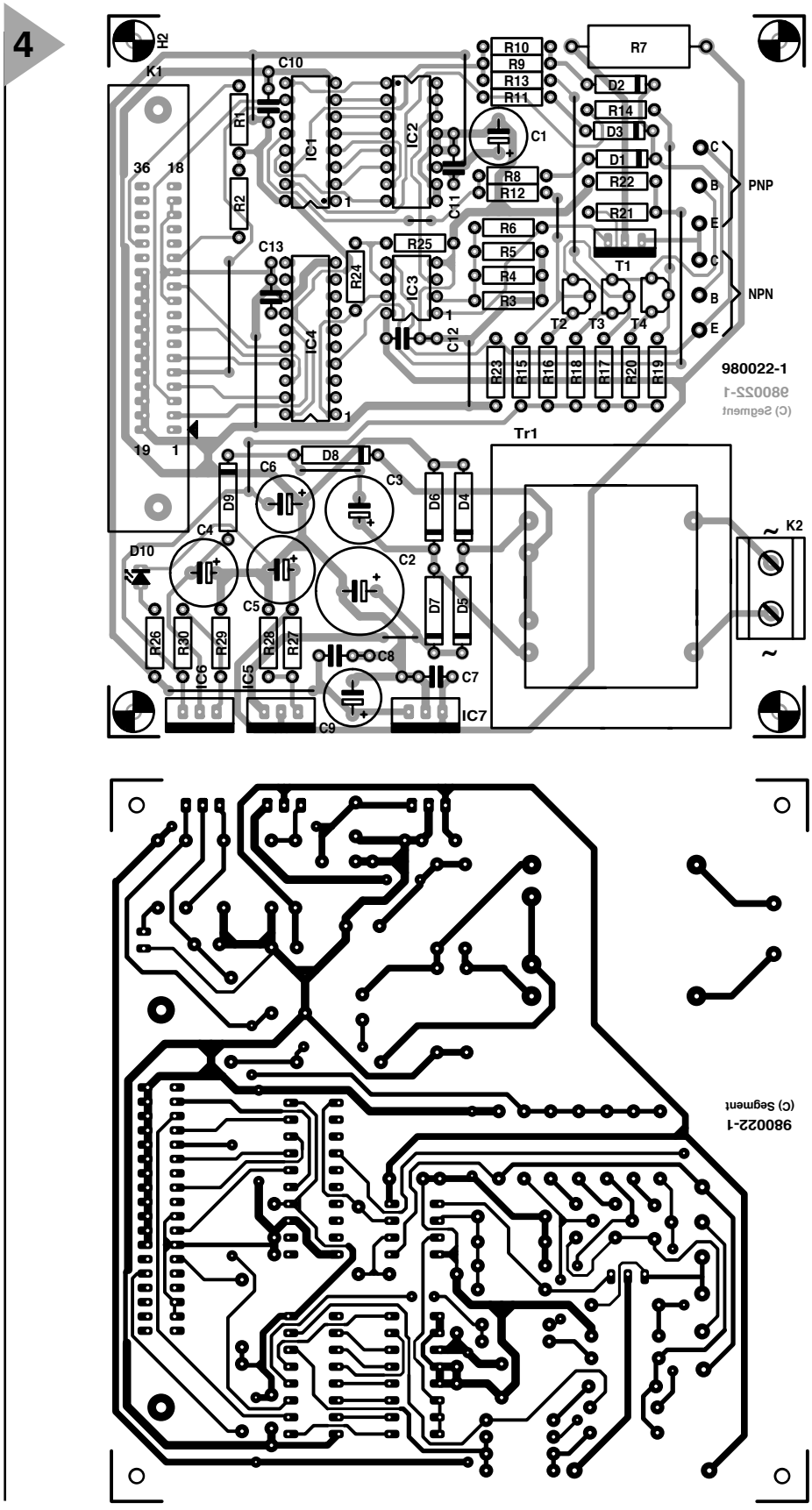


Figure 4. The printed-circuit board is designed to house all components, including the mains transformer, but excepting the on/off switch.

CONSTRUCTION

Building the tester is straightforward, particularly if it is done on the printed-circuit board shown in **Figure 4**. The board is compact and designed to house all components except the on/off switch, but including the mains transformer.

Start by laying the wire bridges and fitting socket K_1. Follow this by fitting first the passive and then the active components. Mind the polarity of the electrolytic capacitors, transistors and integrated circuits.

No special sockets are used for the test terminals, which instead consist of

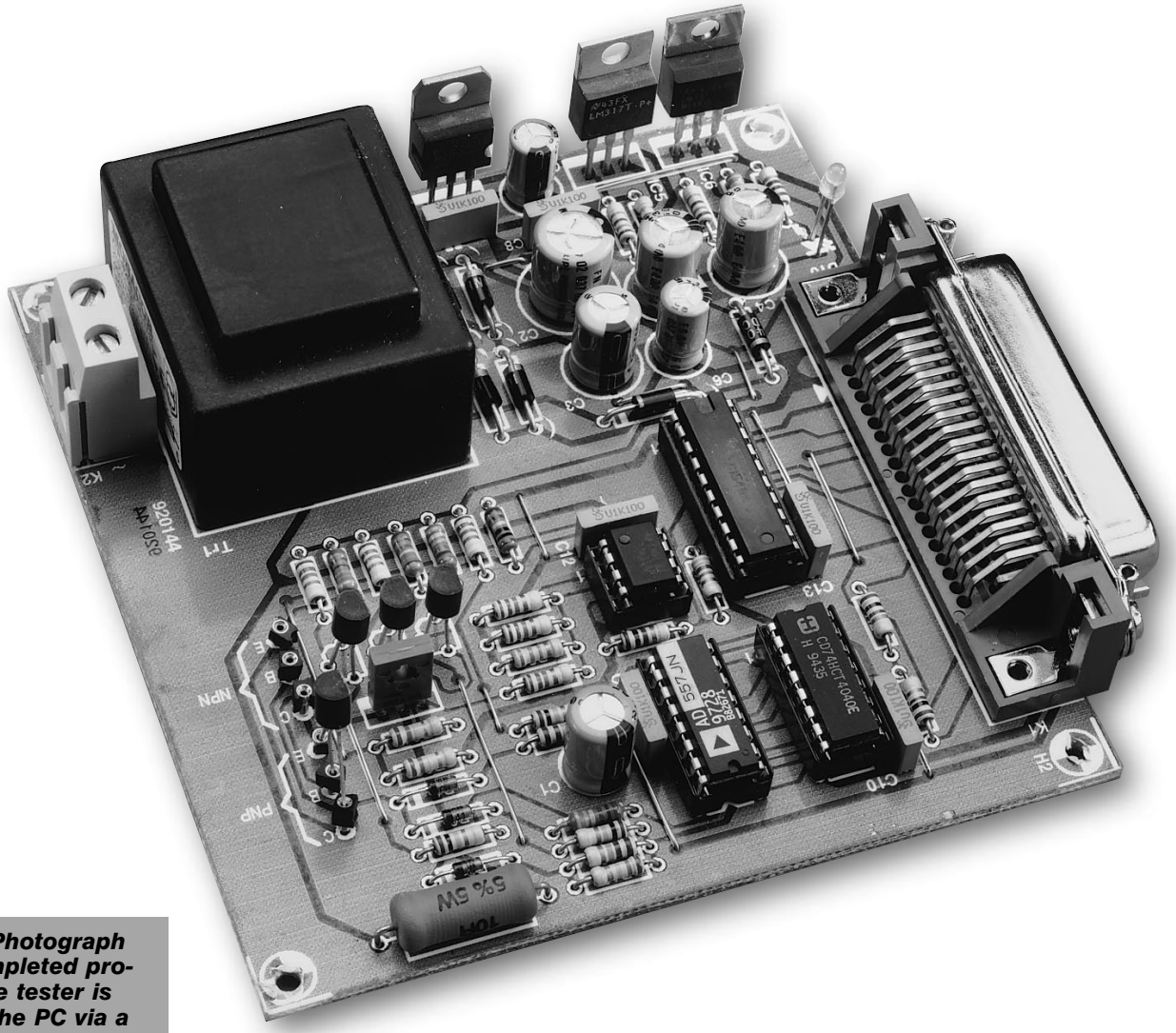


Figure 5. Photograph of the completed prototype. The tester is linked to the PC via a standard printer cable.

coloured banana sockets.

There is no need for the regulators to be mounted on a heat sink.

Since the mains transformer is housed on the board, a space of not less than 5 mm must be allowed when the board is fitted in an enclosure. For security's sake, the underside of the board may be covered with a sheet of PVC or polythene.

THE SOFTWARE

The software has been upgraded to a 32-bit version that runs only under Windows 95 or Windows 3.1 with an Win32S extension. Note, however, that the DOS version of the software is still available (see Readers Services section towards the end of this issue).

After the diskette with the program (npnpnp.exe) has been loaded and the printer port selected, check at which address it is located. Then, in the program, select the correct address location: addresses 378_{HEX}, 278_{HEX}, and $3F8_{HEX}$ can be selected via the menu. A choice then has to be made as to which type of transistor is to be tested, n-p-n or p-n-p, and the scale value of I_{CE}: 80 mA, 100 mA, or 120 mA. Note that the scale value affects only the scale of the characteristic, not the settings of the hardware.

For the **calibration**, state how many settings of base current will be used. This may be as many as eight, that is, no base current or a base current that increases from 25 μA to 175 μA in seven steps. Next, set the number of steps (maximum 256) with which U_{CE} is to be composed from 0 V to 9 V.

The test results may be stored in CSV (Comma Separated Value) format, which enables them to be processed later on in a spreadsheet. In this way, a database with transistor data may be built up.

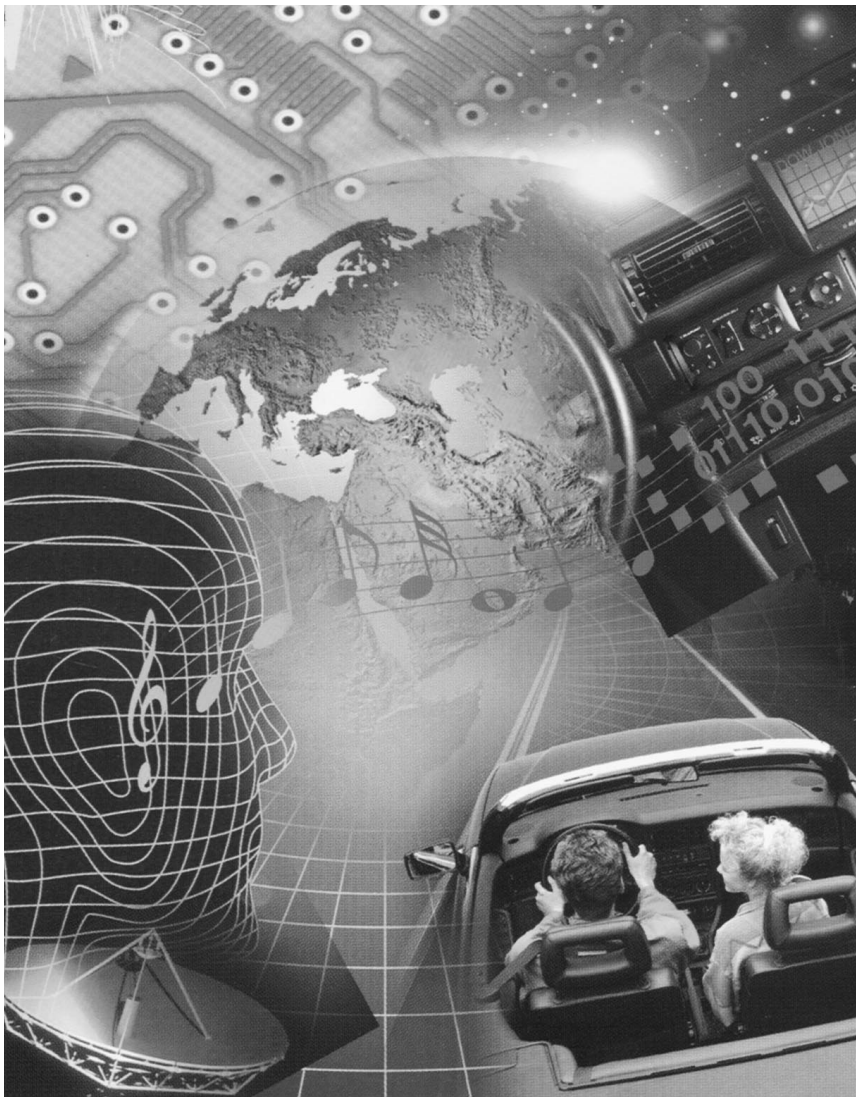
[980022]

ELEKTUUR	
230V~	50Hz
No. 980022	
F = 200 mA T	

Digital Audio Broadcasting (DAB)

Part 2: Data management of the DAB signal

Last month's first instalment of this two-part article dealt with the way the audio data are transmitted. This second and final part looks at the flexible bit rate management used in the production of DAB signals, the likely design of a DAB receiver, and the spread of DAB in the English-speaking world today and tomorrow.



By our Editorial Staff

BIT RATE MANAGEMENT AND DATA SERVICES

The audio programmes and data services carried in a DAB ensemble normally have different requirements as to transmission quality and thus have dissimilar bit rates. A high-quality music programme obviously needs a larger transmission capacity than a simple news channel. But even different data services may have dissimilar requirements. Consequently, individual service (or programme) providers can transmit their services at completely different data rates.

The Eureka 147 standard makes it possible to reconfigure the DAB multiplex dynamically, that is, during an ongoing programme. This is a useful feature in the case of programmes that include a five-minute newscast on each and every hour. In that time, the data rate may be reduced and the capacity so freed used for other services. Such a reconfiguration may look like that

shown in **Figure 3**.

In the DAB system, it is not possible to allocate several frequencies to an individual service provider, since each of these is allocated a relevant data rate in a DAB ensemble. However, data rates in an ensemble may be variable: if, for instance, during a music programme news is broadcast on the hour, the data rate may be briefly reduced from 192 kbit/sec to 96 kbit/sec or even 64 kbit/sec. The capacity so freed can then be used for other services that need only a small capacity, such as the transmission of a software update, or weather information that is transmitted every hour.

Since, technically, the bit rate management is effected in the multiplexer, the additional services may come from different programme providers.

For the transmission of data in addition to, or instead of, audio information, DAB provides in principle three kinds of data service: Programme Associated Data (PAD); radio data services independent of audio information (non-PAD); and complementary services to closed user groups (CA – conditional access).

As already mentioned, PAD is embedded in, and transmitted with, the audio data frame. Normally, the data to be included with the programme are conveyed to the programme providers. This may be data for the volume control of a receiver; or data such as in the Radio Data Service (TP*, TA*, TDC*, PTY*, RT, and so on), but also text and graphics as in teletext information. It is up to the service provider to decide whether the PAD is transmitted at a minimum of 667 bit/sec or a maximum of 64 kbit/sec.

Examples of non-PAD services are electronic newspapers, service information of a local tourist bureau, traffic information direct from the traffic control computer, paging, aircraft flight details, and many more. An interesting one is the transmission of correction data for differential GPS†.

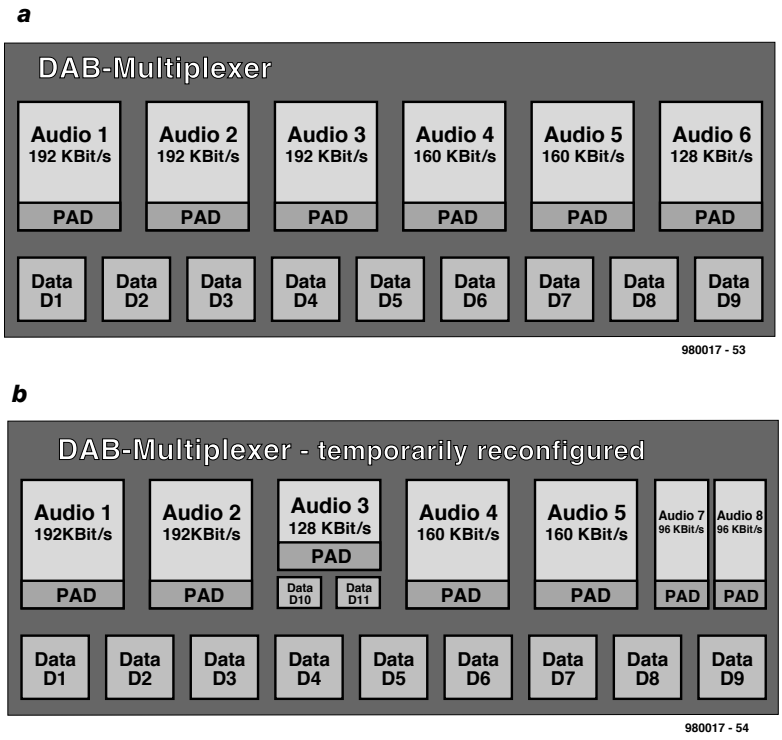
Each and every data service in a DAB ensemble may be used by groups of users or single users with conditional access – relevant encoding and decoding functions are catered for.

The transmission of non-PAD services may be continuous or, in case of small capacity ones, in a submultiplex of a data packet. Three transmission channels are used for this in DAB: a synchronization channel; a Fast Information Channel (FIC); and a Main Service Channel (MSC). Data bits are normally transmitted via the MSC, but sometimes via the FIC. These two channels use dissimilar means to ensure error-free transmission.

The FIC contains all necessary information on the audio and data services and their components (MCI – Multiplex Configuration Information), including position in the multiplex, length, error protection, conditional access, and addressing. If the multiplex contains only few components, only few bits are needed for the description of these components. The capacity

3

Figure 3. The intelligent bit rate management of DAB makes possible a flexible reconfiguration of the individual bits during an ongoing transmission.



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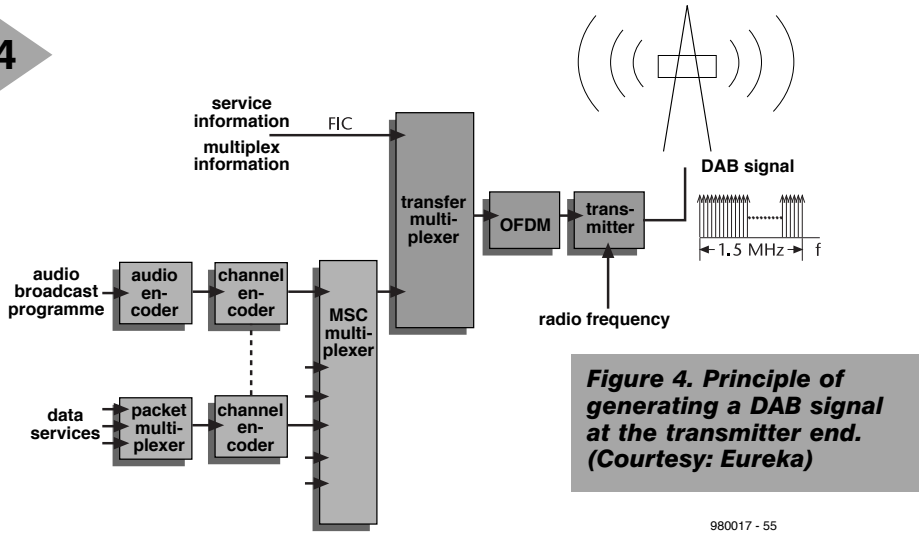

Figure 4. Principle of generating a DAB signal at the transmitter end. (Courtesy: Eureka)

* TA = traffic announcement
TP = traffic programme
PTY = programme type
TDC = transparent data channel
RT = radio text

† GPS = Global Positioning System

**CD-quality audio broadcasts will in themselves be insufficient incentive for the majority of listeners to splash out on a DAB receiver.

Moreover, it is a well-established fact that although most of us spend a lot of money on audio hi-fi equipment, this is usually installed in the living room, while most of our listening is done on a simple (often portable) receiver in the kitchen, bathroom or bedroom.

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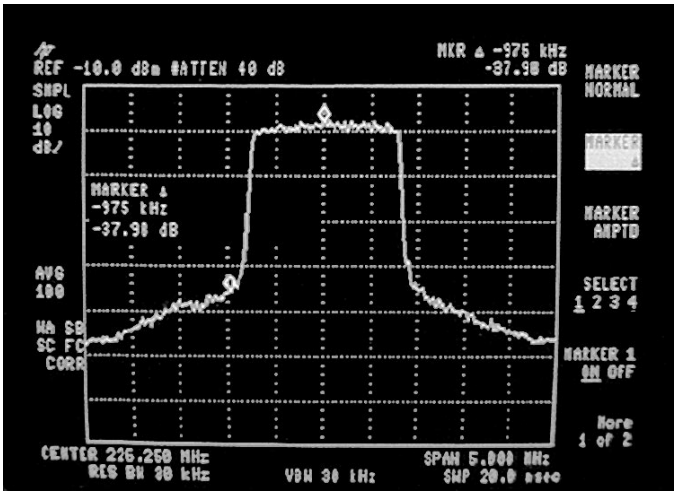


Figure 5. Frequency spectrum of a DAB transmission in Band III. (Courtesy: Eureka)

then released is used for data services; this is termed Fast Information Data Channel. The FIDC may be used for paging or alarm systems.

The MSC is divided into subchannels (SC), whose capacity must be a multiple of 8 kbit/sec. An arbitrary part of the MSC may be used for data services.

In the so-called Stream Mode, a subchannel will cater for only one service at a fixed allocated data rate. In certain circumstances, this leads to an uneconomical use of the capacity, but it has the advantage that the receiver can evaluate the data in a straightforward manner.

In the Packet Mode, the data of several services are divided into packets of fixed length. Each packet has as address the identification of the service to which it belongs. The capacity of each service may be increased if certain service addresses are transmitted more frequently than others.

TODAY ...

Ten years have elapsed from the original concept of Eureka 147 in 1987 to the introduction of the first DAB consumer products (by a number of European as well as Japanese manufacturers) at the International Consumer Electronics Fair in Berlin last year.

Design of suitable chips went hand in hand with the development of the equipment. This design was undertaken by a group of research establishments led by Philips. The chips will be manufactured by Philips, Bosch, Temic and SGS Thomson (at the time of writing: early 1998).

Although Eureka 147 is a combined European development, great interest in it has come from beyond Europe, culminating in the setting up of the WorldDAB Forum early last year. The forum was set up to take DAB from the development laboratory into the industry and thence to the consumer.

It is hoped by manufacturers and retailers alike that DAB will take off in earnest this year. Unfortunately, the signs for this to happen are none too encouraging. There are two problems: one is the dearth of DAB receivers (since no one really knows what the consumer wants** – and is prepared to pay); the second is that, in general, the public has not (yet) been converted to DAB.

Nevertheless, the WorldDAB Forum reckons that this year about 100 million people in Europe will be in reach of DAB services: about 40 million in Germany, 25 million in the UK, and 35 million in Sweden, Belgium, Den-

MUSICAM and MPEG Layer II

The Moving Picture Experts Group (MPEG) has chosen MUSICAM after intensive tests from among 14 competing proposals for normalization by the ISO/IEC (International Standards Organization/International Electrotechnical Commission) as MPEG Audio Layer II.

MPEG Layer II enables the pulse-code modulated (PCM) bit rate required for recording a CD to be reduced by a factor 7, that is, to 192 kbit/sec, without any audible loss of quality.

DAB in the United Kingdom and some Commonwealth countries

*In the **United Kingdom**, the Government set the framework for the development of DAB in the 1996 Broadcasting Act. The BBC began an operational DAB service in September 1995 in the London area and is now building up its transmitter network so that 60% of the British population will be covered by the middle of this year. The regulatory body for commercial radio, the Radio Authority, has announced a "fast burn" approach to licensing private radio multiplexes at both national and local level. A number of private stations are already operating a pilot service.*

***Australia** looks to be moving ahead towards adopting the Eureka 147 system. in 1996, the Government-appointed Digital Radio Advisory Committee expressed support for Eureka 147 as the appropriate delivery system for Australia. Pilot services are operating in three major Australian cities. Tests have also been carried out of satellite-delivered DAB.*

***Canada** has remained at the forefront of Eureka 147 developments after commercial radio and CBC announced their plans for initial DAB services in late 1996. A group of Toronto-based commercial broadcasters have established full-time transmitters on Toronto's CN Tower to carry the programming of 15 radio stations. At the same time, CBC announced some months ago that it would bring DAB to 75% of the population over the next five years.*

***India** is looking to the Eureka 147 system as the future of radio there. The public broadcaster, All India Radio, started preliminary studies and experiments and set up a test transmission system in Delhi. Over the past year or so, work has been orientated towards DAB planning, satellite distribution of a DAB ensemble and its relay in major cities.*

*In **Singapore**, DAB was demonstrated at the Asia Telecom 97 by the Singapore Broadcasting Authority in association with Deutsche Telecom. Further trials, using both L-band and VHF, took place last year.*

*In **South Africa**, a seminar in late 1996 on DAB organized by the South African Broadcasting Corporation and Sentech, the transmission provider, led to the formation of a South African DAB Association. Sentech has set up a test facility in Johannesburg to serve as a pilot and development system.*

mark, the Netherlands, Hungary and Switzerland. Other countries intending to introduce DAB in the very near future are Italy, France, Finland, Switzerland, and Poland.

Outside Europe, Canada is the fastest mover to construct a DAB network. It is hoped that 75 per cent of the population will be in reach of DAB services within five years. Other countries that have made extensive preparations for the introduction of DAB are China, India, Singapore, South Africa, and South Korea.

In Japan, the industry is interested in DAB, but only as far as production for export markets is concerned. The NHK, Japan's national telecoms authority, prefers the VHF In-Band Digital Radio.

In the USA, the National Association of Broadcasters (NAB) opposes the introduction of DAB and has come out in favour of In-Band Digital Radio for operation in the VHF and medium-wave bands. The first licences for satellite-controlled In-Band Digital Radio have already been awarded.

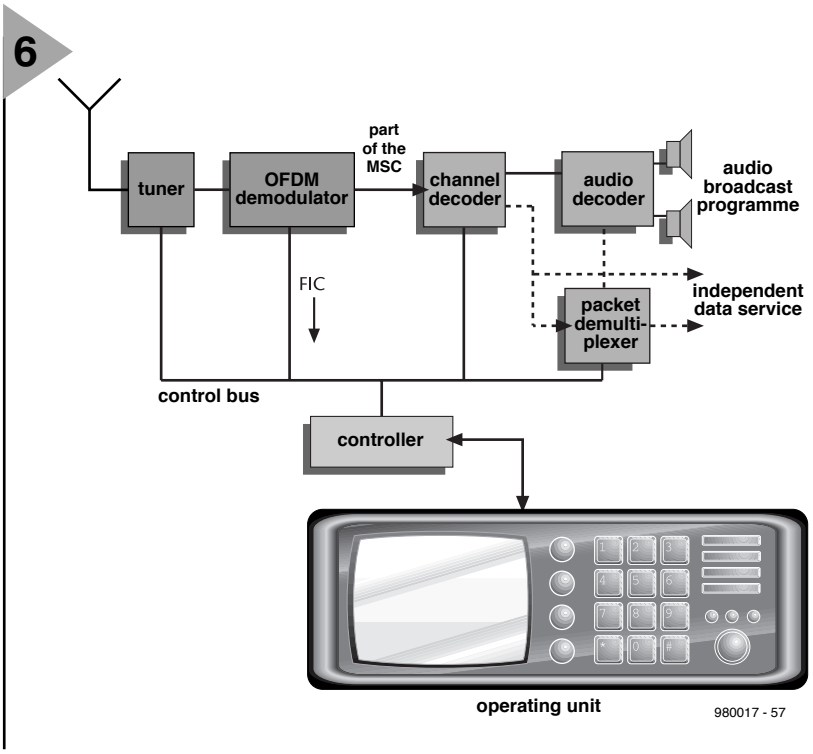


Figure 6. A DAB receiver is likely to consist of a tuner, loudspeaker, graphic screen, processor, and large memory (and a user-friendly interface to operate it). (Courtesy: Eureka)

... AND TOMORROW?

Although the Eureka 147 specification is for terrestrial networks (T-DAB), consideration has been given to the possibility of satellite-supported transmissions (S-DAB) to cater for supranational coverage and also to enable national coverage in large countries such as India and China.

The European Space Agency (ESA) has already proposed a DAB satellite in their Archimedes programme. An unusual feature will be the use of satellites in a highly elliptical orbit (HEO) —see **Figure 8**. The reason for this is that the elevation in northern Europe of geostationary satellites circling above the equator is only about 30°. The likely masking by mountains, tall buildings and forests would seriously degrade the reception of DAB transmissions in mobile units. An HEO ensures that the satellite is more or less at right angles to its target area at its apogee (orbital point farthest away from the earth). This would preclude any masking of the transmission.

The paths of a satellite in an 8-hour orbit (M-HEO) are 120° of longitude away from the equator, so that the satellite can serve, say, Asia, Europe and North America. This requires several satellites in time-spaced identical orbits, since the transmission of a single satellite can be received for only the few hours it is at its apogee. Apart from the satellite's large elevation (>50°), the relatively shorter distance between it and the receiver results in a lower transmitter power being needed.

The first phase of the Archimedes proposal foresees three satellites transmitting at 1.5 GHz. Each of the three transmissions will be a circular spot-beam with a diameter of about 2000 km, so that the three would cover West and Central Europe, South West Europe, and South East Europe, and also provide a pan-European footprint.

[980017]

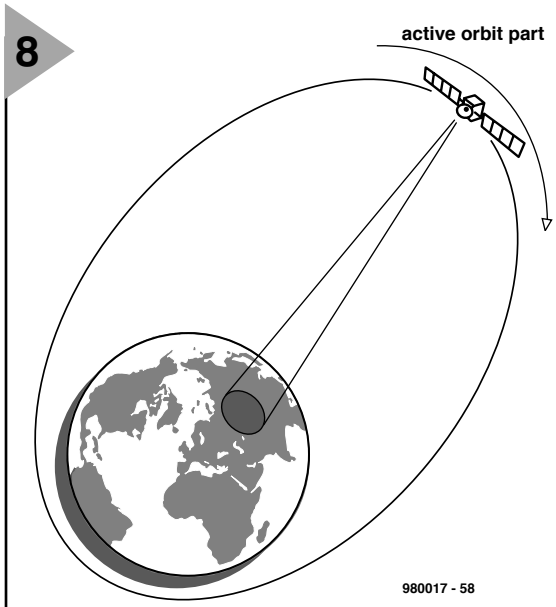
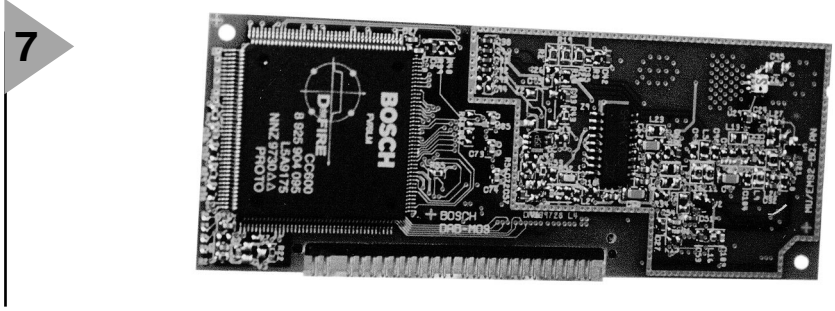


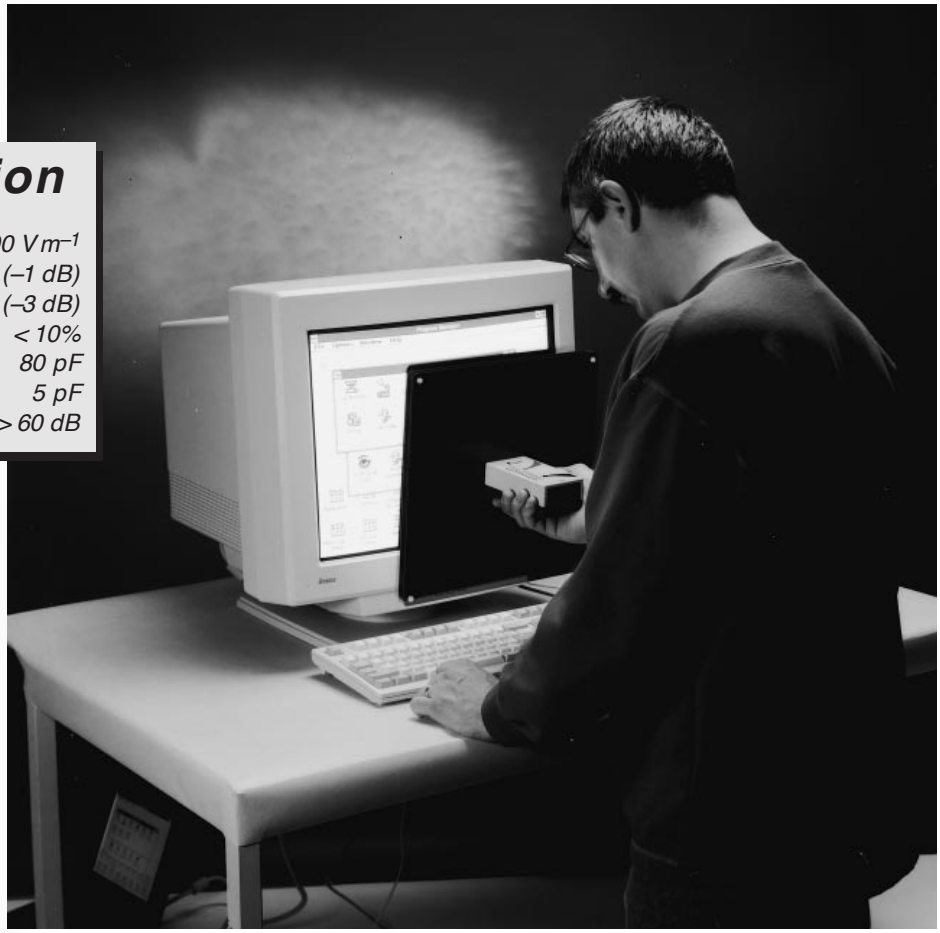
Figure 8. The European Space Agency (ESA) has already proposed a DAB satellite in a Highly Elliptical Orbit (HEO) for coverage of large territories.

Figure 7. Apart from chipsets, manufacturers of DAB products can also buy complete DAB modules.



E-meter

to check the radiation from your VDU



Brief specification

Measurement range	*10–100 V m^{-1}*
Frequency range	*10 Hz – 2 kHz (–1 dB)*
	5 Hz – 5 kHz (–3 dB)
Measurement error	*< 10%*
Sensor capacitance	*80 pF*
Input capacitance	*5 pF*
CMRR	*> 60 dB*

Computer users may have noticed that nowadays there are guidelines as to the limits of radiation a monitor may produce. This is sensible since there are people who believe that high field strengths may adversely affect our well-being. It is a fact, however, that, although we all find ourselves constantly in electric fields, wherever we are in the world, there have as yet been no reliably reported and proven cases of harm to the health of a human being. Nevertheless, most major manufacturers of computer displays make sure that their monitors meet MPRII/MPRIII Recommendations (although these are not mandatory anywhere). Put your mind at rest by ascertaining for yourself that the radiation of your monitor is well below what is believed to be a safe level.

Design by H. Bonekamp

Almost eighteen months ago, this magazine carried an article 'Magnetic-field meter', a small *H*-meter to check the presence or otherwise of alternating magnetic fields. In the present article, an *E*-meter is described to check the presence and strength of alternating electric fields.

Like the *H*-field, the *E*-field is suspected of being harmful to our health, but there are no scientific studies that conclude that levels of these fields well above the MPRII levels (see box) are hazardous.

Sweden has been a leader in developing recommended electromagnetic emission standards for computer displays. In 1987, the Swedish National Board for Measurement and Testing introduced the first, non-mandatory testing procedures for monitors. Called MPRI, they were followed in 1991 by MPRII. These guidelines have generally been adopted by many major manufacturers of computer displays. Yet, even in Sweden, there is no consensus on the limits. The Board stresses that there are no proven biological reasons for limiting the radiation from monitors and that their guidelines are not based on health risks. Rather, the recommended limits are based on what is technically feasible to measure and on what is achievable now or in the foreseeable future.

SAFETY FIRST

So, if a computer display meets the Swedish guidelines, is it safe? No one can say for sure, since there are no conclusive studies that quantify the hazards, if any. But, of course, there is no harm in being cautious. When you are about to buy a monitor, you should know whether it meets MPRII or MPRIII. Buy it from a reputable supplier, or bring your *H*-meter and *E*-meter along and purchase the one with the lowest emission levels (see box).

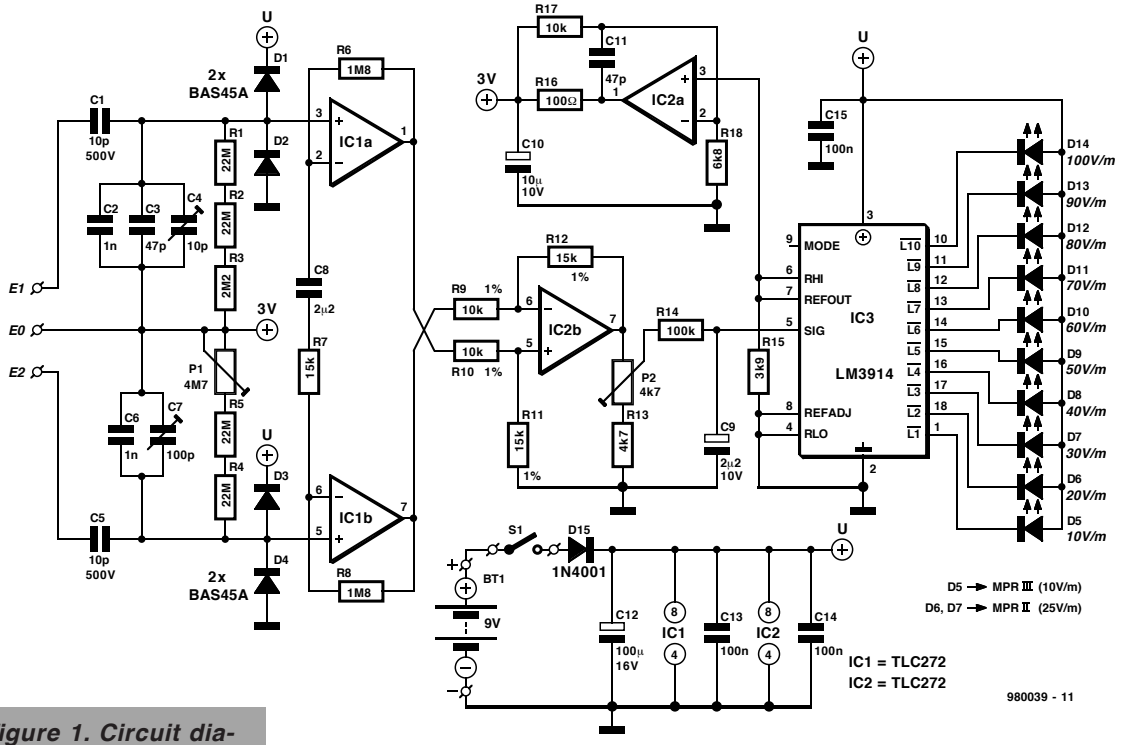


Figure 1. Circuit diagram of the E-meter.

ELECTROMAGNETIC FIELDS

All equipment connected to a source of electricity and switched on generates electromagnetic fields. These fields can be separated into magnetic and electric fields, each of which can be a static or an alternating field. The circuit described in this article monitors alternating *E*-fields. These fields ensue when an apparatus is linked to the mains supply. Every mains outlet, cable, and equipment connected to them generates an *E*-field.

Of course, in a well-designed installation with good earth connections (obligatory in the UK), the field strength remains well within what are considered safe levels.

When a human being is within an *E*-field, his/her body behaves as an antenna, so that tiny voltages are induced in the body. Some people maintain that because of these they become more susceptible to colds and flu, and headaches or stress. It must, however, be stressed again that there is no scientific evidence that even very high field strengths are hazardous. Nevertheless, it is not clear what the effects are on human beings. Some people maintain that there must be some effect since, for instance, a pacemaker with an output of only 1 mV has a biological function, that is, to contract and expand muscles in the heart.

CIRCUIT DESCRIPTION

The circuit of the *E*-meter, shown in **Figure 1**, consists basically of four sections. The sensor is formed by a DIY air capacitor that is linked to the input stage, which is based on a capacitive attenuator. Because of the attenuation, the common-mode voltage may be well outside the limits of the power supply–here, some 300 V_{pp}.

The attenuator is provided with a calibration point to enable a low input capacitance to be combined with a large common-mode suppression. The input capacitance must be low to ensure that the sensor is loaded as lightly as possible. Capacitive coupling with a physically large capacitance is used since this closely resembles a human being in the *E*-field.

The circuit is given a d.c. offset of about 3 V via resistors R_1–R_5 and preset P_1. This offset is used to set up operational amplifiers IC_{1a} and IC_{1b}.

So as to obtain good common-mode suppression and a balanced load from the sensor, a traditional instrumentation amplifier is used.

The d.c. amplification of the input stage is ×1.5 and its a.c. amplification, ×361.5. Because of the low d.c. amplification, it is not necessary to provide compensation to counter the d.c. offset of the op amps.

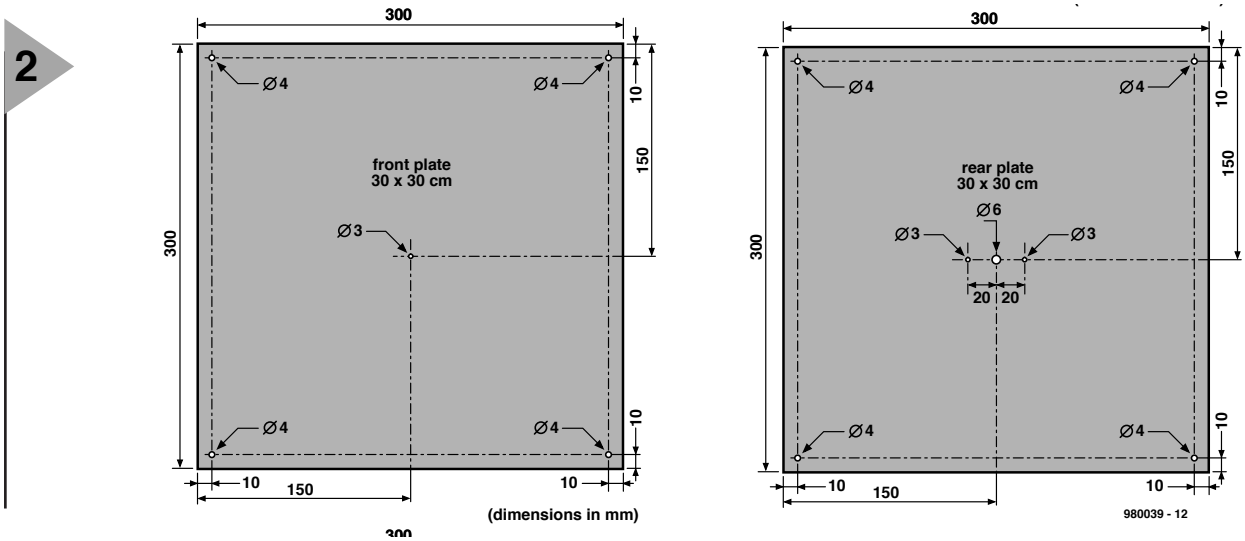


Figure 2. Drilling diagram for the sensor plates. They are separated by five 10 mm nylon spacers to form an 80 pF air capacitor.

Op amp IC_{2b} functions as a half-wave rectifier. This is possible because, although the op amp raises the difference between the signals at its –ve and + ve inputs, the asymmetric power supply allows only positive voltages to be generated. The level of amplification is set with P_2. Network R_{14}-C_9 averages the rectified signal. The direct voltage so obtained is applied to display driver IC_3.

The output of the display driver feeds ten LEDs. The first of these, D_5, lights when the input voltage reaches 125 mV, and the last, D_{14}, when it reaches 1.25 V. This makes possible a meter scale gradated from 10 V m^{-1} to 100 V m^{-1}, which is more than ample for the purposes of the present meter.

Note that for emissions complying with the MPRII and MPRIII recommendations (which is the case with most modern VDUs) only the three lowest LEDs are required.

After it has been buffered and amplified, the reference potential of the display driver is also used as the common-mode voltage for the instrumentation amplifier.

Power for the meter is derived from a single 9-V (dry or rechargeable) battery. Diode D_{15} protects the circuit against wrong polarity.

CONSTRUCTION

The most demanding part of the circuit is the sensor, a DIY air capacitor. This is produced from two 30×30 cm sheets of aluminium cut and drilled as shown in **Figure 2**. The sheets are fastened together with four nylon screws, nuts and 10 mm long spacers: one at each corner. Nylon screws, nuts and spacers are used since these do not affect the capacitance, which is about 80 pF.

Populating the printed-circuit board (see **Figure 3**) should not present undue difficulties. Start by placing the wire bridges, followed by all passive components.

Use good-quality sockets for the ICs, since static charges can easily damage the inputs of the operational amplifiers. Such damage is normally not immediately noticeable, but it does debase the performance.

The board is fitted in the enclosure on 15 mm spacers to ensure that the LEDs protrude slightly through the lid of the enclosure. The battery is best fitted with some suitable tape or bluetack to the bottom panel of the enclosure

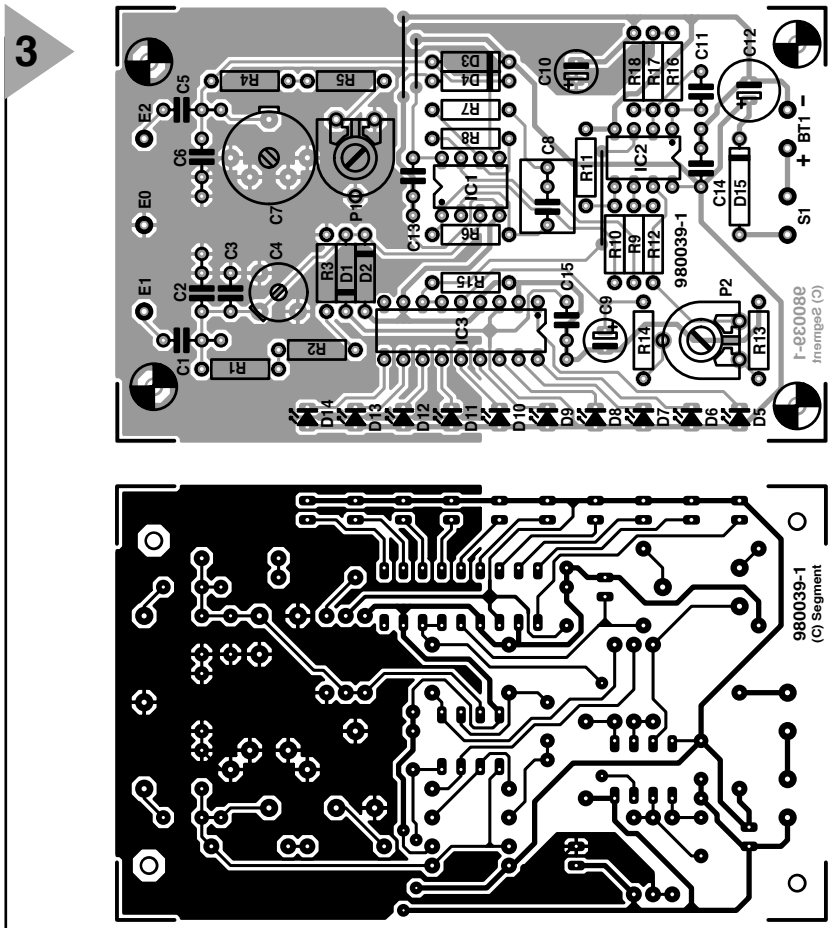


Figure 3. Component layout of the single-sided printed-circuit board for the E-meter.

underneath the board (under IC_2).

The sensor is fitted to the front panel of the enclosure with two 10 mm long and one 20 mm long M3 size nylon screws and nuts. Place a solder tag under one of the nuts at the back plate. For this purpose the back plate of the sensor has 3 mm holes at either side of the 6 mm centre hole. These three holes should also be drilled in the front panel of the enclosure at the appropriate positions. The 20 mm long screw should pass through a 10 mm nylon spacer and the front plate of the sensor where it is fastened with a nylon nut, under which a solder tag is placed. The nylon fasteners ensure electrical isolation of the two plates.

The front plate is linked to input E_1 via a short length of insulated circuit wire from the solder tag under the central fixing nut. The rear plate is linked to input E_2 via a short length of insulated circuit wire from the solder tag under one of the fixing nuts. The photograph of the completed prototype in **Figure 4** shows how it is all done.

Finally, fit the on/off switch on the front panel of the enclosure.

CALIBRATION

Ideally, a function generator and a digital multimeter are required for setting up the instrument. If a function generator is not to hand, a bell transformer may be used—see later.

To ensure good common-mode suppression, the attenuators must be well balanced. Below frequencies of about 100 Hz the resistors are dominant, at higher frequencies, the capacitors.

Connect the multimeter, set to a relevant direct voltage range, across C_9. Short-circuit E_1 to E_2 and connect the function generator between E_1 and E_0 (earth).

MPRII/MPRIII Recommendations

Magnetic fields	*ELF (5 Hz – 2 kHz)*	*< 250 nT**
	VLF (2 kHz – 400 kHz)	*< 25 nT**
Electric fields	*ELF (5 Hz – 2 kHz)*	*< 25 V m^{-1}*
	VLF (2 kHz – 400 kHz)	*< 2.5 V m^{-1}*

**nT = nano Tesla (1 Tesla = 1 Weber m^{-2})*

For the MPRII recommendations, these limits are measured at 48 different positions around the monitor at a distance of 50 cm. For the MPRIII recommendations, the measurements are taken at a distance of 30 cm from the monitor, also at 48 positions.

Parts list

Resistors:
R_1, R_2, R_4, R_5 = 22 MΩ
R_3 = 2.2 MΩ
R_6, R_8 = 1.8 MΩ
R_7 = 15 kΩ
R_9, R_{10} = 10 kΩ, 1%
R_{11}, R_{12} = 15 kΩ, 1%
R_{13} = 4.7 kΩ
R_{14} = 100 kΩ
R_{15} = 3.9 kΩ
R_{16} = 100 Ω
R_{17} = 10 kΩ
R_{18} = 6.8 kΩ
P_1 = 4.7 MΩ preset potentiometer
P_2 = 4.7 kΩ preset potentiometer

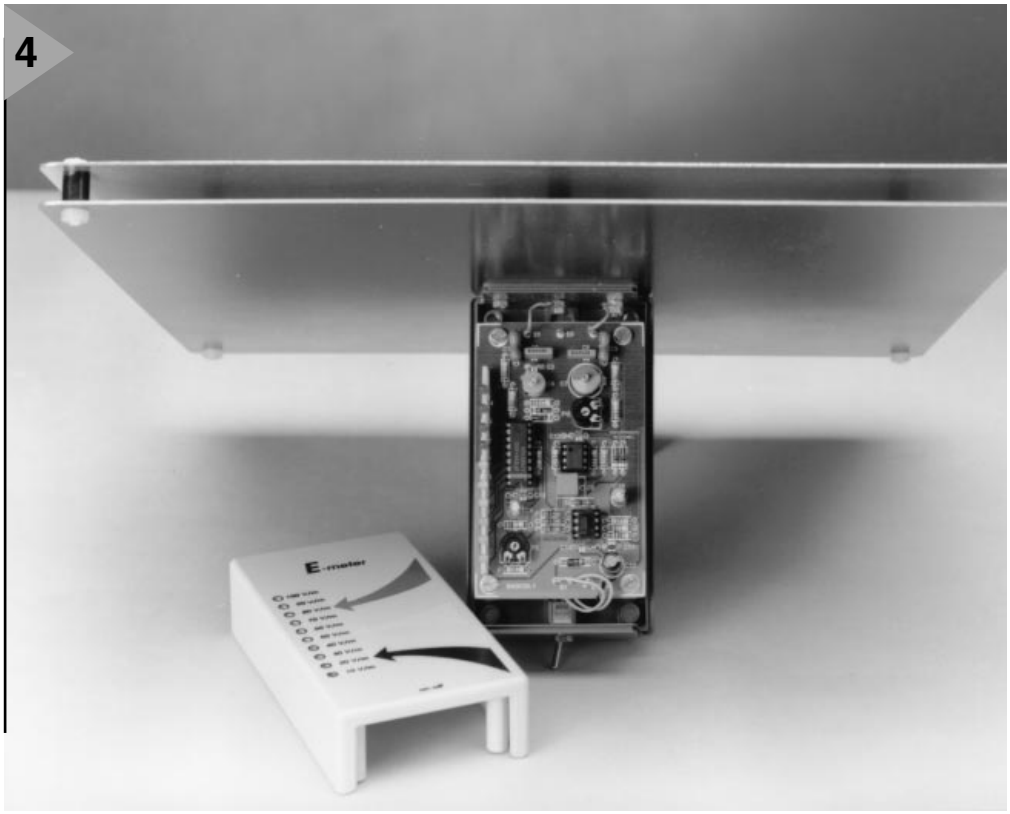
Capacitors:
C_1, C_5 = 10 pF, 500 V, 5%
C_2, C_6 = 0.001 µF, metallized polyester (MKT), 5%
C_3, C_{11} = 47 pF
C_4 = 10 pF trimmer
C_7 = 100 pF trimmer
C_8 = 2.2 µF, metallized polyester (MKT)
C_9 = 2.2 µF, 10 V, radial
C_{10} = 10 µF, 16 V, radial
C_{12} = 100 µF, 16 V, radial
C_{13}–C_{15} = 0.1 µF. high stability

Semiconductors:
D_1–D_4 = BAS45A (Philips)
D_5–D_7 = LED, green, high efficiency
D_8–D_{10} = LED, orange, high efficiency
D_{11}–D_{14} = LED, red, high efficiency
D_{15} = 1N4001

Integrated circuits:
IC_1, IC_2 = TLC272CP
IC_3 = LM3914N

Miscellaneous:
BT_1 = 9-V battery with terminal clips
S_1 = single-pole on/off switch
Enclosure = Bopla E430 (from Phoenix Mecano Ltd, phone 01296 398 855) or similar
Aluminium sheet, 1 mm thick, 2 off 300×300 mm
4 off M4 nylon screw, 15 mm long
4 off M4 nylon nut
1 off M3 metal screw, 15 mm long
2 off M3 metal screw, 10 mm long
4 off M3 metal screw, 20 mm long (for board mounting)
4 off spacers, 15 mm long (for board mounting)
5 off M3 nut, nylon or metal
5 off nylon spacer, 10 mm long (for sensor)
2 off solder tag, 3 mm
Insulated circuit wire as required.
PCB Order no. 980039 (see Readers' services towards the end of this issue)

Figure 4. Photograph of the completed prototype.



Apply a sinusoidal signal at a frequency of 1 kHz and maximum output. Turn first C_7 (coarse) and then C_4 (fine) for minimum reading on the multimeter.

Lower the frequency to 10 Hz and adjust P_1 for minimum reading on the multimeter.

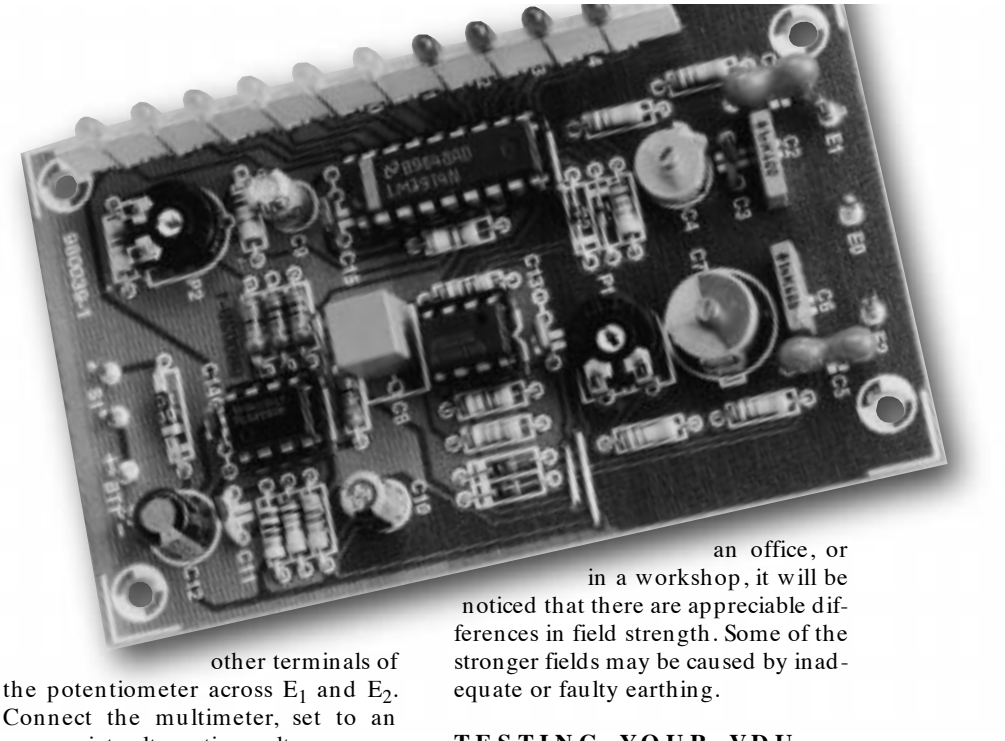
Remove the short-circuit from E_1 and E_2 and connect the function generator between these terminals. Connect the multimeter, set to an appropriate alternating voltage range, in parallel with the function generator output, making sure that the leads of the multimeter are not in the vicinity of the attenuators (so as to avoid crosstalk). Set the output of the function generator to 1 V rms and adjust P_2 until D_{14} just begins to light.

If a function generator is not available, use a 12 V bell transformer. Short-circuit E_1 to E_2 and connect the secondary of the transformer between these terminals and earth (E_0). Connect the multimeter, set to an appropriate direct voltage range, across C_9.

Turn first C_7 (coarse), then C_4 (fine) and finally P_1 for minimum reading on the multimeter.

Remove the short-circuit from E_1 and E_2. Connect the secondary of the transformer across a 1 kΩ potentiometer. Link the wiper and one of the other terminals of the potentiometer across E_1 and E_2. Connect the multimeter, set to an appropriate alternating voltage range, across E_1 and E_2. Adjust the potentiometer until the meter reads 1 V rms. Turn P_2 until D_{14} just begins to light.

If it appears that the range of C_7 is not large enough (which may happen when the tolerance of C_1, C_2, C_5 or C_6 is too large), alter the value of C_3 by trial and error.



During measurements of the *E*-field at home, at school or college, in an office, or in a workshop, it will be noticed that there are appreciable differences in field strength. Some of the stronger fields may be caused by inadequate or faulty earthing.

TESTING YOUR VDU

The alternating electric field of a VDU is a maximum when the background is a bright white. This can be set easily on most modern monitors.

If the VDU meets the recommendations of MPRII, D_7 will light at distances between the meter and VDU of up to 50 cm. The recommendations of MPRIII specify this distance as 30 cm; only D_5 should then light. [980038]

IC tester

Part 2: menu structure and test-vector building

Last month we gave you the low-down on the hardware aspects of this powerful and versatile IC tester. In this second and concluding instalment, we turn to programming matters.

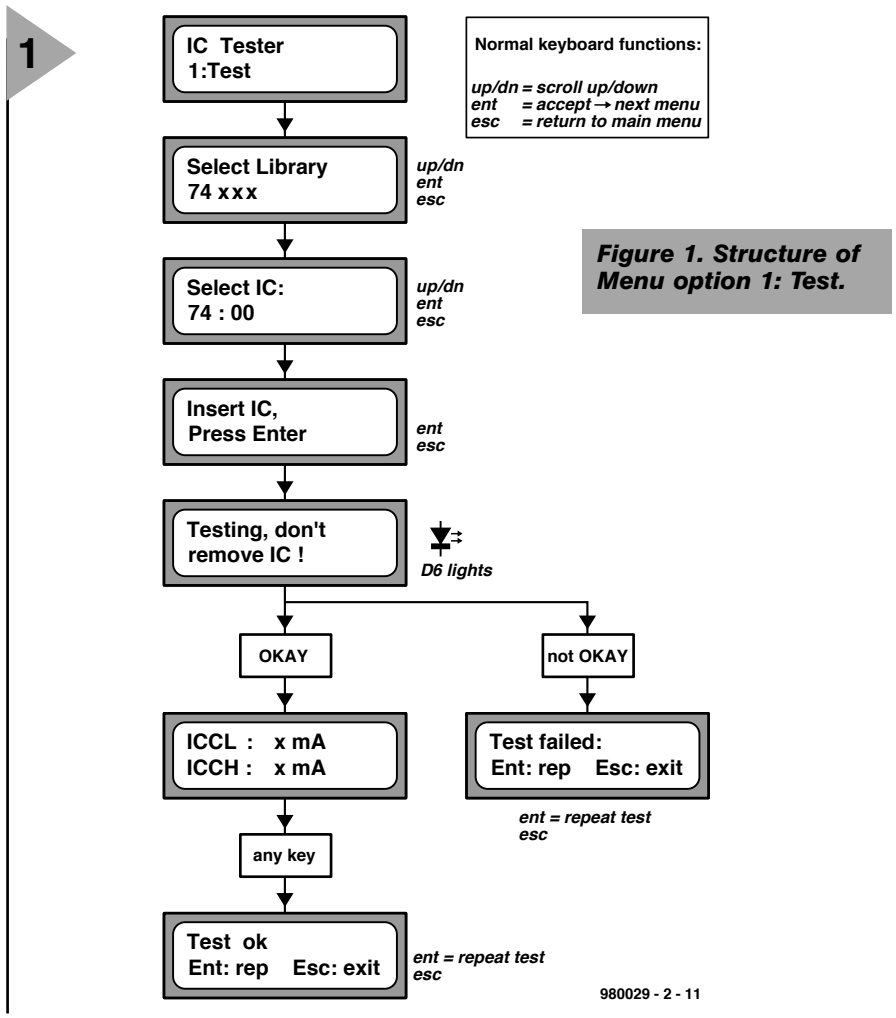


Figure 1. Structure of Menu option 1: Test.

To be able to apply the information presented in this instalment, you have to have a working IC tester available, together with all the files found on the diskette with order number 986014-1 or CD-ROM 986001-1 (see further on). The tester is very likely to function properly if the message

IC Tester
1:Test

appears on the LCD when you switch the power on. However, this project features a number of clever hardware checking options. Although you may not need to do any hardware checking at all, the relevant routines are briefly mentioned further on. For now, it is assumed that the tester works properly.

MENU STRUCTURE

As already mentioned in last month's instalment, you are looking at a test instrument which offers three communication channels with the real world: a keyboard, an LCD and a serial computer interface. Throughout the operation of the IC tester, menus are used to interact with you, the user. Selecting from the plethora of functions offered by the instrument is basically very simple and easy to learn once you know the functions of the (few) keys on the keyboard. Fortunately, the use of these keys is consistent in most menus. To help you stay oriented, the structure of each of the major sub-menus offered by the tester is shown in **Figures 1 through 8**. Where a key has a non-standard function, this is indicated separately.

Many of you will be perfectly happy to use the '1:Test' menu most of the time, or the '3:Retest' menu if you are looking at a pile of identical ICs which should be subjected to a go/non-go test.

TEST VECTOR FILE

From here on, we are addressing the more advanced users among you who require a deeper knowledge of the way the instrument uses built-in software to test logic integrated circuits. For a good understanding of the hardware/software interaction, it is necessary to analyse the structure of the file Test Vector File which is permanently stored in the system EPROM, together with the program executed by the microcontroller.

A copy of the test vector file which is compiled, converted to binary and then stored in the 'default' system EPROM (order code 986507-1) may be found on the project diskette, order code 986014-1, as well as on the '*µP-µC Hard & Software 97-98*' CD-ROM, order

Design by L. Lamesch

code 986001-1 (look in the subdirectory /INT/BIN). The file is called VECT.TVC, and contains all information the system needs to check the massive amount of ICs listed in Table 1 in last month's instalment. For now, let's load 'VECT.TVC' into a word processor, and examine the syntax used. What do all these keywords mean?

;
Comment delimiter. All characters following the semicolon are treated as comment, and ignored by the system.

LIBRARY **lib_name**
Defines the start of an IC library. This should be the first keyword in the .TVC file (except comment, of course). All IC types which follow this keyword belong to the library with the name 'lib_name'. The name of the library may consist of up to 15 characters. There is no limit to the number of libraries in a .TVC file.

NAME **ic_name**
Defines the start of IC data, and launches the test vector set for the IC with the name 'ic_name' (max. length is 15 characters). There is no limit to the number of ICs in a library. The end of the test vector set is marked by the next occurrence of 'NAME', 'LIBRARY', or the end of the .TVC file.

CHILD **parent_ic_name**
If an IC employs the same test vectors as one already defined, it is sufficient to identify it as a 'child' of a 'parent'. For example, the 74:132 has the same function and pinout as the 74:00, except that the gates are of the Schmitt trigger type (which is not recognised by the tester). A 74:132 is defined as follows:

```
NAME     74:132   ;define new IC
CHILD    74:00    ;declare as 74:00
                   offspring
```

A parent may have up to 100 children.

PINS **pin_count**
Unless a certain IC is a 'child', its test vectors have to be defined. In that case, the first keyword to use is always 'PINS' which defines the number of pins on the IC.

PINORDER **pin_order**
Links the individual IC pins to the columns that supply the test vectors. 'PINORDER' may only follow 'PINS', and the pins are identified using their pin numbers. Individual pin numbers should be separated by a space character. All IC pins have to be identified in 'pin_order', including pins which are not tested.

PINDEF pin_definition

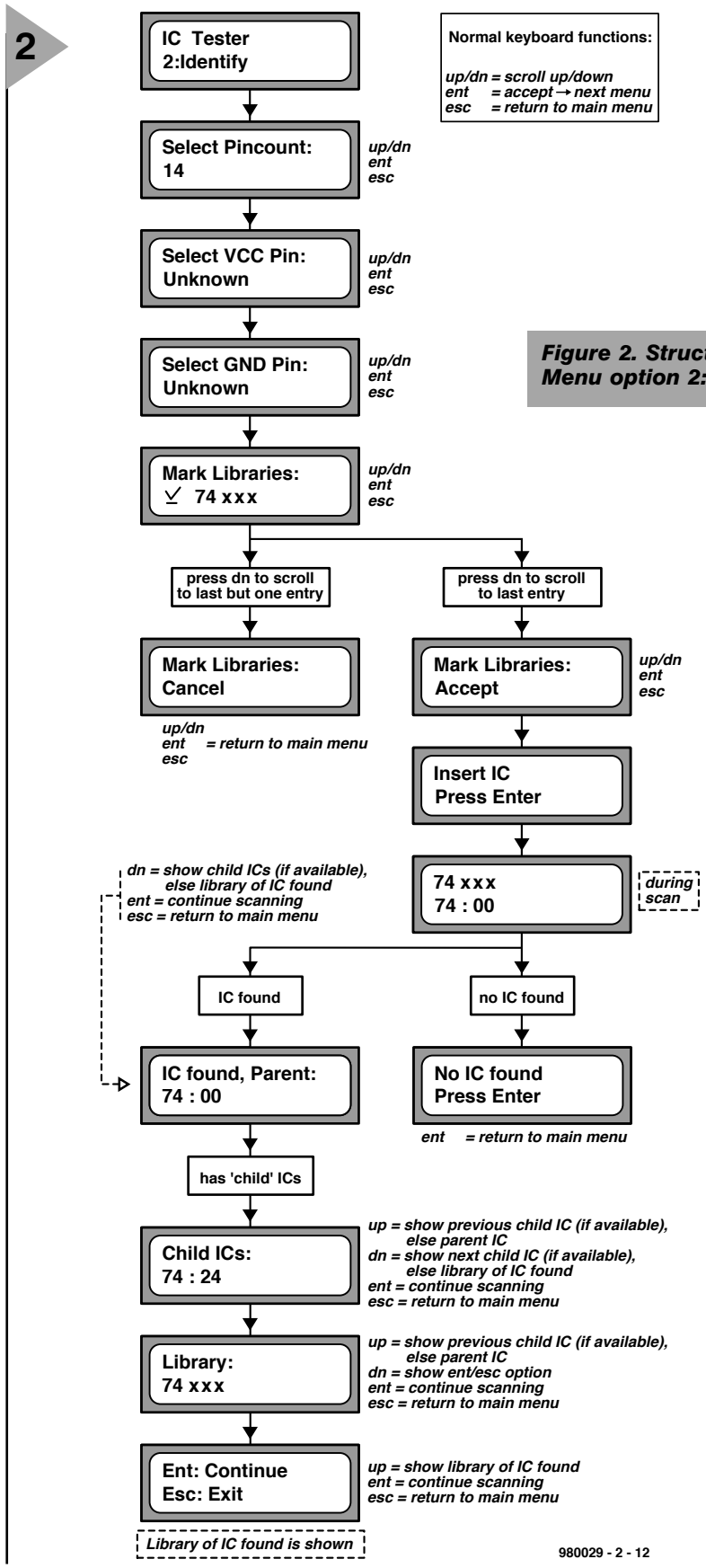


Figure 2. Structure of Menu option 2: Identify.

This defines the function of each individual pin. The following functions are available:
O output
I input
G ground pin
V Vcc (+supply) pin
The individual pin functions may be separated by spaces (not obligatory, though), and all pins must be included in 'pin_definition'. Pins which should not be tested are defined as outputs ('O'), and not tested in the 'VECT' line ('X'). 'PINDEF' should precede the first 'VECT'. After a 'VECT' line, the pin functions may be redefined using 'PINDEF'.

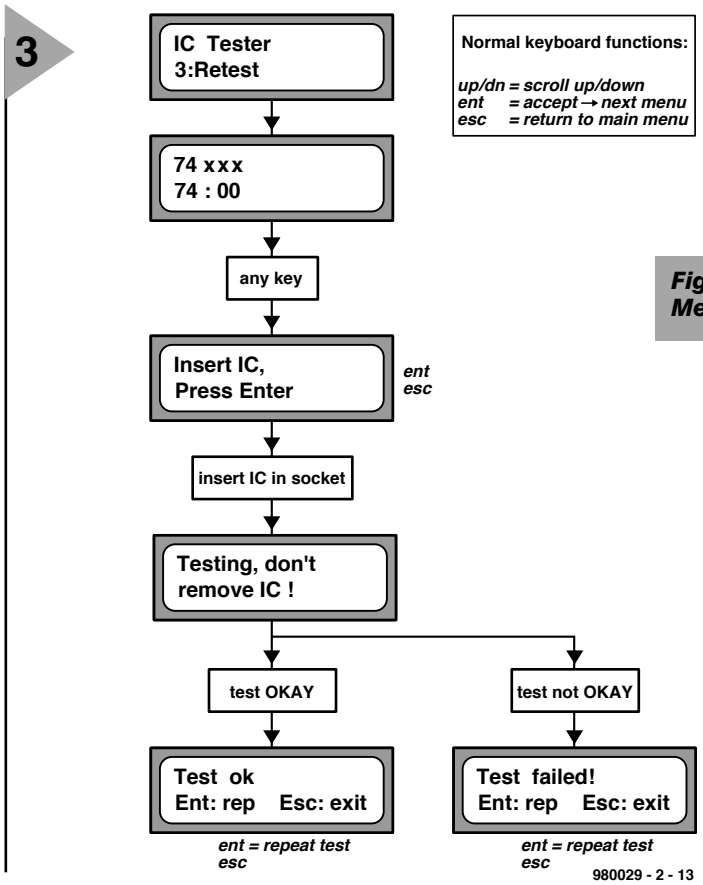


Figure 3. Structure of Menu option 3: Retest IC.

VECT **test_vector**
A test vector may consist of the following elements:

1 output pin: check if pin is at 1;
input pin: apply 1 to pin.

0 output pin: check if pin is at 0;
input pin: apply 0 to pin.

Z test if pin is at high impedance.

X do not test this pin.

The individual elements may be separated by spaces (not obligatory). If a pin is defined as 'GND', it should have a 0 at the relevant position in the test vector. Likewise, 'VCC' should be matched with a 1.

REPEAT **count,** ENDR
This keyword allows a loop to be implemented, containing test vectors (VECT) and pin function definitions (PINDEF). The loop is repeated 'count' times. Each loop has to be terminated with an 'ENDR' keyword. Nested loops are not allowed.

PULL **on_off**
This keyword tells the IC tester hardware to connect the IC outputs to pull-down resistors during the test (on_off = 1) or not (on_off = 0). When on_off is at 0, the outputs are continuously loaded by a pull-up resistor, and testing for a high-Z state is not possible.

ICCL
When this instruction is encountered, the regulated power supply measures the IC supply current. After the test, the supply current is indicated as 'ICCL'. 'ICCL' may only be used once for any one IC.

ICCH
When this instruction is encountered, the regulated power supply measures the IC supply current. After the test, the supply current is indicated as 'ICCH'. 'ICCH' may only be used once for any one IC.

The following points should be noted when writing your own test vectors for ICs not included in the default library.

- All IC inputs have to be made logic 0 and logic 1 at least once, in a manner that ensures that this change can be detected on at least one IC output.
- All IC outputs have to go 0 and 1 at least once during the test, and also 'Z' (high-impedance or tri-state) when an output can assume this state.
- With ICs having a sequential internal circuit, IC inputs driving the clock input of a register flip-flop may not change state in unison with inputs of these flip-flops, if this transition equals the active edge of the clock input. For example, the clock input of a 74:74 may not change from 0 to 1 when the level at the data input changes at the same time. This proviso also applies to clock and enable inputs of synchronous counters.
- If an enable input of a latching flip-flop toggles, the level at the data input of the flip-flop is not allowed to toggle at the same time. This applies to rising as well as falling pulse edges.

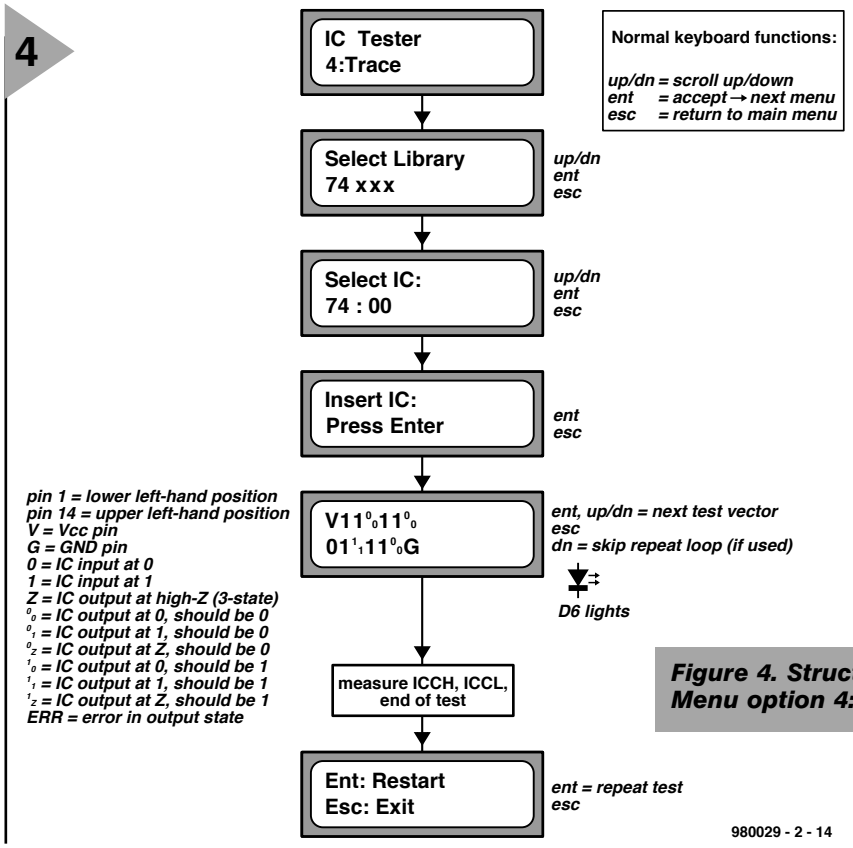


Figure 4. Structure of Menu option 4: Trace.

To close off this section, **Figure 9** shows

an example of a set of test vectors written for the type 4040 CMOS 12-stage ripple-carry binary counter. Although not all compiler keywords are used, the example is still useful to unravel the structure of the vectors in relation to the internal operation of the IC. A pinout diagram is included for your convenience. Note how the 'repeat' instruction is used to toggle the logic level at the clock pulse input (cp). Depending on the number of clock pulses applied in this way, a particular IC output (Q_x) should go high. The hardware monitors this output, and its level is compared with that stated by the test vector. For example, a logic 1 should occur on output Q8 of the 4040 after 128 clock pulses. If this logic one is not measured after the 'endr' instruction, in other words, if the response of the IC under test does not match the test vector after 'endr', the IC is identified as faulty, and may be binned! Comment is also used in this test vector script: the fourth line contains the logic labels of the IC pins. Note that some manufacturers of the 4040 start with output label Q1 rather than Q0 as indicated by the comment. This does not affect the operation of the IC, however.

More IC test vector scripts and internal diagrams are given on this month's *Datasheets*.

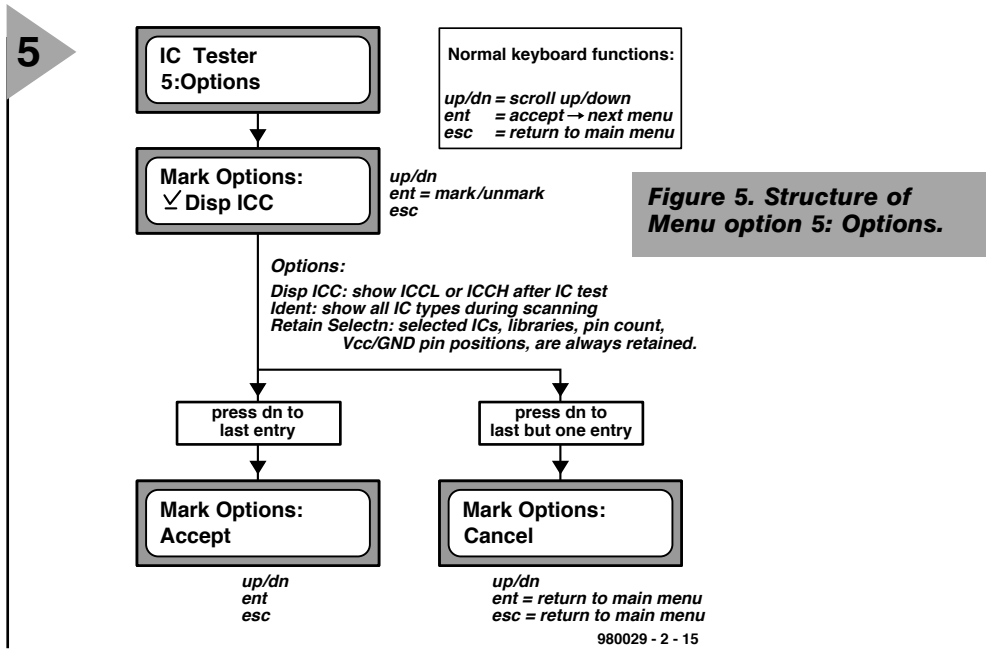


Figure 5. Structure of Menu option 5: Options.

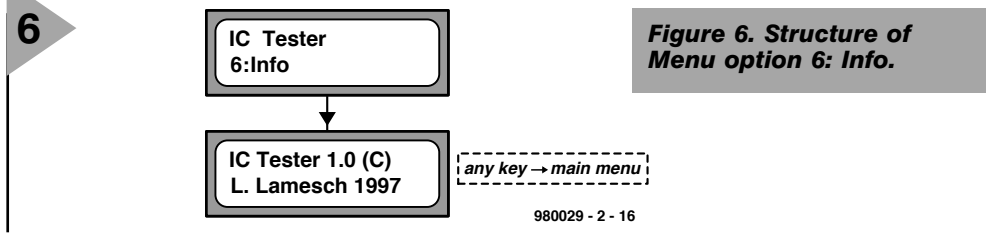


Figure 6. Structure of Menu option 6: Info.

TEST VECTOR COMPILING AND DEBUGGING

The purpose of analysing the master test-vector file as we just did is to enable you to write your own test scripts for ICs not included in the default library (see Table 1 in part 1). In principle, you only need a datasheet of the IC to reason how it *should* work. Eventually, you may want to add the new test vectors to the ones already available in 'vect.tvc', and burn the lot into a new system EPROM. The programs and general procedures to do so will be described below. Remember that all of the information presented below may be totally academic to you if you are satisfied with the collection of ICs in the default library.

Do not launch the programs directly from the floppy disk. First run `CHECK 1` from the DOS prompt as indicated on the floppy to make sure the data is intact and virus-free. Next, copy all files on the floppy to a suitably named subdirectory on the hard disk.

ICTVC.EXE

This is the **Test Vector Compiler**. Its function is to turn a test vector source file (like VECT.TVC) into a test vector binary file. Next, the latter file has to be appended to the microcontroller program, ICT.BIN, to create a large binary file that can be burned into an EPROM. File appending, by the way, is achieved with the aid of the DOS command `copy ict.bin+vect.out /b eprom.bin`.

The compiler is invoked by typing

```
ICTVC [source file.TVC]
```

For example,

```
ICTVC VECT.TVC
```

It generates the following files:

TVC.OUT: test vector file (binary);
ERR.OUT: error report;
LIST.OUT: list-file containing information on the source file, binary file, a copy of the source file with line num-

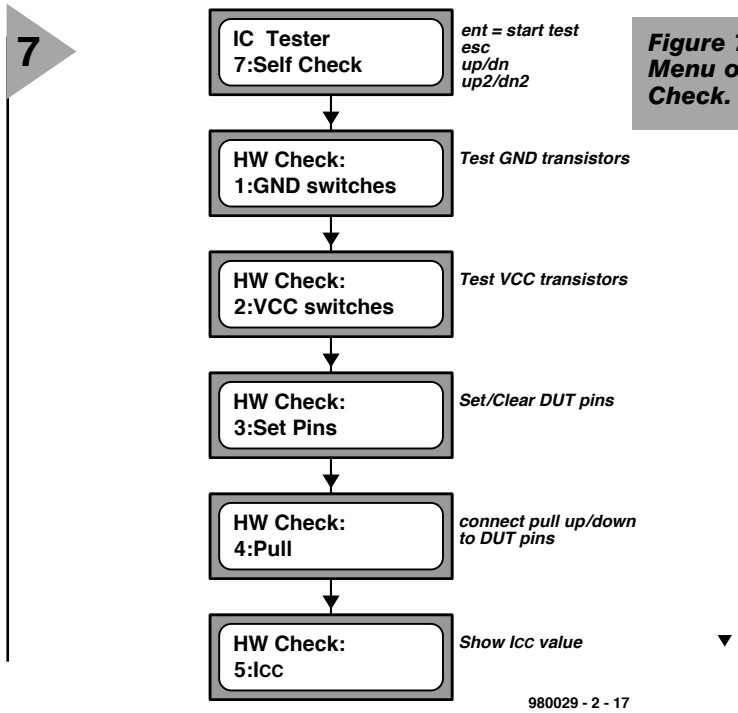


Figure 7. Structure of Menu option 7: Self Check.

8

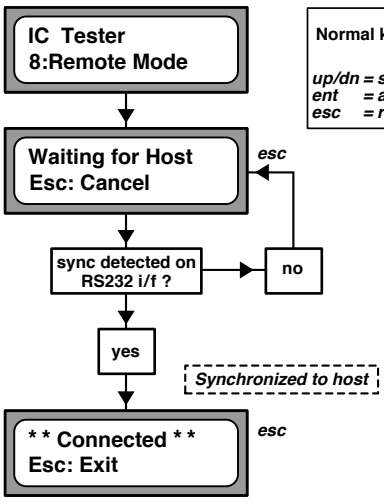


Figure 8. Structure of Menu option 8: Remote mode.

9

```
name         4040
; 12-bit CMOS ripple carry counter
pins      16
pinorder  10  11  1   15  14  12  13  4   2   3   5   6   7   9   8   16
;         /cp mr  q11 q10 q9  q8  q7  q6  q5  q4  q3  q2  q1  q0  gnd vcc
pindef    I   I   O   O   O   O   O   O   O   O   O   O   O   O   G   V
vect      0   1   0   0   0   0   0   0   0   0   0   0   0   0   0   1
vect      0   0   0   0   0   0   0   0   0   0   0   0   0   0   0   1
vect      1   0   0   0   0   0   0   0   0   0   0   0   0   0   0   1
vect      0   0   0   0   0   0   0   0   0   0   0   0   0   1   0   1
vect      1   0   0   0   0   0   0   0   0   0   0   0   0   1   0   1
vect      0   0   0   0   0   0   0   0   0   0   0   0   1   0   0   1
vect      1   0   0   0   0   0   0   0   0   0   0   0   1   0   0   1
vect      0   0   0   0   0   0   0   0   0   0   0   0   1   1   0   1
vect      1   0   0   0   0   0   0   0   0   0   0   0   1   1   0   1
vect      0   0   0   0   0   0   0   0   0   0   0   1   0   0   0   1
repeat 4
vect      0   0   0   0   0   0   0   0   0   0   0   0   X   X   X   0   1
vect      1   0   0   0   0   0   0   0   0   0   0   0   X   X   X   0   1
endr
vect      0   0   0   0   0   0   0   0   0   0   0   1   0   0   0   0   1
repeat 8
vect      0   0   0   0   0   0   0   0   0   0   0   X   X   X   X   0   1
vect      1   0   0   0   0   0   0   0   0   0   0   X   X   X   X   0   1
endr
vect      0   0   0   0   0   0   0   0   0   0   1   0   0   0   0   0   1
repeat 16
vect      0   0   0   0   0   0   0   0   0   0   X   X   X   X   X   0   1
vect      1   0   0   0   0   0   0   0   0   0   X   X   X   X   X   0   1
endr
vect      0   0   0   0   0   0   0   0   0   1   0   0   0   0   0   0   1
repeat 32
vect      0   0   0   0   0   0   0   0   0   X   X   X   X   X   X   0   1
vect      1   0   0   0   0   0   0   0   0   X   X   X   X   X   X   0   1
endr
vect      0   0   0   0   0   0   0   0   1   0   0   0   0   0   0   0   1
repeat 64
vect      0   0   0   0   0   0   0   0   X   X   X   X   X   X   X   0   1
vect      1   0   0   0   0   0   0   0   X   X   X   X   X   X   X   0   1
endr
vect      0   0   0   0   0   0   0   1   0   0   0   0   0   0   0   0   1
repeat 128
vect      0   0   0   0   0   0   0   X   X   X   X   X   X   X   X   0   1
vect      1   0   0   0   0   0   0   X   X   X   X   X   X   X   X   0   1
endr
vect      0   0   0   0   0   0   1   0   0   0   0   0   0   0   0   0   1
repeat 256
vect      0   0   0   0   0   0   X   X   X   X   X   X   X   X   X   0   1
vect      1   0   0   0   0   0   X   X   X   X   X   X   X   X   X   0   1
endr
vect      0   0   0   0   0   1   0   0   0   0   0   0   0   0   0   0   1
repeat 512
vect      0   0   0   0   0   X   X   X   X   X   X   X   X   X   X   0   1
vect      1   0   0   0   0   X   X   X   X   X   X   X   X   X   X   0   1
endr
vect      0   0   0   0   1   0   0   0   0   0   0   0   0   0   0   0   1
repeat 1024
vect      0   0   0   0   X   X   X   X   X   X   X   X   X   X   X   0   1
vect      1   0   0   0   X   X   X   X   X   X   X   X   X   X   X   0   1
endr
vect      0   0   0   1   0   0   0   0   0   0   0   0   0   0   0   0   1
vect      0   0   1   0   0   0   0   0   0   0   0   0   0   0   0   0   1
vect      0   1   0   0   0   0   0   0   0   0   0   0   0   0   0   0   1
vect      0   0   0   0   0   0   0   0   0   0   0   0   0   0   0   0   1
iccl      ; measure IC current
icch      ; measure IC current
```

bers added as well as the bytes generated from each line;
TMP.OUT: temporary file used by ICTVC.EXE.

Any errors occurring during the compilation process are recorded in ERR.OUT only. They do not appear on the PC screen.

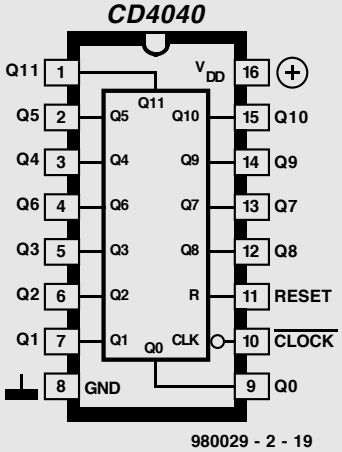
TVCHK.EXE

This is a kind of shell program that launches ICTVC.EXE, and enables test vector scripts to be debugged. For this program to operate you have to connect the IC Tester to your PC via the 3-wire serial link. TVCHK should be launched with an appended parameter which is either the COM port number (1-4), or the COM port address (in hex) followed by the associated interrupt line (1-7). Example: *TVCHK 2*. Obviously, we are talking of the COM port to which the IC Tester is connected! A screendump illustrating some of the options offered by TVCHK is shown in **Figure 9**.

EDT.BAT

This extremely small batch file is used to launch the word processor you will be using to load, modify and save test vector files. If you do not want to employ EDIT.COM, change EDT.BAT as required to make it point to your favourite DOS text editor. Type the name of the file you want to process after '*EDT*'. In case 'VECT.TVC' is too large for your wordprocessor, consider creating the part to be appended as a separate file. Once the new test-vector

Figure 9. Example illustrating the operation of a test vector script. The diagram and the script are all you need to put the 4040 12-bit counter through its paces.



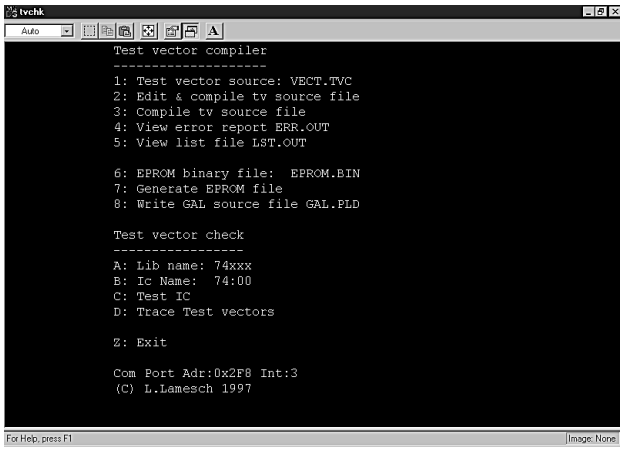


Figure 10. The TVCHCK program offers a useful shell around the utilities for test vector testing and compiling.

scripts have been debugged, they may be appended to VECT.TVC without using TVCHK. Next, the option 'Compile tv source' from TVCHK is used to compile the complete file for burning an EPROM.

A good start for practising is the file 'SMALL.TVC'. To get the feel, try replacing 'VECT.TVC' by 'SMALL.TVC' under menu option 2 in TVCHK.

The main menu of TVCHK comprises the following options:

Test Vector Compiler

1: Test vector source: VECT.TVC
Indicate name of test vector source file.
2: Edit & Compile tv source file.
3: Compile tv source file.
4: View error report ERR.OUT.
5: View list file LST.OUT.
6: EPROM binary file: EPROM.BIN
Indicate the name of the binary file to be burned into the EPROM.
7: Generate EPROM file.
Remember, the output format is binary!
8: Write GAL source file GAL.PLD.

Test Vector Checking

A: Lib name: 74xxx
Indicate name of the library containing the test-vector set to be tested/debugged.
B: IC name: 74:00
Indicate name of test-vector set to be tested/debugged.
C: Test IC
This may take a while when many test vectors have to be applied (e.g., more than 10 minutes when testing a script for the 4020).
D: Trace Test Vectors
This is the actual debugging tool. For each test vector, the expected logic states and the ones actually measured on the DUT are indicated. Errors are highlighted in red. Pin 1 is always indicated at the left-hand side, and the pin with the highest pin number, at the right-hand side. REPEAT…ENDR loops may be skipped by pressing the 's' key.
Z: Exit
Quit the program.
COM Port Addr: xxx Int: y
Tell the PC which COM port to use for communication with the IC Tester.

LARGER eproms

Those of you who wish to add test vector scripts for ICs not supported by the default system EPROM may soon find that the size of the .BIN file generated by TVCHK option '7' exceeds the capacity of a 512-kbit (64-kByte) EPROM like the 27(C)512. That is not a problem, however, because the IC tester hardware accommodates larger EPROMs like the 2-Mbit (256-kByte) 27020 without problems. Because these giant EPROMs are divided into 64-kByte banks, bank-switching then has to be implemented by means of outputs B6 and B7 of PIO device IC2. Address line A17 is then also required, so you have to set jumper JP1 to the 'not-A' position when using a 27C020 EPROM.

CONCLUSION

You have been reading an article discussing a test instrument which, in its standard version, allows a vast number of integrated logic circuits from the 74 (TTL) and 4000 (CMOS) series to be subjected to some pretty thorough testing. If you are not satisfied with the range of ICs that can be tested, a number of powerful software tools are available to 'roll your own', just using a common-or-garden PC (running plain old DOS) and, optionally, an EPROM programmer capable of handling EPROMs with a capacity of at least 512 kbits. Happy testing!

(980029-2)

The 100% DIY approach

Although the best guarantee to successful construction of this project is to order a ready-programmed GAL and EPROM from the Publishers, together with a PCB and a floppy disk (order as a set, order code 980029-C), there is are two alternative, cheaper, ways for the more audacious.

The CD-ROM entitled 'µP-µC Hard & Software 97-98' (order code 986001-1) contains THE WORKS, i.e., all files to program your own GAL and EPROM for this project, in addition to the 'master' test vector file, the 535's executable code, source code files in C and assembly language, and all software utilities mentioned in this instalment. So, if you are completely self-supporting, that is, have access to a PC, a GAL programmer and an EPROM programmer, we suggest buying just the PCB and the CD-ROM. The relevant subdirectory on the CD-ROM is /INT. Remember, you can not run the test vector utilities from the CD-ROM since they need to create files!

The second option for the more advanced among you is to buy only the PCB and the floppy disk. The floppy contains a sub-set of the files on the CD-ROM: not included are the assembler files and the PCB artwork and circuit diagrams as originally supplied by the author. For the rest, everything is included to create and debug your own test vector files, and prepare a binary file for burning into an EPROM, as described in this article. The .JED file for programming your own GAL is also included.

Whichever option you choose, remember that any hardware or software component needed to build (and understand) this project is available separately through our Readers Services.

APPLICATION NOTE

µProcessor System Hardware Monitor

Single IC monitors whole system

Features

- *Temperature sensing*
- *Five positive voltage inputs*
- *Two op amps for negative voltage monitoring*
- *Three fan speed monitoring inputs*
- *Input for additional temperature sensors*
- *Chassis Intrusion Detector input*
- *WATCHDOG™ comparison of all monitored values*
- *POST code storage RAM*
- *ISA and I²C™ Serial Bus Interfaces*

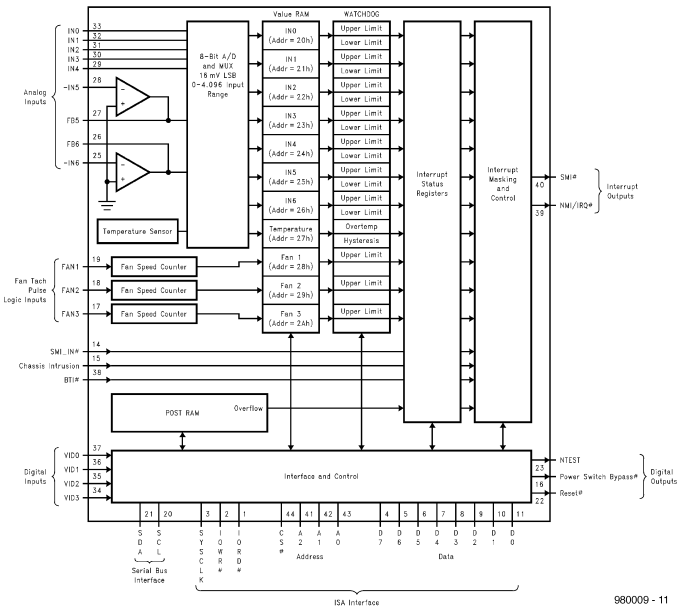
A computer system or, indeed, any microprocessor-based system, can operate reliably only when its internal temperature and supply rails are held stable within specified limits. The hardware monitoring of these quantities, and others, is simplified by National Semiconductor's new Integrated Data Acquisition System Type LM78.

GENERAL DESCRIPTION

The LM78 is intended for hardware monitoring of servers, PCs, or virtually any microprocessor-based system. In a PC, the LM78 may be used to monitor power supply voltage, temperatures, and fan speeds. Actual values of these quantities can be read at any time, and programmable WATCHDOG™ limits in the LM78 actuate a fully programmable and maskable interrupt system

Figure 1. Block diagram of the LM78.

1



WATCHDOG™ is a trademark of National Semiconductor Corporation

I²C™ is a registered trademark of the Philips Corporation

A National Semiconductor Application

with two outputs.

The LM78 has an on-chip temperature sensor, five positive analogue inputs, two inverting inputs (for monitoring negative voltages), and an eight-bit Delta-Sigma analogue-to-digital converter (ADC). See the block diagram in **Figure 1**.

An input is provided for the overtemperature outputs of additional temperature sensors and this is linked to the interrupt system.

The LM78 provides inputs for three fan tachometer outputs. Additional inputs are provided for chassis intrusion detection circuits, VID monitor inputs, and chainable interrupt.

The LM78 provides both ISA and Serial Bus interfaces. A 32-byte auto-increment RAM is provided for POST (Power On Self Test) code storage.

FUNCTIONAL DESCRIPTION

The LM78 continuously converts analogue inputs to 8-bit digital words with a 16 mV LSB (least significant bit) weighting, yielding input ranges of 0–4.096 V. The two negative analogue inputs provide inverting op amps with their non-inverting input referred to ground. With additional external feedback resistors, these inputs provide measurements of negative voltages (such as –5 V and –12 V power rails). The values of these resistors for a number of voltage measurements are shown in **Figure 2**. The result of the various processes is stored in a bank of registers (20_H–$2A_H$) which are found under Value RAM in Figure 1. The analogue inputs are useful for monitoring several power supplies present in a typical computer.

Temperature is converted to an 8-bit two's-complement digital word with a 1 °C LSB.

Fan inputs measure the period of tachometer pulses from the fans, providing a higher count for lower fan speeds. The fan inputs are digital inputs with an acceptable range of 0–5 V and a transition level of about 1.4 V. Full-scale fan counts are 255 (8-bit counter) and this represents a stopped or very slow fan. Nominal speeds, based on a count of 153, are programmable from 1100 to 8800 rev/min. Signal conditioning circuitry is included to accommodate slow rise and fall times.

The LM78 provides a number of internal registers as detailed in **Figure 3**. These include

Configuration Register providing control and configuration of the chip.

Interrupt Status Registers. providing the status of each WATCHDOG™ limit or event.

Interrupt Mask Registers allowing masking of individual interrupt sources, as well as separately masking each of both hardware interrupt outputs.

VID/Fab Divisor Register for reading the status of the VID input lines. The high bits of this register contain the divisor bits for Fan1 and Fan2 inputs.

Serial Bus Address Register which contains the Serial Bus address. At power on, it assumes the default value of 0101101, and can be altered via the ISA or Serial Bus Interface.

Chip Reset/ID Register which allows the resetting of all the registers to the default power-on reset value. It provides a bit for identification between the current version of the device and an older version which does not have this reset capability.

POST RAM. This FIFO RAM stores up to 32 bytes of 8-bit POST codes. Overflow of this register will set an interrupt. The register, located at base address x0h and x4h, allows

2

Voltage Measurements (V_S)	R1 or R_{IN}	R2 or R_F	Voltage at Analog Inputs
+2.50V	0	NONE	+2.50V
+3.30V	0	NONE	+3.30V
+5V	6.8 kΩ	10 kΩ	+2.98V
+12V	30 kΩ	10 kΩ	+3.00V
12V	240 kΩ	60 kΩ	+3.00V
5V	100 kΩ	60 kΩ	+3.00V

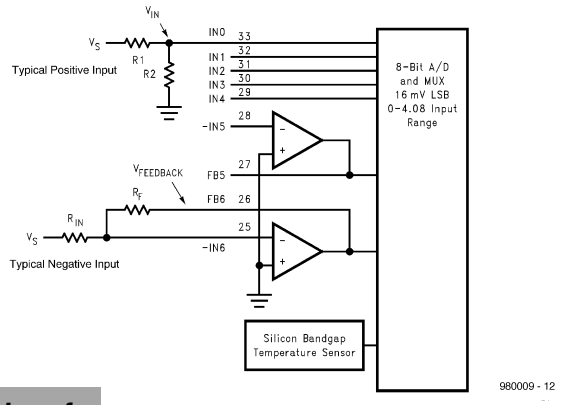


Figure 2. Examples of the analogue inputs that monitor the supply rails in a PC. The resistor values shown provide about 3 V at these inputs.

3

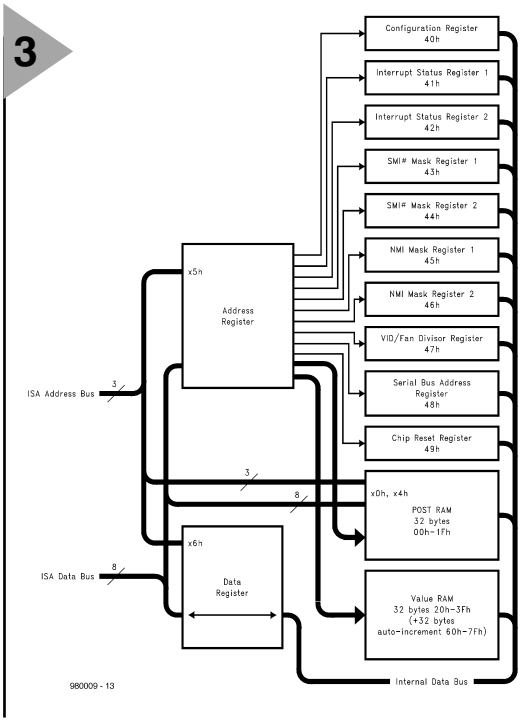


Figure 3. Register structure of the LM78. Relevant software sets the limits at which interrupt lines will be set. Monitoring results are easily read.

for easy decoding to address 80h and 84h, the normal addresses for outputting of POST codes. Interrupt will be set only when writing to port x0h or x4h is taking place. The register can be read via ports 85h and 86h.

Value RAM containing the monitoring results: temperature, voltages, fan counts, and WATCHDOG™ limits. This register consists of a total of 64 bytes. The first 11 bytes are all of the results, the next 19 bytes are the WATCHDOG™ limits, and are located at 20h–3Fh, including two unused bytes in the upper locations. The next 32 bytes, located at 60h–7Fh, mirror the first 32 bytes with identical contents. The only difference in the upper bytes is that they auto-increment the LM78 Internal Address Register when read from, or written to, via the ISA Bus (auto-increment is not available for Serial Bus communications).

When the LM78 is started, it cycles through each measurement in sequence, and it continuously loops through the sequence about once every second. Each measured value is compared to values stored in WATCHDOG™ or Limit registers.

When the measured value violates the programmed limit, the LM78 will set a corresponding interrupt in the Interrupt Status. Two hardware interrupt lines, SMI# (System Management Interrupt) and NMI/IRQ# (Non-maskable interrupt/interrupt request), are fully programmable with separate masking of each interrupt source, and masking of each output. In addition, the Configuration Register has control bits to enable or disable the hardware interrupts.

INTERFACE

The LM78 decodes only the three lowest address bits on the ISA Bus, resulting in the following base addresses.

Port x0h: POST codes from the ISA Bus.
Port x4h: POST codes from the ISA Bus.
Port x5h: The LM78 Internal Address Register.
Port x6h: Data Register.

IORD# is the standard ISA Bus signal that indicates to the LM78 that it may drive data on to the ISA data bus.

IOWR# is the standard ISA command to the LM78 that it may latch data from the ISA Bus.

SYSCLK is the standard ISA system clock, typically 8.33 MHz. This clock is used only for timing of the ISA interface. All other clock functions within the LM78, such as the ADC and fan counters, are done with a separate asynchronous internal clock.

A typical application designed to use the POST RAM would decode the LM78 to the address space starting at 80h, which is where POST codes are output to. Otherwise, the LM78 can be decoded into a different desired address space.

To communicate with an LM78 register, first write the address of that register to Port x5h. Read or write data from or to that register via Port x6h. A write will take IOWR# low, while a read will take IORD# low.

If the Serial Bus interface and ISA Bus interface are used simultaneously, there is the possibility of collision. To prevent this from occurring in applications where both interfaces are used, read Port x5h and if the Most Significant Bit (MSB), D_7, is high, ISA communication is limited to reading Port x5h only until this bit is low. A Serial Bus communication occurring while ISA is active will not be a problem, since even a single bit of Serial Bus communication requires 10 microseconds, in comparison to less than a microsecond for an entire ISA communication.

TYPICAL APPLICATION

The setup of a typical application is shown in **Figure 4**. It monitors temperature, the speed of three fans, and seven power supply voltages. The chassis intrusion detector is based on a photodiode and discrete bistable. When the chassis has been opened (intruded), the relevant data are stored thanks to a battery backup. The bistable may be reset via the LM78.

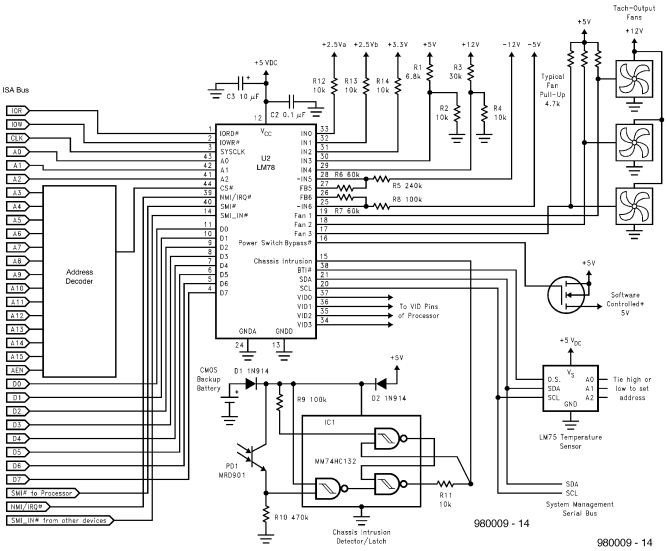
A link with the System Management Serial Bus of the PC may be established via the I²C™ Bus.

A software-controlled 5 V power supply is provided with the aid of a MOSFET. This supplies the entire circuit, which draws a current of only about 1 mA during normal operation, and about 10 µA in the standby mode.

[980009]

Figure 4. In this application, the LM78 monitors temperature, fan speed of three fans, and seven power supply voltages. It also monitors the O.S. output of up to eight LM75 digital temperature sensors as well as an optical chassis intrusion detector.

4



introduction to digital signal processing

Part 4 – From echo to FIR filter

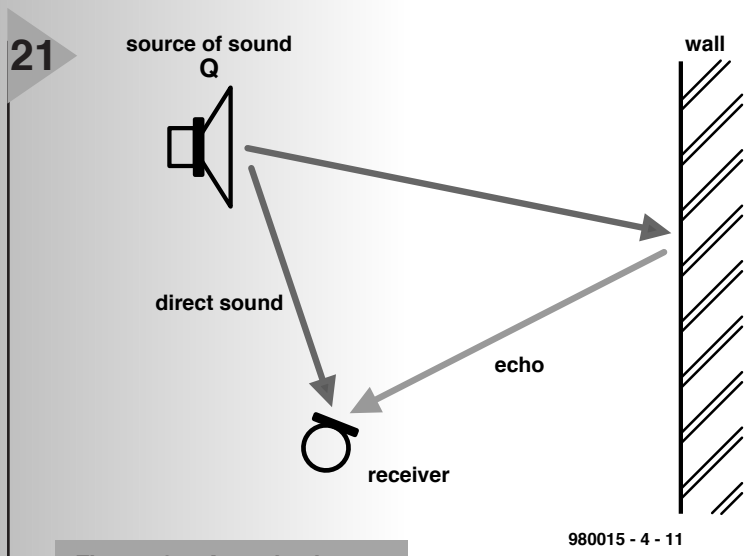


Figure 21. An echo is caused by reflection of the original sound by an object, and is subject to attenuation and delay.

An important function of digital audio signal processing is the generation of reverberation and echo. This instalment looks at how echoes can be generated in a simple manner and how the knowledge gained in this can be put in a general form. These findings lead naturally to digital filters.

By Dr. Ing. M. Ohsmann

SINGLE ECHO

An echo is the repetition of a sound by reflection of sound waves by an object in the path of the original sound. Thus, the reflected sound is identical to the original sound, except for some attenuation and a time delay. If the delay is M samples long, the received signal is

$$y_k = s_k + a s_{k-M},$$

where s_k is the original sound, a is the attenuation constant and s_{k-M} is the delayed signal. How can this be arranged as a program? It is clear that to determine signal y_k at a point in time k, the input signal M samples ago must be known. For this, a buffer is required that can hold at least M sample values. The most appropriate for this is a circulating register in which a data stream circulates in a loop. It is reminiscent of the old echo generators that used an endless magnetic tape for storage. The difference is, however, that in a circulating register the read and write heads move, but not the data as with the endless magnetic tape.

A program (ECHO1.PAS) for $M = 8192$ samples is given in **Figure 2**.

The time delay depends on the sampling rate. If, for example, the rate is 22050 samples/s, the time delay is 8192/22050 = 0.37 s. First, listen to the original file WD1R.WAV, then produce it with the instruction

```
ECHO1 \inp= wd1r.wav
out= tmp.wav
```

and furnish it with an echo that can be heard clearly in file TMP.WAV.

MULTIPLE ECHOES

A single echo is not often satisfactory. To obtain two or more echoes, the original sound must be combined with a

Window functions

The frequency characteristic of a digital filter is a periodic function related to the sampling period, T, which can be expanded as a Fourier series. The coefficients of this series represent the impulse response of the filter. When, in a practical case, this infinite series has to be truncated to n terms, the sharp cut-off leads to overshoots and oscillations in the characteristic. This is know as the *Gibbs phenomenon* and the effect can be minimized by multiplying the impulse response by a weighting factor described as a *window function w(n)*. This function can easily be incorporated in the design of an FIR. Some of the common window functions have the mathematical form listed below.

Rectangular	$w(n) = 1$	$0 \le n \le (N-1)$
Triangular	$w(n) = 2n/(N-1)$	$0 \le n \le (N-1)/2$
Bartlett	$w(n) = 2-[(2n)/(N-1)]$	$(N-1)/2 \le n \le (N-1)$
Hanning	$w(n) = 0.5-0.5\cos[(2\pi n)/(N-1)]$	$0 \le n \le (N-1)$
Hamming	$w(n) = 0.54-0.46\cos[(2\pi n)/(N-1)]$	$0 \le n \le (N-1)$

number of reflections that have been delayed by times L and M, and attenuated by factors a and b.

$$y_k = s_k + as_{k-L} + bs_{k-M}.$$

If still more echoes are desired, use more addends as appropriate. There is a program for this on the CD-ROM entitled FIRFIL1. The true meaning of this name will be revealed later. It enables the computation of echoes in general. The number of echoes required must be specified, together with their time delay and amplitude, by a number in a file. For example, with the file XECHO2.SPP

```
\\file 'exec.bat'
firfil1\inp= speech1.wav\out=
tmp.wav\filter= fir1.fir
\\eof

\\file 'fir1.fir 'a simple test filter0
0       0.5
3000    0.4
6000    0.3
12000   0.2
16000   0.1
\\eof

\\end
```

five echoes are obtained with delay times 0, 3000, 6000, 12000 and 16000 samples long, and amplitudes 0.5, 0.4, 0.3, 0.2, 0.1. The maximum delay is 16383 samples long, and the maximum number of echoes is 1000.

Try these echoes with XECHO2.SPP. In file TMP.WAV, a number of beautiful echoes may be heard. The addition of a sufficiently large number of echoes results in reverberation.

FIR FILTERS*

The program FIRFIL1 is capable of much more than the generation of echoes. As an experiment, generate a sweep signal and pass it through the filter defined in ECHO3.SPP. This results in 256 echoes with rather unusual values as may be seen on the oscillogram in **Figure 23**. This clearly indicates that the sweep signal is passed over a certain frequency range only: that is, the filter is a band-pass section.

Unfortunately, it is not easy to average the sound intensity of 256 echoes in a manner that results in a band-pass function. Before the actual technique is discussed, we will take a look at how finite impulse response (FIR) filters* function.

A FIR filter that generates echoes with time delays 0, 1, 2, … and sound intensities $a_0, a_1, a_2, \ldots$ is described by the equation

$$y_k = a_0x_k + a_1x_{k-1} + a_2x_{k-2} + \ldots$$

where x_k and y_k are the input and output values respectively.

To find the impulse response of the filter, that is, the value of y_k when $x_0 = 1$ and all other values $x_j = 0$, we must first calculate the value of

$$y_0 = a_0x_0 + a_1x_{-1} + a_2x_{-2} + \ldots$$

Only the first term remains, so that $y_0 = a_0$.

When $k = 1$,

$$y_1 = a_0x_1 + a_1x_0 + a_2x_{-1} + \ldots$$

* Also known as non-recursive filters or transversal filters.

22

```
program echo1 ;
uses dos,crt,graph ;
{I SIGLIB.PAS }

var k:int;
      x,y:float ;
      buffer:array[0..8191] of float ;
      pointer:int ;

begin
start('simple echo') ;
inp_fn:='tmp1.wav'     ; set_par_string('\inp=',inp_fn) ;
out_fn:='tmp.wav'      ; set_par_string('\out=',out_fn) ;

open_inp(inp_fn) ;
open_out(out_fn) ;

pointer:=0 ;
for k:=0 to 8191 do buffer[k]:=0 ;

for k:=1 to nsamples do
   begin
   x:=input ;
   y:=buffer[pointer] ;
   buffer[pointer]:=x ;
   pointer:=pointer+1 ;
   if pointer>=8192 then pointer:=0 ;
   output(x+0.5*y) ;
   end ;

stop ;
end.
```

Figure 22. Program for generating an echo.

23

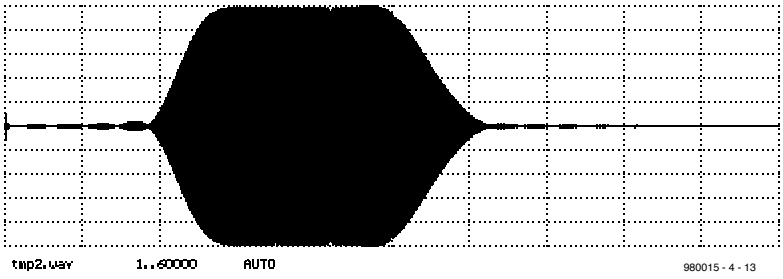


Figure 23. When a sweep signal is passed through an echo-filter, the result is a band-pass characteristic.

24

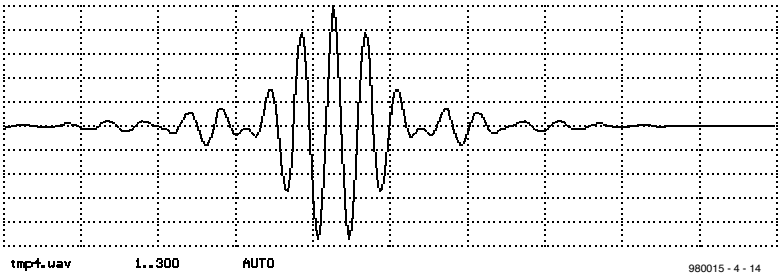


Figure 24. Impulse response of a band-pass filter.

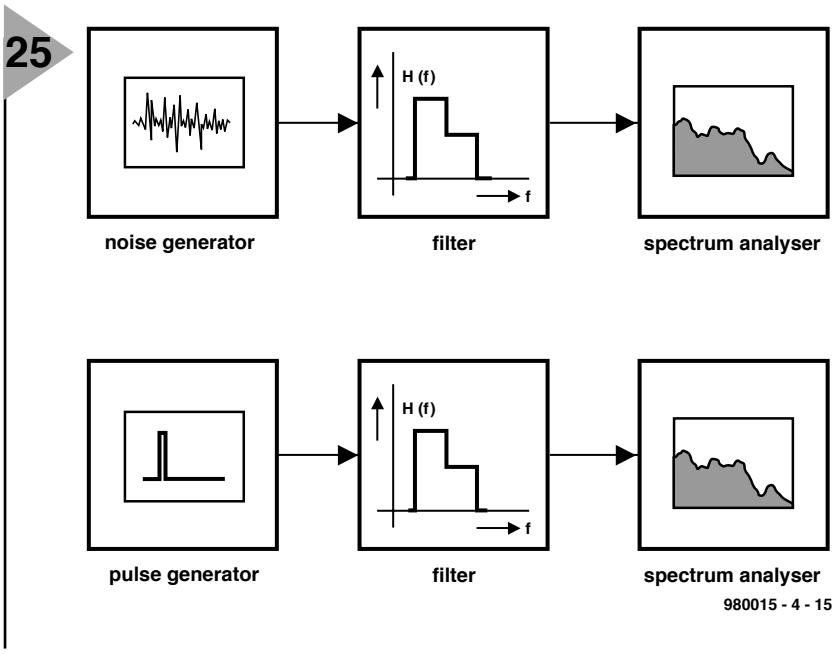


Figure 25. Noise and pulse signals contain all frequencies.

only the second term remains, so that $y_1 = a_1$.

Continuing this process shows that for all values of $k \geq 0$, $y_k = a_k$. This means that the impulse response is the filter coefficient. In other words, if an impuls is passed through such a filter, the result is the filter coefficient. This is due to the second part of XECHO3.SPP. The impuls response of the filter just discussed is shown in **Figure 24**. It resembles that of an oscillating circuit. This is to be expected because hardware band-pass filters behave like coupled oscillating circuits.

ALL-FREQUENCY SIGNALS

In Part 3, a noise signal was used to determine the frequency response of a filter. This is possible since one of the properties of white noise is that it contains all frequencies at the same amplitude. After the signal has been passed through a band-pass filter (**Figure 25** top), all frequencies in the out-

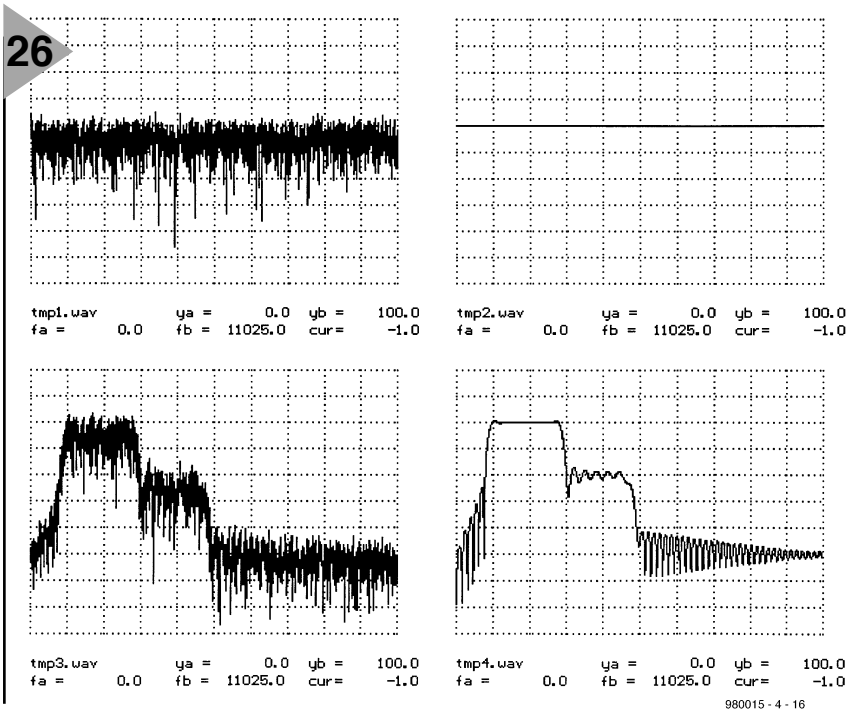


Figure 26. Determining the frequency response with a noise signal (left) or a pulse (right). At the top, the input signals, and below the output signals.

put still have the same amplitude (see **Figure 26** left) (Experiment XPULSE1.SPP).

When noise signals are used, arriving at a result through averaging takes a fairly long time. Researchers therefore asked themselves whether there is another kind of signal that gives quicker results and still contains all frequencies. The answer is: yes, a pulse as produced by signal generator PULSE1.EXE.

The spectrum of this pulse shows a virtually constant amplitude for all frequencies (**Figure 26** right). Thus, the noise signal used for determining the frequency response may be replaced by a pulse.

A filter reacts to a pulse in accor-

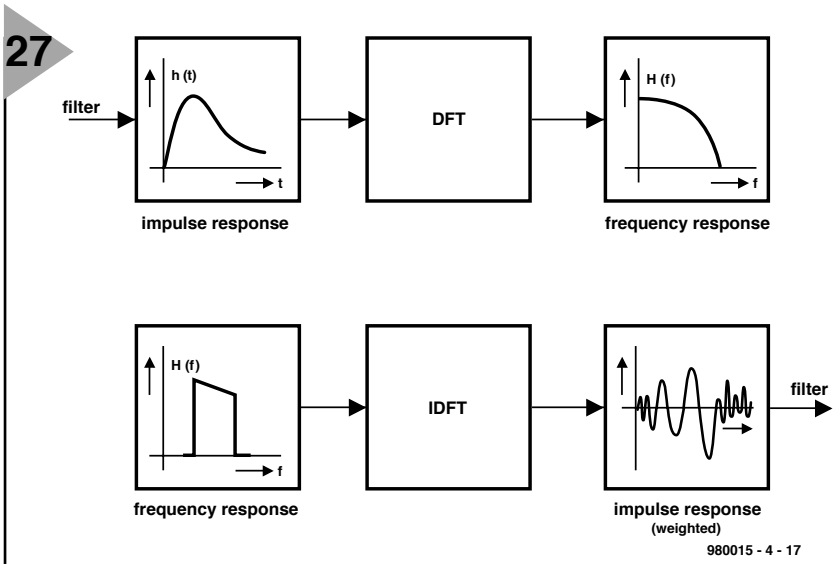


Figure 27. A DFT enables the frequency response to be determined from the impulse response. An IDFT enables the impulse response to be determined from the frequency response.

dance with its impulse response. This contains all frequencies at the same level as they are passed by the filter, or, in other words, the spectrum of the impulse response is the same as the frequency response of the filter, as shown by tmp3.wav and tmp4.wave in Figure 26. This is an important principle of DSP, which can also be expressed in mathematical terms.

When the spectrum and impulse response are to be determined by a spectrum analyser, the window function (see box) must be disabled to avoid erroneous results. It is important that the impulse response is short enough (here, 4096 samples) to ensure that it fits in the DFT (Discrete Fourier Transform) of the spectrum analyser.

Determining the frequency response of a filter by means of a DFT of its impulse response (see **Figure 27**) is a fast, simple and accurate method. However, when the frequency response of an amplifier is to be determined, care must be taken to ensure that the input pulses cannot overload the amplifier. If this means the use of low-level pulses, the result may be a very poor signal-to-noise ratio. In such cases, pseudo-noise signals, which have a limited amplitude over the whole frequency range, are often used.

FILTER DESIGN

Since the frequency response of a filter may be determined by a DFT of its impulse response, the question arises whether the impulse response can be derived from the frequency response by an Inverse Discrete Fourier Transform (IDFT), to which the answer is: 'yes'. Moreover, when the impulse response is known, the filter may be simulated with the aid of program FIRFIL1.EXE. Filters in digital signal processors are frequently designed in this way.

The design of FIR filters is simplified by program SPECFIL1.EXE. The operation is shown diagrammatically in the lower row of Figure 27. From the frequency response of a filter, its impulse response is determined by an IDFT, which is modified by a window function (see box). This enables the properties of the filter to be fine-tuned. The impulse response of the filter is then written into a file, which processes the FIR program as a data input. A file (XFILDES.1.SPP) to compute a simple filter is shown in **Figure 28**.

The filter specification, the sampling rate, the number of samples in the impulse response, the parameters of the window function, and the value of amplification at the desired frequencies are given in file TMP.FIL. The amplification between the stated frequencies is interpolated linearly as shown in **Figure 29**.

The result of the program is shown in **Figure 30**. At the top left are the default and actual frequency responses on a logarithmic scale. The impulse response is at the bottom left, and the frequency response on a linear scale is at the bottom right.

[980015-4]

28

```
\\file 'exec.bat'
\\ generate filter
specfil1 \filter=tmp.fil \fir=tmpa.fir \bitmap=pic.ps
\\eof

\\ filter specification

\\file 'tmp.fil'
a simple filter as example
normal
44100     ; sample frequency
128       ; number of taps
7         ; alpha for window
7         ; number of data points in frequency domain
0       0
1990    0
2000   100
5000   100
5200   10
8000   10
8200   0
\\eof
```

Figure 28. Data file XFILDES1.SPP

29

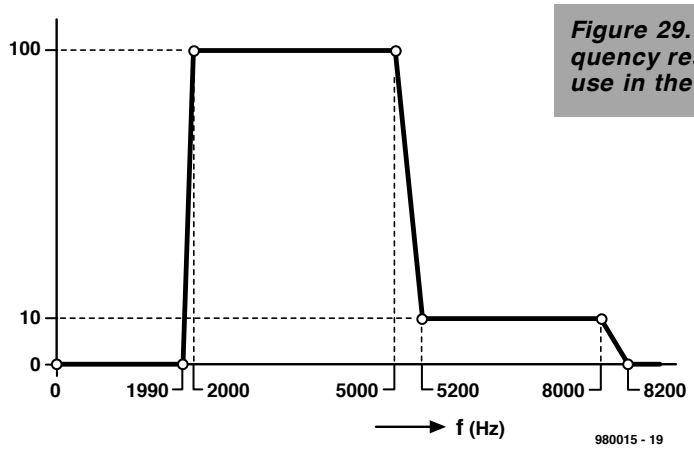


Figure 29. Default frequency response for use in the filter design.

30

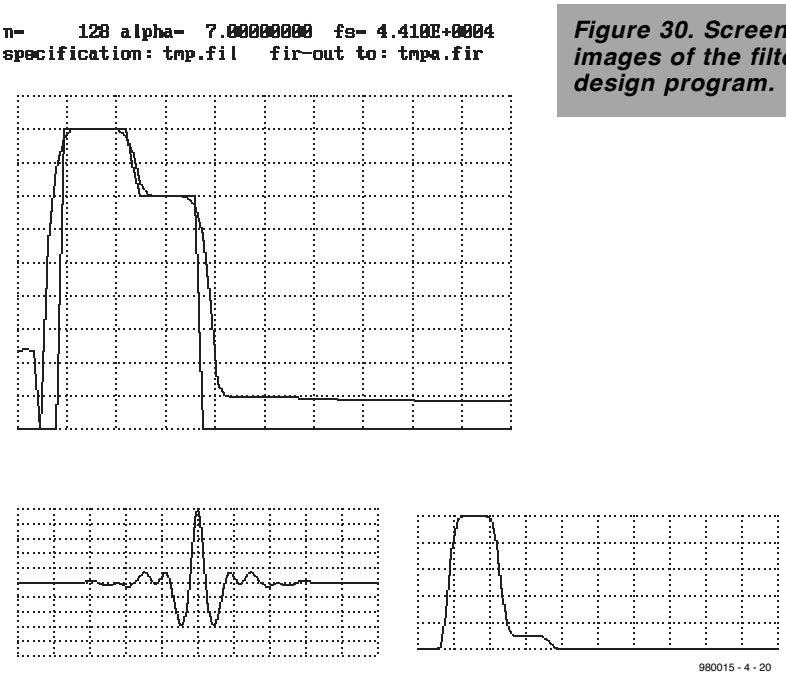


Figure 30. Screen images of the filter design program.

We can only answer questions or remarks of general interest to our readers, concerning projects not older than two years and published in *Elektor Electronics*. In view of the amount of post received, it is not possible to answer all letters, and we are unable to respond to individual wishes and requests for modifications to, or additional information about, *Elektor Electronics* projects.

PCB Design System

Dear Editor—I am looking for a PCB design system that allows me to first simulate the electrical operation of a circuit and then use turn the approved circuit diagram into PCB artwork. Having read all reviews and adverts in *Elektor Electronics*, I am none the wiser. Therefore, I am curious to know what software is being used in the *Elektor Electronics* design laboratory.

T. Will (by email)

The PCB design process adopted by ourselves is by no means unusual: once a certain software system has been accepted, it is updated and extended whenever necessary, enabling it to grow with our requirements.
In our design lab, the cad age dawned about 10 years ago with the introduction of Ultimate Technology's Ultiboard pcb design program suite. At that time, the dos version was used on at computers. Because Ultiboard was just a pcb design program at that time, a different program had to be used for schematic drawing: Orcad sdt. This combination is still in use as we write this. Pspice has been in use since 1989 for circuit simulation tasks.
The article 'Printed Circuit Board Production' in Elektor Electronics November 1994 briefly describes our pcb production process.

Stereo Microphone Amplifier

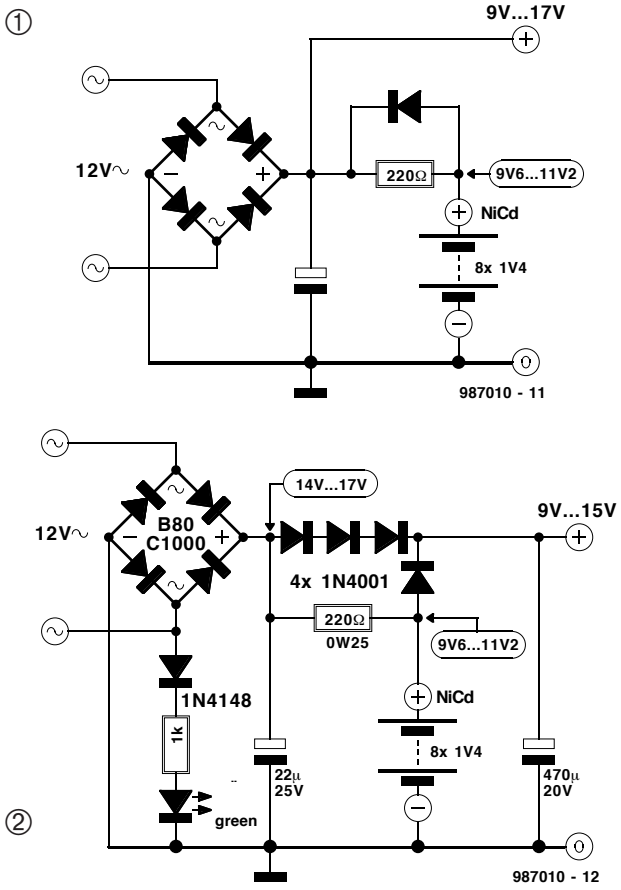
Dear Editor—A while ago you published a superb audio A/D converter ('20-bit A/D Converter', December 1996—Tech. Ed.), so I really looked forward to seeing the 'Stereo Microphone Amplifier' (November 1997—Tech. Ed.). I was a little disappointed, however, when I saw the output configuration: unbalanced! I had already omitted the unbalanced input from the A/D converter circuit. How about doing a microphone preamplifier with a balanced input to match the above mentioned converter?

B. Gillisberger (by email)

We're pretty sure that the microphone preamplifier meets your demands—it just lacks a balanced output. Enter our SSM412-based converter from the article 'Balanced/Unbalanced Converters for Audio Signals' (March 1998), which offers the perfect solution. Preset P1 is then the equivalent of P1a (or P1b for the other channel) at the output of the microphone preamp. The SSM4142 board is conveniently powered by the ± 18-volt supply for the microphone preamplifier.

Diodes instead of a relay?

Dear Editor—Since I was fortunate enough to receive a cordless telephone as my Christmas present, your article 'Uninterruptible Power Supply for Cordless Telephones' came at the right time.
Notwithstanding the obvious merits of the circuit, I wish to criticise you on the use of a relay. Are you out of diodes? Normally (circuit diagram no. 1—Tech. Ed.), the battery pack is charged via the resistor. When the mains voltage disappears, the voltage across the reservoir capacitor drops until the diode starts to conduct, eventually enabling the battery to take over. A much smaller reservoir capacitor may be employed because it is no longer necessary to cover the time needed by the relay to change state.



The no-load voltage of 17 V is a bit too high, I think, because the print on original mains adaptors usually reads something like 9.0-15 V. Additional voltage regulation is, however, by no means required because that is usually catered for by the telephone set itself. A couple of diodes are all it takes to replace the (expensive) relay, and an indicator LED is, no doubt useful (circuit diagram no. 2—Tech. Ed.). An alternative would be to use a transformer with a 10-V secondary. However, I realise that the battery charging voltage may then be on the low side.

W. Pressner

Thanks for your positive criticisms. Even if we do not have enough diodes to start trading, stocks levels easily meet our lab requirements, so that is not the reason for using a relay. The point is that there are always different ways of arriving at circuits with relatively simple functionality. True, the use of a diode is one of the best known solutions to this kind of problem, but it is no more original than a relay. At some moment, the original designer of this circuit, Pradeep G. (a reader of our Indian sister-magazine) decided in favour of the relay-based solution, which works fine, and was no cause for our lab staff to do major revisions on the circuit. Not mentioning the fact that a relay contact does not introduce a serious voltage drop, it has the distinct advantage of electrically disconnecting the telephone from the mains outlet. Surely this has to be a great boon in a country where the mains supply is, at best, unpredictable. The relay does not respond immediately when the mains voltage disappears or returns, the short delay enabling voltage surges to be kept away from the telephone set. Finally, it is our opinion that there is nothing improper about using a relay!

IC Tester

Elektor Electronics
March & April 1998

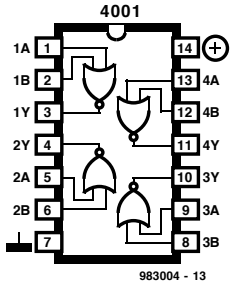
ELEKTOR ELECTRONICS

DATASHEET 4/98

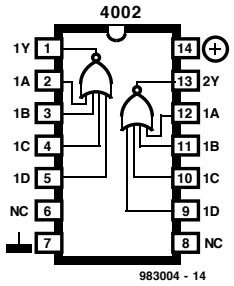
IC Test Vectors (illustrated examples) Extract from: vect.tvc

Note: tabbed formatting and IC functional diagrams added for clarity's sake, these are not available in file 'vect.tvc'.
1 = logic high 0 = logic low G = ground V = positive supply voltage
I = input O = output nc = not connected XX = don't care
** = vectors not yet verified with a correctly operating IC*
iccl = measure supply current icch = measure supply current

name	4001												
pins	14												
pinorder	1	2	3	6	5	4	13	12	11	8	9	10	7	14
pindef	I	I	O	I	I	O	I	I	O	I	I	O	G	V
vect	0	0	1	1	1	0	1	1	0	1	1	0	0	1
vect	1	0	0	1	1	0	1	1	0	1	1	0	0	1
vect	0	1	0	1	1	0	1	1	0	1	1	0	0	1
vect	1	1	0	0	0	1	1	1	0	1	1	0	0	1
vect	1	1	0	0	1	0	1	1	0	1	1	0	0	1
vect	1	1	0	1	0	0	1	1	0	1	1	0	0	1
vect	1	1	0	1	1	0	0	0	1	1	1	0	0	1
vect	1	1	0	1	1	0	0	1	0	1	1	0	0	1
vect	1	1	0	1	1	0	1	0	0	1	1	0	0	1
vect	1	1	0	1	1	0	1	1	0	0	0	1	0	1
vect	1	1	0	1	1	0	1	1	0	0	1	0	0	1
vect	1	1	0	1	1	0	1	1	0	1	0	0	0	1
vect	1	1	0	1	1	0	1	1	0	1	1	0	0	1
iccl														
vect	0	0	1	0	0	1	0	0	1	0	0	1	0	1
icch														



name	4002												
pins	14												
pinorder	2	3	4	5	1	12	11	10	9	13	7	14	6	8
;	1a	1b	1c	1d	1y	2a	2b	2c	2d	2y	gnd	vcc	nc	nc
pindef	I	I	I	I	O	I	I	I	I	O	G	V	O	O
vect	1	0	0	0	0	0	0	0	0	1	0	1	X	X
vect	0	1	0	0	0	0	0	0	0	1	0	1	X	X
vect	0	0	1	0	0	0	0	0	0	1	0	1	X	X
vect	0	0	0	1	0	0	0	0	0	1	0	1	X	X
vect	0	0	0	0	1	1	0	0	0	0	0	1	X	X
vect	0	0	0	0	1	0	1	0	0	0	0	1	X	X
vect	0	0	0	0	1	0	0	1	0	0	0	1	X	X
vect	0	0	0	0	1	0	0	0	1	0	0	1	X	X
vect	0	0	0	1	0	0	0	0	1	0	0	1	X	X
iccl														
vect	0	0	0	0	1	0	0	0	0	1	0	1	X	X
icch														



AD557

Integrated circuits
Special Applications

ELEKTOR ELECTRONICS

DATASHEET 4/98

AD557
DACPORT, Low-Cost Complete µP-Compatible 8-bit DAC

Manufacturer

Analog Devices, One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, USA. Tel. (617) 329-4700, fax (617) 326-8703.
Internet: www.analog.com.

Features

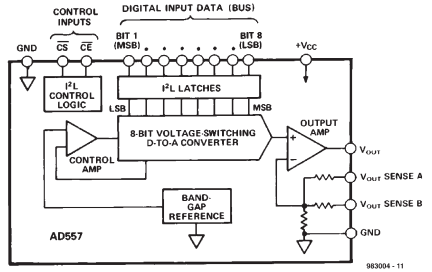
Complete 8-Bit DAC
Voltage Output: 0 V to 2.56 V
Internal Precision Band-Gap Reference
Single-Supply Operation: + 5 V (± 10%)
Full Microprocessor Interface
Fast: 1 µs Voltage Settling to ± ½ LSB
Low Power: 75 mW
No User Trims Required
Guaranteed Monotonic Over Temperature
All Errors Specified T_{MIN} to T_{MAX}
Small 16-Pin DIP or 20-Pin PLCC Package
Low Cost

General description

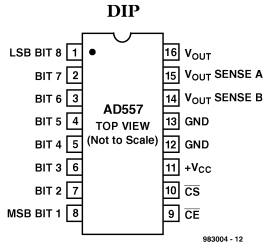
The AD557 DACPORT® is a complete voltage-output 8-bit digital-to-analogue converter, including output amplifier, full microprocessor interface and precision voltage reference on a single monolithic chip. No external components or trims are required to interface, with full accuracy, an 8-bit data bus to an analogue system.
The low cost and versatility of the AD557 DACPORT are the result of continued development in monolithic bipolar technologies.
The complete microprocessor interface and control logic is implemented with integrated injection logic (I^2L), an extremely dense and low-power logic structure that is process-compatible with linear bipolar fabrication. The internal precision voltage reference is the patented low-voltage band-gap circuit which permits full-accuracy performance on a single + 5 V power supply.
Thin-film silicon-chromium resistors provide the stability required for guaranteed monotonic operation over the entire operating temperature range, while laser-wafer trimming of these thin-film resistors permits absolute calibration at the factory to within ± 2.5 LSB; thus, no user-trims for gain or offset are required. A new circuit design provides voltage settling to ± ½ LSB for a full-scale step in 800 ns.
The AD557 is available in two package configurations. The AD557JN is packaged in a 16-pin plastic, 0.3"-wide DIP. For surface mount applications, the AD557JP is packaged in a 20-pin JEDEC standard PLCC. Both versions are specified over the operating temperature range of 0°C to + 70°C.

Application Example

PC-aided BJT transistor tester revisited, *Elektor Electronics* April 1998.



functional block diagram



pin configuration (DIP)

AD557

ELEKTOR ELECTRONICS

Integrated circuits
Special Applications

DATASHEET 4/98

Electrical Specifications

(@ T_A = + 25°C, V_{CC} = + 5 V unless otherwise noted)

Model		Min	Typ	Max	Units
RESOLUTION				8	Bits
RELATIVE ACCURACY[1]	0 to + 70°C		± 1/2	1	LSB
OUTPUT	Ranges		0 to + 2.56		V
	Current Source	+ 5			mA
	Sink		Internal Passive Pull-Down to Ground[2]		
OUTPUT SETTLING TIME[3]			0.8	1.5	µs
FULL-SCALE ACCURACY[4]	@ + 25°C		± 1.5	± 2.5	LSB
	T_{MIN} to T_{MAX}		± 2.5	± 4.0	LSB
ZERO ERROR	@ + 25°C			± 1	LSB
	T_{MIN} to T_{MAX}			± 3	LSB
MONOTONICITY[5]	T_{MIN} to T_{MAX}		Guaranteed		
DIGITAL INPUTS	T_{MIN} to T_{MAX} Input Current			± 100	µA
Data Inputs, Voltage	Bit On—Logic "1"	2.0			V
	Bit On—Logic "0"	0		0.8	V
Control Inputs, Voltage	On—Logic "1"	2.0			V
	On—Logic "0"	0		0.8	V
	Input Capacitance		4		pF
TIMING	t_W Strobe Pulse Width	225			ns
	T_{MIN} to T_{MAX}	300			
	t_{DH} Data Hold Time	10			
	T_{MIN} to T_{MAX}	10			
	t_{DS} Data Setup Time	225			
	T_{MIN} to T_{MAX}	300			
POWER SUPPLY	Operating Voltage Range (V_{CC})				
	2.56 Volt Range	+ 4.5		+ 5.5	V
	Current (I_{CC})		15	25	mA
	Rejection Ratio			0.03	%/%
POWER DISSIPATION, V_{CC} = 5 V			75	125	mW
OPERATING TEMPERATURE RANGE		0		+ 70	°C

[1] Relative Accuracy is defined as the deviation of the code transition points from the ideal transfer point on a straight line from the zero the the full scale of the device.
[2] Passive pull-down resistance is 2 kΩ.
[3] Settling time is specified for a positive-going full-scale step to ± ½ LSB. Negative-going steps to zero are slower, but can be improved with an external pull-down.
[4] The full-scale output voltage is 2.55 V and is guaranteed with a + 5 V supply.
[5] A monotonic converter has a maximum differential linearity error of ± 1 LSB.
Specifications subject to change without notice.

IC Tester

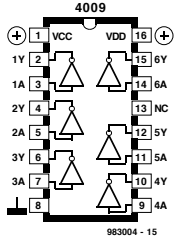
ELEKTOR ELECTRONICS

Elektor Electronics
March & April 1998

DATASHEET 4/98

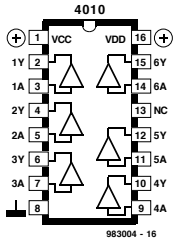
name 4009*
pins 16

pinorder	3	2	5	4	7	6	9	10	11	12	14	15	8	11	16	13
pindef	I	O	I	O	I	O	I	O	I	O	I	O	G	I	V	O
vect	1	0	1	0	1	0	1	0	1	0	1	0	0	1	1	X
vect	0	1	1	0	1	0	1	0	1	0	1	0	0	1	1	X
vect	1	0	0	1	1	0	1	0	1	0	1	0	0	1	1	X
vect	1	0	1	0	0	1	1	0	1	0	1	0	0	1	1	X
vect	1	0	1	0	1	0	0	1	1	0	1	0	0	1	1	X
vect	1	0	1	0	1	0	1	0	0	1	1	0	0	1	1	X
vect	1	0	1	0	1	0	1	0	1	0	0	1	0	1	1	X
vect	1	0	1	0	1	0	1	0	1	0	1	0	0	1	1	X
iccl																
vect	0	1	0	1	0	1	0	1	0	1	0	1	0	1	1	X
icch																



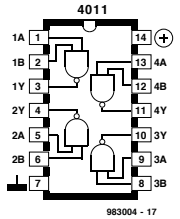
name 4010*
pins 16

pinorder	3	2	5	4	7	6	9	10	11	12	14	15	8	1	16	13
pindef	I	O	I	O	I	O	I	O	I	O	I	O	G	I	V	O
vect	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	X
vect	0	0	1	1	1	1	1	1	1	1	1	1	0	1	1	X
vect	1	1	0	0	1	1	1	1	1	1	1	1	0	1	1	X
vect	1	1	1	1	0	0	1	1	1	1	1	1	0	1	1	X
vect	1	1	1	1	1	1	0	0	1	1	1	1	0	1	1	X
vect	1	1	1	1	1	1	1	1	0	0	1	1	0	1	1	X
vect	1	1	1	1	1	1	1	1	1	1	0	0	0	1	1	X
vect	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	X
icch																
vect	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	X
iccl																



name 4011
pins 14

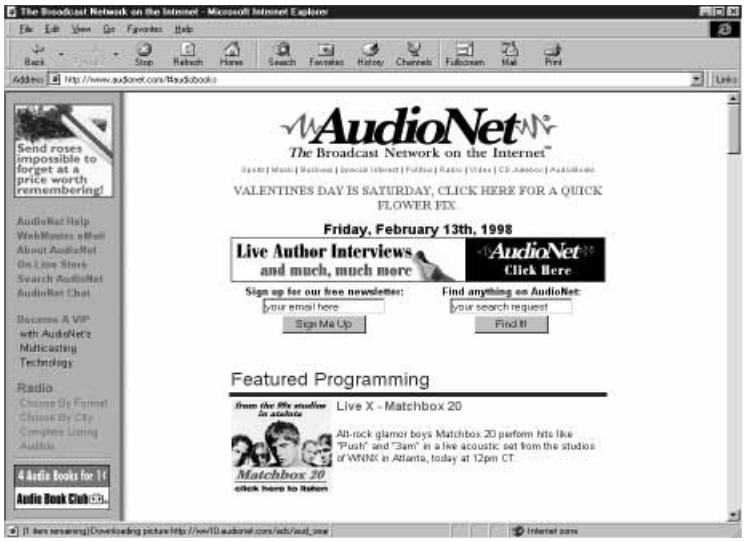
pinorder	1	2	3	6	5	4	13	12	11	8	9	10	7	14
pindef	I	I	O	I	I	O	I	I	O	I	I	O	G	V
vect	0	0	1	1	1	0	1	1	0	1	1	0	0	1
vect	0	1	1	1	1	0	1	1	0	1	1	0	0	1
vect	1	0	1	1	1	0	1	1	0	1	1	0	0	1
vect	1	1	0	0	0	1	1	1	0	1	1	0	0	1
vect	1	1	0	0	1	1	1	1	0	1	1	0	0	1
vect	1	1	0	1	0	1	1	1	0	1	1	0	0	1
vect	1	1	0	1	1	0	0	0	1	1	1	0	0	1
vect	1	1	0	1	1	0	0	1	1	1	1	0	0	1
vect	1	1	0	1	1	0	1	0	1	1	1	0	0	1
vect	1	1	0	1	1	0	1	1	0	0	0	1	0	1
vect	1	1	0	1	1	0	1	1	0	0	1	1	0	1
vect	1	1	0	1	1	0	1	1	0	1	0	1	0	1
vect	1	1	0	1	1	0	1	1	0	1	1	0	0	1
iccl														
vect	1	0	1	1	0	1	1	0	1	1	0	1	0	1
icch														



Free radio!

Radio stations on the Internet

The Radio Caroline's which some of you may fondly remember have been towed ashore and superseded by radio stations not using transmitters at all. The Internet has been discovered as a replacement for those good old radio waves. From now on, free radio will reach you by telephone line.



These days you do not need to have a general coverage receiver anymore to be able to listen to radio stations from distant shores and exotic regions. The modern equivalent of the short-wave receiver consists of an Internet browser, an Internet connection (via an Internet Service Provider) and the so-called RealAudio plug-in module.

An interesting web site demonstrating the many possibilities of webbed radio may be found at *http://www.audionet.com*.

Audionet calls itself 'The Broadcast Network on the Internet'. Its web site provides access to a wide variety of radio programmes and radio services. Using various menus you may choose from sports reports, news, lectures, shows and concerts.

That's not all, however. The web site also offers exclusive services to listeners, like the spoken book and compact disc (CD) listening. Pick a CD title from the stock list, and listen to it via the Internet. Because of the American principle "There Ain't No Such Thing As Free Lunch" (TANSTAFL), you will have to take for granted that each CD is preceded by a 'commercial'. Likewise you can pick a book title, sit back and listen to the book being read to you. The service called AudioBooks at *http://www.audionet.com/#audiobooks* has a number of titles available.

Scanner fans

The above mentioned web site also offers some very 'special' services. For example, AudioNet allows you to listen in on certain non-broadcast radio communication channels. For example, the site *http://www.policescanner.com* allows you to eavesdrop on the mobile radio network used by the police in Dallas, New York, Los Angeles or Plano.

Aeroplane spotters are probably more interested in the site *http://www.audionet.com/simufite* which provides a live feed to the Dallas/Fort Worth Traffic Control Tower. In this way, you can listen to communication between Traffic Control and pilots.

RealAudio

If you want to listen to these webbed Free Radio stations, you need to extend the functionality of your Netscape or Microsoft Internet explorer with the Real Audio plug-in. This program, RealPlayer 5, may be downloaded free of charge from *http://www.realaudio.com* after supplying your name and e-mail address.

(985029-1)