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## RLilumaiz

## BAR LEER LREERESHER

 LRE2E2DALALOUSIHON CARD
COLBLL ADC



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CONSUMER PRESS

## remote data logging on a budget

> This article describes a low-cost low-power analogue and digital data acquisition card that will interface directly to any personal computer having an RS232 port. The card offers an 8-channel, 8 -bit analogue-to-digital converter, 6 configurable logic lines and a 16-bit programmable counter.

This design is based around a PIC16C71 microcontroller (supplied ready-programmed) whose real-time software emulates a 9600 -baud UART (universal asynchronous receiver/ transmitter), and provides the necessary control of the various signal ports. The entire circuit operates off a single 5 -V supply which is provided by an on-board regulator. Battery powering is also possible with a total consumption of 10 mA .

## Circuit description

 The heart of the circuit shown in Figure 1 is a PIC type 16 C 71 from Arizona Microchip. This device is supplied ready-programmed through our Readers Services, or through a kit dealer. The on-chip PROM contains an amount of machine code developed by the author. The 16 C 71 has an onboard 8 -bit successive approximation analogue-to-digital converter (ADC). The A-D converter module features four analogue inputs multiplexed into one A-D converter, sample and hold, 8 -bit resolution and $\pm 1$ LSB accuracy. Conversion time is typically $30-\mu \mathrm{s}$ in-
cluding sampling time. The remainder of the circuit consists of four sections: analogue port, digital port, 16 -bit counter and RS232 interface.

In the present application, the operation of the analogue port is based on only two programmable lines on the PIC which are used as analogue inputs: RA0 and RA1 (pins 17 and 18 respectively). Two other programmable pins, RA2 and RA3 (pins 1 and 2 respectively), are internally programmed to function as digital outputs which control the channel selection of a dual 4 -to- 1 line CMOS analogue multiplexer type 74HCT4052 (IC3). In this way, eight analogue voltages (applied to the inputs of the '4052) are multiplexed and read in rapid succession by the ADC contained in the PIC. Remember, without the additional 4052 there would have been four channels only, read directly by the PIC. The ADC inputs have a voltage range of 0 to 5 V , and should be driven from a voltage source with an impedance of $10 \mathrm{k} \Omega$ or smaller to reduce conversion errors. All unused channels should be grounded to avoid static damage to the CMOS inputs.

The data acquisition card also has a digital port offering six TTL-compati-
inputs/outputs (D0-D5) and a clock input line (CLK) for event counter purline (CLK) for event counter pur-
poses. The six digital lines may be individually programmed as either inputs or outputs. When configured as an output ( $\mathrm{d}=0$, see Table 2), each line can deliver up to 20 mA for driving
LEDs, buzzers, etc. As inputs $(\mathrm{d}=1)$, can deliver up to 20 mA for driving
LEDs, buzzers, etc. As inputs ( $\mathrm{d}=1$ ), the lines have weak (approx. $250 \mu \mathrm{~A}$ ) pull-ups to 5-V.

The programmable 16 -bit counter may be initialised in many ways as seen from the control bit assignment seen from the control bit assignment
given in Table 1. Clock signals (TTLcompatible, i.e. having a swing be-
tween 0 and 5 V ) may be applied to compatible, i.e. having a swing be-
tween 0 and 5 V ) may be applied to the CLK pin, this has a direct connection to the RA4 pin of the PIC ( $\operatorname{pin} 3$ ). tion to the RA4 pin of the PIC (pin 3).
When used as a 16 -bit counter, the low byte should be read first (register ad-
dress 09 . . The high byte is stored at byte should be read first (register ad-
dress $09_{\mathrm{h}}$ ). The high byte is stored at this point until it is read (register address $0 A_{h}$ ). The 'auto-reset' function causes the counter to be reset after the
MAIN SPECIFICATI
digital lines, inputs or outputs

.8 analogue inputs, multiplexed, range 0.5 | - 8 -bit $A D C$ with 1 -bit resor 1 MHz |
| :--- |
| - counter input, max. 1 MH . 15 m | - simple RS232 connection on disk program an

- demo
low byte is read, allowing interval rather than accumulative counting (note: the high byte is stored before the reset).

The input prescaler divides the input clock before it reaches the 16 -bit counter, zero representing no divide while, say, 3 (binary 011) would give a divide by $2^{3}=8$. The external clock frequency must not exceed 1 MHz .

The RS232 interface is built around the familiar MAX232 level converter which has an on-chip $\pm 12-V$ voltage generator and line drivers to interface to the PIC. The real-time software that runs inside the PIC (using the RB6 and RB7 pins) emulates an asynchronous serial port which is initialised to the following format:

> Figure 1. Circuit diagram of the data acquisition card. All intelligence of the card is vested in a PIC16C71, IC4. The card works in conjunction with software running on a PC.


9600 baud, 1 stop bit, 8 data bits, no parity.

Note that no handshaking is required, allowing a simple three-wire connection to be made between the PC and the card, covering a distance of up to 15 m . Pins 4,6 and 8 are linked on the RS232 connector (K2) to ensure that the PC 'sees' a null-modem device and does not wait indefinitely for handshaking signals.

The power supply, finally, is run-of-the-mill being based on a 5 -volt regulator, IC2, and a voltage reversal protection diode, D1. The card is best powered from an inexpensive mains adaptor having an output voltage of
between 9 VDC and 12 VDC . Although the circuit itself draws a modest 15 mA , additional current may be required by an external circuit powered via pins $12 / 24(+5 \mathrm{~V})$ and $5 / 6 / 17 / 18$ (GND) of the analogue/digital I/O connector on the board. When

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | DO |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| File address |  | Clock source | Edge triggering | Auto Reset | Clock Prescaler value (input divider) |  |  |
| 1 | 1 | $\begin{gathered} 0=\text { int. } 1 \mu s \\ 1=\text { ext. clk } \end{gathered}$ | $\begin{aligned} & 0=\text { positive } \\ & 1=\text { negative } \end{aligned}$ | $\begin{aligned} & 0=y e s \\ & 1=n o \end{aligned}$ | $000=$ no clock prescaler $n n n=2^{n}$ prescaler |  |  |


| Address (hex) | Control | Function | Default |
| :---: | :---: | :---: | :---: |
| 00-07 | Read | 8 -bit ADC channels 0 to 7 | 0 |
| 08 | Read | 6-bit digital input port | 0 |
| 09 | Read | 16-bit counter lower byte | 0 |
| OA | Read | 16-bit counter upper byte | 0 |
| OB-3F | Read | Not implemented | 0 |
| Address (binary) |  |  |  |
| 01we uwn | Write | 6-bit digital port, output | $v=0$ |
| 10dd dddd | Write | 6-bit digital port, direction | $d=1$ |
| 11se rppp | Write | Counter function control | $s=1, e=1, r=1, p=0$ |
| $\boldsymbol{v}=$ logic. value (0/1), $\boldsymbol{d}=$ direction control, $\boldsymbol{s}=$ clock source <br> $\mathbf{e}=$ active clock edge, $\boldsymbol{r}=$ auto reset, $\boldsymbol{p}=$ prescaler value. |  |  |  |

powering external devices in this way, be sure to keep the power consumption below 85 mA so as not to exceed the maximum capacity of the 78L05.

## File allocation and

 CONTROL SOFTWAREAn overview of the card's registers and bit allocations is shown in Table 2. Don't worry if you do not understand the implications of a read/write operations from/to an invisible register bank straight away, there's a programming example and demo software to follow!

The card is seen as a slave unit, and will not respond until it is told to do so. It does not generate interrupts or any kind of report to the PC when a change in input data occurs, whether analogue or digital. Data transfer to/from the card has two forms:

Read file:
The PC sends a byte to the card which contains the address of the file register to be read (see Table 2). The card then returns a byte containing the value at that address.

## Write file:

The PC sends a byte to the card which contains the address of the file register to be written, as well as the value to be written (nothing is returned by the card).

```
#include <bios.h>
#include <conio.h>
#include <stdio.h>
#include <dos.h>
#define COM2 1
#define SETTINGS (0xEO | 0x03) | 0x00 | 0x00)
```

Figure 2. A small program written in C++ to demonstrate how ADC channel 0 may be read. Note that this is NOT the larger program mentioned in the text.
three DIL ICs in sockets. All electrolytic capacitors are radial types for vertical mounting on the board. Make sure you get the polarities right! The two sub-D connectors are both female types (sockets) with angled pins that allow direct fitting to the board. For your reference, the pin functions of the combined analogue/digital/counter socket, K3, are shown separately in Figure 4.
(960098)

```
int main(void)
{
    int byte, file =0;
    bioscom(0, SETTINGS, COM2); /* Set up RS232 */
    bioscom(1, file, COM2); /* Ask for 'file'*/
    byte = bioscom(2, 0, COM2); /* Read result */
    printf("ADCO = %2X ", byte); /* Print result */
}

Resistors:
\(\mathrm{R} 1=10 \mathrm{k} \Omega\)
\(R 2, R 3=22 \Omega\)
Capacitors:
\(\mathrm{C} 1, \mathrm{C} 2, \mathrm{C} 12, \mathrm{C} 13=100 \mathrm{nF}\)
\(\mathrm{C} 3, \mathrm{C} 9=10 \mu \mathrm{~F} 16 \mathrm{~V}\) radial
\(\mathrm{C} 4-\mathrm{C} 8=22 \mu \mathrm{~F} 25 \mathrm{~V}\) radial
\(\mathrm{C} 10, \mathrm{C} 11=100 \mathrm{pF}\)
\(\mathrm{C} 14, \mathrm{C} 15=22 \mathrm{pF}\)
Semiconductors:
D1 \(=1\) N4148
IC1 = MAX232
\(\mathrm{IC} 2=78 \mathrm{~L} 05\)
IC3 \(=4052\)
IC4 \(=\) PIC16C71-04/P ( \(0 / \mathrm{n} 966508\) 1)

\section*{Miscellaneous:}

K1 = 2-way PCB terminal block, pitch 5 mm
K2 \(=9\)-way sub-D socket, PCB mount, angled
K3 \(=25\)-way sub-D socket, PCB mount, angled
X1 \(=\) crystal 4 MHz
Demo program on disk: o/n 966019 -
Printed circuit board, o/n 960098-1 PCB, programmed PIC and disk: set o/n 960098-C

The get-you-going software example shown in Figure 2 was written in Turbo \(\mathrm{C}++\) to demonstrate a simple read of ADC channel zero. The value returned by the card represents an analogue voltage, where \(0=0 \mathrm{~V}\), and 255 \(=5 \mathrm{~V}\). This value may be used for further processing, logging, or displaying, in fact, anything you would like the PC to do with it. Actually, the card was initially designed as part of a virtual reality project to \(\log\) head tracking movement! Finally, it is assumed that serial port COM2 is used. If you want to another COM port, the program has to be modified accordingly.

A more powerful program called RSDEMO.C (also written in \(\mathrm{C}++\) ) is available on a disk with order code 966019-1 which also contains the executable program (RSDEMO.EXE). This program reads all eight analogue inputs, six digital inputs and the counter input, and presents a neatly arranged

overview of the respective values on your PC screen. It also prompts you to select your COM port (COM1 through COM4 may be used). All relevant command words necesary to initialise the RS232 port and convey data along this path are arranged via \(\mathrm{C}++\) commands that address the BIOS. The program also writes the necessary control words to the card registers to enable all of the above mentioned input values (or logic states) to be read. Readers interested in the programming aspects related to the data acquisition card will find this program indispensable as well as easy to implement in other software, so ordering the disk is well worth considering.

\section*{Construction} The circuit is very easy to build if you use the printed circuit board layout shown in Figure 3. It is recommended to fit the

Figure 4. Pinout of the combined analogue/digital/counter input/output socket. There's also a +5 V connection which may be loaded with 80 mA .

Figure 3. Track layout and component mounting plan of the single-sided printed circuit board designed for the data acquisition card (board available ready-made, see Readers Services page).


\section*{effects switch}

\section*{and unplugging}


When playing an electric guitar, you often have to use one or more effects units, since each and every kind of music played on the guitar requires its own special effects (tremolo; distortion; chorus; phaser; flanger; and so on). In practice, this often means that various units have to be plugged in and then out again to make place for others. With the switch unit described in this article all this becomes a thing of the past.

There is a plethora of effects units for electric guitars. Many of these are almost a must, because without them the required sound for a particular kind of music would be unattainable.

Although many guitar amplifiers have provision for selecting a few special (integral) effects, most of these have to be obtained from discrete add-on units connected in series with the cable linking the guitar to the amplifier. This works well, as does the operation, as long as there is only one effects unit in use. Most of such units have a foot pedal which enables the effect to be switched on or off. A different situation arises when there are several of such units in use and the effects have to be changed during a performance.

This usually means unplugging one unit and plugging another in. Quite a commotion, particularly since it is often accompanied by interfering side effects.

If you are one of those long-suffering guitarists confronted with such problems, the present switch unit may come as a godsend. It enables three effects units to be connected permanently to the amplifier and any one of them to be selected at will by a footswitch. Switching is effected by

> Figure 1. Principle of the circuit: squares 1 , 2 and 3 represent effects units.

a relay to ensure that the original signal is not affected by any kind of electronic circuit.

\section*{SIMPLICITY ITSELF}

Since the action of the switch unit may not immediately be clear from the circuit diagram, a simplified version of the diagram is shown in Figure 1 . In this, squares 1,2 and 3 represent the effects units (Eus). Switches \(S_{1}\) and \(S_{2}\) are double-pole change-over types. When \(S_{1}\) is in the upper position, EU1 is always in circuit, irrespective of the position of \(\mathrm{S}_{2}\). When \(\mathrm{S}_{1}\) is in the lower position, either EU2 or eU3 is in circuit, depending on the position of \(S_{2}\).

The reason that a simple 3-position switch is not used is that this would preclude the use of pedal switches. Also, this design has the advantage that change-over from one effect to another can be effected without overlap. If, for instance, in Figure 1 a change-over from EU1 to eu3 is desired, \(\mathrm{S}_{2}\) is first (inaudibly) operated, whereupon the wanted change is effected by pressing \(S_{1}\). If a 3-position switch were used, EU 2 would be actuated, however briefly.

\section*{CIRCUIT}

\section*{DESCRIPTION}

The circuit diagram of the switch unit is shown in Figure 2. The guitar is connected to socket \(\mathrm{K}_{1}\), while \(\mathrm{K}_{10}\) is the output socket. In between these two, three effects units may be inserted: eu1 between \(\mathrm{K}_{2}\) and \(\mathrm{K}_{9}\); EU2 between \(\mathrm{K}_{3}\) and \(\mathrm{K}_{8}\); and EU3 between \(\mathrm{K}_{4}\) and \(\mathrm{K}_{7}\). Changing over between these units is effected by relays \(\mathrm{Re}_{1}-\mathrm{Re}_{4}\), which are controlled by the switches connected to \(\mathrm{K}_{5}\) and \(\mathrm{K}_{6}\).

Relays \(\mathrm{Re}_{1}\) and \(\mathrm{Re}_{3}\), as well as \(\mathrm{Re}_{2}\) and \(\mathrm{Re}_{4}\), are connected in parallel. The first of these pairs changes over the input from the effects units, while the other changes over the output signal. To prevent any possibility of earth-loops, all relays have a twin set of change-over contacts, with which the signal line and the earth return are changed over simultaneously.

Change-over between EU1 and EU \(2 / 3\) is effected by the level at switching input \(\mathrm{K}_{5}\), and between EU2


> Figure 2. In practice, relays instead of switches are used. These may be operated by footswitches or digital signals.

and eu3 by the level at \(\mathrm{K}_{6}\).
The switching inputs are linked to simple stages consisting of a resistor, a zener diode and a field-effect transistor - FET. In the absence of a signal at the inputs, \(R_{1}-D_{5}\) and \(R_{2}-D_{6}\) ensure that \(T_{1}\) and \(T_{2}\) are on, so that the relays are energized, whereupon diode pairs \(D_{11}-\mathrm{D}_{13}\) and \(\mathrm{D}_{15}-\mathrm{D}_{17}\) light.

When \(\mathrm{K}_{5}\) and \(\mathrm{K}_{6}\) are short-circuited or linked to earth by a pedal switch or a low logic level, the fets are cut off, the relays are deactuated, and the earlier mentioned pairs of
diodes go out. Instead, diode pairs \(\mathrm{D}_{12}-\mathrm{D}_{14}\) and \(\mathrm{D}_{16}-\mathrm{D}_{18}\) light.

The switch unit may be powered by a standard mains adaptor capable of supplying a current of up to 300 mA (most adaptors can). The output of the adaptor need not be regulated. Diode \(\mathrm{D}_{19}\) prevents damage in case the adaptor is connected with incorrect polarity.

\section*{CONSTRUCTION}

The switch unit is best built on the printed-circuit board shown in Figure 3 (which is not available ready made). The board may be used in two different ways. The first is to leave it as it is, so that the unit can be mounted behind a 1-unit, 19 -in front panel. Many guitarists, however, may prefer to build the unit in a


> Figure 3. Printed-circuit board for the switch unit, which is not available ready made. When this is cut into two at the centre, the two halves can be formed into a 'sandwich'.
small, discrete enclosure. In that case, the board should be cut into two at the centre, and the two halves formed into a 'sandwich' with the aid of insulated spacers. This construction has the further advantage that connector pairs \(K_{1}-\mathrm{K}_{10}, \mathrm{~K}_{2}-\mathrm{K}_{9}\), \(\mathrm{K}_{3}-\mathrm{K}_{8}\), and \(\mathrm{K}_{4}-\mathrm{K}_{7}\) are positioned above one another, which is convenient from an operating point of view.

A close look at the board will show why the indicator diodes are in sets of two. They are positioned in line with the associated connector, which makes it easy to see at a glance, irrespective of which half of the board is viewed, which of the three effects units is connected in circuit. Diodes \(D_{11}\) and \(D_{13}\) indicate that eU 2 or EU3 is selected, and this is why these diodes are positioned in between \(K_{3}\) and \(K_{4}\), and \(K_{7}\) and \(K_{8}\), respectively.

Jack sockets \(K_{1}-K_{10}\) can be mounted directly on to the board; they may be mono or stereo versions. To prevent undesired hum, the break contact of \(K_{1}\) is connected so that the input is short-circuited when no jack is inserted into the socket.

The output of the mains adaptor \((12 \mathrm{~V} / 300 \mathrm{~mA})\) is applied to \(\mathrm{K}_{11}\), which may also be mounted directly on to the board. In fact, the board layout is such that the socket can be positioned for entry at the side or at the rear of the board.

\section*{Parts list}

Resistors:
\(\mathrm{R}_{1}, \mathrm{R}_{2}=10 \mathrm{k} \Omega\)
\(R_{3}-R_{6}=1 \mathrm{k} \Omega\)

\section*{Capacitors}
\(\mathrm{C}_{1}=220 \mu \mathrm{~F}, 25 \mathrm{~V}\), radial

\section*{Semiconductors:}
\(D_{1}-D_{4}, D_{7}-D_{10}=1 \mathrm{~N} 4148\)
\(\mathrm{D}_{5}, \mathrm{D}_{6}=\) zener diode 3.9 V
\(\mathrm{D}_{19}=1 \mathrm{~N} 4002\)
\(\mathrm{D}_{11}-\mathrm{D}_{18}=\) LED, 3 mm , red
\(T_{1}, T_{2}=B S 170\)

\section*{Miscellaneous}
\(\mathrm{K}_{1}-\mathrm{K}_{10}=6.5 \mathrm{~mm}\) phono jack for board mounting (mono or stereo)
\(\mathrm{K}_{11}=\) power jack for board mounting
\(R e_{1}-\mathrm{Re}_{4}=12 \mathrm{~V}\) relay with 2
change-over contacts
Mains adaptor \(12 \mathrm{~V}, 300 \mathrm{~mA}\).

Jump leads may be connected to points 1 and 2 on the board to enable the earth lines of the effects units to be commoned.

A photograph of the completed prototype board is shown in Figure 4.

CONNECTING UP
Although all connections have been



\section*{for 1.5 V AA/R6/HP7 dry batteries}

There has always been doubt about the claims that dry alkaline manganese batteries could be revived by charging, especially since manufacturers warn that attempts at doing so might result in the battery exploding. However, several units of which it is claimed that they can regenerate dry alkaline manganese batteries have now been on the market for well around years. Advertisements claim that these units can breathe new life into used dry batteries. We had our doubts about these claims and decided therefore to investigate them. The results are described in this article. The article is aimed at experimentalists rather than the average diy enthusiast.

Design by H . Bonekamp


\section*{Brief specification}

Application
Suitable for
Battery size
No. of batteries
Charging time
Initial charging current
Final charging current
Power supply
Special properties
Refreshing and charging unit
Dry alkaline manganese and NiCd batteries MN1500/AA/LR6/HP7
1-4
24 hours (dry battery); 8-10 hours (NiCd battery) 100 mA
80 mA
Mains adaptor, 12 V, 500 mA
Separate charging current setting for each holder; voltage monitor for each battery; automatic discontinuation of charging at low and high battery terminal voltage

It has been known for some time that, theoretically, partly discharged dry alkaline manganese batteries can be refreshed by charging with a small current. This current has to be small to avoid any risk of the battery exploding. With the appearance on the market of regenerating units for these batteries, the question was asked if such batteries could really be resuscitated, and, if so, to what extent.

Some years ago, we carried out extensive tests on special, rechargeable
dry alkaline manganese batteries that, together with appropriate chargers, had then come on to the market. These tests showed that those particular batteries could, indeed, be revived over a number of discharge/charge cycles. However, we were not able to do so over the number of cycles claimed by the producers. If these batteries had cost about the same as standard dry alkaline manganese batteries, there would have been a future in them. However, since their price was closer
to that of nickel metal hydride, NiMH , they were a non-starter.

When we were recently offered a refresher unit for standard dry alkaline manganese batteries, we were not too enthusiastic. And, indeed, initial findings were not encouraging. To start with, there were vast differences in the results with batteries from various manufacturers. Some could not be given any new life at all, whereas others could indeed be revitalized to some extent. It must be admitted that the exact state of charge of many of the tested batteries could not be ascertained. It is interesting, however, that even the really flat ones showed no tendency to explode or even leak.

It must also be admitted that the supplier of the 'charger' in the notes accompanying the unit had expressly stated that any batteries to be refreshed should

Figure 1. Typical discharge characteristics of a size MN1500 alkaline manganese battery (Duracell). not be flat, and that best results would be obtained of they were only partly discharged. 'When refreshing is undertaken after only a partial discharge, the battery can be regenerated many times. If, moreover, the battery is used in an application where the current drawn from it is small, it may be recharged up to 30 times'.

The initial tests were deemed to be inconclusive and we decided therefore to test dry alkaline manganese batteries (whose state of charge was known) from three different manufacturers: Mallory (Duracell), Philips, and Varta. Furthermore, it was decided to have the tests carried out by a proprietary regenerating unit and a refresher developed by ourselves (which is discussed later on in this article).

\section*{OBSERVATIONS AND}

\section*{RESULTS}

In the design of the refresher, inspiration was drawn from earlier investigations and experiences with the 'charger for alkaline manganese batteries' published in the July/August 1995 issue of this magazine. The refresher is, basically, a simple charger providing a constant charging current. In the tests, no noticeable difference was experienced between the con-stant-current method and the pulsed-charging-current method used in the 1995 charger. This is an interesting finding, because it was claimed that the positive findings obtained with special, proprietary chargers for use with dry alkaline manganese batteries were attributable to the pulsed-charging current. It should be noted that this is not the case with the proprietary charger used in the current tests.

Sets of four brand-new batteries from three different manufacturers

were used in the tests. Each test run concentrated on a set of four identical batteries. Two of these were partly discharged and then charged and partly discharged again several times. The other two were used as a control set to check the true available capacity. This was done by discharging them at a current, which, with a load consisting of a \(3.3 \Omega, 1 \mathrm{~W}\) resistor, is the maximum permissible discharge current of 1.5 V AA batteries: 0.5 A or, on average, 0.35 A .

Such a high discharge current has a detrimental effect on the number of cycles these batteries can be charged and discharged. The results are far better with normal levels of discharge current. The high-current discharge was aimed at giving the regeneration method a really tough test.

When the batteries were discharged at

Figure 2. Voltage vs time characteristics of a size MN1500 alkaline manganese battery (Duracell) discharged at high current (load \(=3.3 \Omega\) ) and recharged one to six times.
fairly small current levels, an alkaline manganese battery that lends itself well to refreshing, such as the Duracell types, had, after being refreshed for the first time, about the same capacity as a new battery. Thus, it would be possible to replace a partly discharged battery in a clock or small battery-operated radio receiver by a refreshed battery.

Now for the test with batteries discharged at high current levels. Figure 1 shows typical discharge characteristics of an MN1500/AA/HP7/LR6 dry alkaline manganese battery. These characteristics were obtained from Mallory's handbook of Duracell batteries.

The nominal capacity of these batteries is 1800 mAh when discharged at an ambient temperature of \(20^{\circ} \mathrm{C}\) to 0.8 V (from the nominal e.m.f. of 1.5 V ) through a \(50 \Omega\) load. The curves show clearly that the capacity drops fairly rapidly when the discharge current rises,

\section*{Duracell}



Figure 3. Similar characteristics to those in Figure 2 but pertaining to a Philips size LR6 alkaline manganese battery.
that is, when the load resistance is reduced. With a load of \(10 \Omega\), the capacity drops to 1550 mAh ; with \(5 \Omega\), to 1350 mAh ; and with \(3 \Omega\), to 1200 mAh .

The high-current discharge characteristics of a Duracell MN1500 battery that has been discharged and recharged a couple of times are shown in Figure 2. The battery was discharged via a \(3.3 \Omega\) resistor until its voltage (under load) had dropped to 0.8 V . The solid curve was obtained from a new battery. It took well over 4

Figure 4. Similar characteristics to those in Figure 2 but pertaining to a Varta size LR6 alkaline manganese battery. hours before this was discharged to a voltage of 0.8 via a \(3.3 \Omega\) load. It was then recharged and again discharged via the same load. It is
astonishing to note that it then took again over 4 hours for the battery to be discharged to a voltage of 0.8 V . Even size AA rechargeable NiCd or NiMH batteries do not offer that sort of performance.

Subsequent discharge/charge cycles reduced the capacity of the battery fairly rapidly, which is to be expected at such high discharge currents. In fact, after six cycles, the battery had all but lost its capacity. This rapid decrease is caused by the rise of the battery's internal resistance. With lower discharge currents, the fall in battery capacity was not so pronounced and more than six discharge/charge cycles were attainable.

Identical tests on AA size dry alkaline batteries from Philips and Varta showed a rather different picture, as seen in Figures 3 and 4. The Philips battery had a rather flatter initial characteristic (solid curve) than the Dura-

cell battery: it took over 6 hours for its terminal voltage to drop to \(0.8 \mathrm{~V}-\mathrm{a}\) very good performance, indeed. However, after it had been recharged, it had nowhere near the regenerated capacity of the Duracell battery - a mere 3 hours. This was found to be almost entirely because of its increased internal resistance. With lower load currents, the drop in capacity will, no doubt, be nowhere near as severe.

A similar picture emerged from the tests on the Varta battery. The terminal voltage of this shows a rather steeper fall during the first discharge than that of the other two batteries.

It should of course be borne in mind that even batteries of the same type from the same manufacturer may exhibit fairly large differences in performance, depending on the storage life and storage temperature.

The test results show clearly that the total capacity of dry alkaline manganese batteries, attainable over their life, can be increased to 3-5 times the nominal figure. Where high load currents are needed, these batteries do not perform anywhere near as well as (re-chargeable) NiCd batteries, and this is particularly true of refreshed dry batteries.

In our tests, the Duracell batteries stood out, since after the first discharge/charge cycle they had virtually regained their initial capacity.

Tests were also carried out with carbon zinc dry batteries, but these, without exception, could not be refreshed.

Finally, it may interest readers that the tests were carried out with a PCdriven Type HP34401A multimeter.

\section*{REFRESHER CIRCUIT}

The refresher, whose circuit is shown in Figure 6, is designed to receive four size MN1500/AA/LR6/HP7 batteries. It has protection against wrong polarity and a current and voltage limiter. So as to enable 1, 2, 3 or 4 batteries to be regenerated, these are not recharged in series, but independently of each other. The charging current lies between 80 mA for a completely refreshed battery and 100 mA for a battery discharged to a terminal voltage of 0.8 V . The maximum charging time is 24 hours.

The refresher (see block diagram in Figure 5) consists of a mains supply, a reference-voltage source (serving both limits of the terminal voltage), a voltage monitor, and a charging-current limiter derived from the voltage monitor. The last two stages are quadrupled to enable each battery being refreshed to have its own voltage monitor and discharge-current limiter.

For safety's sake, and also to keep costs down, the mains supply consists of a simple \(12 \mathrm{~V}, 500 \mathrm{~mA}\) mains adaptor. Protection against wrong polarity


Figure 5. Block diagram of the alkaline manganese battery refresher.
is afforded by diode \(\mathrm{D}_{1}\). The supply line for the refresher is set at 5 V by regulator \(\mathrm{IC}_{1}\), while that for the op amps and the reference voltage source is held at 8 V by regulator \(\mathrm{Ic}_{2}\). The presence of 5 V on the refresher supply line is indicated by \(\mathrm{D}_{2}\).

The reference-voltage source uses a potential divider, whose value may be varied with \(P_{1}\), to set the maximum

Figure 6. Circuit diagram of the alkaline manganese battery refresher.
charging voltage to 1.7 V and the minimum battery voltage to 0.85 V .

Charging current limiting is effected by a series resistor \(\left(\mathrm{R}_{11}, \mathrm{R}_{18}, \mathrm{R}_{25}\right.\), \(R_{32}\) ) in the lines to each battery being refreshed. Diodes \(D_{3}, D_{7}, D_{11}\), and \(D_{15}\) prevent the batteries being discharged via the charging circuit when the mains fails for whatever reason.

The voltage monitor consists of a two op amps operating as comparators. They liken the voltage at the relevant battery terminals with the 0.85 V and 1.7 V reference potentials. If the battery terminal voltage is below 0.85 V , the battery is discharged to too great an extent or it has been inserted wrongly. In either case, the output of the relevant op amp \(\left(\mathrm{IC}_{3 \mathrm{~b}}-\mathrm{IC}_{6 \mathrm{~b}}\right)\) goes high (about 8 V ), whereupon the tran-
sistor \(\left(\mathrm{T}_{1}-\mathrm{T}_{4}\right)\) in the charging-current path is cut off. The red Led \(\left(\mathrm{D}_{6}, \mathrm{D}_{10}\right.\), \(\mathrm{D}_{14}, \mathrm{D}_{18}\) ) then lights to warn of a too deep discharge or wrong connection.

The supply to the op amps is deliberately made higher than that to the transistors. This guarantees that the base becomes positive with respect to the emitter, which ensures that the ( \(p-n-p\) ) transistor is cut off.

When the battery terminal voltage reaches a level of 1.7 V , the other comparator \(\left(\mathrm{IC}_{3 \mathrm{a}}-\mathrm{IC}_{6 \mathrm{a}}\right)\) changes state, and again the relevant transistor is cut off. Charging of the relevant battery is then stopped. In that case the green LED ( \(\mathrm{D}_{5}, \mathrm{D}_{9}, \mathrm{D}_{13}, \mathrm{D}_{17}\) ) lights.

In our tests, the cut-off voltage of 1.7 V was attained with the Duracell batteries, but not the Varta batteries. In case of the latter, the reference voltage may be lowered to some degree. If the reference voltage is kept at 1.7 V , it is fairly easy to arrange for a timer switch to disconnect the mains to the refresher after 24 hours.

If the circuit is used to charge NiCd batteries, discontinuing the charging at 1.7 V is, of course, wrong, since that level is reached when the battery has been charged to only 80 per cent of its nominal capacity. In this case it is, therefore, necessary to stop charging after 8-10 hours, which again can be arranged by a suitable timer switch.




Figure 7. Printed-circuit board for the alkaline manganese battery refresher.

\section*{CONSTRUCTION}

The refresher is best built on the printed-circuit board shown in Figure 7 with the aid of the component layout and the parts list.

Start with laying the wire bridges near \(\mathrm{IC}_{2}\) and \(\mathrm{P}_{1}\).

Take good care to position the following components correctly on the board: \(\mathrm{IC}_{1}-\mathrm{IC}_{6}, \mathrm{D}_{1}-\mathrm{D}_{18}, \mathrm{C}_{1}\).

It is advisable to use sockets for op amps \(\mathrm{IC}_{3}-\mathrm{IC}_{6}\).

The wiring consists merely of the leads to the four battery holders.

\section*{INITIAL TESTS}

Before applying power to the circuit, carefully check the component layout, the soldering and the polarity of the
output of the mains adaptor: inner pin +ve , outer bush -ve.

Before inserting any batteries into the holders, connect the mains adaptor to the circuit, whereupon the green LEDS should light, not the red ones.

Connect a digital multimeter set to its 2 V d.c. range between test point E and earth and adjust \(\mathrm{P}_{1}\) for a reading of 1.7 V .

Test the correct functioning of the voltage monitor by short-circuiting one of the battery holders. The relevant green led should then go out and the associated red one light.

When all this is in order, insert a size AA/LR6/HP7P dry alkaline manganese battery, which has been discharged to some extent - not too deeply - into one of the holders Neither of the associated leds should light.

\section*{FAULT-FINDING}

If the refresher does not function as described, check the voltages at the annotated test points in Figure 6 with a digital multimeter ( \(10 \mathrm{M} \Omega\) input impedance). If the voltage levels differ greatly, the following list shows possible causes of the failure. Check the voltages in order of the test points: it is assumed that when a test point is being checked, the potentials at the previous ones are in order.

A The mains adaptor is faulty.
The polarity at the mains adaptor output is wrong.
The supply line is open-circuited.
If the voltage is present after \(D_{1}\) has
been removed, suspect a short-circuit in the diode or on the PCB.
B Diode \(D_{1}\) is connected with wrong polarity or is defect.
Capacitor \(\mathrm{C}_{1}\) is short-circuited.
C \(\mathrm{IC}_{1}\) is defect or wrongly connected or there is a short-circuit in the subsequent circuitry.
D \(\mathrm{IC}_{2}\) is defect or wrongly connected or there is a short-circuit in the subsequent circuitry.
E The setting of \(P_{1}\) is incorrect or there is a fault in the subsequent circuitry.


Beware!
Discharged batteries are generally not leakproof. The risk of leakage increases with storage time. while the likelihood of the baller. These factors for refreshing becomes forleshing to be done make it necessary for any batteries should not be untimely. Refreshing old bach and every dry dertaken. All manuarning that, owing to the dang not be charged. ballolosion, these batteries mower, that as long as Our tests have shown, how with low charging currefreshing is carried out wach an explosion. As rents, there is no dang has been no published acfar as we know, there has refresher units that have cident with any of the rerre past two years, other been on the market for the e a of old dy batteries.
than the occasional leake

F The value of \(R_{4}\) and/or \(R_{5}\) is wrong or there is a fault in the subsequent circuitry.
G When there is no battery in the relevant holder, the potential here should be 4.5 V and the green LED should light. When a battery with a terminal voltage of 1.5 V is inserted into the relevant holder, the green LED must go out and the potential at this test point should rise to about 4.8 V . If this is not so, remove the relevant ic from its socket, whereupon the green LED should light again. If there is still no voltage at the test point, the relevant transistor is defect.
H When there is no battery in the relevant holder, the potential here should be 4.5 V and the green LED should light. When a battery is inserted into the relevant holder, the potential should drop to \(1.5-1.7 \mathrm{~V}\). When it is lower than 1.7 V , neither relevant LeD should light; when it is \(\geq 1.7 \mathrm{~V}\), the green LED should light. If the relevant green LED does not go out, or the voltage at pin 2 of the op amp is 1.7 V , but that at the test point is lower than 1.7 V , it must be assumed that the IC is defect.
J When there is no battery in the holder, the potential should be about 6.5 V and the green LED should light. If this is not so, check the potential at pin 1 of the op amp. If this is around 7 V , the fault lies with the series resistor \(\left(\mathrm{R}_{8}, \mathrm{R}_{15}, \mathrm{R}_{22}\right.\), \(\mathrm{R}_{29}\) ) or the relevant green LED. When the voltage at pin 1 is low, that is, \(<1 \mathrm{~V}\), or that at pin 2 is 1.7 V and that at pin 3 is 4 V , it must be assumed that the IC is defect.
[960106-1]

Figure 8. The wiring of the refresher consists merely of the leads to the four battery holders.


\title{
satellite communications
}

\section*{everything gone cligitial}

Although some of you will have a choice of over 50 TV programmes brought to you via satellite, instead of five or so
less than two decades ago, television is still basically a passive medium. The arrival of DVB/MPEG-2, a unified digital transmission standard for TV, audio and more is sure to change all that, and soon you will be able to talk back to a satellite via your PC or multimedia set-top box. Are you ready to be launched into the digital era?


Without oversimplifying matters, the trend towards digital transmission of TV and radio programmes has two causes, both of which are in the realm of the programme suppliers and equipment manufacturers, and, to put it bluntly, mainly economical: (1) scrambling is easily implemented using Smartcards, easily leading up to Pay-per-View; and (2) transponders may be shared. The customer has little say in this, not even mentioning that practical tests have indicated that most viewers do not notice a difference in picture quality between digital and analogue programme material.

Because a typical satellite transponder can carry about ten times more digital channels than analogue channels, transponder rental costs may be
shared by broadcasters. Studies conducted by Eutelsat indicate that there will be some 350 satellites in geostationary orbit above Europe by the next millennium. With compression techniques like MPEG-2 resulting in about 10 channels per transponder, sufficient capacity will be available for a staggering 3,500 digital TV channels. Looking the vast amount of pulp-TV broadcast in these half analogue, half digital days, programme quality and quantity will be even more out of step by 2001. And, if you are bored with watching TV, why not switch to the Internet which will shortly come from the skies, too.

Although (enhanced) analogue TV still holds a strong position, and will co-exist for at least 10 years with digital TV, broadcasters, satellite operators
and equipment manufacturers are determined to 'push' a receiver/decoder for digital TV on to the market at an ultimate price of about \(£ 200\). Interestingly, some programme providers will subsidise this 'box' as they have contracts with manufacturing companies (for example Nethold, Canal Plus, but also the re-vamped BSkyB).
to emerge shortly for DVB-to-PPP (point-to-point protocol) and DVB-toDVD (digital video disk).

All of the above mentioned systems will use a common core of elements. These are the MPEG (Motion Pictures Experts Group) vision and sound coding and multiplexing, and ReedSolomon error correction. The re-


According to the April 1994 survey of the International Institute of Communications, about \(47 \%\) of Europe's homes will have a digital TV decoder by the year 2015 . However, looking at the current success of, say, PALPlus, there are fears that digital TV is a technology push rather than a response to a consumer demand.

All digital TV is supposed to be broadcast in the new panoramic 16:9 format, so how are we doing with compatible TV sets? An indication of the developments in this area is given by Figure 1. Obviously, a lot will have to be done by programme providers as well as retailers to increase sales of 16:9 sets. Whether or not this will be helped by PALPlus broadcasts is as yet unclear. Sports and feature films will be the work horses in this respect.

\section*{The Standard}

Today, DVB (Digital Video Broadcasting) has been accepted by all major European broadcasters as the standard for digital television, radio and data services over satellite, cable, microwaves and terrestrial transmissions. DVB specs have been laid down by the EBU (European Broadcasting Union) and the ETSI (European Telecommunication Standards Institute), and cover many sub-standards like DVB-S (satellites), DVB-C (cable services), DVB-SI (service information), DVB-TXT (teletext) and DVB-CS (cable distribution systems). The next step will be to agree on systems for digital broadcasting by terrestrial transmitters. Facts and full standards are available via the Internet from the EBU site at www.ebu.ch. Seamless links are sure

Figure 1. Sales of 16:9 format TV sets in Europe. (source: Vision 1250).
maining elements like modulation and channel coding need to be individually tailored to the transport media being used, which, after all, have different requirements as regards power and bandwidth. With the satellite and cable systems firmly defined, individual organisations are finalising their plans to produce and distribute DVB receivers. Early types of these receivers were shown at the recent International Broadcasting Conference (IBC) in Amsterdam.

\section*{INTERNET IN THE}

\section*{SKy: Teledesic}

Graig McCaw, entrepreneur and exowner of McCaw Cellular Communications (now renamed AT\&T Wireless Services) and Bill Gates, president of Microsoft Corp. have a wild plan, or a dream, as they say.

A constellation of \(84020-\mathrm{GHz}\) (Kaband) satellites, they hope, will gird the globe at low altitude (approx. 700 km , Figure 2), linking any two points on the world with the speed and capacity of fibre-optic cable. The name of this 9 -billion dollar venture, planned for launching by the year 2001 and originally conceived for wireless phones only, is Teledesic. Some people dismiss these plans as utter science fiction, arguing that the vast expansion of fibre networks will diminish the need for a satellite-based supplement. The people at Teledesic, of course, disagree, claiming that the project is never intended to carry all the world's high-speed traffic, and that there will be many locations that will never have fibre, but still need high-capacity data links (Fig-

\section*{Gcrambling systems - verview}

Some people consider everything that does not appear normally on a PAL TV as scrambled. This indicates a basic confusion between the terms 'TV standard' and 'encryption'. A D2MAC transmission, for example, does not produce a viewable picture on a regular PAL TV, although it may not be scrambled at all.

EBU (SIS, Sound-in-Sync): not a scrambling system, but a peculiar transmission format applied by the European Broadcasting Unit (EBU) for newsfeeds. Official decoders are not available but second source models are capable of stabilizing the picture and making the digital sound audible.
Decoder: no card; unclamped video input signal.

LuxCrypt: until recently, this system was used by RTL4, RTL5, SBS6 and Veronica (Holland Media Group/SBS6), who encrypt their transmissions for bookkeeping only, i.e., to have an audited number of viewers within the Benelux. In this way, suppliers of programme material can not bill the broadcasters for viewers outside the Benelux. Decoders used to be available at cost only. Direct-to-home viewers (expatriates and viewers not connected to the Benelux cable TV networks) produced an outcry when HMG changed to digital transmission (DVB/MPEG-2) at the beginning of September 1996.
Decoder: no card; unclamped video input signal.

Videocrypt: available in two standards which are mutually incompatible: VideoCrypt I and II. VideoCrypt II decoders are usually incorporated in receivers. Based on cut-and-rotate of picture lines. Decoder: Smartcard; unclamped video input signal.

D2MAC: not a scrambling system in itself, but a quasi-digital transmission standard. EuroCrypt scrambling is an option.
Decoder: Smartcard; flat baseband input signal.

EuroCrypt: scrambling system associated with D/D2MAC. Two basic versions: EuroCrypt M and S.
Decoder: usually contained in receiver; Smartcard; flat baseband input signal.

Syster: mainly used on German, Spanish and Italian stations.
Decoder: rental or available in combination with subscription only; Smartcard; unclamped video input signal.

Obsolete analogue scrambling systems (video only): SatPac (FilmNet), SAVE (BBC World Service), Discret 1 (Canal Plus), Irdeto.


Figure 2. Orbiting scheme for the 840 LEOs (low-earth orbiting satellites) in the Teledesic plan proposed by Microsoft and AT\&T Wireless services.
ure 3). Examples include remote villages, farms, and the all of today's underdeveloped countries.

Apart from the problem of finding investors for these ultra-ambitious plans, Teledesic might have a problem building all those satellites and launch them without breaking the bank. The target is about \(\$ 5.5\) million per satellite, way under the \(\$ 100\) million or so of today's big communications satellites and about half of what Motorola intend to spend on the satellites in their Iridium venture (a partly competitive satellite-based global communication system). Software for the earth stations will not be a problem as it will probably be developed by a team of programmers at Microsoft. Top-of-the-bill (pun intended) of the Teledesic features is its \(1.2 \mathrm{~Gb} / \mathrm{s}\) Gigalink to fixed sites.

\section*{Back to earth:}

\section*{Telenor and Astra 1H} Since 1995, Eutelsat as well as other service providers in Europe and North America have been developing digital platforms for multimedia services carried by satellite, as well as data broadcasting (datacasting). In Europe, these initiatives are based on DVB and MPEG-2 technology. Simply by applying (virtually) the same technology as the one used for digital TV and radio, it becomes possible to raise the speed of multimedia services to end users to, for example, \(2 \mathrm{Mbit} / \mathrm{s}\) per session for an Internet connection, or \(40 \mathrm{MBit} / \mathrm{s}\) for downloading huge files to a large
number of customers. Mind you, these initiatives are aimed at business users. In practice, DVB is easily used for a PPP (point-to-point protocol). As with ActiveMovie in your web browser, it's the perfect link if your connection is fast enough.

The risk of serious bandwidth shortage caused by millions of Internet users is recognized worldwide. Cable TV operators, in a smart move to steal Internet users from telephone companies, are working hard to come up with cable modems. Phone companies are fighting back with much reduced ISDN subscription prices. Neither the cable TV system nor the ISDN network does, however, offer the vast geographical scale of satellites carrying data, simply because a satellite can, in principle, be received everywhere.

Although Eutelsat have helped to pave the way for digital broadcasting, others have put multimedia broadcasting in practice. Telenor's 'Multimedia Channel' will be beamed down early next year, not by an Eutelsat satellite, but by Thor, the ex-BSkyB Marco Polo satellite, now pulled to the Scandinavian geostationary position of \(1^{\circ}\) West. The Multimedia Channel will offer, among other services: a business multimedia newspaper, video broadcasting, an infochannel, interactive business TV, turbo internet and a game channel. The Multimedia Channel is available for:
\(\rightleftharpoons\) PCs, as a complete add-on card with turbo-internet capability, and containing a complete satellite receiver for direct viewing on a TV set;
\(\Delta\) or TV, which involves a complete set-top box that combines traditional TV with Turbo Internet and other multimedia applications transferred at a rate of up to 48 MByte/s.

Although Telenor's initiative is aimed at the Scandinavian world, the technology is of interest because it opens a market for satellite receivers on a PC insertion card! All in all, the new service appears to be initially designed for teleshopping, large warehouses being able to provide clients with product information that reaches them via satellite. In this system, telephone lines are still used for the low-bandwidth link from the end user to the server. Some cable-TV modems will also use this split-line system: high bandwidth over the cable TV network (server-to- user); low bandwidth over the telephone line (user-to-server).

Société Européenne des Satellites (SES) Luxembourg, owners and operators of the well-known Astra satellites, follow in the footsteps of Telenor by mid-1998 when their Astra 1H, the 'multimedia satellite', will be operational as the eighth satellite positioned at \(19.2^{\circ}\) East. As shown in Figure 4, many of the intentions unveiled recently by SES are identical with those launched by Telenor as described above. There are, however, two marked differences. First is the use of an uplink frequency (in other words, a wireless link) to convey information from the user to the satellite, and from there, to the ground station. Second is the use of two dedicated Ka band (2030 GHz ) transponders for all data traf-


Figure 3. If all goes according to plan, the 840 LEOs in Teledesic's constellation will carry rivers of digital information as they orbit the globe from pole to pole, continuously transmitting and receiving in the Ka band (20-30 GHz). Phone companies will use the birds to extend their wired and cellular networks. People everywhere would thus be able to surf the Internet, share computer files, and make videophone calls with the blinding speed of fibre optics. (source: Tony Mikolajczyk for Fortune magazine).


\section*{Dhe chip for all descramblers!}

The latest set-top box chip set marketed by LSI Logic is able to handle all currently used conditional access systems for satellite TV. The chip set, called Integra, has been designed by News Datacom. Because it can be switched on by downloading code over the air, a single settop decoder box based on Integra would be capable of decoding, say, BSkyB as well as Canal Plus (provided, of course, you turn the dish). The next generation of Integra is said to add MPEG decoders and a controller for DVD (digital video disc). Major players in the DVD field such as Sony are already using the Integra chip set.
fic (up and down!). This will create a market for a totally new type of LNB having a (lowpower) transmit capability. Although technical details are not yet available, it is reasonable to expect that this LNB will be incorporated as a Ka-band extension into existing Ku-band \(\quad(12-\mathrm{GHz})\) types. Interestingly, the 1 H satellite will also contain 28 Ku -band transponders.

Rivals in Space: Astra and Hotbird Another series of Astra satellites, of


Figure 5. Hotbird 2 satellite under construction. Lets' hope it goes into orbit with the new Ariane 5 rocket shortly (photograph courtesy Eutelsat).

Figure 4. The Astra 1H satellite, planned for deployment in 1998, will add a totally new aspect to multimedia computing: a direct-from-home (DFH) uplink to the satellite, using a transmitting LNB which operates in the Ka band (2030 GHz ). (source: SES Luxembourg).
which the first is to be deployed by the autumn of 1997, will be positioned at \(28.2^{\circ}\) East. The Astra 2A will be a Hughes Space HS 601 HP providing 28 Ku -band transponders ( 32 for the first five years) with an output of 100 watts each. Next comes the 2 B spacecraft to be built by Matra Marconi Space, having roughly the same specs as the 2 A . The first customer to commit to the new Astra position of \(28.2^{\circ}\) east is UK broadcaster BSkyB, who have leased no fewer than 14 transponders on the Astra 2A for their digital programme 'bouquet' targeted at the UK and Eire by the autumn of 1997.

Meanwhile, Eutelsat's Hotbird 2 is said to be a full sell-out. This satellite (shown under construction in Figure 5) will be launched by mid-November, and is fully booked with all 20 transponders leased with 12 -year contracts. Hotbird 2 will be the second
of five satellites co-positioned at \(13^{\circ}\) East (Figure 6). By early 1998, Eutelsat hope to have 98 transponders operational from this slot, although this may be optimistic in view of the possibilities of launch failures! In the fourth quarter of 1995, some 55.4 million households were watching channels from the Hot Bird position, mainly, of course, via cable TV networks. Eutelsat is in cyberspace, too, at www.eutelsat.org. Have a look at their site!
(960021)

Figure 6. Artist's impression of Eutelsat's Hotbird 1 and 2 satellites co-positioned in geostationary orbit at 13 degrees East. Hotbird 2 in particular will carry a vast number of digital TV programmes, each of the 20 transponders being able to beam down up to ten programmes. (photograph courtesy Eutelsat)


\section*{remote control}

\section*{with visible (red) light}


> The article describes a remote control (send/receive) system that does not use infra-red light, but visible light. It is particularly suitable for use with a door opener or alarm system. The use of visible light is not only original, but has other advantages as well.

Based on an idea from W. Zeiller

Current remote control systems either use radio waves or infra-red light. The first is used particularly where long distances have to be spanned and/or where obstacles, such as walls or closed doors, have to be negotiated. These systems are generally complex and expensive. Infra-red (IR) light is by far the most common system in use in domestic premises and offices. Its use is restricted to line of sight, but it can span distance of a couple of meters (10 feet or so). An advantage of IR systems is that the likelihood of their causing spurious radiations and other inter-ference is very small indeed, which precludes having to take measures against these phenomena.

The system described may be seen as a variation on an IR system: it uses visible (red) light as the transmission medium. This has the disadvantage that ambient light has some effect on the transmission and consequently the distance spanned is rather shorter.

On the other hand, red light has two important advantages. In the first place, you can see what is happening: particularly in dark or semi-dark spaces the red beam is clearly visible (as a secondary benefit, it gives an indication of the state of the battery).

The second advantage is that the controller of the system can be used for purposes other than remote control, for example as a keyhole finder or map reader in a car. In this context, it
is worth noting that the LED used in the controller is much more robust than the bulb in a small torch.

\section*{DESIGN}

The system consists of a controller and a receiver. The controller is about the same size as a cigarette lighter and is powered by a small battery. It is, as it were, the optical key of a door opener or alarm system, which can easily be carried about.

The receiver is rather larger, but still fairly compact. It is powered by a standard mains voltage adaptor. At its input is a phototransistor and at its output a relay with which the various functions can be carried out.

The signal between controller and receiver consists of red light pulsing at a rate of 3.2 kHz . The controller generates this pulse train with the aid of an LED. Although the pulse rate is high for our eyes, so that it seems to us as if the LED lights continuously, the phototransistor in the receiver detects the discrete pulses and translates them into a switching command for the output relay. The design of the receiver makes it insensitive to daylight or artificial light.

\section*{CONTROLLER}

The diagram of the controller is shown at the bottom left of Figure 1. It is based on the well-known Type 555 timer (here in CMOS version): \(\mathrm{IC}_{3}\).

The IC is arranged in its standard application as an astable multivibrator (AMV). It generates a signal at a frequency of 3.2 kHz , which is determined by \(R_{12}, R_{13}\) and \(C_{13}\). To ensure a square-wave signal (duty factor 50 per cent) at the output, \(\mathrm{R}_{13}\) is bridged by a Schottky diode, \(\mathrm{D}_{4}\). It would have been possible to lower the value of \(R_{12}\), but this would have increased the current drain and thus shortened the life of the battery. A square-wave rather than a rectangular output was chosen, because this yields the highest fundamental frequency and gives the highest possible signal level at the receiver.

The square-wave output signal is used directly to drive an LED. Since the highest possible light intensity is required, this diode is a super luminosity type ( 3 cd at 20 mA ).

Switch \(\mathrm{S}_{1}\) is the send button: it is the only operating control in the system. The actuated controller draws a current of about 10 mA , which is provided by a 3 V lithium manganese battery. Since the operating signal is invariably of short duration, the battery will have a useful life of several years.

\section*{RECEIVER}

Two ICs fulfil all receiver functions, which makes construction a very simple affair indeed.

Some constructors may have expected that the well-known tone decoder IC Type NE567 would have been used. However, it was found that the FSK demodulator/tone-decoder Type XR2211 from Exar, \(\mathrm{IC}_{1}\), although slightly more expensive, has several real advantages.

Where the use of an external voltage regulator is vital in case of the NR567, this is not required with the XR2211 since it has a regulator on board.

Moreover, the input of the NE567 is not very sensitive, so that a preamplifier is indispensable. Again, this is not required with the XR2211.

Even more important is that the XR2211 has a wide reception band and yet offers good selectivity. In contrast, the NE567 has a tendency to react to signals in adjacent bands.

Finally, the quiescent current drawn by the XR2211 is only half that of the NE567.

These four points make it clear why the XR2211 was preferred over the NE567.

The design of the receiver/decoder circuit based on \(\mathrm{IC}_{1}\) follows the standard application preference of the manufacturers. The tone detector has a sensitivity of 2 mV .

Capacitor \(C_{2}\) in conjunction with the input impedance of the \(I C\), forms a high-pass section with a cut-off frequency of 170 Hz . This filter ensures

adequate suppression of any interfering 100 Hz components. The centre frequency is determined by \(\mathrm{R}_{7}, \mathrm{P}_{1}\) and \(\mathrm{C}_{4}\); in the prototype it was set at 3.2 kHz . Preset \(\mathrm{P}_{1}\) allows a range of 118 Hz to be scanned. Network \(\mathrm{R}_{5}-\mathrm{C}_{3}\) forms a lock-detect filter, whose time constant is 0.5 s .

The light-sensitive sensor could have been formed simply by a phototransistor \(\left(\mathrm{T}_{3}\right)\) and a resistor. However, in the prototype it soon became clear that this combination was far too easily influenced by ambient light. A particular nuisance was created by neon lights whose 100 Hz interference was not suppressed by the input filter \(\left(C_{2}\right)\) either.

The solution to this problem is the collector load formed by \(T_{1}\) and \(T_{2}\). This network acts as a source of direct voltage and very-low-frequency signals. However, at higher frequencies, the feedback loop created by \(R_{1}\) and \(R_{2}\) is negated by \(C_{1}\), so that the circuit behaves like a high impedance. This means that at the transfer frequency \((3.2 \mathrm{kHz})\) the phototransistor works into a high impedance and has a consequently high amplification. The result is that the 3.2 kHz light pulses are magnified, while any interfering lowfrequency signals have little or no effect.

\section*{Figure 1. Circuit dia-} gram of the controller (within dashed lines at the bottom left) and receiver. When \(S_{1}\) is pressed, the led in the controller sends a stream of red light pulses at a rate of 3.2 kHz to phototransistor \(T_{3}\).

Since the input impedance of \(\mathrm{IC}_{1}\) is only about \(20 \mathrm{k} \Omega\), it will be clear from the foregoing that the collector of \(\mathrm{T}_{3}\) cannot simply be connected to the input of the demodulator. The two are, therefore, linked via a buffer: emitter follower \(\mathrm{T}_{4}\).

The circuit based on \(\mathrm{IC}_{2}\) is a retriggerable monostable multivibrator (MMV), which ensures that relay \(\mathrm{Re}_{1}\) is always actuated for a well-defined period of time. With component values as specified in the diagram, this time can be set with \(\mathrm{P}_{2}\) between 0.1 s and 10 s . If a slightly longer time is felt to be desirable, the value of \(\mathrm{R}_{9}\) and/or \(\mathrm{C}_{8}\) may be increased slightly.

The terminals of connector \(\mathrm{K}_{1}\) are in series with the load to be controlled (door opener, lamp, or ...).

\section*{CONSTRUCTION}

The printed-circuit boards for the controller and receiver are produced as one and must, therefore, be separated before any construction work can be undertaken. The combined board is shown in Figure 2.

Populating the receiver board is very simple: following the layout in Figure 2 should prevent any mistakes. The specified relay fits on the board without any difficulty; other types may require the board to be modified.

The phototransistor must be

mounted in such a way that when the board is fitted in an enclosure, it can readily receive light falling on to the aperture in the lid of the enclosure.

The board is intended to be fitted in a Model E430BB enclosure from Bopla, but other suitable cases may be used, of course.

A photograph of the completed prototype board is shown in Figure 3.

The controller is intended to be fitted in a Model KM14 key fob case from Uni Box. This is a flat case about the size of a cigarette lighter-see Figure 4.

It is powered by a 3 V lithium manganese battery (button type \(20 \times 1.6 \mathrm{~mm}\) ). This type of battery fits exactly into the aperture in the board so that its + ve edge makes good contact with the copper that functions as the positive terminal. The -ve case of the battery protrudes just a little from the component side. Fold a strip of thin copper or brass over the battery and the edges of the board as shown in Figure 4 and solder it to the copper at the underside of the board. When the case is closed, the battery is automatically pushed into position.

The controller case is provided with a push-button located exactly over switch \(\mathrm{S}_{1}\).

The LED is fitted in the recess on the board so that its light beam is emitted through the aperture in the front of the case as shown in Figure 4.

Figure 2. The printedcircuit boards for the controller and receiver are produced as one and they should, therefore, be cut apart before any construction work is done.

\section*{The XR2211}

The Type XR2211 IC from Exar is designed especially for use in data communication systems. Typical applications are FSK demodulation, data synchronization, tone decoding, FM detection and carrier detection. It can operate from supply lines between 4.5 V and 20 V . Its frequency range extends from 0.01 Hz to 300 kHz .

The IC has an internal phase-locked loop (PLL), which consists of an input amplifier, an analogue multiplier that functions as a phase detector, and an accurate voltage-controlled oscillator (VCO). The input amplifier functions also as a limiter: it ensures that all input signals above a level of 2 mV r.m.s. are raised to a constant level.

The phase detector functions as a sort of digital XOR gate whose output contains the sum and difference signals resulting from the multiplying of the input signal and VCO output. The sum signal is filtered out, while the difference signal (d.c.) is used to control the VCO.


The VCO is strictly speaking not voltage-controlled but current-controlled. The nominal current at \(f_{0}\) is set by a resistance in the phase detector.

Apart from the PLL, the IC has several other functional sections. One of these is an FSK comparator which monitors whether the VCO frequency is at, above, or below, \(t_{o}\). Others are a phase-quadrature detector and a lock-detect detector which serve to detect and indicate whether the PLL is locked.

The IC also has an internal reference voltage source to preclude its operation being affected by supply line variations.

\section*{Parts list}

Resistors:
\(R_{1}=220 \mathrm{k} \Omega\)
\(\mathrm{R}_{2}=1 \mathrm{M} \Omega\)
\(R_{3}=100 \Omega\)
\(\mathrm{R}_{4}=47 \mathrm{k} \Omega\)
\(R_{5}, R_{6}=470 \mathrm{k} \Omega\)
\(R_{7}=15 \mathrm{k} \Omega\)
\(\mathrm{R}_{8}, \mathrm{R}_{9}=10 \mathrm{k} \Omega\)
\(\mathrm{R}_{10}=2.7 \mathrm{k} \Omega\)
\(R_{11}=10 \Omega\)
\(\mathrm{R}_{12}, \mathrm{R}_{13}=4.7 \mathrm{k} \Omega\)
\(\mathrm{P}_{1}=5 \mathrm{k} \Omega\) preset
\(P_{2}=1 \mathrm{M} \Omega\) preset
Capacitors:
\(\mathrm{C}_{1}=3.9 \mathrm{nF}^{\star}\)
\(\mathrm{C}_{2}, \mathrm{C}_{13}=47 \mathrm{nF}^{\star}\)
\(\mathrm{C}_{3}=1 \mu \mathrm{~F}, 16 \mathrm{~V}\), radial
\(\mathrm{C}_{4}=18 \mathrm{nF}^{\star}\), pitch 5 mm
\(\mathrm{C}_{5}, \mathrm{C}_{7}, \mathrm{C}_{12}=100 \mathrm{nF}{ }^{*}\)
\(\mathrm{C}_{6}=4.7 \mathrm{nF}{ }^{*}\)
\(\mathrm{C}_{8}, \mathrm{C}_{14}=10 \mu \mathrm{~F}, 16 \mathrm{~V}\), radial
\(\mathrm{C}_{9}, \mathrm{C}_{10}=10 \mathrm{nF}\), high stability
\(\mathrm{C}_{11}=220 \mu \mathrm{~F}, 16 \mathrm{~V}\)
* metallized polyester

Semiconductors:
\(D_{1}, D_{2}=1 \mathrm{~N} 4001\)
\(D_{3}=\) LED, red (GL5UR3K1 from
Sharp)
(3 cd at 20 mA )
\(\mathrm{D}_{4}=\) BAT85
\(\mathrm{T}_{1}, \mathrm{~T}_{2}=\mathrm{BC} 557 \mathrm{~B}\)
\(T_{3}=\) BPW40 (Telefunken)
\(T_{4}=\) BC547
\(\mathrm{T}_{5}=\mathrm{BC} 337\)
Integrated circuits:
\(\mathrm{IC}_{1}=\mathrm{XR} 2211 \mathrm{CP}\) (Exar)
\(\mathrm{IC}_{2}, \mathrm{IC}_{3}=\) TLC555CP, CMOS

\section*{Miscellaneous:}
\(K_{1}=2\)-way terminal block,
pitch 7.5 mm
\(S_{1}=\) push-button switch for board mounting, Alps Type SKHCAB
\(\mathrm{Re}_{1}=\) relay Type V23127-A0002A201 (Siemens - available from ElectroValue)
\(\mathrm{Bt}_{1}=3 \mathrm{~V}\) lithium manganese battery, button type \(20 \times 1.6 \mathrm{~mm}\)
Strip of copper or brass - see text Enclosures: controller - UniBox KM14 ( \(12 \times 35 \times 70 \mathrm{~mm}\) ) receiver - Bopla Type E430BB, available from Phoenix Mecano ( \(120 \times 65 \times 40 \mathrm{~mm}\) )
PCB Order No. 960068 (see Readers' Services towards the end of this issue)

Adjacent to switch \(\mathrm{S}_{1}\) is a hole through which the locking screw for shutting the case fits.

It should be noted that on the component side of the board the flat surfaces of the LED (that is, the cathode) and phototransistor (that is, the collector) are marked by a dash.

\section*{FINALLY}

When the boards have been completed and checked thoroughly, the controller and receiver should be tested functionally.

> Figure 3. The completed prototype receiver board fitted in a Bopla case. The phototransistor must be exposed to the outside world via an aperture in the lid of the case.

Connect a 9-12 V mains adaptor to the receiver. This unit draws a current of not more than 160 mA so that virtually any good mains adaptor will do. Using a digital multimeter, check at the relevant points whether the voltages there correspond with those indicated on the circuit diagram. Differences of about 10 per cent may be tolerated. In case of larger differences, it is advisable to check the board thoroughly again.

As far as the controller is concerned, once the case is closed and the battery is seated correctly, pressing \(\mathrm{S}_{1}\) should result in the LED lighting brightly. If it does not, check the board thoroughly again. Pay particular attention to \(\mathrm{R}_{12}, \mathrm{R}_{13}\), and \(\mathrm{C}_{13}\).

All that remains to be done is the setting of the receiver range. This is simply done by establishing the two positions of the wiper of \(\mathrm{P}_{1}\) at which the relay just still operates when the switch on the controller is pressed. Set the wiper midway between these two positions. As long as the ambient light is not too bright, the distance spanned by the control system is about 5 m (16 feet). In case of a bright ambience, the distance is only about 2 m (6-7 feet), which is still ample for a door opener.
[960068]


Figure 4. The completed prototype controller board fitted in the specified key fob case. The -ve supply on the board is linked to the -ve terminal of the battery by a strip of copper folded over the edges of the board and soldered to the copper at the track side of the board.



\section*{HANDS-ON ELECTRONICS}

\section*{a short course in circuit simulation}


Last month's article gave a quick preview of SPICE. This is followed this month's by a close look at a common-emitter amplifier and, based on this, an illustration of ways of putting data into a SPICE simulation and getting data from it.

\section*{COMMON-EMITTER AMPLIFIER}

The common-emitter amplifier in Figure 8 was designed to operate on 9 V with a quiescent output voltage of about 4.5 V and to pass signals in the audio range ( \(30 \mathrm{~Hz}-20 \mathrm{kHz}\) ). Select the BJT transistor first, clicking on Component \(\rightarrow\) Analog Primitives \(\rightarrow\) Active Devices \(\rightarrow\) NPN. Before placing the transistor in the centre of the screen, use the right mouse button to turn it the right way up. When it is placed, the Component window asks for its model. Select 2N2222A from the panel on the right. Check the Display Box. The remainder of the circuit is assembled as described last month; for V1, value \(=9\); for V2, value \(=\sin (00.02\)

50000 ). This is a 500 Hz sine wave, amplitude 0.02 V , offset 0 V , zero decay, zero phase delay. To see the specification of the transistor, click on the small button at the bottom right of the screen. This displays the Text Screen on which is the model definition for the transistor:
.MODEL 2 N2222A NPN ( \(\mathrm{IS}=8.57646 \mathrm{P}\) \(\mathrm{BF}=168.002 \ldots\) )
2 N2222A is the model name, NPN is its type, and the brackets contain a list of its parameters. The first two indicate that the saturation current \(I_{S}\) is 8.57646 pA , and the forward gain \(\beta_{\mathrm{F}}\) is 168.002 . There are 21 other parameters, all of which are used, along with state variables (relevant network voltages and currents), in a set of equations by
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow[t]{5}{*}{Node} & \multicolumn{2}{|l|}{Voltage} & Node & Voltage & Node & Voltage & Node & Voltage \\
\hline & 1 & 9 & 92 & 24.3 & 3 & 1.06 & 4 & 1.66 \\
\hline & 5 & 0 & 06 & 60 & & & & \\
\hline & \multicolumn{8}{|c|}{Bipolar Junction Transistors} \\
\hline & \multicolumn{8}{|c|}{Q1} \\
\hline IB & \multicolumn{8}{|c|}{1.283-005} \\
\hline IC & \multicolumn{8}{|c|}{\(1.04 \mathrm{e}-003\)} \\
\hline vBE & \multicolumn{8}{|c|}{\(6.07 \mathrm{e}-001\)} \\
\hline VBC & \multicolumn{8}{|c|}{-2.64e+000} \\
\hline VCE & \multicolumn{8}{|c|}{\(3.25 \mathrm{e}+000\)} \\
\hline
\end{tabular}




Tool Dar

Figure 8. Common-
which the bJt is modelled and its behaviour predicted. Now we look at some the output data that can be obtained from this amplifier.

\section*{DC ANALYSIS}

Click on Analysis \(\rightarrow\) DC Analysis to obtain the DC Analysis Limits window. Input 1 Range of \(10,0,0.5\) is already displayed and is satisfactory. For Input 1, enter V1, the d.c. source. Check the Auto Scale Ranges box. As the d.c. source is swept from 0 V to 10 V , we will plot two variables, the emitter voltage at Node 3 and the collector current. Accordingly, the first plot has X Expression \(v(1)\), and Y Expression \(\mathrm{v}(2)\), while the second plot has \(X\) Expression \(\mathrm{v}(1)\) and \(Y\) Expression \(i(R 1)\). A '1' in each of the P boxes causes both plots to be made on the same grid. In the resulting plot, it is seen that \(v(3)\) rises with increasing \(\mathrm{v}(1)\) but the current appears to be zero. This is because the current is being plotted on the same scale as \(\mathrm{v}(3)\) but, as it is only a few milliamps, there is no discernible change. One way to display the current effectively is to change its \(Y\) expression to \(\mathrm{i}(\mathrm{R} 1)^{*} 1000\). This multiplies it by 1000 before plotting. The result of this is a pair of curves that are almost coincident, since \(v(3)=i(R 2) \times R 2=i(R 2) \times\) \(1000 \approx i(R 1) \times 1000\). Another way of displaying the current is to plot it on a separate grid. Leave the ' 1 ' in the P box in the first line, but enter a ' 2 ' in the P box of the second line. Now we obtain separate plots on appropriate scales (Figure 9). The graphs show that when the supply voltage is 9 V , the collector voltage is close to 4.5 V and the emitter current is 1 mA , as specified in the original design.

\section*{TRANSIENT ANALYSIS}

In the Transient Analysis Limits window, key in 10 m as the Time Range, 10 u as the Maximum Time Step, and check the Operating Point Only box.

SPICE always determines the d.c. operating point as the first step in an analysis. It sets the initial values on which a Transient Analysis is based. Here we have asked it to determine the operating point and then stop. No graph appears when we Run the analysis. The results we have asked for are displayed in the Numeric Output window. Display this by clicking on the 3rd button in the middle row. A table of results is displayed as shown at the bottom of the previous page.

These are the quiescent values to which the node voltages will settle in the absence of an input signal. In particular, the emitter voltage is 1.06 V , in agreement with a 1 mA emitter current, and the base voltage is 1.66 V , giving a 0.6 V base-emitter drop. Having been satisfied that the circuit has a correct quiescent state, click on Transient \(\rightarrow\) Limits, then deselect Operating Point Only, and select Operating Point and also Auto Scale Ranges. In this transient analysis, we look at input and output voltages, by plotting two graphs on one grid. Both P boxes contain '1'. The X Expressions are both 'T' (for 'time') and the Y Expressions are \(v(6)\) and \(v(5)\) respectively. The plot shows \(\mathrm{v}(5)\) as a sine wave, amplitude 2.55 V (use the Vertical Measure mode, top row, button 6), \(180^{\circ}\) out of phase with \(v(6)\). We have specified the amplitude of \(v(6)\) to be 0.02 V , so the amplifier gain is \(2.55 / 0.02=12.6\). Again, \(v(6)\) is too small to show clearly on the same scale as \(v(5)\). Either multiply \(\mathrm{v}(6)\) by a factor such as 10 , or plot them on two grids.

Graphs give a useful overall view of the waveforms but sometimes we might wish to know the voltage at a
given moment with a degree of precision. The Vertical and Horizontal Measure modes are very helpful but, for the most accurate results, we use a table of the actual values from which the graphs are plotted. To obtain this, enable the Numeric Output mode by clicking on the 4th button in the row to the left of the P box. Decide on how many points are required (say 200) and enter this in Number of Points. Run. After the graph is plotted, click on the Numeric Output button (3rd button, middle row). The DC Operating Point data is displayed as before, followed by transistor voltages and some of its parameters. Then comes a table of voltages against time for all 200 points in the Time Range. This data can be printed out or saved to a file, or you can copy it out by hand if you need just one or two points.

\section*{AC ANALYSIS}

Use this to find the response of the amplifier at different frequencies. The first thing is to edit V2 to include its a.c. parameters, v value \(=A C 0.02\) 0 . We have given the swept signal

> Figure 9. Current plots on different scales.
the same amplitude as in the previous tests. In the AC Analysis Limits window set the Frequency Range to 1 E 7 , 10 , which means from 10 Hz to 10 MHz . Only a single graph is required so, if the P box of the second row contains a ' 1 ', replace it with a blank. For the graph plot output voltage, \(\mathrm{v}(5)\), for the Y Expression against frequency ( F for the X Expression). The result is Figure 10 which shows maximum output between 800 Hz and 200 kHz , rolling off at frequencies below and above this range. Alternatively, you could plot gain \(v(5) / v(6)\) against frequency and obtain a graph

of the same shape. It is more usual to plot gain on a decibel scale, for which the \(Y\) Expression is \(\mathrm{db}(\mathrm{v}(5) / \mathrm{v}(6))\). At the same time, as a second graph (a ' 2 ' in the P box), we plot the phase of the output signal relative to the input signal entering the Y Expression as \(\mathrm{ph}(\mathrm{v}(5) / \mathrm{v}(6))\). The result is Figure 11, which is displayed in Cursor mode. The signal level is 42.5 dB for most of the frequency range, falling to 3 dB less than this at 65 Hz . It is necessary to alter \(C_{1}\) to make the -3 dB point at 30 Hz . Phase is

> Figure 11. Amplifier response on a decibel scale. The lower graph shows the phase of the output signal vs that of the input signal.
\(-180^{\circ}\) over a large part of the audio range ( 1 kHz to 20 kHz ), decreasing to \(-105^{\circ}\) at 30 Hz . This is a reasonably even phase response.

\section*{SPICE NETLIST}

An alternative way of entering a circuit is to type in a SPICE netlist. Some users may find it easier to do this than to manipulate the symbols, names and values of the Schematic. The netlist does not present such a clear picture of the connections between components but 1 , for one, find a netlist much easier to edit than a schematic. In the first column, for example, is the netlist of this month's circuit:
The title line begins with an asterisk so that it is ignored by SPICE. Next come the Element Statements which is a list of components, the nodes to which they are connected, and their values. From this we see, for example, that d.c. source V1 is connected to nodes 1 (positive first) and 0 and its value is \(9 \mathrm{~V} . \mathrm{V} 2\) is connected to nodes 6 and 0 , and its operation is defined as we have previously noted. A BJT transistor is coded as Q in SPICE, then follow the nodes to which its collector, base and emitter are respectively connected. The model name QONE is an arbitrary name referring to the model statement later in the list. The model statement begins with .mODEL, followed by model name (QONE), NPN to indicate its type, and then a list of parameters. It is not necessary to assign values to all 40 parameters because default values are used for those left undefined. Here we make the forward gain 150, base resistance \(120 \Omega\), forward Early voltage 105 V and the capacitance of the basecollector junction 5 pF . The .TEMP Control statement sets the running temperature to any chosen value, \(20^{\circ} \mathrm{C}\) in this example instead of the sPICE standard temperature of \(27^{\circ} \mathrm{C}\). The statement .OP directs SPICE to perform a d.c. operating point analysis. This is virtually an essential

preliminary to a Transient Analysis, as explained above. The statement .TRAN 10E-6 0.005, asks for a Transient Analysis, sampled at \(1 \mu\) s intervals for 0.005 s \((5 \mathrm{~ms})\). The .PLOT statement asks for the values of \(v(5)\) to be plotted. Finally, the .END statement is a mandatory part of any SPICE netlist.

This netlist can be typed directly into MC5. Run MC5 and, when the opening window appears, click on File \(\rightarrow\) New \(\rightarrow\) Spice/Text \(\rightarrow\) OK \(\rightarrow\) type in netlist. Or type the netlist in with a word-processor such as MS Works, then copy it to the Clipboard. Run MC5 as above and, after OK, click on Edit \(\rightarrow\) Paste. Click on Analysis \(\rightarrow\) Transient Analysis. The Transient Analysis Limits window appears with the Time Range already set to 0,005 and the number of points set to 501 (equivalent to \(1 \mu\) s intervals). The temperature is already set to \(20^{\circ} \mathrm{C}\) and the Operating Point box already checked. Run the analysis to obtain the plot. If you click on the Numeric Output button, you see the d.c. analysis similar to that described earlier. Click on Transient \(\rightarrow\) Exit Analysis to return to the netlist display, which you can then edit or extend. There is no space here to go further into the details of SPICE netlist syntax, but enough has been shown to demonstrate this alternative way of making input to MC5.

\section*{INVESTIGATION 2}

The amplifier was intended to pass audio frequencies above 30 Hz , by which we mean that the output amplitude at 30 Hz should be no more than 3 dB below its maximum at higher frequencies. Instead, it is about 7.5 dB down, giving a loss of bass tones. Find out what change must be made to the capacitance of one of the capacitors to give a roll-off of -3 dB at 30 Hz .

\section*{INVESTIGATION 1}

\section*{(ANSWERS)}

Last month's circuits are repeated in Figure 12. Circuit (a) demonstrates the charging and discharging of a capacitor by a constant voltage source. It is tested with a 1 V pulse starting at \(t=\) \(1 \mu \mathrm{~s}\) and ending at \(t=14 \mu \mathrm{~s}\). As soon as the pulse begins, the p.d. across the capacitor, \(\mathrm{v}(2)\), rises exponentially to 1 V , according to the equation \(v_{\mathrm{c}}=\) \(v\left(1-\mathrm{e}^{-t / R C}\right)\), where \(v\) is the pulse height \(=1 \mathrm{~V}\). When the pulse ends, \(\mathrm{v}(2)\) falls exponentially from 1 V to 0 V according to the equation \(v_{\mathrm{c}}=v\left(1+\mathrm{e}^{-t / R c}\right)\).

In circuit (b), when the source is a 1 kHz sine wave, amplitude 1 V , the signal across the capacitor is a 1 kHz sine wave, amplitude 0.074 V , lagging \(90^{\circ}\) behind the source. At 1 kHz , the impedance of \(C_{1}\) is \(1 / 2 \pi f \mathrm{C}=79.6 \mathrm{k} \Omega\). In series with \(R_{1}\) this forms a potential divider, total resistance \(1079.6 \mathrm{k} \Omega\). The
proportion of the source voltage ( 1 V ) developed across \(C_{1}\) is \(1 \times 79.6 / 1079.6=\) 0.074 V , as found in the analysis. Note how the average value of the waveform across the capacitor gradually drops; on the first upward swing of V1 the p.d. across the capacitor swings up to 0.74 V , giving an offset of 0.37 V . But gradually this charge leaks away, the average value (or offset) becoming 0 V .

At the beginning of the pulse in circuit (c) the sudden rise in p.d. across the inductor induces an equal and opposite e.m.f. Figure 13), but when there is no further change in p.d. from the source, there is no induced e.m.f. and the p.d. across the inductor falls. Conversely, a sudden fall of p.d. at the end of the pulse induces a negative spike, and again the p.d. gradually falls to zero. With larger inductors there is a slower return to zero so that, for 200 mH or more, the p.d. across the inductor almost follows the pulse. With smaller inductors there are smaller, short-lived spikes.

Circuit (d) illustrates several features of a resonant circuit. With component values as specified, the resonant frequency is \(1 /\{2 \pi \sqrt{ }(L C)\}=\) 35.6 kHz . On the a.c. analysis plot of the inductor p.d.,v(3), against frequency, there is a sharp peak at this frequency. The peak reaches 18.2 V . The voltage falls to zero at lower frequencies and to 1 V at higher frequencies. Increasing \(\mathrm{R}_{1}\) reduces the height of the peak (dampens the response); if \(R\) is \(5 \mathrm{k} \Omega\) or more the peak disappears and then the plot takes the form of the output of a high-pass filter. As expected from the equation, increasing \(\mathrm{C}_{1}\) or increasing \(\mathrm{L}_{1}\) both reduce the resonant frequency.

Figure 14 explains how it is possible for the p.d. across the inductor to rise to 18.2 V or even higher (it rises to

60 V
Figure 13. A sudden rise in p.d. across an inductor produces an equal but opposite e.m.f.


Figure 12. Repeat of Figure 5 in Part 1: a number of circuits for analysis by the reader.
nents. It is possible to model such happenings but this has not been done in these analyses. This is a reminder that a simulation models only those aspects of reality that are written into it. If it is not programmed intelligently, it may sometimes give false results.

Incidentally, the two curves in Figure 14 are distinguished by marking one of them with tokens. This is done automatically by clicking on the 4th button from the right in the bottom row. This feature is useful if graphs are to be reproduced in black-and-white, as in a book or magazine.
[960102-2]

Figure 14. Illustration of how a p.d. across an inductor can rise to many times the level of the source voltage.


Tool bar


\section*{[4] \(V\)}

\section*{A-D converter}

The converter described in this article is, technically speaking, state-of-the-art as far as analogue-todigital conversion is concerned. It offers a true resolution of 20 bits, is of superb quality and has symmetrical inputs. In short: it is difficult to imagine a better converter for quality-conscious sound engineers than the present one - and certainly not at the price.

The circuit is based on a Type CS5390 integrated stereo analogue-to-digital converter (ADC) from Crystal, which is currently taken as the quality standard and is used in much professional equipment. It uses \(\times 64\) oversampling, contains a phase-linear digital antialiasing filter, and has a dynamic range of 110 dB . It is pin-compatible with the 18-bit Type CS5389 ic.

The converter stage is preceded by an elaborate analogue input amplifier, whose outstanding property is its ability to accept symmetric as well as asymmetric signals. The quality of this amplifier can be improved even more by the use of rare (expensive) operational amplifiers.

The coding and sending of the converted audio data is effected with the aid of a Type CS8402A integrated digital audio interface. This Ic is used in the same configuration as in the 'sampling rate converter' published in the October issue of this magazine.

The amplifier has an electrically isolated \(\mathrm{s} /\) pDIF output, but there is also provision for an optical output.

\section*{SYMMETRIC INPUTS}

Attaining a true resolution of 20 bits places a heavy demand on the circuit
designer, whose ingenuity is taxed from the inputs onwards.

If optimum use is to be made of the symmetric inputs of the CS5390 ( \(\mathrm{IC}_{7}\) ), the input amplifier and source signals must also be symmetric. Since, however, many users do not work with symmetric signals, the converter must also be capable of processing asymmetric signals.

Such considerations have led to the converter being given a fairly complex input circuit, whose special property is its capability of processing differential as well as single-ended signal without the need of switching. In the circuit diagram in Figure 1, the circuit for the left-hand channel consists of op amps \(\mathrm{IC}_{1}-\mathrm{IC}_{3}\) and that for the right-hand channel of op amps \(\mathrm{IC}_{4}-\mathrm{IC}_{6}\). Otherwise, the channels are identical.

The following discussion is based on the left-hand channel; components in the right-hand channel are stated in brackets.

Input socket \(K_{1}\) is followed by attenuator \(R_{1}-R_{4}\left(R_{12}-R_{15}\right)\), which is necessary for presetting the input stage, particularly in case of asymmetric signals. Op amps \(\mathrm{IC}_{1}\) and \(\mathrm{IC}_{2}\left(\mathrm{IC}_{4}\right.\) and \(\mathrm{IC}_{5}\) ) are arranged as \(\times 10\) amplifiers


Figure 1. The circuit consists essentially of four sections: the analogue input amplifier, IC \(C_{1}-\mathrm{IC}_{6}\); the ADC proper, \(I C_{7}\); the output interface, \(I C_{10}\); and the power supply, \({ }^{1 C_{12}}{ }^{-1 C_{16}}\).
with an input sensitivity of \(1 \mathrm{~V}_{\text {RMS }}\). When an asymmetric signal is input, the inverting ( - ) input of the op amps is grounded, which disturbs their setting. However, the consequent imbalance of the signals is corrected imme-
diately by \(\mathrm{IC}_{3}\left(\mathrm{IC}_{6}\right)\) with an accuracy of no less than \(\pm 0.08 \mathrm{~dB}\).

The quality of the op amps used is, of course, of paramount importance: the Type AD711 from Analog Devices in the \(\mathrm{IC}_{1}\) and \(\mathrm{IC}_{2}\left(\mathrm{IC}_{4}\right.\) and \(\left.\mathrm{IC}_{5}\right)\) positions was found to give very good performance. In the \(\mathrm{IC}_{3}\left(\mathrm{IC}_{6}\right)\) position, a standard TL071 (which is far less expensive) was found to be perfectly satisfactory. In any case, this latter Ic has no role to play in the case of symmetric signals, while with asymmetric signals it is just part of the feedback loop where it has far less effect on the signal quality than the earlier mentioned
op amps.
If superlative performance is required, use Type OPA627 chips in the \(\mathrm{IC}_{1}-\mathrm{IC}_{3}\left(\mathrm{IC}_{4}-\mathrm{IC}_{6}\right)\) positions. Bear in mind, however, that these ICs are about ten times as costly as an AD711.

\section*{CONVERSION}

Full data of the Type CS5390 A-D converter \(\left(\mathrm{IC}_{7}\right)\), as well as its internal block diagram, are given in the data sheets elsewhere in this issue.

Schottky diodes \(\mathrm{D}_{1}-\mathrm{D}_{8}\) and zener diodes \(D_{11}\) and \(D_{12}\) protect the IC against excessively high input signals. The Schottky diodes protect against

\section*{}

The prototype was, of course, tested thoroughly, including FFT analyses of the output data of the converter chip for which the total harmonic distortion \((T H D+N)\) at 1 kHz was calculated in the digital domain. This gave the following results:
\[
\begin{array}{cc}
\text { Input level } & T H D+N \\
0 d B & <-97 d B \\
-3 d B & <-100 d B \\
-6 d B & <-99 d B \\
-9 d B & <-96 d B \\
-12 d B & <-93 d B \\
-15 d B & <-90 d B
\end{array}
\]

The same calculation was carried out at 7 kHz , since the 3rd harmonic of this falls just within the range of the digital filter. The differences with the results obtained at 1 kHz were negligible.

As the test results show, the manufacturers' stated dynamic range of 110 dB was, in practice, just not attainable. This is partly because of the \(\times 10\) amplification in the input amplifiers and the consequent higher sensitivity. When the ratio of the input level (in \(d B\) ) is added to the \(T H D+N\) value (in \(d B\) ), the noise level is effectively 105 dB below full scale. This changes only when the input signals exceed \(-6 d B\). However, from that point on, there is a noticeable increase in distortion. Note that distortion here means deviations of the order of not more than \(5 \times 10-6\) !

In any case, since in digital recording the normal headroom is 12 dB , it may be assumed that for average signal levels the distortion produced by the A-D converter is negligible.

The frequency spectrum of two FFT analyses is shown. Figure A is measured with a signal of 0 dB and Figure \(B\) with one of \(-12 d B\). To recover the 7th and 9th harmonics from the noise, four measurements were carried out in each case. At an input level of \(-12 d B\), there was no trace of any harmonics.

To satisfy the curiosity of some readers, the frequency spectrum with shorted input was measured: the result is shown in Figure C. This shows a virtually Gaussian distribution without any remains or effects of clock interference, supply ripple or other possible sources of interference.


960110-12


960110-13

latch-ups, while the zener diodes limit an increase in the supply voltage in case of overdrive. The latter is vital, because the maximum permissible supply voltage for the CS5390 is \(\pm 6 \mathrm{~V}\).

The value of series resistors \(\mathrm{R}_{23}\) and \(R_{24}\left(R_{25}\right.\) and \(\left.R_{26}\right)\) ensures optimum source impedance for \(\mathrm{IC}_{7}\).

Parallel capacitor \(\mathrm{C}_{27}\left(\mathrm{C}_{28}\right)\) must be a close-tolerance type, since it suppresses r.f. noise caused by the oversampling. It is, as it were, complementary to the digital filter, since the suppression range of this does not extend into the r.f. bands.

As far as the operation of \(\mathrm{IC}_{7}\) is concerned, it is best to treat it as a black box, into which analogue signals are pumped and from which digital signals are extracted. According to the manufacturers' data, the chip uses delta-sigma modulators with \(\times 64\) oversampling for the conversions. The modulators are followed by a digital filter, whereupon the sampling frequency is reduced to 48 kHz . Because of the very high oversampling rate, a separate anti-aliasing filter is not required.

Most of the remaining circuitry, except the reset circuit connected to the digital power down (DPD) input, and jumper \(\mathrm{JP}_{1}\), serves to decouple the power supply and reference voltage lines.

When switch \(\mathrm{S}_{2}\) is pressed, network \(\mathrm{R}_{28}-\mathrm{C}_{41}\) and Schmitt trigger IC \(\mathrm{C}_{9 \mathrm{~b}}\) provide a 1 s long positive pulse at the DPD input. This results in an overall reset of the entire digital section of \(\mathrm{IC}_{7}\). After the pulse has decayed, an offset calibration cycle is started automatically. During this cycle, the offset in either channel is measured and deducted from the sampling values. It is thus possible to start this calibration at any desired moment, without having to switch the entire converter off and then on again, simply by pressing \(S_{2}\). In other words, this design makes possible a conversion without having to worry about any offset voltages, which for certain applications is of vital importance. It should be borne in mind that each and every cold start results in a (small) drift of any offset voltage in both the converter chip and the input amplifiers.

The level at the acal input determines whether the offset is measured in the input amplifiers or not. If this input is grounded via \(\mathrm{JP}_{1}\), the offset in the input amplifiers will be measured. In this case, there must be no input signal to the amplifiers, since that may lead to measurement errors. If ACAL is linked to dCal via \(\mathrm{JP}_{1}\), the offset in the input amplifiers is ignored. Note that the output of DCAL remains high for 4096 clock pulses after DPD has gone low.

By means of the logic level at

CMODE, the serial output interface of \(\mathrm{IC}_{7}\) enables the value of the requisite ICLKD clock, which has been fixed for an output word rate - owr - of 48 kHz , to be determined. In the present design, CMODE is permanently low, which results in a clock frequency of \(256 \times\) owr \(=12.288 \mathrm{MHz}\).

The level at smode determines whether the ic operates in a slave mode or a master mode. A high level at this terminal results in SCLK, FSYNC, and \(\mathrm{L} / \overline{\mathrm{R}}\) functioning as outputs whose level is derived from ICLKD by internal dividers.

The 20 -bit samples in 2 -complement code are available at output sdata.

The clock generator is a module containing both the crystal and the requisite active circuitry. This arrangement saves space and also minimizes the risk of r.f. interference.

The converted data at the output of \(\mathrm{IC}_{7}\) are applied to output socket \(\mathrm{K}_{4}\) via stoppers \(\mathrm{R}_{30}-\mathrm{R}_{34}\) and the output circuit. The timing of the data is nearly, but not quite, \(\mathrm{I}^{2} \mathrm{~S}\) compatible: it lacks an inverted \(\mathrm{L} / \overline{\mathrm{R}}\) signal, but this is provided by \(\mathrm{IC}_{9 \mathrm{~d}}\).

\section*{OUTPUT}

The general \(I^{2}\) s output is taken from \(\mathrm{K}_{4}\). A miscellany of signal-processing equipment (for volume control, tone control, interface for test purposes, and so on) may be connected to this socket. The output is also well suited for receiving the 'digital vu meter' (a special test instrument for digital audio signals, fitted with a double 30 -segment LED bar and 3.5-digit displays) described in the April/May 1996 issues of this magazine.

Short-circuiting \(\mathrm{JP}_{2}\) links the +5 V supply line to \(K_{4}\), which is usable if the equipment connected to the socket draws a current of not more than a few milliamperes. In all other cases, the equipment must have its own power supply.

There is, of course, an s/PDIF output. For this, use is made of the same digital audio interface transmitter \(\left(\mathrm{IC}_{10}\right)\) as used in the 'sampling rate converter' described in the October 1996 issue of this magazine. The most significant channel-status bits of this IC are set with octal DIP switch \(\mathrm{S}_{1}\).

Apart from coaxial output \(K_{3}\), an optical output is provided by \(\mathrm{IC}_{11}\).

\section*{POWER SUPPLY}

Since the power lines to the digital and analogue sections of the circuit must be isolated, two separate mains transformers are used: \(\operatorname{Tr}_{2}\) for the analogue section, and \(\mathrm{Tr}_{3}\) for the digital section.

The output of \(\mathrm{Tr}_{2}\) is rectified by \(B_{1}\), smoothed by a number of electrolytic capacitors, and regulated by \(\mathrm{IC}_{14}\) and
\(\mathrm{IC}_{15}\). The resulting \(\pm 12 \mathrm{~V}\) output is used to power the input amplifiers, and also to provide the \(\pm 5 \mathrm{~V}\) lines for the analogue circuits in \(\mathrm{IC}_{7}\). The \(\pm 5 \mathrm{~V}\) lines are regulated by \(\mathrm{IC}_{12}\) and \(\mathrm{IC}_{13}\).

The output of \(\mathrm{Tr}_{3}\) is rectified by \(\mathrm{B}_{2}\), smoothed by several electrolytic capacitors, and regulated by \(\mathrm{IC}_{16}\), resulting in a single-ended supply line of +5 V .

The only link between the two supply lines is \(\mathrm{JP}_{3}\), which commons their earth returns.

The supply lines are copiously decoupled for r.f. Also, the arms of the bridge rectifiers are shunted by antirattle capacitors, while the electrolytic buffer capacitors are without exception shunted by 100 nF ceramic capacitors.

\section*{PRINTED-CIRCUIT}

\section*{BOARD}

The converter is best built on the printed-circuit board shown in Figure 2. This board is through-plated an double-sided and has, at the component side, two large earth planes, one each for the analogue and digital circuits.

The board consists of two distinct parts: that for the power supply (shown in dashed lines in Figure 1) must be cut off and built up independently. Not all mains transformers may fit neatly on the supply board, which must then be adapted accordingly. The \(\pm 12 \mathrm{~V}\) and +5 V lines must be linked to the corresponding terminals on the converter board via flexible circuit wire. None of the voltage regulators needs a heat sink.

Populating the converter board is fairly straightforward but, in a quality unit such as the converter, the utmost care must, of course, be observed in the work. Whether or not ic sockets should be used is immaterial: from a technical point of view it is better to solder the ics directly to the board, but some less-experienced constructors may prefer to use sockets.

All constructors are advised not to scrimp on the components. A fair number of \(1 \%\) resistors, as well as quite a few close-tolerance polystyrene (not cheap) capacitors, are used. Furthermore, high-quality types of socket must be used for \(\mathrm{K}_{1}-\mathrm{K}_{3}\).

Output transformer \(\operatorname{Tr}_{1}\) is a DIY component, wound on a toroidal core Type G2/3FT12. Wind the primary, consisting of 20 turns of 0.7 mm dia. enamelled copper wire, evenly spread over the core, first. Leave some space at the centre of the winding, where the two-turn secondary (same wire) is laid. This is exactly the same transformer as used in the 'sampling rate converter' published in the October 1996 issue of this magazine.

Using heavy-duty wire, short-circuit

Figure 2. The doublesided, through-plated printed-circuit board consists of two sections: one for the power supply and the other for the digital and analogue circuits. The board is intended to be cut into two.
the two terminals of wire bridge \(\mathrm{JP}_{3}\).
With \(\mathrm{JP}_{1}\) in the right-hand position (pin 5 of \(\mathrm{IC}_{7}\) to ground), the offset of the input amplifiers is measured during the automatic calibration; with \(\mathrm{JP}_{1}\) in the left-hand position (pin 5 linked to pin 9), this is not done.

If the equipment connected to \(\mathrm{K}_{4}\) can be powered by the converter (current drawn by it no more than a few mA ), the +5 V line is linked to \(\mathrm{K}_{4}\) via wire bridge \(\mathrm{JP}_{2}\).

When both boards have been completed, a thorough check (consulting the circuit as well as the parts list) is recommended. Also, compare the boards with the photograph of the completed prototype in Figure 3.

\section*{INITIAL TEST}

Connect \(2.2 \mathrm{k} \Omega\) resistors to each of the outputs of the supply board.

Connect the mains to terminal block \(K_{5}\) via a suitable mains cable, whereupon on/off indicator \(\mathrm{D}_{10}\) should light.

Using a good multimeter, check the output voltages of the power supply. If all potentials are what they should be, the \(2.2 \mathrm{k} \Omega\) resistors must be removed from the supply board outputs, which should then be linked to the relevant terminals on the converter board.

ENCLOSURE
When all has been found in order, the converter should be fitted in a suitable enclosure. The only restrictions on the choice of this are that it must be of metal and large enough to house the converter and its power supplies.

\begin{tabular}{|c|c|c|}
\hline Parts list & \(\mathrm{R}_{36}=270 \Omega\) & \(\mathrm{C}_{7}, \mathrm{C}_{20}=120 \mathrm{pF}, 160 \mathrm{~V}\), polystyrene \\
\hline & \(\mathrm{R}_{37}=75 \Omega\) & \(\mathrm{C}_{8}-\mathrm{C}_{13}, \mathrm{C}_{21}-\mathrm{C}_{26}, \mathrm{C}_{29}, \mathrm{C}_{31}, \mathrm{C}_{32}, \mathrm{C}_{34}\). \\
\hline Resistors: & \(\mathrm{R}_{38}=8.2 \mathrm{k} \Omega\) & \(\mathrm{C}_{36}-\mathrm{C}_{38}, \mathrm{C}_{40}, \mathrm{C}_{452}, \mathrm{C}_{44}, \mathrm{C}_{46}, \mathrm{C}_{48}-\mathrm{C}_{50}\) \\
\hline \(\mathrm{R}_{1}-\mathrm{R}_{4}, \mathrm{R}_{12}-\mathrm{R}_{15}=7.87 \mathrm{k} \Omega, 1 \%\) & \(\mathrm{R}_{39}=4.7 \Omega\) & \(\mathrm{C}_{53}, \mathrm{C}_{54}, \mathrm{C}_{57}, \mathrm{C}_{59}, \mathrm{C}_{60}, \mathrm{C}_{63}, \mathrm{C}_{64}, \mathrm{C}_{71}\) \\
\hline \(\mathbf{R}_{5}, \mathrm{R}_{8}, \mathrm{R}_{16}, \mathrm{R}_{19}=1.10 \mathrm{k} \Omega, 1 \%\) & \(\mathrm{R}_{40}=2.2 \mathrm{k} \Omega\) & \(\mathrm{C}_{73}=100 \mathrm{nF}\), ceramic \\
\hline \[
\begin{aligned}
& R_{6}, R_{7}, R_{9}, R_{10}, R_{17}, R_{18}, R_{20} \\
& R_{21}=10.0 \mathrm{k} \Omega, 1 \%
\end{aligned}
\] & nductors: & \[
\begin{aligned}
& \mathrm{C}_{27}, \mathrm{C}_{28}=6.8 \mathrm{nF}, 63 \mathrm{~V}, 1 \% \text {, poly- } \\
& \text { styrene, radial, pitch } 7.5 \mathrm{~mm}
\end{aligned}
\] \\
\hline \(\mathrm{R}_{11}, \mathrm{R}_{22}=100 \mathrm{k} \Omega\) & \(\mathrm{L}_{1}-\mathrm{L}_{3}=47 \mu \mathrm{H}\) & \(\mathrm{C}_{30}=100 \mu \mathrm{~F}, 25 \mathrm{~V}\), radial \\
\hline \(\mathrm{R}_{23}-\mathrm{R}_{26}=39.2 \Omega, 1 \%\) & & \(\mathrm{C}_{33}, \mathrm{C}_{35}, \mathrm{C}_{39}, \mathrm{C}_{43}=1 \mu \mathrm{~F}, 35 \mathrm{~V}\), tantalum \\
\hline \(\mathrm{R}_{27}=51.1 \Omega\) & & \[
\mathrm{C}_{41}, \mathrm{C}_{51}, \mathrm{C}_{52}, \mathrm{C}_{55}, \mathrm{C}_{56}, \mathrm{C}_{58}, \mathrm{C}_{61}, \mathrm{C}_{62}
\] \\
\hline \(\mathrm{R}_{28}=120 \mathrm{k} \Omega\) & \[
\mathrm{C}_{1}-\mathrm{C}_{4}, \mathrm{C}_{14}-\mathrm{C}_{17}=100 \mathrm{pF}, 63 \mathrm{~V} \text {, poly- }
\] & \[
\mathrm{C}_{72}=10 \mu \mathrm{~F}, 63 \mathrm{~V} \text {, radial }
\] \\
\hline \(\mathrm{R}_{29}=100 \Omega\) & styrene, radial, pitch 7.5 mm & \[
\mathrm{C}_{45}=47 \mu \mathrm{~F}, 25 \mathrm{~V} \text {, radial }
\] \\
\hline \(\mathrm{R}_{30}-\mathrm{P}_{34}=47 \Omega\) & \(\mathrm{C}_{5}, \mathrm{C}_{6}, \mathrm{C}_{18}, \mathrm{C}_{19}=47 \mathrm{pF}, 160 \mathrm{~V}\), poly. & \(\mathrm{C}_{47}, \mathrm{C}_{67}-\mathrm{C}_{70}, \mathrm{C}_{75}-\mathrm{C}_{78}=47 \mathrm{nF}\), ceramic \\
\hline \(\mathrm{R}_{35}=10 \mathrm{k} \Omega\) octal array & styrene & \(\mathrm{C}_{65}, \mathrm{C}_{66}=470 \mu \mathrm{~F}, 25 \mathrm{~V}\), radial \\
\hline
\end{tabular}

\(\mathrm{C}_{74}=1000 \mu \mathrm{~F}, 16 \mathrm{~V}\), radial

\section*{ISemiconductors:}
\(\mathrm{D}_{1}-\mathrm{D}_{9}=\mathrm{BAT} 85\)
\(\mathrm{D}_{10}=\) LED, low current
\(\mathrm{D}_{11}, \mathrm{D}_{12}=\) zener diode \(5.6 \mathrm{~V}, 1.3 \mathrm{~W}\)
\(B_{1}, B_{2}=B 80 C 1500\) right-angled bridge rectifier

\section*{Integrated Circuits}
\(\mathrm{IC}_{1}, \mathrm{IC}_{2}, \mathrm{IC}_{4}, \mathrm{IC}_{5}=\mathrm{AD} 711 \mathrm{JN}\) (Analog Devices)
\(\mathrm{IC}_{3}, \mathrm{IC}_{6}=\) TLO71CP (see text)
\(\mathrm{IC}_{7}=\mathrm{CS} 5390-\mathrm{KP}\) (Crystal)
\(\mathrm{IC}_{8}=\) oscillator module, 12.288 MHz (Seiko Epson Type SG51P)
\(\mathrm{IC}_{9}=74 \mathrm{HC} 14\)
\(\mathrm{IC}_{10}=\) CS8402A (Crystal)
\(\mathrm{IC}_{11}=\) TOTX173 (Toshiba)
\(\mathrm{IC}_{12}, \mathrm{IC}_{16}=7805\)
\(\mathrm{C}_{13}=7905\)
\(I_{14}=7812\)
\(I_{15}=7912\)

\section*{Miscellaneous:}
\(\mathrm{JP}_{1}=3\)-way pin header and jumper
\(\mathrm{JP}_{2}=2\)-way pin header and jumper
\(\mathrm{JP}_{3}=\) wire bridge
\(K_{1}, K_{2}, K_{3}=\) phono socket for board mounting
\(K_{4}=10\)-way box header
\(K_{5}=3\)-way terminal block (for accept-
ing 3-wire mains cable), pitch 7.5 mm
\(S_{1}=\) octal DIP switch
\(\mathrm{S}_{2}=\) single-pole push-button switch
\(\mathrm{Tr}_{1}=\) see text
\(\mathrm{Tr}_{2}=\) mains transformer \(2 \times 15 \mathrm{~V}, 4.5 \mathrm{VA}\)
\(\mathrm{Tr}_{3}=\) mains transformer \(1 \times 9 \mathrm{~V}, 1.5 \mathrm{VA}\)
PCB, Order no. 960110
 the photograph is small, it may be seen that Type OPA627 circuits are used in the \(I C_{1}-I C_{6}\) positions.

Wiring up the unit is simple, but the best way is to fix the converter in such a way that output sockets \(K_{3}\) and \(\mathrm{IC}_{11}\) protrude through the rear panel of the case.

Next, fit sockets \(\mathrm{K}_{1}\) and \(\mathrm{K}_{2}\) and link these with screened cable to the input terminals of the converter board.

Fit a mains entry, preferably with integral on/off switch, to the rear panel of the case and link this via a length of suitable mains cable to \(K_{5}\). If the on/off switch is preferred on the front panel, insert it in series with the mains entry and K 5 .

The only other operating controls on the front panel are on/off indicator \(\mathrm{D}_{10}\) and reset push-button switch \(\mathrm{S}_{2}\).

To obtain maximum benefit of the screening of the metal enclosure, it should be linked at a single point to the ground of the converter and power supplies and to the mains earth. This is best done with a small bolt, nut, washer and solder tags fitted to a suitably drilled hole in the bottom of the enclosure. Wire bridge \(\mathrm{JP}_{3}\) may also be
used for commoning the earths.
Finally, consult the Safety Guidelines elsewhere in this issue.

\section*{APPLICATIONS}

The converter is suitable for use in a wide range of applications in which analogue-to-digital conversion of the highest quality is needed. One possible application is its use as an upgrade for a DAT recorder (no longer in production), which is straightforward thanks to its symmetric inputs. Where the necessary equipment exists for mixing at digital level, several converters may be used to make a master recording with only one dAT recorder.

Another use is in combination with the 'sampling rate converter' mentioned before. Such a combination would make it possible, for instance, to make analogue recordings with a sampling rate adapted to the CD standard. In principle, that may also be done without a sampling rate converter, but then the clock of \(\mathrm{IC}_{7}\) must be altered to 11.2896 MHz : this would give a sampling rate of 44.1 kHz . However, the published 'sampling rate converter' offers the possibility of converting the 20 -bit data into a 16 -bit format, whereby, through psychoacoustic noise shaping, a resolution of 18 bits is attained.

\section*{In pacsing \\ 표}

\section*{What progress?}

After much discussion, we had finally convinced our managing director that we urgently needed a new, faster computer for communicating over the Internet. The 386 unit to be replaced was, in spite of the Windows 95, a lame duck.

When the new 150 MHz pentium computer finally arrived, we coud not wait to get going on it. Alas, our joy did not last very long. After all connections were made and the mains switched on, all that worked was the internal fan. The computer itself remained dead. Now what? Of course, there is such a thing as a guarantee, but as engineers ourselves, we wanted to find out what was wrong. So, the case was opened and what did we find? The VGA card was suspended somewhere above the PCI connector it should mate with. A further check revealed that the cover of the card was not in the correct position, so that the card could not be pushed far enough into the PCI connector. When all this was righted, hurray! The PC worked.

The supplier had installed Windows 95 on to the hard disc, but he had probably never heard of cluster sizes. The entire 1.6 GB hard disc consisted of one partition! So, we arranged the dise in three partitions and reinstalled the software. After Windows had been reinstalled, the drivers for the VGA card also had to be reinstalled. Not so difficult, you might think, since there was an installation for Windows 95. This worked all right, but the utility for setting the image frequency (which was there originally) could not be found. But we had selected the correct video processor according to the manual and the floppy. So, we installed the DOS utilities, which, strangely enough, were on another floppy that was, according to the instructions, intended for OS/2. The utitlity we wanted could not be found. By now very suspicious, we looked again and found the Windows drivers for this card on a CD-ROM containing all sorts of demo for the VGA card. When these were tried, they proved to be for a different video processor than the present one. Oh, well, you can only try! And, lo and behold, they were the correct drivers with the associated Windows utilities. If you can understand all this, we cannot.

Browsing through the said CD-ROM, we had seen MPEG-player software, and this we had to try, of course. This did not prove to be a success, either. The program worked all right, but every time the film was run, the start menu for Windows disappeared after a second or so, so that there was no time to start the program. By then it was time to go home.

We shall sleep over it. Tomorrow, with fresh suspicions, we shall try the sound card.

Harry Baggen

\title{
parametric equalizer
}

Straightening the frequency characteristic of an audio system is possible by either of two types of equalizer: graphic and parametric.

A graphic equalizer consists of a series of tuneable active filters, normally one for each frequency band. In spite of the complexity of this type of equalizer, it only provides adjustment of the amplification or attenuation in a given band. Also, however carefully the filters have been computed, in practice, the final characteristic never coincides with the positions of the potentiometers on the control panel.

A parametric equalizer normally consists of far fewer filters. Moreover, not only the amplification/attenuation of these filters is variable, but also their central frequency and \(Q\)-factor.

In the present circuit, the central frequency is set with \(\mathrm{P}_{2}\) in each of the three frequency bands \((20-200 \mathrm{~Hz}\), \(200-2000 \mathrm{~Hz}\), and \(2-20 \mathrm{kHz}\) ), selected with \(\mathrm{S}_{1}\).

The \(Q\)-factor is set with \(\mathrm{P}_{1}\) in the range \(0.25-2.5\). This factor determines the slope of the skirts of the frequency characteristic.

The amplification/attenuation is set with \(P_{3}\) over a range from -12 dB to +12 dB .

The curves in the lower diagram show various settings of the equalizer, starting with the upper curve: (a) maximum amplification, lowest \(Q\); (b) maximum amplification, highest \(Q\); (c) maximum attenuation, highest \(Q ;(\mathrm{d})\) maximum attenuation, lowest \(Q\).

The circuit in the diagram can provide only one dip or peak in each frequency curve. If this is not sufficient, a number of circuits per channel may be necessary. This is one of the reasons that it is advisable to use a simple buffer amplifier at the input. Another is that the input impedance of the filter varies appreciably during the setting-up process.

A few notes on the construction. Circuits \(\mathrm{IC}_{1 \mathrm{a}}\) and \(\mathrm{IC}_{1 \mathrm{~b}}\) simulate a tuneable \(L C\) circuit in parallel with \(\mathrm{S}_{1}\) and \(\mathrm{P}_{2}\). The design is such that the reactances of the simulated
inductance and capacitance hardly vary over the range of central frequencies that can be set with \(\mathrm{P}_{2}\). This makes independent setting of the \(Q\) -
ter of \(\mathrm{T}_{1}\) in a ratio determined by the setting of \(\mathrm{P}_{3}\).

The complete filter can be shorted out with \(S_{2}\) to enable a quick comparison to be
below the standard line level.
Since the equalizer draws a current of only 25 mA , the supply voltage may be obtained from the preamplifier

factor with \(\mathrm{P}_{1}\) possible.
The output voltage of the filter is buffered by \(\mathrm{IC}_{2 \mathrm{a}}\), after which it is mixed with the signal originating from the emit-
made with a guaranteed straight frequency characteristic.

The circuit needs an input signal of \(75-100 \mathrm{mV}\), which is
with which the equalizer is used.

The total harmonic distortion plus noise ( \(\mathrm{THD}+\mathrm{N}\) ) is \(\leq 0.008\) per cent at a frequency of \(1 \mathrm{kHz}\left(\mathrm{P}_{3}\right.\) at the centre of its travel).

The value of \(\mathrm{R}_{15}\) is not a standard one and the resistor must, therefore, be made from several others. A similar problem occurs with \(\mathrm{C}_{7}\), although its value is standard in the (often difficult to obtain) E24 series. This capacitor may, therefore, also have to be made from several others.
[R. Shankar - 964115]

\section*{delay line}

The delay line makes possible an improvement of the sur-round-sound decoder published in this magazine in early \(1995^{*}\).

The differential signal of the surround-sound channel is first passed through a lowpass filter and then split into two. Whereas \(\mathrm{IC}_{1 \mathrm{c}}\) functions as a buffer, \(\mathrm{IC}_{1 \mathrm{~b}}\) inverts the signal. Both signals are then applied to identical memories of the bucket-brigade type.

Circuits \(\mathrm{IC}_{3}\) and \(\mathrm{IC}_{4}\) are controlled synchronously by \(\mathrm{IC}_{5}\). The delayed signals are buffered by \(\mathrm{IC}_{2 \mathrm{a}}\) and \(\mathrm{IC}_{2 \mathrm{~d}}\), after which they are applied to differential amplifier \(\mathrm{IC}_{2 \mathrm{c}}\). As the signals are in antiphase, the output of \(\mathrm{IC}_{2 \mathrm{c}}\) is twice the level of each, so that the ripple caused by \(\mathrm{IC}_{5}\) is reduced appreciably (since the interfer-
ing signals are in phase).
The remaining interference signals at the output of \(\mathrm{IC}_{2 \mathrm{c}}\) are inevitable, because they are related to the large tolerances of the memories.

According to data from the manufacturers, the distortion of an MN3008 is 0.5 per cent (average) and 2.5 per cent (maximum), while the amplification may vary up to \(\pm 4 \mathrm{~dB}\) from the nominal value. In the prototype, the use of one memory resulted in a distortion of 06-0.8 per cent at 1 kHz When two memories are used, the distortion drops to below 0.1 per cent. In both measurements, the clock frequency of \(\mathrm{IC}_{5}\) was 40 kHz ( 25 ms delay).

The improvement of the present circuit over the original is particularly noticeable with strong signals, because
the signal-to-noise ratio increases to 63 dB .

The performance may improved even further by matching MN3008s. In the prototype, this reduced the distortion to 0.04 per cent. However, the price of the ics may prove prohibitive for most constructors.

Another way of improving the performance is providing input buffers \(\mathrm{IC}_{1 \mathrm{~b}}\) and \(\mathrm{IC}_{1 \mathrm{c}}\) with an offset compensation control. This requires the availability of a good distortion meter, however.

The bandwidth of the circuit is limited to about 7 kHz by input filter \(\mathrm{IC}_{1 \mathrm{a}}\) and output filter \(\mathrm{IC}_{2 \mathrm{~b}}\). Probably owing to tolerances of the capacitor values, the bandwidth in the prototype is 6.3 kHz . This is not terribly important, however. If desired, the band-
width may be increased by giving \(\mathrm{R}_{2}-\mathrm{R}_{5}\) and \(\mathrm{R}_{24}-\mathrm{R}_{27}\) proportionally lower values. Note that the bandwidth must not become larger than one quarter of the clock frequency, because the slope of the filter skirts does not allow this.

The clock frequency of \(\mathrm{IC}_{5}\) may be set between 30 kHz and 100 kHz with \(\mathrm{P}_{1}\). These values correspond to delays of 33 ms and 10 ms respectively.

The delay line draws a current of about 22 mA .
[T. Giesberts -964119]
* February 1995, p. 26


\section*{faster MCS52 processor}


The difference between the standard MCS52 processors and the deviant DS87C530 from Dallas is that in the latter an instruction is processed in four clock pulses, whereas this takes 12 clock pulses in the former. Moreover, the

\section*{PARTS LIST \\ Capacitors:}
\(\mathrm{C}_{1}, \mathrm{C}_{2}=22 \mathrm{pF}\)
\(\mathrm{C}_{3}, \mathrm{C}_{4}=100 \mathrm{nF}\)

\section*{Integrated circuits:}
\(\mathrm{IC}_{1}=\) DS87C530 (Dallas)
\(\mathrm{IC}_{2}=2\) off row of 20 ic pins

\section*{Miscellaneous:}
\(\mathrm{Bt}_{1}=\) battery, \(3-5 \mathrm{~V}\)
\(X_{1}=\) crystal 32.768 MHz
\(\mathrm{X}_{2}=\) crystal up to 33 MHz
new deviant can work at clock frequencies of up to 33 MHz , which is more than seven times as fast as the standard 8051. Also, the new processor has an additional \(1 / O\) in the shape of a watchdog timer, a real-time clock, 1 kbyte static memory and two serial ports.

A special clock input is provided for the benefit of the real-time clock. There is also an additional input for a back-up battery, via which both the static memory and the clock are powered when the supply is switched off.

The present conversion board simplifies the transfer from a standard 80 xx to a DS87C530. The board has a socket that fits in the original processor socket and a PLCC socket for the new processor. In this way, any 8031,8032 ,


8051 or 8052 may be replaced by the much faster processor.

The IC socket on the board needs to be fitted with long

pins that are simply pushed into the original processor socket. With a \(32-\mathrm{MHz}\) crystal and a DS87C530 fitted, the board becomes a direct replacement for the original processor. If use is made of the new properties, the backup battery may also be added.

A new code must be added to the software, of course, to be able the new facilities to be used. Information as to how the additional hardware may be controlled can be found in the relevant Dallas data sheets.
[A. Rietjens -964118]


\section*{AC millivolt adaptor}


The a.c. millivolt ranges of many inexpensive multimeters have a limited bandwidth, usually only about 1 kHz . The present circuit contains a buffer, a half-wave rectifier, an active potential divider
and a level adjuster.
The bandwidth of the a.c. millivolt ranges is increased to about 40 kHz , which is more than adequate for most applications.

Provided the adaptor is set
up correctly, the maximum measurement error is 4 per cent. The adaptor may be used over the mV range of \(0-1000 \mathrm{mV}\) r.m.s. Its frequency range is 100 Hz to 40 kHz .

Buffer

\begin{tabular}{|c|c|}
\hline PARTS LIST & \(\mathrm{C}_{3}=10 \mathrm{nF}\) \\
\hline Resistors: & \(\mathrm{C}_{4}=47 \mathrm{pF}\) \\
\hline \(\mathrm{R}_{1}, \mathrm{R}_{6}=10 \mathrm{M} \Omega\) & \(\mathrm{C}_{5}=100 \mathrm{nF}\) \\
\hline \(\mathrm{R}_{2}=1 \mathrm{k} \Omega\) & \\
\hline \(\mathrm{R}_{3}, \mathrm{R}_{4}=1.00 \mathrm{k} \Omega, 1 \%\) & Semiconductors: \\
\hline \(\mathrm{R}_{5}, \mathrm{R}_{9}, \mathrm{R}_{10}=100 \mathrm{k} \Omega\) & \(\mathrm{D}_{1}, \mathrm{D}_{2}=\) BAT85 \\
\hline \(\mathrm{R}_{7}=10.0 \mathrm{k} \Omega, 1 \%\) & \(\mathrm{D}_{3}=1 \mathrm{~N} 4148\) \\
\hline \(\mathrm{R}_{8}=12.1 \mathrm{k} \Omega, 1 \%\) & \\
\hline \(\mathrm{R}_{11}=100 \Omega\) & Integrated circuits: \\
\hline \(\mathrm{R}_{12}=10 \mathrm{k} \Omega\) & \(\mathrm{IC}_{1}=\) TLC274 \\
\hline \(\mathrm{P}_{1}=100 \mathrm{k} \Omega\) (see text) & \\
\hline Capacitors: & \begin{tabular}{l}
Miscellaneous: \\
\(\mathrm{Bt}_{1}=9 \mathrm{~V}\) battery with con
\end{tabular} \\
\hline \(\mathrm{C}_{1}=1 \mu \mathrm{~F}\). polystyrene & necting clip \\
\hline
\end{tabular}

\(\mathrm{IC}_{1 \mathrm{~b}}\) guarantees a constant, high input impedance of about \(10 \mathrm{M} \Omega\). The op amp is followed by active half-wave rectifier \(\mathrm{IC}_{1 \mathrm{c}}\). \(\quad \mathrm{A}\) half-wave rectifier is used, since this enables the nonlinear behaviour of the diodes to be compensated. The output signal of the rectifier is averaged by a non-ideal integrator and raised by a factor \(\pi / 2\) by a small amplifier.

The circuit around \(\mathrm{IC}_{1 \mathrm{a}}\) is added to enable power to be derived from a 9 V battery. The op amp is arranged as an active potential divider and provides a low-impedance null at half the supply voltage.

The adaptor is best built on the printed circuit board illustrated (see Readers' Services towards the end of this
issue). Note that \(P_{1}\) may be a standard preset, although a multiturn model is preferred.

There are are two ways of setting up the adaptor. In the first, use a simple bell transformer with an output of about 9 V , across which a potential divider consisting of a \(1 \mathrm{M} \Omega\) resistor and a \(1 \mathrm{k} \Omega\) resistor in series are connected. With the multimeter set to the 50 mV a.c. range, measure the voltage across the \(1 \mathrm{k} \Omega\) resistor, which is about 10 mV . Then, connect the adaptor to the multimeter and set this to the 50 mV d.c. range. Use the adaptor to measure the voltage across the \(1 \mathrm{k} \Omega\) resistor, and adjust \(P_{1}\) until the meter again reads 10 mV . The measurement error may be up to 6 per cent.

The second way is to inject into the adaptor a sinusoidal signal at a level of 10 mV r.m.s. and at a frequency of around 20 kHz . Use a mV meter that can operate at this frequency and measure the output of the adaptor; note the meter reading. Then replace the mV meter by the multimeter and adjust \(P_{1}\) until the same reading is obtained. The measurement error may be up to 4 per cent.

The circuit draws a current of up to 3 mA .
[H. Bonekamp -964031]


\section*{battery indicator LED}

The battery indicator lamp on the dashboard of cars lights when the car's battery is not being charged. The present circuit has a similar function, but it uses an LED instead of a lamp, and it provides rather more information than the existing light.

The LED gives four different indications:
- it flashes slowly to indicate that the battery voltage is below 10 V , which may mean that the battery is
- it is off, indicating a normal state of affairs (battery voltage \(12-15 \mathrm{~V}\) );
- it flashes at a fast rate to show that the battery voltage is \(>15 \mathrm{~V}\) which means a serious defect in the charging circuit-do not drive the car!

The circuit is based on three comparators: \(\mathrm{IC}_{2 \mathrm{a}}, \mathrm{IC}_{2 \mathrm{~b}}\) and \(\mathrm{IC}_{2 \mathrm{c}}\). These stages get their reference voltage from potential divider \(\mathrm{R}_{3}-\mathrm{R}_{6}\), which is supplied by 5 V regu-

1

about to give up the ghost;
- it lights continuously to show that the alternator (in old cars, dynamo) is not charging the battery (sufficiently) (battery voltage \(10-12 \mathrm{~V}\) );
lator \(\mathrm{IC}_{3}\). The reference voltages are likened with a part of the battery voltage set by \(\mathrm{R}_{1}-\mathrm{R}_{2}\). Diodes \(\mathrm{D}_{1}\) and \(\mathrm{D}_{2}\) serve to eliminate any negative voltage peaks.

The output levels of the

comparators are converted to quantities that control the LED by the logic circuit consisting of \(\mathrm{IC}_{2 \mathrm{~d}}\) and the four nand Schmitt triggers in \(\mathrm{IC}_{1}\).

Circuit \(\mathrm{IC}_{1 \mathrm{a}}\) operates as an oscillator at two difference frequencies. When \(T_{1}\) is off, \(\mathrm{C}_{2}\) and \(\mathrm{C}_{3}\) are in series, so that the frequency-determining capacitance of the oscillator is small and the frequency is high. When \(\mathrm{T}_{1}\) conducts, \(\mathrm{C}_{3}\) is short-circuited. The fre-quency-determining capacitance is then larger and the frequency higher. The oscillator is switched on and off by \(\mathrm{IC}_{2 \mathrm{~d}}\).

NAND gates \(\mathrm{IC}_{1 \mathrm{~b}}\) and \(\mathrm{IC}_{1 \mathrm{c}}\), and the OR gates formed by \(D_{3}\) and \(D_{4}\) ensure that the four different states result in the desired operation of \(\mathrm{D}_{5}\).

The circuit is best built on
the printed-circuit board shown in Figure 2 (which, regrettably, is not available ready-made). The completed board is very small, so that will nearly always be possible to find a little space in a car to house it. The LED should, of course, be fitted in a position where it can be clearly seen. It is connected to the board by two lengths of flexible, insulated circuit wire.
[S. Martinsson - 964079]



\section*{logic probe for EPROMS and RAMS}

The probe is a kind of adaptor board that is plugged into the circuit instead of the EPROM or RAM to be tested. The IC is temporarily plugged into the socket on the adaptor board Because of connectors \(K_{1}\) and \(\mathrm{K}_{2}\), all connections are now accessible for testing with a logic analyser. This is a lot more convenient than working with discrete test clips.

The connections to box headers \(K_{1}\) and \(K_{2}\) correspond to those found on Hewlett-Packard logic analysers. Choosing between EPROM and RAM is effected with five jumpers. Bear in mind that the connections are distributed over the box headers in a logical manner. The jumpers shown in the diagram are intended for testing EPROMS; the other jumper positions select a logic sequence for RAMS.

Two logic probes are contained on the board. In the

space reserved for \(\mathrm{IC}_{1}\left(\mathrm{IC}_{2}\right)\) there is no standard IC socket but two long rows of IC pins that protrude at the track side of the board. After they have been soldered in place, the pins can be lengthened with one or more sockets at the track side.

The IC to be tested is mounted at the top of the board onto the two rows of pins. The logic probe is plugged into the socket intended for the IC.

The probe may be used for 32 -pin as well as 28 -pin EPROMS and RAMS.
[A. Rietjens - 964106]

\section*{PARTS LIST}
\(\mathrm{IC}_{1}\left(\mathrm{IC}_{2}\right)=2\) rows of 20 IC pins
\(K_{1}, K_{2},\left(K_{3}, K_{4}\right)=20\)-way box header
5 off jumpers




\title{
wobbulator
}

The characteristics of a loudspeaker cannot be determined (outside a special test room) with a sinusoidal signal, since various frequencies have to be averaged out. Often, noise signals limited to a \(50-60 \mathrm{~Hz}\) band are used.
threshold of \(\mathrm{IC}_{1 \mathrm{a}}\). At that instant, it will be discharged via \(\mathrm{IC}_{1 \mathrm{~b}}\) and \(\mathrm{T}_{1}\), and then the process will repeat itself.

The current source is fairly simple: \(\mathrm{IC}_{2}\) compares the drop across \(\mathrm{R}_{7}\) (reference) with that across the emitter
tion of about \(1 / 3\) octave, which is independent of the frequency set with \(P_{1}\).

The output signal of the vCO consists of needle pulses about \(0.2 \mu \mathrm{~s}\) wide at a rate about 16 times higher than that of the sinusoidal signal.
(bear in mind the \(\times 2\) amplification of the filter).

Capacitor \(\mathrm{C}_{14}\) prevents any d.c. component from reaching the output. Resistor \(\mathrm{R}_{34}\) ensures that this capacitor is charged even when there is no output load.


The present design uses a frequency-modulated sinusoidal signal, which behaves more or less as pink noise, but has the advantage of a stable amplitude. It is ideally suitable for use with the linear sound pressure meter described elsewhere in this issue.

The circuit consists of three parts: a linear voltagecontrolled oscillator-vCO; a sine wave shaper, and a trian-gular-wave generator.

The vco is formed by a sawtooth generator. Capacitor \(\mathrm{C}_{1}\) is charged by constantcurrent source \(\mathrm{IC}_{2}-\mathrm{T}_{2}\). The potential across the capacitor will sooner or later exceed the
resistor of \(\mathrm{T}_{2}\), consisting of \(\mathrm{R}_{3}\) plus \(P_{1}\). Since this resistance is variable, the frequency may be set to \(40-65 \mathrm{~Hz}\) with \(\mathrm{P}_{1}\).

The reference voltage has a triangular-wave shape and is produced by rectangular/triangular-wave oscillator \(\mathrm{IC}_{4}\). Its frequency (wobbulator rate) may be set between 1.5 Hz and 7.5 Hz with \(\mathrm{P}_{2}\).

The output of \(\mathrm{IC}_{4 \mathrm{~b}}\) is at half the supply voltage, so that the ratio \(\mathrm{R}_{7}: \mathrm{R}_{8}\) determines the direct voltage component of the reference voltage.

The triangular voltage across \(\mathrm{R}_{7}\) is used to vary the current through \(\mathrm{T}_{2}\). This results in frequency modula-

This signal is applied to shift register \(\mathrm{IC}_{3}\) via \(\mathrm{IC}_{1 \mathrm{c}}\). The shift register drives a network with weighted currents at a level which ensures that the output voltage is very nearly a sine wave. In this sense, the combination of \(\mathrm{IC}_{3}\) and network \(\mathrm{R}_{15}-\mathrm{R}_{22}\) may be considered a sort of digital-to-analogue converter-DAC.

The final section of the circuit is a 5 th-order Butterworth filter tuned to 100 Hz , which largely suppresses the overtones of the sampling frequency. With carefully selected values of \(\mathrm{C}_{9}-\mathrm{C}_{13}\), the THD +N of the generator in the prototype was \(\leq 0.05 \%\).
The level of the output signal is set with \(P_{3}\) to 1 V r.m.s.

Resistor \(\mathrm{R}_{33}\) protects \(\mathrm{IC}_{5 \mathrm{~b}}\) against highly capacitive loads.

The Schmitt triggers/inverters in \(\mathrm{IC}_{1}\) have quite a spread in hysteresis. This may make it necessary to give \(\mathrm{C}_{1}\) a slightly higher value or to enlarge the control range of \(\mathrm{R}_{3}\) plus \(\mathrm{P}_{1}\).

If the wobbulator is to be used with the sound pressure meter mentioned earlier, it is desirable that the frequency of the vco and filter can be switched between the value of \(40-65 \mathrm{~Hz}\) chosen here and one that is about 10 times as high.

The circuit draws a current of about 21 mA .
[T. Giesberts - 964075]

\section*{electranics anline}

\section*{test and measurement equipment}

Every electronics enthusiast needs test and measurement equipment. Even the most rudimentary electronics workshop should have at least a power supply, a multimeter and an oscilloscope. This sort of equipment is supplied by many specialized firms, in a wide variety of types and price bands. If you are on the lookout for a new test instrument, there's really no need to go out of doors any more to collect catalogues etc. Today, all major suppliers of electronic test and measurement equipment run on-line product overviews on the web, allowing you to see what's on offer, complete with prices and specifications.

Many of you will associate the name Fluke with the great multimeters produced by this company. Fluke's product scope is much larger, however, ranging from calibrators to 'ordinary' oscilloscopes. Over the past few years, Fluke have also released a series of portable equipment sporting graphic displays: the so-called scope meters and graphic multimeters. All these goodies are on display at
www.fluke.com/products.htm.

One of the worlds's largest suppliers of test and measurement equipment is of course Hewlett Packard, a.k.a. 'HP'. Their offerings are overwhelming, and include something in every price band, whether an \(£ 195\) power supply, or an analyser which sets you back some \(£ 40\) k. Have a look around at
www.tmo.hp.com/tmo/bic.
This site allows you to request a catalogue on-line, and even place an order!

Another well-known manufacturer of measurement equipment is Tektronix (a.k.a. 'Tek'), whose multimeters, oscilloscopes, generators and other T\&M jewels may be admired at www.tek.com/Measurement/Prod-ucts/catalog/by-type.html.

Wavetek, too, is a great alternative for various types of advanced measurement and test gear: www.wavetek.com/wwtest.html.

This site allows you to view an extensive overview of the various models. It is also possible to order a catalogue, and request information on a certain piece of equipment.

Although the Japanese manufacturer Yokogawa may not be very well known in Europe, its products are on a par with those of its American and European competitors. The site www.yokogawa.co.jp/YEF/TM.html shows you the product range available for the European market, which includes recorders, digital memory oscilloscopes, function generators and power meters.

Iwatsu is a Far-Eastern manufacturer specialized in digital oscilloscopes featuring extensive operation options. The American branch of Iwatsu presents the technical specifications of some of these oscilloscopes at: www.iwatsu.com \(/ \mathrm{tm}\).html.

Lecroy is an North American company which is also specialized in (digital) oscilloscopes. Lecroy have a branch in Switzerland. The Internet address www.lecroy.com/tm/LecroyTM.htm provides an overview of various LeCroy products, and also allows web surfers to request product information.

Philips seems to have reduced its activities in the field of 'ordinary' test equipment, although a lot of TV test gear is still being produced. Information on these products may be found at www.ptv.dk/cat/index.htm

Finally, a German supplier of excellent test equipment: Rohde \&

\section*{}


Schwartz. This equipment is sure to be of interest to professional electronics engineers. This manufacturer may be found at
www.rsd.de/webpages/21.htm
In case you are looking for other suppliers of T\&M equipment, Internet search engines like AltaVista and Lycos are a great help in locating addresses and other useful information.

Model cars, boats and airplanes may go out of control, causing serious danger and damage when a failure occurs in the radio control system. This circuit helps to prevent such mishaps by taking over the control of, for example, the accelerator/brake servo in a model car when the radio signal fails. The servo is then set to a predetermined position, for example, brake hard. The circuit may be inserted in any servo link.

The heart of the circuit is an astable multivibrator (AMV) consisting of Schmitt trigger gates IClc and ICld. When the receiver pulses fail, the AMV generates replacement servo pulses whose width may be set with preset P1. Capacitor C4 then determines the 'off' time (approx. 20 ms ), and C3, the 'on' time ( \(1.5 \mathrm{~ms} \pm 0.5 \mathrm{~ms}\) ).

During normal operation of the radio link, the received pulses are negated by ICla, which discharges C2 via D1, so that IC1d is disabled. The result is that the servo pulses supplied by the receiver are available again at the output of the circuit.

When the receiver pulses disappear, C2 is no longer discharged, and the AMV is enabled. It starts to oscillate, sup-

\section*{radio failure protection for R/C models}
plying replacement pulses which cause the servo to turn to the predefined position.

The circuit may also be used as a stand-alone tester for servo motors. Current consumption in transparent mode is about \(20 \mu \mathrm{~A}\) at a supply voltage of 5 V , or \(50 \mu \mathrm{~A}\) when the AMV is active.
[Design by B. Sommer 964010]
COMPONENTS LIST
Resistors:
R1 \(=47 \mathrm{k} \Omega\)
R2 \(=220 \mathrm{k} \Omega\)
\(\mathrm{R} 3=27 \mathrm{k} \Omega\)
\(\mathrm{R} 4=120 \mathrm{k} \Omega\)
\(\mathrm{P} 1=50 \mathrm{k} \Omega\) preset H

\(\mathrm{Capacitors}:\)
\(\mathrm{C} 1, \mathrm{C} 2=470 \mathrm{nF}\)
\(\mathrm{C} 3=47 \mathrm{nF}\)
\(\mathrm{C} 4=22 \mathrm{nF}\)
\(\mathrm{C} 5=10 \mu \mathrm{~F} 63 \mathrm{~V}\) radial
\(\mathrm{Semiconductors}:\)
\(\mathrm{D} 1=1 \mathrm{~N} 4148\)
\(\mathrm{IC} 1=4093\)

\section*{Miscellaneous:}

Printed circuit board not available ready-made through the Readers Services


\section*{doorbell limiter}

This circuit ensures that impatient callers or naughty children cannot make an electric doorbell ring continuously. It limits the time the bell can be actuated to one second, followed by a pause of \(10-15\) seconds.

When the bellpush is pressed, the alternating voltage powering the bell is rectified by \(\mathrm{D}_{1}\) and smoothed by \(C_{2}\). Since \(C_{1}\) is not charged, transistor \(T_{1}\) is off owing to the high voltage level at its collector. Transistor \(\mathrm{T}_{2}\) comes on and this results in the relay being energized. The circuit is closed and the bell rings.

Capacitor \(\mathrm{C}_{1}\) is then being charged via \(D_{2}\) and \(R_{2}\). When the potential across \(\mathrm{C}_{1}\) has risen sufficiently to cause \(T_{1}\)

to conduct, transistor \(\mathrm{T}_{2}\) will be cut off. This results in the relay being deenergized, so that the voltage is removed
from the bell.
Capacitor \(\mathrm{C}_{1}\) is then discharged slowly via \(R_{3}\) and the base-emitter junction of \(T_{1}\).

When the potential across it has has dropped to a certain level, which takes \(15-20\) seconds, \(\mathrm{T}_{1}\) is cut off again, so that the bell is powered once more.

Impatiently pressing the bellpush before \(\mathrm{C}_{1}\) has been discharged sufficiently causes the capacitor to be charged, so that it takes a further \(10-15\) seconds before the bell rings.

The charging time of \(\mathrm{C}_{1}\) is determined to a large extent by the value of \(\mathrm{R}_{2}\). The time required for the bell to be powered depends largely on the value of \(\mathrm{R}_{3}\). Both times can be lengthened by making \(\mathrm{C}_{3}\) larger.
[M. Vohburger - 964006]


\section*{Casio interface}


Modern organizers, portable databanks, and mini computers are often considerably more than ingenious devices for playing games. They become even more useful if they can be linked to a PC. Most organizers from Casio have a \(3-\mathrm{mm}\) socket for this purpose.

The socket gives access to a kind of RS232 interface in which the levels are TTL. \((0 \mathrm{~V}\) and +5 V ) instead of the usual \(\pm 12 \mathrm{~V}\). Thanks to this socket, the simple circuit in the diagram and some DIY software make it possible for the organizer to communicate
with a fully fledged PC.
The circuit draws only a tiny current, which is determined primarily by the op amp. In the present circuit it is about 1 mA .

The positive supply is derived via pins 7 and 8 of the RS232 connector on the PC.

Since the negative voltage \((-10 \mathrm{~V})\) is present at pins 3 and 4 of the RS232 connector only during intervals, diodes \(\mathrm{D}_{2}, \mathrm{D}_{3}\) and capacitor \(\mathrm{C}_{1}\) ensure continuity of the negative line for the interface.

Data reach the organizer via \(\mathrm{IC}_{1}\) a, here arranged as an
inverting comparator. The signal level at the input is likened to the reference voltage of 0.7 V at the non-inverting input of the op amp.

The output signal of \(\mathrm{IC}_{1 \mathrm{a}}\) is applied directly to the RS232 connector.

The RS232 signals applied to the organizer are limited to \(\pm 10 \mathrm{~V}\) by \(\mathrm{R}_{4}\) and \(\mathrm{R}_{5}\) and then compared with the reference voltage. Since the output voltage of the op amp switches between \(\pm 10 \mathrm{~V}\), network \(\mathrm{R}_{3}-\mathrm{D}_{4}\) ensures that it is limited to 0 V and +5 V .

Because some computer
manufacturers do not rigorously follow the RS232 norm, it may in certain cases be necessary to adapt the hardware to some extent.

As far as software is concerned, the standard communication programs for PCS use a different protocol. It is, therefore, necessary to find out how the original Casio software works: observe the signals at the serial interface. Once these are known, it should not be too difficult to arrange a simple program.
[G. Klein -964017]


It is clear that power consumption may be reduced if ancillary equipment is on only when the master unit is switched on. This is, for instance, the case in an audio system where the amplifier may be considered the master unit. It does not make sense to have the tuner, cassette deck and CD player on standby when the amplifier is switched off. This is true also in computer systems, which, apart from the computer, normally contain at least a monitor, a printer, external drive, and, perhaps, a scanner. It would be very user-friendly and energyfriendly if all those units were switched on and off together with the computer.

In a computer system, this is arranged fairly easily, since the mains voltage for the monitor is
often taken from a special (switched) mains outlet at the back of the computer. If a mul-
tiple extension socket is plugged into this outlet and the various ancillary units connected to the
extension outlets, our aim has been achieved.
[K. Walraven - 964011]

To determine whether two capacitances are equal or not, the comparator measures the change in period of a triangular oscillator into whose circuit the two capacitances are alternately connected.

In the circuit diagram, \(C_{\mathrm{x} 1}\) and \(C_{\mathrm{x} 2}\) are the two capacitances that need to be compared. They are connected to the circuit via flexible circuit wire.

Transistors \(\mathrm{T}_{1}\) and \(\mathrm{T}_{2}\) form current sources that alternately charge \(C_{\mathrm{x} 1}\) and \(C_{\mathrm{x} 2}\). The voltage drop across the capacitors, \(U_{\mathrm{c} 1}\) and \(U_{\mathrm{c} 2}\) respectively, is applied to a Schmitt trigger. The output of \(\mathrm{IC}_{1 \mathrm{~b}}\) remains stable until one of the voltages exceeds the switching threshold of \(\mathrm{IC}_{\mathrm{la}}\), when it changes state.

When the output of \(\mathrm{IC}_{1 \mathrm{~b}}\) is high, \(\mathrm{T}_{2}\) provides just a little more current than \(\mathrm{T}_{1}\), which causes the connected capacitor to be discharged. If the output is low, the relevant capacitor is charged.

It is imperative that the change-over from one capacitor to the other happens at exactly the end of an oscillator period, for instance, when the output of \(\mathrm{IC}_{1 \mathrm{~b}}\) changes state.

D-bistable \(\mathrm{IC}_{2 \mathrm{a}}\) is arranged as a binary scaler which produces a pulse whose width is equal to the oscillator period.

\section*{capacitance comparator}


When pin 1 of \(\mathrm{IC}_{2 \mathrm{a}}\) is high, the period is determined by \(C_{x 1}\). When it is low, the period is determined by \(C_{\mathrm{x} 2}\).

Circuit \(\mathrm{IC}_{2 \mathrm{a}}\) drives two ana-
logue switches, \(\mathrm{IC}_{3 \mathrm{a}}\) and \(\mathrm{IC}_{3 \mathrm{~b}}\), which alternately connect \(C_{\mathrm{x} 1}\) and \(C_{\mathrm{x} 2}\) to the oscillator.

The amount of hysteresis of a 40106 depends largely on
the maker: in a Philips device, it is typically 1.8 V , whereas in an SGS-Thomson device, it is typically 3.5 V . Such differences in hysteresis do not ad-
\begin{tabular}{|c|c|c|c|}
\hline PARTS LSt & \(\mathrm{C}_{1}=\mathrm{C}_{\mathrm{x} 1}\) & & \(\mathrm{IC}_{3}=4066\) \\
\hline Resistors: & \(\mathrm{C}_{2}=\mathrm{C}_{\mathrm{x}}\) & Semiconductors: & \(1 \mathrm{C}_{4}\) - TLC272CP \\
\hline \(\mathrm{R}_{1}=10 \mathrm{k} \Omega\) & \(\mathrm{C}_{3}=3.9 \mathrm{pF}\) & \(\mathrm{T}_{1}=\mathrm{BC} 557 \mathrm{~B}\) & \\
\hline \(\mathrm{R}_{2}-\mathrm{R}_{5}=562 \Omega, 1 \%\) & \(\mathrm{C}_{4}=5 \mathrm{pF}\) trimmer & \(\mathrm{T}_{2}=\mathrm{BC} 547 \mathrm{~B}\) & Miscellaneous: \\
\hline \(\mathrm{R}_{6}, \mathrm{R}_{7}=10.0 \mathrm{k} \Omega, 1 \%\) & \(\mathrm{C}_{5}, \mathrm{C}_{6}=2.2 \mu \mathrm{~F}\), polystyrene, & & \(\mathrm{JP}_{1}=3\)-way pin header with \\
\hline \(\mathrm{R}_{8}, \mathrm{R}_{9}=1 \mathrm{M} \Omega\) & pitch 5 mm
\[
\mathrm{C}_{7}-\mathrm{C}_{10}=100 \mathrm{nF}
\] & Integrated circuits:
\[
\mathrm{IC}_{1}=40106
\] & jump lead (see text) \\
\hline Capacitors: & \(\mathrm{C}_{11}=100 \mu \mathrm{~F}, 25 \mathrm{~V}\) & \(\mathrm{IC}_{2}=4013\) & \\
\hline
\end{tabular}

versely affect the comparator, but they do cause a shift in the measuring frequencies.

If the capacitances are equal, the duty factors of the signals at pins 1 and 2 of \(\mathrm{IC}_{2}\) a must also be equal. Therefore, the pulse/pause ratio at the output of \(\mathrm{IC}_{2 \mathrm{a}}\) is directly proportional to the ratio of the capacitances. Averaging the two outputs of the binary scaler and comparing them, which is carried out by \(\mathrm{IC}_{4 \mathrm{a}}\) and \(\mathrm{IC}_{4 \mathrm{~b}}\), gives an accurate
determination of the difference between the two capacitances: 75 mV per per cent.

Time constants \(\mathrm{R}_{8}-\mathrm{C}_{5}\) and \(\mathrm{R}_{9}-\mathrm{C}_{6}\) are deliberately made large to provide a continuous measurement range from 220 pF to 220 nF .

Use a \(4^{1 / 2}\)-digit multimeter ( 20 V range) or a \(31 / 2\)-digit model ( 2 V range). The maximum voltage difference is 15 V . With capacitance values below 220 pF , the mutual differences result in a lower and
lower potential difference. This is because of the parasitic capacitance, which is about 35 pF . The effect of this capacitance is lessened by trimmer \(\mathrm{C}_{4}\).

Calibrating the circuit is simple: place jumper \(\mathrm{JP}_{1}\) and adjust \(\mathrm{C}_{4}\) until the output voltage is zero. If this cannot be done, set \(\mathrm{JP}_{1}\) to the other position.

With capacitance values above 220 nF , the frequency becomes very low. Also rip-
ples are caused across \(\mathrm{C}_{5}\) and \(\mathrm{C}_{6}\), which are out of phase. This causes the meter reading to become unstable.

The measurement frequency extends from about \(21 \mathrm{~Hz}(220 \mathrm{nF})\) to 18 kHz \((220 \mathrm{pF})\). If measurements are required up to \(2.2 \mu \mathrm{~F}, \mathrm{R}_{6}\) and \(\mathrm{R}_{7}\) may be lowered to \(1 \mathrm{k} \Omega\).

The circuit draws a current of about 10 mA .
[K Giesterts 964089]

Remote control transmitters come in countless different shapes and for many different functions. They are also so cheap and beautifully styled that most of you will not even contemplate home construction from scratch as that would probably result in an ungainly box which is not at all easy to

\section*{personal RC5 infra-red remote control}

The crux is to change the resonator frequency of the transmitter. As an example, a creditcard size RC5 compatible remote control was modified by removing the existing \(432-\mathrm{kHz}\) resonator and replacing it with a

SAA3009 based receivers (note: the SAA3009 is no longer manufactured, it may be replaced by the pin compatible SAA3049). Actually, the circuits are based on the input stage of the Gen-eral-Purpose Infra-Red Volume
within \(10 \%\) of the theoretical value. The SFH506-40 has a bandpass filter at 40 kHz instead of 36 kHz , and is thus better matched to the new modulation frequency. The result is a considerable increase in the dis-

credit card
remote control

hold in one hand!
Here's an idea how to make your own, personalized, remote control transmitter which will control only those receivers that have been modified accordingly.
\(503-\mathrm{kHz}\) type. This results in a higher modulation frequency of approximately 42 kHz instead of the standardized 36 kHz , while the pulse rate increases, too. To enable standard RC5 receiver ICs like the SAA3049 and SAA3009 to recognize a valid signal, the crystal frequency has to be changed.

The two diagrams show the modifications for SAA3049 and

Control described in the July/August 1994 issue of Elektor Electronics. Twelve resistors are added, while one is omitted, as well as two capacitors. The IR receiver is replaced by the Siemens SFH506-40, and the crystal by a \(5-\mathrm{MHz}\) type. The resulting clock frequency actually causes a receive pulse rate which is a little too high. Fortunately, everything still functions normally if the data speed is
tance that can be covered with the remote control.

A receiver modified as described here will no longer respond to signals transmitted by normal ( \(36-\mathrm{kHz}\) ) RC5 remote controls. The reverse situation is slightly less favourable: a standard receiver will respond to a modified transmitter only at distances smaller than 30 cm or so.
[Design by T. Giesberts -964041]

\section*{silent volume control}

There is a growing tendency to fit audio equipment with electronic volume controls (virtually always remote controlled). This consists of a series of potential dividers actuated by electronic switches. Regrettably, this setup has a small drawback: faint click are sometimes heard when the volume is changed. These clicks are the result of the brief shortcircuit of the multiplexers in 4000 series cmOs ics to the negative supply line when they are switched over.

In the quad audio switch Type SSM2404 from Analog Devices this flaw is obviated by break-before-make logic drive circuits and by switching the output transistors gradually via

a sawtooth generator. This switch has further benefits in that \(\mathrm{R}_{\text {DSon }}\) is low and that it can operate from a high supply voltage (up to 13.5 V ).

Since break-before-make electronic switches are used, it is not possible to construct a volume control from a potential divider with several branches followed by a buffer stage. This is

because the switches in series with the buffer would briefly not have a bias setting when switching takes place. Therefore, the present design uses an inverting amplifier with a virtual ground. The total amplification is -1 , but that may be changed by altering the value of \(\mathrm{R}_{17}\).

The voltage divider is designed for steps of 1.25 dB , so that an attenuation of \(0-8.75 \mathrm{~dB}\)
is possible. Resistor values for a total range of 70 dB are given in the table. Connecting two of these circuits (one with a range of 8.75 dB , and the other with a range of 70 dB ) in series gives a volume control with a range of 0 dB to -78.5 dB . The volume control may be driven by a 6 -bit counter or a microprocessor.

In the diagram, the switches of one chain of attenuators are
driven by a BCD-to-decimal decoder Type 4028. The attenuation may be set manually with DIP switch \(\mathrm{S}_{1}\). Resistor \(\mathrm{R}_{18}\) and diodes \(\mathrm{D}_{1}, \mathrm{D}_{2}\) serve as overdrive protection for \(\mathrm{IC}_{1}\) and \(\mathrm{IC}_{2}\). These components may be omitted between two successive attenuator sections.

As far as the d.c. setting of the circuit is concerned, it suffices to state that the level at all points in the output condition (all DIP switches open) is 0 V . except at pin 6 of \(\mathrm{IC}_{2}\), which is at +12 V .

The maximum undistorted input voltage is 7.6 V r.m.s. In the prototype, the THD+noise with an input voltage of 2 V r.m.s. was \(0.0007 \%\) at 1 kHz and \(0.0009 \%\) at 20 kHz . At the largest attenuation \((-8.75 \mathrm{~dB})\) this figures rose to \(0.001 \%\) and \(0.0016 \%\) respectively. The overall bandwidth of the amplifier is 200 kHz . The current drain of a complete attenuator section is about 6 mA .
[T. Giesberts -964029]
\begin{tabular}{|c|c|}
\hline \begin{tabular}{c} 
Table 1. Resistor values for a \\
range of \(\mathbf{0} \mathbf{d B}\) to \(\mathbf{- 7 0} \mathbf{d B}\).
\end{tabular} \\
\hline\(R 1\) & \(6.04 \mathrm{k} \Omega\) \\
\hline\(R 2\) & \(2.80 \Omega\) \\
\hline\(R 3\) & \(768 \Omega\) \\
\hline\(R 4\) & \(226 \Omega\) \\
\hline\(R 5\) & \(69.8 \Omega\) \\
\hline\(R 6\) & \(21.5 \Omega\) \\
\hline\(R 7\) & \(6.81 \Omega\) \\
\hline\(R 8\) & \(3.16 \Omega\) \\
\hline
\end{tabular}

\section*{defect-fuse indicator}

In certain cars, caravans and campers fuses are often located in a most awkward place. Where this is so, the present indicator may be of help, since it enables a fuse to be checked without having to remove it from its holder.

The circuit is very simple: a signal diode, a resistor and an LED. Its operation is just as simple. If the fuse is all right,
diode \(D_{2}\) is practically in parallel with \(D_{1}\), since the very small resistance of the fuse may be ignored. The potential drop across \(D_{2}\) is about 0.6 V , but since \(\mathrm{D}_{1}\) needs about 1.6 V to light it remains dark. If, however, the fuse is defect, \(D_{2}\) is no longer in parallel with \(D_{1}\), so that this lights. It does not matter whether the lamp shown in
the diagram is switched on or not. If it is on, \(D_{2}\) is reversebiased, so that the LED is powered via \(\mathrm{R}_{3}\). Since the resulting current flows continuously, the value of \(\mathrm{R}_{3}\) is chosen to ensure that with a battery voltage of 12 V it does not exceed 1.9 mA . This level of current is quite sufficient for a low-current LED.
[W. Cohaupt - 964109]


\title{
stroboscope for motorcycles
}


The stroboscope is especially intended for use on motorcycles with electronic ignition. It has a fixed duty factor (pulse/ pause ratio), so that, irrespective of the engine speed, the LEDS light the flywheel at a fixed distance of \(1-2^{\circ}\). The output is buffered. The output voltage is directly proportional to the engine speed.

The circuit is powered by the motorcycle battery: \(\mathrm{IC}_{1}\) stabilizes this at 10 V .

Ignition pulses are detected by \(\mathrm{L}_{1}\), a coil of 100 turns with a diameter of 30 mm , which is pushed over the plug cable. The potential induced in the coil is damped by \(\mathrm{R}_{11}\). This resistor may be replaced by a \(1 \mathrm{k} \Omega\) poten-
tiometer if variable sensitivity is desired.

The induced pulses (width about \(5 \mu \mathrm{~s}\) ) appearing at the collector of \(\mathrm{T}_{3}\) are applied to monostable \(\mathrm{IC}_{2 \mathrm{~b}}\). The monostable is not retriggerable and reacts to the trailing edges of the pulses; this ensures that any noise pulses following the ignition pulses cannot upset the circuit.

One of the outputs of \(\mathrm{IC}_{2 \mathrm{~b}}\) is used to charge \(\mathrm{C}_{5}\). The potential across \(\mathrm{C}_{5}\) is thus directly proportional to the engine speed. It is buffered and then led out via \(\mathrm{IC}_{3 \mathrm{~b}}\) to drive a multimeter or moving-coil meter.

The other output of \(\mathrm{IC}_{2 \mathrm{~b}}\) drives a second monostable, \(\mathrm{IC}_{2 \mathrm{a}}\). The duty factor of this monostable is held constant by integrator \(\mathrm{IC}_{3 \mathrm{a}}\) and current source \(\mathrm{T}_{1}\). The control range extends from 1 Hz to 50 Hz . The pulse/pause ratio is set with \(\mathrm{P}_{2}\).

The Q-output of \(\mathrm{IC}_{2 \mathrm{a}}\) drives 12 Leds via emitter follower \(\mathrm{T}_{2}\). With values of \(\mathrm{R}_{1}-\mathrm{R}_{4}\) as specified, the peak current through the LEDS is about 30 mA . The light intensity of the diodes can be increased by reducing the values of the four resistors to \(68 \Omega\).

The stroboscope is set up with the use of the output voltage of a \(5-\mathrm{V}\) transformer or mains adaptor as test signal. Connect this signal to the input of the stroboscope via a \(1 \mathrm{k} \Omega\) resistor and adjust \(P_{1}\) to obtain an output voltage of 6 V in case of a two-stroke motorcycle, or to 3 V in case of single-stroke machine. Then, adjust \(\mathrm{P}_{2}\) for a pulsewidth across the LEDs of \(30 \mu\) s or \(60 \mu\) s respectively.

The unit is best built on the printed-circuit board shown. The design of the board allows the section in-


tended for the LeDs to be cut off to give greater flexibility in fitting the stroboscope. The unit should be fitted in a metal case to reduce spurious radiations.

In the prototype, the LEDS were covered by a perspex magnifier. The diodes were bent inwards to such an extent that a clear point of light was obtained about 80 mm above the magnifying perspex. This extra work is well worth it, particularly since the light output of the LEDS with the short duty factor is small.

A tip before you start: clearly identify the marks on the flywheel with Tipp-Ex \({ }^{\text {n }}\) or white paint and screen the flywheel as much as possible from ambient light.
[E.M.v.d.Eb - 964088]


\section*{sound pressure meter}

The design, consisting of an electret microphone, amplifier, and moving-coil meter, arranges for the meter to give a reading that is linearly proportional to the sound pressure. Sound pressure meters usually have a logarithmic scale, but this would make the design more complicated. Moreover, linear proportionality results in greater sensitivity to sound pressure differences. If a test CD with noise bands in \(60-\mathrm{Hz}\) steps is available, the meter may be used to obtain a frequency characteristic of a loudspeaker.

The microphone is a Type MCE2000 electret from Monacor. The operating point of the FET contained in this is set with \(R_{1}\). Resistor \(R_{2}\) and capacitor \(\mathrm{C}_{2}\) prevent noise on the supply lines from reaching the input.

The operating point of op amp \(\mathrm{IC}_{1 \mathrm{a}}\) is set to half the supply voltage with \(R_{3}\) and \(\mathrm{R}_{4}\).

The degree of amplification is determined by the ratio of \(\mathrm{P}_{1}\) to the output impedance of the microphone. With component values as specified in the circuit diagram, the amplification is \(\times 60\), which makes a 90 dB sound pressure result in fullscale deflection of the meter.

In the prototype, \(\mathrm{P}_{1}\) is then roughly at the centre of its travel.
input of the op amp. Note, by the way, that the voltages shown in the circuit diagram are taken from the prototype.


Capacitor \(\mathrm{C}_{1}\) is a bipolar electrolytic type, since the spread of the FET in the mi crophone may cause the voltage at metering point B to be lower than the 4.5 V at the

Half the supply voltage is buffered by \(\mathrm{IC}_{1 \mathrm{~b}}\), so that the circuit can be driven by \(\mathrm{IC}_{1 \mathrm{a}}\) without any difficulty. The buffering makes an additional potential divider in the meter-
ing circuit superfluous; this is a benefit, because such a divider affects the meter deflection and increases the current drain.

The meter, M , is a \(30 \mu \mathrm{~A}\) moving-coil type with an internal resistance of \(6.5 \mathrm{k} \Omega\). The use of a meter with as low a current drain as possible keeps the voltage drop across bridge rectifier \(\mathrm{D}_{1}-\mathrm{D}_{4}\) low. Resistor \(\mathrm{R}_{5}\) and diode \(D_{5}\) limit the peak current through the meter.

The current drain of the complete circuit is only 1.5 mA .

The use of a wobbulator and the present meter enables, say, a subwoofer to be matched to an existing system. First measure the standard speakers at a frequency of \(400-500 \mathrm{~Hz}\), wobbulated over \(1 / 3\) octave. The level of the signal must be high enough to suppress ambient noises. Adjust \(\mathrm{P}_{1}\) for maximum meter reading. The, apply a \(40-50 \mathrm{~Hz}\) signal to the subwoofer and adjust the active filter in the amplifier or subwoofer for an identical meter reading. These measurements should be taken at a distance of about \(1 \mathrm{~m}(3 \mathrm{ft})\) from the loudspeakers.
[T. Giesberts -964074]

This circuit converts a serial pulse train into a sinusoidal output voltage consisting of 30discrete steps. The 4 -bit output of up/down counter IC1, \(\mathrm{Q}_{\mathrm{A}}-\mathrm{Q}_{\mathrm{D}}\), is applied to the inputs of a 4-to-16 line demultiplexer, IC3. Counter IC1 supplies binary codes that repeatedly scan the range 0000 through 1111, and then back to 0000 again.
The up/down ( \(\overline{\mathrm{U}} / \mathrm{D}\) ) input pin of the counter is controlled by the Qoutput of a bistable, IC2a. The reset input of the bistable and the load input of the counter are connected to a power-on reset network, R2C 1 , to provide a defined count state at power-on.

Each of the 15 demultiplexer outputs used here is connected to a precision resistor. Only one demultiplexer is low at a time, requiring the weighing factor of the resistors to be made such that the total current is sinusoidal (in theory) relative to a \(2.5-\mathrm{V}\) reference potential set up at the - input of IC4 by resistors R19 and R21. The value of R20 brings the swing of the digitized sine-wave into the output voltage range of the TLC271. The output voltage level is set to \(1 \mathrm{~V}_{\mathrm{rms}}\) by R22.

The theoretical values of R3

\section*{pulse train to sine wave converter}

through R17 are rounded off to the nearest available values in the E96 series. Unfortunately the resulting deviations cause a less than perfect shape of the
sine-wave. The overall result is quite acceptable, though, for most practical purposes.

The maximum input frequency that may be applied to
the circuit is about 3 MHz , while the overall scaling factor is 30 . The circuit draws about 3 mA from a regulated \(5-\mathrm{V}\) supply.
[Design by H. Bonckamp - 964072]

\section*{a.f. generator}

The generator produces a sinusoidal signal at a frequency of about 1 kHz . This makes it suitable for use in a variety of measurements, such as the testing of an a.f. amplifier.

The operation of the circuit is based on selective phase shifts. Each of \(R C\) networks \(\mathrm{R}_{1}-\mathrm{C}_{1}, \mathrm{R}_{2}-\mathrm{C}_{2}\), and \(\mathrm{R}_{\mathrm{x}}\) \(\mathrm{C}_{3}\) introduces a phase shift of \(60^{\circ}\), resulting in a total shift of \(180^{\circ}\). Transistor \(\mathrm{T}_{1}\) adds a further \(180^{\circ}\), so that the circuit as a whole gives a phase shift of \(360^{\circ}\). This is one of the two requirements of an oscillator.

Resistance \(\mathrm{R}_{\mathrm{x}}\) is the input impedance of transistor \(T_{1}\), which is about \(4.7 \mathrm{k} \Omega\), that is, roughly equal to \(R_{1}\) and \(R_{2}\).

The second requirement of an oscillator is the positive

\(f_{o}=\frac{1}{2 \cdot \pi \cdot \sqrt{6} \cdot R \cdot C}=\frac{1}{2 \cdot \pi \cdot \sqrt{6} \cdot 4.7 \cdot 10^{3} \cdot 12 \cdot 10^{-9}}=1.15 \mathrm{kHz}\).
feedback provided by \(P_{1}\). This potentiometer sets the amplification of \(T_{1}\) and thus the
output voltage level of the generator.

The oscillator frequency,
\(f_{\mathrm{o}}\), is determined solely by the values of the three \(R C\) networks: with values as specified, it is 1.15 kHz :
\[
f_{\mathrm{o}}=1 / 2 \pi 6 R c
\]

The collector voltage of \(\mathrm{T}_{1}\) is applied to the output of the generator via emitter follower \(\mathrm{T}_{2}\).

For optimum operation, \(P_{1}\) must be adjusted to give an output voltage of \(2.5 \mathrm{~V}_{\mathrm{pp}}\), that is, 1.78 V r.m.s.

The total harmonic distortion, THD, is better than -30 dB .

The circuit draws a current of about 6 mA .
[H. Bonekamp - 964064]

\section*{Ioudspeaker protector}

This circuit automatically disconnects a mid-range loudspeaker or a tweeter from the output of an amplifier when too much power is applied. A relay with a normally closed ( \(\mathrm{n} / \mathrm{c}\) ) contact is used as the switching device.

The relay coil voltage is derived from the loudspeaker signal with the aid of bridge rectifier, B 1 . A current source, T 2 , is used to ensure a reasonably constant coil current. To ensure that the maximum coil current does not depend too much on level of the loudspeaker signal, the voltage across R2 is limited to about 1.2 V by an LED, D2. The maximum energizing current is then about 66 mA . The 6 -V Siemens relay used here has a coil resistance of about \(80 \Omega\). To keep the extra load on the amplifier to a minimum, the relay receives a coil voltage which is a little below the nominal value. Remember, the circuit draws current even when the relay is not energized! Fortunately, the current consumption is negligible at signal levels up to \(5 \mathrm{~V}_{\text {peak }}\).

The AD8037 is a rather special opamp because its positive and negative inputs have internal clamps. The clamp at the negative input is essential for the operation of the circuit shown here, which does not work with any conventional opamp fitted instead of the AD8037.

According to Analog Devices, the full-wave rectifier works well up to 20 MHz . The distortion is significantly lower than that of diode-based fullwave rectifiers, especially at high frequencies. Applications of the circuit include AM signal detection, high-frequency a.c. voltmeters and various arithmetic operations.

When the negative halfcycle is applied, the circuit acts as a regular unity gain inverting amplifier ( \(\alpha=-\) \(R 5 / R 3=-1\) ). When the signal is positive, the negative clamp prevents current flow through the feedback circuit. This is

The saturation current which flows through the J-FET current source, T1, is about 4 mA , enabling a low-current LED to act as a visual 'overload' indicator. Turn the volume down when the LED lights! A zener diode is connected in series with the current source and the LED to define
the threshold at which the relay toggles. The zener value shown here results in an actuation level of about 7.5 V , or about 8.5 W into \(8 \Omega\). The loudspeaker is connected again at a power level of about 3.5 W . Note that these are average power levels, so you may get quite different results when

testing with music or white noise ( 13 W off, 5 W on). Network R1-C1 is a rudimentary peak detector which helps to improve the response of the circuit to noise.

The circuit works fine from a frequency of about 60 Hz . At lower frequencies, the relay may chatter. The protection is, therefore, mainly suitable for mid-range drive units and tweeters.

If you want to use the protection for higher signal levels, it is recommended to use a 12 V relay, and change the value of R2 according to \(\mathrm{R} 2=1.2 \mathrm{~V} / \mathrm{I}_{\text {(nom) }}\)
where \(\mathrm{I}_{\text {nom }}\) is the nominal coil current of the relay. The calculated value of R2 is then rounded off to the nearest (higher) E12 value.

FET T1 limits the maximum permissible input voltage to about 38 V . Current consumption of the protector is about 70 mA when actuated. The indicated test voltages apply to that state.
[Design by T . Giesberts -964077]

\section*{high-speed full-wave rectifier}

achieved by driving the positive input (behind the clamp) with the same signal as the negative input. Consequently the output signal is then a
copy of the input signal.
A possible problem is the input impedance variation caused by the clamp action. As soon as the clamp is actuated,
the - input receives the same signal as the input of the circuit, so that the input impedance rises from the value of R3 to a much higher value. The rectifier should, therefore, be driven from a source with a very low impedance.

The symmetry of the output voltage is tweaked using preset P1. The positive input is only active as long as the negative clamp is not actuated. In other words, only when the input signal is negative.

The other preset, P 2 , is used to null the output offset voltage. This preset controls the offset via the negative input, so it is active during the entire input signal.

Current consumption of the fast rectifier is about 25 mA . The measured effective bandwidth is greater than 5 MHz . The input voltage should be smaller than \(2.8 \mathrm{~V}_{\text {peak }}\).
[Source: Analog Devices - 964078]

\title{
Centronics I/O port
}


The printer port of a PC may be misused simply as a digital \(\mathrm{I} / \mathrm{O}\) interface. The present circuit provides 32 outputs and 20 inputs.

When the printer port is used as an output, the software deals with an 8-bit data word and a 4-bit control word. When it is used as an input, a 5 -bit status word comes into play. The software locates these three registers at the data address, the control address and
the status address respectively.

The data word can be processed in two ways. If it is used for selecting a group of \(\mathrm{I} / \mathrm{o}\) lines, it is stored in \(\mathrm{IC}_{2}\). If it concerns the data that have to appear at the output, these are stored in \(\mathrm{IC}_{1}\).

Storing in \(\mathrm{IC}_{2}\) occurs at the command of the strobe pulse. The output signals of \(\mathrm{IC}_{2}\) are used for selecting the various \(1 / 0\) elements. To this end, the output signal is split into two nibbles. One of these goes to the 3 -to- 8 converter \(\left(\mathrm{IC}_{3}\right)\); the other provides the four control signals for the enable inputs of \(\mathrm{IC}_{4}-\mathrm{IC}_{7}\). Since the output signals of \(\mathrm{IC}_{3}\) can be switched with the aid of the auto signal, it is readily possible to address the same input and output.

REM
REM . . . . ............................ DEFINE ADDRESSES, CLEAR SCREEN ADDRESS \(=8 H 378\) : REM SEL. PRINTER PORT ADDRESS \(\& \mathrm{H} 278 / \mathrm{sH} 378 / \mathrm{sH} 3 \mathrm{BC}\) CLS
PORT \(=0:\) INOUT \(=6\) HFF \(-8:\) REM ADDRESS MULTIPLEXER ENABLED DATAADDRESS \(=\) ADDRESS
STATUSADDRESS \(=\) ADDRESS +1
CONTROLADDRESS \(=\) ADDRESS +2
REM . . . . . . . . . . . . . . . . . . . . . . SAVE OLD OUTPUTS
OLDDATA \(=\) INP(DATAADDRESS)
OLDREG2 \(=\) INP (CONTROLADDRESS)
OUT CONTROLADDRESS, \&HFD:
REM REM INITIAL CONTROL SETUP
.. TEST ROUTINES
FOR PORT \(=0\) TO 3
GOSUB ENABLEPORTOUT:
GOSUB OUTPUTTEST:
GOSUB DISABLEPORTOUT:
NEXT PORT
FOR PORT \(=4\) TO 7
GOSUB DISPLAY:
GOSUB INPUTTEST:
NEXT PORT
GOSUB RESTOR:
END
REM ....
OUT DATAADDRESS, OLDDATA: OUT (CONTROLADDRESS), OLDREG2
RETURN
REM ...
STROBE:
\(I=\operatorname{INP}\) (CONTROLADDRESS)
OUT (CONTROLADDRESS), (I AND 30): REM STROBE OUTPUT LOW OUT (CONTROLADDRESS), (I OR I): REM STROBE OUTPUT HIGH RETURN
REM ..
PULSESELECT:
\(I=I N P(C O N T R O L A D D R E S S)\)
OUT (CONTROLADDRESS), (I AND 247): REM SELECT OUTPUT LOW
OUT (CONTROLADDRESS), I:
REM SELECT OUTPUT HIGH
RETURN
REM ....
WRITE OUTPUT
PORTOUT:
REM CHANGE OUTPUT PORT 0 TO 3
PORT \(=\) PORT AND 7: IF PORT \(>3\) THEN RETURN: REM CHECK PORTNUMBER
OUT DATAADDRESS, PORTDATA: GOSUB PULSESELECT: REM DATA IN BUFFER
INOUT \(=\) (INOUT AND 248) OR PORT: REM SELECT PORTNUMBER
OUT DATAADDRESS, INOUT: GOSUB STROBE: REM SET PORTNUMBER
\(I=\operatorname{INP}(\) CONTROLADDRESS \():\) REM GET OLD VALUE
OUT (CONTROLADDRESS), (I OR 2): REM AUTO LOW
OUT (CONTROLADDRESS), (I AND 253): REM AUTO HIGH
RETURN
REM ..
ENABLE OUTPUT PORT X
ENABLEPORTOUT:
REM CHANGE OUTPUT PORT O TO 3
PORT \(=\) PORT AND \(7:\) IF PORT \(>3\) THEN RETURN: REM CHECK PORTNUMBER
INOUT \(=\) INOUT AND \(\left(255-\left(2{ }^{-}(\right.\right.\)PORT +4\(\left.\left.)\right)\right)\) :
REM SELECT ENABLE OF PORT-
NUMBER

OUT DATAADDRESS, INOUT: GOSUB STROBE: REM ENABLE PORTNUMBER RETURN
REM.

\section*{DISABLE OUTPUT PORT X}

REM CHANGE OUTPUT PORT 0 TO 3
DISABLEPORTOUT:
PORT \(=\) PORT AND 7: IF PORT \(>3\) THEN RETURN: REM CHECK PORTNUMBER INOUT \(=\) INOUT OR \((2\) ^ \((\) PORT +4\()):\) REM SEL.DISABLE OF PORTNUMBER OUT DATAADDRESS, INOUT: GOSUB STROBE: REM DISABLE PORTNUMBER RETURN

REM
................................ READ INPUT PORT \(x\)
INPORT: REM READ INPUT PORT 4 TO 7
PORT \(=\) PORT AND 7: IF PORT \(<4\) THEN RETURN: REM CHECK PORTNUMBER INOUT \(=\) (INOUT AND 248) OR PORT: REM SELECT PORTNUMBER
OUT DATAADDRESS, INOUT: GOSUB STROBE: REM SET PORTNUMBER
I \(=\) INP (CONTROLADDRESS \()\)
OUT (CONTROLADDRESS), ( 1 OR 2): REM ENABLE INPUT
PORTDATA = INP(STATUSADDRESS): REM READ INPUT
OUT (CONTROLADDRESS), (I AND 253): REM DISABLE INPUT
PORTDATA \(=((\) PORTDATA OR 7) \(\mid\) 8) XOR 16: REM CALCULATE INPUT RETURN
REM ...
DISPLAY:
LOCATE 9, 20: PRINT "PORT IN/OUT"
LOCATE 11, 21: PRINT PORT
VALUE \(=\) PORTDATA
FOR \(I=0\) TO 7: REM CALCULATE BINARY VALUE
LOCATE 11, (32 - I)
REST \(=\) VALUE MOD \(2:\) VALUE \(=\) VALUE 12
IF REST \(=0\) THEN PRINT " 0 "; ELSE PRINT " 1 ";
NEXT I
RETURN
REM .
OUTPUT TEST ROUTINE
OUTPUTTEST:
FOR PORTDATA \(=0\) TO 255
GOSUB DISPLAY
GOSUB PORTOUT
REM FOR J \(=0\) TO 1000: NEXT J: REM DELAY
IF INKEY \(\langle\gg "\) THEN STOPPED \(=1\) ELSE STOPPED \(=0\) :
IF STOPPED THEN PORTDATA \(=255\)
NEXT PORTDATA
IF STOPPED \(=0\) THEN GOTO OUTPUTTEST
WAIT1: IF INKEY\$ <> "* THEN GOTO WAIT1:
REM WAIT UNTIL NO KEY

\section*{PRESSED}

RETURN
REM .......
GOSUB INPORT: REM READ INPUT
IF BACKUP \(<>\) PORTDATA THEN GOSUB DISPLAY:
REM DISPLAY DATA IF CHANGED
BACKUP \(=\) PORTDATA
IF INKEY \(=* *\) THEN GOTO INPUTTEST
WAIT2: IF INKEYS <> *" THEN GOTO WAIT2
RETURN


The outputs are formed by four 8 -bit registers. At the command of a clock pulse, these registers acquire the data on the data bus (data lines from the printer port). The enable input of the registers ensures that the outputs can be set to the high-impedance mode.

The inputs of the \(\mathrm{I} / \mathrm{o}\) card are composed of four buffers, of which five channels are used at all times. This gives a total of 20 digital inputs. The five input signals that have to be processed simultaneously are returned to the PC via five control lines: ERROR, ONLINE, PE, ACK and busy. These bits may be read via the five highest bits in the status word.


The software ensures correct reproduction of the measurement results.

The circuit is readily connected to the printer port via a 1 -to-1 link.

When the hardware is built and tested, the program whose listing follows may be used. Since everything is written in Basic, the software is easily adapted to individual requirements.
[A. Rietjens - 964116]
\begin{tabular}{|l|}
\hline PARTS LIST \\
Capacitors: \\
\(\mathrm{C}_{1}-\mathrm{C}_{11}, \mathrm{C}_{13}=100 \mathrm{nF}\) \\
\(\mathrm{C}_{12}=1000 \mu \mathrm{~F}, 16 \mathrm{~V}\) \\
\\
\\
Integrated circuits: \(^{\mathrm{IC}_{1}, \mathrm{IC}_{2}, \mathrm{IC}_{4}-\mathrm{IC}_{7}=}\) \\
74 HCT 574 \\
\(\mathrm{IC}_{3}=74 \mathrm{HCT} 138\) \\
\(\mathrm{IC}_{8}-\mathrm{IC}_{11}=74 \mathrm{HCT} 245\) \\
\(\mathrm{IC}_{12}=7805\) \\
Miscellaneous: \\
\(\mathrm{K}_{1}=25\)-way right-angled \\
sub-D plug \\
\(\mathrm{K}_{2}, \mathrm{~K}_{3}=40\)-pin box header \\
\(\mathrm{K}_{4}=2\)-way terminal block \\
\(\mathrm{K}_{5}=26\)-pin box header \\
Note: use either \(\mathrm{K}_{1}\) or \(\mathrm{K}_{5}\) \\
\hline
\end{tabular}


\section*{current inverter}

\section*{Some technical \(U_{i}\) chit.}

\section*{\(U_{0}=\) \\ \(I_{0}=\)}
\(I_{0}\) and \(I_{i}\) are unipolar
\(<10 \mathrm{~mA}\) 10 MHz \(I_{0}\left(I_{i}\right) \max =\) Bandwidth =
moved by the present cir-
Transistors \(\mathrm{T}_{1 \mathrm{a}}\) and \(\mathrm{T}_{1 \mathrm{~b}}\) are contained in a dual Type SSM2210 from Burr Brown. In the present circuit they
are connected as diodes. The negative-direction input current \(I_{\mathrm{i}}\) flowing into the inverting input of \(\mathrm{IC}_{1}\) produces a positive output voltage from the op amp, which is roughly equal to the base-emitter
voltage of \(\mathrm{T}_{1 \mathrm{a}}\).
Assuming that the characteristics of \(T_{1 a}\) and \(T_{1 b}\) are identical and that the offset voltage of \(\mathrm{IC}_{1}\) is negligible, the current at the output of the circuit, \(I_{0}\), has a positive direction and its level is equal to that of the input current.

In the circuit, an input voltage of 1 V is assumed: all other potentials are referred to this.

Note that in contrasts to several other types of converter, the SSM2210 has internal protection diodes between base and emitter, so that these need not be fitted externally.
[Burr-Brown Application - 964063]

\section*{CS5390 \\ Integrated Circuits \\ ELECTRONLES}

Digital, Audio
20-bit stereo \(\mathrm{A} / \mathrm{D}\) converter for digital audio

\section*{Manufacturer}

\section*{ \\ Semiconductor Corporation}

Crystal Semiconductor Corporation, P.O. Box 17847, Austin, TX 78760, U.S.A. Tel. (512) 4457222, fax (512) 445-7581.
European sales office; Crystal Semiconductor (UK) Ltd., Lyons House, 2 Station Road, Frimley, Surrey GU16 5HF.

\section*{Description}

The CS5390 is a complete analogue-to-digital (A/D) converter for stereo digital audio systems. It performs sampling, A/D conversion and anti-alias filtering, generating 20 -bit values for both left and right inputs in serial form. The output word rate can be up to 50 kHz per channel.
The CS5390 uses 5th-order, delta-sigma modulation with \(64 \times\) oversampling followed by digital filtering and decimation, which removes the need for an external anti-alias filter. The ADC uses a differential architecture which provides excellent noise rejection.
The CS5390 has a filter passband of dc to 21.7 kHz . The filters have linear phase, 0.005 dB passband ripple, and \(>100 \mathrm{~dB}\) stopband rejection.

\section*{Features}
\(\checkmark 110 \mathrm{~dB}\) dynamic range
\(\checkmark\) THD \(+N\) better than -100 dB
\(\checkmark\) Adjustable system sampling rates including
\(32 \mathrm{kHz}, 44.1 \mathrm{kHz}\) and 48 kHz
\(\checkmark\) Complete CMOS stereo A/D system
delta-sigma A/D converters digital anti-alias filtering S/H circuity and voltage reference \(\checkmark\) Internal \(64 \times\) oversampling \(\checkmark\) Linear phase digital anti-alias filtering

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\(>100 \mathrm{~dB}\) stopband attenuation 0.005 dB passband ripple
\(\checkmark\) Low power dissipation: 550 mW power-down mode
\(\checkmark\) Pin compatible with CS5389

\section*{Application Example}

20-bit analogue-to-digital converter (ADC), Elektor Electronics December 1996.
\begin{tabular}{|c|c|c|}
\hline AGND & \({ }^{28}\) & VREF+ \\
\hline APD \(\square^{2}\) & 27 & VREF- \\
\hline AINL+ [ \({ }^{3}\) & 26 & AINR+ \\
\hline AINL- [4 & 25 & AINR- \\
\hline ACAL [5 & 24 & VA- \\
\hline LGND \(\square^{6}\) & \({ }^{23}\) & \(\mathrm{VA}+\) \\
\hline VL+ \(\square^{7}\) & 22 & ICLKA \\
\hline TSTO1 \(\square 8\) & 21 & \(\square\) TSTO2 \\
\hline DCAL \(\square^{\text {a }}\) & 20 & \(\square\) OCLKD \\
\hline DPD \({ }^{10}\) & 19 & ICLKD \\
\hline CMODE - \({ }^{1}\) & 18 & DGND \\
\hline SMODE [ \({ }^{12}\) & 17 & VD+ \\
\hline L/R [ \({ }^{13}\) & 16 & FSYNC \\
\hline SCLK \({ }^{14}\) & 15 & SDATA \\
\hline
\end{tabular}

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\begin{tabular}{|c|c|c|}
\hline \multicolumn{3}{|l|}{Pin Descriptions} \\
\hline Pin & Ref. & Description \\
\hline 15 & SDATA & Serial Data Output. Audio data bits are presented MSB first, in 2's complement format. \\
\hline 16 & FSYNC & \begin{tabular}{l}
Frame Synchronization Signal. In master mode (SMODE high). FSYNC is an output which goes high coincident with the start of the first SDATA bit (MSB), and falls low immediately after the 16th SDATA audio data bit. \\
In slave mode (SMODE low), FSYNC is an input which controls the clocking out of the data bits on SDATA. FSYNC is normally tied high, which causes the data bits to be clocked out immediately following \(L / R\) transitions. If it is desired to delay the data bits from the L/R edge, then FSYNC must be low during the delay period. Bringing FSYNC high will then enable the clocking out of the SDATA bits. Note that the MSB will be clocked out based on the L/R edge, independent of the state of FSYNC.
\end{tabular} \\
\hline 17 & VD+ & Positive Digital Power. Positive supply for the digital section. Nominally +5 V . \\
\hline 18 & DGND & Digital Ground. Digital ground for the digital section. \\
\hline 19 & ICLKD & Digital Section Input Clock. ICLKD clocks the digital filter and is the source for modulator sampling clock, OCLKD. The required ICLKD frequency is determined by the desired output word rate and the CMODE pin. If CMODE is low, ICLKD is \(256 \times\) the desired output word rate. If CMODE is high, ICLKD is \(384 \times\) the output word rate. For example, with CMODE Iow, ICLKD is 12.288 MHz for an output word rate of 48 kHz . \\
\hline 20 & OCLKD & Digital Section Output Clock. OCLKD is always \(128 \times\) the output word rate. Normally connected to ICLKA. \\
\hline 22 & ICLKA & Analogue Section Input Clock. This clock is internally divided by 2 to set the modulator's sample rate. Sampling rates, output rates and digital filter characteristics scale to ICLKA frequency. ICLKA frequency is \(128 \times\) the output word rate. For example, 6.144 MHz ICLKA corresponds to an output word rate of 48 kHz per channel. Normally connected to OCLKD. \\
\hline 23 & VA+ & Positive Analogue Power. Positive analogue supply. Nominally +5 V . \\
\hline 24 & VA- & Negative Analogue Power. Negative analogue supply. Nominally -5 V. \\
\hline 25,26 & AINR - , AINR + & Differential Right Channel Analogue Inputs. Analogue input connections for the right channel differential inputs. Nominally \(14.72 \mathrm{~V}_{\mathrm{pp}}\) (differential) full-scale. \\
\hline 27,28 & VREF - VREF + & Voltage Reference Outputs. Nominally +3.68 V (VREF + ) and -3.68 V (VREF-). Note the negative output polarity on VREF-. \\
\hline
\end{tabular}

\section*{Digital Characteristics}
\(\left(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} ; \mathrm{VA}+, \mathrm{VL}+, V D+=5 \mathrm{~V} ; \pm 5 \% ; \mathrm{VA}-=-5 \mathrm{~V} \pm 5 \%\right)\)

\section*{Parameter}
\begin{tabular}{|l|c|c|c|c|c|}
\hline Parameter & Symbol & Min & Typ & Max & Units \\
\hline High-level Input Voltage & \(\mathrm{V}_{\mathrm{IH}}\) & \(70 \% \mathrm{VD}+\) & - & - & V \\
\hline Low-level Input Voltage & \(\mathrm{V}_{\mathrm{IL}}\) & - & - & \(30 \% \mathrm{VD}+\) & V \\
\hline High-level Output Voltage at \(\mathrm{I}_{0}=-20 \mu \mathrm{~A}\) & \(\mathrm{~V}_{\text {OH }}\) & 4.4 & - & - & V \\
\hline Low-level Output Voltage at \(\mathrm{I}_{0}=20 \mu \mathrm{~A}\) & \(\mathrm{~V}_{0 \mathrm{~L}}\) & - & - & 0.1 & V \\
\hline Input Leakage Current & \(\mathrm{I}_{\text {in }}\) & - & 1.0 & - & \(\mu \mathrm{A}\) \\
\hline
\end{tabular}

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\section*{Analogue characteristics}
\(T_{A}=25^{\circ} \mathrm{C} \cdot \mathrm{VA}+\mathrm{VL}+\mathrm{VD}+=5 \mathrm{~V}, \mathrm{VA}-=-5 \mathrm{~V}\) ；Full－scale input signal sinewave， 1 kHz ：Output word rate \(=48 \mathrm{kHz}\) ；SCLK \(=3.072 \mathrm{MHz}\) Source impedance \(=39 \Omega\) with 6.8 nF across AIN＋，AIN－；measurement bandwidth is 20 Hz to 20 kHz unless otherwise specified；Logic \(0=0 \mathrm{~V}\) ，Logic \(1=\mathrm{VD}+\)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline Parameter & & Symbol & Min & \[
\underset{\text { (CS5380-k) }}{\text { Typ }}
\] & Max & Units \\
\hline Resolution & & & 20 & － & － & Bits \\
\hline \multicolumn{7}{|l|}{Dynamic Performance} \\
\hline \multirow[t]{2}{*}{Dynamic Range} & \multirow[b]{2}{*}{（A－weighted）} & \multirow{6}{*}{THD +N} & TBD & 107 & － & dB \\
\hline & & & － & 110 & － & dB \\
\hline \multirow[t]{4}{*}{Total Harmonic Distortion＋Noise} & \multirow[b]{4}{*}{\[
\begin{array}{r}
0 \mathrm{~dB} \\
-20 \mathrm{~dB} \\
-60 \mathrm{~dB} \\
\hline
\end{array}
\]} & & \multicolumn{4}{|l|}{} \\
\hline & & & － & －100 & \(\cdot\) & dB \\
\hline & & & － & －87 & TBD & dB \\
\hline & & & － & －47 & TBD & dB \\
\hline Interchannel Phase Deviation & & & － & 0.0001 & － & ． \\
\hline Interchannel Isolation & & & 106 & 120 & － & dB \\
\hline \multicolumn{7}{|l|}{dc Accuracy} \\
\hline Interchannel Gain Mismatch & & & － & 0.05 & \(\cdot\) & dB \\
\hline Gain Error & & & － & \(\pm 1\) & \(\pm 5\) & \％ \\
\hline Gain Drift & & & － & 50 & 150 & ppm／\({ }^{\circ} \mathrm{C}\) \\
\hline Bipolar Offset Error（after calibration） & & & － & \(\pm 5\) & \(\pm 20\) & LSB \\
\hline Offset Calibration Range & & & － & \(\pm 50\) & ． & mV \\
\hline \multicolumn{7}{|l|}{} \\
\hline Full－scale Differential Input Voltage（Note 1） & & \(\mathrm{V}_{\mathbb{N}}\) & 14.0 & 14.72 & － & Vpp \\
\hline Input Impedance & & \(\mathrm{Z}_{1 /}\) & ． & 25 & － & \(\mathrm{k} \Omega\) \\
\hline Common－Mode Rejection Ratio & & CMRR & \(\cdot\) & 115 & － & dB \\
\hline \multicolumn{7}{|l|}{Power Supplies} \\
\hline \multirow[t]{3}{*}{Power Supply Current with APD，DPD low （Normal Operation）} & \((\mathrm{VA}+)+(\mathrm{VL}+\) ） & \(\mathrm{I}_{\text {A＋}}\) & － & 37.5 & 55 & mA \\
\hline & VA－ & \(\mathrm{I}_{\text {A－}}\) & － & 37.5 & 55 & mA \\
\hline & \(\mathrm{VD}+\) & \(l_{\text {d }+}\) & － & 35.0 & TBD & mA \\
\hline \multirow[t]{3}{*}{Power Supply Current with APD，DPD high （power－down mode）} & \((\mathrm{VA}+)+(\mathrm{VL}+\) ） & \(\mathrm{I}_{\text {A }}\) & \(\cdot\) & 100 & － & \(\mu \mathrm{A}\) \\
\hline & VA－ & \(\mathrm{I}_{\text {A－}}\) & － & 100 & － & \(\mu \mathrm{A}\) \\
\hline & VD＋ & \(\mathrm{I}_{+}\) & \(\cdot\) & 100 & － & \(\mu \mathrm{A}\) \\
\hline \multirow[t]{2}{*}{Power Consumption} & （APD，DPD low） & PDN & － & 550 & TBD & mW \\
\hline & （APD，DPD high） & PDS & － & 1.5 & － & mW \\
\hline Power Supply & （dc to 29 kHz ） & \multirow[t]{2}{*}{PSRR} & － & 65 & － & dB \\
\hline Rejection Ratio & \((29 \mathrm{kHz}\) to 3.046 MHz ） & & \(\cdot\) & 90 & － & dB \\
\hline
\end{tabular}

Note 1：specified for a fully differential input \(\pm\{(\) AINR +\()-\)（AINR -\()\}\) ．The ADC accepts input voltages up to the analogue supplies \((V A+, V A-)\) ．Full－scale outputs will be produced for differential inputs beyond \(V_{\mathbb{I}}\) ．This value is subject to the gain error tolerance specification
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\section*{Pin Descriptions}
\begin{tabular}{|c|c|c|}
\hline Pin & Ref． & Description \\
\hline 1 & AGND & Analogue ground．Analogue ground reference \\
\hline 2 & APD & Analogue Power Down．Analogue power down command．When high，the analogue circuitry is in power－down mode．APD is normally connected to DPD when using the power－down feature．APD should be connected to AGND if analogue power－down is not used． \\
\hline 3.4 & AINL＋，AINL－ & Differential Left Channel Analogue Inputs．Analogue input connections for the left channel differen－ tial inputs．Nominally \(14.72 \mathrm{~V}_{\mathrm{pp}}\)（differential）full－scale． \\
\hline 5 & ACAL & Analogue Calibrate．Analogue section calibrate command．When high，causes the left and right channel modulator inputs to be internally connected to AGND respectively．Should be connected to DCAL． \\
\hline 6 & LGND & Logic Ground．Ground for the logic portions of the analogue section． \\
\hline 7 & VL＋ & Positive Logic Power．Positive logic supply for the analogue section．Nominally +5 V ． \\
\hline 8，21 & TST01，TST02 & Test Output．These two pins are bonded out for factory test outputs．They must not be connected to any external component or any length of PC trace． \\
\hline 9 & DCAL & Digital Calibrate Output．DCAL rises immediately upon entering the power－down state（DPD brought high）．It returns low \(4096 \mathrm{~L} / \mathrm{R}\) periods after leaving the power down state（DPD brought low），indicating the end of the offset calibration cycle（which \(=85.33 \mathrm{~ms}\) with a 12.288 MHz ICLKD）．May be connected to ACAL． \\
\hline 10 & DPD & Digital Power Down．Digital section power－down command．Bringing DPD high puts the digital sec－ tion into power－down mode．Upon returning low，the ADC starts an offset calibration cycle．This takes \(4096 \mathrm{~L} / \mathrm{K}\) periods（ 85.33 ms with a 12.288 MHz ICLKD）．DCAL is high during the calibrate cycle and goes low upon completion．DPD is normally connected to APD when using the power down feature．A calibration cycle should always be initiated after applying power to the supply pins． \\
\hline 11 & CMODE & Clock Mode Select．CMODE should be tied low to select an ICLKD frequency of \(256 \times\) the output word rate．CMODE should be tied high to select an ICLKD frequency of \(384 \times\) the output word rate． \\
\hline 12 & SMODE & Serial Interface Mode Select．SMODE should be tied high to select the serial interface master mode．SCLK，FSYNC and L／R are outputs generated by internal dividers operating from CLKD， SMODE should be tied low to select serial interface slave mode，where SCLK，FSYNC and L／R are all inputs．In slave mode，L／R，FSYNC and SCLK need to be derived from ICLKD using external di－ viders． \\
\hline 13 & L／R & \begin{tabular}{l}
Left／Right Select．In master mode（SMODE high），L／R is an output whose frequency is at the out－ put word rate．L／R edges occur 1 SCLK cycle before FSYNC rises．When L／R is high，left channel data is on SDATA，except for the first SCLK cycle．When L／R is low，right channel data is on SDATA， except for the first SCLK cycle．The MSB data bit appears on SDATA one SCLK cycle after L／R changes． \\
In slave mode（SMODE low），L／R is an input which selects the left or right channel for output on SDATA．The rising edge of \(L / / R\) starts the MSB of the left channel data．L／R trequency must be equal to the output word rate． \\
Although the outputs of each channel are transmitted at different times，the two words in an \(\mathrm{L} / \mathbb{R}\) cycle represent simultaneously sampled analogue outputs．
\end{tabular} \\
\hline 14 & SCLK & Serial Data Clock．Data is clocked out on the falling edge of SCLK． In master mode（SMODE high），SCLK is a continuous output clock at \(64 \times\) the output word rate． In slave mode（SMODE low），SCLK is an input，which requires a continuously supplied clock at any frequency from \(32 \times\) to \(128 \times\) the output word rate（ \(64 \times\) is preferred）．When FSYNC is high，SCLK \\
\hline
\end{tabular}

In slave mode（SMODE low）．SCLK is an input which requires a continuously supplied clock at any红 \(32 \times\) to \(128 \times\) the output word rate（ \(64 \times\) is preferred）．When FSNCC is high，SCLK clocks out serial data，except for the MSB which appears on SDATA when L／R changes

\section*{active filter Type UAF42}

Burr-Brown's integrated circuit Type UAF42 is a generalpurpose active filter that may be used as a high-pass, a lowpass, a band-pass, or a bandstop section. It is designed in the traditional state-variable architecture with an inverting amplifier and two integrators. The \(1000 \mathrm{pF} \pm 0.5 \%\) integrator capacitors are on the chip, which makes looking for such loss-free, high-precision devices unnecessary.

Nevertheless, some of the other external components may be difficult to obtain, which is the reason that BurrBrown can provide dos program 'Filter42.exe V1.0', to simplify the computation of Butterworth, Chebyshev and Bessel filters. In the program, simply choose the wanted filter type, the slope, minimal

attenuation in the cut-off areas, the cut-off point(s), and some other parameters, and the computer produces not only a list with compo-
nent values, but also a computed phase and frequency characteristic.

The diagram shows an inverse 2nd-order Chebyshev
low-pass filter with an attenuation of 40 dB and a cut-off frequency of 1 kHz . The program shows that this filter attains the wanted attenuation at a frequency of 7.1 kHz . Maximum attenuation is obtained at 10 kHz , after which it gradually drops back to 40 dB .

The filter draws a current of 6 mA .

The overall distortion at 100 Hz is \(\leq 0.001 \%\) with an input voltage of 1 V r.m.s. and a bandwidth of 80 kHz .

The maximum input voltage is 1.93 V .

The transfer amplification is \(\times 0.986(-0.1 \mathrm{~dB})\).

The ic is eminently suitable for experimentation with all kinds of filter. The price of the IC includes the development program.
[Burr-Brown - 964087]



Build this filter by connecting filter subcircuits in order as shown
in the 'Filter Block Diagran' above. She Application Bulletin AB-O35 for in the 'Pilter component Values' table, onit the component.
in a component

964087-13

\section*{Iow-noise crystal oscillator}

Nowadays, the design of many oscillators is based on a couple of logic gates and a crystal. Unfortunately, these oscillators are very noisy and have a tendency to overdrive the crystal. These drawbacks adversely affect the shortterm as well as the long-term stability.

Oscillators using bipolar transistors or FETS perform much better, but it means, of course, that the oscillator circuit must be tuned to the crystal frequency.


The present circuit is a Colpitts oscillator specially designed for a 16 MHz crystal that requires a shunt capacitance of 20 pF . Feedback is provided by capacitive divider \(\mathrm{C}_{1}-\mathrm{C}_{2}\), which, owing to the resonance current, functions like a kind of auto transformer.

The output voltage is transformed up, so that the overall amplification is \(>1\).

In this type of oscillator, there is no likelihood of the crystal being overdriven.

In contrast to the squarewave output of a gated oscillator, the output of the present oscillator is a sine wave, so that the phase noise is considerably less. (In a gated oscillator, the instant that the gate changes state is determined primarily by amplitude noise and this produces phase noise).

The oscillator output level is around 1.5 V .

The circuit draws a current of about 2 mA .
[H. Bonckamp - 964081]

\title{
logic probe for buffer ICs
}

This is another device for making working with the logic analyser published in our May 1996 issue more convenient. It increases the versatility of the analyser.

The probe, consisting of an IC socket and a box header, enables the direct display on the analyser of the channels of a buffer IC. As in other projects, the pinout follows that of the HewlettPackard analyser. To enable
all pins of the buffer ic to be measured, it is possible with the aid of two jumpers to selectively interchange pins 1 and 19 with pins 12 and 11 .

The PCB is not available ready made, but is fairly simple to make or have made.

In the space reserved for \(\mathrm{IC}_{1}\) there is no standard IC socket b u t
rows of long ic pins that protrude at the track side of the board. After they have been soldered in place, they may be lengthened with one or more sockets at the track side.

The ic to be tested is mounted at the top of th e board onto t h e \(\begin{array}{lll}\mathrm{t} & \mathrm{h} & \mathrm{e} \\ \mathrm{t} & \mathrm{w} & \mathrm{o}\end{array}\)


\section*{PARTS LIST}
\(\mathrm{IC}_{1}, \mathrm{IC}_{2}=74 \mathrm{HCT} 245\) to be tested
\(K_{1}, K_{2}=20\)-way box header 4 off jumper

\section*{current limiting with a 555}

Strictly speaking, the title 'current limiting' is not entirely right, since the circuit itself does not limit, but detects. When the current through the load is too high, pin 3 of \(\mathrm{IC}_{1}\) goes low. Reset switch \(\mathrm{S}_{1}\) needs to be operated to make the pin high again, but this is, of course, only possible after the current has dropped to an acceptable level. For whichever purposes the level change at pin 3 is used is up to individual requirements.

The circuit uses the comparator and bistable in the 555 , which often are not used at all. Resistor \(\mathrm{R}_{2}\) functions as current sensor. Since the drop across this resistor is not needed to switch on a transistor, it need not be large. Consequently, the supply voltage is nearly equal to the input

potential, so that the dissipation of the sensor is tiny.

Between pin 8 and earth, there is in the IC a potential divider, which provides the two comparators with a reference potential. The positive inputs of the comparators, pins 2 and 6 , are linked to \(P_{1}\) and \(S_{1}\) respectively. The outputs of the comparators con-
trol the set and reset input of the internal bistable. The output of the bistable is available at pin 3.

The intention is to adjust \(P_{1}\) to obtain a potential at pin 6 that lies just under \(2 / 3\) of the supply voltage, that is, without load. If, because of the load, the voltage at pin 8 drops too much, the potential
at pin 6 becomes greater than that at pin 5 . The comparator linked to pin 6 then changes state and the bistable is reset, whereupon pin 3 goes low. This situation is maintained until the reset switch is pressed, which pulls the inverting input of the second comparator to ground. This comparator then changes state and sets the bistable.

The prototype worked reliably with supply voltages between 5 V and about 14.5 V . The current drain is about 7 mA at 10 V .

Note that the configuration described results in the potential at pin 8 being lower than that at various other pins. According to the manufacturers' data, this is all right as long as the difference does not exceed 300 mV .
[A. Lötgens -964095]


\section*{U/f converter}

The present circuit combines simplicity and linearity: it is highly suitable for use as an \(\mathrm{A}-\mathrm{D}\) converter ( ADC ) for a microprocessor. It consists of integrator \(\mathrm{IC}_{1}\) and monostable \(\mathrm{IC}_{2 \mathrm{a}}\). The design is such that each triggering of the monostable causes the integrator to be discharged. The amount of charge is proportional to the input voltage. The frequency at which all this happens is a measure of the input voltage.

Provided the right components are used, an accuracy of eight bits may be obtained with a simple converter like this. The accuracy is enhanced if the processor used does not base the measurement of the output signal on the frequency but rather on the duty factor. This is a relative measurement in which any drift effects are largely eliminated.

The relationship between duty factor (df) and input voltage \(\left(U_{\text {in }}\right)\) is
\[
\mathrm{df}=1 /\left(1+U_{\mathrm{in}} / U_{\mathrm{B}}\right),
\]
where \(U_{\mathrm{B}}\) is the supply voltage. This assumes that
\[
\mathrm{R}_{1}=\mathrm{R}_{2}=\mathrm{R}_{3} / 2
\]

The specified values of the components are correct for a


The input voltage range is determined by the ratio \(\mathrm{R}_{1} / \mathrm{R}_{2}\) and is \(0-2.5 \mathrm{~V}\) in the present circuit.

To ensure a good start or restart of the converter, a somewhat unusual reset circuit, \(\mathrm{R}_{4}-\mathrm{C}_{2}-\mathrm{D}_{1}\), is used. The charging of \(\mathrm{C}_{2}\) causes the integrator to operate into a negative direction in the first instance. Once the capacitor is fully charged, it no longer affects the integrator, which then operates into a positive direction, whereby the cycle is begun.

When the input voltage drops below -2.25 V , the conversion process stops. A restart then needs to be generated by the connected processor, which enables the reset circuit via \(\mathrm{R}_{6}\) and \(\mathrm{D}_{2}\).
[H. Bonekamp - 964096]
frequency of 48 Hz . This frequency is intentionally kept low, so that even fairly slow processors can still measure the duty factor with a resolution of eight bits. An additional benefit of such a low frequency is that any mains hum is more easily suppressed.

The frequency, \(f_{\mathrm{o}}\), is determined by
\[
f_{\mathrm{o}}=1 / 1.4 \mathrm{R}_{7} \mathrm{C}_{3}[\mathrm{~Hz}] .
\]


\section*{light barrier with TTL output}

Digital systems need an interface to communicate with the outside world. Since only voltage drops can be used by the hardware, auxiliary circuits are often used to convert the ambient data into a logic level.
A light barrier is a frequently used aid to determine the endstop or end-position. When the light barrier is interrupted, the level at the \(\mathrm{I} / \mathrm{o}\) line of a computer changes. Since the I/O lines usually work at TTL level, an interface must be used that can convert optical data into TTL levels.

In the present design, the light barrier is a Type CNY37 optoisolator, but other types will do just as well. If, for in-

stance, an \(n-p-n\) version is used, only the collector and emitter connections of the transistor need to be inter-
changed.
The conversion of the analogue potential level at the collector of the transistor into
a digital level is effected by a Type \(\mu \mathrm{A} 741\) op amp. Although this is not intended to work from a single 5 Vsupply, it will do so in the present design.

The output of the op amp is at TTL level. Because of the relatively high output impedance, provided bt \(\mathrm{R}_{5}\), it is not advisable to connect the output directly to a standard TTL gate. The use of LS, HC, or нст versions offers no difficulties, however.

When the light barrier is on, the circuit draws a current of about 18 mA ; this drops by a few mA when the light barrier is interrupted.
[K. Walraven - 964073]

\section*{low-noise voltage reference}

The peak-to-peak noise of many voltage references is specified by the makers for a bandwidth of \(0.1-10 \mathrm{~Hz}\). However, when the reference is to be used in an A-D convertor (ADC), the wideband noise is of much greater importance.

The reference used in the present circuit, a Type AD586, consists of an ion-implanted buried zener diodes and an integrated output buffer. With a bandwidth of 1 MHz , it contributes unfiltered noise at a level of \(200 \mu \mathrm{~V}_{\mathrm{pp}}\), which is equivalent to \(33 \mu \mathrm{~V}\) r.m.s. This is already very good compared with most bandgap references, but with proper filtering the wideband noise may be all but eliminated.

Some voltage references, among them the AD586, have a special pin to reduce noise. When this pin (8) is linked to ground via a \(1 \mu \mathrm{~F}\) electrolytic capacitor, a first-order lowpass filter is formed with internal resistance \(R_{\mathrm{S}}\). The cutoff frequency of this filter is about 40 Hz .

Although this filter largely eliminates the wideband noise of the zener, the noise level at the output (pin 6) is still around \(160 \mu \mathrm{~V}_{\mathrm{pp}}\). This noise may be reduced by a

fairly large capacitor between output and ground, but this is not wholly satisfactory for two reasons. In the first place, at low frequencies, the output buffer/ amplifier has an output impedance of only a few ohms. This impedance is not reduced much by the capacitor. In the second place, the capacitor does not improve the stability of the output op amp.

A much better solution is provided by external filter \(\mathrm{R}_{1}-\mathrm{C}_{4}\) in the diagram. This
has a cut-off point of 1.6 Hz and reduces the noise voltage to around \(4 \mu \mathrm{~V}\).

The passive filter is followed by a precision lownoise buffer/amplifier, such as the OP27GZ \(\left(\mathrm{IC}_{2}\right)\).

The large capacitor, \(\mathrm{C}_{7}\), at the output of the op amp serves a dual function. With \(\mathrm{R}_{2}\), it forms a low-pass filter with a cut-off frequency of about 160 Hz . This reduces the noise at the output of the op amp to a negligibly low level. Also, the capacitor im-
proves the stability of the reference voltage, since it behaves as a buffer reservoir for load variations. Against this, the capacitor forms a highly capacitive load at the output of the op amp, but this compensated by \(\mathrm{R}_{2}\) and \(\mathrm{C}_{6}\).

Since electrolytic capacitors become less effective at high frequencies, \(\mathrm{C}_{7}\) is shunted by a 100 nF capacitor to ensure that at high frequencies the output impedance of \(\mathrm{IC}_{2}\) remains low.
[H. Bonekamp - 964098]

\section*{mains-operated flashing light}

The present circuit, consisting of only a handful of components, enables a mains-operated lamp to flash at intervals of about one second. It is useful in, for instance, an alarm system to give a visual warning.

Diodes \(\mathrm{D}_{1}-\mathrm{D}_{4}\) rectify the mains voltage applied to \(\mathrm{K}_{1}\). The resulting direct voltage is used to charge capacitors \(\mathrm{C}_{1}\) and \(\mathrm{C}_{2}\). Charging continues until the breakdown voltage of neon lamp \(L_{2}\) is reached. The thyristor is then switched on, whereupon lamp \(\mathrm{L}_{1}\) lights.

At the same time, \(\mathrm{C}_{1}\) is discharged via \(R_{2}\) and \(D_{5}\). This causes the neon lamp to be cut off, so that \(\mathrm{Th}_{1}\) gets no gate current. This results in
the thyristor being switched off at the next zero crossing and \(\mathrm{L}_{1}\) going out.

Since the thyristor is off, \(\mathrm{C}_{1}\) and \(\mathrm{C}_{2}\) are charged again, whereupon the action repeats itself.

As this is a mains-operated circuit, extreme care should be taken in the construction and testing of it. It should be impossible for any mains-carrying parts to be touched when the circuit is in operation. Moreover, the distance between mains-carrying parts should be at least 3 mm .

Because a high potential will exist across the capacitors when \(\mathrm{L}_{2}\) or the thyristor are not on, the capacitors should have a rating of \(\geq 630 \mathrm{~V}\).
[A. Rietjens - 964101]


The digital-to-analogue converter presented here could not be simpler. It consists of the logic circuit of a printer port of a computer and an R-2R network. One of its applications is as a sound card, but, of course, it can also be used in other applications in which a digital code has to be converted into a voltage

When the converter is used as a sound card, applications programs are required. Several of these are available via freeware and shareware, with which, for instance, MOD files (that is, Amiga sound files) can be made audible when the present card is connected to the printer port of a computer.

The July/August 1996 issue of this magazine describes an AD/DA converter (p. 102), including Turbo-Pas-

\section*{mini sound card}

cal routines to communicate via a parallel printer port.
[L. Lemmens - 964103



\section*{PARTS LIST}

\section*{Resistors:}
\(\mathrm{R}_{1}, \mathrm{R}_{2}, \mathrm{R}_{4}, \mathrm{R}_{6}, \mathrm{R}_{8}, \mathrm{R}_{10}, \mathrm{R}_{12}\), \(\mathrm{R}_{14}, \mathrm{R}_{16}=20 \mathrm{k} \Omega, 1 \%, \mathrm{SMD}\)
\[
\begin{aligned}
& \mathbf{R}_{3}, \mathbf{R}_{5}, \mathbf{R}_{7}, \mathbf{R}_{9}, \mathbf{R}_{11}, \mathbf{R}_{13}, \mathbf{R}_{15}, \\
& \mathbf{R}_{15}, \mathbf{R}_{17}, R_{19}=10 \mathrm{k} \Omega, 1 \%, \\
& \operatorname{sMD}, \\
& \mathbf{R}_{18}=2.2 \mathrm{k} \Omega
\end{aligned}
\]

Capacitors:
\(C_{1}=470 \mathrm{nF}, \mathrm{sMD}\)
\(\mathrm{C}_{2}=10 \mathrm{nF}, \mathrm{SMD}\)

\section*{Miscellaneous:}
\(\mathrm{K}_{1}=\) audio socket for board mounting
\(\mathrm{K}_{2}=25\)-way sub-D plug for
board mounting


\section*{Nicd battery discharger}

After a battery has been discharged, it is often found that the separate cells have been discharged to different values. This is, of course, not good for the battery and may shorten its life considerably, which is an expensive business. This danger may be prevented by discharging the cells individually by a circuit such as the one in the diagram. Since this discharger is inexpensive to build, several can be used in parallel.

Circuit \(\mathrm{IC}_{2 \mathrm{a}}\) is arranged as a comparator. The necessary reference voltage at it inverting input is derived from potential divider \(\mathrm{R}_{2}-\mathrm{R}_{3}\). The level of the reference voltage is the same as that of a discharged cell, that

is, about 0.9 V .
The non-inverting input of \(\mathrm{IC}_{2 \mathrm{a}}\) is at the same potential as the actual cell voltage. If this is higher than the reference voltage, the comparator output goes high, whereupon \(\mathrm{T}_{1}\) is switched on, so that the
cell is discharged via \(\mathrm{R}_{5}\) and the transistor. The value of \(\mathrm{R}_{5}\) is chosen to give a discharge current of about 80 mA .

Since the collector voltage of \(T_{1}\) is virtually constant \((0.2 \mathrm{~V})\), the discharge current
drops with falling cell potential. When this potential has decreased to about 0.9 V , the comparator changes state, which terminates the discharging process. The process may take several hours.

Resistor \(\mathrm{R}_{4}\) provides a small hysteresis of about 3 mV .

The LED at the output of the comparator lights when the cell is being discharged. To keep the current drain of the circuit low, it is advisable to use a low-current type Led.

The circuit is powered by a mains adaptor followed by regulator \(\mathrm{IC}_{1}\), which converts the \(9-12 \mathrm{~V}\) from the adaptor into a stable \(5-\mathrm{V}\) supply.
[L. Lemmens - 964114]

\section*{capacitive proximity switch}

A proximity switch is one which requires your hand to be merely near it as opposed to on it to operate.

The present switch is based on a capacitively coupled oscillator-receiver combination. If the coupling is upset, the output state of the receiver alters. The resulting change in level may be used, for instance, to switch a light on or off via a relay.

The switch has four elements: an oscillator to drive the sensor, a selective amplifier that raises the sensor signal, a rectifier, and a comparator. The sensor, located between the oscillator and amplifier consists of two metal strips (about \(100 \times 20 \mathrm{~mm}\) ) at a parallel distance of about 10 mm from each other.

The oscillator, \(\mathrm{IC}_{1 \mathrm{a}}\), may be tuned between 7 MHz and 10 MHz with \(\mathrm{P}_{1}\). The tuned circuit formed by \(\mathrm{L}_{1}\) and the capacitance of the sensor is designed for a central frequency of 8.2 MHz . Owing to tolerances in \(\mathrm{IC}_{1 \mathrm{a}}\), it may be necessary to give \(\mathrm{C}_{1}\) a slightly different value if \(\mathrm{P}_{1}\) does not cover the indicated range.

The oscillator signal is ap-

plied to amplifier \(T_{1}\) via the sensor. The amplifier is tuned to the correct frequency with trimmer \(\mathrm{C}_{4}\). The output voltage of the amplifier may be varied with \(\mathrm{P}_{2}\).

The amplified signal is rectified and smoothed by \(\mathrm{D}_{1}, \mathrm{D}_{2}\), \(\mathrm{C}_{5}\) and \(\mathrm{C}_{6}\), and split into two branches. Since the signals represent the instantaneous value of the potential across the sensor, one is applied directly to the inverting input of com-
parator \(\mathrm{IC}_{2 \mathrm{~b}}\), while the other is applied to peak detector \(\mathrm{IC}_{2 \mathrm{a}}-\mathrm{D}_{3}-\mathrm{C}_{7}\). The detector has a fairly large time constant; its output is applied as a reference of the nominally present signal level to the non-inverting input of the comparator.

When the oscillator circuit is detuned owing to a change in the sensor capacitance, the instantaneous value of the rectified signal will vary immediately, whereas the out-
put of the peak detector will remain virtually constant. Consequently, the comparator changes state, which causes transistor \(\mathrm{T}_{2}\) to be switched on. The collector voltage of this transistor may be used to drive a relay or similar device.

For the calibration of the circuit, an oscilloscope is handy, but not essential.

Set the presets and trim-
mer \(\mathrm{C}_{4}\) to the centre of their travel.

Adjust \(\mathrm{P}_{2}\) to give a potential across \(\mathrm{C}_{6}\) and \(\mathrm{C}_{7}\) - test point \(C-\) of 2.5 V .

Leave the voltmeter across \(\mathrm{C}_{7}\) and adjust \(\mathrm{P}_{1}\) and \(\mathrm{C}_{4}\) for maximum meter reading. Bear in mind that this takes a little time owing to the large
tim e constant of the peak detector.

Readjust \(\mathrm{P}_{2}\) to obtain a meter reading of exactly 2.5 V .

Adjust \(\mathrm{P}_{3}\) to obtain the desired sensitivity. With a sensor as described, the sensitivity of the prototype was such that an operating distance of

100 mm was obtained. It is, of course, essential that the circuit is fitted adjacent to the sensor. Long(ish) wires between them would make the circuit vulnerable to spurious radiations and this would degrade the reliability.

The circuit is powered by a \(5-\mathrm{V}\) supply and draws a cur-
rent of only 4.5 mA .
Finally, \(L_{1}\) and \(L_{2}\) need not be wound: they are small chokes that are readily available from your local retailer or mail order houses.
[I Giesberts - 964120]

\section*{logic probe for 8031}


This is yet another variant of a probe to make working with the logic analyser published in our May 1996 issue more convenient. The present variant is intended particularly for use with 8031-derived devices.

When the probe is in place, all ports of the relevant processor are accessible externally via two box headers, so that 32 test points can be connected to the logic analyser simultaneously. It is, however, also necessary to make a selection for six signals with three jumpers.

In critical cases, particularly when high clock frequencies are used, it may be advisable to provide the processor on the adaptor board with a crystal. This means, of course, that the crystal in the relevant equipment must be removed temporarily.

In the space reserved for IC1 (IC2) there is no standard ic socket but two long rows of IC pins that protrude at the track side of the board. After they have been soldered in place, the pins can be lengthened with one or more sockets at the track side.

The IC to be tested is mounted at the top of the board onto the two rows of pins. The logic probe is plugged into the socket intended for the IC.
[A. Rietjens - 964112]


\section*{PARTS LIST}
\(\mathrm{C}_{1}, \mathrm{C}_{2}=27 \mathrm{pF}\)
\(\mathrm{IC}_{1}=8031\) ( \(40-\mathrm{pin} \mathrm{DIL}\) ) to be tested
\(K_{1} \cdot K_{2}=20\)-way box
header
\(X_{1}=\) crystal removed from circuit


\section*{electrically isolated I2C bus}

In some cases, it is desirable for the input and output of an \(\mathrm{I}^{2} \mathrm{C}\) bus to be electrically isolated. This is achieved in the present circuit by a couple of optoisolators. Since the bus is
actuates the LED in the first optoisolator, and so on.

This vicious circle is broken as shown in the diagram. The circuit consists of identical and symmetrical SDA and

bidirectional, at least two optoisolators are needed for the SDA line and two for the SCL line.

The first idea for the design was to couple these two pairs of optoisolators in cascade. This idea was quickly discarded, however, because if the first optoisolator is driven from the bus and the LED lights, the phototransistor causes the LED in the second optoisolator to light also, whereupon the phototransistor in the second optoisolator

SCL lines.
Assuming that pin 2 of \(\mathrm{K}_{1}\) is logic low at a given instant, the LED of optoisolator \(\mathrm{IC}_{1}\) lights. The associated phototransistor is then on, which earthes pin 2 of \(\mathrm{K}_{2}\) via \(\mathrm{D}_{7}\). At the same time, the LED in \(\mathrm{IC}_{2}\) is virtually short-circuited by \(\mathrm{D}_{8}\), so that it cannot light.

The phototransistor in \(\mathrm{IC}_{1}\) also ensures that indicator \(D_{3}\) lights. Note that this LED does not load the \(\mathrm{I}^{2} \mathrm{C}\) bus in the slightest.

Operation in the opposite

direction is similar, but then it is \(\mathrm{D}_{6}\) that prevents the LED in \(\mathrm{IC}_{1}\) from lighting, while \(\mathrm{D}_{1}\) functions as indicator.

The circuit around \(\mathrm{IC}_{3}\) and \(\mathrm{IC}_{4}\) forms an identical coupling between pins 5 of \(\mathrm{K}_{1}\) and \(\mathrm{K}_{2}\) respectively.

Note that \(\mathrm{D}_{1}-\mathrm{D}_{4}\) serve to indicate in which direction the data stream is moving.

The optoisolators are Type 6N139, which are typified by their high speed ( \(100 \mathrm{kbit} \mathrm{s}^{-1}\) ) and very low drive current. The latter makes it possible
for them to driven directly from the \(I^{2} \mathrm{C}\) bus without the need of an amplifier.

Finally note the following. Each half of the circuit draws a current of about 2.5 mA . Use low-current types of LED. In case of supply difficulties, Schottky diodes \(\mathrm{D}_{5}-\mathrm{D}_{12}\) may be replaced by standard Type 1N4148 diodes.
[C. Bajeux - 964062]
\begin{tabular}{l} 
PARTS LIST \\
Resistors: \\
\(R_{1}-R_{4}=3.3 \mathrm{k} \Omega\) \\
\(R_{5}-R_{8}=1 \mathrm{k} \Omega\) \\
\\
Semiconductors: \\
\(D_{1}-D_{4}=\) low-current LED \\
\((2 \mathrm{~mA})\) \\
\(D_{5}-D_{12}=\) BAT82 \\
Integrated circuits: \\
IC \(\mathrm{C}_{1}-I C_{4}=6 \mathrm{~N} 139\) (Tele- \\
funken) \\
\\
Miscellaneous: \\
\(\mathrm{K}_{1}, \mathrm{~K}_{2}=6\)-way mini DIN \\
bus for board mounting \\
PCB Order No. 964062 (see \\
Readers Services) \\
\hline
\end{tabular}



netic interference (EMI), particularly at frequencies above 30 MHz .

The unit consists of a detector, a current-to-voltage \((I-U)\) convertor that drives a small moving-coil meter, and a tiny whip antenna.

The antenna should really be \(1 / 4 \lambda\), but this is difficult to arrange with a wide-band circuit. In practice, a length of about 70 cm will do fine. Note that the antenna may also be a telescopic type.

Capacitor \(\mathrm{C}_{1}\) and choke \(\mathrm{L}_{1}\) form a high-pass filter with a cut-off frequency of about

30 MHz . Detection of the received signals is effected by \(\mathrm{D}_{1}-\mathrm{C}_{1}\). The diode is held at +4.5 V via the inverting input of \(\mathrm{IC}_{1}\). The non-inverting input is at earth potential for alternating voltages via \(\mathrm{C}_{2}\). The anti-parallel-connected diodes \(D_{2}\) and \(D_{3}\) serve to protect the sensitive input of the unit against large fieldstrengths.

Operational amplifier \(\mathrm{IC}_{1 \mathrm{~b}}\) converts the current through \(\mathrm{D}_{1}\) into a voltage. Its amplification is very high, and its transimpedance is
\(10^{7} \Omega \mathrm{~V}^{-1}\). The output of the op amp drives a small \(50 \mu \mathrm{~A}\) meter.

The unit is powered by a 9 V alkaline or rechargeable battery. So as not to load the battery too heavily, halving the supply voltage is effected by an active voltage splitter: \(\mathrm{IC}_{1 \mathrm{a}}\). This op amp converts the voltage derived from high-impedance divider \(\mathrm{R}_{4}-\mathrm{R}_{5}\) into a potential of 4.5 V that can be used with low-impedance loads. Resistor \(\mathrm{R}_{3}\) prevents the op amp from becoming unstable
owing to the capacitive load formed by \(\mathrm{C}_{2}\) and \(\mathrm{C}_{4}\).
[H. Bonekamp - 964082]

> PARTS LIST
> Resistors:
> \(R_{1}=10 \mathrm{M} \Omega\)
> \(R_{2}=1 \mathrm{k} \Omega\)
> \(R_{3}=100 \Omega\)
> \(R_{4}, R_{5}=100 \mathrm{k} \Omega\)

\section*{Capacitors:}
\(\mathrm{C}_{1}=10 \mathrm{pF}\)
\(\mathrm{C}_{2}=100 \mathrm{nF}\), high stability
\(\mathrm{C}_{3}=100 \mathrm{pF}\)
\(\mathrm{C}_{4}, \mathrm{C}_{6}=10 \mu \mathrm{~F}, 16 \mathrm{~V}\), radial
\(\mathrm{C}_{5}=10 \mathrm{nF}\), high stability

\section*{Inductors:}
\(\mathrm{L}_{1}=2.7 \mu \mathrm{~F}\)
Semiconductors:
\(\mathrm{D}_{1}=\mathrm{BAT} 82\)
\(\mathrm{D}_{2}-\mathrm{D}_{4}=1 \mathrm{~N} 4148\)

\section*{Integrated circuit:}
\(I_{1}=\) TLC272

\section*{Miscellaneous:}
\(\mathrm{S}_{1}=\) single-pole on/off switch
\(\mathrm{Ant}_{1}=70 \mathrm{~cm}\) whip or telescopic antenna
\(M_{1}=50 \mu \mathrm{~A}, 3 \mathrm{k} \Omega\), movingcoil meter
\(\mathrm{Bt}_{1}=9 \mathrm{~V}\) battery

It is a frequent requirement in computer and audio systems that several units are switched on or off simultaneously. The simplest way of arranging this is to switch the various units via an extension
socket. This may, however, cause such a large current that the mains fuse blows or that other equipment is affected by the current peak. This can be prevented by the use of the present circuit. It
ensures that the various units are switched on one after another, so that the load on the mains is spread, and also that situations such as a nonparked printer head are avoided.

The circuit is based on a Type 4060 counter, \(\mathrm{IC}_{2}\). The values of the external components of the internal oscillator are selected to result in an oscillator frequency, \(f_{\mathrm{o}}\), of about 10 Hz . The pulse rate of the

signal at pin \(7\left(\mathrm{Q}_{3}\right)\) of \(\mathrm{IC}_{2}\) is \(f_{\mathrm{o}} / 16\). These pulses are used to clock 8-bit shift register \(\mathrm{ICla}_{\mathrm{a}} \mathrm{IC}_{1 \mathrm{~b}}\). Since the D-input of \(I C_{1 a}\) is at the supply level, the eight outputs will become high one after another in the rhythm of the clock (that is, each 1.5 s ). The transistor, \(\mathrm{T}_{1}-\mathrm{T}_{8}\), at each of the outputs then actuates the associated relay, \(\mathrm{Re}_{1}-\mathrm{Re}_{8}\), and this switches on the relevant
mains-operated unit.
At the instant the eighth output, pin \(10\left(\mathrm{Q}_{\mathrm{D}}\right)\) of \(\mathrm{IC}_{1 \mathrm{~b}}\) goes high, the counter is reset. The relays remain energized until the supply voltage is switched off.

Network \(\mathrm{R}_{29}-\mathrm{C}_{2}\) arranges the resetting of the shift register when the mains is switched on (again).

The supply for the circuit consists of mains transformer
\(\mathrm{Tr}_{1}\), bridge rectifier \(\mathrm{B}_{1}\), and reservoir capacitor \(\mathrm{C}_{4}\). This is used to energize the relays. The supply for the ICS is additionally regulated by zener diode \(\mathrm{D}_{9}\). Diode \(\mathrm{D}_{10}\) is the mains on/off indicator.

The specified relays can switch up to 2 kW .

It is advisable to use a short-circuit-proof mains transformer.

Connection between the
various units and the relay contacts is best made via a 3 -way mains terminal block.

It is advisable to build the circuit in a Class I enclosure.

If fewer than eight units are used, the superfluous relays, free-wheeling diodes and switching transistor, starting with \(\mathrm{Re}_{8}, \mathrm{D}_{8}, \mathrm{~T}_{8}, \mathrm{R}_{8}\).
[T. Giesberts - 964059]


\section*{surround-sound loudspeaker}

In a surround-sound system, the quality of the drive units is not particularly important. After all, the audio bandwidth of this channel is limited to about 100 Hz to 7 kHz , and it does not make sense, therefore, to use highquality loudspeakers with a straight response characteristic from 45 Hz to 20 kHz .

This article presents a small enclosure of 21 volume that for all its simplicity is eminently suitable for use as a surround-sound loudspeaker.

The drive unit is a wideband Monacor Type SP45 with a diameter of 75 mm which retails at about \(£ 6\) to \(£ 8\). In spite of its modest di-

1

mensions, the SP45 has (relatively) excellent reproduction properties. It can handle up to 40 W and its frequency range is a commendable 100 Hz to 15 kHz . Figure 1 shows the frequency response curve of the SP45 fitted in the enclosure. The curve shows only one weakness: a 5 dB dip above 3.5 kHz . In view of the earlier stated bandwidth limitation, this is hardly a serious flaw, however.

Figure 2 shows the construction plan of the enclosure. For the prototype, 8 mm thick plywood was used, but this is, of course, not mandatory: what is important is that the inside dimensions remain \(84 \times 154 \times 184 \mathrm{~mm}\).

The bass reflex gate consists of a 43 mm long piece of PVC tube with O/D of 32 mm and \(\mathrm{I} / \mathrm{D}\) of 25.5 mm . If this proves difficult to obtain, use a piece of PVC tube with the

2

more common o/D of 40 mm and an I/D of 33.6 mm , but the length must then be increased to 82.5 mm . Since the pipe is then very close to the rear wall of the enclosure, it is advisable to increase the depth of the box by 20 mm and re-
duce the other dimensions accordingly: the volume must remain the same.

The SP45 is available with an \(8 \Omega\) or a \(4 \Omega\) voice coil. Since the surround-sound decoder published in this magazine last year must be loaded
with at least \(8 \Omega\), it is advisable to use two or more \(4 \Omega\) types in series.

Finally, the enclosure must be filled with suitable wadding, but make sure that the reflex pipe stays clear.

\section*{serial 3-wire control}

For specific applications, there are ICs whose operation may be influenced by the programming of the control registers. Communication between such an IC and the processor is usually via a serial 3-wire link.

The present circuit uses a Type CS3310. The two 8-bit words are converted into serial form by two shift registers Type 4021. This enables the code set by DIP switches \(\mathrm{S}_{2}\) and \(S_{3}\) to be sent to the CS3310.

The parallel-load input (pin 9) operates asynchronously. This means that that the data applied to parallel inputs A-H are accepted by the internal registers as long as pin 9 is high. If this pin is made low, that data are shifted into the direction of \(\mathrm{OH}(\operatorname{pin} 3)\) at the next leading edge of the clock signal. At that same instant, that data at the serial input (pin 11) is accepted by QA . Since QH of \(\mathrm{IC}_{3}\) is linked to the serial input of \(\mathrm{IC}_{4}\), all 16 bits of data are shifted to QH after 16 clock pulses.

The clock is provided by oscillator/scaler \(\mathrm{IC}_{2}\). The first branch of the divider is \(Q_{3}\). The shifting and accepting of

1


2

\(\square\)
SCLK

DATA

the data always takes place at the leading edge of the clock. To ensure that the edge oc-
curs in the middle of a data bit, the clock for the shift registers is inverted by \(\mathrm{IC}_{1 \mathrm{~d}}\).

The cycle is started when \(\mathrm{S} / \mathrm{R}\) bistable \(\mathrm{IC}_{1 \mathrm{a}}-\mathrm{IC}_{1 \mathrm{~b}}\) is set with \(\mathrm{S}_{1}\). When it is completed,
after about 120 ms , the output of \(\mathrm{IC}_{1 \mathrm{~b}}\) goes low, whereupon the shift registers transfer to the serial mode and \(\mathrm{IC}_{2}\) is enabled: \(\overline{\mathrm{Cs}}\) is then active.

After \(Q_{3}\) has been high 16 times, the bistable is reset via \(\mathrm{Q}_{8}\) and inverter \(\mathrm{IC}_{1 \mathrm{c}}\). About \(20-30 \mu \mathrm{~s}\) after the last trailing edge of the clock, \(\overline{\mathrm{CS}}\) becomes inactive.

The current drain of the circuit is determined primarily by \(\mathrm{R}_{5}\) and \(\mathrm{R}_{6}\) : with closed DIP switches, it is \(\leq 0.1 \mathrm{~mA}\).
[T. Giesberts - 964080]

\section*{thrifty mains-slave unit}

A mains-slave unit has a master outlet and one or more slave outlets. The master outlet is connected permanently to the mains, but the slave outlets via a relay (or similar switching element). When the equipment connected to the master outlet is switched on, the mains-slave unit detects that a current flows through the transformer and arranges for the slave outlets to be connected to the mains as well.

There are many types and varieties of mains-slave, most of which have in common that even in the quiescent state they use a certain amount of power. The present circuit only draws power when the equipment connected to the slave outlet(s) is switched on. Even then, it draws only 25 mA from the mains.

In the diagram, \(\mathrm{K}_{1}\) is the mains input connector, \(\mathrm{K}_{2}\) the master outlet, and \(K_{3}\) the slave outlet, which can, of course, apply the mains to a number of mains sockets.

Transformer \(\mathrm{Tr}_{1}\) functions as a current sensor. When the equipment connected to \(K_{2}\) is switched on, a voltage is induced across the secondary win ding. This voltage is rectified and smoothed by \(\mathrm{D}_{5 \mathrm{p}}\), \(\mathrm{D}^{6}, \mathrm{C}_{5}\) and \(\mathrm{C}_{6}\), and then applied via sensitivity control \(\mathrm{P}_{1}\) to the gate of \(\mathrm{T}_{1}\) (a \(500-\mathrm{V}\) MOSFET). This transistor is switched on, causing relay \(\mathrm{Re}_{1}\) to be energized. The relay contacts then connect the mains voltage to \(\mathrm{K}_{3}\). The relay specified can switch up to 2000 VA .

The transformer can detect currents of up to 30 mA . This sensitivity is attained by resonant circuit \(\mathrm{Tr}_{1}-\mathrm{C}_{3}-\mathrm{C}_{4}\) \((f=50 \mathrm{~Hz})\). This arrangements also prevents any highfrequency interference affecting the proper operation of the circuit. The capacitors may be replaced by a \(\sin\) gle bipolar electrolytic type of \(10 \mu \mathrm{~F}, 63 \mathrm{~V}\).

The rectifier is a cascade type, whose output voltage is equal to the peak-to-peak potential across \(\mathrm{C}_{3}-\mathrm{C}_{4}\).

Resistor \(\mathrm{R}_{4}\) and diode \(\mathrm{D}_{7}\) protect the gate of \(\mathrm{T}_{1}\) against high voltages.

The sensitivity of the circuit is set with \(P_{1}\) so that when the master equipment is switched on, the relay is just energized.

The supply voltage for the relay and \(\mathrm{T}_{1}\) is derived directly from the mains by the reactance of \(\mathrm{C}_{1}\) and \(\mathrm{C}_{2}\) and bridge rectifier \(\mathrm{D}_{1}-\mathrm{D}_{4}\). Capacitor \(\mathrm{C}_{7}\) smooths the potential across the relay.

Bear in mind that when the gate voltage for \(T_{1}\) is too low to switch on the transistor, the full mains voltage is dropped across it.

Resistors \(R_{2}\) and \(R_{3}\) dis-
charge \(C_{1}\) and \(C_{2}\) in the quiescent state to prevent any dangerous potential remaining at the input.

The transformer is wound on an ETD29 former and E27
insulating tape. With a wire as specified for the primary, the master equipment may draw a current of up to 2 A .

As always with mains-operated equipment, the great-

core material. The primary winding consists of 24 turns of 0.8 mm enamelled copper wire, and the secondary of 500 turns of 0.2 mm enamelled copper wire. Wind the secondary first, cover it with a layer of insulating tape, then wind the primary over this and cover this also with a layer of
est care should be taken in the construction. Always make sure that no mains-carrying parts can be touched and that the distance between such parts is at least 3 mm .
[T. Giesberts - 964102]

\section*{mains voltage 'cleaner'}

Some people are worried by the contamination of the environment by electric fields. A few even speak of 'electrosmog' and are even suspicious of the radiation by the domestic mains circuits. The cleaner presented here is intended for those who want to reduce any risk they run by exposure to the latter radiation. The circuit breaks, for instance, the wiring in bedrooms or other places where no mains voltage is required for certain periods.

In the quiescent state, the mains circuit between \(\mathrm{K}_{1}\) and \(\mathrm{K}_{2}\) is broken by the contact of relay \(\mathrm{Re}_{1}\). Instead of the mains, the contact places a direct voltage (no radiation!) of 12 V on to \(\mathrm{K}_{1}\). This auxiliary voltage makes it possible for the mains voltage to be restored as soon as this is required. When, for instance, an appliance, such as a bedside light, connected to \(\mathrm{K}_{1}\), is switched on, the auxiliary voltage will cause a small current to flow, which results in a potential drop of about 0.2 V across diodes \(\mathrm{D}_{1}\) and \(\mathrm{D}_{2}\). Shunt resistor \(\mathrm{R}_{1}\) suppresses any voltage peaks.

The drop across the diodes is applied to the noninverting input of comparator \(\mathrm{IC}_{1 \mathrm{a}}\). The switching threshold of this op amp is arranged at about 0.1 V by resistors \(\mathrm{R}_{3}\) and \(R_{4}\), to reduce the effect of spurious voltages, such as the offset voltage of the op amp, to a minimum.

The comparator output is applied to a simple peak detector formed by network \(\mathrm{C}_{1}-\mathrm{D}_{3}\). When the circuit is active, the potential across \(\mathrm{C}_{1}\) is about +10 V . The output of comparator \(\mathrm{IC}_{1 \mathrm{~b}}\) is then high, so that \(\mathrm{T}_{1}\) conducts, which results in the relay being energized. \(K_{1}\) is then isolated from the 12 V line and connected to \(\mathrm{K}_{2}\), so that mains voltage is applied to it.

When the load (lamp) is switched off, \(\mathrm{C}_{1}\) is discharged via \(R_{5}\), so that after a short while comparator \(\mathrm{IC}_{1 \mathrm{~b}}\) changes state, whereupon the relay is deenergized again.

The power supply for the circuit is traditional. Note that regulator \(\mathrm{IC}_{2}\) in the positive line is loaded more heav-

ily than \(\mathrm{IC}_{3}\) in the negative line.

The circuit is best built on the pCB shown. Diodes \(D_{1}\) and \(\mathrm{D}_{2}\) must be mounted (insulated!) on a common heat
\(\operatorname{sink}\left(\geq 5 \mathrm{~K} \mathrm{~W}^{-1}\right)\).
When the unit has been checked thoroughly, it must be fitted in a non-metal enclosure. When this has been done, connect it to the central
junction box for the relevant location.

Note that the unit is of no use in locations with a ring circuit.
[A. Pöschl - 964070]


\section*{PARTS LIST}

Resistors:
\(\mathrm{R}_{1}=1 \mathrm{k} \Omega\)
\(\mathrm{R}_{2}=100 \mathrm{k} \Omega\)
\(\mathrm{R}_{3}=120 \mathrm{k} \Omega\)
\(\mathrm{R}_{4}=1.2 \mathrm{k} \Omega\)
\(\mathrm{R}_{5}=1 \mathrm{M} \Omega\)
\(\mathrm{R}_{6}=10 \mathrm{k} \Omega\)

\section*{Capacitors:}
\(\mathrm{C}_{1}=220 \mathrm{nF}\)
\(\mathrm{C}_{2}, \mathrm{C}_{3}=470 \mu \mathrm{~F}, 25 \mathrm{~V}\), radial
\(\mathrm{C}_{4}-\mathrm{C}_{7}=100 \mathrm{nF}\), high stability

\section*{Semiconductors:}
\(\mathrm{D}_{1}, \mathrm{D}_{2}=\) BYW29-100
\(D_{3}=1\) N4148
\(\mathrm{D}_{4}-\mathrm{D}_{8}=1 \mathrm{~N} 4001\)
\(\mathrm{T}_{1}=\mathrm{BD} 679\)


Integrated Circuits:
\(\mathrm{IC}_{1}=\) TL082
\(\mathrm{IC}_{2}=7812\)
\(\mathrm{IC}_{3}=7912\)

\section*{Miscellaneous:}
\(\mathrm{K}_{1}, \mathrm{~K}_{2}=3\)-way terminal block, pitch 7.5 mm \(F_{1}=\) fuse, 8 A , slow, with holder for board mounting \(F_{2}=\) fuse, 50 mA , slow, with holder for board mounting \(R e_{1}=\) relay, \(12 \mathrm{~V}, 8 \mathrm{~A}\), with one change-over contact
\(\mathrm{Tr}_{1}=\) mains transformer, \(2 \times 15 \mathrm{~V}, 4.5 \mathrm{VA}\) secondary, e.g. Velleman (Maplin) Type 2150050M Heat sink \(\geq 5 \mathrm{KW}^{-1}\), e.g. Fischer SK129/38 (from Dau)
Enclosure \(150 \times 80 \times 55 \mathrm{~mm}\), e.g. Bopla E440

PCB Order No. 964070 (see
Readers Services)



Most of you will be familiar with the classic resistor-capacitor combination which serves to reset a microprocessor or -controller. Unfortunately, these power-on circuits do not always function reliably. The enhanced power-on reset (POR) circuit shown here is suitable for 'ac-tive-low reset' controllers, and has an advantage over the classic R-C combination in that it keeps the processor reset until the supply voltage has reached the nominal value. That hap-

\section*{alternative power-on reset circuit}
pens because transistor T1 does not conduct and pull the reset input high until potential divider R1-R2 supplies a sufficiently high base voltage. The result of the improved poweron reset timing is a much more reliable start of some microcontrollers, which may be essential in unattended systems where start-up faults can not be tolerated.


The operation of the circuit is perfected by capacitor Cl , which ensures that the reset line does not go high until the full supply voltage has been present for some time. The value of C 1 depends to some extent on the application |s the value of \(10 \mu \mathrm{~F}\) is given as guidance only.
[Source: Parallax Inc. - 964068]

\section*{harmonics generator}

This simple circuit acts as frequency multiplier which converts any sloped input waveform into a distorted output waveform whose frequency spectrum is marked by a rich harmonics content. The input frequency does not disappear from the spectrum, however.

When a pure sinewave input signal is applied, the circuit generates odd harmonics only. That is, in theory, and assuming that the two input comparators are exactly equal, with \(0-\mathrm{V}\) reference settings at their -inputs. The push-pull outputs of comparators IC1b and IC1a then
supply differential signals to adder IC2, which cancels out even-numbered harmonics. For different mark/space ratios of the comparator output signals, as set with P1 and P2, the harmonic spectrum changes. A duty factor of 0.25 , for instance, will cause the circuit to supply the second, sixth and tenth harmonics, but not the fourth one. The spectrum function is then written as \(\sin (x) / x\).

For pulse-shaped alternating input voltages, the output spectrum may also be described by \(\sin (\mathrm{x}) / \mathrm{x}\), but only the odd-numbered harmonics are generated.

The reference levels for the input comparators determine the output waveform. The desired degree of distortion of the input waveform is, therefore, adjusted with the two presets. For the best possible accuracy of the adding operation, the input opamps should have matching a.c. performance. For the same reason, R2 and R3
should be matched to within \(1 \%\).

Current consumption of the circuit is smaller than 5 mA from a regulated symmetrical 5volt supply. The level of the input waveform should be stable and smaller than \(5 \mathrm{~V}_{\text {peak }}\).
[Design by H. Bonekamp - 964069]

\(\square\) water level monitor

When combining water and electricity it is essential that the current flow be a.c., else electrolysis will eat one electrode away. This circuit was devised to give an audible alarm when a water tank was approaching empty. A switch was then changed over, a pump turned on manually, and when the alarm sounded again the pump was switched off and the switch reset, again manually. Sure, it would have been an easy matter to automate the process, but that was not considered appropriate for the application.

The circuit consists of two conventional CMOS oscillator gate pairs as found in the text books. With the switch in the 'low' position, gates IC1a and IC1d provide an alternating current flow through \(\mathrm{C} 2, \mathrm{R} 3\), the common electrode, through the water and the low elec-
trode, to earth. When the water level drops, the circuit to earth is interrupted and the a.c. is then fed via S1 to the junction of D1-D2. This charges C3 so that pin 5 of IC1b goes positive, causing gates IClb and ICl c to start oscillating. The audible transducer is an a.c. buzzer, although a telephone earpiece may also be used.

The switch is then moved to the 'high' position waiting for the tank to fill. Pin 6 of IC1 is then at ground potential via R5, waiting for the tank to fill and connect the common and high electrodes via the water. The a.c. then flows through D2 to once again sound the alarm. The pump is turned off and S1 restored to sense empty once more. There is no setting up to the circuit, although the rate of charge of capacitor C3 may be changed

by altering the value of R3.
Power supply for the circuit may be from 5 to 12 volts derived from a standard transformer/rectifier/capacitor setup or from battery. With the latter an on/off switch is recom-
mended despite the low current drain of about 0.3 mA in standby mode, and 1 mA when the buzzer sounds. No regulation is necessary.
[Design by D. Nelson 964048]

\section*{car lights monitor}

The Highway Code and Road Traffic Act stipulate that before starting a journey in his/her car a driver must verify that all the car's lights are working correctly. Many modern cars are. therefore, fitted with a monitor panel on the dashboard. It is highly unlikely that many drivers of cars not so equipped ever do this regularly as evinced by the number of cars one sees on the road with defect lights, particularly brake warning lights. The failure of such lights is at best a nuisance and at worst a danger to other road users.

It is relatively simple to construct an effective lights monitor. The only proviso for this is that the fuse terminals of the electric circuits are in easy reach: this is normally the case.

The design is based on the (tiny) voltage drop across the fuse in series with the relevant lamps. It is, of course, essential to know which lamps are connected to a particular fuse and how much drop the current causes across the fuse.

As a rule, side lights and rear lights use one common fuse, as do the two (in many cases, three) brake warning lights. Headlights normally
use two-filament lamps rated at \(55-60\) W. Each filament is protected by a separate 10 A fuse. There are, of course, variations on this, but these do not alter the

principle of the circuit.
The car's battery voltage, \(U_{\mathrm{B}}\), less the voltage drop across the fuse, \(U_{\mathrm{f}}\), is applied to the non-inverting input of comparator \(\mathrm{IC}_{1}\). The constant drop, \(U_{\mathrm{D}}\), across diode diode \(\mathrm{D}_{1}\) is 0.6 V . A portion of \(U_{\mathrm{D}}\), determined by poten-
tial divider \(\mathrm{R}_{3}-\mathrm{R}_{2}\) is deducted from \(U_{\mathrm{B}}\), and the remaining voltage, that is, \(U_{\mathrm{B}}-U_{\mathrm{D}}\), is applied to the inverting input of the comparator.

The output of the com-
parator is low (lights on, LED off) as long as \(U_{\mathrm{f}}>U_{\mathrm{D}}\) and high (lamp defect, LED on) when \(U_{\mathrm{f}}<U_{\mathrm{D}}\).

The value of \(R_{3}\) must be determined empirically. This because the very small level of \(U_{\mathrm{f}}\) depends on many factors and cannot, therefore, be
readily predicted. In the prototype, it was 6 mV in the case of 10 W bulbs, and 25 mV in the case of 42 W bulbs.

Because of the tiny voltage differential at the inputs of the comparator, the offset adjustment with \(P_{1}\) is very precise. Set the control carefully to obtain 0 mV output with the inputs short-circuited.

Note that it is imperative that the op amp is a Type TL081 or its dual version TL082 since these op amps are some of the very few that can handle the input voltage right up to the upper limit of the supply voltage.

The circuit draws only a small current: about 15 mA when the LED lights.

In case the light switch is located between battery and fuse, as shown in the diagram, the op amp is powered only when the lights are switched on. In the case of brake lights, the op amp needs to be powered by the switched positive supply line.

In the (unlikely) case that a large and a small load use a common fuse, the present circuit is not of much use, since the failing of the small lamp will hardly be detectable.
[U. Mūnch - 964049]

When voltages are measured, it is not always necessary to find the exact value Often, it is sufficient to check whether a potential lies within a certain range of voltages. The present circuit indicates by means of three LEDS whether a voltage is greater than 4 V , 5.7 V or 7.4 V .

The reference potential is provided by a series network of diodes \(\mathrm{D}_{4}-\mathrm{D}_{9}\). The Leds are connected to various junctions in this network. The measurand is applied to the LEDS via emitter follower \(\mathrm{T}_{1}\) and series resistors.

Any one LED will light only if the input voltage exceeds the sum of the base-emitter junction of \(T_{1}\), the drop

\section*{voltage monitor}
across the relevant series resistor, the LED voltage, and the the drop across the diodes following the LED. In this way the following potentials are obtained:
\(\mathrm{D}_{3}: 4 \mathrm{~V}\)
\(\left(2 U_{\mathrm{D}}+U_{\mathrm{D} 3}+U_{\mathrm{R} 4}+U_{\mathrm{be}}\right)\);
\(\mathrm{D}_{4}: 5.7 \mathrm{~V}\)
\(\left(4 U_{\mathrm{D}}+U_{\mathrm{D} 4}+U_{\mathrm{R} 3}+U_{\text {be }}\right) ;\)
\(\mathrm{D}_{5}: 7.4 \mathrm{~V}\)
\(\left(6 U_{\mathrm{D}}+U_{\mathrm{D} 5}+U_{\mathrm{R} 2}+U_{\text {be }}\right)\).
A slight drawback of the circuit is that the light intensity of the Leds does not remain constant when the input voltage changes, but that is a small price to pay for such a very simple design.
[H. Bonekamp -965054]
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