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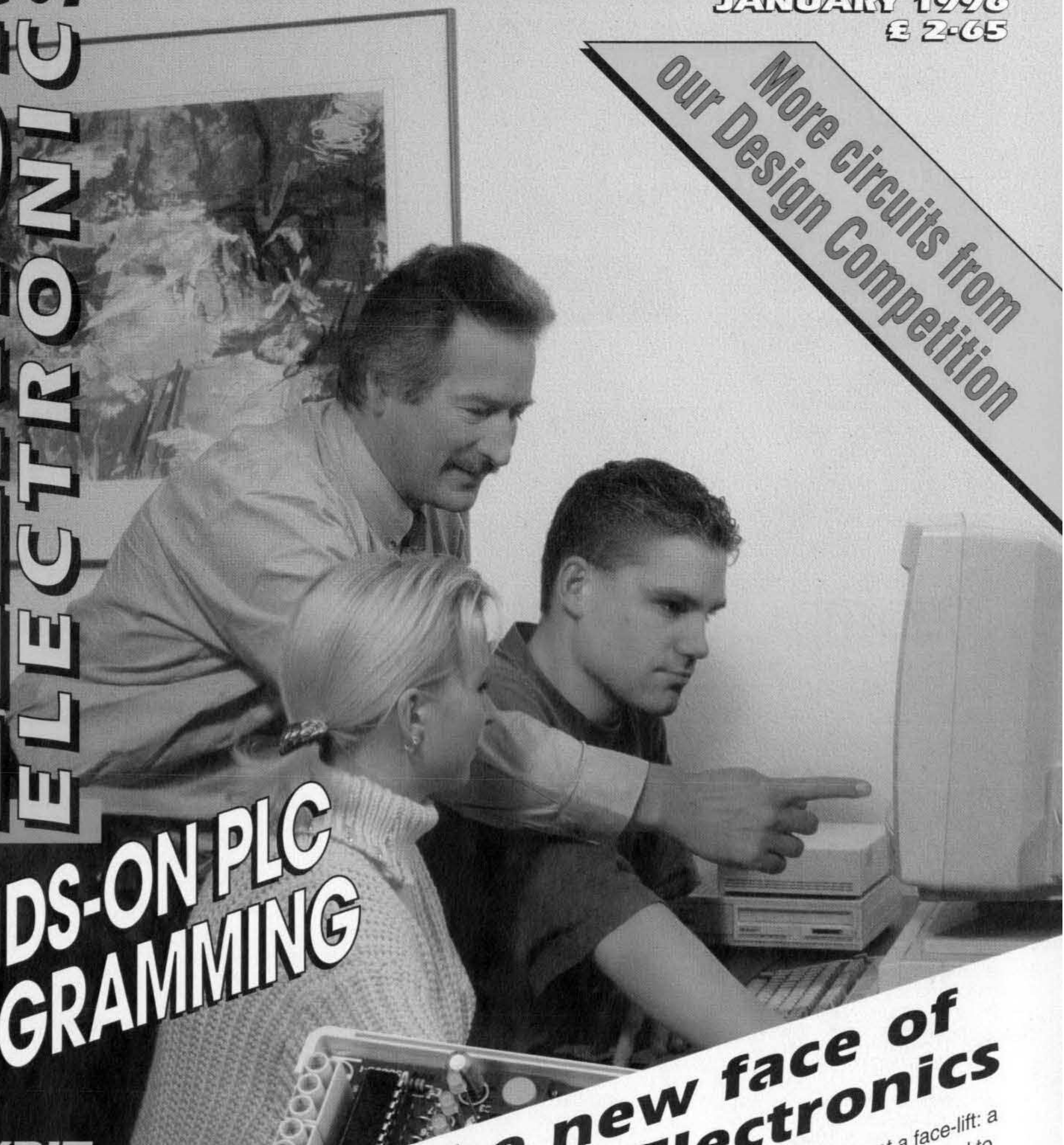

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COMPONENT TESTER

The new face of Elektor Electronics

Starting with the March 1996 issue. *Elektor Electronics* will get a face-lift: a new masthead and a new cover layout. This 'second' cover is intended to give you an impression of what it will look like.Apart from a facelift, the magazine will also undergo some body repairs. These will consist of an altered article layout, and an improvement in the presentation and selection of information. All these changes are intended to make Europe's largest international electronicsmonthly more interesting, more lucid and more reader-friendly for an increasing circle of readers. Do not miss the March issue when you will see all these improvements and changes in reality.

Pierre Kersemakers (Editor-in-Chief/Publisher)

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HANDS-ON PLC PROGRAMMING (PART 1)

Last month we described a low-cost Programmable Logic Controller system, the Micro PLC. This system uses an instruction set which is largely similar to that of the well-known SAIA PCs from Landls & Gyr. The short course we start this month begins with a general description of a typical industrial PLC. Next, we leave the hardware altogether, and concentrate on software only.

PART 1: THE INDUSTRIAL PLC

Software by J. Joostens

IN last month's article on the Micro PLC it was explained that a PLC is basically a computer which has a host of facilities geared to controlling an industrial process in a simple but most efficient way. This applies equally to the Micro PLC, although you have to take its modest setup into account. Arguably, the Micro PLC is not suitable for the control of a complex industrial process involving a large number of operations. It is great, however, for many smaller applications, for instance, a traffic lights controller.

General layout of a PLC

Before attempting to explore the exact operation of a PLC, it may be useful to have a look at the block diagram in **Fig. 1**. This diagram shows all major parts of the unit, arranged in a logical layout.

The **control system** of the PLC is the program core which arranges the overall operation of the PLC. This core is usually located in a ROM or EPROM. With the Micro PLC, it is loaded in the processor's internal EPROM memory. Thanks to the control program, the user is able to write an application program which may be read, interpreted and, of course, executed by the PLC. Apart from that function, the control system also takes care of the communication with the I/O functions and the peripherals connected to the system. With an industrial PLC, the control system is usually so powerful that the user is given the opportunity to debug his/her software.

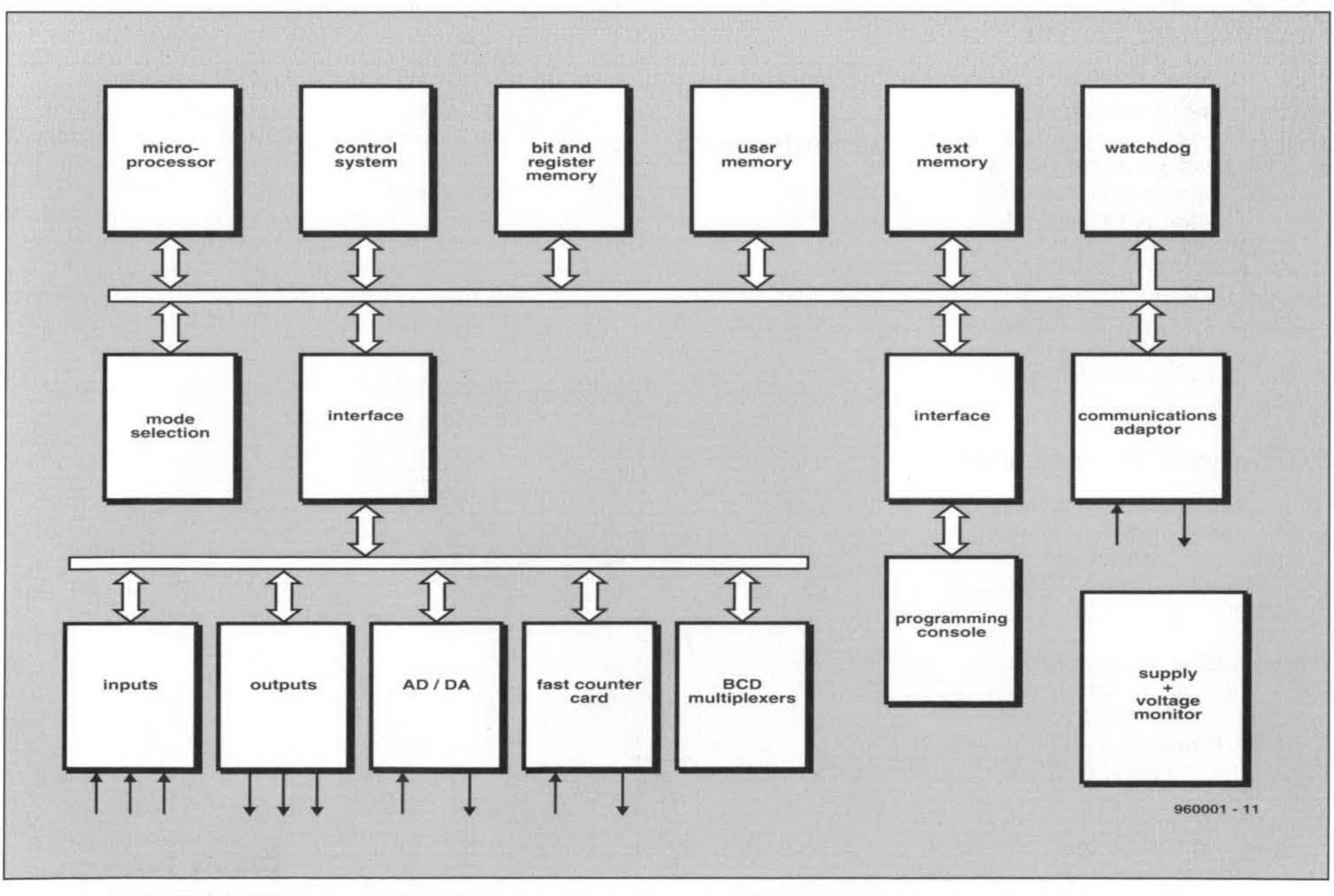


Fig. 1. Block diagram of a typical industrial PLC. The function of the blocks shown here is discussed in the text.

Bit and register memories may be found in most PLCs. These memories enable current values of variables to be stored while the program is being executed. A special location is reserved for the accumulator, which is a register used by nearly all instructions.

The register memory allows the storage of different types of number, both binary and BCD. The size of the memory location may be 8 bits (byte) or 16 bits (word). Register memories are mainly used for the processing of analogue signals, and the reading and processing of BCD values. If available in the PLC, timers, counters and shift registers also make use of the internal registers.

The **user memory** contains the code for the application program to be run by the PLC. Usually, this is a RAM area with battery backup. In many cases, PLCs also allow the user program to be stored in EPROM or EEPROM. A special ZIF socket then enables system developers to supply a PLC which is tailored and ready-programmed for a specific application.

The **text memory** is used to define a number of messages which the PLC, depending on certain situations, sends to a terminal or a printer, with or without additional information. It is usually possible to incorporate the register contents or the time into the message. Here is an example of such a message:

```
*** ERROR 04 *** Oven temperature
too high!
```

The **watchdog** increases the stability of the applications running on the PLC. As soon as the watchdog is active, the PlC program is forced to address the timer at certain intervals. If that does not happen in time, for instance, when the system has crashed, the watchdog is actuated, and generates an alarm signal for the user. If desired, the watchdog may also generate a signal to re-initialize the PLC, and restart the user program.

PLC modes of operation

A PLC may operate in different modes which may be actuated via a switch, or a command received via the RS232 port. The main modes found on most PLCs are:

Programming Mode: this mode enables the user to put the application program into the PLC's memory.

Execute Program: in this mode, the PLC actually executes the user program.

Single-step mode: this allows the user program to be executed step-by-step. In some cases PLCs may use breakpoints. This mode is very useful for the debugging of a program.

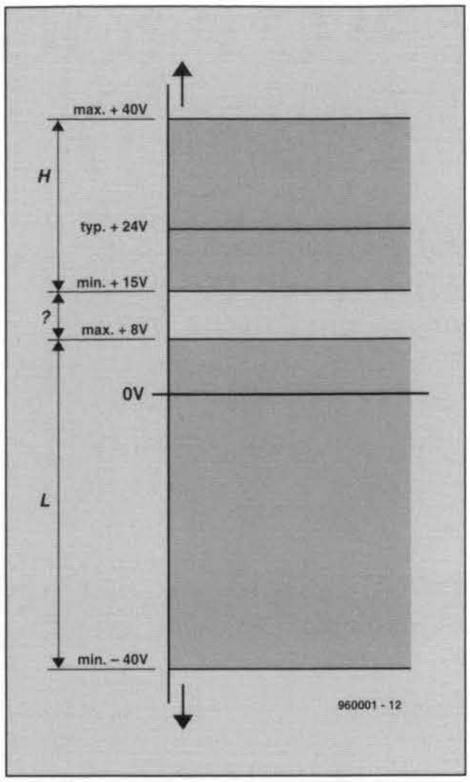


Fig. 2. The switching levels pertaining to a PLC input are clearly defined. Only a level between +8 V and +15 V does not have a clear logic level.

Manual mode: this enables outputs to be switched on and off manually. This function comes in handy while testing fans, valves, signal lights, etc. which are connected to the PLC's output.

About inputs

Ordinary PLC inputs play an important role in the process of reading switch states and detector states. Depending on the application, PLC inputs may be realized in a number of ways. Most inputs, however, are compatible with direct voltages between 0 V and 24 V. In rare cases, PLC inputs may even be suitable for direct connection to the mains. **Figure 2** shows the input characteristic of a typical PLC input using switching levels of 0 V and 24 V. Note that the range between 8 V and 15 V is not defined. Apart from differences as regards the input voltage levels, PLC inputs may also be classified according to the presence or absence of electrical isolation. The drawing in **Fig. 3** shows how a 24-V PLC input may be provided with electrical isolation. The permissible input voltage may lie between –40 VDC and +10 VDC. The inputs are symmetrical for direct voltages as well as RF noise. The integrated RF filter suppresses noise caused by electromagnetic interference. The actual electrical isolation goes on account of an opto-isolator, whose output signal is filtered by a simple *RC* network which introduces a delay of 8 to 10 ms. Thanks to this delay, even pulsating signals applied to the input are recognized as a direct voltage.

About outputs

The outputs of a PLC are used to switch loads such as magnetic valves, small motors and signal lights. Just as with the inputs, PLCs differ in respect of the practical realization of their outputs. Usually, the outputs have either an open collector, a relay or a triac. Most open-collector outputs are capable of switching voltages between 5 and 36 VDC at a maximum current of 1 A. Here, too, there are versions with and without electrical isolation.

In practice, there is a large difference between switching the positive voltage and switching ground via open-collector outputs. With switching

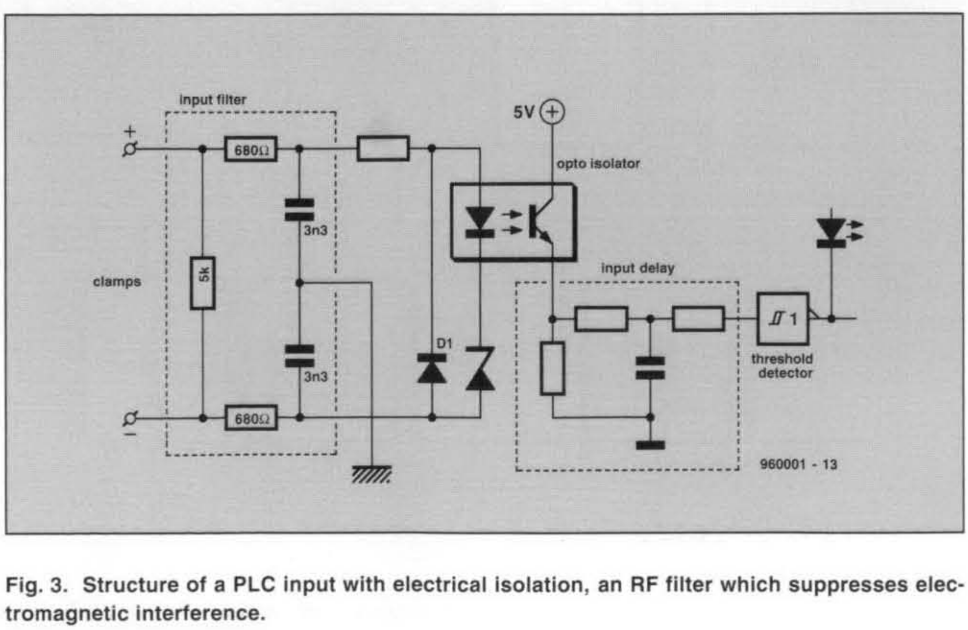


Fig. 3. Structure of a PLC input with electrical isolation, an RF filter which suppresses electromagnetic interference.

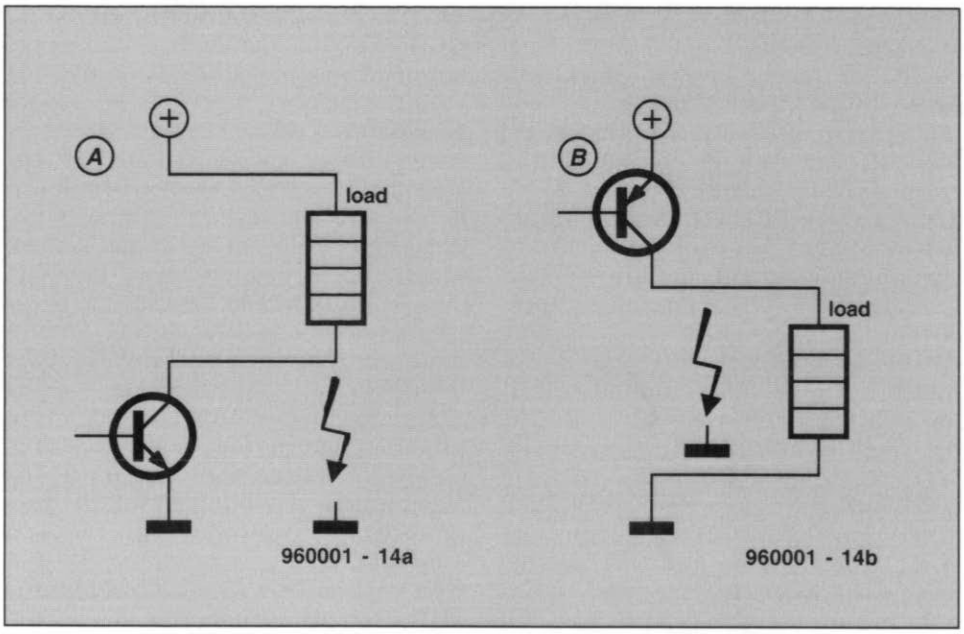


Fig. 4. The left-hand section of this drawing (a) shows the results of a short-circuit to ground on a an open-collector output which switches to ground. The right-hand section (b) shows you what happens if an output is used which switches the supply voltage.

ground, a short-circuit to ground (system chassis) may cause unwanted actuation of the load (**Fig. 4a**). This may give rise to very dangerous situations. Switching the positive voltage (**Fig. 4b**) has no such risks. if such an output is active, and a short-circuit to ground occurs, the protection in the supply line will be actuated. It is then impossible for the actual load to be actuated erroneously. It will be clear that this type of safety precaution is essential in the industrial environment where cables and equipment are subject to heavy mechanical stress.

Counting quickly

As a result of their relative slowness, PLC inputs can not be used to count more than about 100 pulses per second. Hence, special cards have been developed for this purpose. Such cards are capable of counting up to 10,000 pulses per second, independent of the PLC's microcontroller, and may be programmed to warn the PLC if a predetermined number of pulses is reached. Most of these cards may be used to read the position of incremental angle encoders, often coupled with the detection of the rotational direction.

Sometimes these cards are equipped with special outputs for the control of one or more stepper motors. If that is the case, a number of parameters for the driving of stepper motors, such as acceleration and deceleration, may be defined by the user.

A-D and D-A cards

These cards are employed whenever the PLC has to process analogue quantities such as pressure, electrical voltage and current, temperature, speed, rotational speed, etc. The opposite is also possible, i.e., a card may be used to drive analogue loads such as frequency controls, power controls, and positioning systems. The A-to-D card converts an analogue electrical value (voltage or current) supplied by, for example, a sensor, into a digital value (at a resolution of 8, 12 or sometimes even 16 bits). With the aid of a D-A card, the PLC is capable of generating analogue voltages. The voltage and current ranges used for analogue signal processing in the industry are, in general, as follows:

Voltage
–5 to +5 V
–10 to +10 V
0 to +5 V
0 to +10 V

Current
–20 to +20 mA
0 to +20 mA
+4 to +20 mA

Finishing touches

It is sometimes required for the user to be able to change certain parameters, for instance, delay times, wile the program is running. For that purpose, most PLCs have an externally accessible switch whose state is interrogated frequently by the program. Thanks to this arrangement, it is not necessary to re-program the PLC any time one of the parameters has to be changed.

The PLC is usually programmed via a special programming console. This separate unit contains a display and is only connected to the PLC during programming. It allows parameters to be modified, a program to be loaded, the memory to be examined, and any errors to be removed from the program.

A standard feature on all modern PLCs is a communication interface in the form of a serial port. This may be an RS232, RS485, or current loop type. Using this port, the PLC communicates with peripherals such as terminals, printers, measurement equipment, or a PC. An optional barcode reader is an important aid when

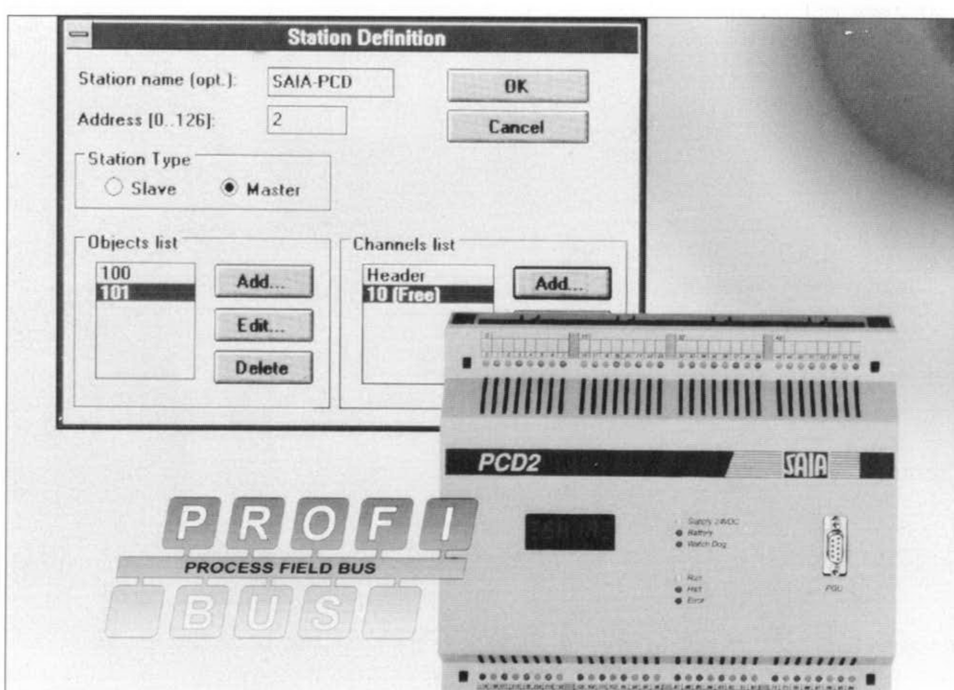


Fig. 5. An industrial PLC from Landis & Gyr.

the system is programmed to sort products on a conveyer belt in a warehouse.

Vanity features

Today's PLCs may be taken up in a network just like PCs, but only if a special network card is installed. In principle, it is even possible to incorporate PLCs into an existing PC network. Furthermore, a number of special buses are in use. These so-called field buses, for instance, Interbus-S or Profibus, see rapid acceptance and increasing popularity. Most PLCs have a modular structure. They consist of a basic system which can be given extra functionality by adding insertion cards. The basic system comprises a power supply, a CPU, some memory and a limited number of inputs and outputs. In some cases, there is even a fast counter input and an AD/DA card. Modern PLCs can be fitted with 128 inputs and outputs without problems.

The Micro PLC

After a cursory look at the structure and applications of industrial PLCs it is time to get back to our Micro PLC. In the previous instalment we already printed a quick rundown of the instruction set. This month we discuss each instruction in detail.

NOP no operation
STH reads the specified input, output or the specified auxiliary memory, and copies the contents to the accumulator.
STL as STH, however the level read is inverted before it is copied into the accumulator.
ANH performs a logic function between the current accumulator contents and the level read from the specified input, output, or aux. memory.
ANL as ANH, however the AND function is performed between the current accumulator contents and the inverted level read from the specified input, output, or aux. memory.
ORH Performs a logic OR operation between the current accumulator contents and the level read from the specified input, output or aux. memory.
ORL as ORH, however the OR function is performed between the current accumulator contents and the inverted level read from the specified input, output, or aux. memory.
XOR performs a logic XOR function between the current accumulator contents and the level read from the specified input, output or aux. memory.
CPA inverts the current contents of the accumulator.
OUT writes the level contained in the accumulator to the specified output or aux. memory.
SEO writes a high level to the specified output or aux. memory.
REO writes a low level to the specified output or aux. memory.
CPO inverts the level of the specified output or aux. memory.
DLY generates delays between 0.1 s and 25 s. Operand indicates delay in 0.1 s.
ICR Copies specified operand into counter.
INC increments counter by 1.
DEC decrements counter by 1.
CCR compares contents of counter to specified operand. If the two are equal, the accumulator is set. If not, the accumulator is cleared (reset).
JMP jumps unconditionally to the specified location. Location should be between 16 and 63.
JIO jumps to specified location if accumulator has a high level. Location should be between 16 and 63. If the accumulator has a low level, the program simply continues with the next instruction.
JIZ jumps to specified location if accumulator has a low level. Location should be between 16 and 63. If the accumulator has a high level, the program simply continues with the next instruction.
WIH wait as long as specified input is high. This instruction may not refer to outputs or aux. memories.
WIL wait as long as specified input is low. This instruction may not refer to outputs or aux. memories.
WTO writes specified operand (between 0 and 63 binary) to the outputs (6 to 11).
SEA set accumulator.
REA reset accumulator.
RPM return from run mode to program mode.
VER transmits software version number via the serial interface.

External instructions in programming mode

chr(0) to chr(250): data; increased by one (for acknowledgement) and returned.
chr(251): returns the status of inputs 0 to 5 as a binary number (0-63), followed by a 'hash' character (#).
chr(252): returns the status of outputs 6 to 11 as a binary number (0-63), followed by a 'hash' character (#).
chr(253): expects a number between 0 and 63, and writes it to the outputs. On completion of this instruction, a # is returned.
chr(254): transmits the software version number in the form CR/LF<string> CR/LF '#'.
chr(255) ends programming mode, and switches to run mode.

About MicroPLC.exe

The program is launched as follows:

```
microplc.exe [options] <enter>
```

where the options are -com2, -com3 and -com4. The default option is com1. If a colour screen is used, you should use the DOS command SET COLOR=ON <enter> before running 'microplc'. Colour use may be switched off again by typing SET COLOR= <enter>. After starting the program

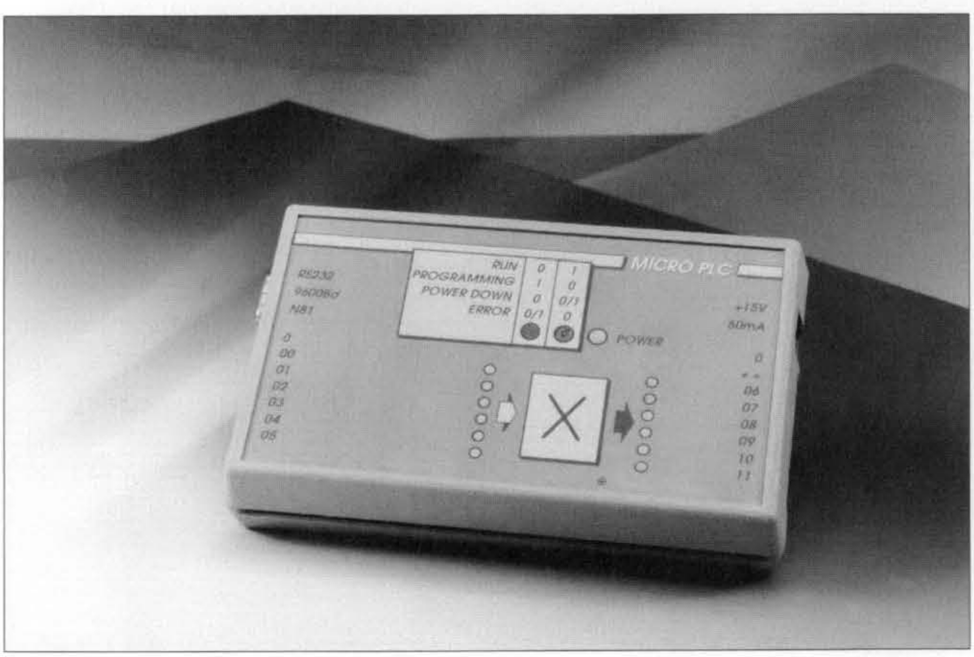


Fig. 6. The Micro PLC described in the December 1995 issue of Elektor Electronics is smaller and more compact than an industrial type. None the less, it will find many applications where it can be used successfully.

you are presented with a number of options, which may be selected via a menu.

Load Buffer with File
prompts you for a file name, and copies this file into the buffer. The length of the file must be 48 bytes (as generated by microplc).

Save buffer to File
writes data contained in the buffer to a file specified by the user. If the specified file name already exists, the user is notified.

Edit Buffer Contents
Mnemonics
allows the user to enter the program with the aid of mnemonics. Microplc always starts from location 16. The program can be made to return to the main menu by typing END. The program as entered is then available in numerical form in the buffer. Non-used program locations in the buffer are automatically filled with the value 26 (RPM, return to Program Mode). Because it is practically impossible to enter invalid instructions, this is the best way to enter PLC programs.

Numerical
allows the contents of one specific location in the buffer to be modified. This method may be used to make minor changes to the program. The user should ensure however that no invalid program steps are created.

Program Microplc
Download & Autostart
Buffer data are sent to the PLC via the serial link. When this option is selected, the program waits for the user to reset the PLC. If the transmission of the buffer contents does not start within two seconds after the PLC has been reset, the serial link has be checked. In that case, you may interrupt the program by pressing any key.

Restart Program
allows you to switch the PLC to run mode when the program to be executed is already in the PLC's memory, and the PLC itself is in programming mode.

Preset Outputs
ON
If on, this option causes the PLC outputs to be initialized with a certain value (preset value) before the actual program is started. This initialization is performed automatically when the menu options 'Download & Autostart' and 'Restart Program' are selected.

OFF
Turns the above option off. All outputs are off when the program is started.

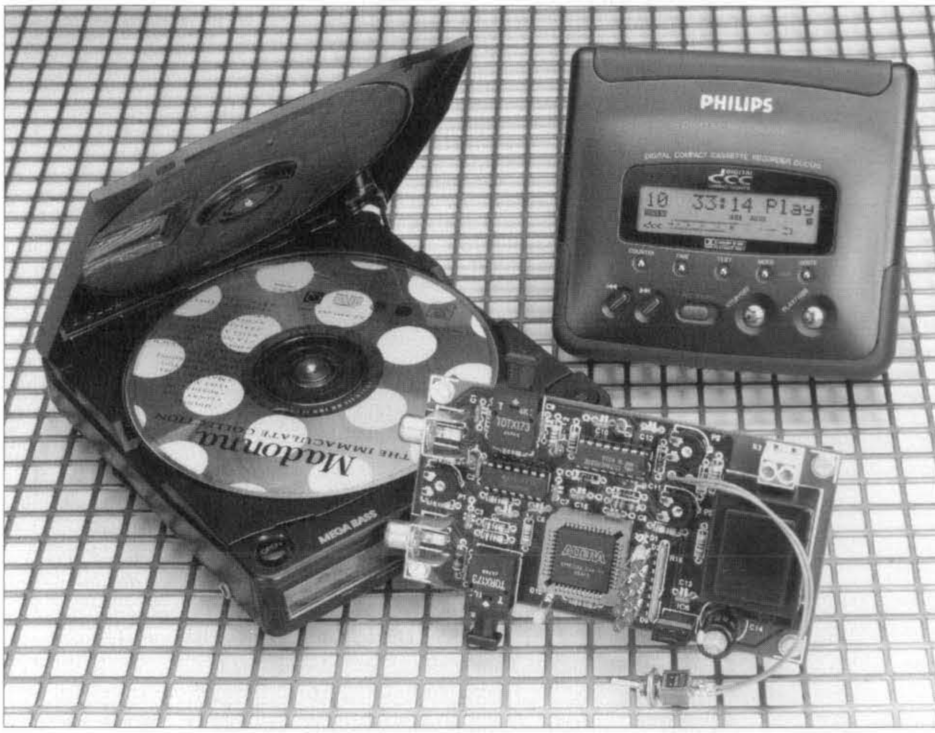
Reset Value
Enables the preset value on the outputs to be modified. The value is indicated in binary form.

Serial Port
allows you to change to another serial port than the one stated when the program was invoked. You may select one of COM1 through COM4.

Exit Microplc
leaves the program, and returns the PC to DOS.

That concludes the description of the instructions offered by the program. Some practical programming examples will be discussed in next month's instalment. (960001-1)

COPYBIT INVERTER



The copybit eliminator published in the February 1994 issue of this magazine has two drawbacks. The first of these is that it cannot be used without modifying the digital audio equipment. The second is clear from the revisit to the eliminator in the September 1995 issue: from time to time, the eliminator needs updating – it is not 'future-proof'. The copy-permit converter described in this article does not have these drawbacks

Design by W. Foede

Like the copybit eliminator published in this magazine in the February 1994 and September 1995 issues, the copybit inverter is an inexpensive and simple-to-build circuit for inverting the copybit in a digital S/PDIF* audio signal to enable users to copy (digitally) their own musical work many times without degradation by the SCMS**.

The inverter can be included in the S/PDIF link between any digital a.f. signal source (such as a DCC recorder, a CD player, a DSR receiver) and a (second) DCC recorder without the need of opening or modifying any of the equipment. During the copying, any copybit is inverted and at the same time the category code is altered. This means that the S/PDIF signal so modified is accepted by the recorder as if it comes from a CD player (so that unlimited copying of the signal becomes possible). The inverter also offers a number of other facilities, such as S/PDIF detection.

WARNING. The information in this article is intended solely for the recording, processing and copying of private musical work. The Editor and Publishers disclaim all responsibility for any use that may infringe any copyright vested in commercial compact discs and (digital) tape cassettes.

Category code

The coding of the S/PDIF has been described in detail in the article on the 'Copybit eliminator'. The following description is therefore limited to the most important aspects of it.

In all domestic audio equipment, the format uses sample frequencies of 32 kHz, 44.1 kHz and 48 kHz. These data contain, among others, information as to the copybit. The format reacts to the content of the S/PDIF. The SCMS, which inhibits multiple (digital) copying of the source signal, can be bypassed as shown in the flow diagram in **Fig. 1**. It is not sufficient to invert only copybit 1. As the diagram shows, when copying with category code 00 000 000 (general) takes place, for instance, the copybit is not sampled. This means that the recording has to be passed through a copybit eliminator a second time. It is, therefore, much safer to set the copybit to (or hold it at) 1 and assign to it the category code of an apparatus whose copybit is always sampled.

The present inverter always outputs the category code of a DAT or a CD, depending on the input signal. The code changes automatically, so that the subdata in the USER channel

Brief specification

- Opening or modification of the audio equipment not required
- 'Future-proof', since it is independent of the category code
- Unlimited (digital) copying of source material
- Optical or coaxial inputs and outputs as required
- S/PDIF detector
- Indication of the position of the copybit and automatic setting to 1 (= digital copying permitted)
- Indication of the category code and automatic setting to 10 000 000 (CD) or 11 000 000 (DAT)
- AES/EBU format can be copied
- Transparent USER-Subcode channel
- Indication as to whether operation is as converter or as inverter
- Minimal number of components
- Non-critical setting up without test instruments

* Sony/Philips Digital Interface Format – the consumer version of the AES/EBU standard. This standard was devised by the American Audio Engineering Society and the European Broadcasting Union to define the signal format, electrical characteristics and connectors to be used for digital interfaces between professional audio products.

** Serial Copy Management System.

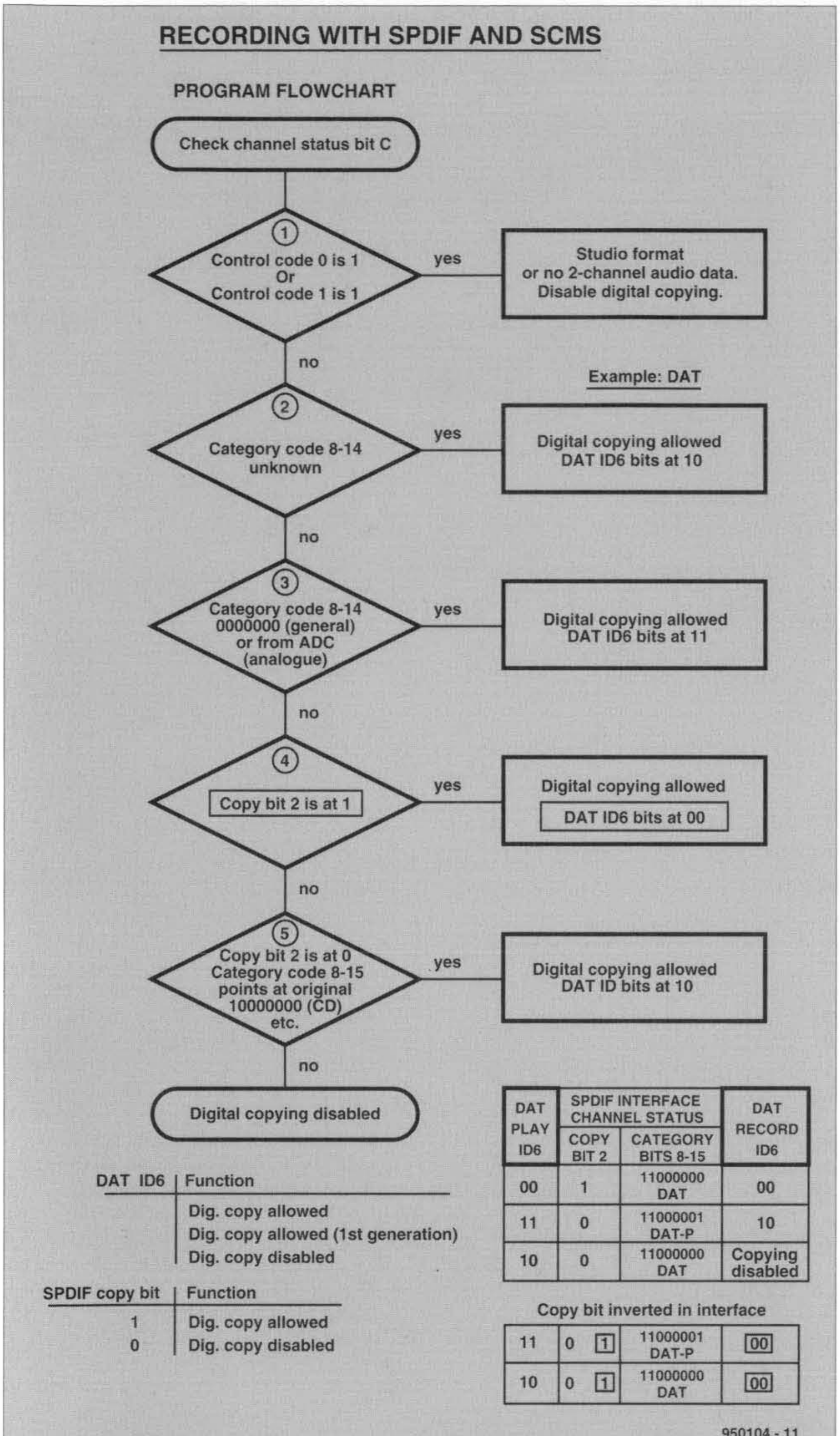


Fig. 1. Flow diagram of the evaluation process of the copybit in an S/PDIF signal.

of the relevant equipment are retained.

The unit can be used as a converter with either optical or coaxial inputs and outputs without any change in the input signal.

The left-hand and right-hand channels each build a subframe of 32 bits, which together form a frame of 64 bits with a sampling frequency of, say, 44.1 kHz. A block contains a total of 192 frames (or 384 subframes) as shown in **Fig. 2**. The data are transmitted in biphase mark code, in which a bit is split into two bit-cells. In case of a digital 0, both cells have the same level, that is, 00 or 11. In case of a logic 1, the levels of the cells are in-equal, that is, 01 or 10, which means that there is a level change at the centre of the bit. The longest a level can last is thus 1 bit—see **Fig. 3**.

This process also means that the clock is included in the transmitted information.

So as to identify the subframes and the start of the block, eight bit-cells have a bit sequence that does not occur in the biphase code—see **Fig. 4**. They are the block preamble *B*, which also identifies the left-hand channel in subframe 0, subframe preamble *M* (left-hand channel) and subframe preamble *W* (right-hand channel).

For the inversion of the SCMS, only bit 30, the channel status bit *C* of each subframe, is of importance. A complete channel status is repeated in each block of 384 subframes. The assignment of copy and category is the same in both channels.

The copybit is contained in subframes 4 and 5, and the category code in subframes 16–31.

Bits 30 and 31 in frame 15 have a special meaning. The so-called generation bit indicates whether the signal is an original or a copy. The assignment of a level for the original signal depends o the equipment. When the copybit is 0, bits C_{15} are sampled. An original signal permits one copy, and this must be an analogue copy. When the copybit is 1, no sampling takes place. To avoid any interference in the biphase code, two successive bits must be altered in the left-hand and right-hand channels respectively.

Reverting to the data contained in the user bit. only parity bit *P* needs to be considered as adjacent second bit. This thus determines the parity.

Conversion with PLD chip

The block diagram of the copybit inverter is shown in **Fig. 7**, and the circuit diagram in **Fig. 8**.

The digital a.f. signal – 0.5 V_{pp} into 75 Ω – is coupled capacitively to inverter IC_{1a}, which is arranged as an amplifier. The standard circuit is an inverter with feedback, but this has the disadvantage that the circuit tends to oscillate with open input. In the present circuit, the operating point is set permanently with P_1.

Inverter IC_{1a} is followed by a delay circuit with a delay time of 120 ns.

To ensure that both inputs (optical and coaxial) provide equal signal levels, the output of the opto-receiver, which is about 1.5 V_{pp}, is applied to the coaxial input via R_8. A change-over switch is not needed, since R_8 decouples both inputs adequately. In optical operation, the signal can thus be taken straight from the coaxial socket.

The direct and delayed signals are XOR-gated in IC_2 This makes the sig-

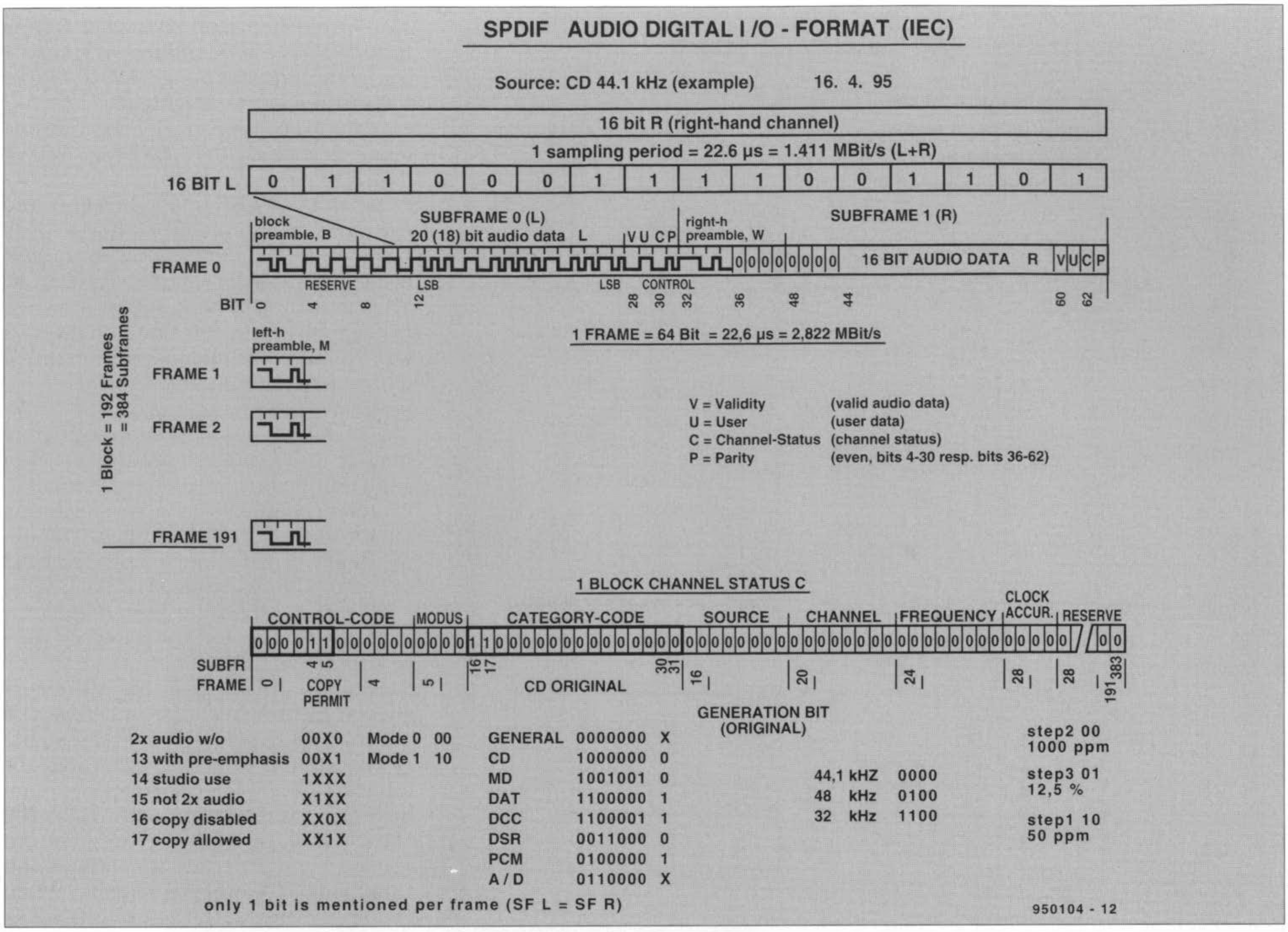


Fig. 2. Composition of a digital audio signal.

nal independent of the polarity at the input, since all subsequent steps are related to the XOR signal. The spacing of the positive edge in case of a logic 0 is 354 ns and in case of a logic 1, 177 ns—see **Fig. 5**.

Normally, the clock is retrieved by a phase-locked loop, PLL, which, as far as time and phase ratios are concerned, is not easily kept stable. Moreover, the voltage-controlled oscillator, VCO, remains operational in the absence of an input signal, which makes decoding of the block and subframe clocks more complicated.

The XOR signal starts non-retriggerable monostable IC_{3a}, which has a dwell time of about 240 ns, to retrieve the bit clock. In the range of the preambles, the start spacings are >350 ns. This is made use of by retriggerable monostable IC_{3b}, which has a mono time of around 420 ns, to generate the subframe clock. The X-coded XOR pulse occurs only with the block preamble at the first pulse of the subframe clock. This enables the block clock to be decoded.

The block clock is generated regularly when the circuit operates as specified, that is, when there is a digital input signal in S/PDIF format, and the dwell times of the monostables are in accord. The block clock is stretched to a constant-1 signal (NOINV) by IC_{1d} and IC_{1e}; its presence is indicated by D_{10}. If, for instance, the signal has an incorrect frequency, NOINV prevents it being modified and this is indicated by D_{10} lighting less brightly. The LED does not light at all when the input signal is not of the S/PDIF format.

To count the subframes, a 9-bit counter is timed by the subframe clock and reset by the block clock. The 5-bit counter for the subframe bits is in synchrony with the bit clock and is reset by the subframe clock.

Filtering the desired bits (bit 30 in subframes 4, 5, and 16–31) is effected by programmable IC_2. The INVERT pulse has the correct position when signal IN_1 is delayed by about 60 ns (IN_2). A logic 1 is indicated when the relevant LED is driven by the level detector signal output by IC_2. This signal is generated in a manner similar to that of the block clock. Each D-bistable associated with a given LED is reset by the block clock and set

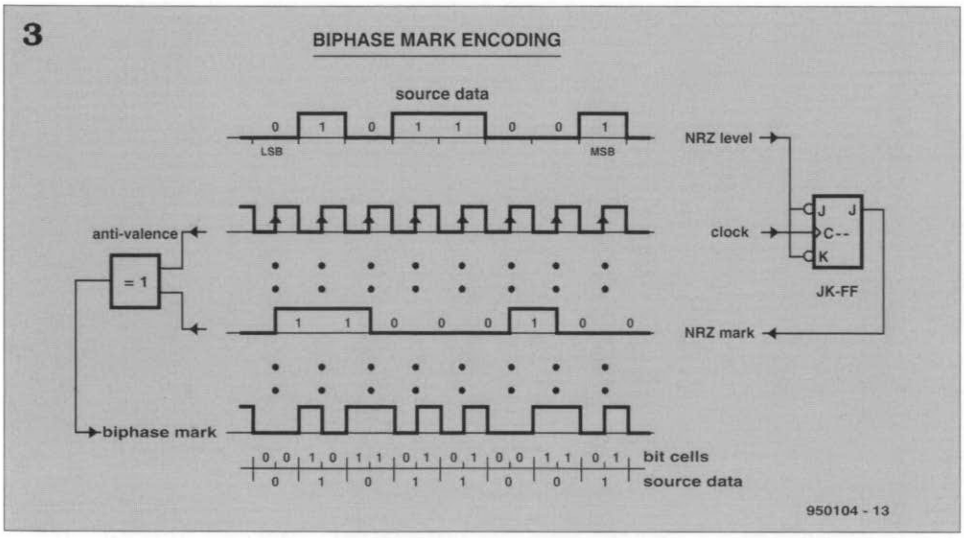
LED indications

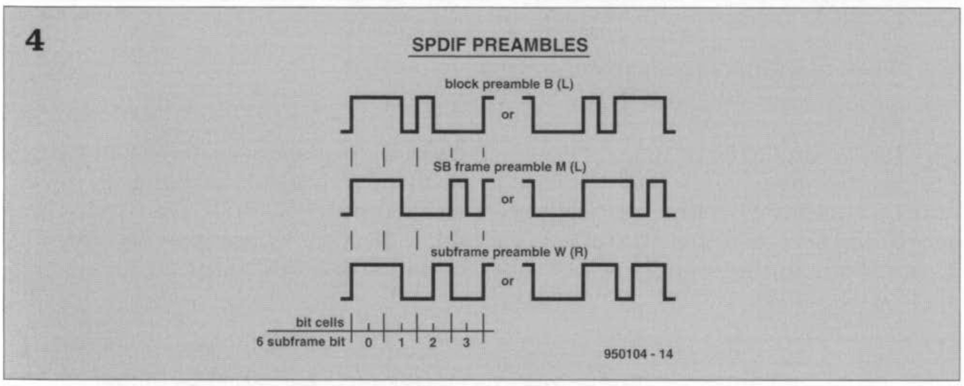
- Only D_9 lights in both switch positions: ready for use; no S/PDIF

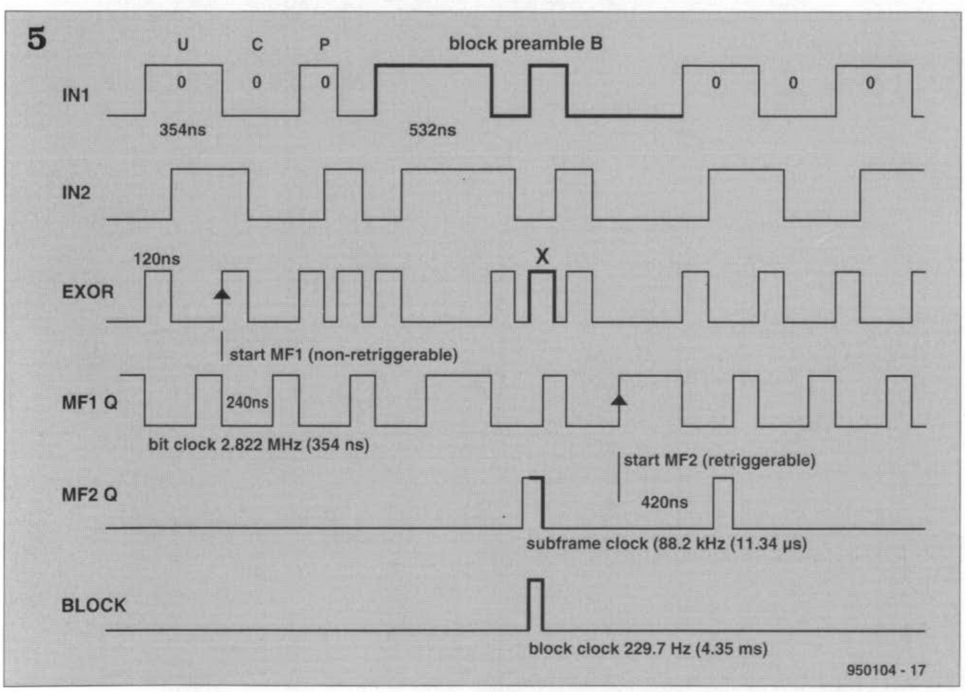
- LEDs flicker: unit is not operating correctly. It may be that both inputs are used simultaneously, or that the input signal is not of the correct format, or that the setup is incorrect, or that the optical input receives spurious signals.

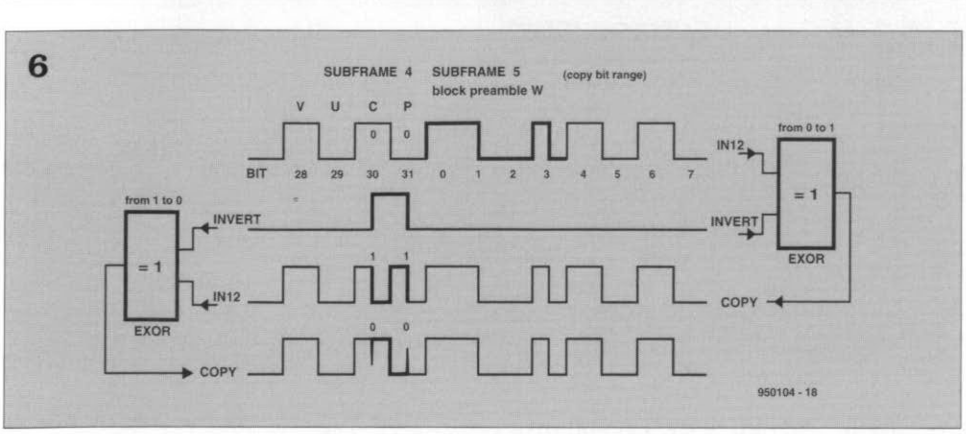
- D_9 and D_{10} do not light: unit functions as converter; S/PDIF signal is transferred unchanged.

- D_{10} lights brightly: the S/PDIF input signal, with copybit and category, is indicated The output signal is DAT when the input comes from a magnetic tape drive, and CD when comes from any other source. In both cases, copying is permitted.









with the 1-signal. The period to the next reset is long enough to enable the LED indicating the 1 in a stable way (without flickering).

Inversion of the bit is accomplished by an XOR gate and the 354 ns long INVERT pulse that is located half-way between the C-bit and P-bit—see **Fig. 6**. The change from 0 to 1 presents no difficulties, since the edges of the INVERT pulse in signal IN_{12} meet at the centre of the bit at equal levels. Short spurious pulses at the centre of the bit can, however, not be avoided entirely. This does not matter, however, since the biphase-modulated signal is always sampled at the centre of a bit-cell, that is, at 1/3 and 2/3 of the bit.

When bit C_8 and C_9 in the input signal are logic 1 (magnetic tape drive), they will not be affected. All other signal sources are assigned the code of a CD player.

Moreover, bits 0 and 1 of the channel status are held at logic 0. Although this is not really necessary in domestic equipment (since the bits then are always logic 0), it makes it possible for professional recordings or other recordings marked by these bits (which are inhibited) to be copied—but see warning at beginning of this article.

With switch S_1 open, the inverter accepts sampling frequencies of 44.1 kHz and 48 kHz, but with 32 kHz it must be closed to alter the time constants of the monostables. If this switch is in the wrong position, D_9 and dimly lit D_{10} indicate that the signal is unchanged: the unit functions as a converter. A no-signal condition is indicated by D_9 lighting.

It is highly improbable that only the generation bit, which does not count in the equipment coding, is encoded. Anyway, there is always D_{10} as a controlling element.

The output is buffered by inverter IC_{1f}. Resistors R_4 and R_5 lower the signal level to about 0.5 V_{pp} into 75 Ω. Capacitor C_1 blocks any direct voltage.

Timing the monostables

Construction of the inverter on the

Fig. 3. Biphase coding enables the simultaneous transmission of the audio signal and the clock.

Fig. 4. Various waveforms of a non-biphase coded preamble.

Fig. 5. Extraction of the bit-clock, subframe clock and block clock.

Fig. 6. Principle of bit inversion.

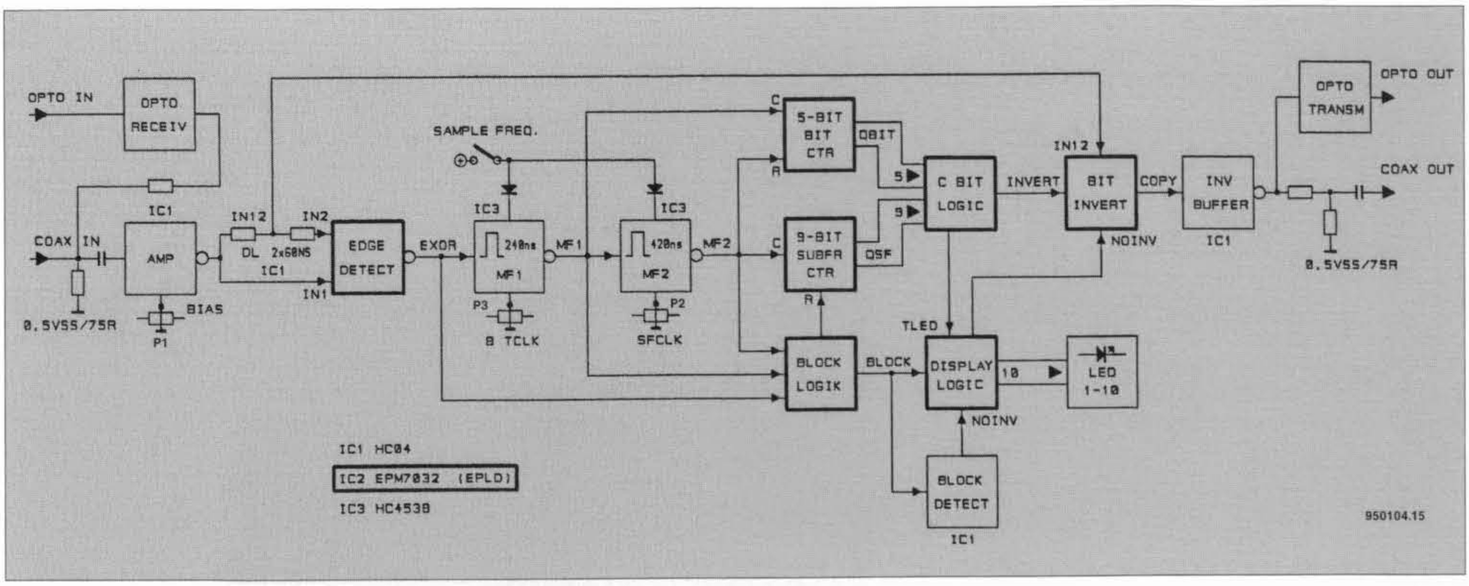


Fig. 7. Block diagram of the copybit inverter.

printed-circuit board in **Fig. 9** should not present any undue difficulties. All ICs, except IC_6, should be seated in sockets. Be careful with inserting IC_2 into its PLCC socket. Do not forget the wire bridge underneath IC_2.

After the board has been finished and thoroughly checked, set the presets to the centre of their travel.

Apply an audio signal, preferably from a CD player set to PAUSE (which ensures a very stable signal) to the coaxial input socket. Set switch S_1 to 44.1/48 kHz, whereupon D_3 (category code CD) should light. If an oscillo-

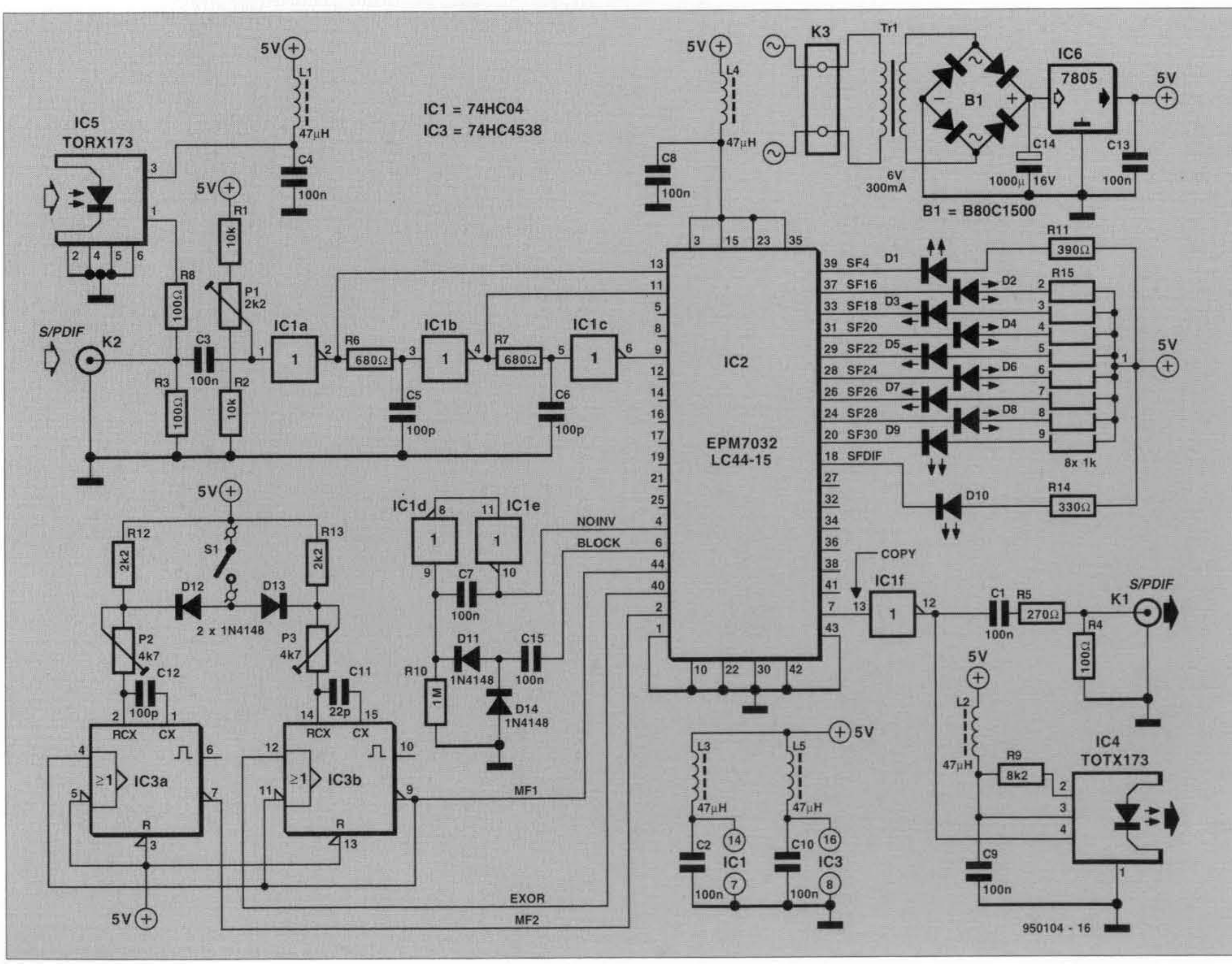


Fig. 8. Circuit diagram of the copybit inverter.

scope or logic analyser is not available, adjust presets P_1, P_2 and P_3 (in that order) on to the centre of the stable LED indication.

With S_1 in position 32 kHz, the signal source must be a DAT recorder, set to the long-play analogue recording mode, or a DSR tuner. Carefully readjust P_3 (which should not be much) and recheck the settings with a signal from a CD player. For most practical purposes, these settings are fine.

If more accurate settings of the presets are required, an oscilloscope is needed. Apply an a.f. signal at a level of 0.5 V_{pp} to the coaxial, not to the optical, input. Set the oscilloscope time base to 100 ns cm^{-1} and connect the instrument to pin 9 of IC_3. Adjust P_1 so that all edges cover one another as well as possible. This ensures that the operating point of the unit is centralized and that the delay of the rising edge of signal IN_2 is equal to that of the trailing edge.

With P_2, set the pulse width of the subframe clock at pin 7 of IC_3 to 100–150 ns. If there is an appreciable difference in dwell times between the standard and long-play settings, the value of R_{12} may be adapted accordingly.

If the oscilloscope has a second time base or x-multiplier ×10, the copybit (bit 30) corrected to logic 1 in subframe 4 or 5 can be timed in the output signal with P_3 [time base set to 10 (1) μs cm^{-1} and triggering to start the block at the leading edge of the cathode signal of a lighted LED (D_1–D_9)].

The high and low level portions of the C-bit set to logic 1 should be equal or very nearly so. If the P-bit is inverted from logic 0 to 1, it should be virtually undistorted.

If the bits away from the block start are to be checked, the LED voltage (trigger at trailing edge) associated with the P-bit can be used for marking them.

During the setting up, make sure that the LEDs light over a fairly wide range. Appreciable differences can be negated by adapting the value of R_{13}.

As a final check, record the output of the copybit inverter on a DAT or DCC recorder. Some DAT recorders show the ID6: this must be 00 both during recording and subsequent playback of the recording—see Fig. 1. Make sure that D_1 lights as an indication that the unit has correctly inverted and processed the input signal.

Parts list

Resistors:

R_1, R_2 = 10 kΩ
R_3, R_4, R_8 = 100 Ω
R_5 = 270 Ω
R_6, R_7 = 680 Ω

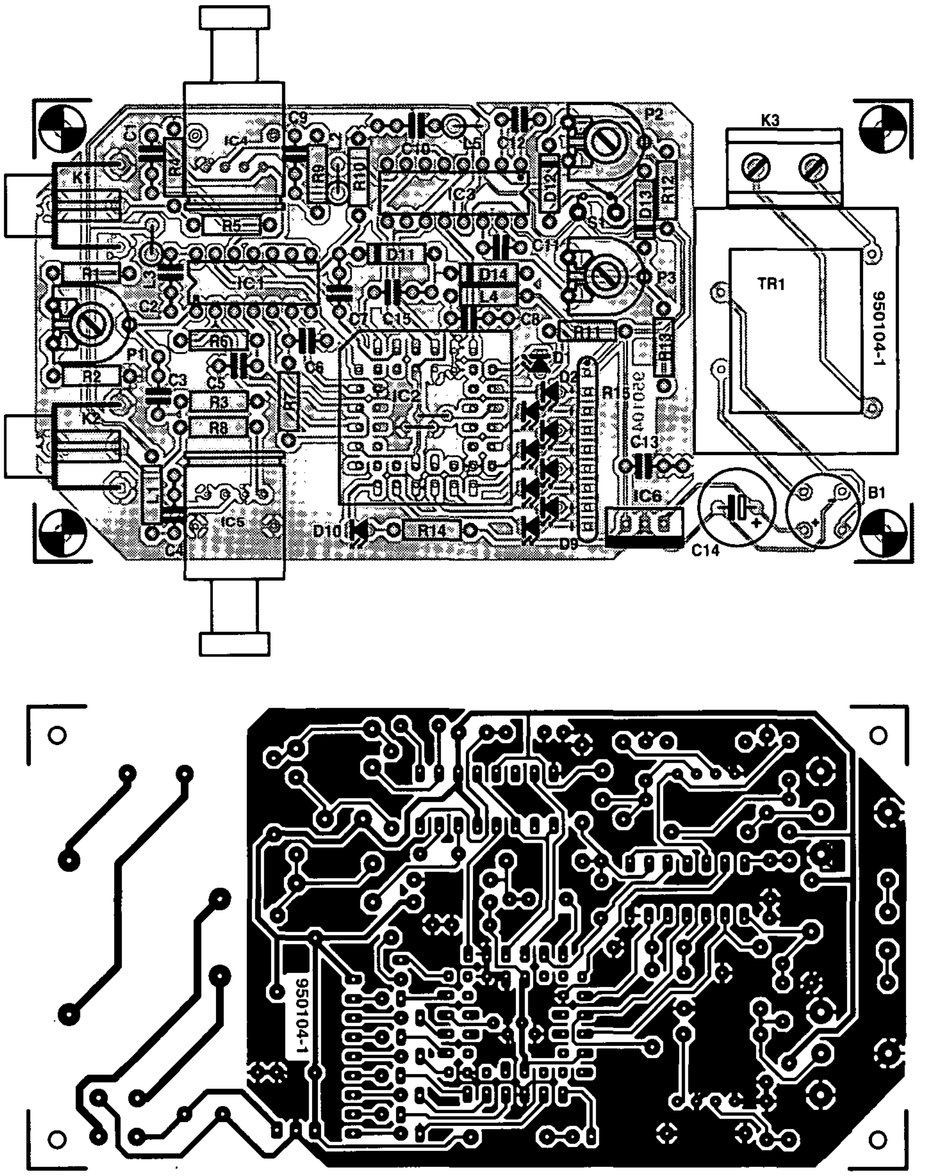


Fig. 9. Printed-circuit board for the copybit inverter (scale 1:1).

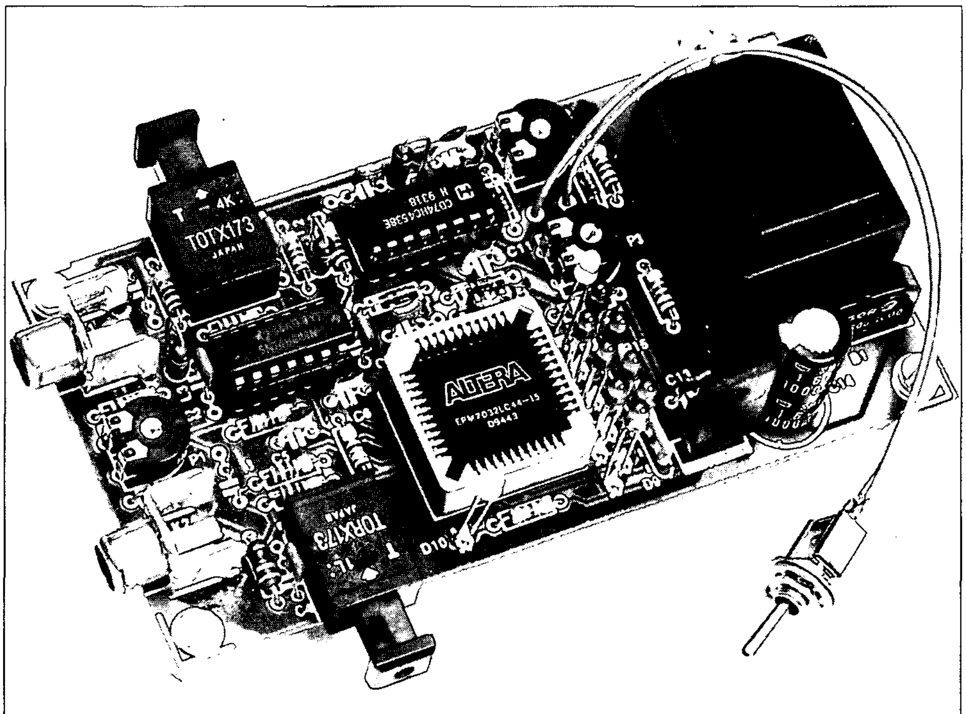


Fig. 10. Finished prototype board.

R_9 = 8.2 kΩ
R_{10} = 1 MΩ
R_{11} = 390 Ω
R_{12}, R_{13} = 2.2 kΩ
R_{14} = 330 Ω
R_{15} = resistor array, 8.1 kΩ
P_1 = preset, 2.2 kΩ
P_2, P_3 = preset, 4.7 kΩ

Capacitors:
C_1–C_4, C_7–C_{10}, C_{13}, C_{15} = 100 nF, ceramic
C_5, C_6, C_{12} = 100 pF
C_{11} = 22 pF
C_{14} = 1000 μF, 16 V, vertical

Semiconductors:
D_1, D_{10} = LED, low-current, 3 mm, green
D_2–D_9 = LED, low-current, 3 mm, red
D_{11}–D_{14} = 1N4148

Integrated circuits:
IC_1 = 74HC04
IC_2 = EPM7032LC44-15 (Altera), programmed with software 956513-1*
IC_3 = 74HC4538
IC_4 = TOTX173 (Toshiba)
IC_5 = TORX173 (Toshiba)
IC_6 = 7805

Miscellaneous:
K_1, K_2 = audio socket for board mounting
K_3 = 2-way spring-loaded terminals for board mounting, pitch 7.5 mm
S_1 = toggle switch with on contact
B_1 = B80C1500, round
Tr_1 = mains transformer, 6 V, 300 mA
44-pin PLCC socket for IC_2
Enclosure 120×40×70 mm
PCB Order no. 950104*

* Combination packet Order no. 950104C

Sources:
Sony SCMS Handbook DTC-55ES

Valvo TI871011

DIN EN 60 968

[950104]

Dark-room timer

(October 1996 - 960086)

The proposed stop scale for the timer (Figure 5) should be turned around because the delay time increases when the control is turned clockwise. Also, the value of C_1 is incorrectly given as 1 μF in the parts list, whereas the correct value is 1.8 μF as shown in the circuit diagram.

Matchbox BASIC computer as data logger

(September 1996 - 960065)

Owing to a text conversion error, all underscores in the names of variables have dropped out of the program listing shown in Figure 4. The correct variable names are LOG_MAX, START_LOG, COM_CHR, LOG_RAM, LOG_DATA, READ_MAXIM and DUMP_PTR.

Also, The compiler is unable to process the line

WHILE DUMP_PTRG MAX DO

which is best replaced by

WHILE DUMP_PTR GMAX DO

Motor controller for R/C models

(February 1997 - 960095)

The text incorrectly states that D_1 and D_2 are not required for unidirectional mode. This should be D_1 and T_1. The penultimate paragraph on page 17 and the first complete paragraph in the right-hand column on page 18 should be amended accordingly.

68HC11 Emulator

(February 1997 - 970008)

The correct name of the Talker for use with a 5 MHz crystal is TKAXTS_B00 (inset *Talkers for use with the emulator*, page 25).

Contrary to what is stated under the *Applications examples, FAQs* heading, the Hi-Tech compiler is not in the M11DISK\UTILI\ directory. Users having access to version 7 of this compiler may, however, use SYMWICE.EXE to build a small high-level debugger. Likewise, the SYMWICE.C file may help users of other compilers or earlier versions of the Hi-Tech compiler. SYMWICE.EXE also works for the WICE emulator.

The text *In the latter case, ports B and C ...* (page 23, third line from the bottom) should be corrected to read: *In both cases, ports B and C ....*

The TL7705 will switch at a low-supply voltage of 4.5 V, not 3.6 V as stated at the top of the right-hand column on page 24. The reference voltage is calculated from:

$V_{ref}\,(R_2+R_1)/R_1 =$
$2.53\times17.8/10 = 4.5$ V.

Simple inductance meter

(February 1997 - 970009)

In the circuit diagram on page 32, diodes D_2 through D_9 should be connected to K_1 pins 2 through 9, not pins 1 through 8. The layout of the printed circuit board is not affected.

Copybit inverter

(January 1996 - 950104)

The input stage around gate IC_{1a} may start to oscillate when the optimum sensitivity is reached by adjusting preset P_1. This spurious oscillation may upset the normal operation of the circuit. The problem is remedied by fitting a 47μF/25V electrolytic capacitor in parallel with C_2 at the track side of the board. The relevant connections should be kept as short as possible.

The settings of the three presets on the board are determined to a large extent by the quality of the applied S/PDIF signal. The settings are, therefore, dependent on the digital signal source.

lcr meter - part 1

(April 1997 - 970028/1)

Some unfortunate errors have crept into some text and the box on p. 32.

In the 8th line, centre column, $10^2/10^5$ should read $10^2//10^5$.

Z_{out} in the 9th and 12th lines should read Z_{dot} (where dot is the device on test).

In the formulas in the box, $2ni$ should read $2\pi i$ in all five cases. The first formula should start: $U_1\cos\varphi_1 =$, and the second formula: $U_1\sin\varphi_1$.

SYNCHRONOUS OSCILLATORS

When a digital-to-analogue converter (DAC) is used in conjunction with a CD player, their clocks must be in synchrony to make sure that the DAC can process the data error-free. In practice, this means that the clock of the CD player has to be applied to the DAC.

If the DAC is built into the CD player, the CD player clock can be applied as shown in the upper diagram. The clock signal is available at TTL level at the output of IC_{1b}. The DAC clock, IC_{2a}, is synchronized with IC_{1a} via P_1 and C_6. In practice, P_1 is set just past the point where synchrony commences: this ensures that oscillator IC_2 continues to work when IC_{1a} is disabled for whatever reason.

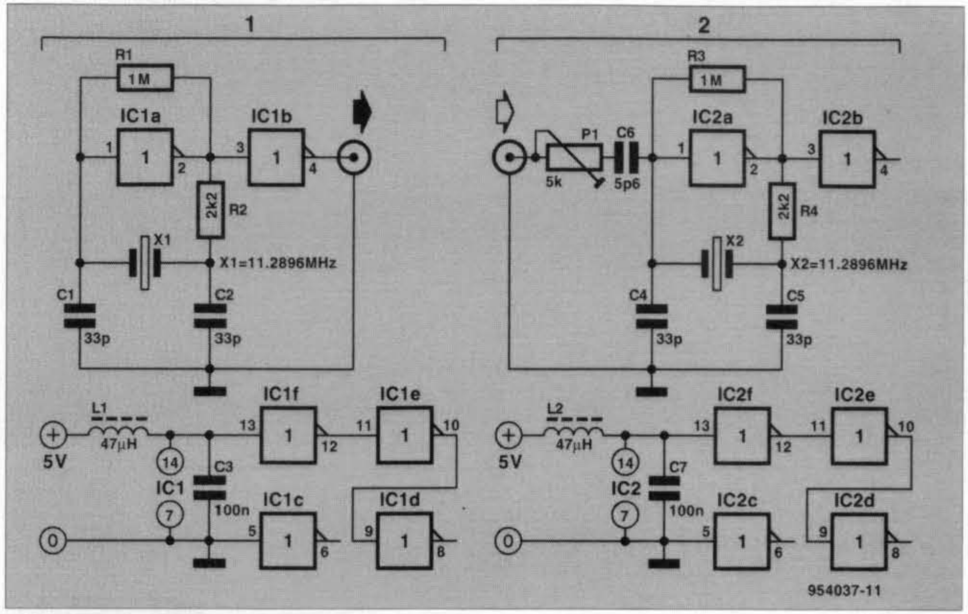
An important advantage of the design is that the circuit does not influence the operation of the electronics in the CD player (which thus retains its original functionality).

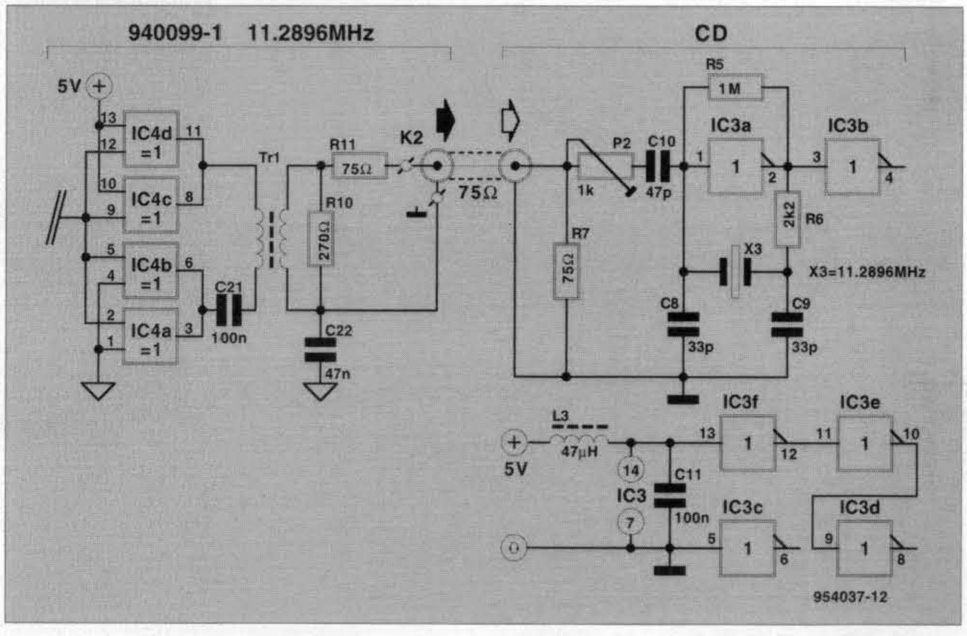
If the DAC is used as a stand-alone unit, a transmission line for the data and clock signals is required. As usual, this is a 75 Ω coaxial cable. The lower diagram shows how this setup can be arranged.

The chosen signal level of 1.5 V_{pp} is more than sufficient to ensure synchrony. The values of coupling components P_2 and C_{10} are, however, different from those of P_1 and C_6 in the upper diagram.

A drawback of this setup is that the oscillator no longer starts spontaneously owing to the increased damping. Fortunately, this can be remedied readily. Resistor R_6 limits the energy transferred from the buffer amplifier to the crystal. If the value of this resistor is greatly reduced, even down to 0 (wire bridge), it will be found that the oscillator starts spontaneously again. Note that in some CD players R_6 is replaced by a wire bridge.

Another remedy is reducing the turns ratio of the transformer, which increases the level of the clock signal.





If this is done, the value of P_2 can be increased an that of C_{10} reduced. The load on the oscillator is then smaller, so that it starts spontaneously.

The oscillator circuit draws a current of about 10 mA.

Design by T. Giesberts
[954037]

SECAM-TO-PAL CONVERTER

The circuit described in this article is, in principle, an add-on for the popular Picture-in-Picture (PIP) Processor featured in the October and November 1995 issues of this magazine. Because the PIP processor has only a PAL decoder, it is unable to display a colour inset picture in countries where the SECAM TV system is used. That problem may be overcome by inserting the present converter between the inset source and the PIP processor. The circuit offers more goodies, however, particularly for owners of satellite TV receiver systems.

Design by T. Giesberts

WHILE this circuit was being developed, it became clear that it could have more functions than just converting SECAM to PAL. The PAL encoder used here is capable of modulating colour difference signals as well as RGB signals, and in addition offers a 'fast switching' mode between these two options. Obviously, this presents the possibility to convert RGB signals into PAL format. But that's not all! The present converter also doubles as an interface between the PIP unit and older TV sets. By 'older' we mean tellies which do have a SCART connector at the back, but lack the required 'fast blanking' and 'RGB' inputs on this connector. In that case, the present converter is inserted between the PIP unit and the TV set, so that the PIP unit supplies the input signals for the converter. Obviously, the synchronization of the inset picture requires the CVBS signal of the TV to be fed back to the PIP unit. This option has been taken into account in the practical realization of the converter.

A few blocks only

Although integrated circuits have been used wherever possible in the practical circuit, the actual circuit diagram is quite complex. So, we give you a block diagram first to make sure you can understand how the circuit works. The block diagram in **Fig. 1** gives a good indication of the structure of the converter.

The heart of the converter is formed by the blocks marked 'SECAM decoder' and 'PAL decoder'. The remainder of the circuitry shown is, well, necessary to make it all work! The SECAM decoder is a type TDA8395. This is a fully integrated decoder, complete with RF and LF filters, a PLL demodulator and a line identifier. The IC functions with a minimum number of external components and requires no adjustment. As a baseband delay line, the manufacturer recommends the TDA4661 (IC_2) — yes, the one used in the PIP processor also. The same goes for the practical realization of the block marked 'sync. circuit', because it is based on the TDA2579B (IC_5).

The most important function in the circuit, the encoding of the PAL signal, is performed by a TDA8501. This is an almost entirely integrated encoder IC specially designed for all applications requiring the conversion of R, G and B (or Y, U and V) into PAL or NTSC values. The external parts required to make the TDA8501 work are limited to two delay lines and a reference oscillator.

For the following description of the operation of the circuit we recommend keeping one eye on the block diagram because the signal paths in it are probably easier to trace than those in the actual circuit diagram. The latter is shown in **Fig. 2**, and is drawn such that the position of the elementary parts is about the same as those in the block diagram.

SECAM dissected

The SECAM/CVBS signal which arrives on socket K_1 is applied to pin 16 of SECAM decoder IC_1 via jumper JP_4. The outputs of the decoder (pins 9 and 10) supply the modulated colour difference signals. Since only one colour difference signal is transmitted per line in the SECAM system (the two colour difference signals are actually transmitted alternately), a delay line is necessary to join the two signals again for each TV picture line. That is, admittedly, not ideal, but it is inherent to the SECAM system (see the inset box). The result is that one of the colour difference signals is never actually up to date. Obviously, that creates errors in determining mixed colours. By contrast, the current colour differences do get transmitted in the PAL system, resulting in much better picture quality.

For proper operation of the SECAM decoder it was found necessary to put the levels of the horizontal and vertical blanking at about half-way the sand-

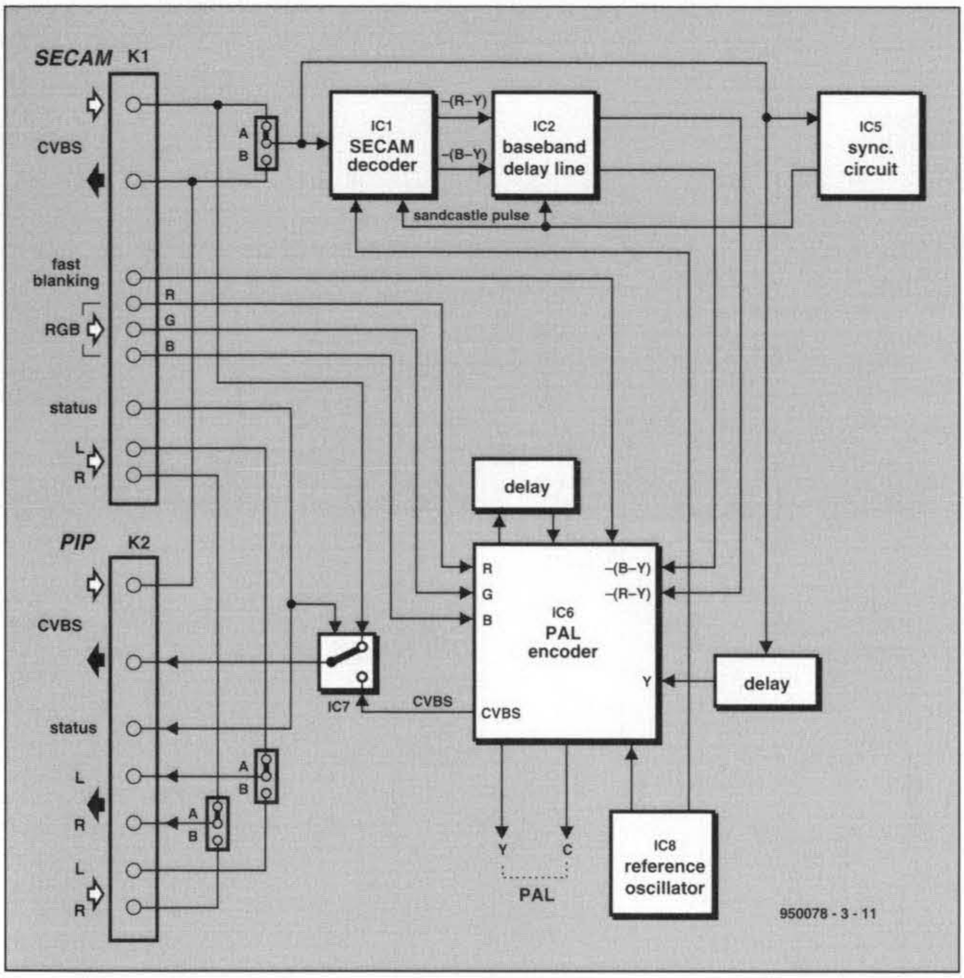


Fig. 1. The architecture of the converter is obviously based on the blocks marked 'SECAM decoder' and 'PAL encoder'. The nice thing about the circuit is that it will do more than 'just' converting SECAM into PAL.

castle pulse. Only then is it possible for the decoder to suppress all kinds of interference resulting from the demodulation process. Components R_6 and D_1 at pin 15 of the relevant IC limit the size of the sandcastle pulse to a level which is acceptable for IC_1.

The output signals from IC_1 are fed to the baseband delay line simulator, IC_2. This IC adds the information pertaining to the received TV line to that of the previous line, which has been delayed exactly 64 µs. Hence this IC is suitable for PAL as well as SECAM, although a gain of 0 dB is stated for the SECAM standard, and 6 dB for the PAL standard. That is because both colour difference signals are present in a PAL signal, resulting in a doubled output level after addition. With IC_2, too, the level of the sandcastle pulse is limited, in this case, with the aid of R_{10}/R_{11}.

The sandcastle pulse required for IC_1 and IC_2 is supplied by IC_5. For proper operation of the SECAM decoder, the sandcastle pulse should contain vertical as well as horizontal blanking information. Consequently, an IC is used which is specially designed for this purpose, the TDA2579B. Again, this IC was also used in the PIP processor. Here, however, a practical problem has to be overcome: the horizontal blanking calls for a flyback pulse. In a TV set, the flyback pulse is supplied by the deflection system, and that is an element which is not present in the decoder. To solve the problem, the horizontal output of IC_5 (pin 11) is connected directly to the flyback input (pin 12). An RC network, R_{73}-R_{41}-C_{78}, determines the exact length of the horizontal blanking in the sandcastle pulse, and R_{74} in particular determines the proper timing of the horizontal blanking.

Level shifting

In practice, the voltage levels of video signals are often on the low side. Add to that the fact that the converter's output buffer introduces some loss, and you will see the need to 'boost' the input voltages to the PAL encoder at least a little. The gain is accomplished by inserting two small amplifiers, IC_{3a} and IC_{3b}, between delay line IC_2 and the PAL encoder. The same function is performed by IC_4 for the Y signal. The bandwidth of the opamps used here, the AD847 and its 'dual' counterpart the AD827, ensure that there is no corruption whatsoever of the signals. Incidentally, IC_4 has to supply 6 dB of additional gain to compensate the attenuation of the delay line. Because the exact gain may vary a little, it is adjustable (within a small range) with preset P_2. The 4.4-MHz trap at the input of IC_4, R_{20}-C_{17}-L_1, already suppresses a large part of the colour information contained in the SECAM signal, before this is applied to the PAL decoder as a Y signal. The function of delay line DL_1 is to compensate the propagation delays of the colour difference signals incurred in IC_1 and IC_2. A type DL330 delay line is used because a delay of 330 µs was found to be the optimum value. However, when we started to use standard RGB signals, it was found that the CVBS signal supplied by IC_6 was only 60% of its nominal value. If problems occur because of this signal reduction, the solution is to increase the value of R_3, R_4 and R_5 to 120 Ω.

Final station: PAL

Although the TDA8501 PAL encoder used here can be used, in principle, as an NTSC decoder, this option is not used in the basic version of our converter. A fixed 'PAL' setting is created by voltage divider R_{46}-R_{47}. The most important reason to skip the NTSC option is that the colour information is modulated on a 4.43 MHz carrier in the PAL system, and that the SECAM decoder uses that very same frequency as a reference. That allows double use of a single oscillator. For NTSC television, a 3.579-MHz crystal would be required, which, in turn, would call for an extra oscillator.

Speaking of oscillators, the one built around IC_{8a} supplies the reference signal for decoder IC_1 (via IC_{8b}) as well as the carrier for IC_6 (via IC_{8c}). Although the oscillator has a simple layout, it is important to observe the crystal's exact frequency as well as its C_{LOAD} value of 20 pF. Jumper JP_3 allows an external carrier signal to be used for IC_6. Such a signal may be connected via K_8, and the option is primarily intended for a complex circuit which locks the line frequency to the carrier. In that case, the carrier frequency should be 4.433361875 MHz **exactly**. The filtered video signal is available at connector K_7 to enable an external oscillator to be synchronized to the video signal.

Returning to the PAL decoder, it is seen that the 'multiplex switch control input' (pin 2) is connected to the fast blanking terminal on K_1 via jumper JP_1. Consequently, switching transistor T_2 provides a simple way of making the converter process RGB signals only. All you have to do is interconnect the two PCB terminals marked 'RGB'.

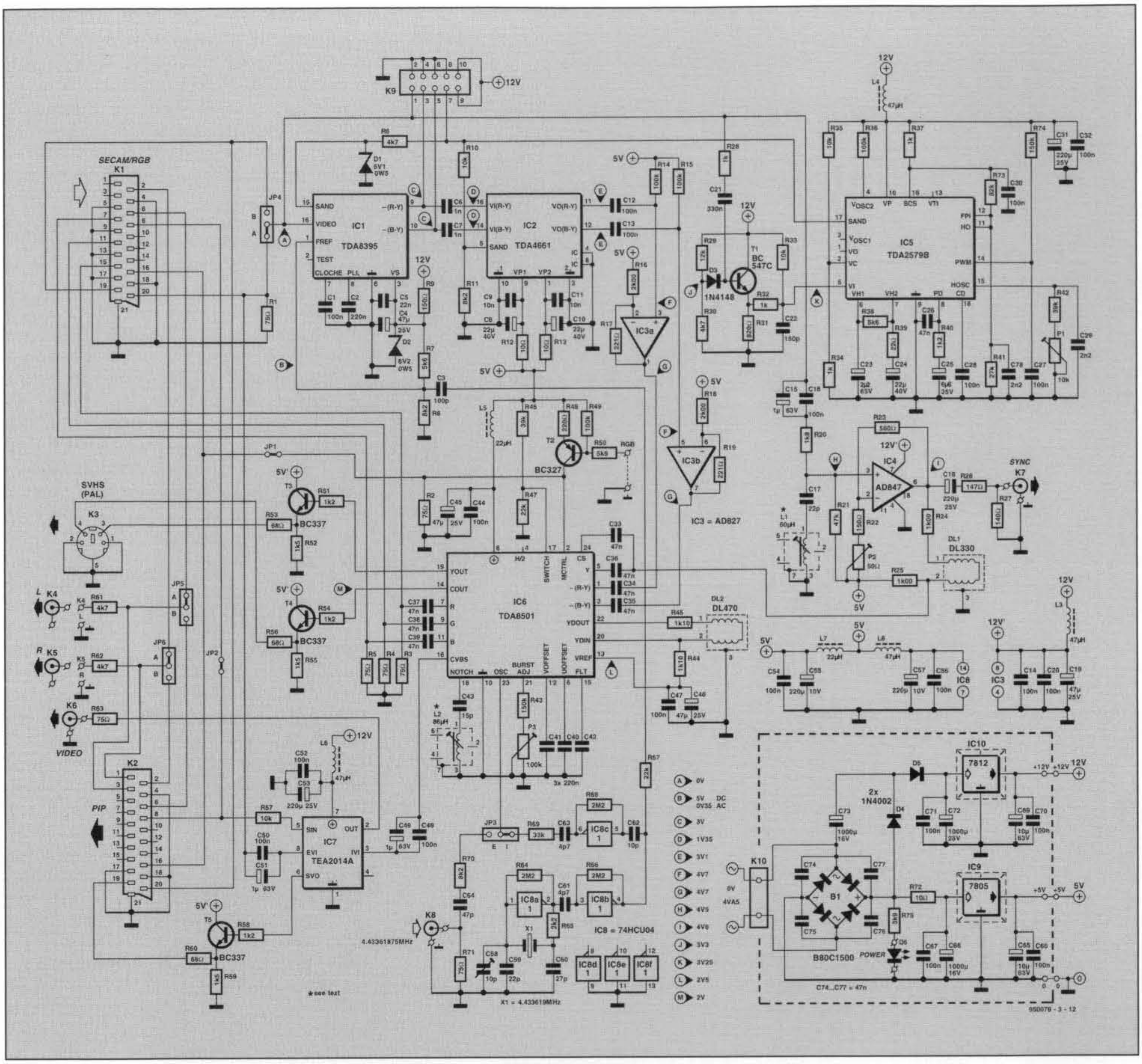


Fig. 2. This is the complete circuit diagram, including the power supply and all connections. Connector K9 has been added to enable the converter to be extended with an extra PAL decoder.

Pin 16 of IC_6 supplies the encoded PAL/CVBS signal. In addition to this, the TDA8501 also provides separate Y and C outputs. These are bonded out via buffers T_3 and T_4 and a mini-DIN socket. This S-VHS socket should, however, be considered as a kind of 'bonus' for test purposes etc., because the quality of the output signal is rather poor for lack of proper filtering and clipping. Moreover, the signal contains a measurable residue of the SECAM colour information. By contrast, the CVBS signal is pretty clean, mainly because of a notch filter, L_2-C_{43}, which affords excellent suppression of the SECAM carriers.

IC_7 is described by the manufacturer as a 'video switch'. Here, it actually functions as a combined video switch/buffer/amplifier. The IC has two outputs: one 'ordinary' (pin 2), and one switched video output (pin 6). The former supplies a buffered copy of the PAL/CVBS signal applied to pin 3; this output signal is fed out via K_6, for which a cinch or BNC socket may be used. The signal at the other output of IC_7 (pin 6) depends on the switching level applied to pin 5. When a low level is applied, pin 6 is connected through to the PAL/CVBS signal at pin 3. A high level causes the video (or CVBS) signal arriving via K_1 to be switched through (amplified) from pin 8 to pin 6. This is done to enable the incoming video signal from a VCR in 'play' mode to be fed directly to K_2. In case a SECAM signal arrives, that can be displayed in colour on the TV set, via the PIP processor.

Different modes

After the conversion from SECAM to PAL (*mode 1*), the translation from RGB into PAL (*mode 2*) is probably the most frequently used feature of the converter. In support of this second mode, jumper JP_1 allows the fast blanking signal from K_1 to be interrupted, and to set the PAL encoder permanently to RGB via the 'multiplex switch control input' (pin 2). Obviously, the RGB source connected to K_1 should then supply the sync pulses (via pin 20). Both *mode 1* and *mode 2* require jumpers JP_4, JP_5 and JP_6 to be set to position 'A'.

As already mentioned, *mode 3* enables the PIP unit to be used in combination with 'older' TV sets without

RGB and fast blanking input lines on the SCART socket. This is accomplished by setting jumpers JP_4, JP_5 and JP_6 to position 'B'. Evidently, the TV set should receive back its own sound, and that is why the audio input signals are connected directly to the output audio contacts of K_2. By the way, the extra (cinch) audio sockets, K_4 and K_5, are always connected to the audio output signals of K_2.

A few more remarks about *mode 3*. In this application (for PAL), the PIP processor supplies the input signals for the converter. As already mentioned, the synchronization of the inset picture requires the CVBS signal to be fed back from the TV set to the PIP processor. Hence, the circuit diagram shows pin 20 of K_2 as connected to pin 19 of K_1. But that is not all. Strictly speaking, this signal should be modulated again so that the inset picture and the TV picture can be joined via the fast blanking feature of the PAL encoder. If the main picture is to be shown in colour, then an external PAL decoder is required, which may be hooked up to the converter via connector K_9. All signals needed for that purpose are available on K_9, including the 12-V supply voltage.

Finally, it should be mentioned that a fourth mode is feasible. Those of you who use a PAL TV set to watch SECAM satellite TV stations not only have the possibility to convert a SECAM signal into PAL and use it as the parent ('main') picture (JP_4 in position 'A'), but in addition may feed the TV's own PAL signal back to the TV, through the PIP unit (as an RGB signal), and employ it as an inset picture. Both the parent and the inset picture then appear in colour! As regards sound, a choice is available between 'parent picture' sound and 'inset picture' sound. This selection is made with the aid of JP_5 and JP_6. The only condition for being able to use all these features is that the TV set must be able to fully process the PAL signals that arrive via its SCART socket (in many cases, that can only be achieved via the antenna input).

Construction and power supply

The double-sided printed circuit board for the project is shown in **Fig. 3**. This board is available through the Readers Services (see page 70). Construction is straightforward, and mostly a matter of locating the component on the component overlay, soldering and cutting wires. All essential connectors (in most cases, only K_1 and K_2 will be used) may be fitted straight on to the board. Only K_6, K_7 and K_8 are connected externally with short wires to the respective solder pins. For the audio outputs belonging with the S-VHS option, K_4 and K_5, both solder pins and cinch sockets are available on the board. The pins and the sockets are not interconnected, so may have to establish the links yourself with the aid of two short lengths of screened cable.

Among the passive parts are eight inductors. Six of these, L_3 through L_8, are ready-made miniature chokes. L_1 and L_2 however are home-made, adjustable, inductors, built from type 7F1S assemblies from Neosid. Making these inductors is not difficult because there are no taps or secondary windings. L_1 should have a value of about 60 μH, and L_2, 86 μH. These values are achieved by winding 70.5 and 84.5 turns of 0.1-mm dia. enamelled copper wire on the formers, respectively. Be sure to solder the wire ends to the right base pins, if necessary look

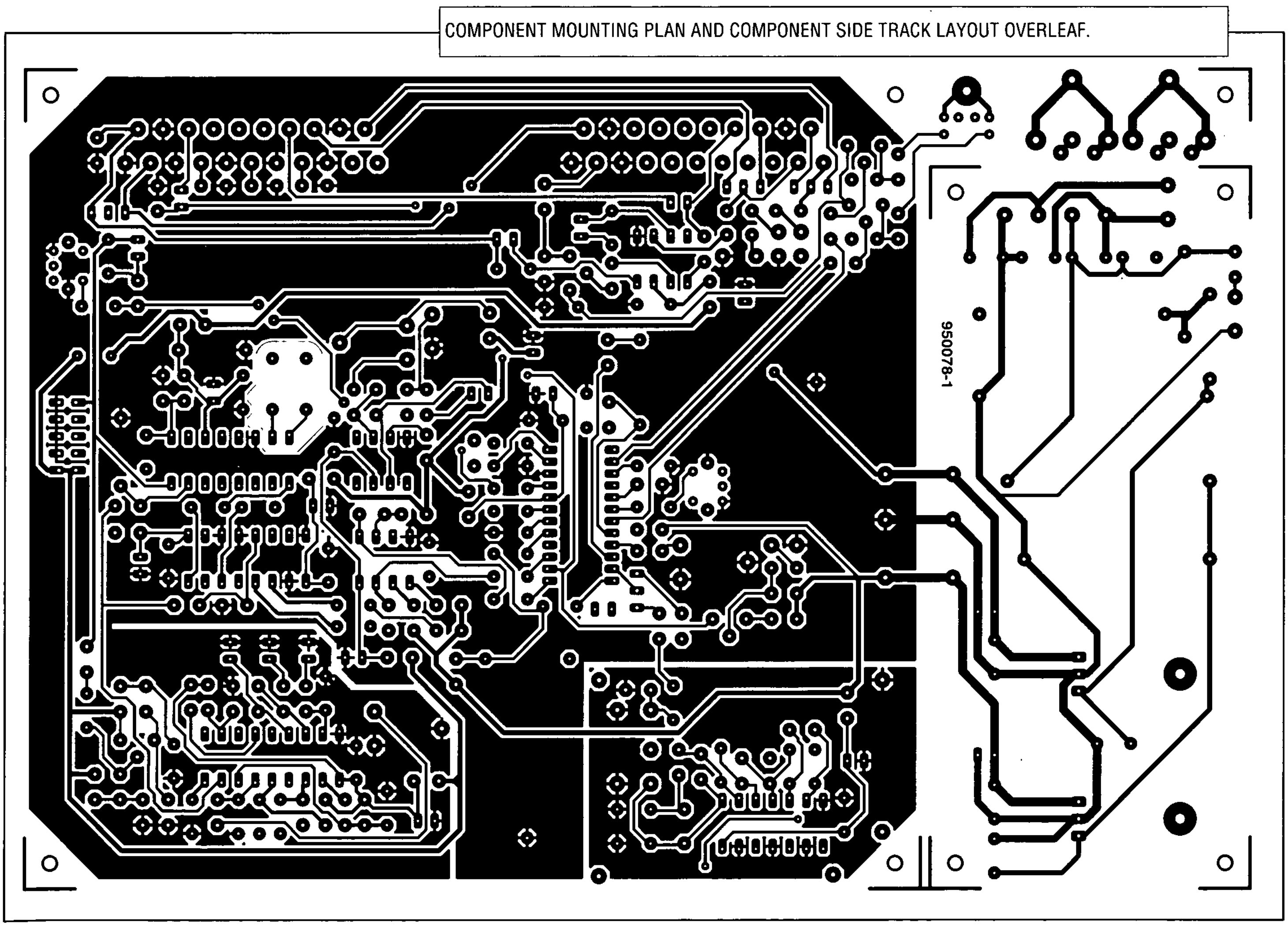
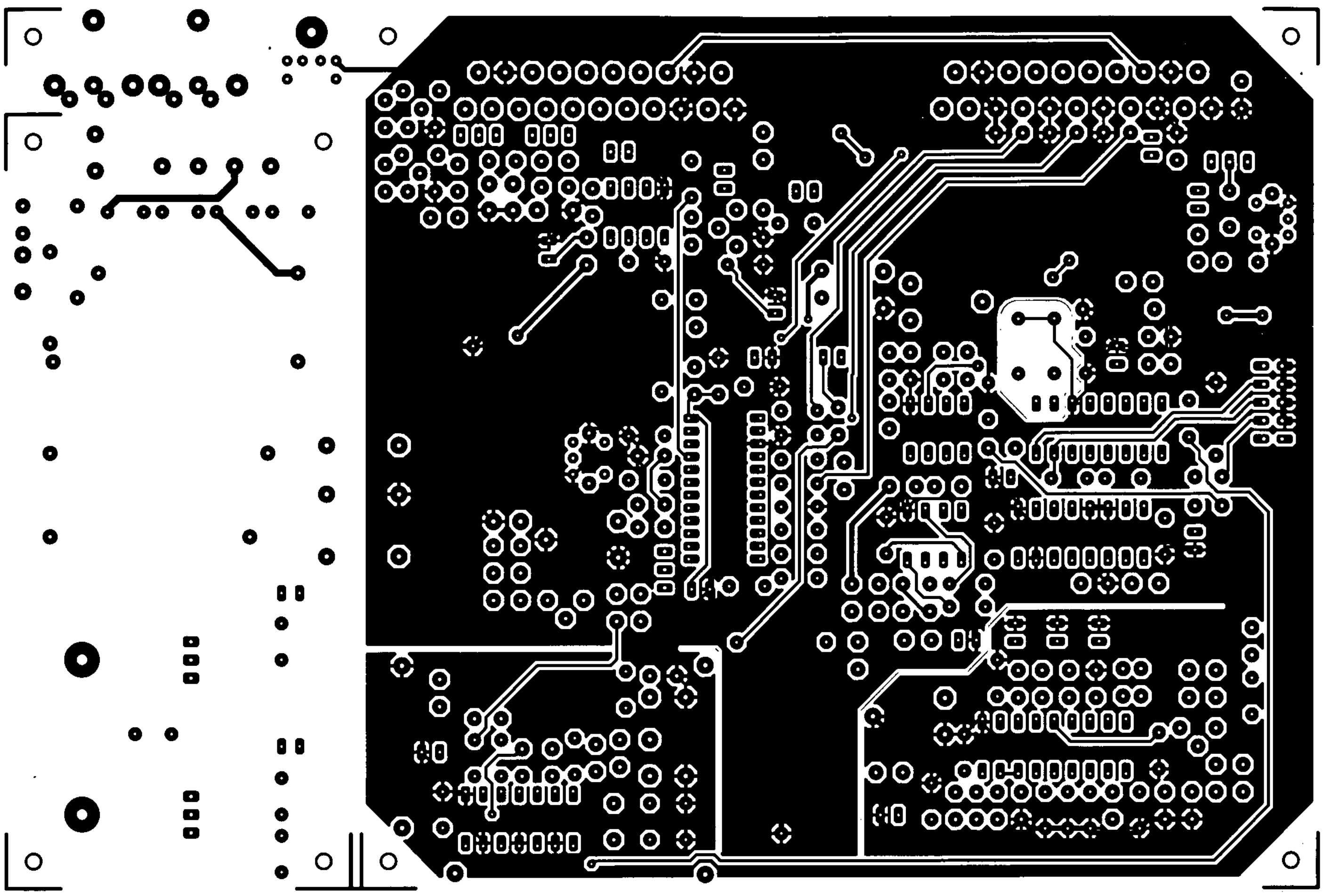
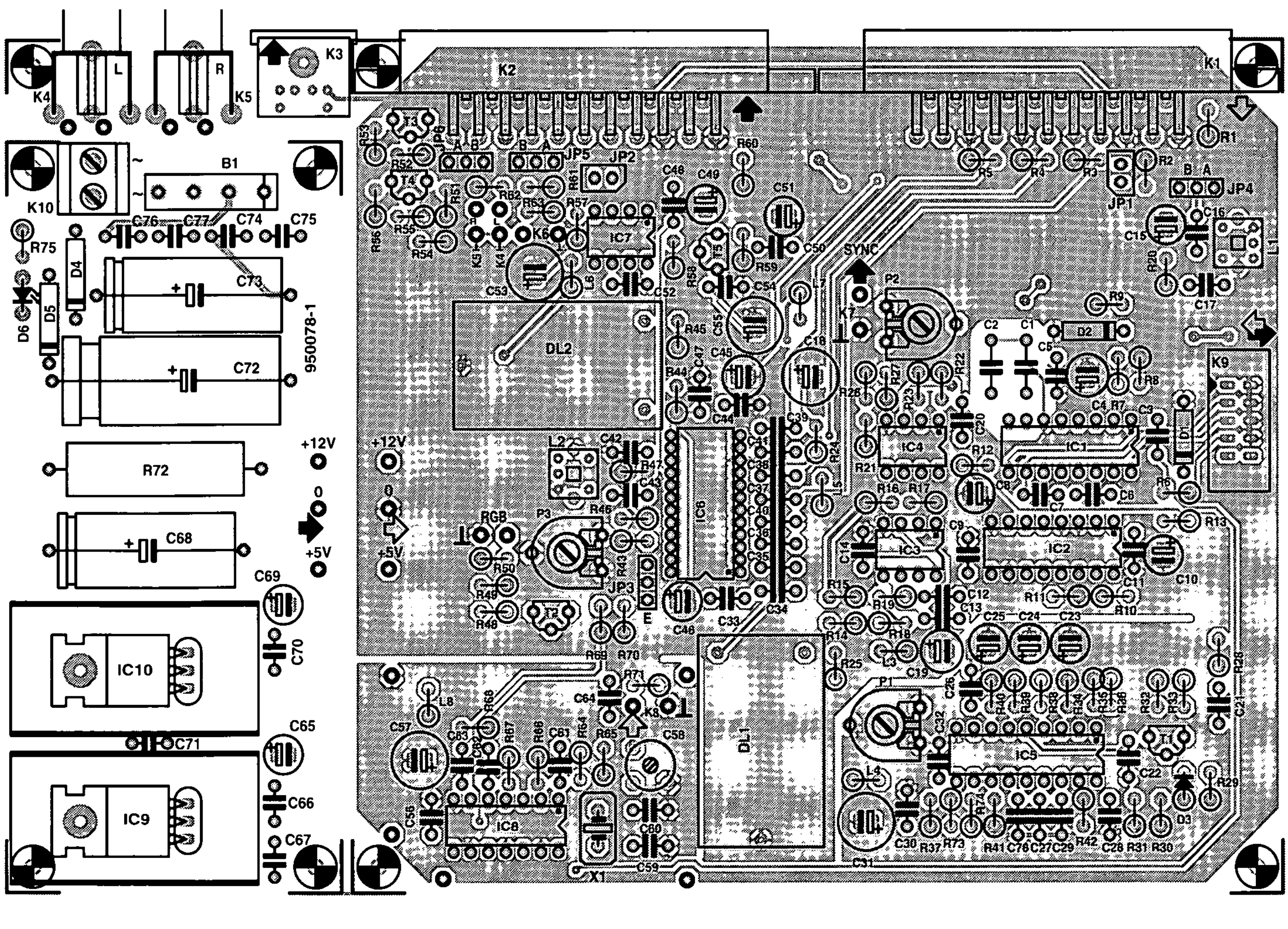


Fig. 3. The printed circuit board has the same size as that of the PIP processor, and offers more than enough room for all components. If desired, the power supply section, IC9, IC10, etc., may be cut off (board available ready made through he Readers Services, see page 70).





K1
K2
K3
K4
K5
K6
K7
K8
K9
K10
L
R
B1
950078-1
+12V
0
+5V
IC1
IC2
IC3
IC4
IC5
IC6
IC7
IC8
IC9
IC10
DL1
DL2
P1
P2
P3
SYNC
RGB
X1
JP1
JP2
JP3
JP4
JP5
C68
C72
C73
R72

COMPONENTS LIST

Resistors:
R1-R5,R63,R71 = 75Ω
R6,R30,R61,R62 = 4kΩ7
R7,R38,R50 = 5kΩ6
R8,R11,R70 = 8kΩ2
R9,R22 = 150Ω
R10,R33,R35,R57 = 10kΩ
R12,R13 = 10Ω
R14,R15,R36,R49 = 100kΩ
R16,R18 = 2kΩ00 1%
R17,R19 = 221Ω 1%
R20 = 1kΩ8
R21 = 47kΩ
R23 = 560Ω
R24,R25 = 1kΩ00 1%
R26 = 147Ω 1%
R27 = 140Ω 1%
R28,R32,R34,R37 = 1kΩ
R29 = 12kΩ
R31 = 820Ω
R39 = 22Ω
R40,R51,R54,R58 = 1kΩ2
R41 = 27kΩ
R42,R46 = 39kΩ
R43,R74 = 150kΩ
R44,R45 = 1kΩ10 1%
R47,R67 = 22kΩ
R48 = 220Ω
R52,R55,R59 = 1kΩ5
R53,R56,R60 = 68Ω
R64,R66,R68 = 2MΩ2
R65 = 2kΩ2
R69 = 33kΩ
R72 = 10Ω 5W
R73 = 82kΩ
R75 = 3kΩ9
P1 = 10kΩ preset
P2 = 50Ω preset
P3 = 100kΩ preset

Capacitors:
C1 = 100nF, raster 7.5 mm
C2 = 220nF, raster 7.5 mm
C3 = 100pF
C4,C19,C45,C46 = 47μF 25V radial
C5 = 22nF ceramic
C6,C7 = 1nF ceramic
C8,C10,C24 = 22μF 40V radial
C9,C11 = 10nF ceramic
C12,C13,C14,C16,C20,C32,C44,C47,
C48,C50,C52,C54,C56,C66,C67,C70,
C71 = 100nF ceramic
C15,C49,C51 = 1μF 63V radial
C17,C59 = 22pF
C18,C31,C53 = 220μF 25V radial
C21 = 330nF, 5mm
C22 = 150pF
C23 = 2μF2 63V radial
C25 = 6μF8 35V tantalum
C26 = 47nF, 5mm
C27,C28,C30 = 100nF, 5mm
C29,C78 = 2nF2, 5mm
C33-C39,C74-C77 = 47nF ceramic
C40...C42 = 220nF, 5mm
C43 = 15pF
C55,C57 = 220μF 10V radial
C58 = 10pF trimmer
C60 = 27pF
C61,C63 = 4pF7
C62 = 10pF
C64 = 47pF
C65,C69 = 10μF 63V radial
C72 = 1000μF 25V
C68,C73 = 1000μF 16V

Inductors:
L1 = 60μH: 70.5 turns 0.1mm e.c.w. on 7F1S (Neosid)
L2 = 86μH: 84.5 turns 0.1mm e.c.w. on 7F1S (Neosid)
L3,L4,L6,L8 = 47μH choke
L5,L7 = 22μH choke

Semiconductors:
D1 = 5V1 zener, 0W5
D2 = 8V2 zener, 0W5
D3 = 1N4148
D4,D5 = 1N4002
D6 = low current LED
B1 = B80C1500 (straight)
T1 = BC547C
T2 = BC327
T3,T4,T5 = BC337
IC1 = TDA8395 (Philips)
IC2 = TDA4661 (Philips)
IC3 = AD827 (Analog Devices)
IC4 = AD847 (Analog Devices)
IC5 = TDA2579B (Philips)
IC6 = TDA8501 (Philips)
IC7 = TEA2014A (SGS-Thomson)
IC8 = 74HCU04
IC9 = 7805
IC10 = 7812

Miscellaneous:
JP1,JP2 = 2-pin PCB header with jumper.
JP3-JP6 = 3-pin PCB header with jumper.
K1,K2 = SCART socket, PCB mount.
K3 = 4-way mini-DIN socket, PCB mount (SVHS).
K4,K5 = cinch socket, PCB mount, e.g. T-709G (Monacor/Monarch).
K6 = cinch socket, chassis mount.
K7,K8 = see text.
K9 = 10-way boxheader
K10 = 2-way PCB terminal block, raster 5mm.
X1 = crystal, 4.433619MHz, C_{load} = 20pF.
DL1 = DL330 (Philips)
DL2 = DL470 (Philips)
Printed circuit board, order code 950078-2 (see page 70).

at the component overlay.

Although it did not seem to be strictly necessary on the prototype, screening may be fitted around the oscillator section on the board. This section (IC_8 and surrounding parts) is bordered by five holes intended for solder pins which serve to hold pieces of tin-plate in place. If you want, you may also fit a cover on the screening. If you do, remember to drill a small hole so you can access trimmer C_{58} with a trimming tool.

The power supply is also accommodated on the PCB. Referring back to the circuit diagram, you will notice that the power supply looks different from that in the PIP unit. Although the converter's power supply is also based on two fixed voltage regulators, one for 5 V and one for 12 V, the transformer's secondary voltage (applied to K_{10}) is much lower at about 9 V. This voltage is used to keep the dissipation in the 5-V section of the supply within safe limits. However, because the 9-V a.c. from the transformer is too low for the 12 V regulator, it is first doubled by a cascade circuit consisting of D_4-C_{73}-D_5-C_{72}. To ensure the best possible cooling, the heatsinks on regulators IC_9 and IC_{10} should be mounted a little above the circuit board. That is easily achieved with a small spacer, an extra nut, or similar. With IC_9, such a construction is even essential to ensure that the fixing hole of the PCB remains accessible.

The layout of the board allows the power supply section to be separated from the main circuit, where K_3, K_4 and K_5 may remain in their positions. If you do not envisage using the optional S-VHS connection, that section of the board may be cut off without problems.

Adjustment

Once the board has been built up and checked, the mains transformer may be connected to K_{10}, and the converter may be taken into use. No special tools or equipment are required at this point, although a plastic trimming tool may be useful to set L_1 and L_2.

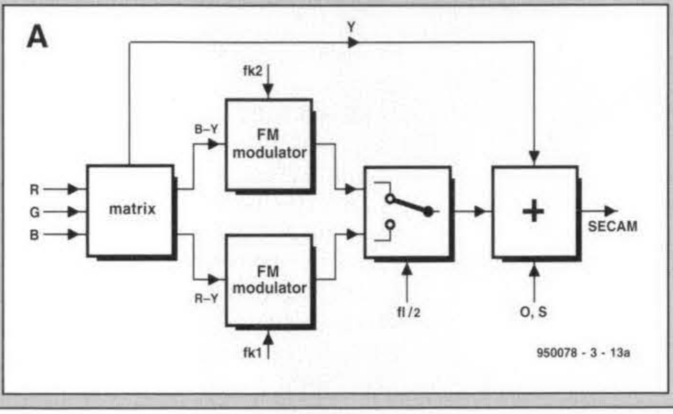
Start by setting the jumpers to the positions which correspond to the standard mode of the converter. So: JP_1 and JP_2 closed, JP_3 in position 'I' and JP_4 in position 'A'. Do **not** interconnect the PCB pins marked 'RGB'! Turn preset P_1 about ⅔ clockwise, and

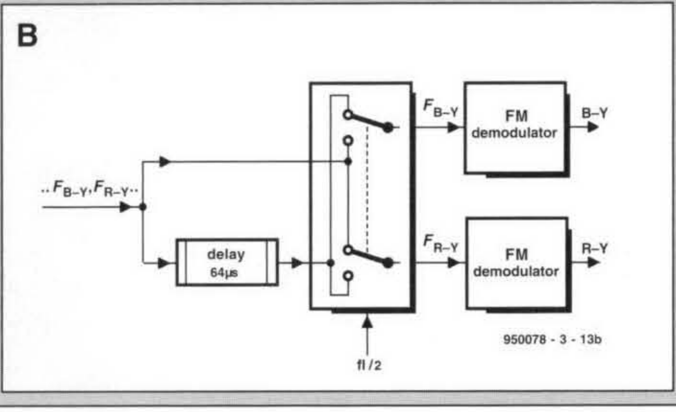
SECAM: THE FRENCH WAY

SECAM stands for 'séquentielle à mémoire', which indicates that this TV system is sequential and based on signal storage. As with the PAL system, the underlying principle of SECAM is that the colour information never changes drastically from one picture line to another. Furthermore, the human visual perception system is not 'annoyed' by a slightly decreased ability to resolve colour vertically. This gave the designers of the SECAM TV system the idea to transmit colour difference signals (which represent all colour information) in successive lines, rather than simultaneously. Consequently, the signal of one line has to be stored in a delay line for a period of 64 µs. After the delay, the output signal supplied by the delay line is combined with the signal of the next line. **Figure A** presents a simplified block diagram of a SECAM encoder. The associated decoder is shown in **Fig. B**. In the encoder, each of the two colour difference signals, B–Y and R–Y, is fed to an FM modulator. Next, the output signals of the two modulators are alternately connected through to a summing circuit. This switching is controlled by the line frequency. The summing circuit then adds the black-and-white signal. The carriers used to convey the composite signal are locked on to the line frequency. Noise suppression is improved by using different carrier frequencies for the two colour difference signals.

Apart from two FM demodulators, the decoder also contains a switching circuit and a delay line. In this way, the FM demodulators alternately receive a current colour carrier and one which has been delayed. To prevent distortion of the output signal, the reference frequencies of the demodulators have to be very stable. In the present decoder, the actual decoding operation differs a little from that illustrated in Fig. B. Although the principle remains the same, the present design has a delay line for each colour difference signal, and lacks a switch.

Obviously, there is a lot more to say about the SECAM TV system but unfortunately that is beyond the scope of this article.





P_2, P_3 and trimmer C_{58} to about the centre of their travel. Turn the cores in L_1 and L_2 so that their tops just protrude from the formers. In most cases, this adjustment will be fine, and no further action is necessary.

Next, connect a SECAM signal to K_1, and a PAL TV to K_2. Use **fully wired** SCART cables for both connections.

Switch on the converter, and turn P_1 until the picture synchronization is optimum. By turning the preset, try to find the extremes which still give a synchronized picture, and then set the preset exactly between these extremes. Next, adjust trimmer C_{58} for the best possible picture quality, preferably using a plastic trimming tool. Then try to find the settings on P_2 and P_3 which give the best possible picture quality. In most cases, these adjustments will be uncritical. For the ideal setting of gain adjustment P_2, you may also measure the output video signal at pin 19 of K_2. The measured level should be 1 V_{pp} into 75 Ω.

Finally, there are L_1 and L_2 which may require fine adjusting. These inductors serve to suppress residual levels of the SECAM signal, and should be adjusted for minimum interference in the output picture. Owners of an oscilloscope may adjust the cores for maximum suppression of both carriers.

Fitting the converter board into a case is left to your own ingenuity. Do consider, however, that the converter, based on its function, may be fitted into the same enclosure as the PIP processor! (950078-3)

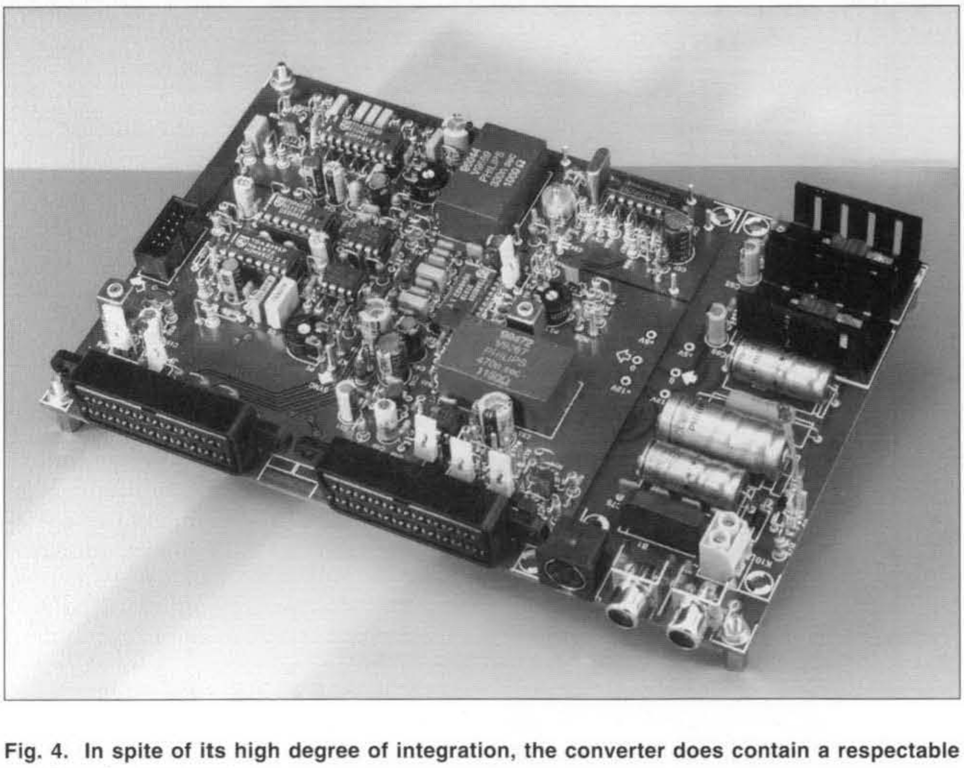


Fig. 4. In spite of its high degree of integration, the converter does contain a respectable number of components.

TRIANGULAR WAVEFORM GENERATOR AS ANALOGUE-TO-DIGITAL CONVERTER

Design by M. Brüggenwirth

A triangular waveform generator can be converted into a very precise analogue-to-digital converter with the aid of a single resistor. This converter may be configured for a variety of applications.

The basic setup of an analogue function generator is shown in **Fig. 1**. It is an integrator followed by a Schmitt trigger comparator, whose output is fed back to the input of the integrator. As long as the output signal is high, the capacitor is being charged; when the comparator changes state, the capacitor is being discharged. In this way, a triangular voltage ensues at the integrator output, and a rectangular one at the comparator output. Integrated circuit function generators, be it the old standby XR2206 or the modern MAX038, operate on the same principle. Often, a waveshaper is added to the comparator to derive a virtually undistorted sinusoidal signal. This is, however, not needed in the present design.

If, in Fig. 1, the output signal of the comparator is symmetrical with respect to earth, it is a square wave. If, however, an additional voltage is applied across *R'* at the integrator input, the comparator output is a rectangular wave of different frequency. The duty factor of this signal depends on $U_{R'}$.

Charging and discharging

The inverting input of the operational amplifier forms a virtual earth, so that a current $I = U_b/R$ flows through resistor *R*. The state of the comparator output (high or low) determines the direction of flow of the current. A current $I_{in} = U_{in}/R$ flows through resistor *R'*, so that capacitor *C* is charged or discharged linearly with a current $I_C = I + I_{in}$.

Up to time t_1 in **Fig. 2**, the voltage at the integrator is positive waveform peak, U_{SO}. Then, the output of the comparator changes states (goes high). A current $I_t = I + I_{in}$ flows into the capacitor, and the output voltage of the (inverting) integrator falls linearly until t_2 is reached, when the potential at the integrator is negative peak U_{SU}. The comparator again changes state, that is, becomes negative for a time T_E. If during that time the level of *I* is higher than that of I_{in}, that is, I_t becomes negative, the integrator output rises until time t_3 is reached, whereupon the process repeats itself.

Circuit description.

A practical circuit is, of course, not as straightforward as just described. For example, the basic circuit was powered by a symmetrical supply, whereas the circuit in **Fig. 3** has a single 5-V supply.

Reference voltage CV at pin 5 of IC_2, which is derived from an internal potential divider, is buffered by IC_{1a} and applied to the non-inverting input of integrator IC_{1b}. With a supply voltage U_b = 5 V, the reference voltage is typically 3.3 V ($2/3U_b$), but may be quite different.

Since the output of IC_{1a} is capacitively loaded by the input source, compensating network R_4-C_2 is essential.

The peak positive and negative voltages of the comparator are:

$U_{SO} = 2/3U_b$

and

$U_{SU} = 1/3U_b$ (CV plus TR – pin 2)

The potential across C_1 fluctuates between these values.

The timer output is not applied directly to the integrator, but via T_1.

The current through R_2 is

$I_{R2} = (5 - 3.3)/39 \times 10^{-3} = 45\ \mu A.$

As long as the output of IC_2 is low, T_1 is cut off and C_1 is charged with a current of 45 µA.

When the output of IC_2 goes high, T_1 conducts and connects the output to earth. The current through R_3-P_1 to earth is then

$I_{R3} = 3.3/(R_3 + P_1) = 90\ \mu A.$

Half this current derives from the power line, the other half is the dis-

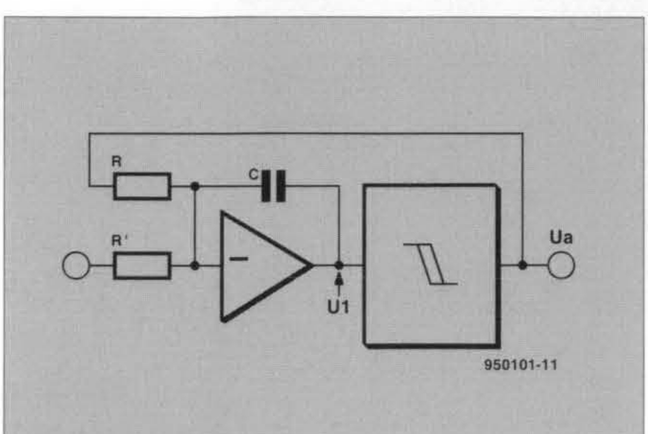


Fig. 1. Block diagram of a simple function generator with additional analogue input via *R'*.

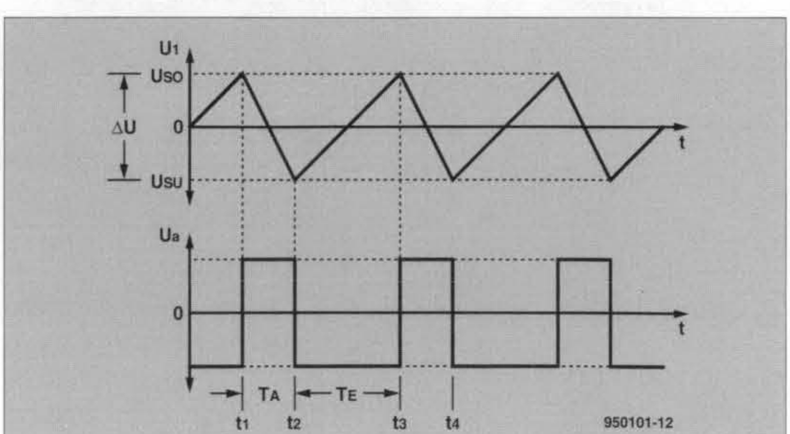


Fig. 2. Timing diagram of the integrator signal, U_1, and of the rectangular output signal, U_a, of the comparator.

charge current of C_1. Thus, provided P_1 is set correctly, the charging and discharge times of C_1 are equal. The consequent output is a square wave signal (but, of course, only if no input voltage is applied across R_1. This means that the level of the supply voltage, the level of the reference voltage, the potential across the capacitor, the value of C_1, and the charging and discharge resistors, provided these are all constant, have no effect on the duty factor, which is determined solely by the input voltage.

Some design formulas

The integrator capacitance, C, is defined as

$$C = \frac{Q}{U} = \frac{I\Delta t}{\Delta U}$$

where ΔU is determined by the two peak values of the comparator; the capacitor is charged (T_A) and discharged (T_E) in the time interval Δt.

$$C = \frac{(I + I_{in})T_A}{U_b / 3}$$

$$C = \frac{(-I + I_{in}) \cdot T_E}{-U_b / 3}$$

Equalizing these two quotations and solving for I_{in} gives

$$\frac{(-I + I_{in}) \cdot T_E}{-U_b / 3} = \frac{(I + I_{in}) \cdot T_A}{U_b / 3}$$

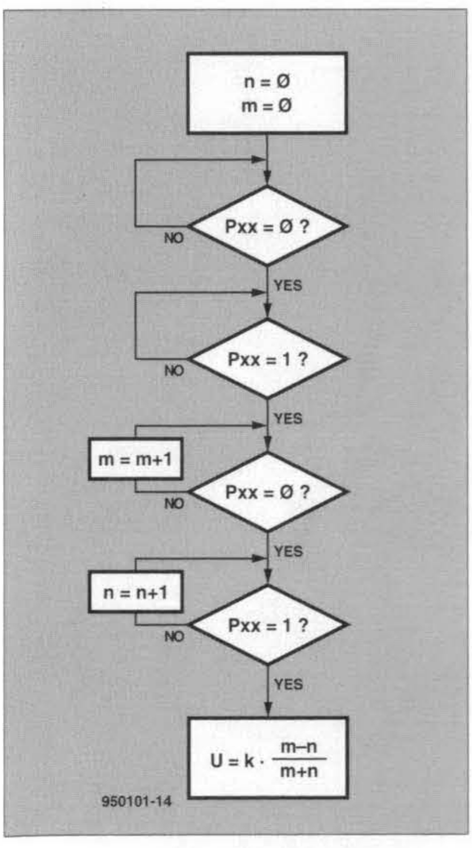


Fig. 4. Flow diagram of a control program of the converter.

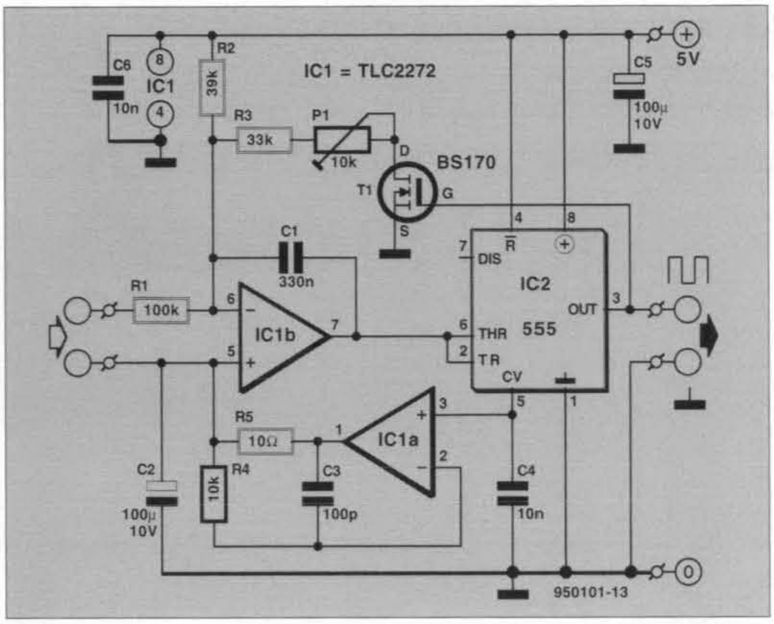


Fig. 3. The circuit of the analogue-to-digital converter comprises two op amps and a timer.

$$I_{in} = I\,\frac{T_E - T_A}{T_E + T_A}$$

The current I may be replaced by

$$I = \frac{U_b}{3R_2} \qquad (\text{if } U_{R2} = U_b / 3)$$

and I_{in} by:

$$I_{in} = \frac{U_{in}}{R_1}$$

Substituting these equations gives

$$U_{in} = \frac{R_1}{3R_2} \cdot U_b \cdot \frac{T_E - T_A}{T_E + T_A}$$

Unlike the duty factor, the period (and thus the frequency) of the output signal depends on the peak values of the output voltage, the supply voltage and the value of C_1.

$$T = T_A + T_E = C \cdot \frac{U_b}{3} \cdot \frac{I}{I^2 - I_{in}^2}$$

$$f = \frac{3I}{2CU_b} \cdot \left[1 - \left(\frac{I_{in}}{I}\right)^2\right]$$

$$f = \frac{1}{2R_2C_1} \cdot \left[1 - \left(\frac{U_{in}}{U_b} \cdot \frac{3R_2}{R_1}\right)^2\right]$$

To avoid large frequency fluctuations, the right-hand term should not exceed about 0.25.

$$\frac{U_{in}}{U_b} \cdot \frac{3R_2}{R_1} \le 0.5$$

To obtain an accuracy of eight bits, the write frequency, f_{CPU}, of the computer must be at least a factor 2^9 higher than the converter frequency, f_{DAW}. This allows the value of C_1 to be determined:

$$C_1 > \frac{2^9}{f_{CPU} \cdot R_2}$$

The value of R_1 must be chosen such that the input signal can vary within the desired limits.

Software with three routines

The necessary software consists of one compute and two count routines—see **Fig. 4**—taking no more than a few blocks in a language like BASIC. The counting loops should be sampled about 4000 times (depending on the values of R_2 and C_1) in any measurement period. If the software is too slow, or too fast, the value of C_1 must be altered accordingly. This changes the measurement period (normally about 200 ms), but it avoids rounding off errors in the computation.

The program must, of course, not be interrupted during the counting loops. Unless an additional card with real-time timers is used, the PC is normally not able to drive the program.

After the converter has been connected to the PC, P_1 must be adjusted to give exactly 0 V at the open-circuit output. Apply a known voltage, U_{in}, to the input and turn P_1 until 0 V is obtained. The preset is not required if the software provides scaling of the indicated values. In this case, R_3 must be 39 kΩ.

[950101]

g65016-I

FROM THE WORLD OF ELECTRONICS

Our International Editorial Team wishes all our Readers

A Happy and Peaceful 1996

(from left to right: Jan Buiting, Harry Baggen, Giel Dols, Sjef van Rooy, Ernst Krempelsauer, Hans Steeman, Guy Raedersdorf, Rolf Gerstendorf, Len Seymour, Pierre Kersemakers)

THE LIBERATED SOFTWARE MARKET

The liberalization of the British telecommunications market did not just allow new companies, such as Mercury and Energis, to compete with BT for customers. Another result is that, because today's customers are receptive to new ideas, companies have grown up to develop new and innovative products which were unimaginable just a few years ago.

To strengthen this sector, and to help UK companies compete effectively, a joint initiative called Telecoms 2000 has been set up by the UK Department of Trade and Industry (DTI) and the trade association Federation of the Electronics Industry (FEI) in collaboration with BT, Cable & Wireless, Ericsson, GPT, Motorola and Nortel. The aim of the initiative is to encourage a UK≠based network of small supplier companies who can deliver world class products and services. In particular, this applies to software, which is a particularly strong area within the UK telecoms industry.

User software

A very fruitful area is in user software which, by improving access to a service, boosts usage and thus has a multiplier effect on the size of its potential marketplace. For example, the off-line readers (OLRs) developed by Ashmount Research Ltd (ARL) have been instrumental in making CIX easier and cheaper to use.

Compulink Information eXchange (CIX – pronounced kicks)[1] was set up in 1985 as the UK's first public-access on-line e-mail and conferencing service. It allowed both private individuals and companies to send local and world-wide e-mail as well as set up both private and public discussion groups known as conferences. They are extensively used for product support and information distribution.

In the early days of systems such as CIX, users would dial in from their computer via modems and give the appropriate commands to request the system to download any waiting messages and then type in their replies or new messages directly. Being connected to the remote computer while carrying out these actions (in countries with high telephone charges) resulted in fairly high – some thought 'horrendous' – system and telephone usage charges.

New messages

An OLR allows a user to write new messages (both private and for conference 'discussion') and read existing replies off-line without being connected to the remote system. The, when the user dials in, the OLR automates all the necessary activities and is typically 40 times faster than when on-line manually to carry out the same activities.

ARL was founded in 1990 to provide the corporate communications market with an OLR offering conferencing, e-mail, file transfer and information retrieval. It was not long before the appeal of the product also took it into the leisure or single-user sector of the market.

The company has been a pioneer in developing OLR or Navigator software that works with a variety of host commercial systems and was the first organization in the world providing unified integrated interfaces to multiple host systems. Today, it offers both standalone and network products to access CompuServe, Delphi, CIX, BIX and others.

In September 1995, Ashmount Research[2] launched a new generation of its software to supersede its WigWam and PowWow range to take a new direction in product strategy. From then, all products are known as Virtual Access, a name which is felt to truly describe the nature of the product.

Information transfer

Although the product still gives the user the ability to work off-line, it offers much, much more in the way of information transfer and management and will also include extensive Internet functionality.

Internet is also the *raison d'être* of Turnpike Ltd[3]. It was established by Locomotive Software Group Ltd, which has been producing low-cost software for the past seven years to address the need for easy-to-use, cost-effective electronic messaging software for both major Internet suppliers, small business and home users.

Chris Hall, Turnpike's managing director, explains: "As users of the Internet, we quickly discovered that there was little or no software which was simple to use and offered all the basic Internet functions for the dial-up user. So, we decided to develop our own. People don't need to be computer experts to use Turnpike. It's designed to be easy to use and straightforward to install. Most popular modems and access providers are supported."

Basic functions

Turnpike, which was launched in May 1995, offers all the basic Internet functions: Mail, News, FTP, Finger and Ping. There is also a built-in Winsock to provide access to other Internet functions such as WWW (the World Wide Web) with registered users being offered a copy of a Web browser.

The aim of the designers of Turnpike has been to produce a package which meets the needs of businessmen wishing to make use of the Internet without the computer or software getting in the way.

While Turnpike is a new company formed to take advantage of an emergent market, Wordcraft International Ltd (WIL)[4] was formed in 1978 when the first version of the Wordcraft word processing package for the Commodore PET range of microcomputers was written. Since then, it has become a major force in fax software.

Now, its LaserFAX is the market leader in the fax machines' PC-connectivity market world-wide. Furthermore, its computer fax protocol CFP has been submitted to the ITU (International Telecommunications Union) for consideration as an international standard.

Close relationships

Mike Lake, WIL's managing director, points out that the company has developed very close relationships with fax machine manufacturers in many countries around the world. A number of these are, or will be, bundling WIL software with their equipment. Furthermore, in the new market for multifunction digital machines – printer, scanner, copier, manual fax and computer fax – a wide variety of manufacturers world-wide already feature WIL's software.

However, hardware and software can come together. Psion[5], makers of the Series 3a, which is the world's number one selling palmtop, has developed Psion SMS Link, which it is selling as a cable and software bundle to enable 3a users to hook up to a Nokia 2110 digital phone or Orange phone to make use of the SMS (Short Message Service). This is intended as a corporate product for vertical applications and will be used as a development kit for value-added resellers.

Not only will this provide an opportunity for even smaller companies to move into communications software applications, it will enable applications to be developed to meet specific user needs. And, after all, this is the requirement because telecommunications is a means to an end and not the end itself.

[1] CIX Ltd, London House, The Square, Llanrwst, Gwynned, Wales, United Kingdom LL26 0LD. Tel: +44 (0)1492 641 961. Fax +44 (0) 1492 641 538.

[2] Ashmount Research Ltd, 26 Baker Street, London, United Kingdom W1M 1DF. Tel: +44 (0)171 935 7712. Fax +44 (0)171 935 7713.

[3] Turnpike Ltd, Dorking Business Park, Dorking, Surrey, United Kingdom RH4 1HN. Tel: +44 (0)1306 747 747. Fax +44 (0)1306 747 749.

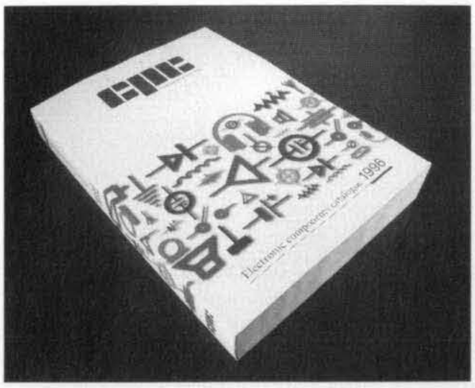
[4] Wordcraft International Ltd, Kelmscot House, Vernon Street, Derby, United Kingdom DE1 1FR. Tel: +44 (0)1332 371 428. Fax: +44 (0)1332 295 525.

[5] Psion PLC, Alexander House, 85 Frampton Street, London, United Kingdom NW8 8NQ. Tel: +44 (0)171 262 5580. Fax: +44 (0)171 258 7341.

NEW CATALOGUE FROM COMBINED PRECISION COMPONENTS

The new 1996 catalogue from Combined Precision Components—CPC—contains an extensive range of products in over 1600 pages of full colour. It features everything from OEM spares to the latest computer, electrical and mechanical accessories and components.

In total, over 39,000 products, including nearly 10,000 new items are shown in the new catalogue. All items are competitively priced to give the customer one of the most cost-effective, off-the-shelf and comprehensive methods of sourcing products.



Recent additions to the catalogue are products from blue-chip companies such as Brother, IBM Lexmark, Samsung, and Black & Decker. Several new product sections have been added to this year's catalogue, including opto-electronics, PCB prototyping, surface mount, motor control and data comms/networking.

The catalogue now contains 53 sections, including switches, tools, and remote controls. Every one of the sections has been tailored to meet the demand of the ever-changing market. To assist customers, each product is accompanied by a brief description and colour photograph.

CPC is dedicated to service the industrial and commercial user, but its catalogue and service are becoming increasingly popular with other market sectors, such as education.

Another aspect of the CPC operation is that customers need not waste time looking for the part number they require. By simply ringing CPC's Partfinder Service, operators will access the vast and constantly expanding database of 750,000 products to find the parts you need. The highly trained staff, backed by the latest technology, handle 3500 calls and 3000 orders a day and four new fax lines are being installed to help cope with demand. Not only this, but CPC ensures that language is no barrier to their potential customers. Qualified personnel in the Export Department are able to deal with orders and enquiries in German, French and Spanish.

On the day the 1996 catalogue was published, CPC opened a new 2800 m^2 extension to its warehouse at Preston. The company is currently drawing up plans for a high-bay warehouse to join this extension by the end of 1997.

Available free of charge, CPC's 1996 catalogue is offered to all account holders; new accounts can be opened simply by ringing one of the many telephone sales operators.

For a copy of the catalogue, contact:

Combined Precision Components PLC
Component House
Faraday Drive
Fulwood
Preston PR2 4PP
Telephone 01772 654455
Fax 01772 654466

ATMEL MICRO PRO FOR ONLY £ 99

Equinox Technologies has recently launched a low-cost programmer to support the Atmel range of FLASH-8051 microcontrollers. The 'Atmel Micro Pro' can program both the 40-pin 8951/8952, the new 20-pin 1051/2051 micros and most serial EEPROMs from Atmel. To meet popular demand, the Intel and Philips 87C51/52 generic parts are now also supported.

The 'Micro Pro' is different from most low-cost programmers in that it is based around Field Programmable Gate Array (FPGA) technology rather than using a microcontroller. Every time a device is to be programmed, the digital circuitry required for programming the target device is downloaded from the PC into the FPGA. This allows the hardware to be customized to suit each device, giving faster programming times and future device support without the need for expensive adapters.

The new AT89C2051 from Atmel is an 8051 in a 20-pin package. The 2 kb on-chip reprogrammable FLASH ROM can be erased, programmed and verified in under five seconds with no need for a UV eraser (guaranteed 1000+ reprogramming cycles). The device features 128 bytes of RAM, 15 I/O lines capable of direct LED drive, two 16-bit counter/timers and five interrupt sources. The standard 8051 serial UART has also been included, together with an analogue comparator useful for A/D conversions.

The 'Micro Pro' has recently gained official programming approval from the Atmel Corporation for programming their complete range of FLASH microcontrollers. To celebrate the association, Equinox are offering an Atmel 'Micro Pro' programming system, together with a FREE Atmel AT89C1051 and a FREE AT89C2051 microcontroller, data sheets, PSU, parallel cable and an IC extractor tool for only £99, excl. VAT and p&p. The offer ends on 31 December 1995. For further details call John Marriott on +44 1204 491 110. See also advertisement on p. 39.

SKY TELEVISION WORLD LARGEST

Last November, Sky Television launched six new channels, bringing their total to 28; this makes it the world's largest direct-to-home network.

965013-1

NEW PRODUCTS NEW PRODUCTS NEW PRODUCTS

Slash PIC16/17 Development Time

Microchip's new MPLAB Integrated Development Environment software gives PIC16/17 microcontroller developers the flexibility to edit, compile and emulate from a single user interface. The sophisticated MPLAB software is now available as part of Microchip's PICMASTER Universal Development System.

MPLAB includes a project manager and program text editor, a user-configurable toolbar containing four predefined toolsets and a status bar which communicates editing and debugging information. A dynamic error capability allows rapid application development with a simple click on any error listing, returning the user to the source code for quick editing.

Integrated development tools have long since been available for workstation and high-end PC-based developers. MPLAB offers the same flexibility to 8-bit microcontroller developers. Operating under a Microsoft Windows environment, the PICMASTER development system also includes an emulator control pod, target specific emulator probe, PRO-MATE device programmer, PC hist interface card, demonstration hardware and software.

Existing PICMASTER users can integrate the MPLAB software into their systems at no cost by downloading the new productivity tool from Microchip's Bulletin Board System (BBS). Users can connect to the Microchip BBS through the CompuServe communications network.

Arizona Microchip Technology Ltd., Unit 6, The Courtyard, Meadowbank, Furlong Road, Bourne End, Bucks SL8 5AJ. Tel. (01628) 851077, fax (01628) 850259.

Simpler Access to IDT Product Info: WWW and CD-ROM

Integrated Device Technology Inc. (IDT) has set up a number of new methods to access product and company information, including data sheets for IDT's complete range of products.

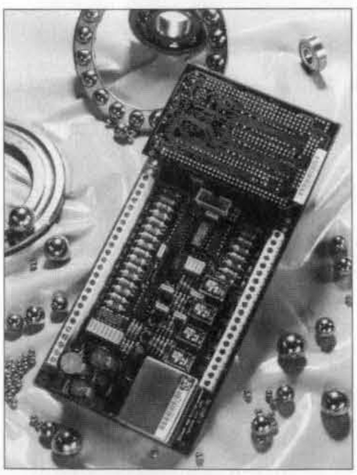
A free CD-ROM, designed for use on Macintosh, Windows, DOS and SUN Unix systems, is now available. It uses the Adobe Acrobat portable document format reader to display and print pages of information from the many sources that IDT has brought together onto this one medium. Macintosh and Windows users can use hyperlinks to move easily between documents.

Information on the CD-ROM includes data on RISC processors, multiport and FIFO memories, and high-speed logic and interfacing devices, plus product selector guides, application notes, quality reports, and background information on the company.

For those users who are on-line, almost all of the same information is provided via IDT's home page on the World Wide Web (http://www.idt.com). The advantage of this system is that the information is always the most up-to-date available, with pages being updated daily. Information can also be retrieved using anonymous ftp using ftp.idt.com/docs/docid.ext. All documents on the ftp server are in Adobe Acrobat format. On-line users can also contact IDT's European sales operation by sending e-mail to eurosales@idt.com.

Anyone who is not on-line but who needs information immediately, can use IDT's fax server. This Fax-on-Demand service offers all the same information as the CD-ROM, except manuals, which are too long to be practical to send. Fax-on-Demand can be accessed by calling +1-408-492-8341 and following simple directions.

Integrated Device Technology, Europe, Prime House, Barnett Wood Lane, Leatherhead, Surrey KT22 7DG. Tel. (01372) 363734, fax (01372) 378851.



Intelligent I/O and PLC from Cambridge Micro Systems

A new low-cost industrial controller from CMS provides full signal conditioning on each of 12 opto-isolated non-polarized inputs and 4 isolated voltage-free outputs. The card can be programmed in Ladder Logic, 'C', or both, the latter offering full deterministic control of the I/O but providing the flexibility of 'C'. When used as a PLC the user can select the scan time required, for fast applications this can be as low as 500 μs and still provide full communications and networking, the default is 10 ms.

CMS claim that at £95 in quantity this is the highest specified, lowest cost controller available today. the specification includes: 16/32-bit CPU 68000 compatible up to 1 MByte of EPROM, and 512 Kbytes of SRAM plus EEPROM, 2 fast hardware timer/counters, on board PSU, expansion options, I^2C or MBus, RS232 or RS485 with full networking and remote I/O protocols such as MODBUS etc. The latter can also be used for remote programming and re-programming as well as interfacing to most SCADA packages and Visual BASIC. A low-cost radio option is also available for remote locations or remote networking.

Cambridge Microprocessor Systems Ltd., Unit 17-18 Zone D, Chelmsford Road Ind. Estate, Great Dunmow, Essex CM6 1XG. Tel. (01371) 875644, fax (01371) 876077.

(965013-1)

INTERNATIONAL CIRCUIT DESIGN COMPETITION RESULTS

Last month we published the design that won the International First Prize, a Tekscope THS720.

This month we continue the success story of our International Circuit Design Competition (July/August 1995) with a 16-page supplement which contains a selection of prize winning designs submitted to the German (G), Dutch (NL), French (F) and English (UK) language editions of Elektor magazine. It is our intention to publish, in random order, the Top-3 winning designs from each language edition, giving a total of 12 circuits, in two instalments of 16 pages each.

Designs are published 'as is', i.e., with only minor editorial corrections to the text. **Please note that none of the published circuits have been tested by ourselves.**

Results Overview

Prize	Winner	Design
1st, Int.	L. Lamesch	50 MHz 16/32-bit logic analyser
UK advertiser sponsored prizes:		
1st	**C. John Dakin**	**A low-cost wind powered battery charger**
2nd	**Sami Karhulahtie**	**Simple stepper motor control**
3rd	**Jankjijewic Ninoslav**	**8-bit logic analyser for PC parallel port**
4th (1)	P.J. McGrath	Power reduction in domestic refrigeration appliances
4th (2)	Robert Kiss	Eight channels timer
4th (3)	Pawel Rosiak	Universal clock oscilator unit
4th (4)	Robert Postula	Low-cost packet radio modem
5th	Tapio Tyni	Measure 20log(U1/U2) with an ordinary DVM
6th	Christian de Godzinsky	Telephone intercom system
7th	Gary Taylor	Garage door / driveway gate controller
8th	Hans Henrik Skovgaard	Parallel I/O interface
9th	Jose M. Miguel	Active probe for Pico ADC-10
10th (1)	P. M. R. dos Reis Metelo	Car light alarm
10th (2)	Erik Larsen	Small remote camera & flash releasing gear
10th (3)	Zdzislaw Kaszta	One-IC metal detector
10th (4)	D. Nelson	Water level monitor
10th (5)	Sved Martinsson	Car battery control

EIGHT-BIT LOGIC ANALYSER

3rd Prize (UK)

For PC Parallel Port

An 8-bit 50-MHz on PC parallel port Logic Analyser for home application is always a useful tool for small digital projects, especially in field µP applications. Eight bits with two triggers, 512 bytes and a maximum sample rate of 50 MHz are good specifications for hobby users. Low power and portability are also important if you want to use this tool with a laptop computer on the road. Optionally, you may use one 6-bit flash A/D converter at the input and so obtain a combination of one analogue and two digital inputs.

By Jankijewic Ninoslav, el. ing.

My first idea was to make a logic analyser with a very small number of components, and as simple as possible. I had one sample of a CMOS FIFO from IDT (Integrated Device Technology, Inc.) type IDT72210 in a 28-pin 300-mil plastic DIP case. Important features for this project are: a 512×8 bit memory array structure, 15-ns read/write cycle time (66-MHz clock), and dual ports for input and output data. I decided to use this chip (with 25 ns cycle time) for my application.

To tackle another problem, the triggering and time base, I selected a PAL from Altera, type EP910. The time base is built from a 2-5-10 dual decade counter 74HC390 which produces three output frequencies, 20 MHz, 8 MHz and 4 MHz.

In the block diagram, **Fig 1**, the signal from the XTAL oscillator (40 MHz) goes to the decade counter and a selector which switches the programmable clock or the maximum clock from the XTAL generator.

Programmable clock is selected with four bits named A, B, C and D. With these four bits the desired sampling rate is selected as shown in **Table 1**. A programmable counter contained in the PAL can divide one of three input frequencies by 1, 10, 100 or 1000.

The trigger section is also based on a PAL, and uses two direct signals from input ch0 and ch1. With four bits E0, T0, E1 and T1 we can select the trigger edge polarity. **Table 2** gives an overview of these settings.

Register 1 (CD4094) is used to set all eight bits and select the mode of operation for the Logic Analyser. To read data from FIFO memory, a MUX (74HC157) is used with a control input (1, low/high) to select and read four low or four high bits of data.

The procedure to start

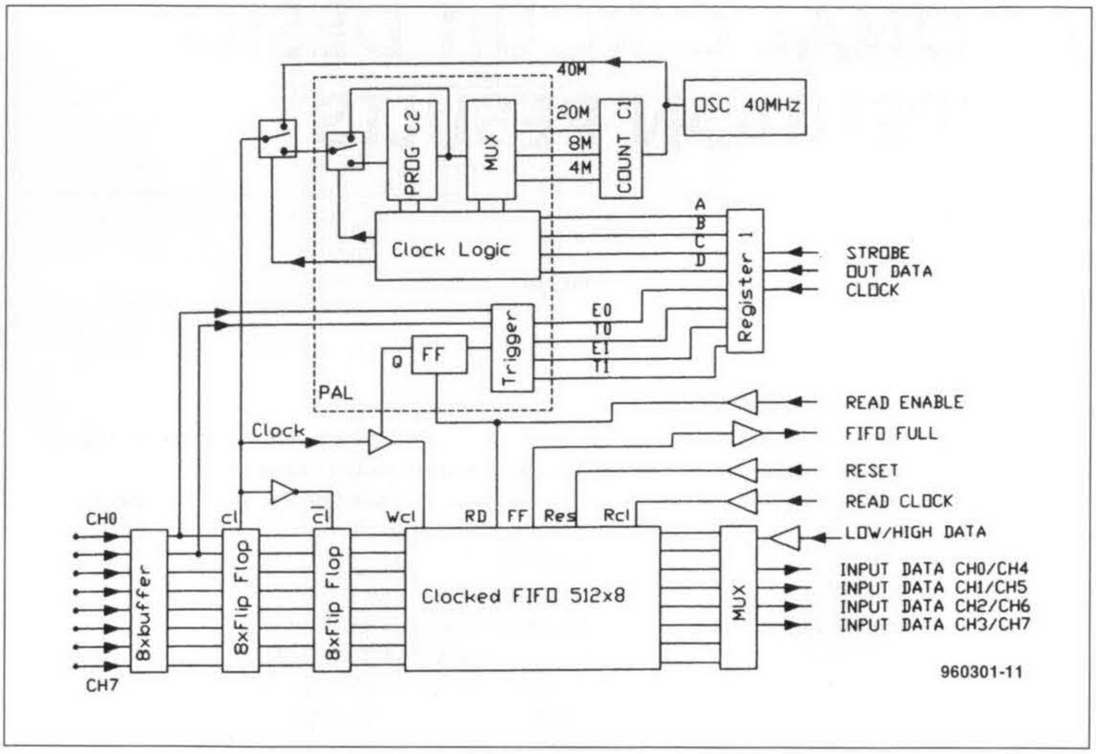


Fig. 1. Logic analyser block diagram.

Table 1

A	B	C	D	RATE
0	0	0	0	40 MHz
1	0	0	0	20 MHz
0	1	0	0	8 MHz
1	1	0	0	4 MHz
1	0	1	0	2 MHZ
0	1	1	0	800 KHz
1	1	1	0	400 KHz
1	0	0	1	200 KHz
0	1	0	1	80 KHz
1	1	0	1	40 KHz
1	0	1	1	20 KHz
0	1	1	1	8 KHz
1	1	1	1	4 KHz

Table 2.

E0	T0	E1	T1	action
0	x	0	x	disable trigger
1	0	x	x	+trigger ch0
1	1	x	x	–trigger ch0
x	x	1	0	+trigger ch1
x	x	1	1	–trigger ch1

scanning the digital input, read data and display it on the PC screen is :

1. Reset FIFO signal, RES=0, and reset FIFO read function, RD,OE=1. At the same time the trigger flipflop will be reset.
2. Set trigger and time base bits (Tables 1 and 2).
3. Reset FIFO signal, RES=1.
4. Wait till FIFO Full Flag, FF=1.
5. Enable read FIFO function, RD=1.
6. Read all 512 bytes of data (Q0/Q7) in three steps:
a) output one read clock RCL;
b) read low data (4 bits from MUX);
c) read high data (4 bits from MUX).
7. Display data on PC display and go to step 1.

The first three steps may be controlled and programmed in BASIC (I used Power Basic). For the remaining steps (4 through 7) it is best to use assembler for fast data updating.

Hardware

The power supply may be an external unregulated 9-V DC source. The board contains a standard 7805 regulator for a clean 5 V supply rail. Supply current is about 250 mA at 40-MHz sampling rate. A 40-MHz XTO and a buffer 74ACT04 are used for the clock source.

Frequency selection outside of the PAL is achieved with a three-state buffer (74HC125) which is also used for the trigger gate. Digital input signals are buffered by a standard 74HC541 and then passed

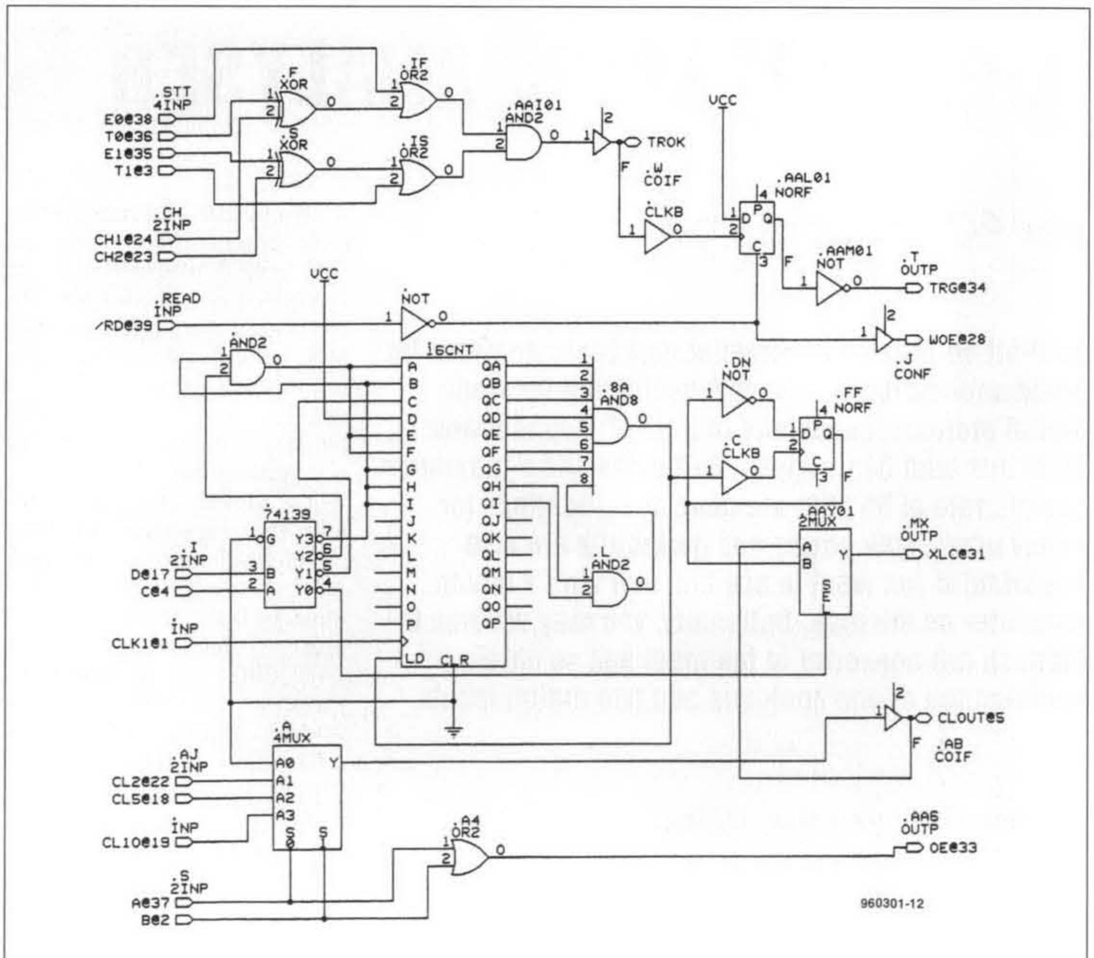


Fig. 2. PAL EP910 internal schematic.

to two octal D-type flipflops 74HC574 which are clocked at the same clock and opposite phase. When the main trigger occurs, the FIFO input receives a one-clock delayed signal which occurs one clock before the trigger action.

The printed board is a single-sided home-made product with seven jumpers at the top side and one jumper (j4) at the bottom side. If you use double-sided board it is recommended to use the top side for a ground plane. There are no direct connections between the computer and critical components like the FIFO and the PAL. To separate signals like Read Enable, Fifo Reset, Read Clock and Fifo Full Flag from the computer a darlington transistor array type ULN2003 is used. Each collector has a load resistor of 3k3(RN2). There are no critical parts except the blank PAL which must be programmed with a special PAL programmer. A PAL from INTEL, series EPLD type 85C090-20, may also be

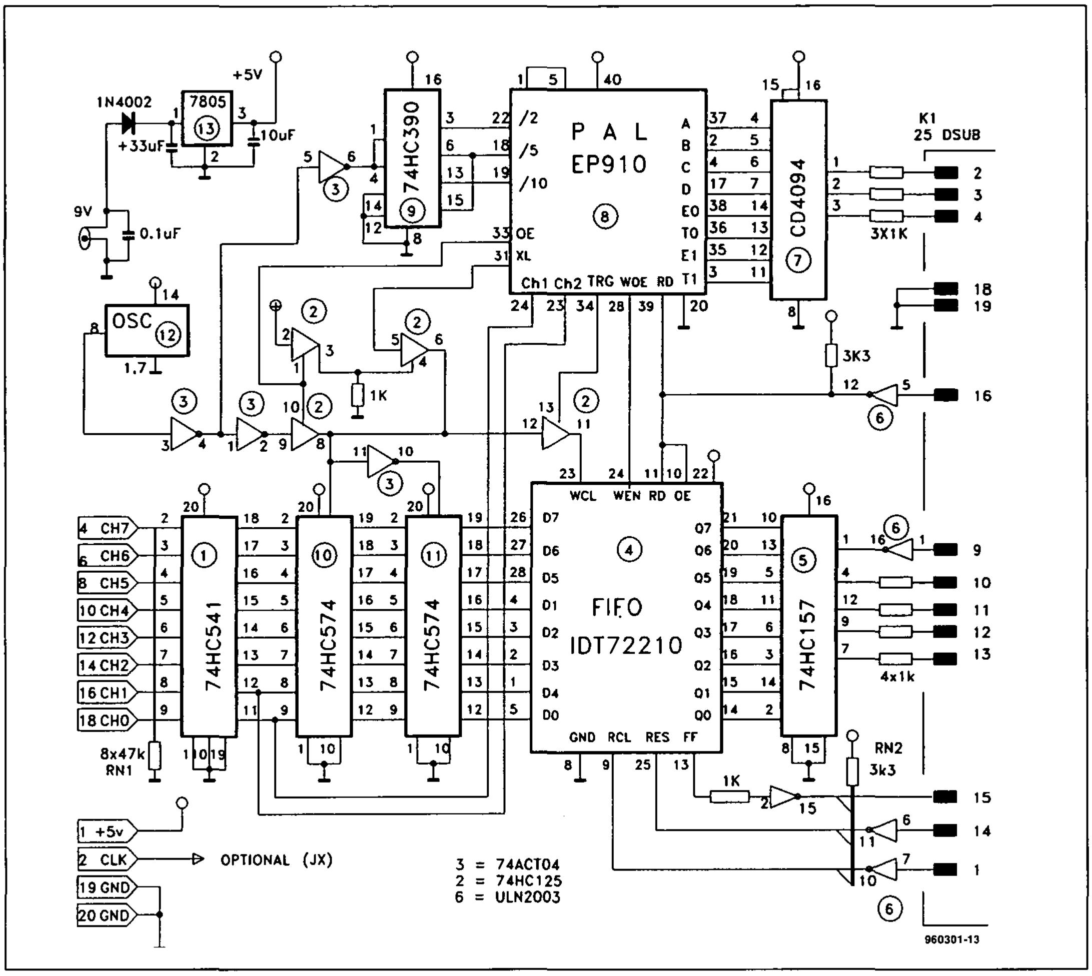


Fig. 3. Circuit diagram of the Logic Analyser.

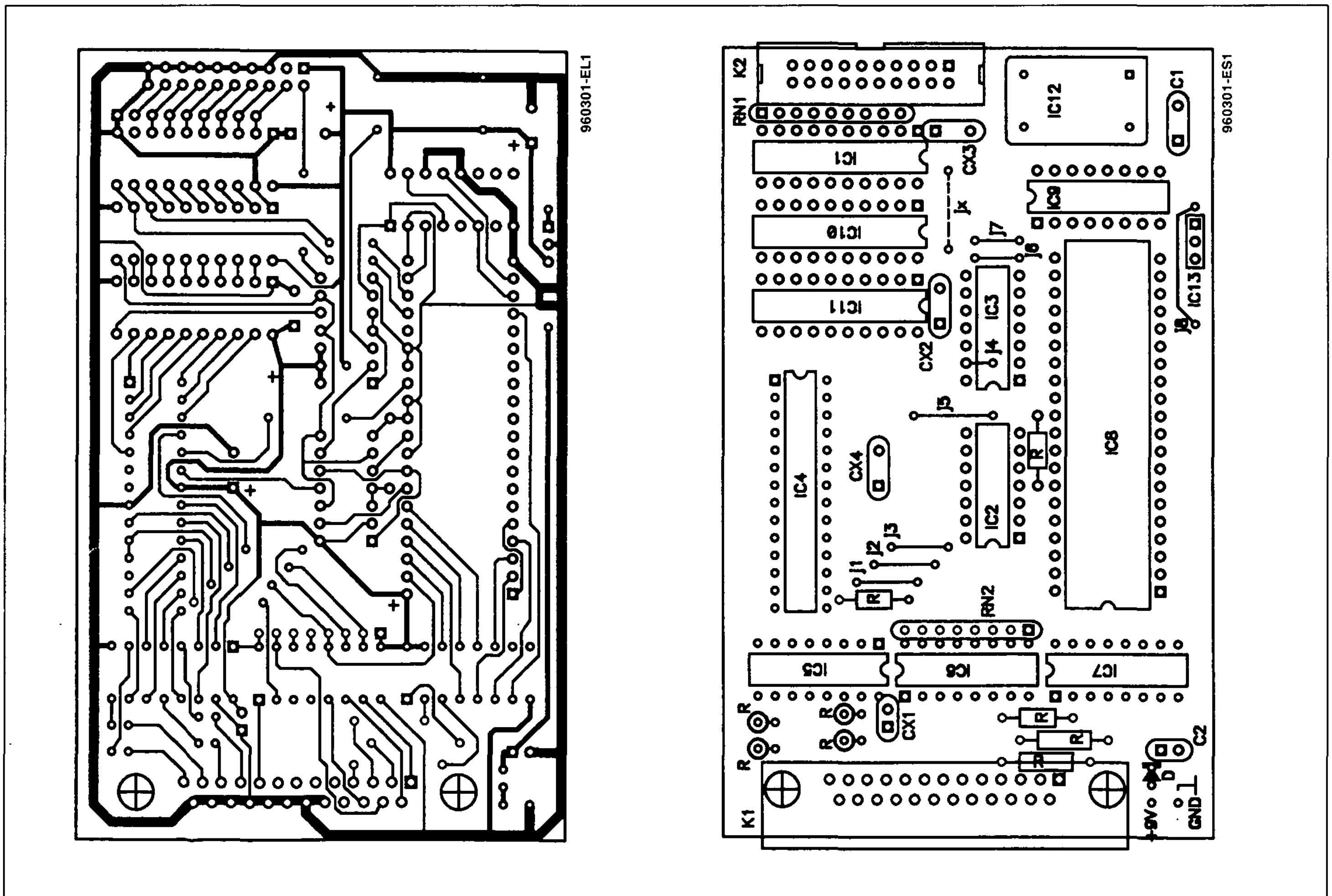


Fig. 4. PCB copper track layout and component mounting plan.

Table 3.

LPT1 pin	signal	port address	function	name
1	STROBE	out 37A bit 0	read clock for FIFO	RCL
2	DATA0	out 378 bit 0	strobe for Register 1	STR
3	DATA1	out 378 bit 1	Data for Register 1	DOUT
4	DATA2	out 378 bit 2	clock for Register 1	CL
5-8	DATA3-6	out 378 bit 3-6	not used	
9	DATA7	out 378 bit 7	select L/H data	LOW/HIGH
10	ACK	in 379 bit 6	data input bit 3/7	Q3/Q7
11	BUSY	in 379 bit 7	data input bit 2/6	Q2/Q6
12	PE	in 379 bit 5	data input bit 1/5	Q1/Q5
13	SEL	in 379 bit 4	data input bit 0/4	Q0/Q4
14	AFD	out 37A bit 1	reset FIFO	RES
15	ERR	in 379 bit 3	read FIFO Full Flag	FF
16	INI	out 37A bit 2	read enable for FIFO	RD-OE
17	SLC	out 37A bit 3		not used
18-25	GND		ground	GND

used here. The PAL's internal diagram is given in **Fig 2**.

Software

Before I started to write a driver in assembler, all hardware test were performed in Power Basic. The test program was based on the information contained in **Table 3**.

The final software is divided in two parts. The main program, written in BASIC, sets all modes for the Logic Analyser. The assembly code driver is linked with the BASIC program, and is used for fast reading of the FIFO buffer, and displaying data on the screen. (960301)

Components list

CX1,CX2,CX3,CX4	0.1μF
All R	1kΩ
RN1	47kΩ network
RN2	3kΩ3 network
C1	10μF tantalum
C2	33μF tantalum
D	1N4002
IC1	74HC541
IC2	74HC125
IC3	74ACT04
IC4	IDT72210-25 (clocked FIFO)
IC5	74HC157
IC6	ULN2003
IC7	CD4094
IC8	EP910-25T (EPLD PAL 40-pin)
IC9	74HC390
IC10,IC11	74HC574
XTAL 40MHz	IC12 (TTL oscillator)
uA7805	IC13
D25-SUB-90°	K1
20P-90°	K2

Programming files for this project available on disk, see Readers Services page (p. 70).

A LOW COST WIND GENERATOR BATTERY CHARGER

1st Prize (UK)

Small wind powered generators are useful devices for people dependent on battery power, such as caravaners and yachtsmen. Commercial products are expensive. The smallest models cost over £250. A generator giving up to 30 watts output can be made using a permanent magnet radiator fan motor, obtainable from a car breaker, costing about £5, a DC-DC converter, described here, costing less than £15, and an 800-mm diameter wooden propeller described by Mr. Piggott in Ref. 1.

Design by C. John Dakin

The DC-DC converter is necessary because the voltage output of the motor when used as a generator is much less than 12 V, the commonest battery voltage.

As shown by the circuit diagram in **Fig. 2**, the converter uses an inductor, L1, and a power MOSFET switch, T2. Each time T2 switches off, the current which has built up in L1 during the 180 μs T1 was on, is steered into the battery, B1, by D2. The current in L1 is sensed by R11, a 10-mΩ resistor, and two voltage comparators, IC1b and IC1c. When the input voltage, V_i, is 3 V, IC1b detects when the current rises to 10.4 A, and IC1c detects when it falls to 0.9 A. Both current levels are defined by the voltages from R1e, R3 and R4, and are proportional to V_i. The converter looks like a resistor, R_{in}, of 0.57 Ω to the generator. The outputs of IC1b and IC1c reset and set respectively the bistable formed by the two NAND gates IC2b and IC2c. The set

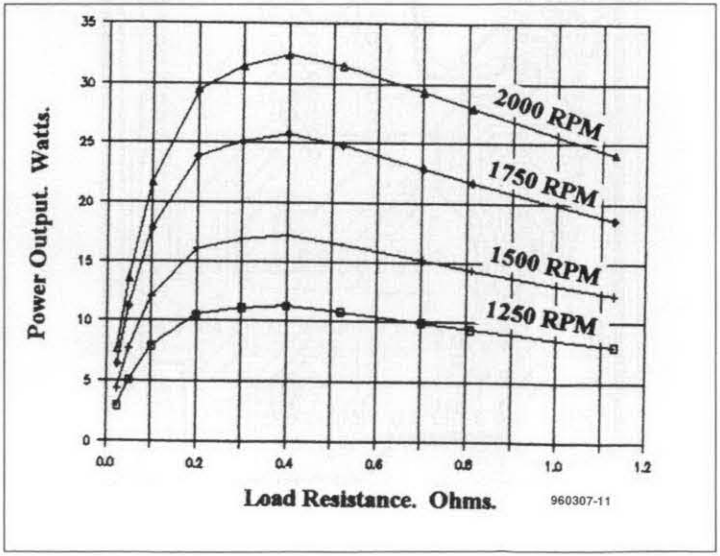


Fig. 1a. Typical 12V car radiator fan motor power output power.

pulse is via a third NAND gate IC2a, the second input to which is held high by IC1a, a third voltage comparator, as long as V_i is more than 2 V. Setting the bistable switches T1 on and the collector falls from +12 V to 0 V. T1's output drives the six inverters of IC3. IC3 drives the gate of T2, which has an input capacitance of 2 nF, from 0 V to +12 V in 2 µs.

When V_i is rising from 0 V to 2 V, IC1a's output stays low as pin 6 is above pin 7. IC1b's and IC1c's outputs stay high as there is no current through R11. The bistable is forced to the reset state by R5 and R6 holding pin 9 of IC2b low. When V_i reaches 2 V, the output of IC1a goes high, the bistable is set and the first operating cycle starts. Whenever V_i is less than 2 V, T1, IC3, C5 and D2 draw only leakage current from the +12 V rail.

The inductor in the circuit consists of 16 turns of 2-mm dia. enamelled copper wire wound on an ETD39 Ferroxcube core. A 0.6-mm air gap is put in the magnetic circuit of the core using pieces of cardboard or other non-magnetic material. Each end of the winding is connected to two pins of the former. See the PCB layout for the correct pins.

ZD1, a BZY93C16, 16-V, 20-W zener, should be fitted if B1 may be disconnected at any time. ZD1 will then limit the peak voltage at the drain of T2 to 17 V. ZD1 requires a suitable heatsink.

Figure 1a shows the power output of a typical car fan motor when used as a generator. The output is maximum with a load of about 0.4 Ω. This equals the output resistance of the generator, R_g. Because the converter losses increase as R_{in} decreases, R_{in} is set higher

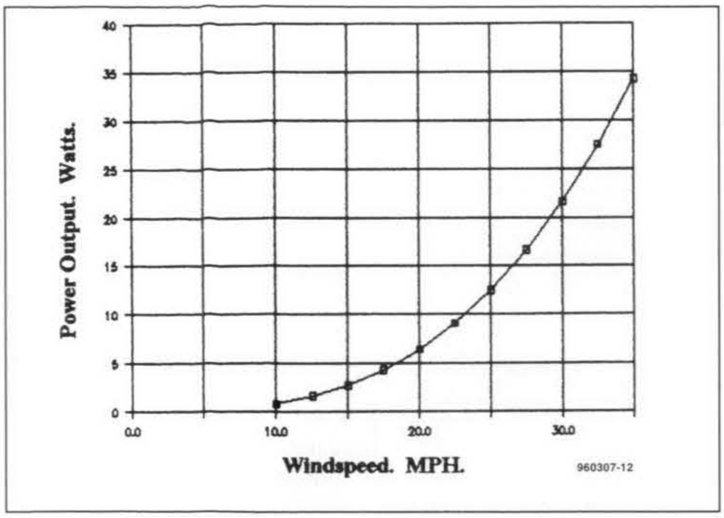


Fig. 1b. Power output of the combined generator and converter against wind speed.

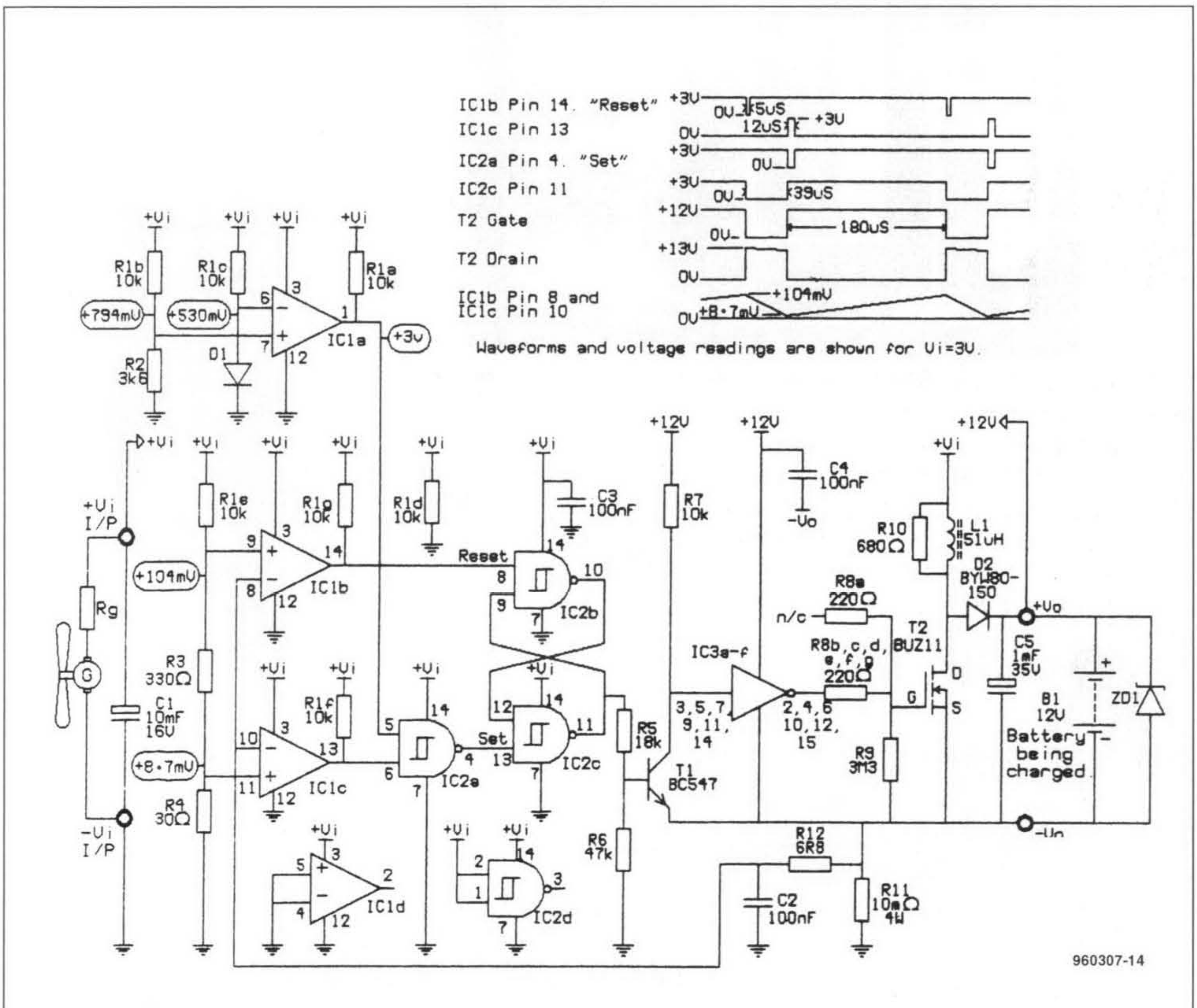


Fig. 2. Circuit diagram of the wind-powered battery charger.

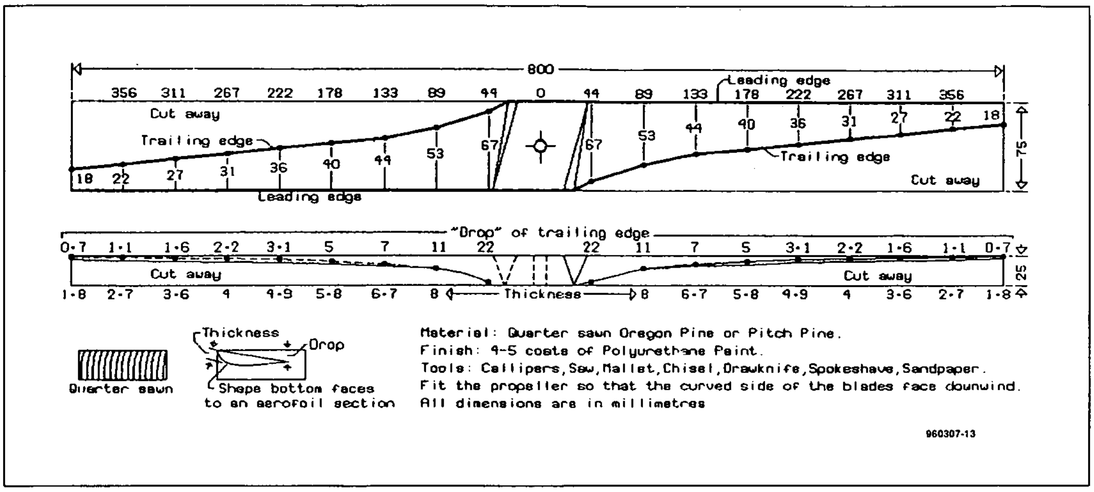


Fig. 3. Design of an 800-mm propeller suitable for a typical fan motor. The reader is recommended to read Mr. Piggott's excellent paper, Ref. 1, for full details of propeller design and construction.

than R_g for the best efficiency of the combined generator and converter. The resistance of the connecting cable between the generator and the converter must be kept as low as possible.

(950307-1)

References:

1. *Scrapyard Windmill Realities — Building Windmills with Recycled Parts* by Hugh Piggott. Published by The Centre for Alternative Technology, Machynlleth, Powys, Wales SY20 9AZ. Telephone: (01654) 702400.

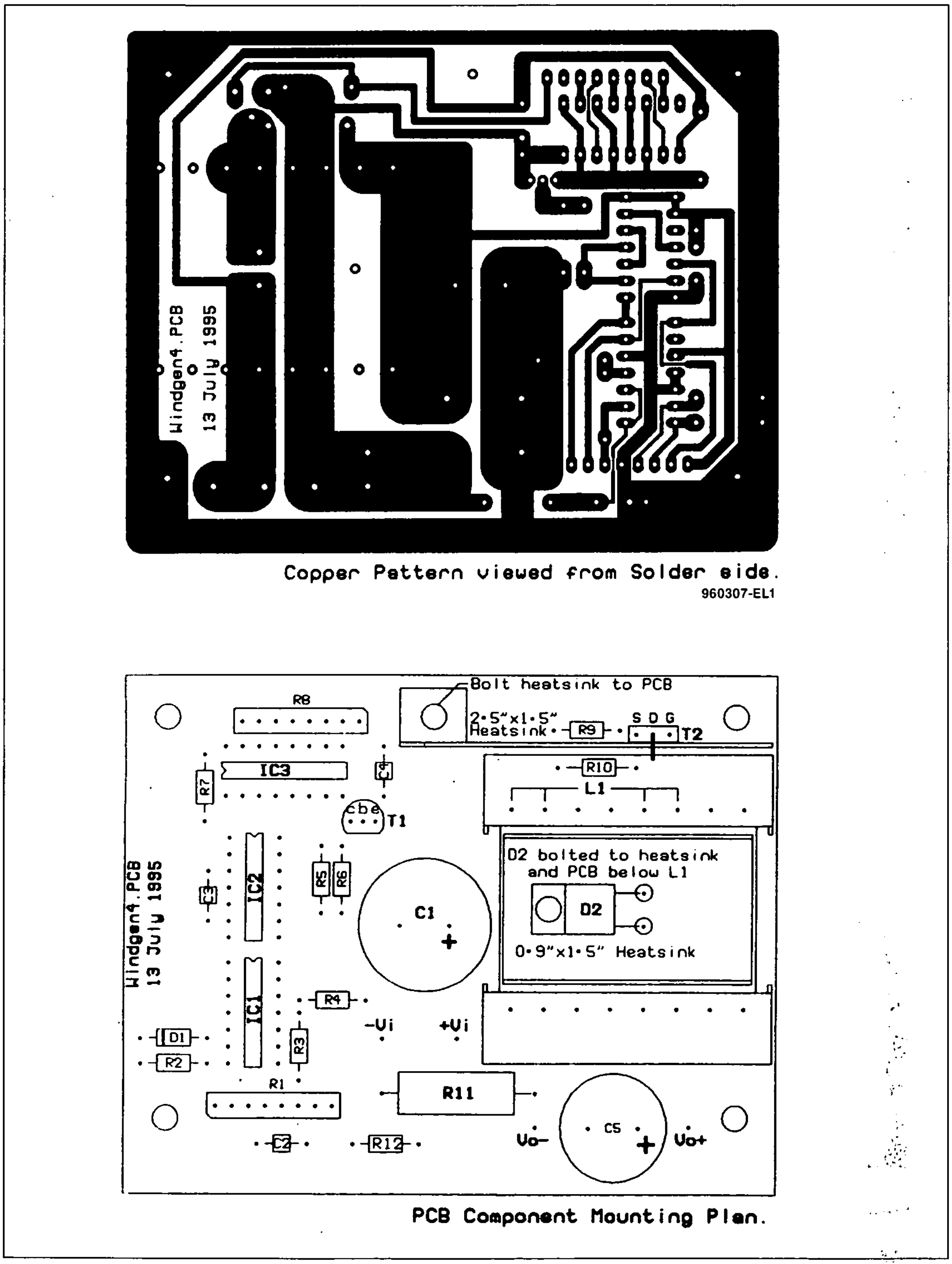


Fig. 4. PCB layout for the battery charger.

COMPONENTS LIST

Resistors:

R1a-g	10kΩ SIL array
R2	3kΩ6
R3	330Ω
R4	30Ω
R5	18kΩ
R6	47kΩ
R7	10kΩ
R8a-g	220Ω SIL array
R9	3MΩ3
R10	680Ω
R11	0.01Ω (Farnell 148-724)
R12	6Ω8

(all single resistors metal film)

Capacitors:

C1	10mF 16V
C2,C3,C4	100nF
C5	1mF 50V

Inductor:

L1 3C8 core, former, clip, ec wire 14SWG (2mm). Maplin order codes: JR81C, JR82D, JR83E, BL16S.

Semiconductors:

T1	BC547
T2	BUZ11
D1	1N4148
D2	BYW80-150
IC1	LM339
IC2	HCF4093
IC3	HCF4049
ZD1	BZY93C16

REMOTE MONITOR FOR CENTRAL HEATING SYSTEMS

2nd Prize (F)

WITH SECURITY ALARM

This circuit allows the proper functioning of different elements of a fuel burning central heating (CH) system to be monitored. An alphanumerical display is used at a convenient location to display useful data, while a buzzer sounds when a problem occurs with the CH system (burner switched to protection).

Design by Bernard Leclerc

In many houses, the central heating boiler/burner is mounted in the attic, or in another place which is not easily accessible. In case of a breakdown, or lack of fuel, you will not notice that there is a problem until the temperature starts to drop appreciably. The CH system monitor presented here uses a minimum of connections, yet enables you to check the current state of the heating system at any time.

The circuit is fitted at a discrete, but easily accessible, location within the normally inhabited space in the house. It will indicate the proper functioning of the various sub-units of the boiler, and will sound an audible alarm (by means of a buzzer) whenever a fault occurs (burner switched to safety mode).

The display indicates whether the CH system operates in standby-mode (overnight, or when no heating is required), or when the accelerator pump is on. It also indicates whether the burner is on, or waiting for 'cold' return water (i.e., having a temperature below the desired temperature), in which case it will switch on again. Each safety action which has to do with burner is immediately signalled by the display and a buzzer, by means of a pulsed sound.

The circuit may be modified to suit other applications, for instance, as regards the alphanumerical characters which appear on the display (edit the microcontroller ROM contents), or as regards the voltage levels at the inputs.

Hardware

Because the circuit can work from a.c. as well as d.c. voltage sources, there are few constraints as regards the power supply of the circuit. You may use either a mains transformer or a suitably rated mains adaptor. All inputs are electrically isolated by means of opto-isolators, of which the internal LEDs are powered via a resistor and a capacitor, which is discharged by a diode. The logic information supplied by the opto-isolators consists of active low levels, which are read by the con-

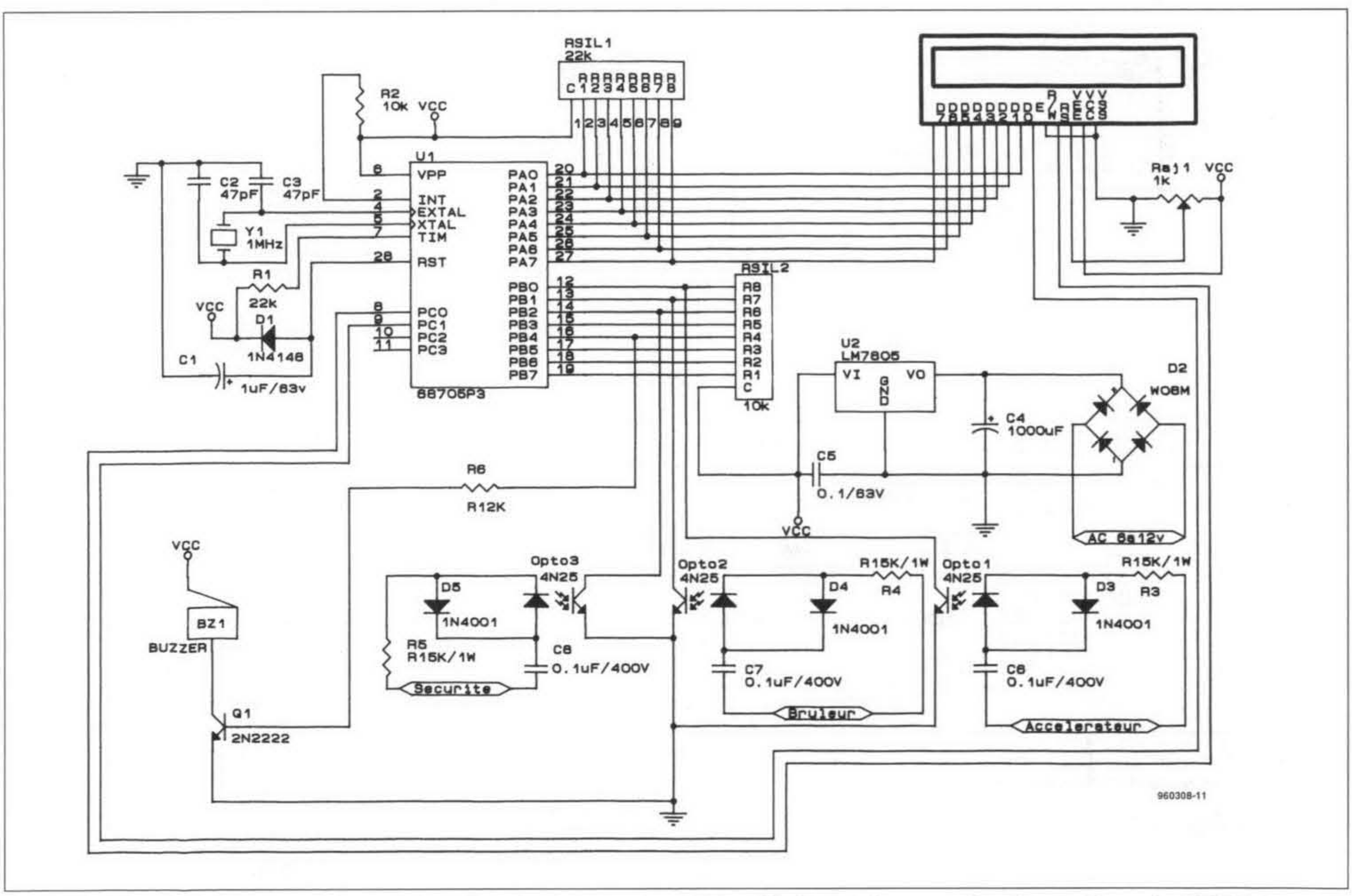


Fig. 1. The circuit of the central heating system monitor is considerably simplified by a microcontroller. Here, a Motorola 68705P3 is used. Translations: security = safety; bruleur = burner; accelerateur = accelerator.

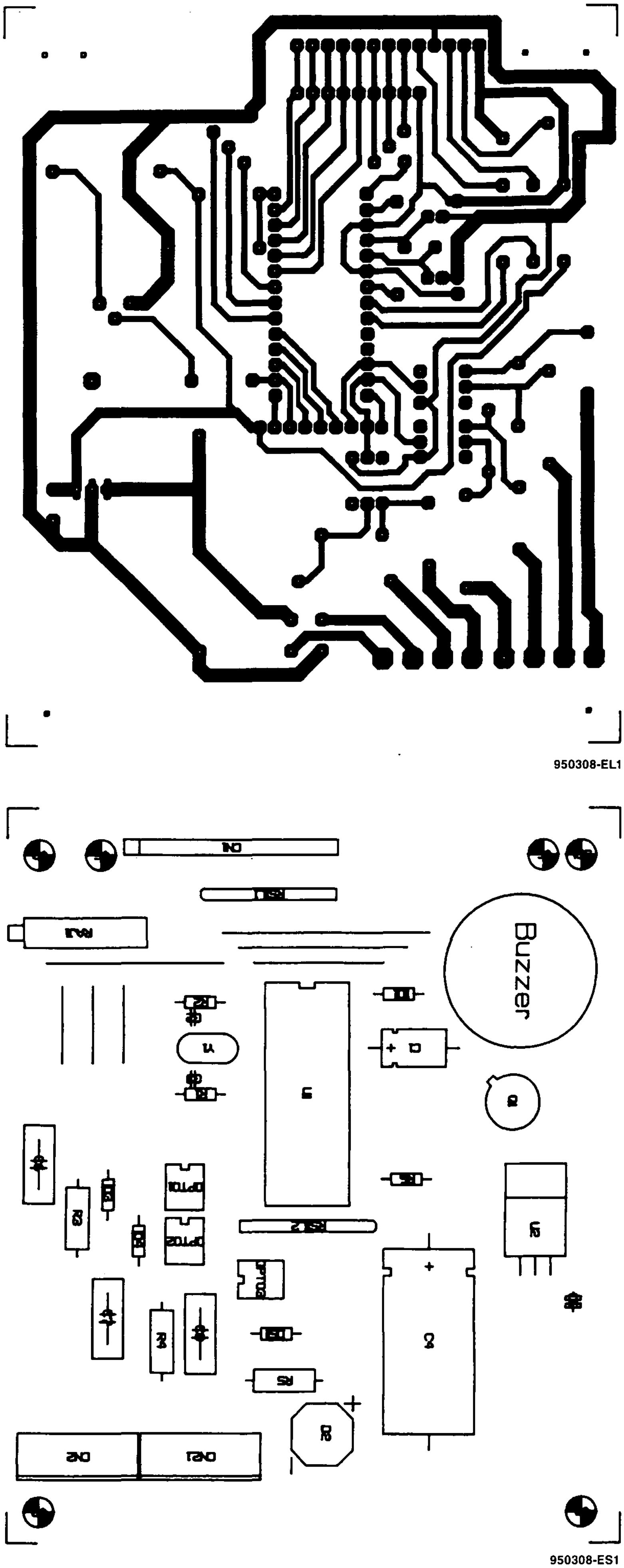


Fig. 2. Component mounting plan and track layout for the PCB designed for the central heating monitor.

COMPONENTS LIST

Resistors:
R1 = 8-way SIL array 22 kΩ
R2 = 8-way SIL array 10 kΩ
R3,R4,R5 = 15kΩ 1W
R6 = 12kΩ
Raj1 = 1kΩ preset

Capacitors:
C1 = 1µF 63V
C2,C3 = 47pF
C4 = 1000µF
C5 = 100nF 63V
C6-C8 = 100nF 400V

Semiconductors:
D1 = 1N4148
D2 = bridge rectifier
D3,D4,D5 = 1N4001
Q1 = 2N2222
Opto1,Opto2,Opto3 = 4N25
U1 = 68705P3 (programmed)*
U2 = LM7805

Miscellaneous:
Y1 = quartz crystal 1MHz
BZ1 = buzzer

* Programming files for this project available on disk, see page 70.

trol software.

The alarm output occupies one line of the other half of port B, split into inputs/outputs, and drives a transistor which supplies the required current for the buzzer. The other ports are programmed to output mode, and deliver the LC display signals: eight-bit data (Data, port A); data/command selection (port C); and data strobe (port C).

The contrast of the LCD module is adjusted by a preset (the multiturn cermet is not obligatory). The system clock is derived from a quartz crystal, Y1. Although the clock will also function if the crystal is replaced by a resistor or a wire link, the timing accuracy will drop unless you modify the MOR in software. The reset pulse is supplied automatically by capacitor C1 when the system is switched on. Diode D1 enables any voltage higher than the supply voltage to be shunted away into the power supply.

Printed circuit board

The circuit board is single-sided. It has only seven wire links, and accommodates all parts except the power transformer. That gives you a wide choice of power supplies which may be used with the circuit. Most holes are drilled at a diameter of 0.8 mm. Not so for the input connector, the voltage regulator, the smoothing capacitor and the buzzer, however, which require 1.5-mm dia. holes.

The connectors for the input information and the supply voltage are PCB mount screw-type terminal blocks for a reliable connection to the various cables. To enable it to be mounted higher than the other components, the display is connected via a couple of stacked turned-pin sockets. A pinheader is then carefully soldered directly to the LCD connections, and inserted into the top socket.

It is recommended to fasten the supply reservoir capacitor on the board by means of a nylon strap. The current consumption of the circuit is so low that a heatsink is not required on the voltage regulator.

Observe the polarity of the diodes and electrolytic capacitors, and make sure the motherboard/display assembly is sturdy.

```
S11B01009CA6FFB704A6F0B705A60FB7063F003F023F013F02A630B795
S11B011800AD6EA60CB700AD68A606B700AD623F101102A680CD01A1C9
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S11B0148AD3FA66EB700AD39A620B700AD33A656B700AD2DA665B70052
S11B0160AD27A669B700AD21A66CB700AD1BA66CB700AD15A665B7003D
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S11B02E002E2A6FFB7121A014A26FBB6121B014A26F25A26ED813F10A7
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S11B0340A620B700CD035FA64FB700CD035FA64BB700CD035FA621B7C5
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S11B037002A610CD0377814A26FD813F101102A680CD0418A601B70034
S11B0388CD04001002A620B700CD0400A642B700CD0400A672B700CD1C
S11B03A00400A675B700CD0400A66CB700CD0400A665B700CD0400A6C7
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S11B0490CD049D1B011302A610CD049D814A26FD81AE02CC04A6A6FF53
S11B04A8B7124A26FD1A01B6124A1B0126F25A26EDCC01A5202020560C
S11B04C06572733A312E312030372D393520422E4C45434C4552432040
S10904D82020202020205A
S1040784016F
S10507FE0100F4
S9030000FC
```

Fig. 4. Object code to be programmed into the 68705P3 controller.

Software

The control software consists basically of a classic I/O line handler and a section which sends characters to the LCD. The texts which appear are easily modified to suit personal requirements, allowing the circuit to be modified quite easily for any other application which requires system status and alarm messages.

Instructions to keep a watchdog asleep appear all over the program. Note, however, that no watchdog is implemented in this version of the hardware. That is because I had to limit myself to 30 components to meet the rules of the Competition.

The software starts by allocating the ports and their direction (I or O). Next, the memories are configured, and the ports are cleared. Then follows the display initialisation and the transmission of the first message. Next, routines are executed which define the permissible setup times of the various signals. Then comes an input line scanning operation in order of priority, followed by a five times over verification of the logic state which should be different from the 0 V belonging with the non-used half-cycle in the sinusoidal wave at the inputs. Return to the loop if nothing is detected, or jump to the relevant subroutine for the message to be written. The subroutine completed, always return to the main program (input reading), except for the audible alarm subroutine, which forms an endless loop.

Next comes the 'version' message, and then the copyright notice. At value $784, there is the programming byte of the chip: the MOR, followed by the rest of the control program.

Connections

The connection is made on the terminal strip of the control panel, where the thee 'signals' required for the monitor are tapped and sent to the remote monitoring unit by a suitably rated multicore cable.

The two screw terminals at the far right are connected to the supply voltage (between 6 and 15 V a.c. or d.c. at about 10 VA). The input voltage may be supplied by a transformer fitted inside the case, a mains adaptor, or it may be supplied by the boiler's internal power supply.

The two terminals at the far left should be connected to the panel strip in parallel with the burner motor.

The two remaining terminals are connected to the same panel, to the points marked 'fault', 'error' or similar.

For reasons of security (risk of shunting, or return currents via other terminals), it is best not to use a common wire. Instead, use two wires for each signal to be fed to the remote monitor.

Options

Obviously it is possible to modify the display messages using a simple editor; that is the reason which prompted me to equip various subroutines with this property.

The input voltages may be adapted to suit another application, simply by shorting out C6 and C8 if direct voltages are applied, or by changing resistors R3, R4 and R5 to limit the input current to 15 mA.

The Competition version of the circuit contains less than 30 components. For my own use, I made a version which is slightly more complex: it has four inputs and a watchdog. The fourth input is connected to the ignition transformer. These additions bring the number of parts to 38, which is more than allowed by the Competition rules.

Conclusion

Although the application of the circuit is neither dedicated nor restricted, the monitor is relatively inexpensive, based on easily found components, and easy to build. (950308)

SIMPLE STEPPER MOTOR CONTROLLER

2nd Prize (UK)

The main feature of the circuit is that it is very easy to construct. In addition, it has a very low price and is based on easily obtainable components. Suitable motors can be salvaged, for example, from old 5.25" floppy disk drives. The other components in my project may be found in just about any junk box. By contrast, special controller chips are often not so easy to obtain or are pretty costly.

Design by Sami Karhulahti

So this simple controller is the answer to this problem. The prototype circuit was used to control a small mirror attached to a motor spindle in a light effect unit.

The heart of the stepper motor controller is a GAL 16V8 chip, which contains the 8-state counter and combinatorial logic required to control the driver transistors. A timer chip (555) is required only to generate clock pulses and is not required if the controller is connected, for example, to a computer's I/O port. This is why the circuit can be adapted to many purposes where simple and cheap stepper motor controllers are needed.

The stepping speed can be adjusted by means of potentiometer P1 and changing the value of C1, while the direction of rotation or full/half step mode can be selected by small DIP switches S1 and S2. When S3 (ENA) is set to low, every output O5-O8 goes low so that the driver transistors all switch to their off state. The internal state counter can also be reset by pulling up the RES line with switch S4. In full-step mode, the motor torque is about 2 times higher than in half-step mode, though in the half-step mode the step resolution is two times better.

The step sequence can be reversed by setting the DIR-input high.

The binary output table

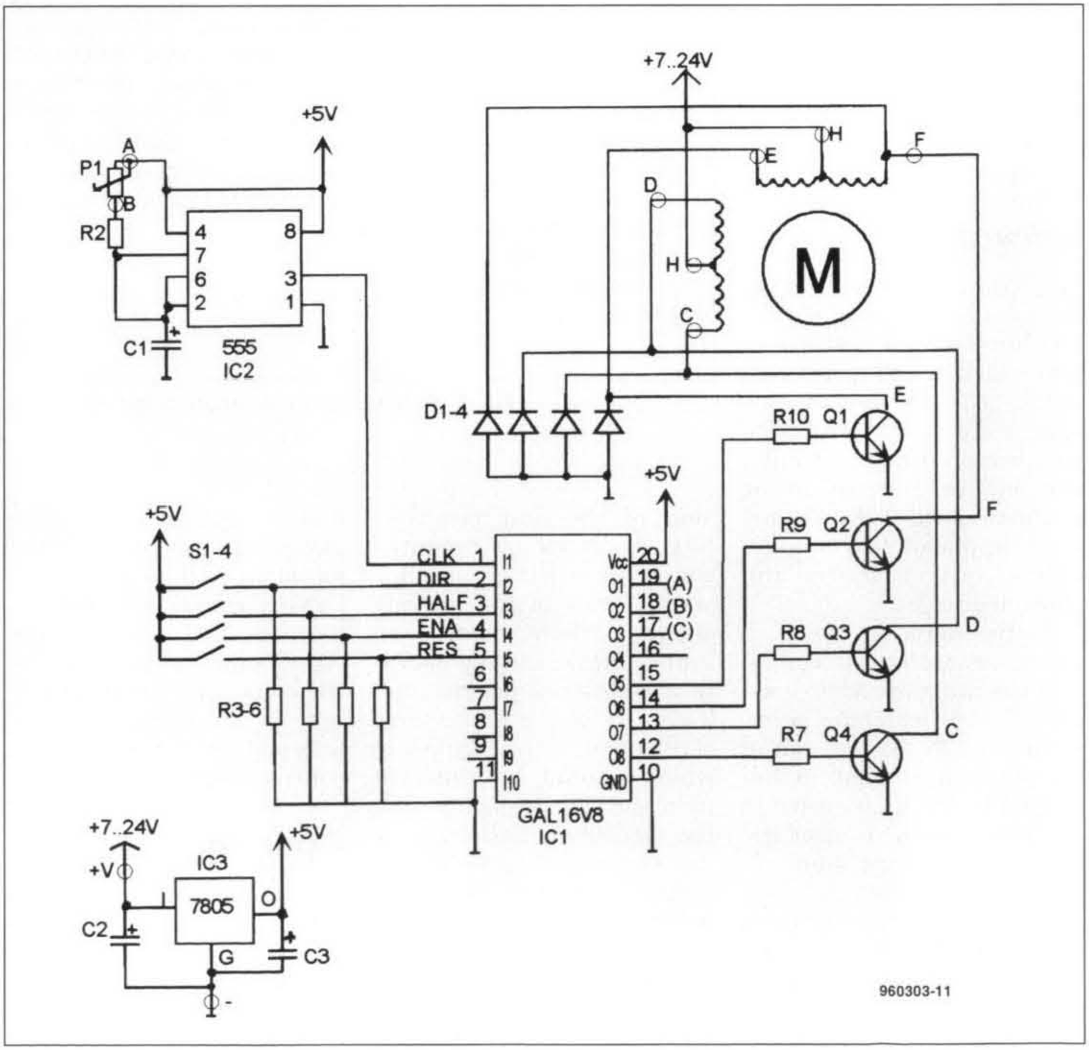


Fig. 1. Circuit diagram of the simple stepper motor controller.

Full-step (I3=L)				
Step	05	06	07	08
1	H	L	H	L
2	H	L	L	H
3	L	H	L	H
4	L	H	H	L
1	H	L	H	L
2	H	L	L	H
3	L	H	L	H
4	L	H	H	L
...				

Half-step (I3=H)				
Step	05	06	07	08
1	H	L	H	L
2	H	L	L	L
3	H	L	L	H
4	L	L	L	H
5	L	H	L	H
6	L	H	L	L
7	L	H	H	L
8	L	L	H	L
...				

(RES=L,ENA=H,DIR=L) is given in a separate box.

The circuit may be powered from a suitable 7-24 volt mains adaptor. Because the controller itself draws negligible current, the current consumption of the whole circuit depends mainly on the motor type selected. (950303)

COMPONENTS LIST

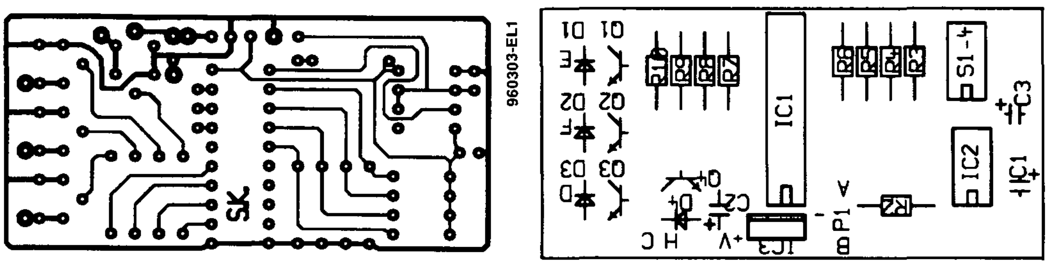
Resistors:
R2 = 1kΩ 0.25W
R3-6 = 4kΩ7 0.25W
R7-10 = 1kΩ 0.25W
P1 = 1MΩ lin/log potentiometer

Capacitors:
C1,C3 = 10µF 10V electrolytic cap.
C2 = 10µF 50V electrolytic cap.

Semiconductors:
IC1 = GAL16V8, programmed (stepper2.jed)*
IC2 = CA555
IC3 = 7805
Q1-4 = BC337
D1-4 = 1N4001

Miscellaneous:
S1-4 = 4-way DIP switch block
M = unipolar stepper motor 7-24V

* Programming files for this project available on disk, see page 70.




```
JEDEC-file generated by amiGAL-Assembler V1.0
(c)1992 by Johannes Schnell & Hans-Peter Dusel
;1912199403
;Unipolar StepperMotor Controller
;2
;16V8A
;19.12.1994
;Sami Karhulahti
;
;
;
*
G0*
QF2194*QP20*F0*
L0224 11101111111110111111111111111111*
L0384 01011101111110111111111111111111*
L0416 01101110111110111111111111111111*
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L1184 11100111011011111111111111111111*
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L1952 11101001011111111111111111111111*
L1984 11011010011111111111111111111111*
L2016 11110101011011111111111111111111*
L2048 11111111001100010011100100110001*
L2080 00110010001110010011010000110000*
L2112 00110011000111110000000100001111*
L2144 00111111000000001000011110000111*
L2176 100011111000111101*
C73FE*
0000
```

```
; Simple steppermotor controller
; Auth: Sami Karhulahti

chip stepper2 GAL16V8(A)

CLK DIR H_F ENA RES nc nc nc nc GND
/OE T4 T3 T2 T1 nc C B A VCC

equations

A := /A * /RES
B := DIR * A * B * /RES
     + DIR * /A * /B * /RES
     + /DIR * /A * B * /RES
     + /DIR * A * /B * /RES
C := DIR * /A * /B * /C * /RES
     + DIR * A * C * /RES
     + DIR * B * C * /RES
     + /DIR * /B * C * /RES
     + /DIR * /A * C * /RES
     + /DIR * A * B * /C * /RES
T1 = /A * H_F * ENA * /C
     + H_F * /B * ENA * /C
     + /H_F * /B * ENA
T1.oe = vcc

T2 = /A * H_F * ENA * C
     + H_F * /B * ENA * C
     + /H_F * B * ENA
T2.oe = vcc

T3 = /A * H_F * /B * ENA * /C
     + /A * /H_F * /B * ENA
     + A * /H_F * B * ENA
     + H_F * B * ENA * C
T3.oe = vcc

T4 = /A * H_F * /B * ENA * C
     + /A * /H_F * B * ENA
     + A * /H_F * /B * ENA
     + H_F * B * ENA * /C
T4.oe = vcc
```

TELLY-GUARD

1st Prize (F)

It is generally known that young children soon develop a habit of watching TV far too long. Although most parents would like to see them reading books or playing quietly, youngsters will spend hours on end in front of the telly if nothing is done about it.

Design by Robert Lacoste

The simple circuit presented here provides an original solution to the above educational problem. It allows you to 'give' a certain amount of TV viewing time to each youngster, who is free, in principle, to use up this time as he or she sees fit. After a short learning phase, you will notice (hopefully) that the children are developing much more intelligent viewing habits. Of course, the Telly-Guard may be used for any other application where electronic time allotment is required.

The principle

Each little rascal has a personal 'key' which 'contains' a certain number of time units. To be able to use the TV set, all he or she has to do is insert the key in a special reader, which then switches on the TV. The remaining time is indicated by an LED scale. When the end of the scale is reached, the time is up, and the TV is switched off without warning. You, the responsible parent, have a 'master key' which enables the user keys to be 'charged' with a certain number of time units. This master key also allows the rightful owner to watch as much TV as he/she likes!

Circuit description

The circuit diagram is very simple indeed, and based on an inexpensive microcontroller, the Motorola MC68705P3. The entire circuit contains only 30 components, including the reader/controller and one key.

A clean 5-V supply voltage is supplied by a voltage regulator consisting of T1, D1 and U1. The TV is switched on and off via a relay, K1, which is controlled via transistor T2. The use of a relay ensures a complete electrical isolation of the circuit from the mains.

The unit is operated by three push-buttons, SW1, SW2 and SW3. Four jumpers, JP1-JP4, allow different modes of operation to be selected, depending on how you would like the unit to function (see below under 'Practical use'). The 'remaining time' indicator is formed by an array of ten LEDs (D4). Don't worry, the meaning of the LED bar is easily learned and understood by children. The unit has two more LEDs. D5 indicates the on/off status of the TV set,

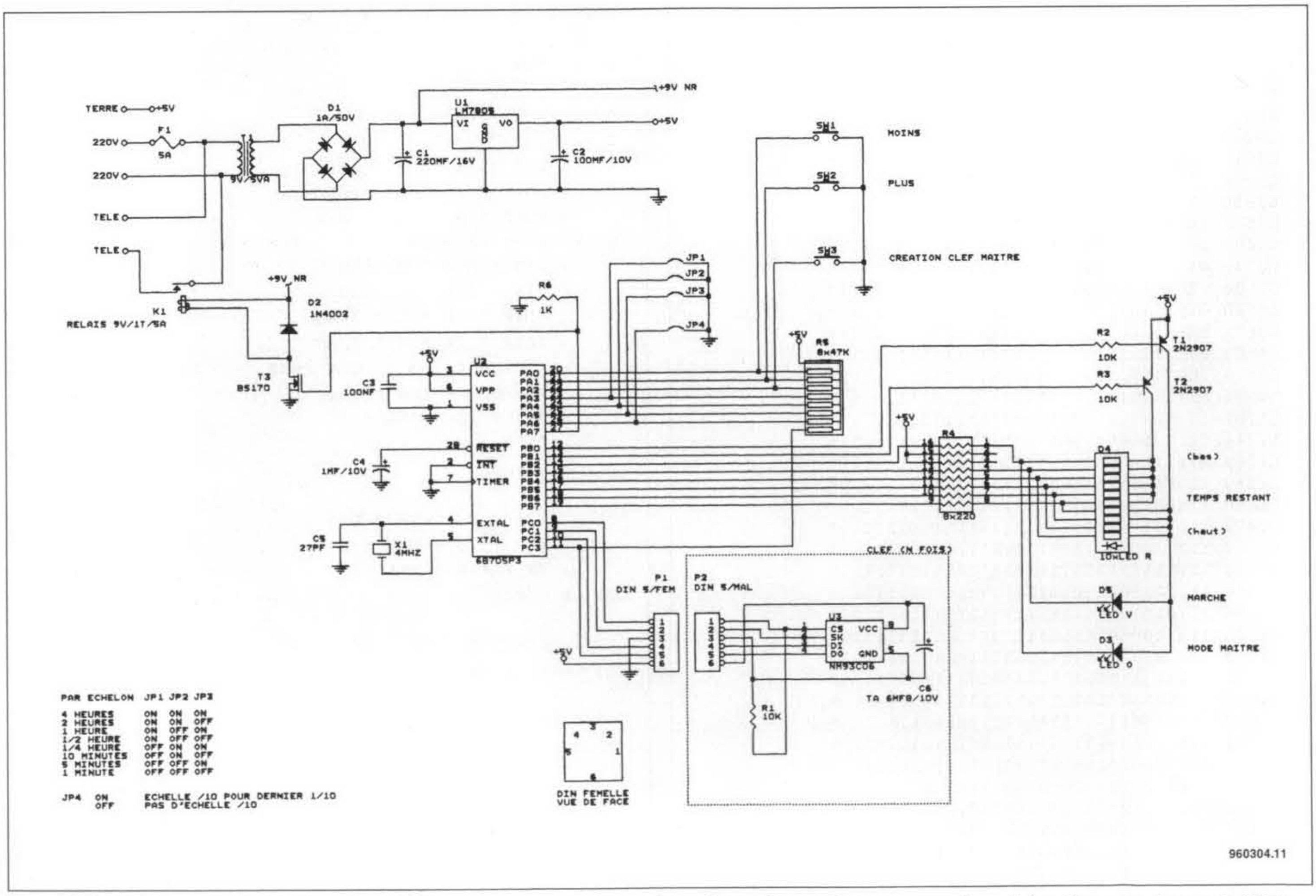

Fig. 1. Circuit diagram of the Telly-Guard. Translations: terre = earth; moins = down; plus = up; creation clef maitre = create master key; temps restant = remaining time; haut = high; bas = low; marche = on; mode maitre = master mode; clef (n fois) = key (n times).

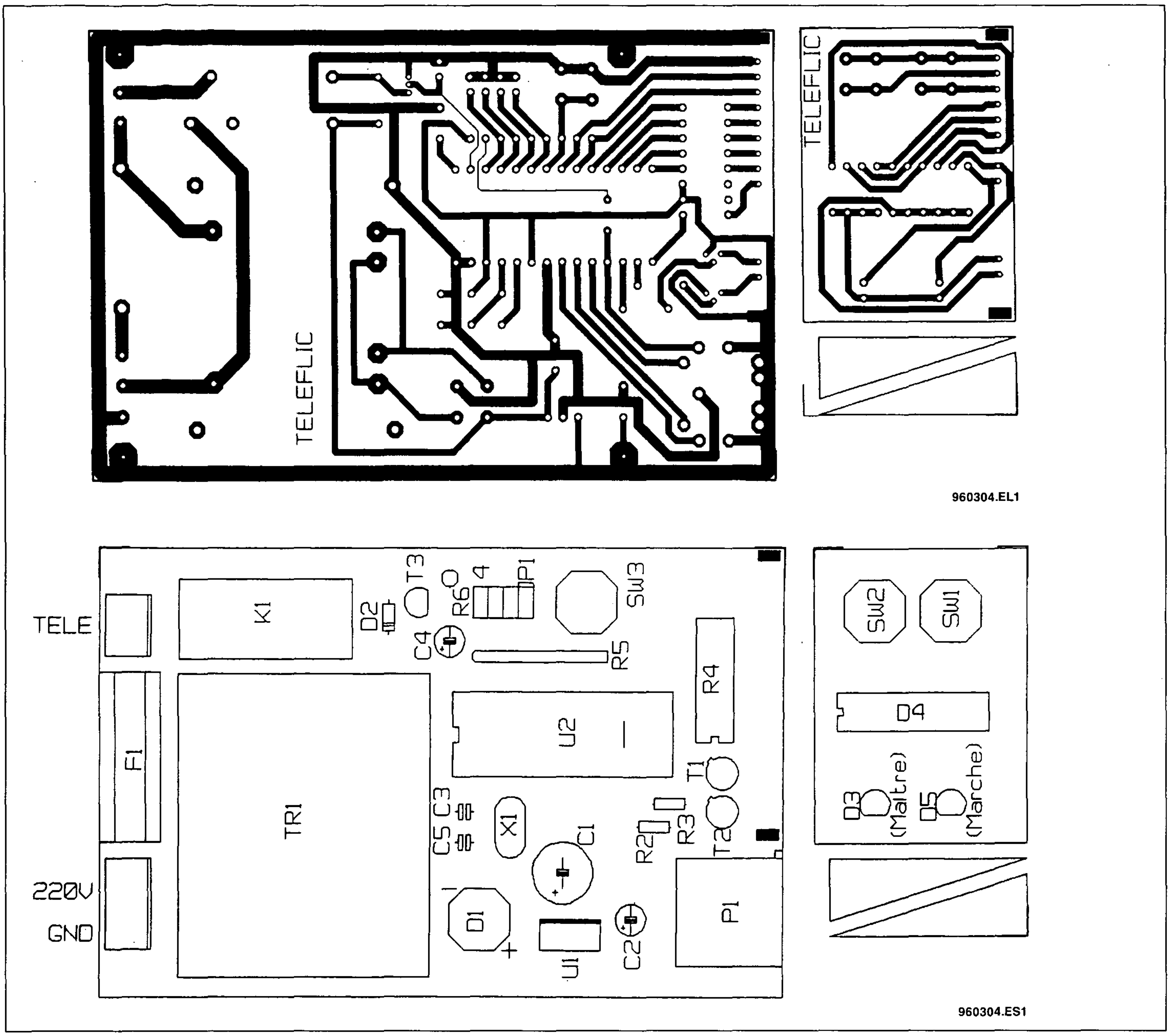

Fig. 2. Copper track layout and component mounting plan. Artwork produced with Layo1E.

while D3 lights when a key is inserted into the reader. In order to limit the number of input/output lines used for the LEDs, they are multiplexed under software control.

To limit the cost of the project, each key contains just one 'classic' EEPROM, a 93C06 256×16 bit type, and two passive parts.

Construction

The printed circuit board designed for the Telly-Guard is single-sided and has only one wire link. It consists of two sections, which should be fitted at an angle of 90°. The larger sub-board holds the main circuit and a hidden button, SW3. The smaller board contains front-panel elements SW1, SW2 and the LEDs. The construction with the two sub-boards allows the circuit to be fitted into a case with almost no wiring.

Start by fitting the wire link, the IC sockets, and then all other parts. Then connect the two boards via a few pieces of solid wire. Use a few drops of glue or epoxy potting compound to fix the boards in the case.

The construction of the personal keys requires some dexterity. The components that make up a key (U3, R1, C6) are soldered 'in the air' inside a 5-way DIN plug. Although this construction

COMPONENTS LIST

Resistors:
R1,R2,R3 = 10kΩ
R4 = 8-way DIL resistor array, 220Ω
R5 = 8-way SIL resistor array, 47kΩ
R6 = 1kΩ

Capacitors:
C1 = 220µF 16V
C2 = 100µF 10V
C3 = 100nF
C4 = 1µF 10V
C5 = 27pF
C6 = 6µF8 10V (tantalum)

Semiconductors:
T1,T2 = 2N2907
T3 = BS170
D1 = bridge 1A 50V
D2 = 1N4002
D3 = LED 5mm orange
D4 = 10-LED bar, red
D5 = LED, 5mm, green
U1 = LM7805
U2 = 68705P3 (programmed)*
U3 = NM93C06

Miscellaneous:
TR1 = mains transformer 9V 5VA.
X1 = quartz crystal 4MHz.
K1 = relay 9V 5A, 1 make contact, 350-V rated.
SW1,SW2,SW3 = PCB mount push button.
F1 = fuse 5 A.
P1 = 5-way DIN socket, 45°, PCB mount.
P2 = 5-way DIN socket, 45°.
JP1-JP4 = 2.54mm pitch jumper

* Programming files for this project available on disk, see page 70.

JP1	JP2	JP2	Unit (h/min)	Total time
X	X	X	4 hours	40 hours
X	X	-	2 hours	20 hours
X	-	X	1 hour	10 hours
X	-	-	30 minutes	5 hours
-	X	X	15 minutes	2 hours 30 min.
-	X	-	10 minutes	1 hour 40 min.
-	-	X	5 minutes	50 minutes
-	-	-	1 minute	10 minutes

is not difficult, it does require accuracy and a little patience. Pay attention to proper isolation between the parts and the metal screening of the plug (which is connected to +5 V).

As with all mains-powered circuits, precautions should be taken to ensure electrical safety. In particular, the circuit must be earthed, so that it remains safe if the transformer or the relay breaks down. This precaution should always be observed, unless you are dealing with a double-isolated device, which is difficult to produce by a hobbyist. Here, the earthing is achieved by connecting the +5 V line to the earth pin of the mains plug. Although the mains voltage is only present at some points at the rear side of the PCB, you must always pull the mains plug before doing any work on the circuit.

Practical use

Fit jumpers JP1, JP2 and JP3 before you switch on the circuit. These jumpers set the length of a time unit. The total number of time units which can be charged is ten. The available options are shown in a separate box.

Jumper JP4, if fitted, gives a 'magnifying' effect during the last time unit. When the available time has dropped to one tenth of the total time, the LED scale is 'magnified' by ten, and the display starts to flash. This function is disabled when JP4 is not fitted. Your choice!

The circuit is adjustment-free. After taking it into use for the first time, you should start by making the 'master key'. This done by inserting a blank key, and then pressing the 'hidden' push-button, SW3. A user key is made as follows: insert a blank key, press SW3, and then SW1 ('down'). This produces a fully charged user key. If you leave this key inserted in the reader, the system starts to count down the time units until the load is switched off.

To charge a user key, first insert the master key (D3 lights), remove it, an then the user key. Next, adjust the number of time units to be given by means of push-buttons SW1 and SW2. Other keys are charged in the same way. The reader switches to normal mode automatically if there is no push-button activity within 10 seconds.

Although the construction and use of the Telly-Guard should be within reach of most of you, getting children to accept the principle of limited TV viewing time may present some fierce problems initially. (960304)

Note: the software mentioned in this article is available on floppy disk, see page 70.

```
S1110100A680B704A6FFB705A6F7B706A600AB
S111010EB712B713B714B716B717B718B71947
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S111012AA650B720A614B722A6FFB721A662DE
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S111026502EFCD02CDCC02393D18270DA600C4
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S111027F0239A6EECD0351811E00A601B7136D
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S11102A9A600B71E811F00A600B713811E0019
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S11102C50AB71FA600B71E81A605B71FA60024
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S11104133D172734A1652504A601205AA151E6
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S111043D203AA1012504A6F92032A6FD202EA6
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S10407840769
S10907F804F501000100FC
S10507FE0100F4
S9030000FC
```

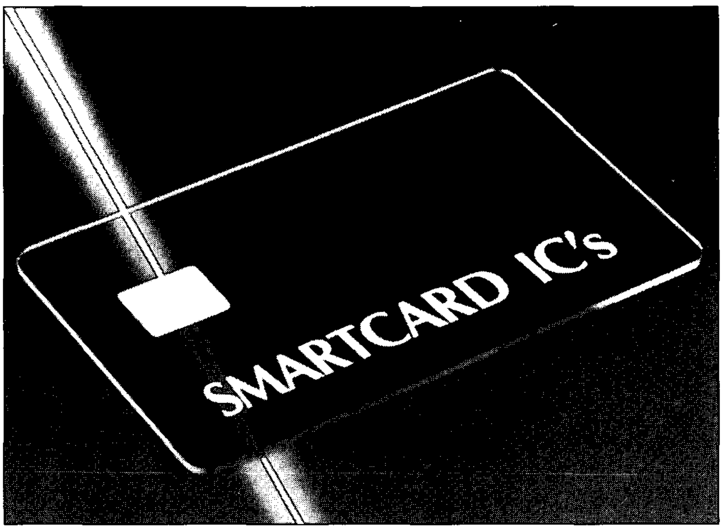
Fig. 4. Object code to be loaded into the microcontroller.

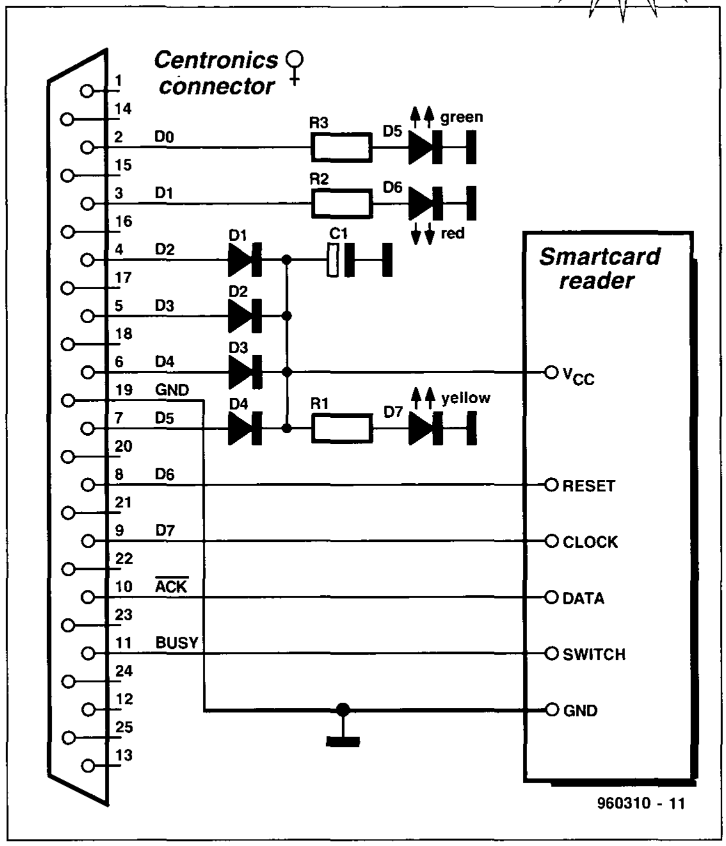
SMARTCARD READER

1st Prize (NL)

This design answers the widespread interest in applications involving smartcards. Chip-type telephone cards and credit cards catch the fancy of many. Those of you thinking of fraud at this point need not read any further, because that is not possible with this design. The circuit is, however, suitable for many other interesting applications, so don't throw away those expired telephone cards!

Design by P.H. Baars



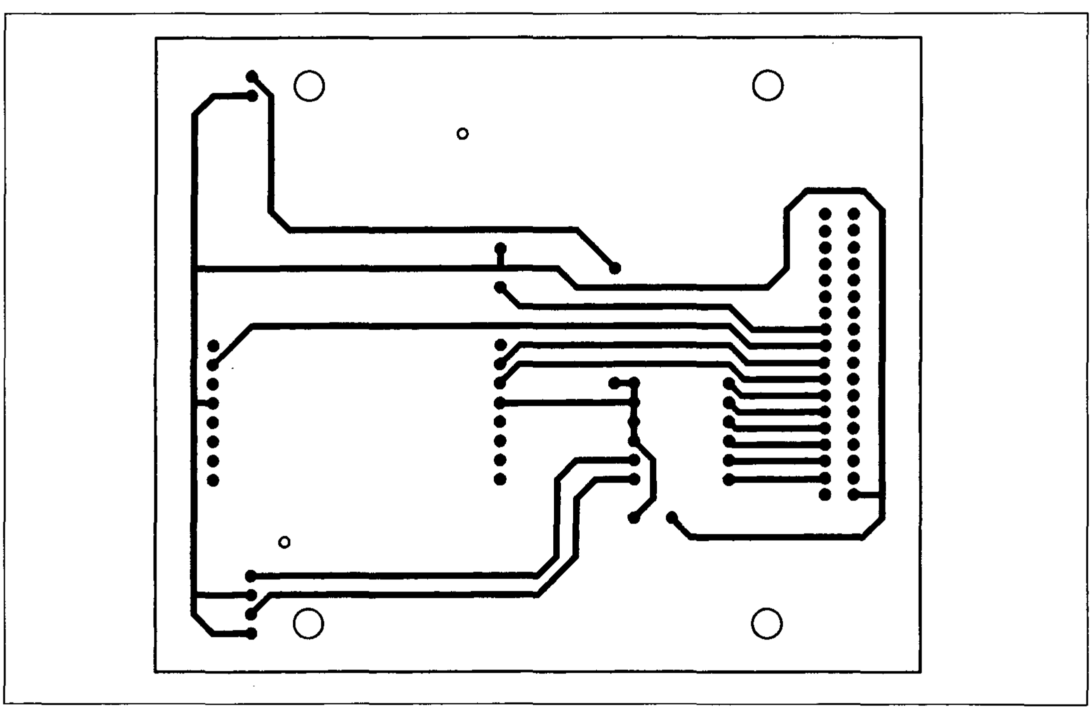


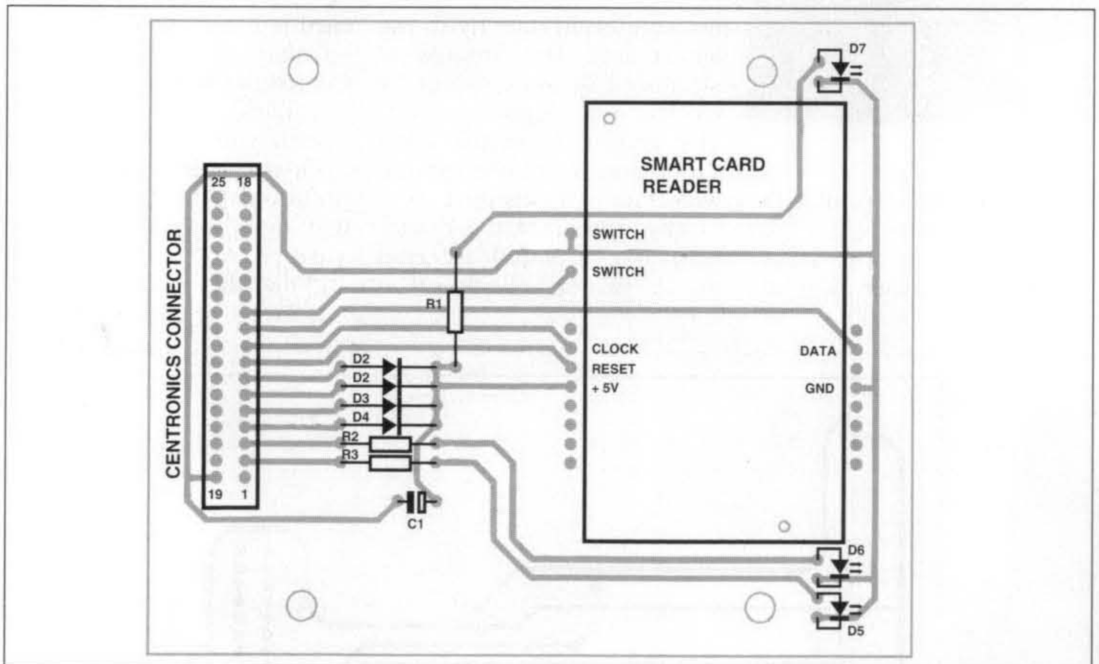
One application of the smartcard reader could be access protection to a program you have written yourself. This means that any user has to insert an authorized smartcard before he or she is allowed to use the program. Similarly, access checking and logging is within easy reach. Only a handful of parts are needed for experiments at home. The present design allows, for instance, telephone chip-cards to be read. The information read from such cards consists of the serial number, production date/month, and the remaining value.

The circuit diagram is so simple that a description is really superfluous. An external power supply is not needed because the supply voltage is stolen from the parallel port. Diodes D1 through D4 serve to prevent short-circuits between the databits. Databit 0 controls the green LED, databit 1 the red LED, and the yellow LED is connected to the power supply. The other databits are connected directly to the smartcard. The voltage is stabilized to some extent by electrolytic capacitor C1. The smartcard connections Clock and Reset are inputs, wile Data is an output.

The smartcard reader unit has a small internal switch which checks if a card is inserted. This switch is also connected to the Centronics port.

Having built the small board, you may check if it work with the aid of the test program (test.exe). If this test is passed, try 'cardtest.exe', which reads and decodes the ATR string.





COMPONENTS LIST

R1,R2,R3 = 1kΩ5
D1-D4 = 1N4148
C1 = 10µF 16V radial
LED1 = 3mm dia., yellow
LED2 = 3mm dia., red
LED3 = 3mm dia., green
Con1 = Centronics socket, PCB mount, angled pins.
Con2 = Smartcard reader unit. Available from eMedia GmbH, Postfach 610106, D-30601 Hannover, Germany. Price DM 12.

The program is relatively simple. There are various routines for the basic functions (LED on/off, clock high/low, etc.). The main program first checks if a card is inserted ('switch'). If so, data are read using the ATR (see Ref. 1), and checked. If this information is okay, it is converted into legible text.

The routine 'my_card' contains the registration number of one of my own telephone cards. The number may be replaced with your own number. The green LED will light when this number matches that on the card. If the numbers are different, the red LED lights.

The program is only intended as a starting point for further experiments, you can make it as intelligent and attractive as you like.

(960310)

Note: the software mentioned in this article is available on floppy disk, see page 70.

Reference:

1. Chip Cards, *Elektor Electronics* April 1995.

N·E·X·T M·O·N·T·H

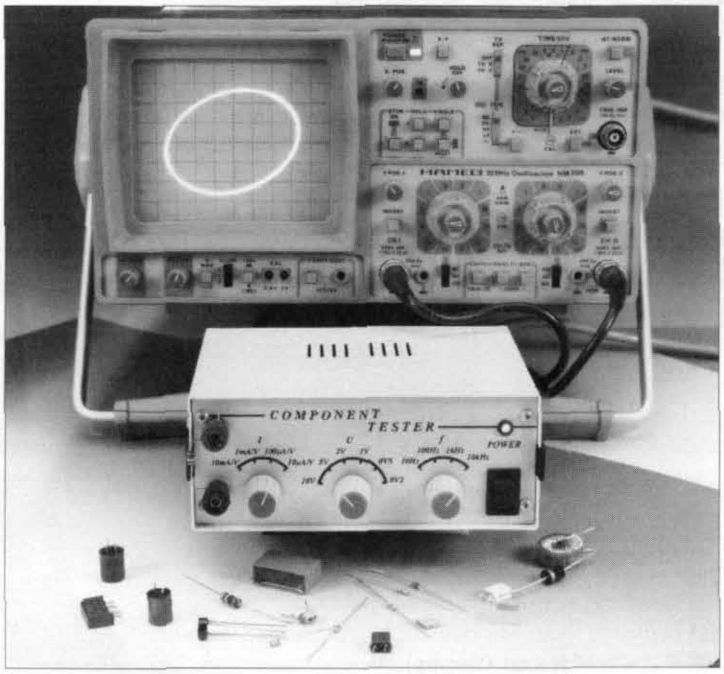
another 16-page section of Elektor Electronics devoted to prize-winning entries from our International Circuit Design Competition 1995.
A selection from the subjects:

- » Microcontroller Switching Clock RTC56
- » PC-Driven Battery Tester
- » 'Green power' for PCs
- » Hybrid Headphones Amplifier
- » Intelligent Motor Control for R/C Models
- » PWM Signal Generator

Don't miss the February 1996 issue!

PASSIVE-COMPONENT TESTER

(FOR USE WITH AN OSCILLOSCOPE)



When testing electronic components, it is not always necessary to gather detailed data on all the properties of a component. Often, gleaning a few facts yields enough information. The tester described quickly gives the user a good idea of various properties of a component on the screen of an oscilloscope.

From an idea by R. Veltkamp

There is a plethora of component testers on the market. Most of these are far too expensive for the average hobbyist or small business. The cost of the present tester is low enough to present no problems to a small budget. It does, however, require an oscilloscope.

Components may be divided into passive and active types. Active ones comprise, for instance, transistors, diodes, opamps. Resistors, capacitors, and inductors, to name but a few, are passive types. The tester is particularly suitable for testing passive components. As far as diodes and transistors are concerned, it can check the p-n junction; for more detailed tests, special test gear is needed.

The technology used is simple: a sinusoidal voltage is applied to the component to be tested (c.o.t.) and the consequent current flowing through the c.o.t. is measured. The applied voltage and resulting current are applied to the *x*-*y* terminals of an oscilloscope (voltage to *x*, current to *y*), which gives a good indication of the state of the c.o.t. In ideal resistors, voltage and current are in phase; in ideal capacitors and inductors, they are shifted 90° with respect to one another. The more the c.o.t. differs from the ideal, the more the phase relationship between voltage and current will differ from the ideal values.

Circuit description

The block diagram of the tester is shown in **Fig. 1**. The test voltage, provided by a discrete sine wave generator, is buffered by an amplifier and then applied to the c.o.t. via test resistor R_M. The voltage drop across the c.o.t. is buffered by a second stage, after which it is applied to the *x*-input of the oscilloscope.

The potential across R_M is a measure of the current flowing through the c.o.t. Moreover, its phase with respect to that of the voltage at the *x* input is the phase angle between voltage and current. This is why an amplifier is used to measure the potential difference across R_M. This voltage is applied to the *y*-input.

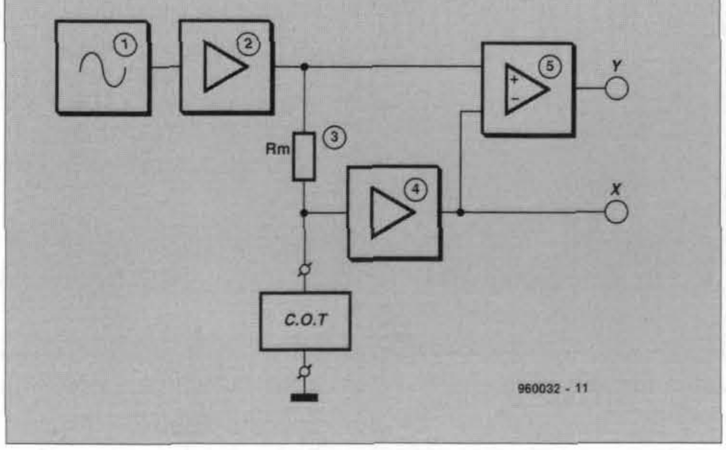


Fig. 1. Block schematic of the passive-component tester. The various blocks remain compact in the actual design.

In **Fig. 2**, the sine wave generator is formed by Wien bridge oscillator IC_1, whose output frequency can be set to 10 Hz, 100 Hz, 1 kHz or 10 kHz with switch S_1. The oscillator is stabilized by T_1, a JFET Type BF256A (it MUST be an A version). When S_1 is set to a different position to alter the frequency, its 'c' section selects a different value capacitor in the stabilizing stage. At the lowest frequency, a 1 µF capacitor is used; at the highest frequency, a 1 nF type.

The output voltage of the generator is applied to power operational amplifier (op amp) IC_2, which provides the current required by the c.o.t. The level of the output voltage depends on the setting of S_2 as shown in Fig. 2.

The generator needs to be calibrated (with P_1), since the properties of two BF256As can be very dissimilar, which may cause an appreciable spread of the output levels.

The component to be tested is connected to terminals c.o.t. (component on test). The voltage drop across the c.o.t. during the test is applied to voltage follower IC_{3a} via R_{26}. Diodes D_4 and D_5 protect the non-inverting input of the op amp against too high voltages. The output voltage of IC_{3a} is applied to the *x*-input of the oscilloscope via R_{27}, which protects the input against short-circuits.

The current through the c.o.t. is determined from the voltage drop across the relevant resistor selected with S_3 from R_{23}–R_{25}, which is measured by IC_{3b}. Note that therefore the sensitivity of the tester is set with S_3.

The output potential of IC_2 is applied to the non-inverting input of op amp IC_{3b}, while the output signal of IC_{3a} (which corresponds to the voltage at the other terminal of the selected resistor) is applied to the inverting input.

The power supply for the tester is straightforward. The voltages at the secondaries of the mains transformer are converted into a symmetrical direct voltage of ±20 V. Regulators IC_4 and IC_5 provide a stable direct voltage of ±15 V. 'Mains on' is indicated by D_{10}.

Construction

The tester can be built quickly and without undue difficulties on the printed-circuit board in **Fig. 3**. Before any assembly work is done, however, the power supply section must be cut off the mother board.

With component values as specified, IC_4 and IC_5 do not need a heat sink, but IC_2 does.

Set the required number of positions of S_2 (6) and S_3 (4) with the stop ring provided with these switches before fitting the switches on to the board.

When the board has been finished, check all soldering carefully and make sure that there are no short-circuits on the tracks. For the time being, set P_1 to the centre of its travel.

A possible front panel layout is shown in **Fig. 4**.

Fit the mother board behind the front panel with the aid of four 50 mm long M3 screws, nuts and washers, and 40 mm long spacers. This gives sufficient space to fit the on/off switch. Mount the BNC sockets for the *x*- and *y*-outputs at the back of the enclosure. Fit the spring-loaded terminals for connecting the c.o.t. at the front panel. It is advisable to use a mains entry with integral fuse holder.

Calibration

Connect an oscilloscope to K_1, set switch S_2 to position 10 V and adjust P_1 to obtain an output of 10 V (peak) on the scope. The tester is then ready for operational use.

Parts list

Resistors:

R_1, R_8 = 715 Ω, 1%

R_2, R_7 = 7.15 kΩ, 1%

R_3, R_6 = 71.5 kΩ, 1%

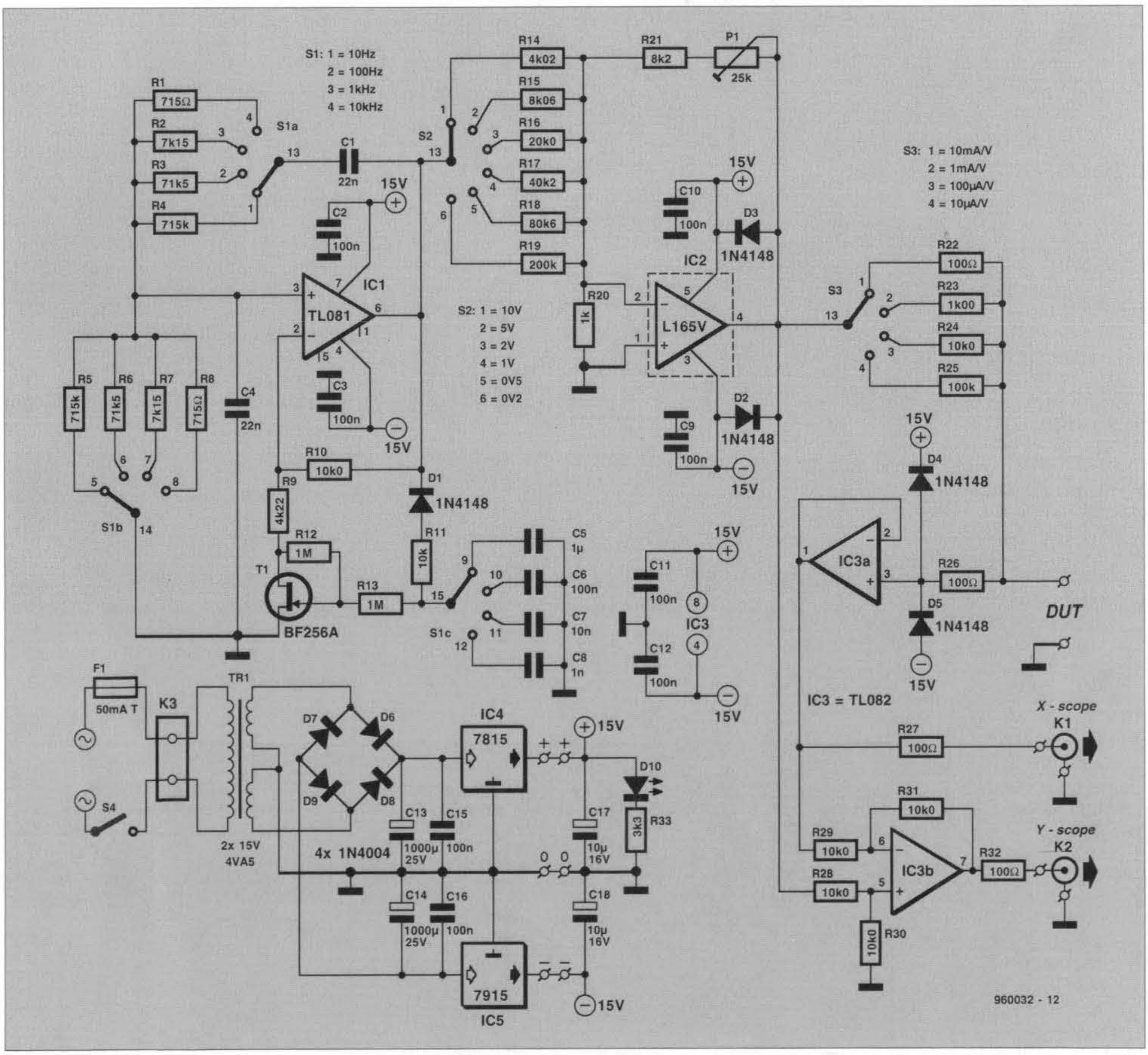


Fig. 2. The circuit uses easily obtainable components.

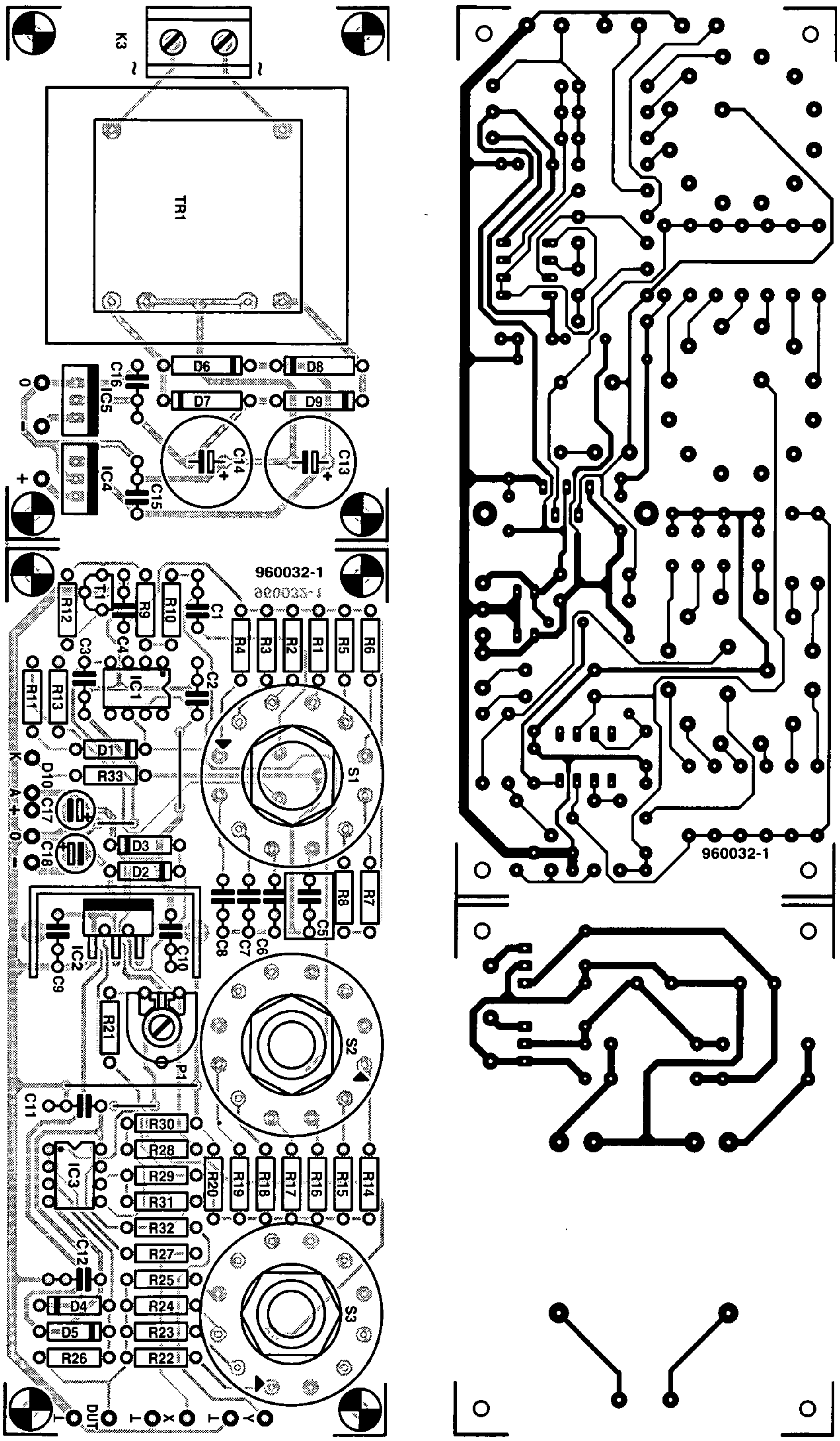


Fig. 3. Printed-circuit board for the passive-component tester.

R_4, R_5 = 715 kΩ, 1%
R_9 = 4.22 kΩ, 1%
R_{10}, R_{24}, R_{28}–R_{31} = 10.0 kΩ, 1%
R_{11} = 10 kΩ
R_{12}, R_{13} = 1 MΩ
R_{14} = 4.02 kΩ, 1%
R_{15} = 8.06 kΩ, 1%
R_{16} = 20.0 kΩ, 1%
R_{17} = 40.2 kΩ, 1%
R_{18} = 80.6 kΩ, 1%
R_{19} = 200 kΩ, 1%
R_{20} = 1 kΩ
R_{21} = 8.2 kΩ
R_{22} = 100 Ω, 1%
R_{26}, R_{27}, R_{32} = 100 Ω
R_{23} = 1.00 kΩ, 1%
R_{25} = 100 kΩ, 1%
R_{33} = 3.3 kΩ
P_1 = 25 kΩ preset

Capacitors:
C_1, C_4 = 22 nF, 5%, metallized polypropylene
C_2, C_3, C_9–C_{12}, C_{15}, C_{16} = 100 nF, high-stability
C_5 = 1 µF, metallized polypropylene
C_6 = 100 nF, metallized polypropylene
C_7 = 10 nF, metallized polypropylene
C_8 = 1 nF, metallized polypropylene
C_{13}, C_{14} = 1000 µF, 25 V, radial
C_{17}, C_{18} = 10 µF, 16 V, radial

Semiconductors:
D_1–D_5 = 1N4148
D_6–D_9 = 1N4001
D_{10} = LED, red, high efficiency
T_1 = BF256A

Integrated Circuits:
IC_1 = TL081
IC_2 = L165V
IC_3 = TL082
IC_4 = 7815
IC_5 = 7915

Miscellaneous:
K_1, K_2 = BNC socket
K_3 = 2-way terminal strip, pitch 7.5 mm
S_1 = rotary switch, 3-pole, 4-position
S_2, S_3 = rotary switch, 1-pole, 12-position (see text)
S_4 = mains on/off switch
Tr_1 = mains transformer, two secon-

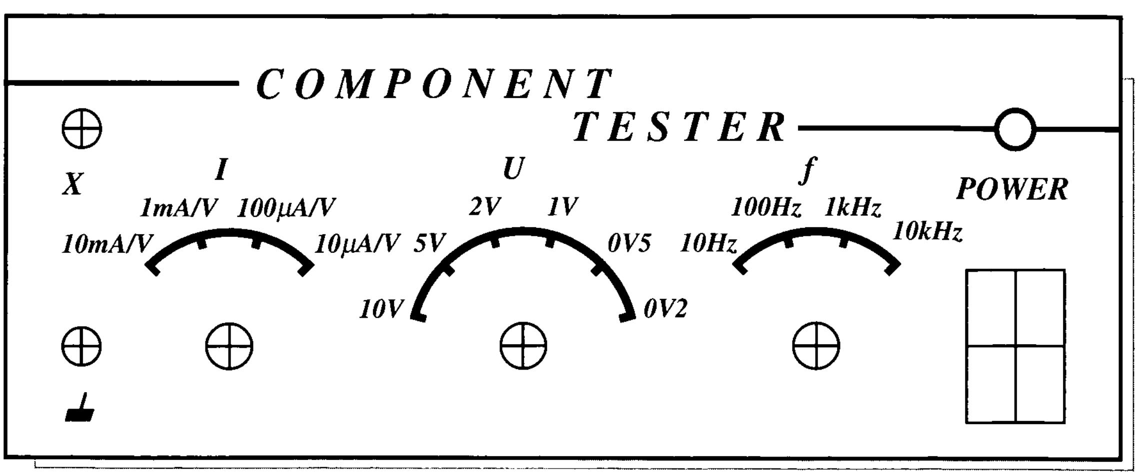


Fig. 4. Suggested front pane;l for the passive-component tester.

Measuring with Lissajous figures

The measurement technology used depends on Lissajous figures. These are plane curves formed by the composition of two sinusoidal waveforms in perpendicular directions, that is, they form a coordinate x-y system. In such a system, the displacement of a point is determined by the vector sum of the x and y values.

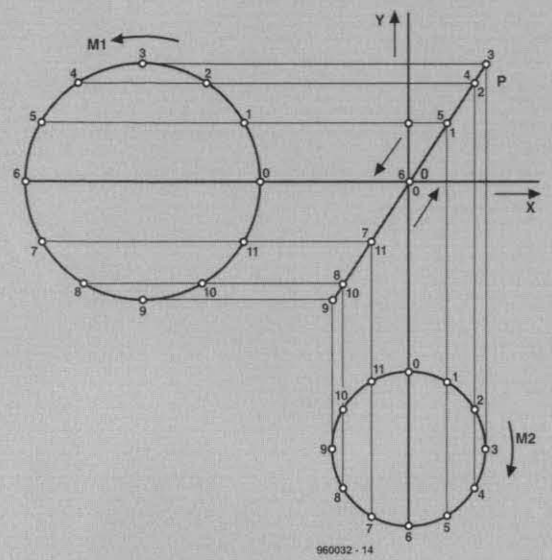


Figure A1 shows how such a figure is obtained. Here, P is the pixel projected on to the screen of an oscilloscope by the electron beam; M_1 is the vertical (y) deflection and M_2 is the horizontal (x) deflection.

In the component tester, the frequencies at which the vector rotates in the circles are identical, since they are derived from the same signal. The diameter of the circles is a measure of the peak levels of the signals.

In Fig. A1 it is assumed that the phases of the two signals are identical, which is the case when the component on test is a pure resistance. The resultant of the two functions is a diagonal line. Since the voltage is represented by the x-axis and the current by the y-axis, the value of the resistance is calculated by summing the x- and y-values.

When the test signal is applied to a pure capacitance or pure inductance, there is a phase shift of 90°. The sinusoidal voltage is coordinated with a cosinusoidal current that is +90° out of phase w.r.t. the voltage in the case of a pure inductance and –90° in case of a pure capacitance. In these cases, the cartesian equations are:

$x = a \sin(\omega t)$

and

$y = b \cos(\omega t)$.

The resultant is:

$x^2 + y^2 = R^2$.

Since

$\sin^2(\omega t) + \cos^2(\omega t) = 1$,

this may be written as:

$[a \sin(\omega t)]^2/a^2 + [b \cos(\omega t)]^2/b^2 = 1$,

from which may be derived:

$x^2/a^2 + y^2/b^2 = 1$.

This corresponds to an ellipse. When $a = b$, that is, when the impedance is a pure reactance, the ellipse becomes a circle.

The ellipse is composed of:

$x(\omega t) = U_1 \sin(\omega t)$

and

$y(\omega t) = U_2 \sin(\omega t + p)$,

where p is the phase shift, whose value is determined by

$\sin^{-1}(y_{(\omega t=0)})/(y_{max})$,

where $y_{(\omega t=0)}$ is the intersection of the ellipse with the y-axis.

Figure A2 shows an example of an ellipse and indicates at which two points the measured values are found. Impedance Z of the c.o.t. is determined simply by dividing the peak values of the two voltages (y into x) that are applied to the oscilloscope:

$Z = U_1/U_2\,S$,

where S is the transfer factor of the current sensor in A V^{-1}. In the present tester, this factor is set with S_3.

Both the reactance and resistance can be derived from the impedance. For instance, in case of a series network of a resistor and a non-ideal inductance:

$R_s = Z \cos p$

and

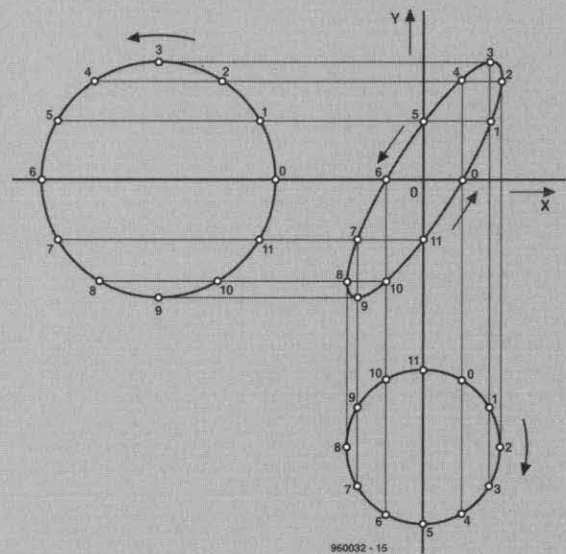
$X_s = Z \sin p$.

In case of a parallel network of a resistor and a non-ideal capacitor:

$R_p = Z \cos p$

and

$X_p = Z \sin p$.



The value of the inductor or capacitor is calculated from the computed value of the reactance:

$C = 1/2\pi fX$

and

$L = X/2\pi f$.

To determine whether the c.o.t. is a capacitance or an inductance, the oscilloscope must be set to the time base position. If U_2 lags U_1, the c.o.t. is a capacitor; if it leads, the c.o.t. is an inductor.

daries, 15 V, 4.5 VA each (for instance, Velleman 2150050M from Maplin)

F_1 = fuseholder (preferably integral in mains entry) with 50 mA slow fuse

1 off heat sink for IC_2, 20 K W^{-1}, for instance, Fischer FK222/SA-220

from Dau Ltd, telephone (01243) 553 031

1 off enclosure, 60×150×132 mm ($2^3/_8$×$5^7/_8$×$5^3/_{16}$ in)

1 off PCB Order no. 960032 (see p.70)

[960032]

Figures talk ...

In this box, a number of measurement results on standard components are given. The curves on your oscilloscope should be roughly in accord with the figures shown here. Note, however, that their shape depends on the oscilloscope settings.

Figure B1 pertains to a 2.2 nF capacitor. The settings were: f = 10 kHz; U = 10 V; i = 1 mA V^{-1}.

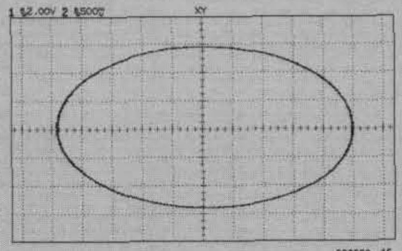
Figure B2 refers to a 2.2 mH inductor. The settings were f = 1 kHz; U = 5 V; I = 10 mA V^{-1}. The measurement shows that the inductor has a series resistance of about 32 Ω, resulting in a phase shift of around 22°.

Figure B3 relates to a 10 kΩ resistor. Settings were f = 1 kHz; U = 10 V; I = 1 mA V^{-1}.

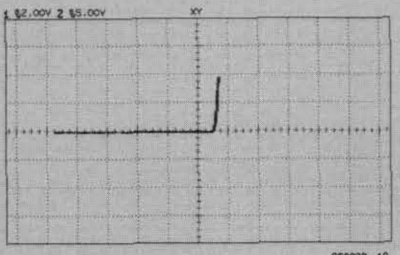
Figure B4 pertains to a 1N4148 diode. The settings were f = 1 kHz; U = 10 V; I = 10 mA V^{-1}.

Figure B5 refers to a zener diode (8.2 V, 500 mW). The settings were f = 1 kHz; U = 10 V; I = 10 mA V^{-1}.

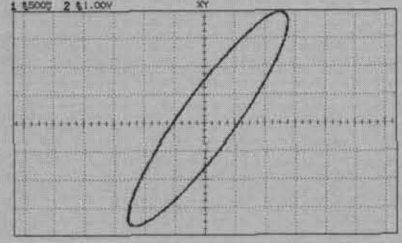
B1



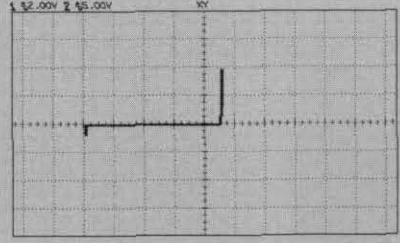
B4



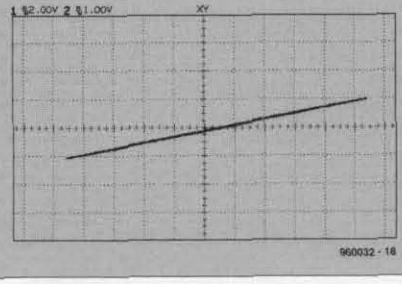
B2



B5



B3



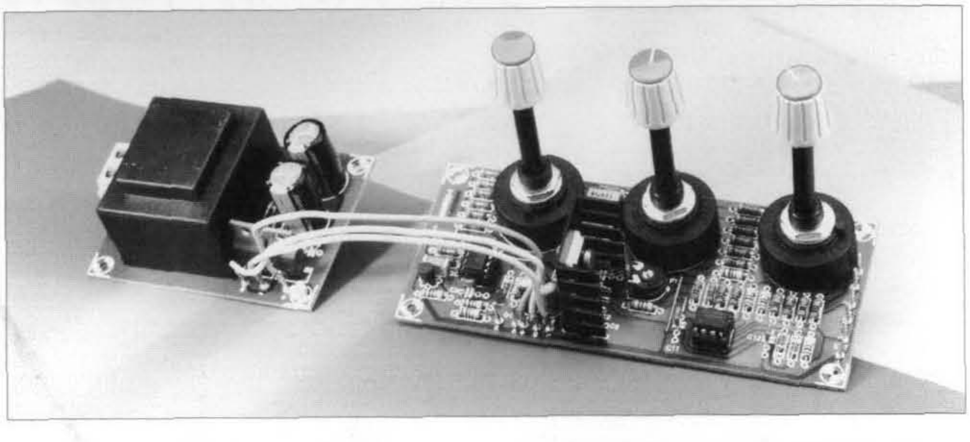


Fig. 5. The finished prototype board of the passive-component tester.