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Focus on:
Digital Television

AUDIO & HI-FI • COMPUTERS & MICROPROCESSORS • DESIGN IDEAS • RADIO, TELEVISION & COMMUNICATIONS • SCIENCE & TECHNOLOGY • TEST & MEASUREMENT

ELEKTOR ELECTRONICS

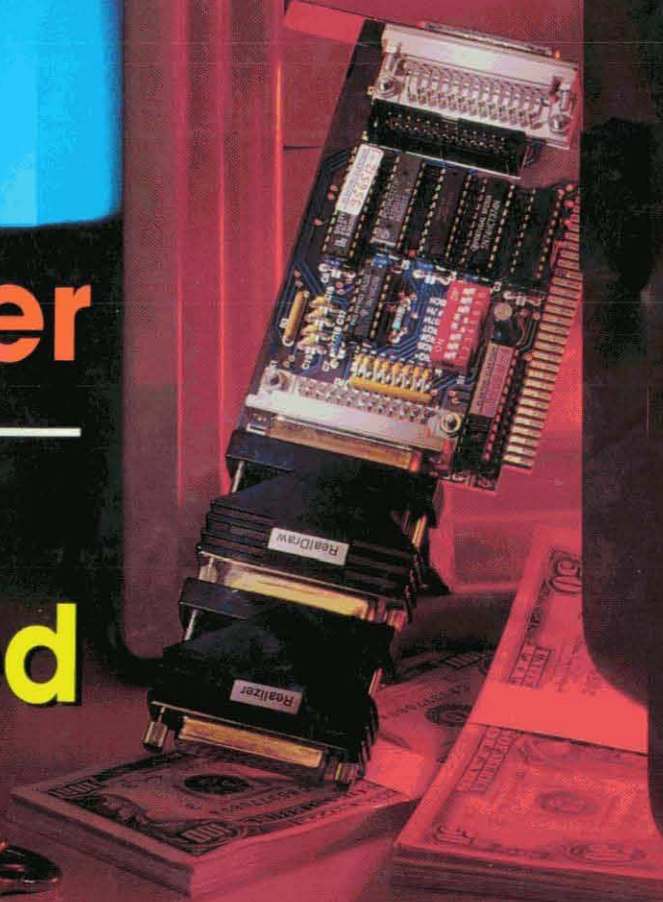
THE INTERNATIONAL
ELECTRONICS MAGAZINE

DONGLE SAFE

RF tone-dip
oscillator

HEXFET
power
amplifier

Layan
reviewed



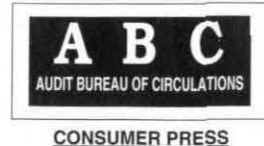
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- **Focus on:** Test and measurement with a personal computer
- Miniature BASIC computer
- Picture-in-picture processor
- Capacitance meter
- CE (Conformité Européenne = European Compliance) labelling of electronic equipment
- and others for your continued interest

Front cover

The dongle, a small plug-in device, is one of the most efficient ways of protecting software against nefarious copying. Unfortunately, that makes it attractive to thieves as well. The dongle safe shown is an insertion card into which several dongles can be plugged. It is intended to give additional security to a dongle by hiding it out of sight.

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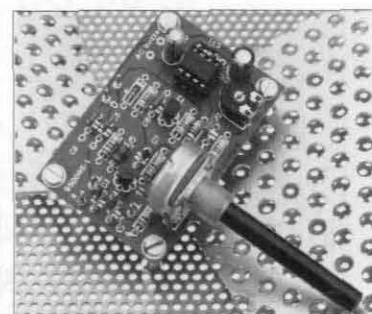
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From the World of Electronics

John Presper Eckert

John Presper Eckert, co-inventor of the first electronic digital computer, died in June in Bryn Mawr, Pennsylvania, aged 76.*

**Eniac - Electronic Numerical Integrator and Computer - was developed in collaboration with John Mauchly, who died in 1980. The computer weighed 30 tons and occupied a whole room. It was ready just in time to confirm the design calculations for the world's first atomic bomb in 1945. Today's desktop computers, a thousand times faster and a fraction of the size, still use the same principle as Eniac.*

OPTOELECTRONICS

Current and future UK trends

The major issue in the future of the British optoelectronics industry lies in the direction taken in creating the UK's information superhighway and this is closely linked to whether BT (British Telecom) will be able to supply programme material across its networks. Until clear decision-taking replaces the present delays, the development of UK superhighway services will remain restricted and will lag behind the USA and Japan.

The industry within the UK has experienced a period of major changes at corporate level which has seen a series of mergers, takeovers and acquisitions. Most observers expect more settled times ahead with the products and the technology making an ever-growing contribution to the economy. Nortel Limited's manufacturing plant at Paignton, southwest England, exports a high proportion of its production and currently is among the more vigorous businesses in its field.

Two institutions, Optical Research Centre - ORC - at Southampton, the responsibility of Southampton University and University College, London, and the Scottish Collaborative Initiative in Optoelectronic Sciences - SCIOS - represent the largest research groupings in the UK. Both are partly Government funded, with SCIOS experiencing a recent boost from the renewal by the Engineering and Physical Sciences Research Council (EPSRC) of four rolling grants.

Other Government support for the industry comes from the LINK collaborative research programme now transferred to the Office of Science and Technology of the Department of Trade and Industry (DTI). Their recently-launched 'Photonics' programme replaces 'Optoelectronics',

started in 1989 and nearing completion, and will continue to assist in the funding of development.

Strong presence.

Optoelectronic research enjoys a strong presence across the central belt of Scotland which the Scottish Enterprise Board expects, following development, to lead to far wider employment opportunities. The formation of the Scottish Optoelectronics Association will further reinforce the industry's position alongside the fruitful research pursued at local universities, among them Glasgow, Edinburgh, Heriot-Watt, St Andrews and Strathclyde.

For most UK suppliers, 1994 has been a most satisfactory year, says Dr Bridget Marx who is Secretary and Chairman of the UK Laser and Electro-Optic Association (UKLEO), a body dedicated to the promotion of a vigorous, high-quality and healthy laser and electro-optic industry in the UK. During 1993, companies sustained growth levels between 25% and 35%, which have extended through 1994, with the highest rates in the supply of smaller components rather than large laser-based systems.

In telecommunications, the market remains strong with estimated growth of 35% during 1994. Similarly, steady growth is taking place in the materials processing market which experienced a later uptake of lasers to remain unaffected by the recession. UK industry is behind a healthy instrumentation market with suppliers looking increasingly to the industrial market as university and other research establishment funding has decreased.

Industry mainstay

While export business is still the UK optoelectronics manufacturing industry's mainstay, each company is helping to expand the use of lasers in the UK at a steady if not spectacular rate, according to Dr Marx.

The medical market has been buoyant with a new dermatological ruby system receiving TÜV certification in Germany and FDA approval in the USA. A laser scalpel is on course for approval in Japan and other spectacular developments of medical optoelectronic equipment are in the pipeline.

In research and development, the UK market remains depressed and has not grown since 1992. This year, however, a realistic prospect emerges from the LINK Photonics funding, with the DTI and the EPSRC together providing around £10 million for research programmes lasting between two and three years. Matching funds are expected from industry to give the sector a much-needed boost. LINK may include laser development besides



This new Edinburgh Instruments Diode Pumped Solid State (DPSS) laser with continuous output power of up to 3 W measures only 270x35x40 mm. Solid-state pumping provides high efficiency and reliability.

applications such as sensing as well as communications and information processing.

Despite the UK providing a relatively small market for industrial lasers, it is disproportionately strong in their manufacture, having originated or brought to fruition some of the key technologies. As examples of this UK pre-eminence UKLEO points to fast axial flow CO₂ lasers and the pioneering systems and applications development work for industrial Nd:YAG lasers.

Pioneering use

The trend continues with pioneering in the use of metal vapour lasers in materials processing and the use of excimer (noble gas) laser processing systems for advanced manufacturing including laser wire and cable marking systems for the aerospace and allied industries. The development of copper vapour laser (CVLs) shows much potential.

In communications, the preponderance of optical fibre will provide a large amount of bandwidth. In considering this, Nortel's Peter Scovell says that by the end of the century the industry expects users in the UK to have access to facilities operating at 40 Gbit s⁻¹ or greater.

He foresees that service providers will be encouraged to devise new ways to exploit that bandwidth and users will demand far more from the network than they have in the past. As a result, there will be dramatic changes in what the network delivers, including enhanced entertainment services, multimedia capabilities, distance learning, telecommuting, teleshopping and personal communication services.

Awesome proportions

The industry does not dispute that the demand for these services will exist, but the issue is emerging of how the network will evolve to provide them. One view is

that a true enabling network will require bandwidths of awesome proportions and a supporting infrastructure built around extremely powerful terminating equipment.

In contrast, photonic switching that could route signals directly without first converting them into electronic signals would enable the establishment of an intelligent network based on optoelectronic technology. Technological developments, market forces, and regulatory decisions will combine to determine the outcome.

UK Laser and Electro-Optic Association (UKLEO), Beech Tree House, The Pathway, Radlett, Herts, United Kingdom. Fax +44 1923 859 395.

Northern Telecom (Nortel Ltd), Brixton Road, Paignton, Devon, United Kingdom TQ4 7BE. Fax +44 1803 662 500.

LINK co-ordinator: The Forbes Partnership Ltd, P O Box 6, Kinross, Scotland, United Kingdom KX13 7BQ. Fax +44 1577 864 152.

APPLE MACINTOSH LEADS WORLD MULTIMEDIA MARKET

A report from Dataquest, a leading US market research consultant, shows that in 1994 the Apple Macintosh led the world multimedia market with a share of 23%, followed by Packard Bell, Compaq, IBM and Gateway 2000.

To insiders, this comes as no surprise, since Apple computers have been working with multimedia since the mid-1980s. Every Macintosh from then on has been equipped as standard with sophisticated sound and graphics facilities. That ease of use is not found in many other computers working with Windows: these often

still require additional cards for sound and graphics. Even Windows 95 will not be able to match the Apple performance, since the world of PC sound and graphics is too fragmented by competing standards. Also, Windows 95 requires a minimum of 8 megabytes memory to run. This is likely to be more expensive than a solution Apple is introducing: an MPEG hardware card (costing under £200) that is simply plugged into their computers and which will enable Cd-i films to be run.

Another boon for Apple has been (and still is) its Power Mac, which can run both DOS and Windows software.

A (not so easily explained) difficulty for Apple is that its equipment is on sale in far fewer retail outlets than competing makes.

Apple Computer (UK) Ltd, 6 Roundwood Avenue, Stockley Park, Uxbridge UB11 1BB, United Kingdom. Phone (0181) 569 1199; fax (0181) 569 2992.

C&G COURSES FOR RADIO AMATEURS

Sevenoaks Adult Education Centre will again run the Radio Amateurs City & Guilds 7650 courses during the forthcoming academic year. Full details of the course, cost, dates and times can be obtained from

Sevenoaks Adult Education Centre, Bradbourne Road, Sevenoaks, Kent TN13 3QN. Phone (01732) 451 618.

CHINA CABLE & SATELLITE TELEVISION SUMMIT '95

The Chinese Institute of Electronics, in co-operation with the Institute for International Research and with the support

of the China Radio and Television Society, has arranged the first international cable and satellite conference in Beijing. The event will be held on 25-27 September 1995. Further information from *Caxton Services Co. Pte Ltd, 29, Tampines Street 92, Caxton Building, Singapore.*

SEARCH COMMENCES FOR 18TH YOUNG WOMAN ENGINEER OF THE YEAR

Young female electronic and electrical engineers interested in holding the prestigious title **1995 Young Woman Engineer of the Year** are invited to apply now to the Institution of Electronics and Electrical Incorporated Engineers (IEEIE) for a nomination form.

The Award will be made to a young woman, under the age of 30, who is able to prove her ability to hold a responsible position in the electronic, electrical or allied engineering field at Incorporated Engineer level. Contender must also have successfully completed all the required technical education and training.

Since the Award's inauguration in 1978, the IEEIE and The Caroline Haslett Memorial Trust, who jointly sponsor the Award, have been delighted with the high calibre of entrants. Past winners have been attracted from every sphere of electronic and electrical engineering—their success makes them ideal role models for other young women who are contemplating a career in the same field.

A cheque for £750 and a silver rose bowl will be presented to the 1995 Young Woman Engineer of the Year at a special ceremony in January 1996. The runner-up will receive the WISE prize of £500.

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The Award often attracts young entrants who, whilst having completed their academic studies, have not had sufficient training and experience to be eligible for the main Award. To encourage such promising young entrants, an additional prize—the Mary George Memorial Prize—will be given. The winner of this prize will receive a cheque for £250 and a silver salver.

Nomination forms for the 1995 Young Woman Engineer of the Year Award are available from *The Secretary, IEEIE, Savoy Hill House, Savoy Hill, London WC2R 0BS. Telephone (0171) 836 3357.*

SIXTH INTERNATIONAL CONFERENCE ON RADIO RECEIVERS AND ASSOCIATED SYSTEMS

The Sixth International Conference on Radio Receivers and Associated Systems will be held at the University of Bath on 26–28 September 1995.

Organized by the IEE, the conference will deal with all frequencies from ELF to millimetre wave. Sessions will be devoted to receiver integrated circuits, receiver measurements and performance, radio systems, mobile and personal radio, paging and cordless communications, antennas and propagation, receiver design, spread spectrum and digital receiver techniques.

Throughout the world, radio receivers are by far the most common types of electronic equipment. Over the past few years, considerable advances have been made in the science and technology upon which the design of receivers depends. At the same time, new system requirements are making increasing demands on receiver designers and are leading to the evolution of essentially new types of receiver.

Full details from *The Institution of Electrical Engineers, Savoy Place, London WC2R 0BL, Telephone 0171 240 1871; fax 0171 836 0190.*

AMATEUR RADIO LICENCES REVISED

The Radiocommunications Agency has announced revisions to both the full and Novice Amateur Radio Licences which:

- allow the Agency to be able to publish the name of individuals whose licences have been revoked; and
- restrict the information released for publications in call books (lists of licensed radio amateurs) where the licence holder has requested their details to be withheld.

Other minor changes have been introduced to update licences including a revised list of CEPT (Conference of European Posts and Telecommunications) member countries and non-CEPT member countries and their association abbreviations.

The Agency will permit the publication of call books by third parties either in written form or as read-only

computer disks (ROMs). The data base of licence holders is held on behalf of the Agency by Subscription Services Ltd (SSL). The database shows whether a licence holder's details may or may not be released for publication in call books. Where details are to be released, the licence holder's call sign, name and mailing address will be released.

Where details are to be withheld, the Agency previously released the call sign and the first part of the licence holder's post code. Following concerns expressed by licence holders, it has been decided to restrict this further so that only the call sign will be released. If licence holders would like to confirm whether or not their details are set up to be released or would like to amend their entry, they should write to SSL at the following address:

*Radio Licensing Centre
Subscription Services Ltd
P O Box 885
Bristol BS99 5LG*

ADVANCED FILTER CIRCUIT SYNTHESIS PROGRAM

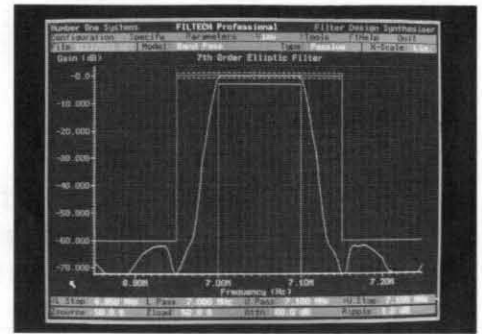
There can be few electronic circuits as widely used as the filter. Almost every piece of electrical equipment contains at least one, even if it is only there to clean up the mains input.

When it comes to designing filter circuits, however, many engineers find the process difficult and time-consuming. Many a circuit designer faced with a choice between advanced mathematics and unwieldy tables has wished there was another way.

Now there is: **FILTECH Professional** from Number One Systems is a low-cost, easy-to-use software package that can completely deskill the process of designing both active and passive filter circuits. The package allows a finished filter design to be obtained simply by specifying the required frequency response and terminating impedances.

However, FILTECH Professional does not eliminate the engineer entirely. Now that the tedious and repetitive calculations are taken over by the program, the designer is free to question and experiment. It takes less than half a minute to see the effect of reducing or increasing the filter order, or changing the filter type from, say, Butterworth to Elliptic, or of altering the frequency limits or attenuation level. You can even force some or all of the components to the nearest preferred value and see the effect straight away.

A circuit simulator is built into FILTECH allowing both the filter specification and the synthesized circuit behaviour to be seen together on the same frequency plot.



Available for just £245 or US\$475, FILTECH Professional designs both active and passive filters up to 12th order and includes support for Bessel, Butterworth, Chebyshev and Cauer (Elliptic) filters.

For addresses, telephone and fax numbers of Number One Systems, see advertisement on page 4.

PC CARDS FOR EMBEDDED CAN NETWORKS

The Controller Area Network (CAN) protocol is rapidly becoming the most widely used protocol for embedded systems. CAN was originally designed for the automotive industry which required a rugged protocol capable of surviving harsh electrical environments together with short message lengths and guaranteed message latency.

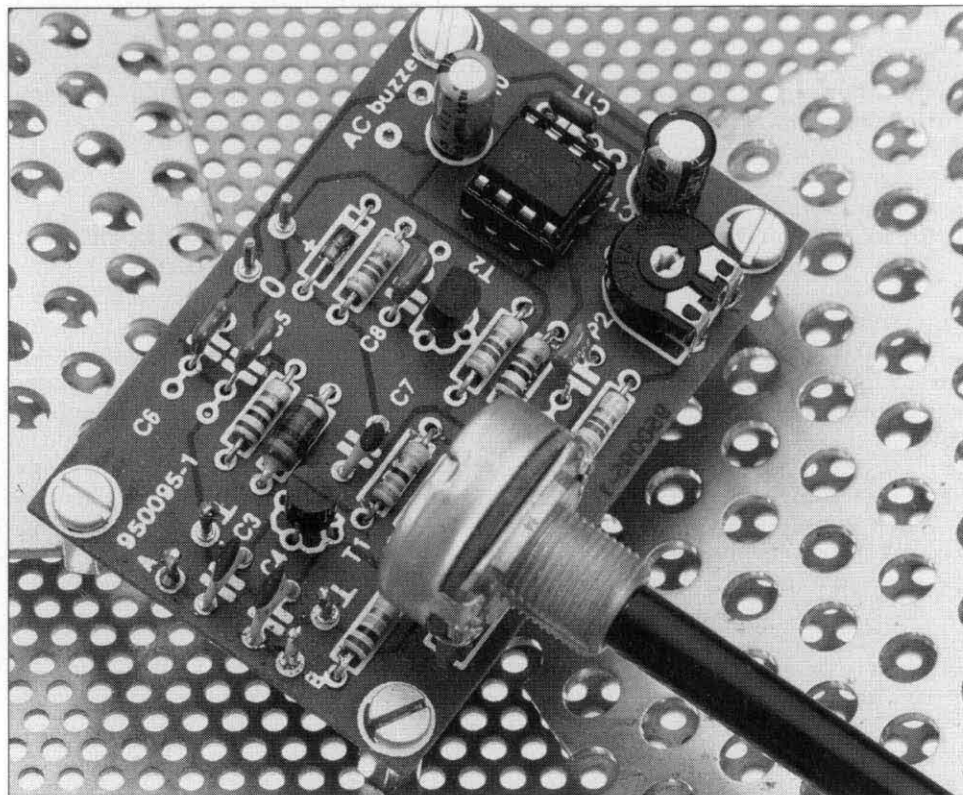
Since many CAN applications require a PC to be added to the network, either for development or as a control or diagnostic terminal, Hitex (UK) are offering a range of high-performance PC CAN cards complete with C libraries for easy development. The CAN cards are available as PC half-cards or PCMCIA cards for applications where portability is a prerequisite. Each card hosts a V25 processor with up to 512 kb of dual-port RAM, which may be used as a FIFO or object buffer. For high-performance systems, a firmware development kit is available, which allows the card to be optimized for customer application.

Further software is also available, which will convert the CAN cards into a CAN bus analyser. The analyser is able to display all of the activity on the network and replay it at a later date. The CAN analyser uses in-built C-like language which may be used to prototype a CAN node on a virtual network before the engineer is committed to any real hardware.

For further details of CAN development tools, contact *Trevor Martin, Hitex (UK) Ltd, Warwick University Science Park, Coventry CV4 7EZ, United Kingdom. Telephone 01203 692066; fax 01203 692131.*

RF TONE-DIP OSCILLATOR

Use this handy instrument to check out the resonance frequency of those unknown or home-brew inductor/capacitor combinations, or as a simple RF signal generator. It works like magic, without any sort of wire connection to the circuit under test, and, remarkably, uses an audible 'tone-dip' indication instead of the traditional moving coil meter.



Design by Edwin Chicken MBE, G3BIK

THE grid dip oscillator is an RF test instrument which has retained its name over a period of more than 50 years despite tremendous changes in electronics technology. Also known as 'grid dipper' or simply 'GDO', the instrument originally had a sensitive moving-coil meter to monitor the grid current of a valve in an oscillator. As the oscillator's resonating elements, a coil and a tuning capacitor, are tuned to the same frequency as the other, unknown, L-C combination, energy transfer occurs ('absorption'), causing the RF output of the GDO to drop appreciably. This is indicated by a 'dip' in the grid current. The resonance frequency of the unknown L-C tuned circuit can then be read from the GDO's calibrated tuning scale. Although the

instrument is basically a frequency measuring device, it is so versatile in both equipment and component measurements that it is generally considered to be the most useful instrument in a radio amateur's shack after the bottle opener and the multimeter.

Nowadays, you would use transistors, diodes and opamps to build such an instrument, but the name 'grid dip oscillator' has remained, although it is really a misnomer. Note that some dip oscillators have appeared on the market by the name of TraDipper (transistorized dipper), but ask any radio amateur and he will still call it a grid dipper!

The disadvantage of using a moving coil meter to detect the 'dip' is that you have to watch it very closely to detect

the needle movement. In particular if you are measuring on a very high-Q circuit, for instance, a crystal oscillator, the needle movement can be very sudden, making the dip frequency difficult to spot as you tune the GDO dial cheerfully. And then, while staring hard at the needle, you easily run into problems with the inductive coupling to the tuned circuit under test because while watching the meter needle, your hands, which hold the instrument, will be unsteady, causing the coil plugged into the instrument to swerve around the target coil. In this way, the distance between the two coils may become too large, or the two may actually touch by accident. In both cases, the degree of (inductive) coupling is not steady, and you need to flick your eyes very quickly between the needle and the coil on the GDO. This can be distracting and difficult for newcomers, hence, a novel method is presented here to make the instrument tell you that it has found the resonance frequency. The idea is to keep your eyes on the GDO coil, your hands steady, and use another of your five senses to detect the dip: hearing!

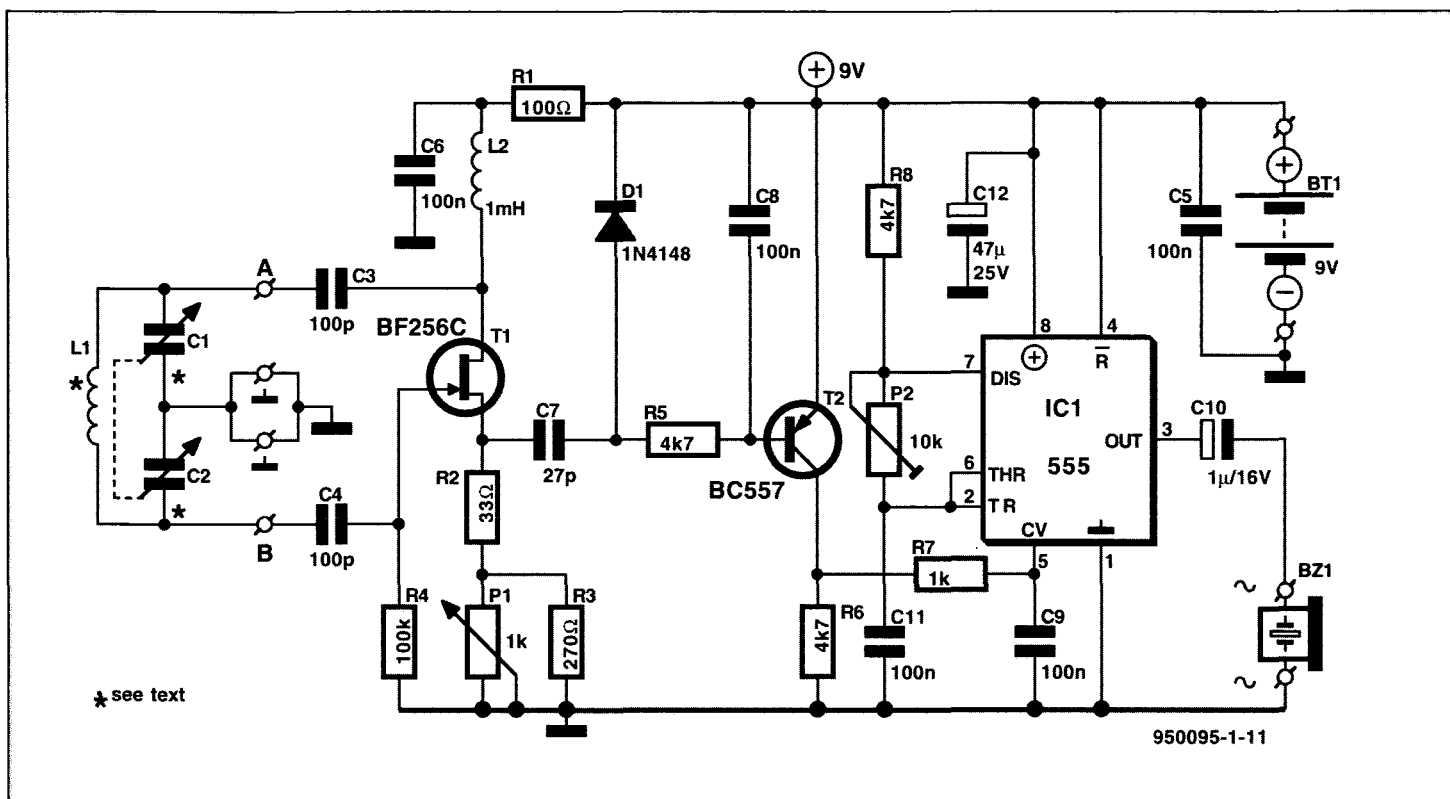
How it works

It is not generally known that the 555 timer IC can be used as a d.c. voltage-to-frequency converter. In the circuit shown in **Fig. 1**, the IC is used as an astable multivibrator to produce an audio tone in an earpiece or a small buzzer. The frequency of the tone is determined in the usual way by the components connected to pins 7, 6 and 2.

That frequency can also be modified to an appreciable extent by applying a positive d.c. voltage to pin 5 of the astable. Pin 5 is d.c. coupled to the collector of p-n-p transistor T_2 , which in association with its collector load resistor acts as a d.c. potential divider.

The RF output voltage from the oscillator built around FET T_1 is rectified by diode D_1 , which so acts as a d.c. control bias to the base of the transistor.

When the tuning coil of the RF oscillator's tuned circuit, L_1 - C_1/C_2 , is proximity-coupled to an external tuned circuit of the same resonating frequency, the RF energy absorbed by the external circuit reduces the RF signal level being fed to the rectifier diode, and so causes a change in bias to T_2 . That small d.c. change is amplified by the transistor to yield a significant change in the voltage level at its collector, and so at pin 5 of the 555.



The magnitude and polarity of the d.c. voltage swing applied to the astable are such that a noticeable lowering (dip) is produced in the audio frequency tone applied to the earphone or buzzer.

The inductor used in the RF oscillator is exchangeable to enable a wide

frequency range to be covered at sufficient tuning accuracy. The tuning ranges and inductor construction information may be found in **Table 1**. Potentiometer P_1 is adjusted for optimum tone-dip effect. In practice, you adjust it for a steady tone roughly in the middle of the tuning range you wish

COMPONENTS LIST

Resistors:

$R_1 = 100\Omega$
 $R_2 = 33\Omega$
 $R_3 = 270\Omega$
 $R_4 = 100k\Omega$
 $R_5; R_6; R_8 = 4k7$
 $R_7 = 1k\Omega$
 $P_1 = 1k\Omega$ linear
 $P_2 = 10k\Omega$ preset H

Capacitors:

$C_1; C_2 =$ polyvaricon, $2 \times 128pF$ (see text)
 $C_3; C_4 = 100pF$
 $C_5; C_6; C_8; C_9; C_{11} = 100nF$
 $C_7 = 27pF$
 $C_{10} = 1\mu F$ 16V radial
 $C_{12} = 47\mu F$ 25V radial

Inductors:

$L_1 =$ plug-in coil, home made, see text
 $L_2 = 1mH$

Semiconductors:

$D_1 = 1N4148$
 $T_1 = BF256C$
 $T_2 = BC557B$
 $IC_1 = TLC555$

Miscellaneous:

$Bz_1 =$ a.c. buzzer or earpiece.
 $Bt_1 = 9V$ PP3 size battery with clip-on lead.
 Printed circuit board, order code 950095-1, see page 70.

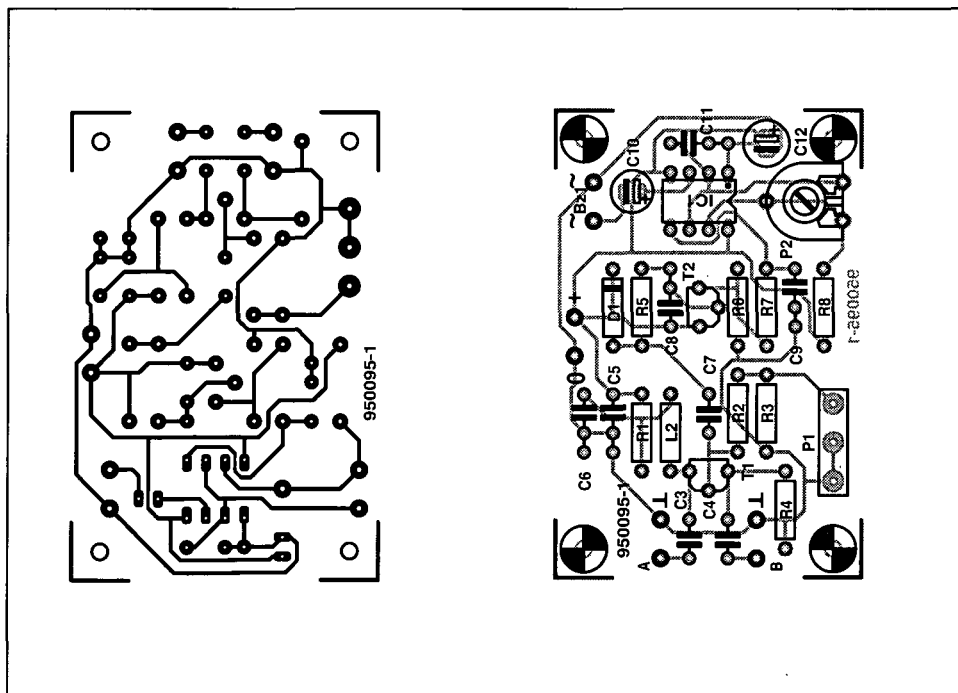


Fig. 2. Printed circuit board design for the RF tone-dip oscillator (board available ready-made). The polyvaricon tuning capacitor is connected to the points marked A, B and ground. Use very short wires!

No. of turns	wire dia. (mm)	inductor dia. (mm)	frequency range (MHz)
65	0.2	8	9-12
40	0.2	8	12-16
24	0.2	8	16-20
17	0.2	8	20-26
22	0.4	6	26-35
14	0.4	6	34-46
10	0.4	6	45-60
6.5	0.4	6	60-80
5	0.4	6	75-100
4	1	10	87-116
3	1	10	104-140

Table 1. Make these inductors if you use a 2x226 pF polyvaricon tuning capacitor.

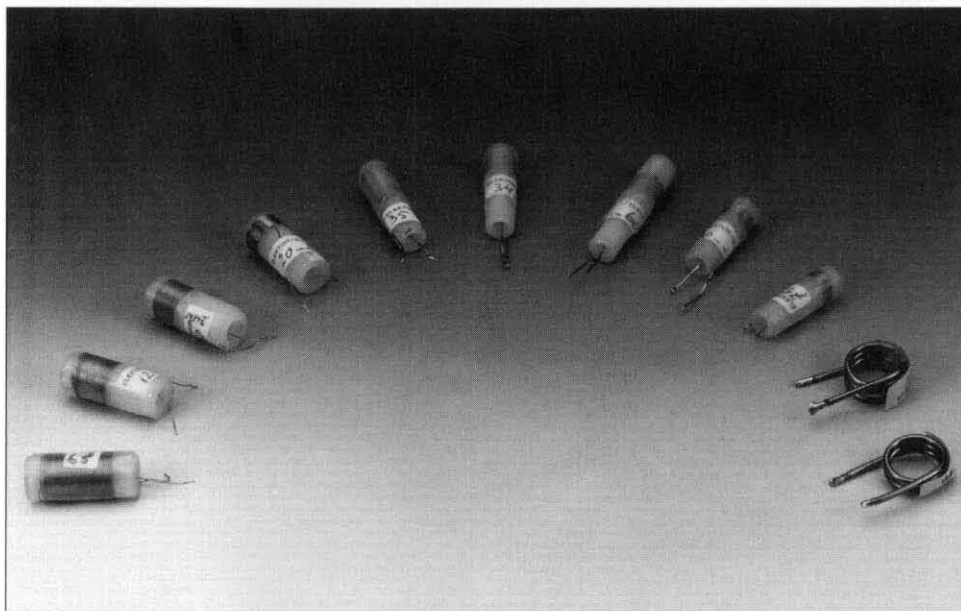


Fig. 4. The plug-in coils wound for the tone dipper. Construction information may be found in Table 1.

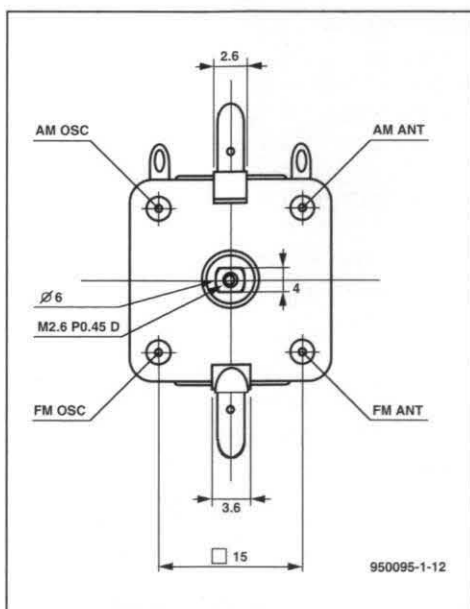


Fig. 3. Mechanical outlines of the FE-2217 dual tuning capacitor from Toko. Note the flattened shaft with internal M2.6 threading.

to use. Preset P_2 enables you to adjust the frequency of the tone. It is normal for the tone to vary gradually as you go through the tuning range.

The instrument is powered by a 9-V PP3 size battery. Current consumption is of the order of 15 mA.

Construction

Construction of the RF tone-dip oscillator should not present problems if you use the printed circuit board shown in Fig. 2. This board is available ready-made through the Readers Services. Simply fit all the parts as per the indications on the component overlay and the components list.

The author used a type FT79L film-dielectric AM/FM miniature variable capacitor from Maplin for C_1 - C_2 (note: this device seems to be superseded by the type AB11M now found in the Maplin catalogue). The two 126-pF sections in series give 63 pF maximum

across the coil. The coils used are ready-made radial lead fixed inductors type 7BS (Toko) purchased from J.A.B. Electronics. Each of the four coils is soldered to the two pins of an DIN loudspeaker plug, and is contained within the plastic plug cover. Each cover has its cable entry end cut off to be level with the top face of the coil within. Frequency coverage, after assembly, is approximately:

inductance	range
120 μ H	1.7-4.3 MHz
27 μ H	3.7-9.2 MHz
5.6 μ H	8-20 MHz
1.0 μ H	19-48 MHz

Other types and brands of 'polyvaricon' tuning capacitors may also be suitable. The *Elektor Electronics* laboratory prototype of the dipper was built with a type FE 2217 polyvaricon from Toko. This type has a capacitance range of 2x226 pF on the AM sections, and unfortunately requires more plug-in inductors to be made than the configuration suggested by the author, see Table 1. The connection details and mechanical outlines of the FE 2217 are shown in Fig. 3. The centre lug between the ones marked AM OSC and AM ANT is connected to ground.

To avoid undue stray capacitance, the leads between the DIN socket (which receives the plug-in coils) and points 'A' and 'B' on the board should be kept shorter than 1 cm.

More construction suggestions

Boxing and mechanical finishing of the instrument is to personal taste and skills, and no hard and fast rules are given here. The tuning capacitor is fitted with a dial which is calibrated with the aid of a shortwave radio and/or a frequency meter with each of the plug-in coils fitted one after another. While fixing the tuning capacitor to the inner face of the box panel, make sure that the 2.5-mm screws can not touch the vanes. As a suggestion, the dial can be made from the flat circular lid from a domestic container. To enable it to protrude from the side of the instrument, so you can turn it, the dial should have a diameter which is slightly larger than the width of the enclosure used. A central 2.5-mm hole is drilled in the dial, so that it can be bolted to the face of the shaft of the tuning capacitor. Two short strips of plastic may be glued to the rear face of the dial, about the central hole, to secure the dial onto the flattened spindle of the tuning capacitor. The cursor may be a strip of clear plastic with a central scored line. This strip is fitted at a small height above the dial.

(950095)

HEXFET AMPLIFIER UPGRADE

Design by T. Giesberts

The Medium Power HEXFET amplifier published in this magazine in December 1993 has one small drawback: it delivers 'only' 60 W into 8 Ω (or 120 W into 4 Ω). Otherwise, it is a first class amplifier that provides excellent music reproduction, which is evidenced not so much by measurement as by audition. To some listeners, it has a quality not unlike that of a valve amplifier. Because of its popularity and the many requests for a version with higher output power, it has been upgraded to provide around 90 W into 8 Ω (about 160 W into 4 Ω).

By a stroke of good fortune, a pair of IGBTs (Insulated Gate Bipolar Transistors - see our June 1995 issue) proved ideal replacements for the HEXFETs used in the original design. Apart from the figures for power output, the technical specification remains virtually the same (see box).

Modification

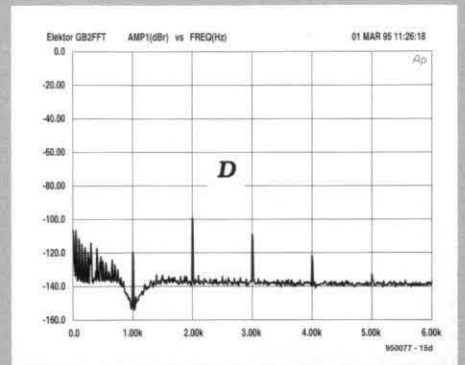
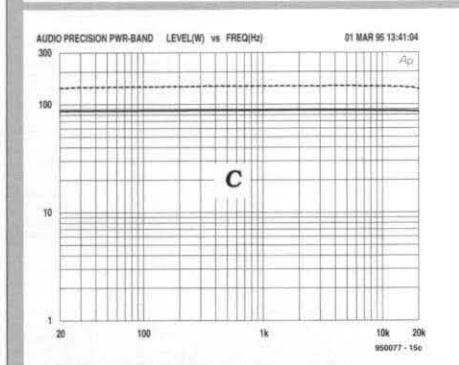
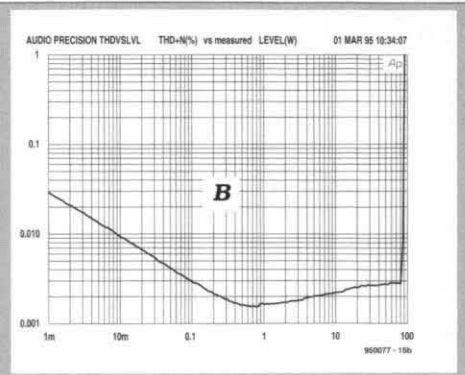
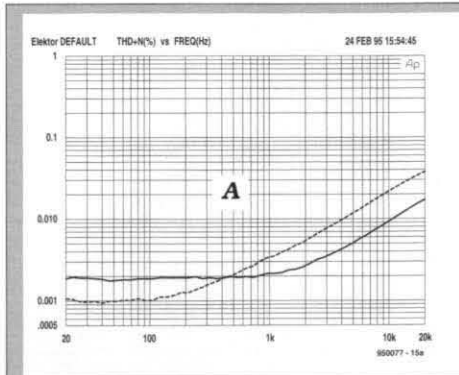
The original design already allowed for a higher-output version, whence the duplicated holes for the output transistors on the printed-circuit board. At that time, advance information on the IGBTs was already available, but samples were not.

Although IGBTs are quite different from HEXFETs, the board for the original design can be used without any modification. In fact, the circuit has hardly changed. The most noticeable alteration is the replacement of the fuses in the source lines of the power FETs by emitter resistors for the IGBTs. The only other changes are in the value of two resistors in the compensating circuit of the input stage, of one in the quiescent-current circuit, and of one resistor and two capacitors in the protection circuit. This means that anyone who has built the original HEXFET amplifier can quickly modify it to the upgraded version.

One item needs to be replaced, however: the mains transformer. After all, more power can not be obtained from the same supply voltage/current. The original transformer with 2x25 V secondaries must be replaced by one that provides 2x30 V at 3.75 A. This will result in a direct voltage of ± 43 V.

Circuit description

The circuit diagram of the upgraded amplifier is given in **Fig. 1**. Changed with respect to the earlier version are



Brief technical data

Input sensitivity	1.1 V r.m.s.
Input impedance	47.7 k Ω
Power output (1 kHz, 0.1% THD)	88 W into 8 Ω 146 W into 4 Ω
Music power (1 kHz burst, 5 cycles on, 5 cycles off)	94 W into 8 Ω 167 W into 4 Ω
Power bandwidth (40 W into 8 Ω)	1.5 Hz - 115 kHz
Slew rate	>35 V μ s ⁻¹
Signal-to-noise ratio (1 W into 8 Ω)	105 dB (A-weighted) 101 dB (linear 22 Hz - 22 kHz)
Harmonic distortion (1 W into 8 Ω)	0.002% (1 kHz)
(80 W into 8 Ω)	0.003% (1 kHz)
Intermodulation distortion	<0.05% (20 Hz - 20 kHz)
(50 Hz:7 kHz; 4:1)	0.002% (1 W into 8 Ω)
Dynamic intermodulation distortion	0.003% (40 W into 8 Ω)
(rectangular 3.15 kHz + sine wave 15 kHz)	0.0025% (1 W into 8 Ω)
Damping factor (at 8 Ω)	0.002% (80 W into 8 Ω)
	>600 (1 kHz)
	>400 (20 kHz)

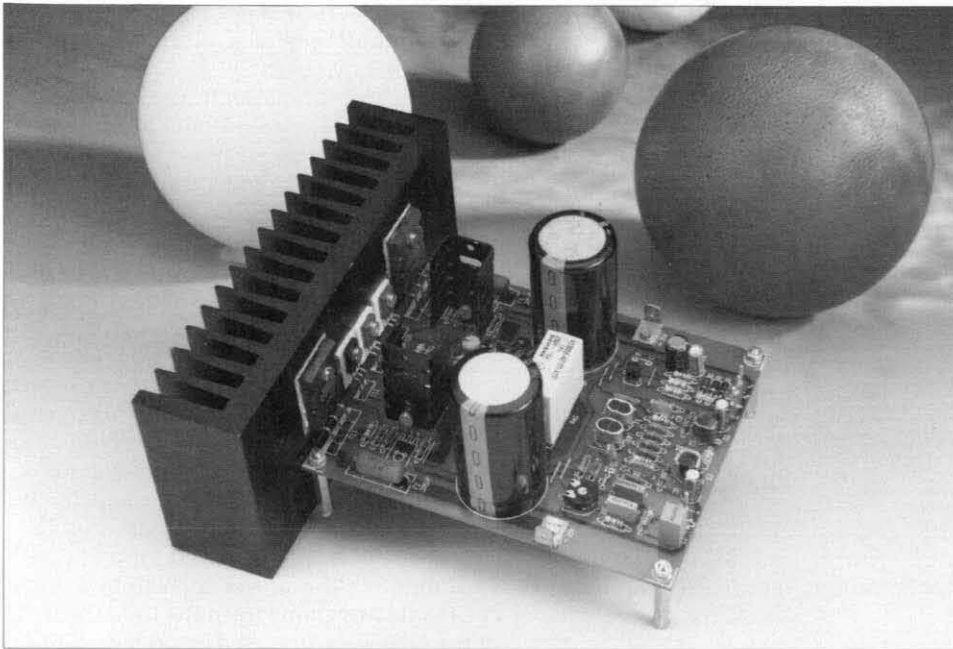
Measurements for the characteristics shown were made with an Audio Precision analyser.

A shows the total harmonic distortion (THD+N) from 20 Hz to 20 kHz. The solid curve refers to 1 W into 8 Ω and the dashed one to 75 W into 8 Ω .

B shows the distortion at 1 kHz as a function of drive (bandwidth 22 Hz - 22 kHz; load 8 Ω). The sharp bend at the end of the curve is the clipping point.

C shows the maximum power output when the distortion is 0.1%. It shows that the power is independent of frequency, whether the load is 8 Ω (solid curve) or 4 Ω (dashed curve).

D shows a Fourier analysis of a 1 kHz signal (1 W into 8 Ω) with the fundamental suppressed. The 2nd, 3rd and 4th harmonics can be seen, but they are attenuated, respectively, by 100 dB, 110 dB and 120 dB with respect to the fundamental frequency.



T₁₂, T₁₃, RF₁, RF₂, R₃, R₄, R₂₁, R₃₅, C₁₃ and C₁₄. Also, to improve performance at high frequencies, a damping resistor has been added to, or rather in, inductor L₁. Finally, to improve the noise figure, the impedance of input filter R₁-C₂ has been lowered.

A symmetrical design has the advantage that it minimizes problems with distortion, particularly that associated with even harmonics. Therefore, the input stages consist of two differential amplifiers, T₁-T₂ and T₃-T₄. These use discrete transistors, not expensive dual devices, to keep the cost down. Performance is excellent, particularly if the transistors are matched.

A differential amplifier is one of the best means of combining two electrical signals: here, the input signal and the feedback signal. The amplification of the stage is determined mainly by the ratio of the collector and emitter resis-

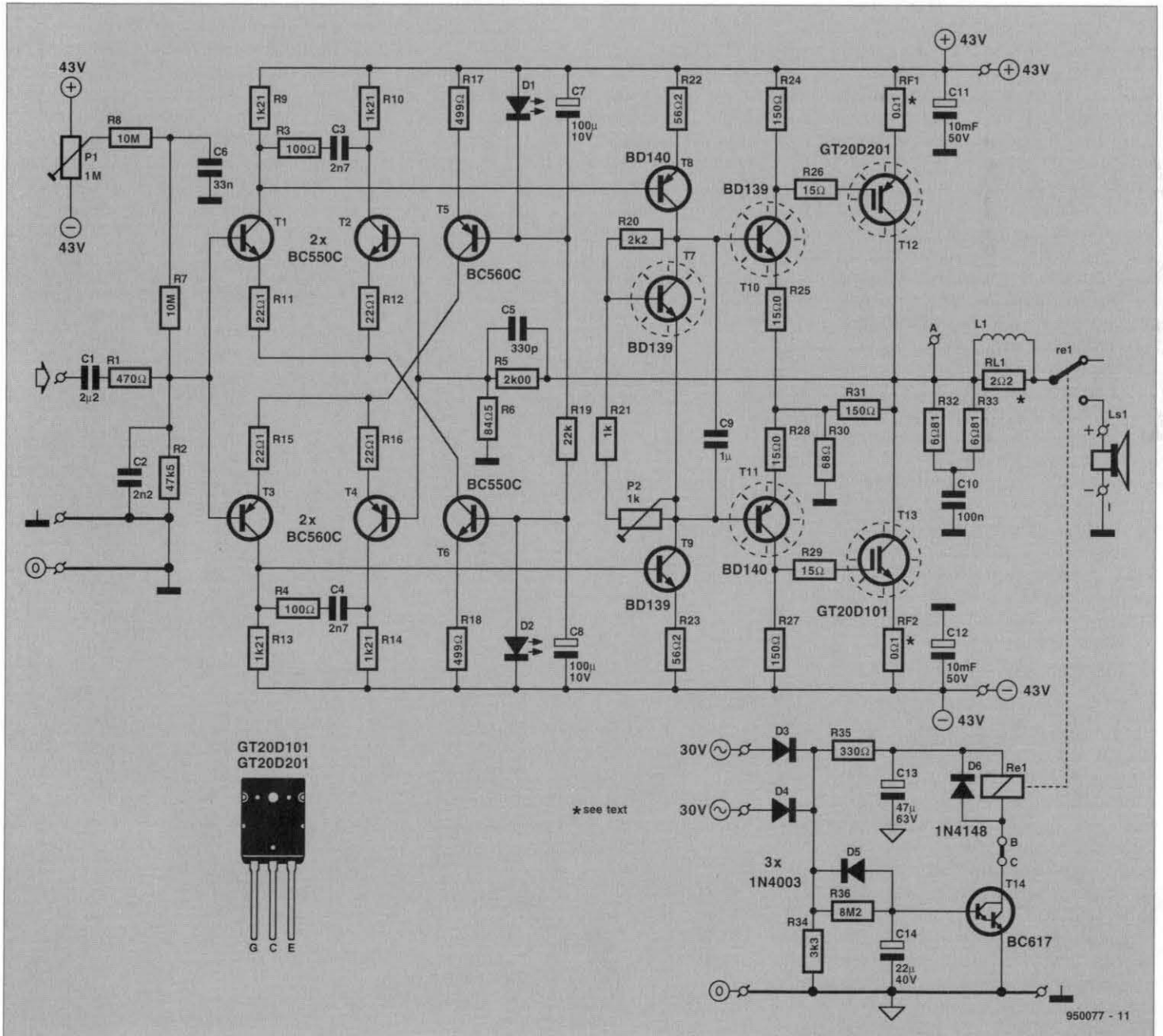


Fig. 1. Circuit diagram of the upgraded (IGBT) amplifier.

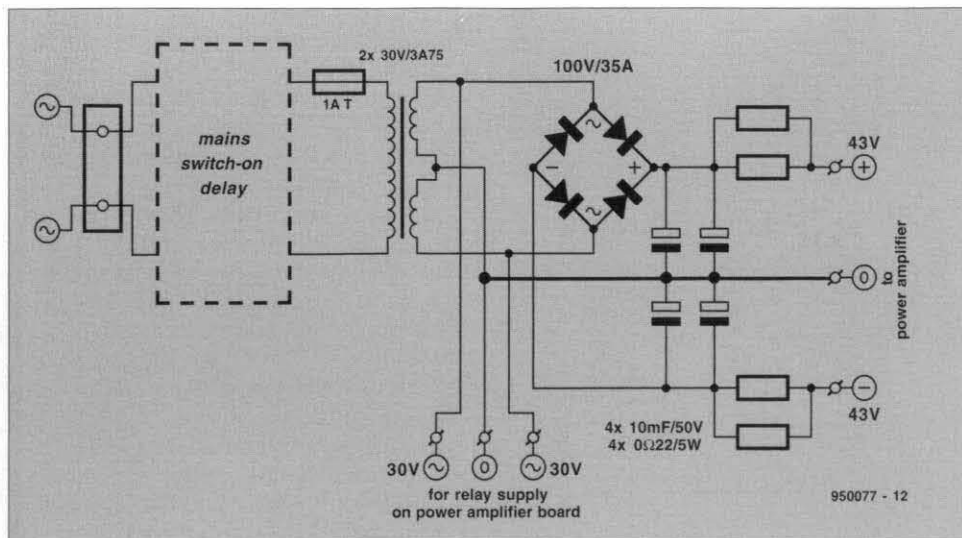


Fig. 2. Circuit diagram of the power supply for one mono IGBT amplifier.

tances (in the case of T_1 - T_2 these are R_9 , R_{10} , R_{11} and R_{12}). These provide a form of local feedback: limiting the amplification reduces the distortion.

Two RC networks (R_3 - C_3 and R_4 - C_4) limit the bandwidth of the differential amplifiers and these determine, to a degree, the open-loop bandwidth of the entire amplifier.

The d.c. operating point of the differential amplifiers is provided by two current sources. Transistor T_6 , in conjunction with R_{18} and D_2 , provides a constant current of about 2 mA for T_1 - T_2 . Transistor T_5 , with R_{17} and D_1 , provides a similar current for T_3 - T_4 . The combination of a transistor and an LED creates a current source that is largely independent of temperature, since the temperature coefficients of the LED and the transistor are virtually the same. It is, however, necessary that these two components are thermally coupled (or nearly so) and they are, therefore, located side by side on the printed-circuit board.

In the input stage, C_1 is followed by a low-pass section, R_1 - C_2 , which limits the bandwidth of the input to a value that the amplifier can handle. Resistor R_2 is the base resistor of T_1 and T_3 . So far, this is all pretty normal. Network P_1 - R_7 - R_8 is somewhat out of the ordinary, however. It forms an offset control to adjust the direct voltage at the output of the amplifier to zero. Such a control is normally found **after** the input stage. The advantage of putting it before that stage is that the inputs of the differential amplifiers are exactly at earth potential, which means that the noise contribution of their base resistors is negligible.

The signals at the collectors of T_1 and T_3 are fed to pre-drivers T_8 and T_9 . Between these transistors is a 'variable zener' formed by T_7 which, in conjunction with P_2 , serves to set the quiescent current of the output transistors.

The output of the pre-drivers is ap-

plied to T_{10} and T_{11} , which drive IGBTs T_{12} and T_{13} . This power section has local feedback (R_{30} - R_{31}).

The design of T_{10} - T_{13} is a kind of compound output stage, since the collector of the power transistors is connected to the output terminal. The voltage amplification is limited to $\times 3$ by the local feedback resistors (R_{30} - R_{31}). Here again, this

feedback serves to reduce the distortion. The overall feedback of the amplifier is provided by R_5 - R - C_5 .

Electrolytic capacitors C_{11} and C_{12} (10,000 μ F each and part of the power supply) are located close to the IGBTs, so that the heavy currents have only a short path to follow.

At the output is a Boucherot network, R_{32} - R_{33} - C_{10} , that ensures an adequate load on the amplifier at high frequencies, since the impedance of the loudspeaker, because of its inductive character, is fairly high at high frequencies.

Inductor L_1 limits any current peaks that may arise with capacitive loads.

The signal is finally applied to the loudspeaker, LS_1 , via relay contact Re_1 . The relay is not energized for a few seconds after the power is switched on to obviate any plops from the loudspeaker. Such plops are caused by brief variations in the direct supply voltage arising in the short period that the amplifier needs to reach its correct operating level.

The supply voltage for the relay is derived directly from the mains transformer via D_3 and D_4 . This has the advantage that the relay is deactuated, by virtue of the low value of C_{13} , immediately the supply voltage fails. The delay

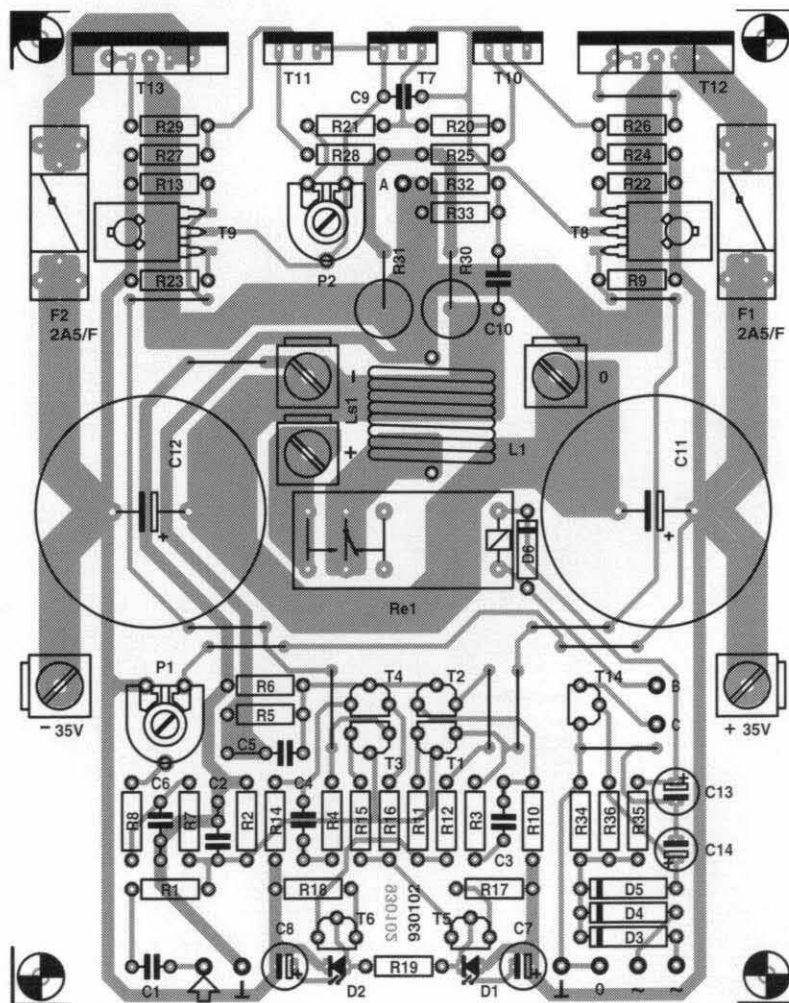


Fig. 3. Printed-circuit board

in energizing the relay is provided by T_{14} in conjunction with R_{36} and C_{14} . It takes a few seconds before the potential across C_{14} has risen to a value at which T_{14} switches on. This darlington transistor requires a base voltage of not less than 1.2 V before it can conduct.

The power supply—see Fig. 2—is traditional, apart from the resistors, R_5 – R_8 , in the power lines. These limit, to some degree, the very large peak charging currents drawn by electrolytic capacitors C_{11} and C_{12} . Moreover, together with these capacitors, they form a filter that prevents most spurious voltages from reaching the amplifier. Measurements on the prototype showed that this was particularly evident at frequencies below 500 Hz.

Construction

The design of the printed-circuit board for the amplifier (Fig. 3) takes good account of the large currents that flow in the amplifier. This has given rise to a couple of tracks being paralleled instead of combined, so that the effect of currents in the power section on the input stages is minimal.

Populating the board is straightforward. Although not strictly necessary,

it is advisable to match the transistors used in the differential amplifiers. This may be done conveniently on an h_{fe} tester by measuring the amplification at a collector current of about 1 mA. If such a tester is not available, use a base resistor that results in a collector current of about 1 mA measured with a multimeter. With the same resistor, test a number of other transistors and note the collector currents. Mount the selected pairs on the board and pack them closely together with a 5 mm wide copper ring (made from a piece of 12 mm copper water pipe).

Inductor L_1 consists of six turns, inner diameter 16 mm ($5/8$ in), of insulated copper wire 1.5 mm ($1/16$ in) thick. Mount RL_1 inside the coil.

The large transistors are located on one side of the board, so that they can be fixed directly to the heat sink. They must be insulated from the heat sink with the aid of ceramic washers.

The two sizes indicated on the board for T_{12} and T_{13} were explained earlier.

Connections from the power supply

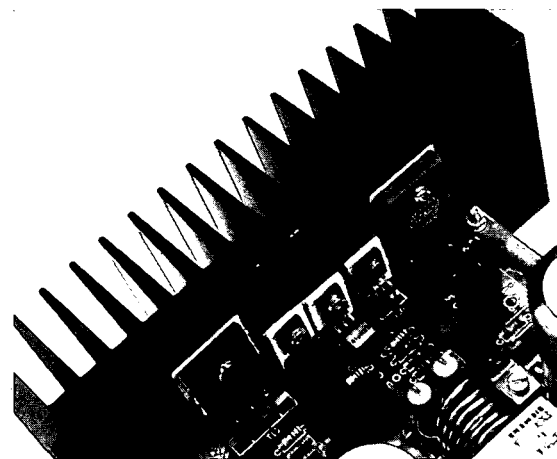


Fig. 4. Good thermal coupling between the transistors and the heat sink ensures a long life of the devices.

and to the loudspeaker are by means of terminal blocks that can be screwed on to the board.

Mount the two amplifier boards, mains transformers and electrolytic capacitors in a suitable enclosure. The wiring diagram for one channel is given in Fig. 5.

It is advisable to measure the supply voltages before they are applied to the amplifiers. Also, turn P_2 to maximum (wiper towards R_{33}) before connecting the power supply to the amplifiers. Set input presets P_1 to the centre of their travel. A few seconds after the supply has been switched on, the relay should come on. Connect a multimeter (1 V direct voltage range) and adjust P_1 until the meter reads zero (both channels!).

Switch the supply off again and connect a multimeter (100 mV d.c. range) across RF_1 or RF_2 . Switch on the supply and adjust P_2 for a meter reading of about 10 mV: this corresponds to a quiescent current of 100 mA through T_{12} and T_{13} . After about half an hour, the current will have stabilized at about 200 mA (meter reading of about 20 mV). Readjust P_2 slightly if required. Note that owing to the positive temperature coefficient of IGBTs, the quiescent current does not increase but drop with rising dissipation.

Finally, recheck the direct voltages at the outputs of the amplifiers and, if necessary, readjust P_1 slightly.

The loudspeakers must be 4-ohm or 8-ohm types, whose impedance must not drop below 3 Ω . It is not permissible to connect two 4-ohm units in parallel to the amplifier, because that would give problems when large drive signals are applied to the IGBTs.

Parts list (one channel)

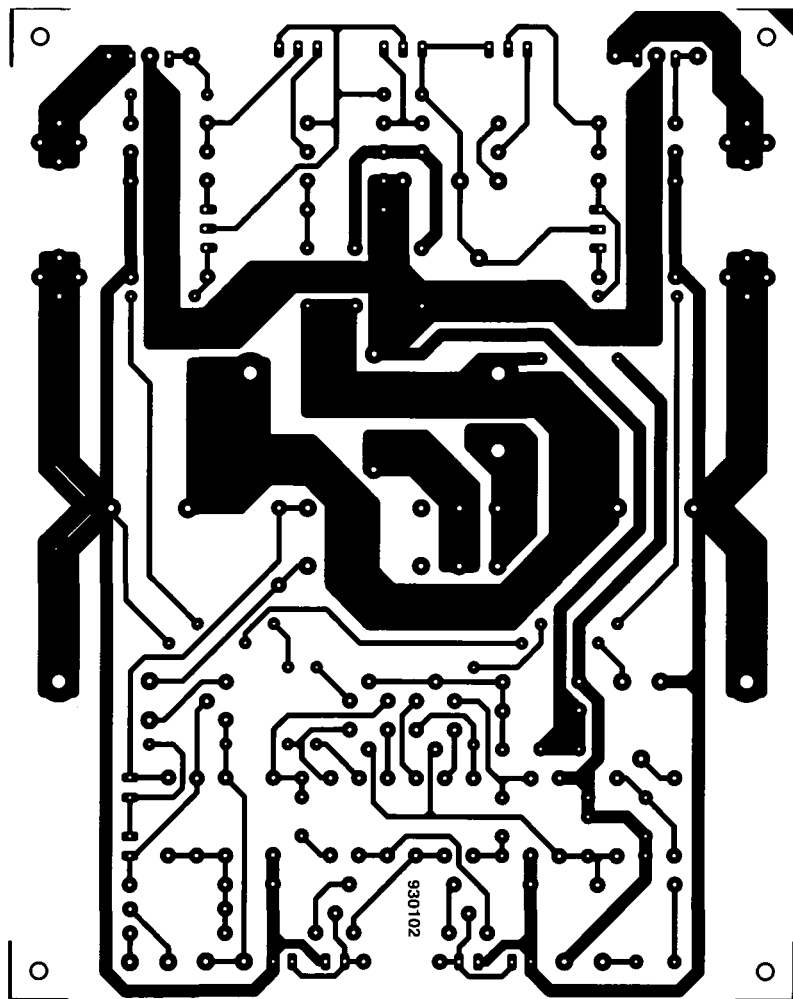
Resistors:

$R_1 = 470 \Omega$

$R_2 = 47.5 \text{ k}\Omega$, 1%

$R_3, R_4 = 100 \Omega$

$R_5 = 2.0 \text{ k}\Omega$, 1%



for the IGBT amplifier.

$R_6 = 84.5 \Omega$, 1%

$R_7, R_8 = 10 \text{ M}\Omega$

$R_9, R_{10}, R_{13}, R_{14} = 1.21 \text{ k}\Omega$, 1%

$R_{11}, R_{12}, R_{15}, R_{16} = 22.1 \Omega$, 1%

$R_{17}, R_{18} = 499 \Omega$, 1%

$R_{19} = 22 \text{ k}\Omega$

$R_{20} = 2.2 \text{ k}\Omega$

$R_{21} = 1 \text{ k}\Omega$

$R_{22}, R_{23} = 56.2 \Omega$, 1%

$R_{24}, R_{27} = 150 \Omega$, 1%

$R_{25}, R_{28} = 15.0 \Omega$, 1%

$R_{26}, R_{29} = 15 \Omega$

$R_{30} = 68 \Omega$, 5 W

$R_{31} = 150 \Omega$, 5 W

$R_{32}, R_{33} = 6.81 \Omega$, 0.6 W, 1%

$R_{34} = 3.3 \text{ k}\Omega$

$R_{35} = 330 \Omega$

$R_{36} = 8.2 \text{ M}\Omega$

$RF_1, RF_2 = 0.1 \Omega$, 5 W

$RL_1 = 2.2 \Omega$, 5 W (fit inside L_1)

$P_1 = 1 \text{ M}\Omega$ preset

$P_2 = 1 \text{ k}\Omega$ preset

Capacitors:

$C_1 = 2.2 \mu\text{F}$, 50 V, polypropylene

$C_2 = 2.2 \text{ nF}$

$C_3, C_4 = 2.7 \text{ nF}$

$C_5 = 330 \text{ pF}$, polystyrene, axial

$C_6 = 33 \text{ nF}$

$C_7, C_8 = 100 \mu\text{F}$, 10 V, radial

$C_9 = 1 \mu\text{F}$, polypropylene, pitch 5 mm

$C_{10} = 100 \text{ nF}$

$C_{11}, C_{12} = 10,000 \mu\text{F}$, 50 V, radial,
for PCB mounting

$C_{13} = 47 \mu\text{F}$, 63 V, radial

$C_{14} = 22 \mu\text{F}$, 40 V, radial

Inductors:

$L_1 = \text{air-core}$, 0.1 mH (see text)

Semiconductors:

$D_1, D_2 = 3 \text{ mm LED}$, red (1.6 V
drop at 3 mA)

$D_3\text{--}D_5 = 1\text{N}4003$

$D_6 = 1\text{N}4148$

$T_1, T_2, T_6 = \text{BC}550\text{C}$

$T_3\text{--}T_5 = \text{BC}560\text{C}$

$T_7, T_9, T_{10} = \text{BD}139$

$T_8, T_{11} = \text{BD}140$

$T_{12} = \text{GT}20\text{D}201$

$T_{13} = \text{GT}20\text{D}101$

$T_{14} = \text{BC}617$

Miscellaneous:

$Re_1 = \text{relay}$, 24 V, 1 make contact (e.g.,
Siemens V23056-A0105-A101*)

$F_1, F_2 = \text{fuse}$, 2.5 A, fast, with holder for
PCB mounting

Ceramic washers (5) for T_7, T_{10}, T_{11}

Mica washers (2) for T_{12}, T_{13}

Terminal block (5) (see text)

Heat sink, 0.6 KW^{-1} (e.g., Fischer SK85**)

PCB Order No. 930102 (see p. 70)

Power supply:

Mains transformer, $2 \times 30 \text{ V}$, 375 VA

Mains on-off switch with indicator

Fuse 1 A, slow with holder

Bridge rectifier Type B200C35000

Electrolytic capacitor (4), $10,000 \mu\text{F}$,
50 V

Resistor (4) 0.22Ω , 5 W

PCB (for mains-on delay) Order no.
924055 (see p. 70)

* ElectroValue, 3 Central Trading Estate,
Staines, TW18 4UX, ☎ (01784) 442 253.
Private customers welcome.

** Dau (UK) Ltd, 7075 Barnham Road,
Barnham, West Sussex PO22 0ES.
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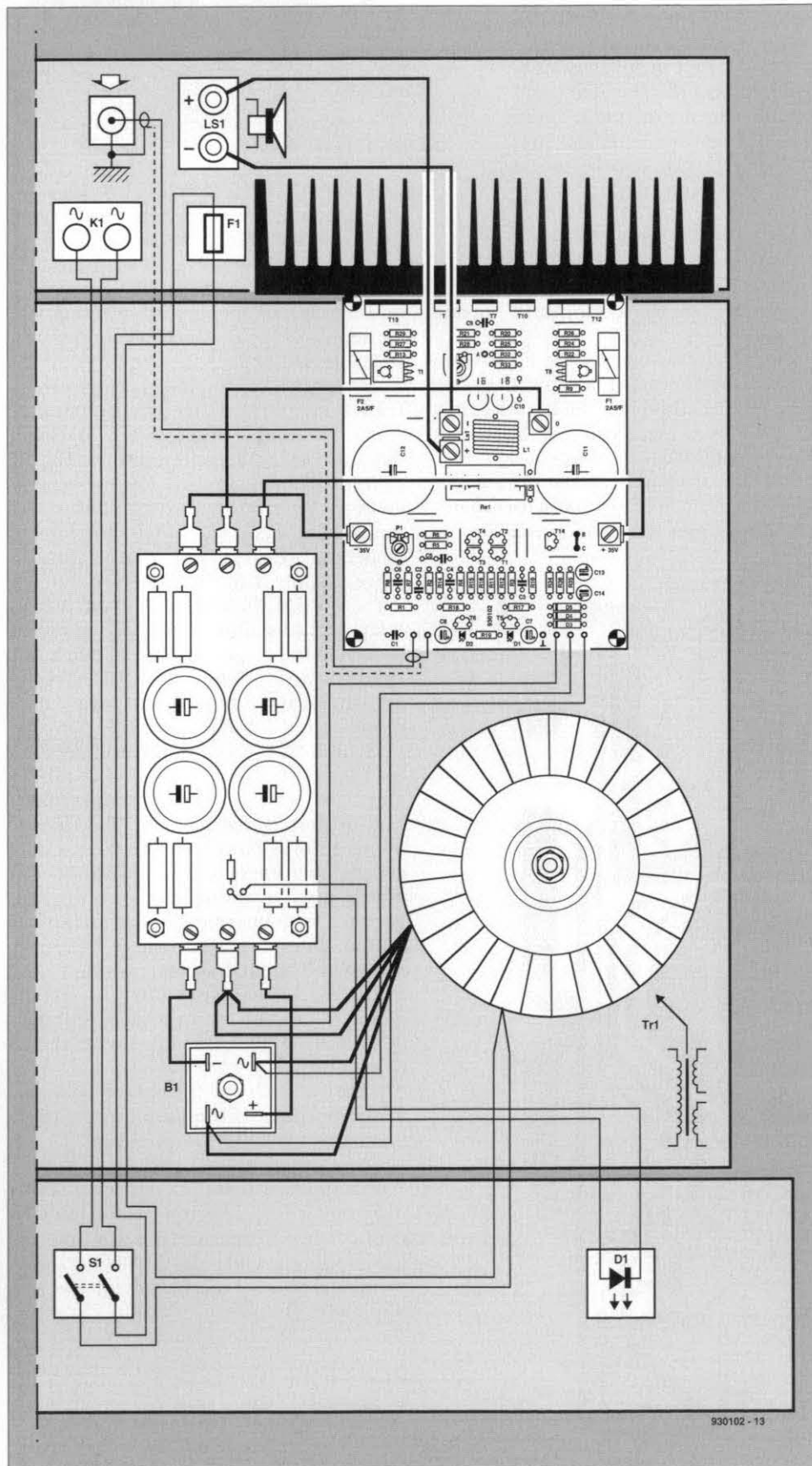


Fig. 5. Wiring diagram of the IGBT amplifier.

[950077]

Mains switch-on delay

The circuitry of the 'black box' (in dashed lines) in Fig. 2 is shown above. It may be asked what the function of it is, since there is already a power-on delay in the amplifier itself. That delay serves to obviate pops and clicks caused by switching; it connects the loudspeakers to the amplifier only after this has had a short period of 'settling down'.

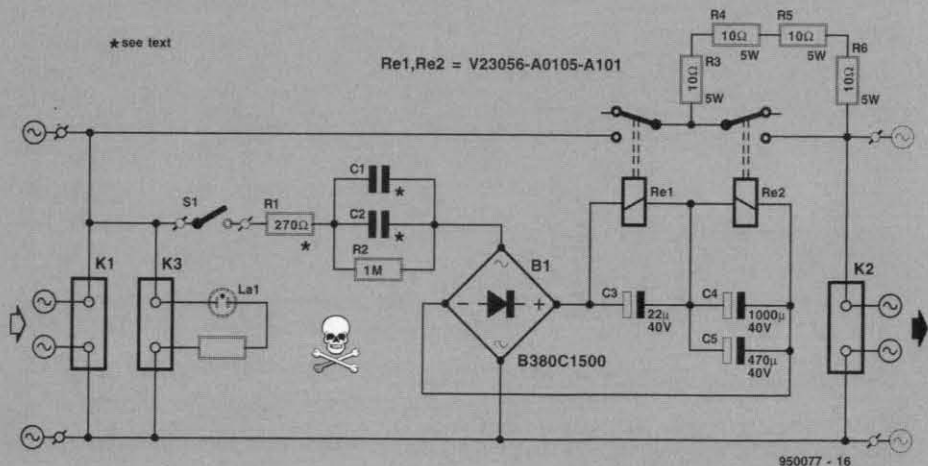
The mains switch-on delay is intended to switch on the mains gradually with heavy loads, so that the fuses do not blow

In the circuit, a number of power resistors, R_3 - R_6 , are connected in series with the mains supply lines to limit the current at switch-on to 5 A. When the mains is switched on with S_1 , only relay Re_1 is energized in the first instance, so that the current must flow through the power resistors. When after a few seconds capacitors C_4 and C_5 have been charged, relay Re_2 is also energized, whereupon

the power resistors are short-circuited by the relay contacts. These few seconds allow the buffer capacitors in the power supply to be charged at a reasonable rate, so that high currents are prevented.

The relay coils are connected in series and are energized directly by the mains via bridge rectifier B_1 , imped-

ances Z_{C1} and Z_{C2} , and R_1 . The value of C_1 and C_2 depends on the current required by the relay coils and the level of the mains voltage. The relays specified are rated at 30 mA. If the mains voltage is 240 V, C_2 can be omitted and C_1 should have a value of 470 nF and a rating of 630 V d.c.



Could you please elaborate on what we would use to produce an INHX8M (Intel hex-8) format file, please.

Ian Gill (by email)

We would be surprised to see a PIC code assembler which does not support the Intel hex-8 format. MPASM (free from Microchip) does the job, too. There are also lots of file conversion utilities around which produce INHX8 output.

Thanks Jan,
You were exactly right, MPASM is the program I was looking for (and free too). Unfortunately entry into the world of PICs is difficult for hobbyists faced with numerous businesses trying to sell high priced programmers and software, we don't always get pointed to the simple solutions and free software. Thanks for your help and thank you for running the very timely June edition mini PIC programmer story.

Regards, Ian Gill

HEXFET amplifier oscillation

I have built the amplifier described in the article 'HexFET Amplifier Upgrade' (September 1995). I am

very pleased with the performance of the amplifier, both as regards measurement and sonic results. However, during my measurements I discovered short high-frequency oscillation burst which occurs any time the amplifier is switched on or off. Although these bursts are without consequence because of the output relay, I am writing to inform if this problem is known, and if there is a possible remedy.

J. Glerum

Yes, we do recognize the phenomenon you mention, it is caused by the IGBT transistors used in the design. Although the oscillation is not harmful, it is not proper! Those of you who want to get rid of it may fit a second Boucherot network in parallel with the one already present (R32-R33-C10). The extra network should consist of a series connection made from a 220-nF (0.22- μ F) capacitor and a 6.8- Ω resistor with a power rating of 5 watts. This combination should be connected between point 'A' and ground, which is best done at the solder side of the board. As far as we have been able to ascertain, this modification does not affect the amplifier's performance.

APPLICATION NOTE

The content of this note is based on information received from manufacturers in the electrical and electronics industries or their representatives and does not imply practical experience by *Elektor Electronics* or its consultants.

8-bit non-volatile digital-to-analogue converters (DACs)

A Wolfson Microelectronics Application

The digital-to-analogue converters (DACs) in the WM80xx series from Wolfson Microelectronics* are 8-bit voltage output devices with high-impedance buffered reference input(s). All devices are available in DIP or SO cases.

Some of the devices have on-board non-volatile memory, which ensures retention of settings on power down. No special voltage is needed for programming the non-volatile memory. Others must be programmed at each and every switch-on. The table gives an overview of the various types.

Typical applications of the devices include programmable voltage source, programmable attenuator, programmable filter. The non-volatile types can also be used as replacement for trim potentiometers.

Inside the DACs

Figure 1 shows the block schematic and pinout of the four devices. The core of each DAC is a resistor with 256 taps, corresponding to the 256 possible codes. One end of each resistor is connected to the GND pin and the other is fed from the output of an input buffer amplifier. Monotonicity is guaranteed by the use of the resistor. Linearity depends on the matching of the resistors in the multi-DAC devices, and on the performance of the output buffer. Because the input is buffered, the DAC always presents a high impedance load to the reference source.

Floating-gate devices are used for the non-volatile memory. The voltage required to program these is generated by an on-chip charge pump that is turned on for the duration of the LATCHB pulse when the store instruction is given.

Power-up causes an immediate re-

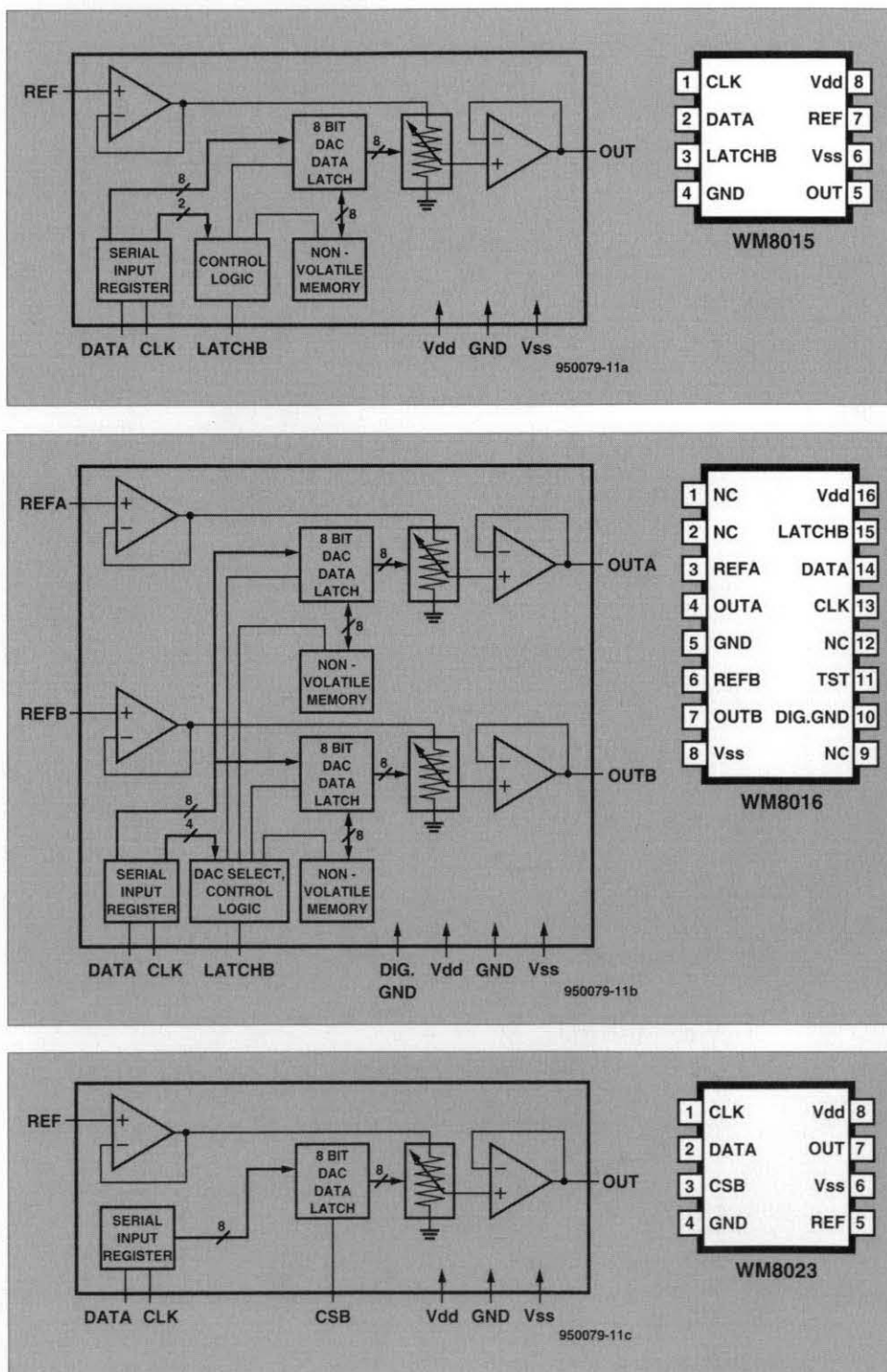


Fig. 1. Block diagrams and pinouts of the four WM80xx devices (fourth on next page).

* Wolfson Microelectronics, Luton Court, 20 Bernard Terrace, Edinburgh EH8 9NX, Great Britain. Telephone +44 (0)131 667 9386; fax +44 (0)131 667 5176.

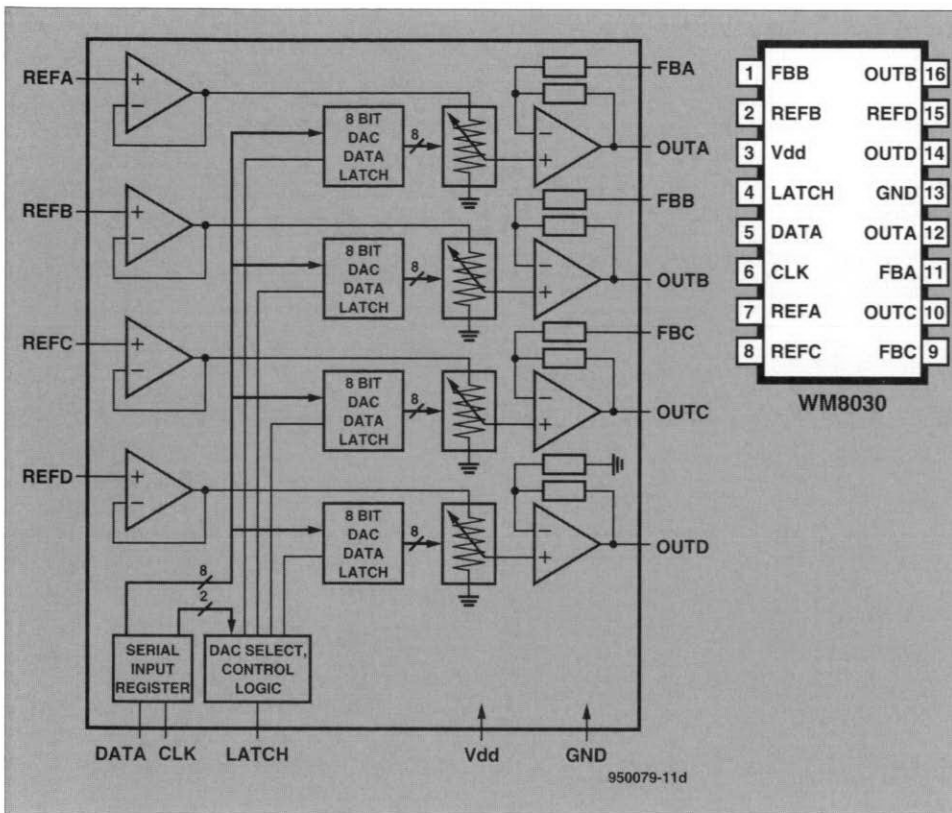


Fig. 1. Continued from preceding page.

call instruction, which remains for typically 5 ms. It is not possible to write to the device during this power-on reset period.

The output voltage, U_o , is given by:

$$U_o = U_{REF} \times \text{CODE}/256,$$

in the case of the WM8015, WM8016 and WM8023, and

$$U_o = U_{REF} \times \text{CODE}/256 (\times 2),$$

in the case of the WM8030, where CODE is the digital input code and is in the range 0–255, and the ($\times 2$) amplification is optional for three of the DACs in the WM8030. The amplification is set when feedback loops FBA, FBB, or FBC are linked to ground. Without this link, the amplification is unity. The amplification of the fourth DAC (outD) is always $\times 2$.

The WM8015, WM8016 and WM8023 run from a single 5 V or a ± 5 V supply; the WM8030 from a 3–10 V supply.

The logic inputs are TTL and CMOS compatible. When a single supply is used, the reference input must not exceed 2 V; with a bipolar supply, it must be within the range -5 V to $+2$ V.

Applications

Some applications of devices in the WM80xx series are shown in Fig. 2. For clarity's sake, programming connections DATA, CLK, and LATCHB (or CSB) have been omitted.

The simplest of the applications is a single-pole, programmable voltage source shown in Fig. 2a. The reference voltage is obtained with a zener diode. As stated earlier, the output voltage is $U_o = U_{REF} \times \text{CODE}/256$. A bipolar, programmable output voltage, if needed, can be obtained with an additional operational amplifier. The output voltage can then be preset in the range $+(127/128)U_{in}$ to $-(127/128)U_{in}$ (see Fig. 2b).

Provided the input voltage is 0–2.5 V (single supply) or -5 V to 2 V (bipolar supply), the devices can be arranged as programmable trim potentiometers as shown in Fig. 2c. The special property of the WM8015 and WM8016 is that the programming is retained by the non-volatile memory on each subsequent power-up. This makes these types particularly suitable as replacement for preset potentiometers.

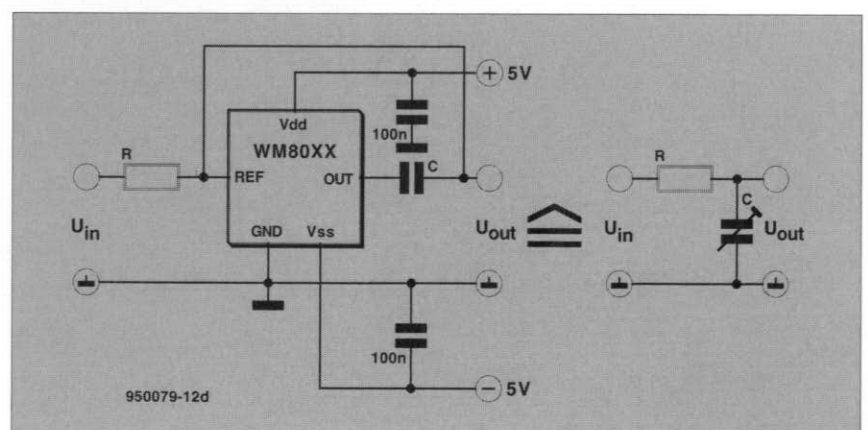
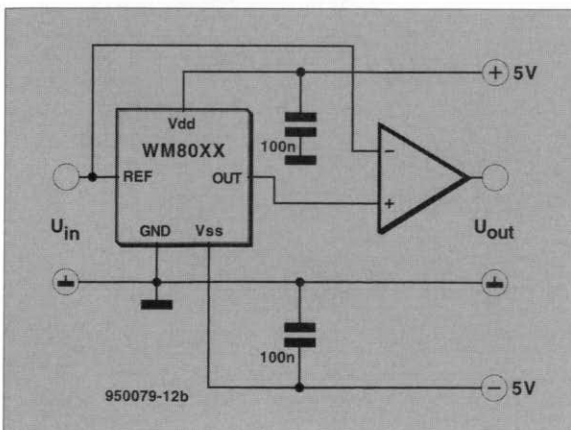
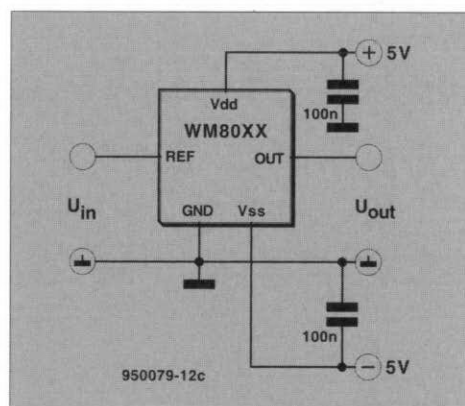
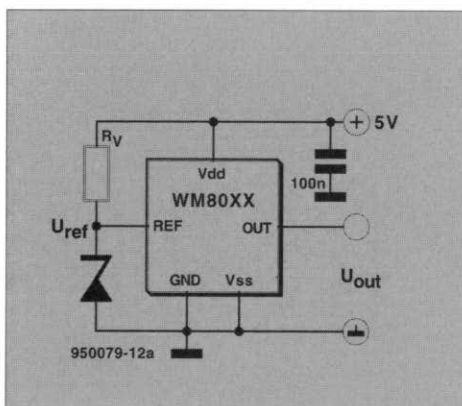


Fig. 2. Application circuits: (a) single-pole, programmable voltage source; (b) bipolar, programmable voltage source; (c) programmable potentiometer; (d) programmable RC low-pass filter.

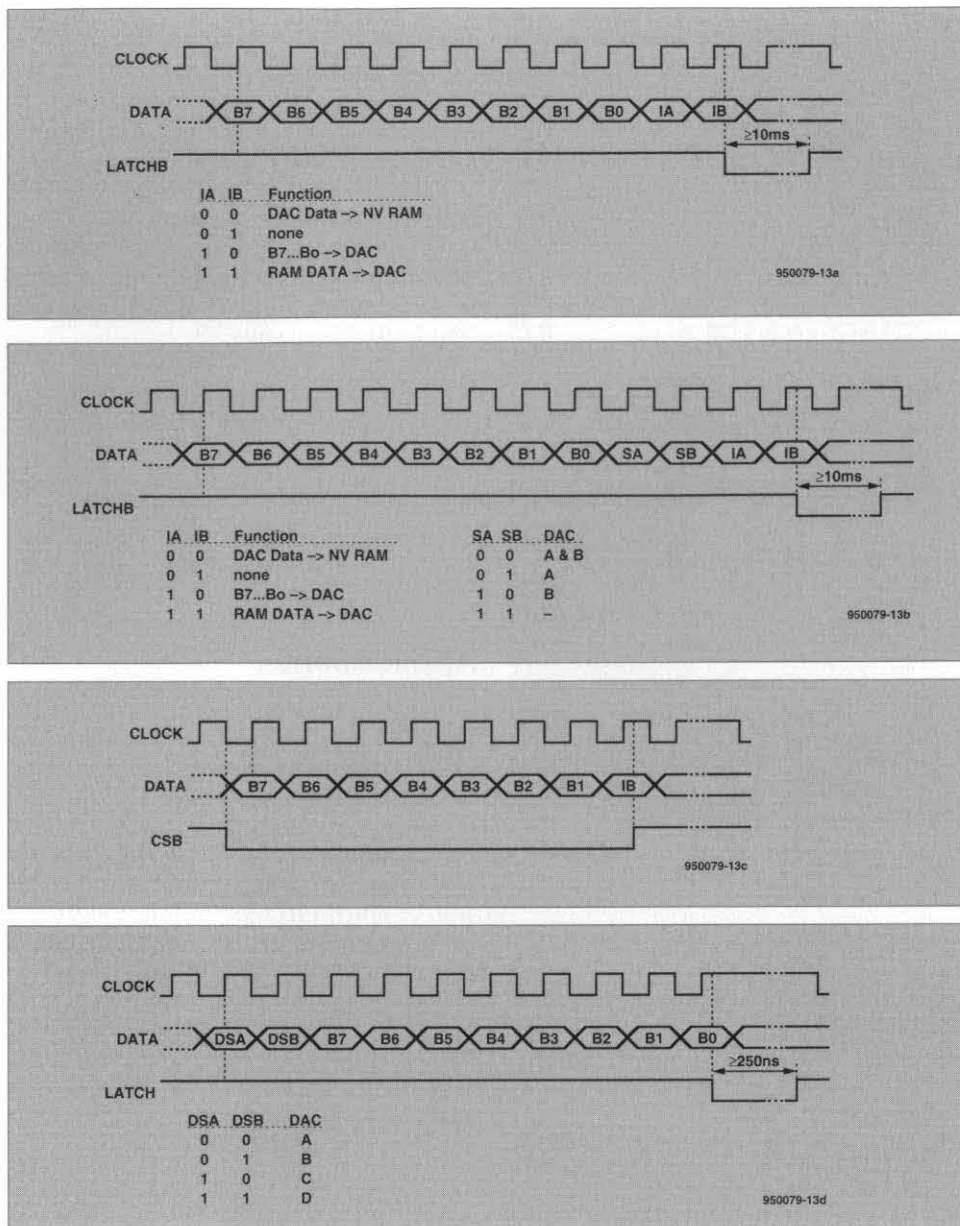


Fig. 3. Timing diagrams: (a) WM8015; (b) WM8016; (c) WM8023; (d) WM8030.

Type	Function	Package
WM8015S	8-bit DAC*	8-pin SO
WM8015D		8-pin plastic DIP
WM8016S	2×8-bit DAC*	16-pin SO
WM8016D		16-pin plastic DIP
WM8023S	8-bit DAC	8-pin SO
WM8023D		8-pin plastic DIP
WM8030S	4×8-bit DAC	16-pin SO
WM8030D		16-pin plastic DIP

* with non-volatile memory

Overview of the four devices in the WM80xx series.

The overall bandwidth for such applications is about 100 kHz.

The devices can also be used to advantage in filter technology. Figure 2d shows a typical application of the WM8023 as a single-pole RC low-pass filter, whose cut-off frequency is programmable over the range 400 Hz to 100 kHz. The equivalent capacitance, C , can be set in the range $\frac{1}{256}C$ to C in 256 steps.

Programming

Devices in the WM80xx series are set with the aid of a 3-pin interface: one for DATA, one for CLOCK and the third for STROBE. Figure 3 shows the pulse diagram for the four devices in the series.

In the case of the WM8015 and WM8016 (3a and 3b respectively), when LATCHB is high, data is clocked into the DATA pin on each leading edge of CLK. Once all data bits have been clocked in, LATCHB is pulsed low to execute the instruction given by the last bits. CLK must be high during the negative-going transition of LATCHB. Data is entered MSB first, that is, $B_7 = \text{MSB}$.

In case of the WM8030, when LATCH is low, data is clocked into the DATA pin on each leading edge of CLK. Once all data bits have been clocked in, LATCH is pulsed high to transfer the data from the serial input register to the selected DAC. Data is entered MSB first.

DACs A, B and C have a configurable output buffer. When the feedback pin (FBA, FBB, FBC) is disconnected, the output amplifier acts as a unity gain buffer. When the feedback pin is linked to ground, the amplifier becomes a ×2 gain stage. The output buffer of DACD is not programmable and is permanently configured as a ×2 gain stage.

[950079]

CORRECTION

Application note 8-bit non-volatile digital-to-analogue converters (DACs) (September 1995)

Figure 3d on p. 24 is incorrect; the correct one is illustrated here. We apologize for any inconvenience caused.

ELEKTOR ELECTRONICS OCTOBER 1995

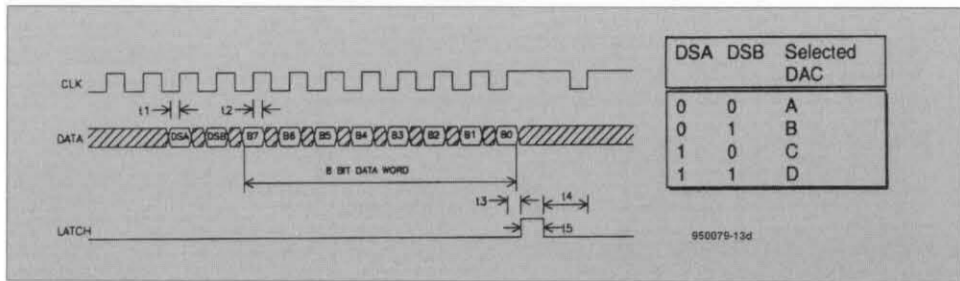


Fig. 3d

DONGLE SAFE

A dongle is a small plug-in device which must be attached to your computer's printer port to be able to run a certain program. Over the years, the dongle has been recognized as one of the most efficient ways of protecting software against illegal copying. Not surprisingly, a (personalized) dongle is supplied with many high-end CAD and DTP programs. These programs look constantly for the dongle, and often will not run at all if it is not fitted. Dongles are generally considered precious objects, but, unfortunately, not only by their rightful owners...

OVER the past few years, various techniques have been devised to combat illegal copying of computer software. In a constant effort to protect its products, the software industry has shown lots of activity in finding a copy protection system which gives a minimum of fuss to the licensed user. The

dongle, probably first used on Commodore-64 computers, has proven to be one of the most effective and least cumbersome protection systems available. And yet, the device has one important disadvantage. Simply because it is so difficult to 'hack' or 'clone', the dongle itself has become an interesting object to steal. Unfortunately, anyone who has a small

screwdriver can remove a dongle from a PC in a few seconds. What's more, because the dongle usually has a sticker on it proclaiming the name of the program it belongs to, it will have a high value on the black market.

The dongle safe presented in this article was designed as a simple, low-cost means of giving extra security and peace of mind to dongle owners. In effect, the safe makes stealing your precious dongle a lot harder, and makes casual theft almost impossible. The basic idea is simply to hide the dongle from sight. That is achieved with the aid of an insertion card into which a number of dongles can be plugged. Because the insertion card with the dongle(s) on it is fitted inside the computer, it is not immediately obvious to an outsider that a dongle is being used. Computer criminals on the hunt for a specific type of dongle will only be able to find it by opening the computer, which takes rather more time than simply pilfering the device from the parallel port at the back of the computer.

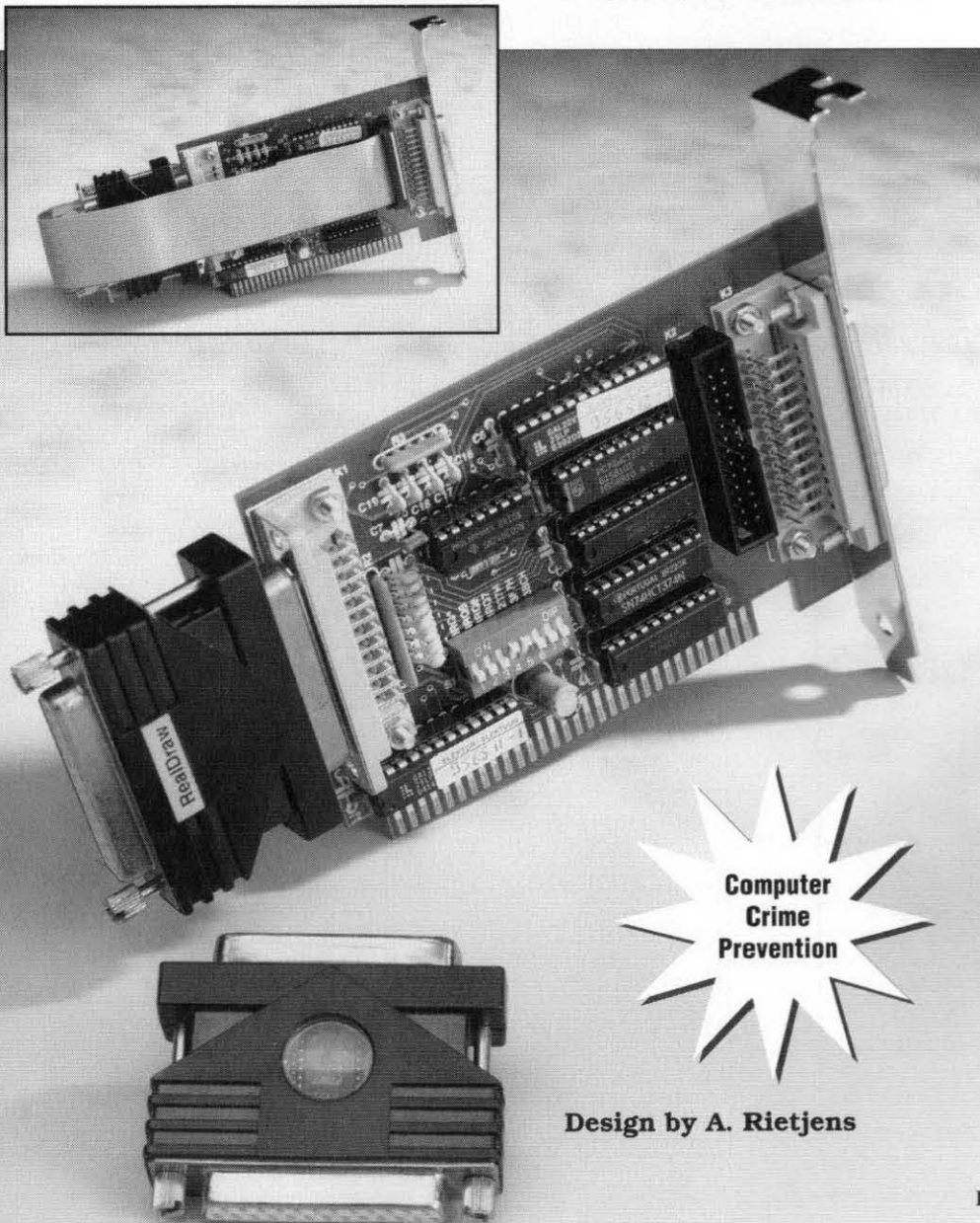
The dongle safe has two additional features. First, the printer port implemented on the insertion card may be connected to a socket on the card fixing bracket, via a short length of flat-cable connected to the last dongle. That is only possible, however, if the dongle is suitable for connecting between the Centronics port and the printer. Unfortunately, some dongles cause problems if that is done in combination with other dongles.

The second additional feature of the dongle safe is its ability to act as an add-on parallel input port. Data applied to the inputs is then directly accessible to the CPU via the databus. This is a feature not offered by a conventional printer port.

A simple approach

Dongles are generally connected to the PC's parallel printer ('Centronics') port. Three base addresses are reserved for this port: 3BCH, 278H and 378H. Printer port logic may be located at each of these addresses. The block diagram of a printer port is shown in **Fig. 1**. The function of the address decoder will be obvious: apart from fixing the base address, it also determines the addresses of the various printer port registers. The PC's databus is buffered via a bidirectional bus transceiver to prevent undue loading.

To be able to control a printer, you need a number of control signals such as strobe and init. The control levels



Design by A. Rietjens

for these lines are switched with the aid of a register. For the purpose of checking, the levels of these lines may be read back via another register.

While it is busy printing, the printer returns status information to the computer. The main signals used for this information exchange are Paper Empty (PE), Acknowledge (ACK) and Busy. The computer reads back this information via the status register.

The process of sending data to the printer operates as follows. First, the data to be transmitted is copied into the write register, whereupon a strobe pulse is generated. For checking purposes, the data can be read back from the write register. Usually, the write register is a buffered latch, so that data is continuously present at the output. This arrangement unfortunately does not allow an output to be used as an input. None the less, the I/O controller used here allows the data register to be switched to high-impedance mode. If this is done, the data register no longer affects signals which are being read. Those of you keen on experimenting may want to write their own software to give extra functionality to the port. Normally, however, you will not notice this option because after a reset the computer automatically arranges for all control signals to be given levels which select 'normal' printer port operation.

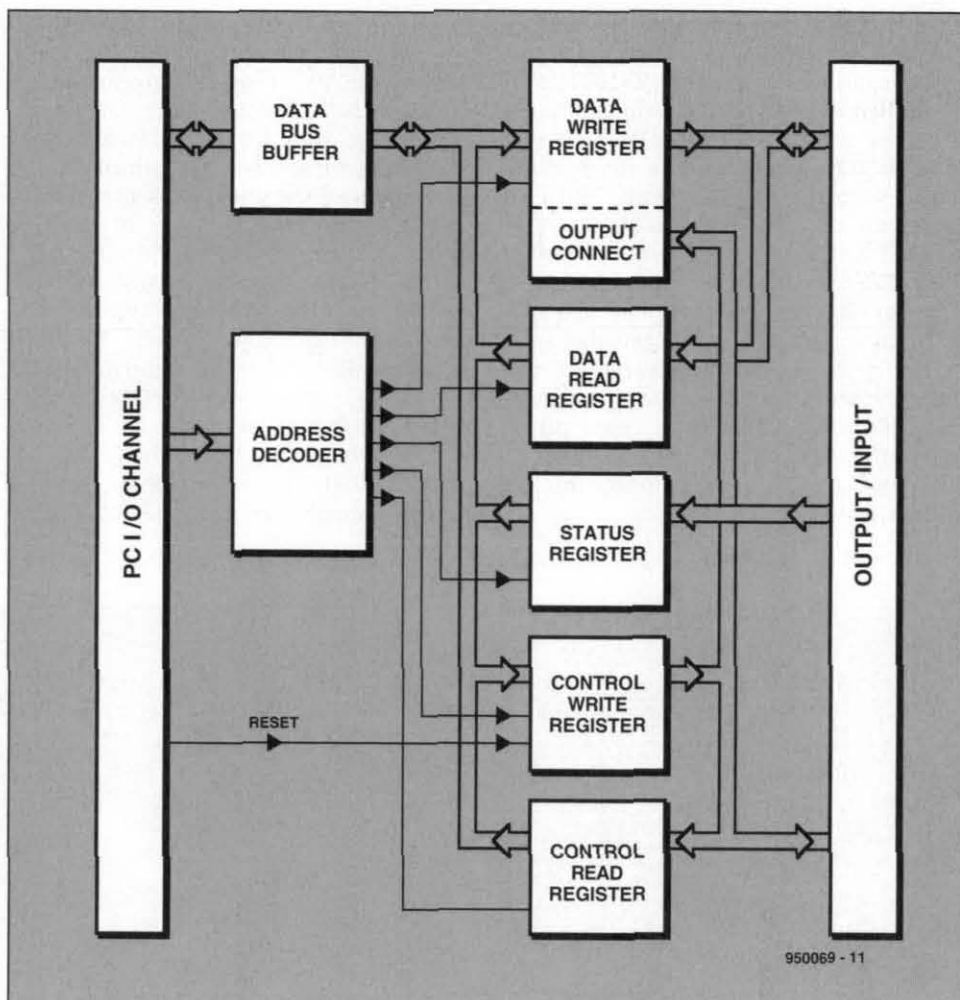


Fig. 1. This block diagram shows the architecture of a printer port in an MS-DOS PC.

Hardware

A number of points which have been made in the previous description are immediately apparent from the circuit diagram in Fig. 3. Although the schematic may look complex at first because of the large number of connectors, it is really quite simple and easy to follow.

The data register is connected directly to the PC's databus, and is formed by IC₁, a type 74HCT245. The data-write register, IC₃, (a type 74HCT374) contains the data to be printed. The output signals of this IC

Base address	R/W action	Effect
+0	write	write data to printer
+0	read	read data from printer's databus
+1	read	read printer status
+2	write	write control word to printer
+2	read	read control word for printer
+3	write	not allowed
+3	read	not allowed

Table 1. Overview of reserved addresses around the base address of the dongle safe card.

```

C:\>debug
-d 0:400
0000:0400  F8 03 F8 02 00 00 00 00-78 02 BC 03 00 00 F1 4B  .....x.....K
0000:0410  63 44 BF 80 02 00 00 00-00 00 30 00 30 00 0D 1C  cD.....0.0...
0000:0420  64 20 20 39 30 0B 3A 27-34 05 30 0B 30 0B 0D 1C  d 90.: '4.0.0...
0000:0430  73 1F 0D 1C 64 20 65 12-62 30 75 16 67 22 00 00  s...d e.b0u.g"..
0000:0440  6F 00 C0 00 00 00 00 00-00 03 50 00 00 10 00 00  o.....P.....
0000:0450  00 08 00 00 00 00 00 00-00 00 00 00 00 00 00 00  .....
0000:0460  07 06 00 D4 03 29 20 88-05 87 90 00 8E EC 0D 00  .....) .....
0000:0470  00 00 00 00 00 01 00 00-14 14 14 14 01 01 01 01  .....
-q
C:\>
    
```

Fig. 2. The DOS program DEBUG gives you an instant overview of the addresses in use for printer (and COM) ports.

go directly to the output (K_1), and is also applied to the inputs of the data-read register, IC_4 (a type 74HCT245). The outputs of IC_3 are connected to an array of pull-up resistors, which ensure steady levels on the lines PD0-PD7 when IC_3 is switched to high-impedance ('three-state'). The control register, IC_5 , consists of a 74HCT273, and really acts as a kind of director in the circuit. The signals transmitted by the circuit (strobe, init, select and auto) are protected via buffer with open-drain outputs (74HC05). IC_5 receives a reset pulse via buffer IC_{7e} when the computer is switched to the start configuration after a 'hard' reset.

The address decoder in the dongle safe is built around IC_2 , a GAL type 20V8. The two read registers (status and control) also take the form of a GAL, only this time the larger type 22V10 is used. The programming descriptions of the two GALs are shown in the box opposite. Those of you not in possession of a GAL programmer will be pleased to know that the two GALs are also available ready-programmed through our Readers Services. The addresses determined by the GALs, and the associated functions, are listed in **Table 1**. The two address decoding functions are realized by GALs because these components reduce the component count

and thus the board space. In effect, they enable the circuit to remain as compact as possible.

The switches in DIL switch block S_1 may be used to select the card address (278_H, 378_H or 3BC_H), as well as the desired interrupt line (IRQ3, IRQ4, IRQ5 or IRQ7). The most obvious choice for the printer port is IRQ5 or IRQ7. The other two, IRQ3 and IRQ4, may also be used, provided they are not already in use by a communication (COM) port. Check to make sure!

Construction

The artwork for the dongle safe insertion card is shown in **Fig. 4**. The card

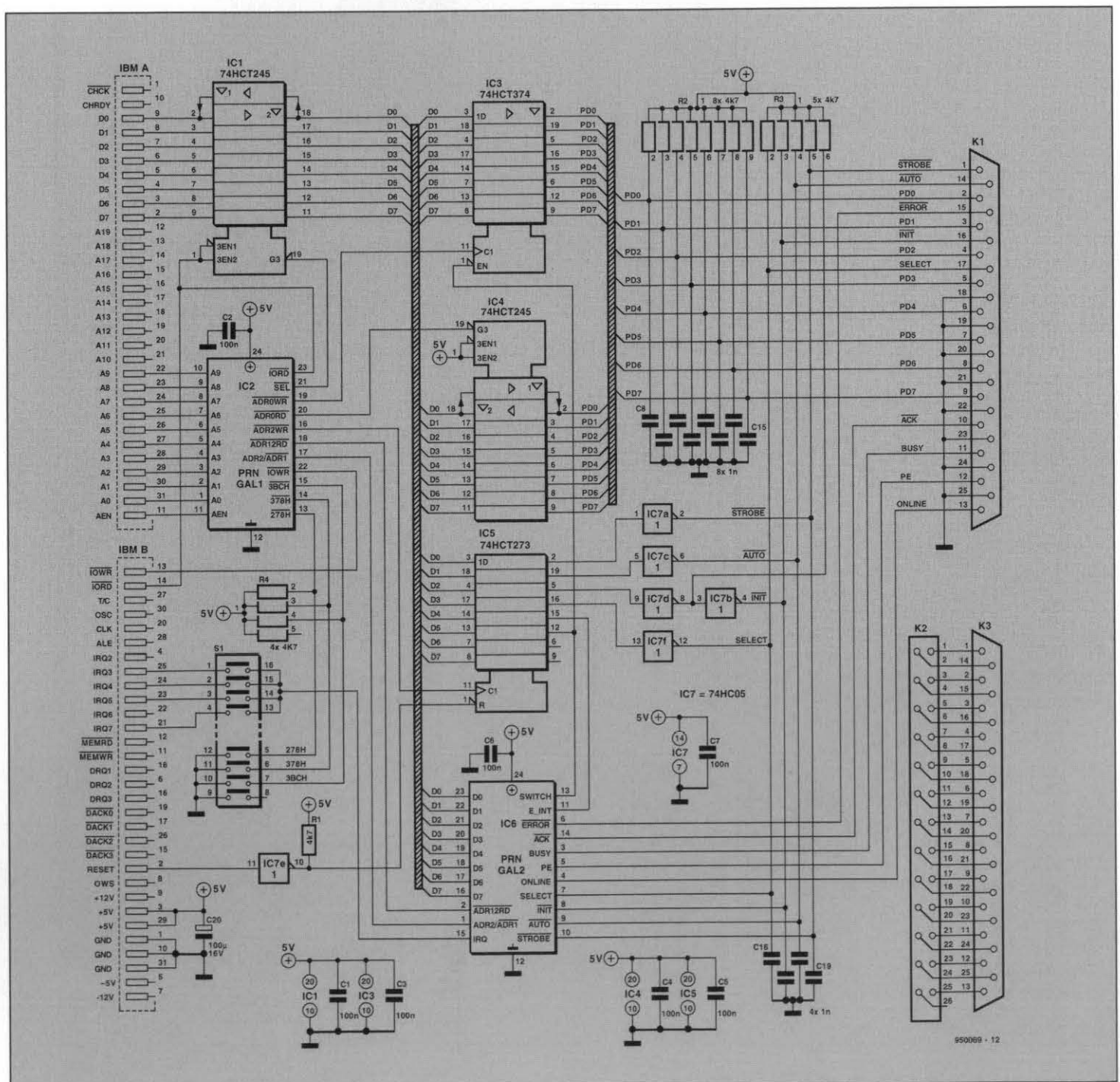


Fig. 3. Circuit diagram of the dongle safe card. The card allows dongles to be housed inside the PC, where they are much safer from theft.

is double-sided and through-plated, and the one supplied through the Readers Services comes with gold-plated PC extension bus connections. Those of you with access to a GAL programming system may burn their own GALs for the project with the aid of the listings on the previous page. Do pay attention to the inverting marks in the equations. Fortunately, these two ICs are also available ready-programmed through our Readers Services.

Boxheader K_2 and connector K_3 may be omitted if you do not wish to use the option of connecting the output of the last dongle to an extra port. If you do want the extra port, that can be created by making a short cable, consisting of a short length of 25-way flatcable. One end is fitted with a 25-way IDC style (press-on) sub-D plug, the other, with a 26-way boxheader (also IDC style). Pin 26 of this header is not used. The connection via the cable is laid out so that it is not necessary to twist the cable at one of the ends. Pin 1 of K_1 is connected to pin 1 of K_2 .

Setting up and testing

Before you install the completed card into your computer, run a check on the addresses already in use for printer ports. Most of today's PCs (i.e.,

COMPONENTS LIST

Resistors:

- $R_1 = 4k\Omega$
- $R_2 = 4k\Omega$ 8-way SIL array
- $R_3 = 4k\Omega$ 5-way SIL array
- $R_4 = 4k\Omega$ 4-way SIL array

Capacitors:

- $C_1 - C_7 = 100 \text{ nF}$
- $C_8 - C_{19} = 1 \text{ nF}$
- $C_{20} = 100\mu\text{F}$ 16 V radial

Semiconductors:

- $IC_1, IC_4 = 74\text{HCT}245$
- $IC_2 = \text{GAL}20\text{V}8$ (order code 956511-1)
- $IC_3 = 74\text{HCT}374$
- $IC_5 = 74\text{HCT}273$
- $IC_6 = \text{GAL}22\text{V}10$ (order code 956512-1)
- $IC_7 = 74\text{HC}05$

Miscellaneous:

- $K_1, K_3 = 25\text{-way}$ angled D socket, PCB mount.
- $K_2 = 26\text{-way}$ boxheader.
- $S_1 = 8\text{-way}$ DIP switch.
- PC card fixing bracket with hole for D25 connector.
- PCB and GALs: set order code 950069-C (see page 70).

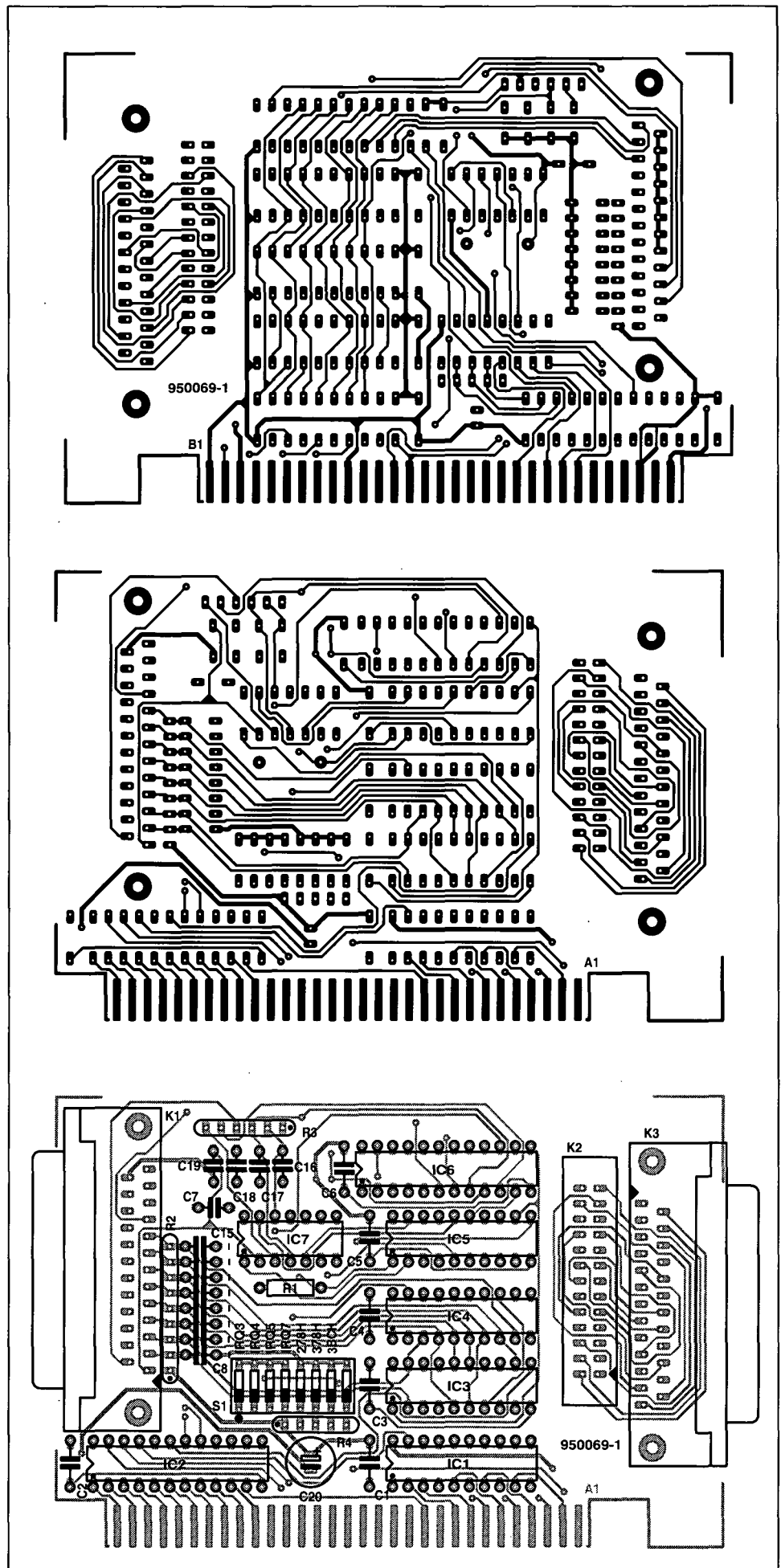


Fig. 4. Copper layouts and component mounting plan of the double-sided through-plated printed circuit board designed for the dongle safe card (board available ready-made through the Readers Services, see page 70).

The two GALs on the dongle safe card

The first GAL to be examined in greater detail here is address decoder IC₂.

The structure of the programmed GAL is straightforward, as illustrated below. The three possible port addresses, 3BC_H, 278_H and 378_H are decoded by three AND gates, and combined into a single selection signal by an OR gate. Next, this selection signal is combined with the lowest address bits (A0 and A1) and the read and write signals (IOR and IOWR). These signals are used to give access to all registers. Because the status and control registers are combined in hardware, a single control signal is created for these functions. The ADR2/ADR1 signal does the final selection between these two registers.

The above structure results in a fairly simple file for the GAL programmer. The command and file format is compatible with the Opal Junior software which is supplied with the *Elektor Electronics* GAL programmer. The listings allow anyone with access to this programming system to burn his/her own GALs for the project.

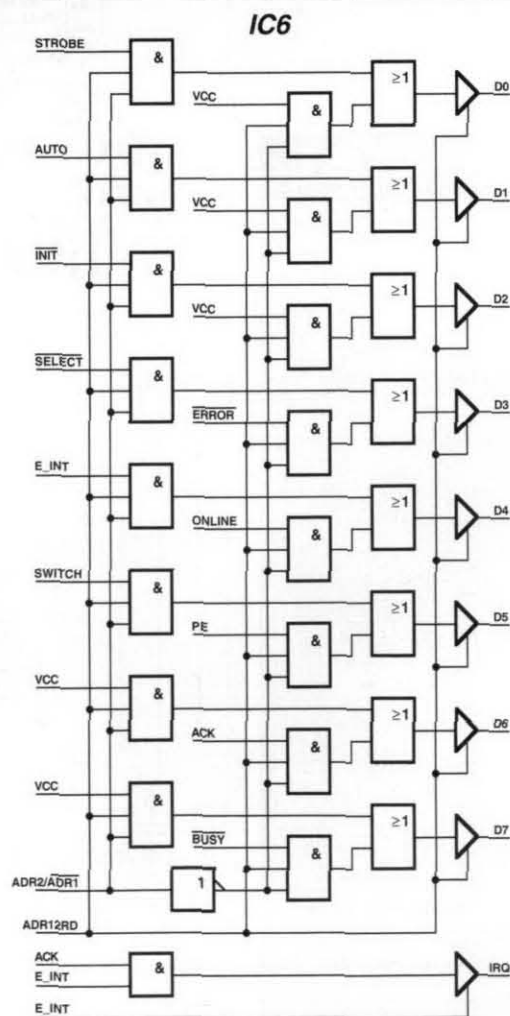
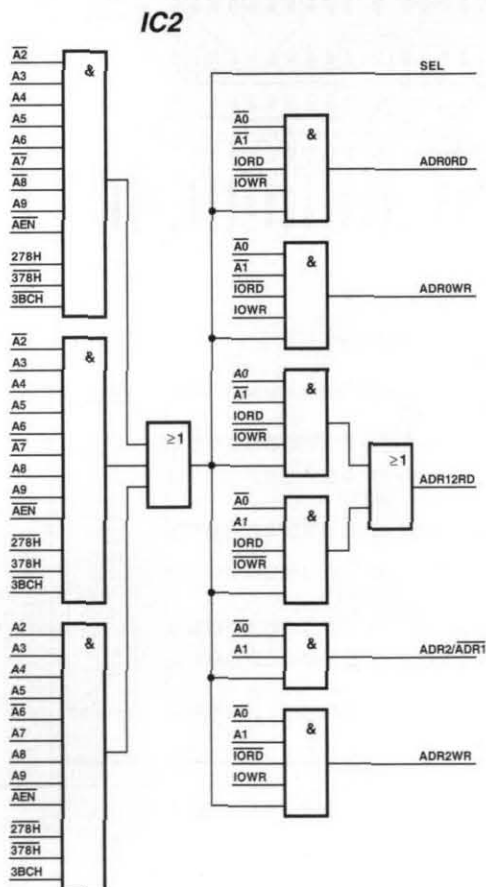
The first few lines of the programming file provide some information on the GAL to be produced. The command CHIP is used to indicate the GAL type to be used, in this case, a 20V8. Next, a logic name is assigned to each pin of the GAL, observing the active level (low or high) of the relevant pin. This makes writing the Boolean equations a lot easier. Because the 'define' instructions described in the next few lines may be inserted in the equations, they too help to make the equations easy to follow.

The mechanism so programmed in the GAL defines the three base addresses as well as the read and write conditions, and makes setting up the final equations very easy indeed.

Status and control registers

The contents of IC₆, the second GAL in this project, is also shown in the box below. This GAL simulates the status and control register. The selection logic is used to choose between one of two AND gate banks. The level of the ADR2/ADR1 line determines which set of AND gates is used. A high level enables the 'control' signals to be passed, a low level, the 'status' signals. As soon as the ADR12RD read signal becomes active, the information appears. In addition to the two previously mentioned registers, the GAL also contains the interrupt enable (E_INT) decoding logic.

The programming file for this GAL is largely similar to that for IC₂. However, a 22V10 is used in lieu of a 20V8 because nine outputs are required. New in the programming file are the **.OE instructions which determine when the outputs may be switched through. Like the file for IC₂, this programming instruction is compatible with the software supplied with the *Elektor Electronics* GAL programmer.



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486s and up) have a BIOS which displays this information as the system starts up. If you find that all three addresses are in use already, one of these ports will have to be disabled. If you don't, bus conflicts are sure to occur if you insert the dongle safe card.

If you have a computer with an older BIOS, the printer port address information may be obtained with the aid of the DOS command DEBUG. **Fig. 2** shows a screendump which illustrates how the required addresses may be read from the system's internal software.

Once a port address is selected, set the card address correspondingly with the aid of the DIP switches. Insert the card into the PC, and switch on the PC. The basic check on the dongle safe is to see if the BIOS (or DEBUG) reports a card present at the selected address. In principle, this test is sufficient. For an extensive test of all available registers, however, use the BASIC program given in **Fig. 6**. Look carefully at lines 40, 50 and the subroutine starting at line 1000. These lines have been added to freeze the contents of the registers, and return them to their original state when the program is ended. This is necessary because the BIOS uses shadow registers to keep track of the LPT registers. Because BASIC bypasses the BIOS to

Programming file for GAL IC2

Address decoder for printer port (IC2)
National Semiconductor OPAL Junior Example

```
CHIP address_printerport GAL20V8

;define pin layout for the GAL

A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 AEN GND
/H278 /H378 /H3BC /ADR2WR ADR2_ADR1
/ADR12RD /ADR0WR /ADR0RD /SEL /IOWR /IORD VCC

;define product terms for each printer port address

;define offsets

@define ADR0  "/A1*/A0"
@define ADR1  "/A1* A0"
@define ADR2  " A1*/A0"

;define address selection for LPT1...LPT3

@define LPT_A  " A9* A8*/A7* A6* A5* A4* A3*/A2*/AEN* H378*/H278*/H3BC"
@define LPT_B  " A9*/A8*/A7* A6* A5* A4* A3*/A2*/AEN* H278*/H378*/H3BC"
@define LPT_C  " A9* A8* A7*/A6* A5* A4* A3* A2*/AEN* H3BC*/H378*/H278"
@define READ   " IORD*/IOWR"
@define WRITE  "/IORD* IOWR"

EQUATIONS

;addresses reading address offsets 1 and 2 are combined to allow output
;enabling for the second GAL with ADR12RD signal
;ADR2_ADR1 selects if the read is directed to address offset 1 or 2

SEL      = LPT_A + LPT_B + LPT_C
ADR0RD   = LPT_A * ADR0* READ + LPT_B * ADR0* READ + LPT_C * ADR0* READ
ADR0WR   = LPT_A * ADR0* WRITE+ LPT_B * ADR0* WRITE+ LPT_C * ADR0* WRITE
ADR12RD  = LPT_A * ADR1* READ + LPT_B * ADR1* READ + LPT_C * ADR1* READ +
          LPT_A * ADR2* READ + LPT_B * ADR2* READ + LPT_C * ADR2* READ
ADR2_ADR1 = ADR2
ADR2WR   = LPT_A * ADR2* WRITE+ LPT_B * ADR2* WRITE+ LPT_C * ADR2* WRITE
```

Programming file for IC6

Register decoder for printer port (IC6)
National Semiconductor OPAL Junior Example

```
CHIP register_printerport GAL22V10

;define pin layout for the GAL

ADR2_ADR1 /ADR12RD BUSY ONLINE PE /ERROR
SELECT /INIT /AUTO /STROBE E_INT GND
SWITCH /ACK IRQ D7 D6 D5 D4 D3 D2 D1 D0 VCC

EQUATIONS

;The register output is enabled when a read of offset address 1 or 2 occurs
;thus enabling bits D0...D7

D0.OE = ADR12RD
D1.OE = ADR12RD
D2.OE = ADR12RD
D3.OE = ADR12RD
D4.OE = ADR12RD
D5.OE = ADR12RD
D6.OE = ADR12RD
D7.OE = ADR12RD

;The contents of of the bits depends on which offset address is selected
;which is determined by the level the ADR2_ADR1 input: zero selects offset
;address 1 and one selects offset address 2

D0 = ADR12RD* /ADR2_ADR1* VCC      +ADR12RD* ADR2_ADR1* STROBE
D1 = ADR12RD* /ADR2_ADR1* VCC      +ADR12RD* ADR2_ADR1* AUTO
D2 = ADR12RD* /ADR2_ADR1* VCC      +ADR12RD* ADR2_ADR1* /INIT
D3 = ADR12RD* /ADR2_ADR1* /ERROR  +ADR12RD* ADR2_ADR1* /SELECT
D4 = ADR12RD* /ADR2_ADR1* ONLINE  +ADR12RD* ADR2_ADR1* E_INT
D5 = ADR12RD* /ADR2_ADR1* PE       +ADR12RD* ADR2_ADR1* SWITCH
D6 = ADR12RD* /ADR2_ADR1* /ACK    +ADR12RD* ADR2_ADR1* VCC
D7 = ADR12RD* /ADR2_ADR1* /BUSY   +ADR12RD* ADR2_ADR1* VCC

; The IRQ output is tristate when interrupts are not allowed
; An interrupt can be generated if an acknowledge signal is received

IRQ.OE =E_INT
IRQ = E_INT*ACK
```

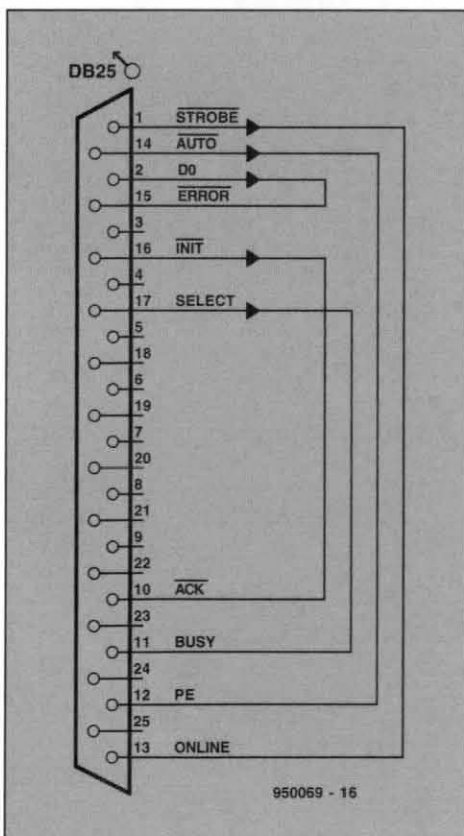
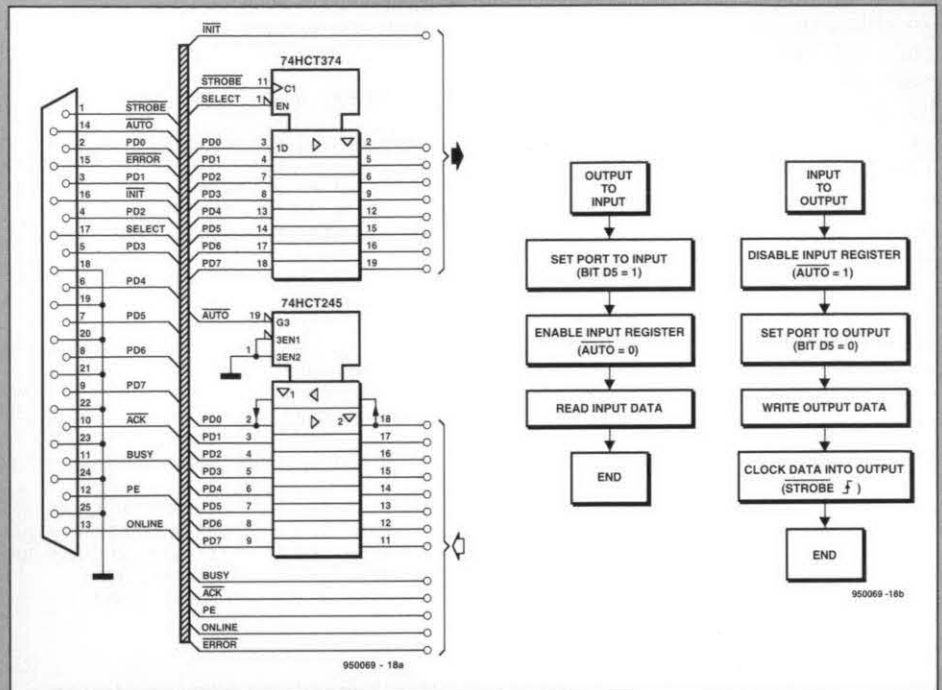


Fig. 5. The BASIC test program requires this simple loopback connector. The plug is compatible with the one that comes with Checkit.

Other applications

As described earlier in this article, the dongle safe card may also be used as an advanced I/O port. The circuit diagram shown here indicates how the extra hardware may be connected. An essential point to look after is the prevention of two outputs short-circuiting each other. Hence, the outputs of the 74HCT245 are switched to high impedance mode ('three-state') after a system reset (output Auto=high). Because Auto goes high during the hardware reset, fault conditions (outputs A0-A7 on outputs PD0-PD7) can not arise as a result of a software reset.

The two flow charts alongside the circuit diagram show the required software structure. The left-hand flowchart shows how to use the output as an input. First, the port is set up as an input (bit 5 of IC₅ is made logic high). Next, output Auto is pulled low (Q8 of IC₅). Finally, information is requested via buffer IC₄. The right-hand flowchart shows how data is written. First, all inputs have to be disabled by making Auto logic high (Q8 of IC₅). Next, the port is set up as an output device by making D5 of IC₅ logic low. Next, write data to IC₃, and generate a strobe pulse by putting a short pulse on Q1 of IC₅. If you write your own software to implement this I/O function, errors can be avoided by keeping strictly to these two cycles.



```

10 REM ..... define base address and clear screen
20 ADDRESS = &H278 : CLS
30 REM ..... save old outputs
40 OLDDATA = INP (ADDRESS)
50 OLDREG2 = INP (ADDRESS+2)
60 REM .....data bus test
70 FOR I = 0 TO 255
80 LOCATE 2,10 : PRINT "Testing data output ";I
90 OUT (ADDRESS),I
100 IF INP (ADDRESS) = I THEN 140
110 LOCATE 4,10
120 PRINT"Error at data output test ";I
130 I = 255
140 NEXT I
150 GOSUB 1000
160 REM ..... control word test
170 FOR I = 0 TO 63
180 LOCATE 6,10 : PRINT "Testing control word output ";I
190 OUT (ADDRESS+2),I
200 IF (INP (ADDRESS+2) AND 63) = I THEN 240
210 LOCATE 8,10
220 PRINT"Error at control word test ";I
230 I = 63
240 NEXT I
250 GOSUB 1000
260 REM ..... status word test
270 FOR I = 0 TO 15
280 LOCATE 10,10 : PRINT "Testing status input with loopback connector ";I
290 OUT (ADDRESS+2),I
300 OUT (ADDRESS),0
310 VALUE = (INP (ADDRESS+1) AND 248) XOR 48
320 IF VALUE = (I*16+0) THEN 350
330 LOCATE 12,10: PRINT "Error at status word ";I*2 : I = 15
340 GOTO 390
350 OUT (ADDRESS),1
360 VALUE = (INP (ADDRESS+1) AND 248) XOR 48
370 IF VALUE = (I*16+8) THEN 390
380 LOCATE 14,10: PRINT "Error at status word ";I*2+1 : I = 15
390 NEXT I
400 GOSUB 1000
410 END
1000 REM ..... restore old output
1010 OUT ADDRESS,OLDDATA : OUT (ADDRESS+2),OLDREG2
1020 RETURN

```

Fig. 7. This BASIC program enables you to run an extensive check on the card.

change the register contents, problems may arise when a print command is given after running a test program as described here. Such problems may be prevented by returning the registers to their original values.

The BASIC program can only complete its extensive testing if a special 'loopback' test plug is connected to K₁. The wiring diagram of the test plug, which connects five outputs to an equal number of inputs, is shown in Fig. 5. As far as the layout is concerned, this wiring corresponds to that of the test plug supplied with the widely known PC test program 'CheckIt'.

If everything functions properly, connect the dongle you wish to use to the connector on the dongle safe card, and start the relevant program. The program should start immediately. If desired, create the extra printer port by attaching the flatcable. Finally, close the PC case. (950069)

COPYBIT ELIMINATOR REVISITED

Design by H. Schaake

Our February 1994 issue carried an article describing an inexpensive and straightforward circuit for eliminating the copybit from a digital S/PDIF* audio signal to enable users to copy (digitally) their own musical work many times without degradation by the SCMS**. The present article describes an updated version of that circuit, which can be used with the latest DAT, DCC and MD players.

A comparison

The integrated circuits used in digital recorders fulfil more and more functions. Even the until recently discrete S/PDIF buffer/amplifier which converts the S/PDIF signal to TTL level is integrated in modern equipment. This is a good thing, of course, since fewer ICs bring the cost, and thus the price to the consumer, down.

The original eliminator needed a TTL signal at its input, but the updated version contains a separate S/PDIF buffer amplifier. However, the design allows S/PDIF signals already at TTL level to be processed without any difficulty.

The ICs used in modern recorders are faster and run at a higher master-clock frequency than those produced only a few years ago. Nowadays, a $256f_s$ master clock is quite normal, and even $384f_s$ and $512f_s$ models are in production. Since the eliminator needs a $128f_s$ clock, a binary scaler is provided in the updated version. If a $128f_s$ clock is available in the recorder and this can be used, it should be preferred: experience shows that this enables some recorders to lock on more readily.

The present version provides a choice of using either a LOCK or an UNLOCK signal and the facility of inverting the clock if required. These options may be useful for modifying types of DAT, DCC or MD recorder that have not been considered by the designer.

The copybit indication outputs, COPYIN and COPYOU, can not only

drive LEDs directly, but may be used, if a copybit is present, as a block (=192 frames) trigger. This allows the S/PDIF signal to be inspected on an oscilloscope at or near the timing-slot position of the copybit frame.

The circuit

The circuit of the original version has been complemented with an IC (by using a MACH210 in the IC₁ position), a couple of resistors, some jumpers, and a capacitor—see Fig. 1. The MACH210 is equivalent to two MACH110s (used in the earlier version). These chips are identical as far as housing is concerned.

The operation of the updated eliminator is identical to that of the earlier version: the reader is therefore referred to the earlier article for background information, block schematic

WARNING. The information in this article is intended solely for the recording, processing and copying of private musical work. The Editor and Publishers disclaim all responsibility for its use that infringes any copyright vested in commercial compacts discs and (digital) tape cassettes.

and timing diagram.

Construction

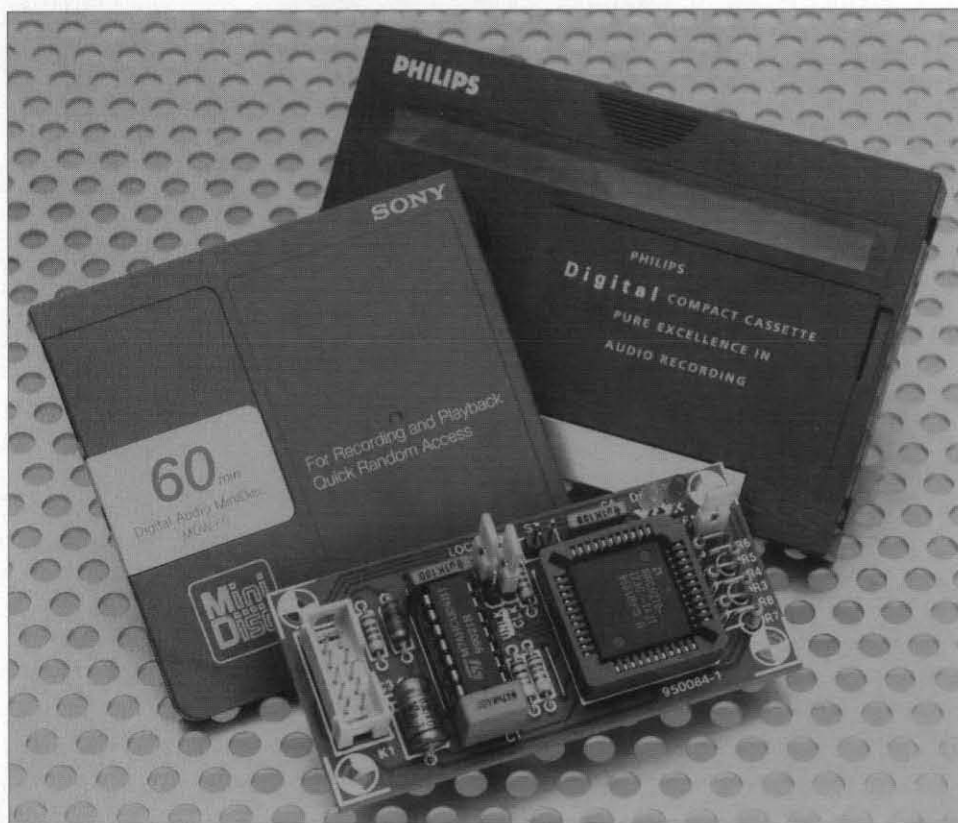
The printed-circuit board in Fig. 3 has been kept small to facilitate its incorporation into a recorder.

Population of the board is straightforward. The MACH210 is housed in a PLCC case. One of the four corners has been chamfered to indicate how the chip should be located in the relevant IC socket.

Header K₁ is signal-compatible with the earlier version.

A length of flatcable (keep this as short as possible) terminated into a 10-pin connector links the circuit with the appropriate points in the recorder.

Switch S₁ enables the eliminator to be switched on and off as required. Thus, if the eliminator is intended to be in circuit at all times, the switch



* Sony/Philips Digital Interface Format – the consumer version of the AES/EBU standard. This standard was devised by the American Audio Engineering Society and the European Broadcasting Union to define the signal format, electrical characteristics and connectors to be used for digital interfaces between professional audio products.

** Serial Copy Management System.

may be omitted.

Building into a recorder

Selecting between $\overline{\text{CLK}}$ and $\overline{\text{CLK}}$, UNLK and LOCK, and $128f_s$ and $256f_s$ is by means of jumpers. The table on the next page gives connection data for a number of modern recorders; these data may also prove useful with recorders not specified. The selection between $\overline{\text{CLK}}$ and $\overline{\text{CLK}}$ is not given; this must be determined empirically, since it depends on other connections. This involves nothing more than reversing the jumper and seeing whether the recorder locks or does not lock to the digital audio data of the eliminator.

If the connections of a particular recorder are not given, order a service manual in which these can normally be found.

A typical interconnection diagram of the signal source, the updated copybit eliminator and a digital recorder is given in Fig. 2.

Pin signals

Pin 1 (CLK). This is either $128f_s$ or $256f_s$, depending on the position of jumper 128/256. A jumper at $\overline{\text{CLK}}$ gives an inverted clock signal; at CLK, it gives a direct clock signal.

Pin 2 (UNLK). This gives the PLL lock indication. The signal must be low when the PLL is locked (jumper at UNLK). If the opposite is the case, set the jumper in position LOCK.

Pin 3 (RXOUT). The relevant track on the board is broken before or after the coaxial/optical S/PDIF input buffer, depending on the accessibility of these points in the recorder. The part of the track from the input bus or the output of the buffer is linked to RXIN and the other part to RXOUT.

Pin 4 (RXIN). See text for pin 3.

Pin 5 (REC/P). The record indication signal is connected to this pin (high level when the equipment is recording).

Pin 6 (Vcc). Supply voltage (+5 V) tapped from the recorder.

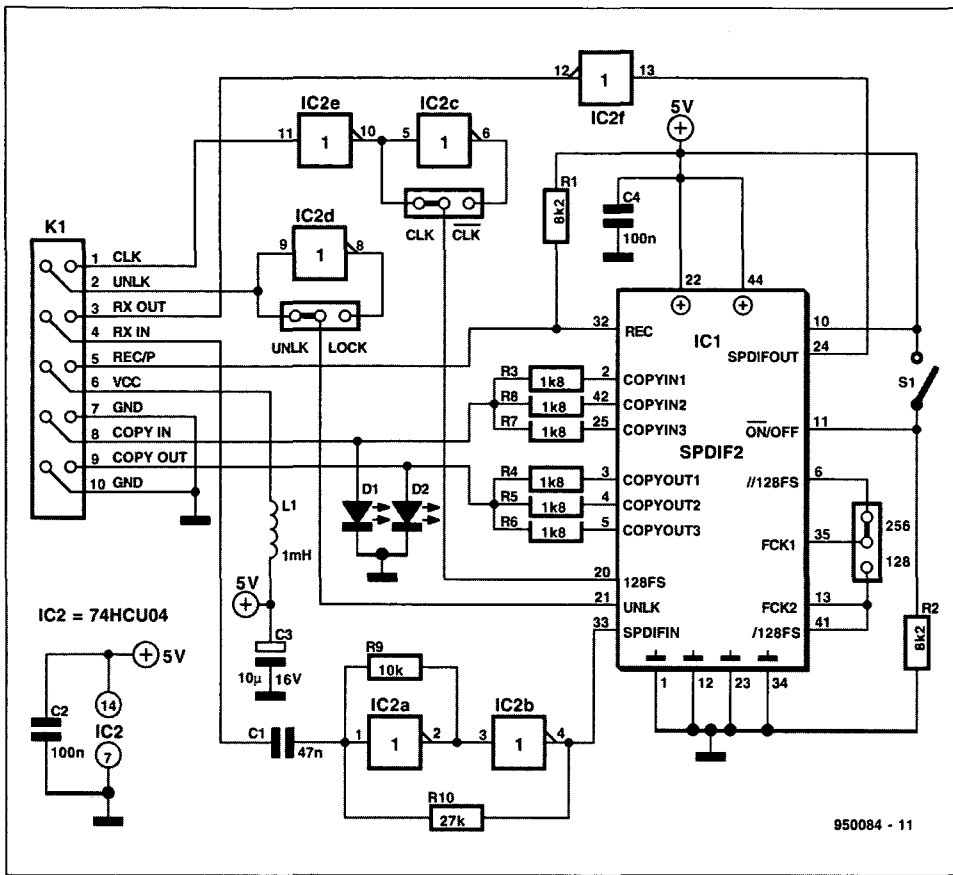


Fig. 1. Circuit diagram of the updated copybit eliminator.

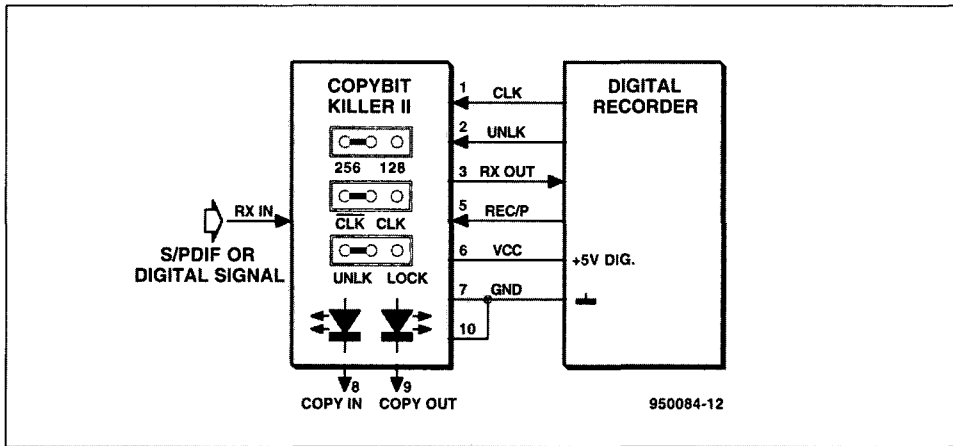


Fig. 2. Interconnection diagram of the signal source, the updated copybit eliminator and the recorder.

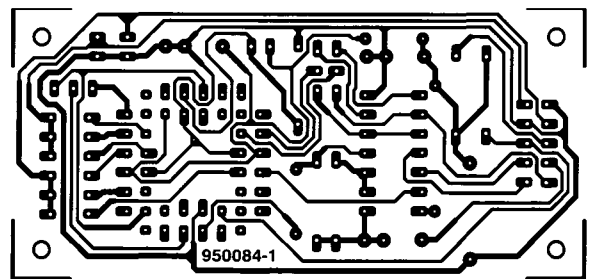
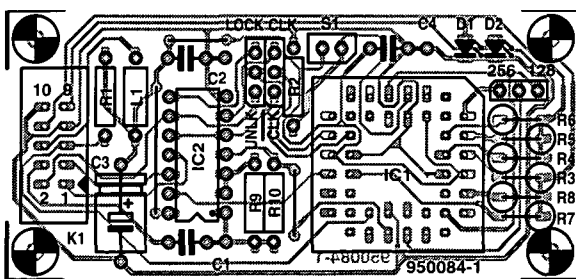


Fig. 3. Printed-circuit board for the updated copybit eliminator.

Pin 7 (GND). Link to ground of recorder.

Pins 8, 9, 10 are for connecting remotely sited LEDs. The signals may also be used as block trigger for inspecting the S/PDIF signal on an oscilloscope (only possible when the copy-bit is present in the input signal).

Parts list

Resistors:

$R_1, R_2 = 8.2 \text{ k}\Omega$
 $R_3\text{--}R_8 = 1.8 \text{ k}\Omega$
 $R_5 = 27 \text{ k}\Omega$
 $R_9 = 10 \text{ k}\Omega$

Capacitors:

$C_1 = 47 \text{ nF}$
 $C_2, C_4 = 100 \text{ nF}$
 $C_3 = 10 \mu\text{F}, 16 \text{ V}$

Semiconductors:

$D_1 = \text{LED}, 3 \text{ mm}, \text{yellow}$
 $D_2 = \text{LED}, 3 \text{ mm}, \text{red}$

Integrated circuits:

$\text{IC}_1 = \text{MACH210}$ (Order no. 956504-1†
 – see p. 70)
 $\text{IC}_2 = 74\text{HCU04}$

Inductors:

$L_1 = 1 \text{ mH}$

Miscellaneous:

$K_1 = 10\text{-way right-angle box header}$
 $S_1 = \text{switch with single make contact}$
 PCB Order no. 950084† (see p. 70)

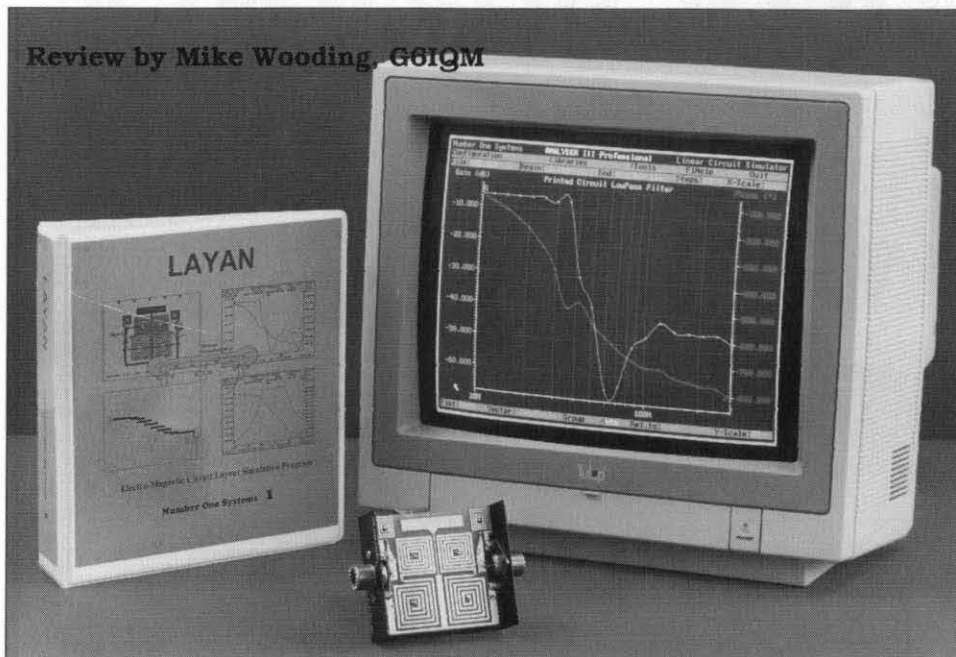
† The board and IC_1 may be ordered as a package: Order no.950084-C [950084]

K₁ pin no.	Connect in recorder to	Remarks	Jumpers on PCB
Sony MDS-101 (MD recorder)			
1 (CLK)	IC_{510} pin 21 ($128f_s$) or IC_{505} pin 6 ($256f_s$)		128 256
2 (UNLK)	IC_{103} pin 5		LOCK
3 (RXOUT)	IC_{103} pin 65		
4 (RXIN)	CNP_{103} (connector) pin 4	break track between through metallization and connector	
5 (REC/P)	IC_{111} pin 70		
6 (VCC)	CNP_{103} pin 7		
7 (GND)	CNP_{103} pin 6		
Philips DCC-900 (DCC recorder)			
1 (CLK)	Q_{441} pin 26 ($256f_s$)		256
2 (UNLK)	Q_{441} pin 9		UNLK
3 (RXOUT)	coaxial: J_{421} (connector) pin 7 optical: J_{421} (connector) pin 3	at mother board side at mother board side	
4 (RXIN)	signal side of C_{457} (150 pF)	break track to J_{421}	
5 (REC/P)	not known	link to VCC	
6 (VCC)	J_{421} (connector) pin 25		
7 (GND)	J_{421} (connector) pin 4		
Sony DTC-59ES (DAT recorder)			
1 (CLK)	IC_{307} pin 58 ($128f_s$)		128
2 (UNLK)	IC_{307} pin 31		UNLK
3 (RXOUT)	IC_{302} pin 6		
4 (RXIN)	IC_{301} pin 8	break track to this pin	
5 (REC/P)	IC_{309} pin 9		
6 (VCC)	IC_{322} pin 3	fit heat sink on to IC	
7 (GND)	chassis		
Sony DTC-690 (DAT recorder)			
1 (CLK)	R_{320} ($256f_s$)		256
2 (UNLK)	eponymous wire bridge		UNLK
3 (RXOUT)	IC_{302} pin 6		
4 (RXIN)	R_{316} at side of IC_{302}	disconnect resistor at IC_{302} side	
5 (REC/P)	not known	link to VCC	
6 (VCC)	eponymous wire bridge		
7 (GND)	eponymous wire bridge		
Sony DTC-750ES (DAT recorder)			
1 (CLK)	IC_{307} pin 58 ($128f_s$)		128
2 (UNLK)	IC_{307} pin 31		UNLK
3 (RXOUT)	IC_{307} pin 52		
4 (RXIN)	IC_{301} pin 8	break track to this pin	
5 (REC/P)	IC_{309} pin 8		
6 (VCC)	IC_{322} pin 3	fit heat sink on to IC	
7 (GND)	chassis		

Connections between K_1 and relevant points in various recorders.

LAYAN — an Electromagnetic Circuit Layout Simulation Program

Review by Mike Wooding, G6IQM



HAVE you ever designed a printed circuit board for a project, especially a high-frequency RF one, only to find that when you have built the circuit it does not perform entirely as predicted? Even if you use circuit simulation software, such as Analyser III™ or Pulsar™ to test your design and then use Easy-PC Professional™ to produce the PCB design, you could still find that there are some undesired products or spurious signals produced, or simply that the circuit does not work as predicted, or even not at all!

What is the answer to this dilemma? and one that will neither cost you an arm

or a leg, nor endless hours of re-design work? LAYAN from Number One Systems is the answer to your problem.

The problem?

The problem that is very often encountered when designing PCB's for RF circuits, is the inability to determine the effects that any inductive and capacitive coupling between the PCB tracks, component pads, stripline components and the ground plane, will have on the performance of the circuit. Even sophisticated software simulation packages are generally unable to determine what effects

these stray couplings may have. The higher the frequency then the more important is the selection of suitable materials, thicknesses and types of surface coating, for the PCB material itself. It is then still very much 'white man's magic' to accurately determine the effects of inter-component coupling, without making lots of prototypes, which entails lots of associated testing and a great deal of expensive time.

With LAYAN, however, comes an extremely powerful software package that enables simulation of the complete circuit, including all the parasitic resistances, inductances and both inductive and capacitive couplings introduced into a circuit by the board or thick/thin film layout on which it is assembled.

LAYAN

LAYAN from Number One Systems integrates fully with their Easy-PC professional XM and Analyser III Professional software packages, in fact it cannot run without them. The result is a complete circuit layout simulation system. The package is a data extraction program that converts physical information provided by Easy-PC Professional XM into a netlist in Analyser III format. All the parameters required by the program, such as the substrate thickness and dielectric constant, the distance from the ground plane, etc., are entered into the 'PCB Simulation' drop-down menu within EASY-PC Professional XM. When the 'Simulate' command is chosen from this same menu, an automatic sequence is set in motion that launches LAYAN, builds a complete netlist including the parasitic components, and finally runs Analyser III. The transfer of data between the programs is completely automatic and requires no intervention on the part of the user. On completing the simulation and reviewing the results displayed by Analyser III control returns directly to Easy-PC Professional.

LAYAN will simulate PCB's with up to two conductor layers with close or distant ground-planes. The program extracts layout resistive, capacitive, inductive and mutual parasitics, it models skin effects and loss tangents, allows simulation of printed components and can deal with any substrate, such as printed circuit board, thick film or thin film. The software also simulates the effects of tracks, component pads and feed-through components.

The hardware requirements for running LAYAN are a PC 386 or higher. However, due to the large amount of data processed and the requirement for floating point math support, a 486 DX or better is recommended. The program files themselves require 10 MB of hard drive space and additional temporary files created during simulation can require up to a further 10 MB of drive space. A VGA

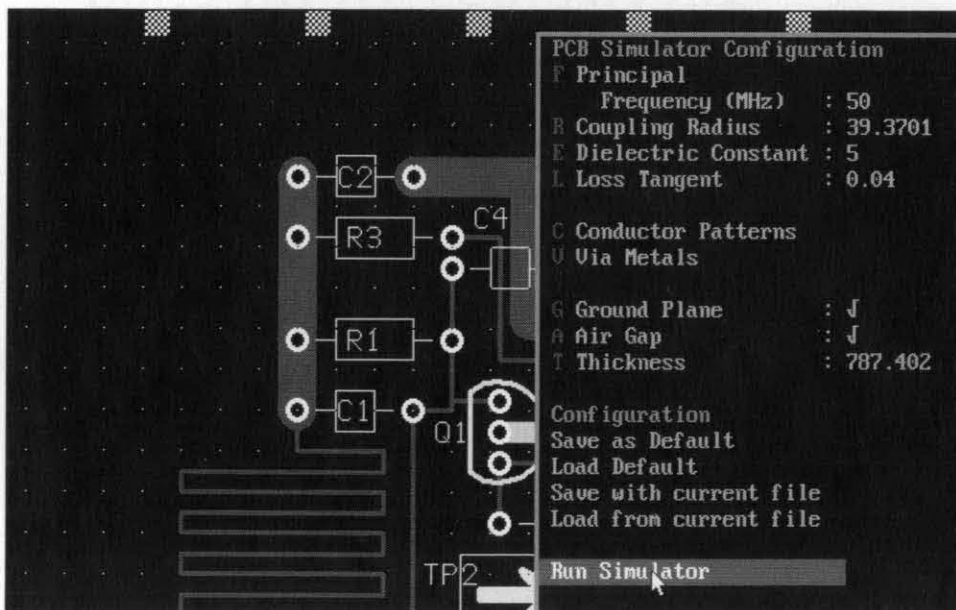


Fig. 1. Part of the example PCB to be simulated, and the Simulation Control menu.

Number One Systems		LAYAN		Layout Analyser - Bet	
Job: EX1 Determining R's, L's, M's Press (Ctrl) Q to Qui					
Layout Elements Processed		TOTAL	From Polygons		
Polygons	:	0			
Rectangular Track Segments	:	211		0	
Triangular Track Segments	:	0		0	
Circular Pads	:	42			
Rectangular Pads	:	0			
Vias	:	21			
Processing Limits					
Maximum Element Length	:	1.999 mm			
Principal Frequency	:	50.00 MHz			
Dielectric Constant	:	5.000			
Coupling Ignored Beyond	:	1 mm			
Board to Ext. Ground Plane	:	20.000 mm			
Board Thickness	:	.800 mm			
Layout Subdivision					
Elements	:	208			
Inductive Links	:	61			
Capacitive Links	:	61			
Generated Components		TOTAL	Original	New	
Resistors	:		0		
Capacitors	:		0		
Inductors	:		0		
Mutual Inductances	:		0		
Nets	:	51	6		45

Fig. 2. LAYAN reads PCB data from a netlist supplied by Easy-PC.

graphics system and a minimum of 4 MB of RAM are also required. It is also recommended that a disc caching system, such as SMARTDRV.SYS, be used.

When LAYAN is launched, by selecting 'Run Simulator' from the Easy-PC Professional menu, a netlist is built by Easy-PC which is then transferred to LAYAN. LAYAN then runs a multi-process simulation based on the netlist data and the data input by the user relative to dielectric constants, frequency range, etc. Next, LAYAN calculates simulated values for the various parasitic capacitances and inductances for the PCB, tracks, pads, etc., and produces another netlist and data table for Analyser III.

Upon completion of the calculations, Analyser III is launched and a simulation run using the modified EASY-PC netlist from LAYAN. The resulting Analyser III simulation displayed now takes account of all the effects that the PCB and its tracks, pads, etc., has on the circuit design as well as the circuit itself.

Upon exiting Analyser III, the option is given to return to EASY-PC, which, if chosen, returns you to the PCB layout display from which the simulation was run, thus allowing any necessary changes to be made prior to another simulation run.

Conclusions

LAYAN is an extremely simple package to use. As the package requires EASY-PC Professional XM and Analyser III Professional to run, the assumption must be made that the user is already conversant with these programs. Consequently, running LAYAN is totally transparent to the user, once the various parameters concerning the PCB material, etc., have been entered into the EASY-PC menu. No further user input is required and the

resultant simulation is displayed in Analyser III.

If all three packages are being used for the first time, as I have described in earlier reviews of EASY-PC and Analyser III, getting to grips with these powerful design packages is very easy, and it takes only a short time to realize their full potential as schematic and PCB design tools. LAYAN now complements the design of AC circuits and PCB's to the extent that almost all the required expensive development and testing can be carried out on your PC, without the need for actually creating a PCB and building the circuit up — only to find that it does not work as predicted.

LAYAN does not slow the system down, even though it has a lot of math to carry out. The review copy was run on my 486 DX2/66 and one of the example circuits supplied with the package,

EX1.PCB was simulated. Running under Windows™ the entire simulation took 4 min 50 sec; running under MS-DOS 6.22™ the same simulation took 3 min 10 sec. Either way, the time taken for a reasonably complex circuit, employing stripline inductors, was well worth the wait, knowing that the result of the run would be a more exact evaluation of the design's performance than without LAYAN.

For anyone working in the RF design field and already using EASY-PC and Analyser III then LAYAN is a must. For anyone working in this area and not using EASY-PC products, then I would suggest that a serious evaluation of them is undertaken. For the total cost of £935.00 plus VAT and p&p, a complete RF design software suite can be obtained, that is as versatile as anything else on the market at far times greater cost.

To purchase LAYAN on its own to add to EASY-PC Professional XM and Analyser III Professional, the cost is £495.00 plus VAT and p&p.

For those already using EASY-PC and Analyser II who wish to purchase LAYAN, but who do not already have the professional versions, upgrades are available from the suppliers.

LAYAN, Easy-PC and Analyser III are available from Number One Systems, Harding Way, St. Ives, Huntingdon, Cambridgeshire PE17 4WR; Tel.: (01480) 461778; Fax: (01480) 494042. These software packages are also available through KM Publications, Tel.: (01788) 890365; Fax: (01788) 891883.

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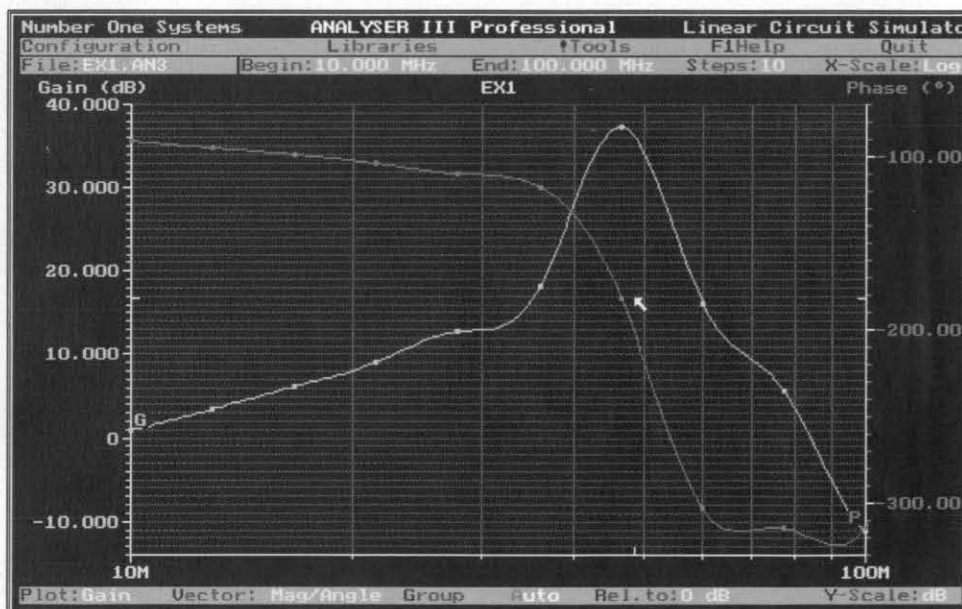


Fig. 3. At a glance: gain and phase response plots of the (example) amplifier.

HEADPHONE AMPLIFIER

Design by T. Giesberts

On much audio equipment, the headphone output is simply derived from the loudspeaker output via a series resistor: not a very elegant design! The present circuit describes a 'real' headphone amplifier that can be added to most equipment, but may also be used as a stand-alone unit.

On much audio equipment, the headphone output is simply derived from the loudspeaker output via a series resistor: not a very elegant design! The present circuit describes a 'real' headphone amplifier that can be added to most equipment, but may also be used as a stand-alone unit.

Although many audiophiles still believe discrete components are best, the relentless progress of integrated circuits can not be stopped: these devices get better and better. Even top-quality commercial equipment is now loaded with ICs and no one can doubt their quality and reliability. In many modern CD players, preamplifiers and digital-to-analogue converters (DACs) there is hardly a transistor to be found. Only the design of power amplifiers often still relies on discrete devices. The present amplifier is based on an IC: a surface mount device (SMD) Type TDA1308T from Philips Components.

The IC was developed specifically for use as a headphone driver: the enthusiastic claims of the manufacturer as to its qualities appear to be rather less exaggerated than is often the case (see opposite page: Performance). A signal-to-noise ratio of 110 dB and a distortion factor of <0.009% (with a 5 k Ω load) are undeniably good.

The IC can be used to good effect in CD players, DCC players, keyboards,

laser disc systems, multimedia amplifiers, and more. It draws a quiescent current of only 3 mA and can work from supplies of 3–7 V. The latter makes it suitable for use in either battery-powered circuits or in standard mains-operated equipment. Its dynamic range is good, its bandwidth is 5.5 MHz and its slew rate is 5 V μ s⁻¹.

The (simplified) internal design of the IC is shown in Fig. 1. The differential input stage uses MOSFETs, M₁, M₂, is provided with current mirrors and is powered by a current source, J₁. The input stage is followed by two operational amplifiers, A₁ and A₂, that drive output stages M₃ and M₆, which are also MOSFETs. The advantage of MOSFETs is that the necessary input bias current is very small: typically 10 pA; moreover, the swing of the amplifier with high impedance loads is nearly equal to the supply voltage.

The inverting and non-inverting inputs of the op amps have an excellent common mode suppression that ranges from the negative supply voltage to 1.5 V under the positive supply voltage. The IC can be fed from single as well as bipolar supplies. The closed-loop gain can be set with two external resistors.

The outputs are short-circuit-proof and totally free of switching noise. The hum suppression is 90 dB.

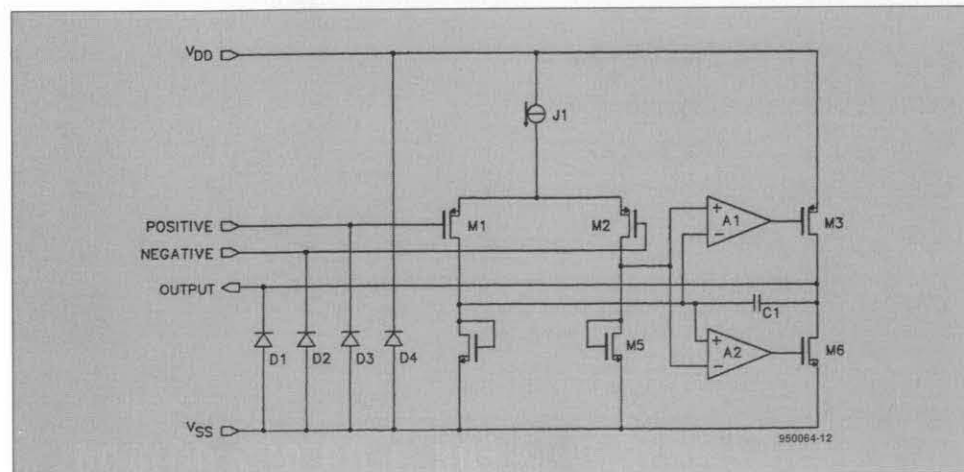
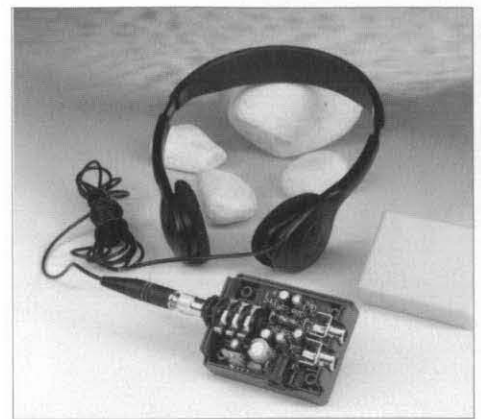


Fig. 1. Diagram of internal circuitry of the TDA1308T.



Circuit description

The circuit diagram is given in Fig. 2. Values of components are generally those recommended by the manufacturer. Power is derived from a single, standard mains adaptor, which should output at least 9 V. The adaptor output is smoothed by C₈ and regulated by IC₂. Diode D₁ protects the circuit against wrong polarity.

The input impedance is determined largely by R₂ (R₆). The value of 3.9 k Ω presents no problems to any preamplifier. The amplification factor is set by the ratio R₂:R₃ (R₆:R₇). As is seen, the factor here is unity, so that the name 'amplifier' is, strictly, a misnomer; 'driver' would have been more appropriate. There is no need for amplification, because the usual line level of 1 V (nominal) is more than enough to drive any headphone. However, a standard line output can not provide sufficient current for driving low-impedance headphones. The present amplifier remedies this.

Resistors R₉ and R₁₀, and capacitor C₅, set the IC for operation from half the supply voltage. Capacitor C₆ provides additional decoupling of the amplifier. Since the supply is asymmetrical, input capacitors C₁ and C₂ (C₃, C₄) are essential. Some audiophiles will raise their eyebrows at this, but in this application no adverse effects of these capacitors have been detected. Resistors R₁ and R₄ (R₅, R₈) make sure that these capacitors are charged even when the input and output are open.

Construction

The design has been kept as compact as feasible as can be seen from the drawings of the printed-circuit board in Fig. 4. In spite of the small dimensions, the construction is no more testing than most, at least not as far as the standard components are concerned. Soldering the surface-mount IC into place (not at the component side of the board, but at the track side as is usual with SMDs) is a tedious job. But, with patience and a small solder-

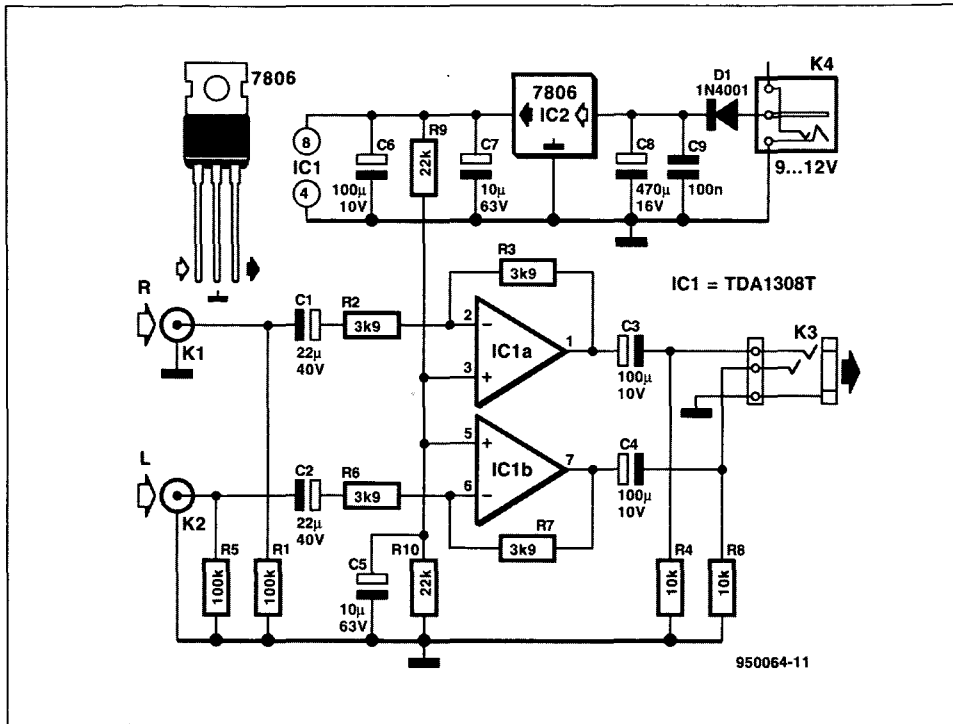


Fig. 2. Circuit diagram of the headphone amplifier.

ing iron with a fine tip, even relatively inexperienced constructors should be able to make a good job of it. Lightly tin the pads on the board and the pins of the IC and place the device in position. Take great care with the positioning of the IC: it is so small that mistakes are easily made. The side of the device where pins 1-4 are located is marked by a chamfered edge on the case. If you can not see this properly, use a magnifying glass. The chamfered edge should point in the direction of R_2 and R_3 . Since it is very small, pressing with a fingernail will do. Gently solder one of the pins into place and make sure that everything is as it should be. If so, carefully solder the other pins on to the board.

The top of the finished board is shown in the photograph in Fig. 5. Note that the various connectors are soldered directly to the board: two phono plugs for inputs K_1 and K_2 ; an adaptor socket for K_4 and a 6.3 mm stereo jack for K_3 . These connectors are, of course, required only if the amplifier is to be used as a stand-alone unit. If the amplifier is built into an equipment, the connectors can all be replaced by soldering pins from where the various connections are made. The signal lines should be in screened cable. Moreover, a mains adaptor will normally not be required, since power can invariably be derived from the main equipment: the amplifier draws only a very small current. If the voltage in the main equipment is too high, it can be dropped by a series resistor and zener diode (9 V or 12 V).

Performance

The performance of the Philips chip is typified by the distortion characteristic in Fig. 3. This shows that the THD+N is, as claimed, low: with a 1 kHz input signal at a level of 1 V and an output load of 600 Ω , the measured value was about 0.0015%. With a load of 32 Ω (Walkman-type headphones), it rose to 0.028%, which is still impressive for such a simple IC.

The channel separation measured at K_3 hovered around 90 dB with a 600 Ω load and 70 dB with a 32 Ω load (frequency range 20 Hz to 20 kHz). These values depend largely on the internal wiring of the headphones: a

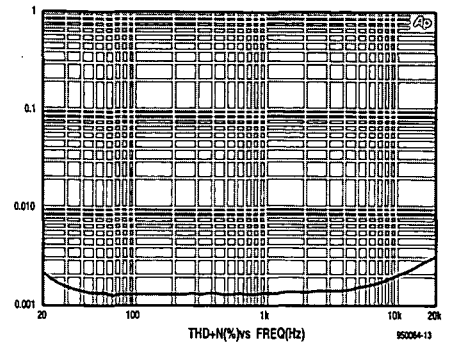


Fig. 3. The THD+N characteristic for 1 V input and a load of 600 Ω .

common earth wire leads to worse channel separation, but this can not really be attributed to the amplifier.

The maximum output voltage is 2 V r.m.s. across 560 Ω and 1.5 V r.m.s. across 32 Ω .

Parts list

Resistors:

$R_1, R_5 = 100 \text{ k}\Omega$
 $R_2, R_3, R_6, R_7 = 3.9 \text{ k}\Omega$
 $R_4, R_8 = 10 \text{ k}\Omega$
 $R_9, R_{10} = 22 \text{ k}\Omega$

Capacitors:

$C_1, C_2 = 22 \text{ }\mu\text{F}, 40 \text{ V}$, radial
 $C_3, C_4 = 100 \text{ }\mu\text{F}, 10 \text{ V}$, radial
 $C_5, C_7 = 10 \text{ }\mu\text{F}, 63 \text{ V}$, radial
 $C_6 = 100 \text{ }\mu\text{F}, 10 \text{ V}$
 $C_8 = 470 \text{ }\mu\text{F}, 16 \text{ V}$, radial
 $C_9 = 100 \text{ nF}$, pitch 5 mm

Semiconductors:

$D_1 = 1\text{N}4001$

Integrated circuits:

$\text{IC}_1 = \text{TDA}1308\text{T}$ (SMD)
 $\text{IC}_2 = 7806$

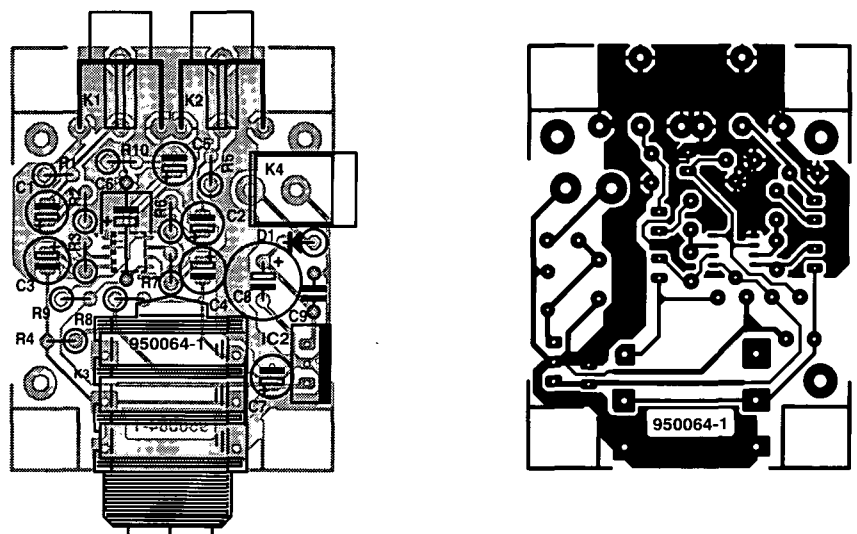


Fig. 4. Printed-circuit board for the headphone amplifier.

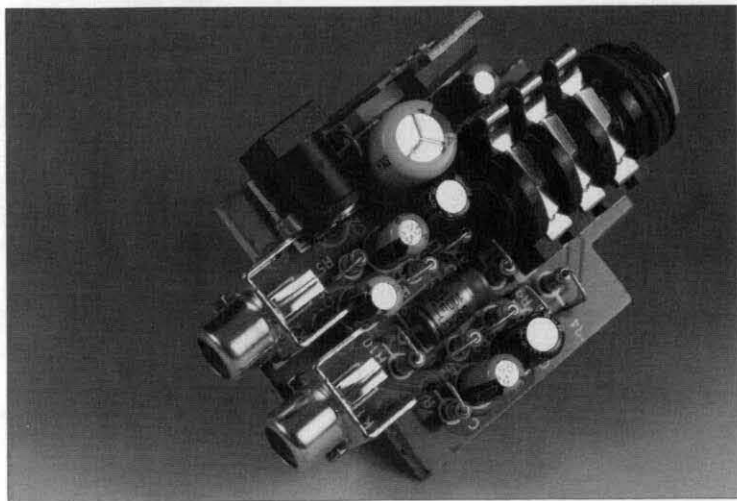


Fig. 5. The completed prototype headphone amplifier board.

Miscellaneous:

K₁, K₂ = audio socket for PCB mounting

K₃ = 6.3 mm stereo jack for PCB mounting

K₄ = Inlet for mains adaptor (for PCB mounting)

Enclosure (optional): 65×50×30 mm
(e.g., Bopla E406 from Phoenix
Mecano Ltd, 6-7 Faraday Road,
Aylesbury HP19 3RY, Great Britain.
Telephone +44 (0)1296 398855)

PCB Order no. 950064 (see p. 70)
[950064]

THE DIGITAL SOLUTION

Part 9 – Sequential logic

By Owen Bishop

In this series we look closely at digital electronics, what it is, what it does, how it works, and its promise for the future.

Whenever we apply a logic high to both inputs of a 2-input NAND gate, its output goes low. This is but one illustration of the nature of a logic gate – the output depends solely on the *present state* of its inputs, as summarized in the truth table (Table 1).

Inputs		Output
A	B	Q
L	L	H
L	H	H
H	L	H
H	H	L

H = high = 1 L = low = 0

Table 1. Truth table for NAND gates.

When we say 'present state', we are ignoring the small propagation delay of a few nanoseconds during which the effects of the input levels are transmitted through the gate to decide the output.

If two NAND gates are connected as in Fig. 65, the behaviour of the individual gates is still in accordance with the truth table, but the behaviour of the circuit as a whole displays a new aspect. The circuit has two inputs, R and S, and two outputs, Q₁ and Q₂. Suppose that both inputs are made high, and use the truth table to discover what the outputs must be. Consideration of the various possibilities leads us to Fig. 66a and Fig. 66b. The circuit is stable in either of these two states. Note that the two states are symmetrical. Are there any other stable states? Fig. 66c shows what happens if we begin with the circuit as in Fig. 66a and make input R low. This has no effect on the output of gate 1, and therefore no effect on gate 2. If we make R high again, the circuit returns to Fig. 66a. The action goes further if

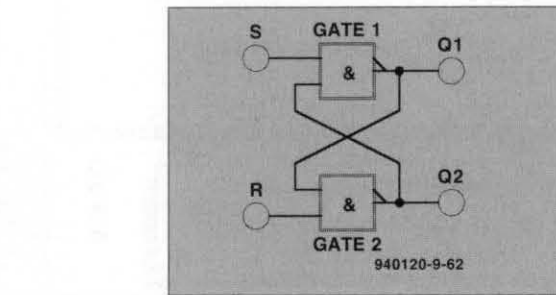


Fig. 65

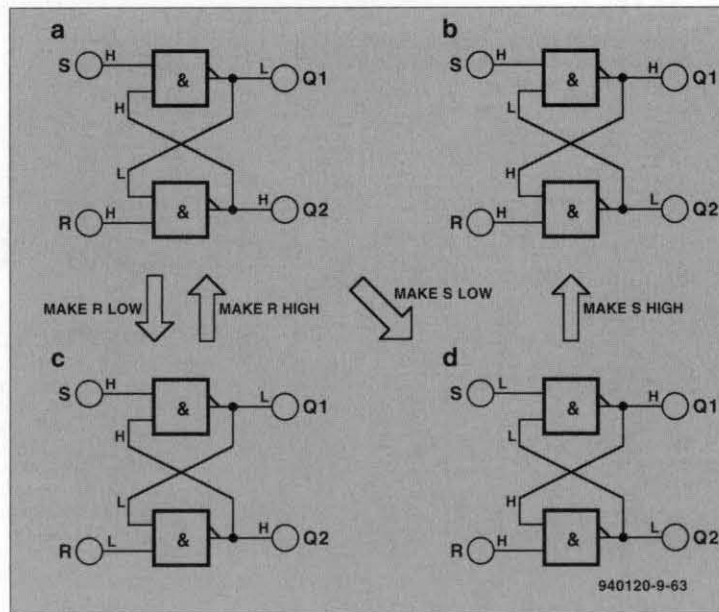


Fig. 66

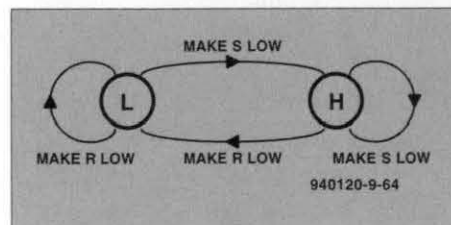


Fig. 67

we leave R high, but make S low. According to the truth table, output Q₁ must go high. This means that gate 2 now

has two high inputs, so Q₂ must become low. This gives gate 1 two low inputs, but this change does not affect Q₁,

which remains high. Having reached this state, we can let input S return to high and the circuit is now in the state shown in Fig. 66b. Even a short low pulse applied to input S in Fig. 66a makes the circuit change to the state of Fig. 66b. Since the circuit is symmetrical, we can deduce that we can make it return to the state of Fig. 66a by applying a low pulse to input R.

If both R and S are made low at the same time, both outputs go high, but this is not a stable state. As soon as the inputs are both made high again at exactly the same instant, the circuit must revert either to Fig. 66a or Fig. 66b. It is not possible to predict which state it will go to. Making both inputs low leads to an unpredictable result, so making both low is not allowed and will not be considered further.

State diagram

We summarize the action (or lack of action) of the circuit in a *state diagram* (Fig. 67). The letters in the two circles refer to output Q₁, which may be either low or high. Apart from transient states, for example, when Fig. 66a is changing to Fig. 66d, the outputs are always the reverse of each other, so we need only specify Q₁. From now on we will follow convention and refer to this output as Q, and the other one, Q₂, as \bar{Q} , pronounced 'Q-bar'. The bar indicates that \bar{Q} is, by definition, the inverse or complement of Q.

The diagram assumes that making an input high has no effect; we say that these are *active-low* inputs. The two circles in Fig. 67 indicate that the circuit has two output states, with Q low and \bar{Q} high or with Q high and \bar{Q} low. The arrows show what happens as we change S or R from high to low. The effect is the same whether we hold the input low indefinitely or simply apply a

brief low-going pulse. However, we must make the changed input high again before we try to change the other input, for it is not allowed to have both low at the same time. The diagram shows the result of making S low. If Q is low, making S low changes Q from low to high. But if Q is high, making S low has no effect. In other words, the effect of making S low depends where we are in the diagram. And where we are depends on the previous input to the circuit. The behaviour of the circuit depends not only on the input being made at a given point in time but upon the sequence of inputs, the previous input *followed by* the present input. This circuit is a simple example of *sequential logic*.

Q_n	R	S	Q_{n+1}
L	L	H	L
L	H	L	H
L	H	H	L
H	L	H	L
H	H	L	H
H	H	H	H

Table 2. State table for Figure 65.

The behaviour of the circuit can also be summarized in a *state table* (Table 2). This has a column for the present state of Q, symbolized as Q_n . Then it shows the various combinations of inputs to R and S, excluding the disallowed 'both low' inputs. On the right, it shows what the next state of Q will be, symbolized as Q_{n+1} .

Memory

The circuit of Fig. 65 has two stable states and is known as a *bistable* circuit; it is also known, particularly in North America, as a *flip-flop*. In Part 5 (Fig. 39), we described a bistable constructed from two n-p-n transistors. That circuit has essentially the same action as that in Fig. 65. The output of a bistable, whether it is constructed from transistors, logic gates or operational amplifiers, depends upon the input previously applied to it. This gives it the property essential for a

unit of memory. Figure 67 shows that a low applied to input S results in Q becoming high if it is not already high. It stores a logic high, or '1', in the bistable. We say that the bistable is *set*, and S is called the *set* input. Conversely, R is the *reset* input, making Q low, or 0.

Latches

The bistable of Fig. 65 is an example of a *latch*, because it changes to a particular state when it receives a suitable input and stays in that state indefinitely. The latch of Fig. 65 changes state as soon as a suitable pulse is received, but in logic circuits which include several latches it may be essential for them all to change state at the same time. The latch must be *gated* or *clocked*. Figure 68 shows a gated R-S latch. The latch proper consists of gates 1 and 2 and is identical to Fig. 65. But the latch is preceded by a second pair of NAND gates. Inputs R and S go to NAND gates

3 and 4. Each of these NAND gates also receives pulses from the clock. Between clocking pulses, the input from the clock is low and the outputs of gates 3 and 4 are high, irrespective of the levels on the R and S inputs. The bistable is not affected. During a clock high pulse, the output of gates 3 and 4 is the inverse of the levels on the R and S lines (see Table 1). Thus, the latch can now be triggered, but it requires a *high* on the R or S input to do this. The clocked latch is *active-high*.

We have gone into the detailed construction of simple and clocked R-S latches to illustrate the fact that sequential logic circuits are built from standard logic gates (see Test Yourself, q.1, for another example). Several other types of latch are derived from the R-S latch. One of these is the delay latch or D-type latch (Fig. 69). Note that we have followed the IEC convention by drawing the Q output as an unlabelled line, while the \bar{Q} output has a short diagonal

line to indicate that it is the complement of Q.

Data on a single line is either high or low. This applies to serial data (which, by definition, is on a single line), or to the data on one of the lines of a parallel data link. If the data is arriving along the S line, the bistable must be set when S is high and reset when S is low. The invert gate makes R high whenever S goes low, so resetting the bistable as required. If we feed the data to S and (inverted) to R as in Fig. 69, Q equals the input D as long as the clock input is high. We say that the latch is *transparent* in that state. But, when the clock input falls to low, Q becomes latched, taking the value of D just as the clock input falls, and remaining in that state until the clock goes high again.

This type of latch is useful for holding data constant while it is transferred to another circuit for subsequent processing. An example of this is found in digital audio, where an array of 16 latches reads the 16-bit parallel data from an analogue-to-digital converter (DAC). They are clocked from a single clock so that, when they latch, they hold the complete 16-bit representation of the signal voltage at that instant. This 16-bit signal is transferred to registers for further processing, then the clock goes low, followed by high to latch the next sample of the audio signal. A similar system is used in a digital multimeter where the voltage is latched every half second or so to give the user a chance to read the display before it changes to its next updated value.

Improvements

One of the problems with circuits such as that in Fig. 69 is that when D changes, S changes instantly, but there is a delay while the signal passes through the invert gate to input R. Thus, when D changes from low to high, there is an instant when both S and R are low, which is a disallowed state with unpredictable outcome. To avoid this situation, most latches are built on the *master-slave* principle, as shown in the

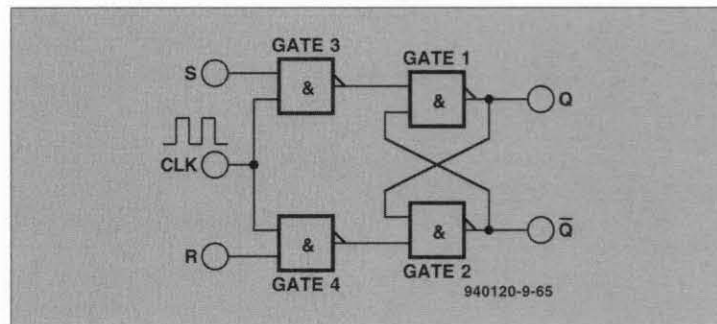


Fig. 68

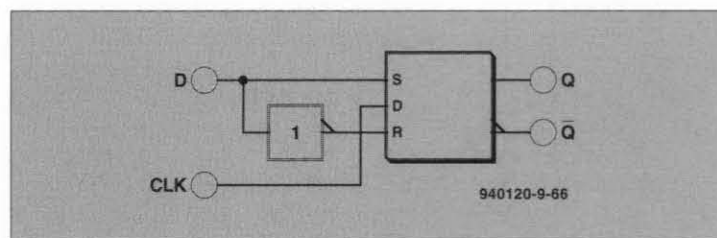


Fig. 69

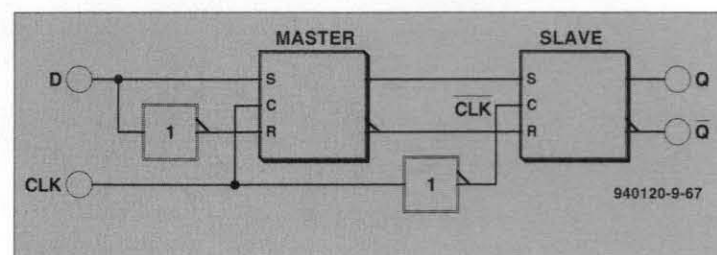


Fig. 70

delay latch of Fig. 70. When the clock is low, the master latch is transparent and the data passes to the inputs of the slave. It can not pass through the slave because this is latched by the inverted clock signal, $\overline{\text{CLOCK}}$. As the clock goes high, the data is latched on the outputs of the master. Now the slave is able to change state, and it accepts the data latched on the master. Output Q now has the same state as input D had at the instant the clock went high. The slave is transparent now, but its output does not change because its input from the latched master is unchanging.

The latches we have looked at so far have all depended on the level of the clock input. While a latch is transparent, its outputs follow its inputs and this may lead to complications. This problem is reduced if the clock input is fed through the circuit of Fig. 71 before going to the latch. Figure 71 is built into the input side of the latch. The AND gate receives the clock signal directly and the inverted clock signal indirectly after a very short delay in the invert gate. As the clock goes high, there is a very short period when the output of the invert gate is still high (from the previous clock low), so the output of the AND gate is high. When the clock goes low, the output of the AND gate goes low without waiting for the changed signal to reach it through the invert gate. The result is a short high pulse each time the clock changes from low to high. A latch using this type of clock input is said to be *positive-edge triggered*, because it changes state on the positive-going or *leading edge* of the clock pulse. Using different logic, latches are also made which trigger on the *trailing edge* (falling) edge. They are said to be *negative-edge triggered*.

Latching types

Figure 72 illustrates some of the many variants of the latch circuit. Figure 72a is an edge-triggered D-type latch, available as the 74HC74 IC. The 'S' symbol at the clock input indicates that it triggers on the negative (trailing) edge of the clock pulse. The 'double-S'

symbol indicates a Schmitt trigger input. Once the clock voltage has fallen below the lower threshold, a small rise in voltage and subsequent fall produces no re-triggering. This makes the action of the latch less subject to noise and to spikes on the supply and signal lines. This particular latch also has a *direct set* and a *direct reset* input. These inputs, not to be confused with the S and R inputs of an R-S latch, allow the the latch to be set or reset at any time, independent of the state of the clock. The inputs are sometimes known as *LOAD* and *CLEAR*. In the latch shown, the triangular symbols indicate that the latch is set or reset by taking the appropriate input low.

Figure 72b is a J-K latch. It has two extra inputs which determine what happens when the latch is clocked. This latch changes state on a trailing edge, but does not have Schmitt trigger inputs. The effect of the J and K in-

J	K	Result on clocking
L	L	No change
L	H	remains or goes low
H	L	remains or goes high
H	H	changes to opposite state

Table 3. Action of J and K inputs.

puts is shown in Table 3. Depending on the levels we apply to J and K, we can steer the output to any state we require. The J-K latch is a very versatile circuit. It can be used for data storage and, in this capacity, is important as a building block of shift registers. One particularly useful application is a toggle or

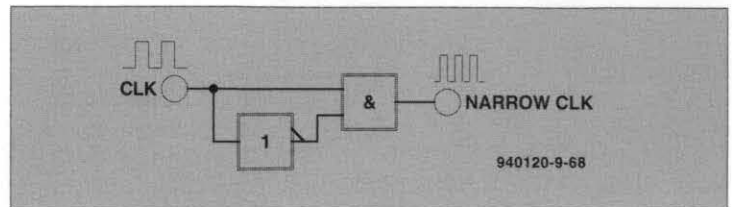


Fig. 71

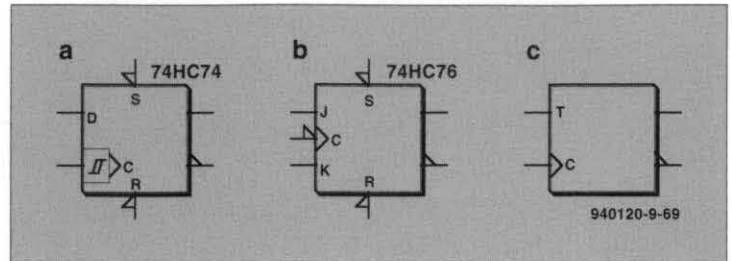


Fig. 72

T-type latch, in which the J and K inputs are connected to the same input pin. When that pin is held low, both J and K are low, so the output does not change. If the pin is held high, both J and K inputs are high and the output changes state (toggles) on each clock pulse. The symbol for this type of latch appears in Fig. 72c. Toggle latches are important as the building blocks of counters and dividers.

Shift registers

A shift register consists of a number of bistables connected in series so that data can be shifted from one bistable to its neighbour. A typical shift register is illustrated in Fig. 73. It consists of a chain of D-type bistables, with the output of one fed to the D input of the next. They are all clocked from a common line and also have their reset inputs fed from a common CLEAR. To start with, the CLEAR input is made low, making the outputs of all latches low. The serial

output is low; if it is made high, the latches hold 1, 0, 0 and 0 (from left to right) after the next clock pulse. If the serial input is now held low, the latches hold 0, 1, 0, 0 after the next clock pulse, and the serial output is still low. At each clock pulse, the 1 is shifted along the row from left to right. On the 4th clock pulse, the 1 has reached the end of the row and is stored in the extreme right latch. The serial output becomes high for the first time. On the next pulse, the latches hold 0, 0, 0, and 0. The 1 has been shifted out of the register. Whatever sequence of 0s and 1s is presented to the serial input, it is shifted down the row one step at each clock pulse and appears at the serial output four clock pulses later. Delaying a pulse train is an important application of this kind of shift register. The 4031 is an extreme example with 64 latches, giving a delay of 64 clock pulses.

Figure 73 is known as a *serial-in-serial-out* (or SISO) register. Another type of register

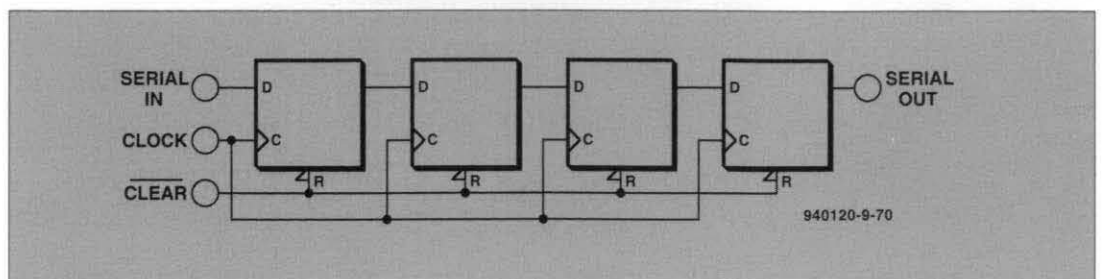


Fig. 73

Contents of latch number				XOR (of 3 & 4) fed back	Output (4)
1	2	3	4		
1	1	1	1	0	1
0	1	1	1	0	1
0	0	1	1	0	1
0	0	0	1	1	1
1	0	0	0	0	0
0	1	0	0	0	0
0	0	1	0	1	0
1	0	0	1	1	1
1	1	0	0	0	0

Table 4. Pseudo-random numbers.

has serial input, but the outputs of the latches are taken to separate terminal pins. This makes it possible to read the contents of all the registers at one time. This *serial-in-parallel-out* (or SIPO) shift register is used for converting serial data into parallel data. For example, in the UART of a receiving modem, the serial data bits are fed into the serial input of the register until the register is full. Then the data is read from all registers at once in parallel and sent to the computer. Shift registers are also available to perform parallel-in-serial-out (useful in the transmitting side of a modem) and parallel-in-parallel-out operations. Most shift registers shift from left to

right as described, but others shift from right to left. Some can be made to shift in either direction by making a 'direction' input high or low.

PIPO registers with left shift can be used for binary multiplication. For example, take a value such as 111001 (57 in decimal) and load it in parallel to a PIPO register. Reading from left to right, the latches hold 00111001. Perform one left shift: the latches now hold 01110010. Reading this out in parallel gives the value 1110010 (114 in decimal), which is the original value multiplied by 2. Operations of this kind are performed in the registers of microprocessors when multiplication is called for.

Clock pulse number	State of output			
	Q ₄	Q ₃	Q ₂	Q ₁
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0

Table 5. Counter/divider output.

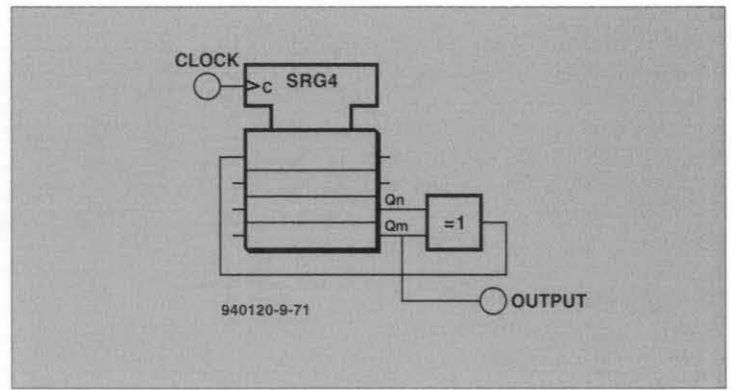


Fig. 74

An interesting application of shift registers is in the generation of random numbers. Given a shift register of length *m*, we feed the *m*th output (one of the earlier stages) to an exclusive-OR (XOR) gate. The output of this is fed back to the serial input (Fig. 74). Reading the output at each clock pulse, we obtain a series of 0s and 1s apparently occurring at random. For example, if we have a 4-stage register and XOR the 3rd and 4th latches, and assuming we begin with all 1s, the series of outputs is shown in Table 4. Actually, the series repeats itself, so it is not truly random, but pseudo-random. The repetition occurs after 2^{m-1} clock pulses. For example, if the register has four stages, it repeats after 15 clock pulses. A long register with, say, 15 stages, tapped also at stage 14, repeats after 32767 pulses. With such a long sequence, the output is virtually random. Such a circuit can be used for generating white noise digitally.

each clock pulse. The output of the second latch changes state on the falling edge of Q₁. This process continues along the line of latches, each latch changing state when the output of the latch before it changes from high to low (1 to 0). Assuming that the latches are reset to start with, Table 5 shows their outputs after the trailing edges of eight clock pulses. There are two aspects to this table. One is that Q₁ goes high *once* for every *two* clock pulses. In other words, its frequency is *half* that of the clock. Next, Q₂ goes high once for every four clock pulses: its frequency is a quarter of that of the clock. Likewise, Q₃ is an eighth of the clock frequency and Q₄ is a sixteenth. Frequency is divided by 2 at each stage in the chain. In this sense, the circuit acts as a *frequency divider*. This has many applications in circuits for tone production, including electronic organs and synthesizers.

Counters and dividers

In Fig. 75, output Q₁ of the first toggle latch changes state on the trailing edge of

The second aspect of the circuit action is that if we consider the four outputs at each pulse to be a binary number, they are equal at each stage to the number of pulses sent to the circuit. In other words, the circuit is a *pulse counter*. Counters, too, have many applications, particularly in calculating circuits, frequency meters and other devices. Although the pulse input in Fig. 75 is labelled as a 'clock', it does not have to come from a regular pulse generator. For example, the clock input can come from a circuit detecting objects passing by on a conveyor belt; the counter registers the number of objects that have passed since it was

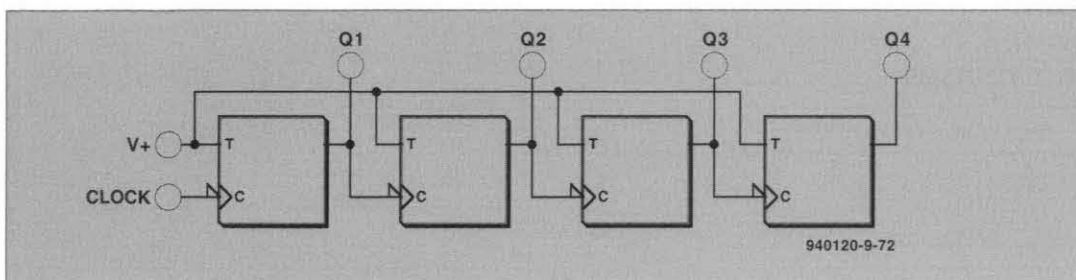


Fig. 75

last reset.

The counter of Fig. 75 is a 4-bit *up counter*. There are also *down counters*, which decrease their count at each clock pulse, and *up/down counters* which can be made to count in either direction by making a control input high or low. Counters also have reset inputs and some can be loaded with a required value before counting begins.

The maximum count that can be registered on a counter with n stages is $(2^n - 1)$. For example, the counter in Fig. 75 can count up to 15, then it reverts to all zeros at the next pulse. Some counter ICs have 14 stages, so that the maximum count is $2^{14} - 1$, or 16383. Counters can be cascaded for even larger counts. Since most people represent numbers in decimal form, it is useful to have a counter which counts up to 9 and then returns to zero to begin again. **Figure 76** shows one way of building such a counter. The AND gate receives its inputs from the \bar{Q} outputs of latches 1 and 3, and from the Q outputs of latches 2 and 4. The counter operates like Fig. 75 until it reaches the count of 9 (1001). The next pulse produces 1010, but when this happens, the inputs to the AND gate are all low. Its output goes low, resetting all the latches. Thus, the tenth count is extremely short-lived and is immediately converted to zero. It is possible to build counters of other lengths by using this technique.

Figures 75 and 76 are known as *ripple counters*, because each latch changes state only when the one before it has changed state. The change ripples along the chain. For example, the change from 0111 to 1000 goes through these stages, changing one bit at a time:

0111 → 0110 → 0100 → 0000 → 1000

When changing from 7 to 8, it goes through 6, 4 and 0 on the way. The change is too rapid for anyone to notice by observing a digital display of the count. But if there are logic circuits set to detect 6, 4 or 0 outputs from the counter, they could well be triggered by the transient values. This

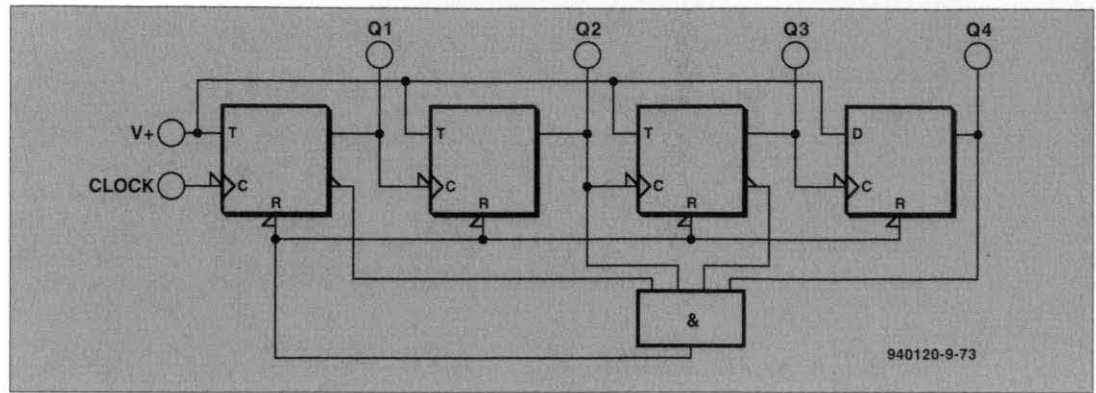


Fig. 76

problem is minimized by using a *synchronous counter* in which all latches are triggered by a common clock, so all change at the same time.

Figure 77 shows a 3-bit synchronous counter. The T input of latch 1 is high, so this latch toggles at each clock pulse. Latch 2 can toggle only when Q_1 is high. Table 5 shows that this occurs only on the odd counts 1, 3, 5 and 7. Latch 2 changes state only as the count continues to multiples of 4. Further logic is needed to extend the counting chain. There is a propagation delay in each latch, so the output of every latch changes a short time after the trailing edge of the clock signal. This considerably reduces, but does not completely eliminate, transient errors. It is inevitable that there are very small *differences* between the propagation times of the individual latches, and these produce transient errors of short duration. If it is essential to eliminate these, the outputs are not read until a short time after the clock has gone low, giving the circuit time for outputs to settle to their new states.

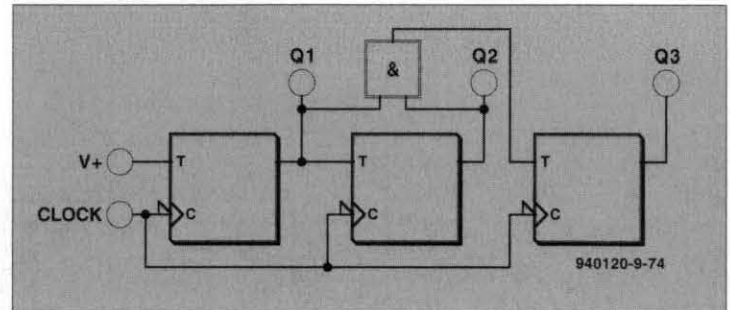


Fig. 77

2. Continue the pseudo-random number sequence of Table 4 until it repeats.
3. What is the maximum count obtainable on (a) a 12-stage counter; (b) two cascaded 12-stage counters?

Answers to Test yourself (8)

1. 2025 Hz.
2. 01000001100.
3. ASTONISH; 51.6%.

[940120-9]

Test yourself

1. An R-S latch can also be constructed by substituting NOR gates for the NAND gates in Fig. 65. Is this active-low or active-high? Write out the state table for such a latch.

FOCUS ON: DIGITAL TELEVISION

Just in case you had not noticed it, the buzzword in the discussions about digital television is MPEG-2. Pushed mainly by the broadcasters, the electronics industry is working hard to produce hardware to complement the new data compression techniques for moving pictures, which were finalized more than a year ago. The tactic aim of the TV industry conglomerates is to make the start of the first MPEG-2 broadcasts coincide with this year's prestigious Berlin Funkaustellung (broadcasting exhibition).

By Gregor Kleine

THIS article aims at giving you a useful background to MPEG-2, and attempts to offer a glimpse of the future of digital television.

MPEG is an acronym for Moving Picture Experts Group, a council of technical experts which drew up the MPEG-2 standard at the beginning of 1994. The standard comprises a number of rules which describe a video and audio data compression technique. The actual MPEG-2 standard is divided into three sections: video, audio and 'system'. The latter describes the structure of the packets which contain compressed audio and video data.

However, the descriptions in the MPEG-2 standard are limited to the processing of audio and video data in the source. Subjects like error protection and data structures with satellite and cable links remain part and parcel of the channel encoding, which is not described by the MPEG-2 standard. To enable errors

to be corrected (to a certain extent), the channel encoding adds redundancy to the source data. The different channel properties of satellite, cable and terrestrial signal distribution call for different channel encoding systems to make sure the best possible solutions are found for each type of link. Consequently, the modulation types are different also: while QPSK (quadrature phase shift keying) is used on satellites, cable systems allow QAM (quadrature amplitude modulation) to be used, which greatly reduces the bandwidth.

Because of a general shortage of available frequencies, digital TV via terrestrial transmitters is not feasible right now, and no modulation system has been agreed upon yet. Consequently, digital TV broadcasts will be limited to satellite and cable for a while to come. None the less, the modulation system for digital terrestrial TV is a subject of discussion which currently seems to narrow to

OFDM (orthogonal frequency division multiplex). OFDM is proposed for a network of synchronized transmitters, as used with DAB (digital audio broadcasting). This wide band modulation system distributes the bits over a multitude of individual, digitally generated, carriers. This allows bit errors, which can arise as certain narrow frequency ranges are temporarily blotted out during mobile or portable reception, to be eliminated by the error correcting system in the receiver.

MPEG-2 digital TV receiver

Figure 1 shows a block diagram of the all-digital TV set of the future. Because of the different modulation systems, the digital TV set should have the appropriate demodulators for broadcasts received via satellites, cable networks and terrestrial transmitters. To give the viewer his selected programme, a demultiplexer lifts the desired data from the input datastream, and copies this data to the video and audio decoder. With encrypted programmes (Pay TV etc.), an enable signal is produced to switch on the relevant decoder, but only if the viewer is authorized to receive the program. The decoder then also charges you on a pay-per-view basis via your Smart card. If no authorization is available, the relevant decoder remains disabled. The decoded and decompressed data are subsequently converted to analogue, and fed to the picture tube and to the loudspeakers.

Profiles and levels

MPEG-2 describes different levels of quality and resolution in relation to the digital data compression for video and audio signals. The quality levels are referred to as 'profiles' in the standard, while the resolution indicators are called 'levels'. The profiles indicate which of the data reduction systems are selected from the list of tricks offered by MPEG-2. The higher the profile, the more complex the function of the relevant decoder. The levels determine the maximum picture resolution, enabling decoder hardware manufacturers to provide the necessary picture memory capacity. **Table 1** shows the maximum data rates for different combinations of profile and level.

A decoder which is capable of handling a certain profile and a certain level should also be able to decode all profiles to the left, and all levels below. The combinations without a data rate figure are not foreseen in MPEG-2. A fully compatible decoder need not be able to process these combinations. The first applica-

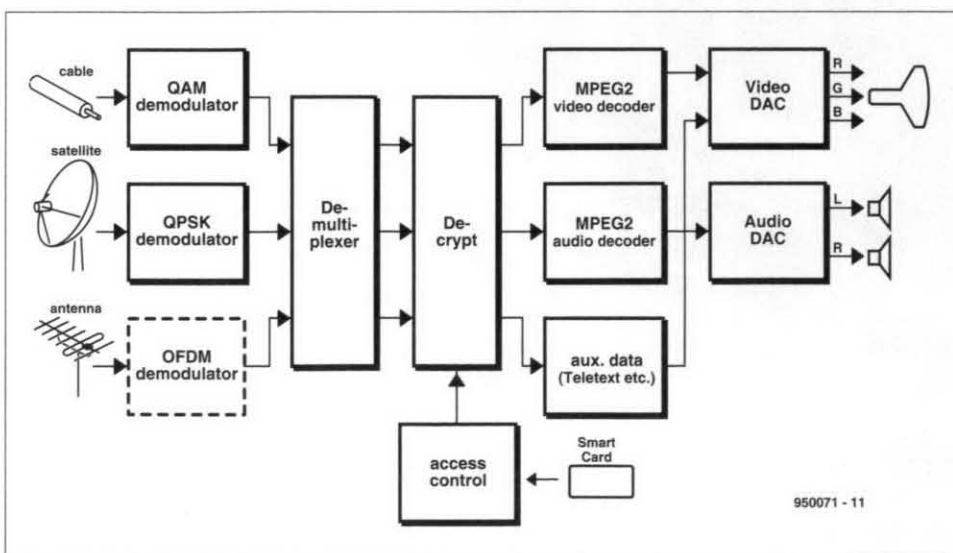


Fig. 1. Block diagram of a digital TV receiver.

tions of MPEG-2 will be based on the Main Profile and the Main Level (denoted by the experts as 'MP@ML'). In cases where a lower quality is sufficient, the Low Level may be used in the Main Profile (MP@LL).

A new feature for digital data transmission systems is achieved with the higher profiles by *scalable* and *hierarchical* encoding. Normally, a digital signal disappears altogether if the signal-to-noise ratio falls below a certain threshold. This effect is not known in analogue transmission systems, where the corruption of pictures and sound is gradual as the S/N ratio drops. To be able to mimic this gradual disappearance with digital TV, for instance, when a portable receiver is used, a feature referred to as scalability is introduced with the three highest level profiles. This scalability distributes the datastreams in such a way that the basic data for a reduced picture quality are transmitted in the form of a 'robust' coarse modulation. All other data, which serves to give additional picture quality, is packed in a type of 'fine' modulation superimposed on the 'coarse' information. This principle is illustrated in **Fig. 2**, which shows an example of 16QAM ('fine' modulation) which can be demodulated as QPSK also ('coarse' modulation) simply by shifting the phase state locations.

An MPEG-2 receiver which is being fed with a signal having a high S/N ratio (for instance, with fixed location reception) will show the full available quality. A portable receiver, on the other hand, is capable of showing a picture with less quality if the S/N is low by processing the coarse modulation only. This remarkable feature built into the MPEG-2 standard is referred to as 'graceful degradation' by the experts. The four quality levels which offer graceful degradation are shown in **Table 2**.

I, P and B pictures

The need of data reduction is apparent from the studio data rates listed in **Table 3**. A starting point for data reduction is to exploit the similarity between successive half pictures (fields or rasters). Actually, the MPEG-2 standard recognizes three different types of picture: **I pictures** (I for 'intra') are the only ones to be transmitted in full, and serve as a basis for the computation of P and B pictures (see below). This picture type should occur several times each second in the datastream to make sure that viewers who switch on to a channel are quickly presented with an error-free picture. Also, in order to prevent error propagation in the system, I pictures should frequently eliminate accumulated errors.

The **P picture** (P = predictive) is a difference picture which may be computed from the previous I picture with the aid of a significantly smaller amount

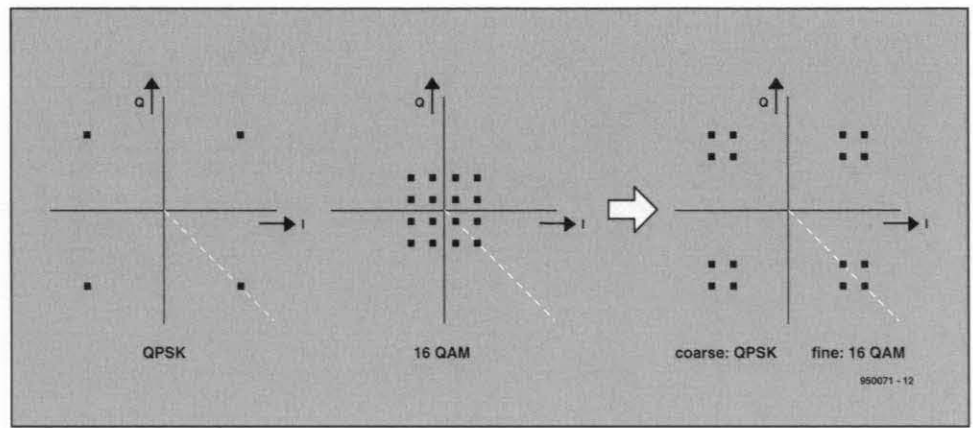


Fig. 2. Coarse and fine modulation for the purpose of graceful degradation.

	Simple Profile	Main Profile	SNR Scalable Profile	Spatial Scalable Profile	High Profile
B pictures:	no	yes	yes	yes	yes
Format:	4:2:0	4:2:0	4:2:0	4:2:0	4:2:0/4:2:2
Scalable:	no	no	SNR	SNR/spat.	SNR/spat.
High Level max. 1920x1152	-	80 MBit/s	-	-	100 MBit/s
High 1440 Level max. 1440x1152	60 MBit/s	-	60 Mbit/s	80 MBit/s	-
Main Level max. 720x576	15 MBit/s	15 MBit/s	15 MBit/s	-	20 MBit/s
Low Level max. 352x288	-	4 MBit/s	4 MBit/s	-	-

Table 1. Combinations of profiles and levels with their maximum data rates.

of data. In between I and P pictures there may occur **B pictures** (B = bidirectional predictive). These inserted pictures are also differential, and require even less data than P and I pictures. They are built from nearby P and I pictures. Their computation is based mainly on movement vectors which indicate the direction and the amount of travel of a certain picture section. This is made possible by a so called 'block matching scan' operation carried out by the coder.

The overview in **Fig. 3a** once again indicates the pictures from which the individual picture types are predicted.

The top drawing in **Fig. 3b** shows the timing diagram of a picture sequence consisting of I, P and B pictures. The dis-

tance between two I pictures is set arbitrarily to 12 (N). Each third picture between the I pictures is a P picture ($M=3$). In between these are two B pictures each. The MPEG-2 encoder is capable of setting the values for M and N in certain predetermined steps, depending on the quality to be achieved, and the maximum desired data rate in a certain transmission channel. The picture type is flagged to the receiver decoder by the header in the packet structure of the data stream. Only with the Simple Profile there are no B pictures, so that $M=1$.

To give the decoder sufficient time to compute the intermediate pictures of the 'B' type, the picture sequence must be changed for the transmission (Fig. 3b,

HDTV	High Definition Television	20-30 MBit/s	very high picture and sound quality
EDTV	Extended Definition Television	6-8 MBit/s	16:9, approx. PAL+ quality
SDTV	Standard Definition Television	3-4 MBit/s	PAL quality
LVDT	Low-definition Television	1.5-2 MBit/s	VHS quality, small screens

Table 2. TV quality levels when graceful degradation is applied.

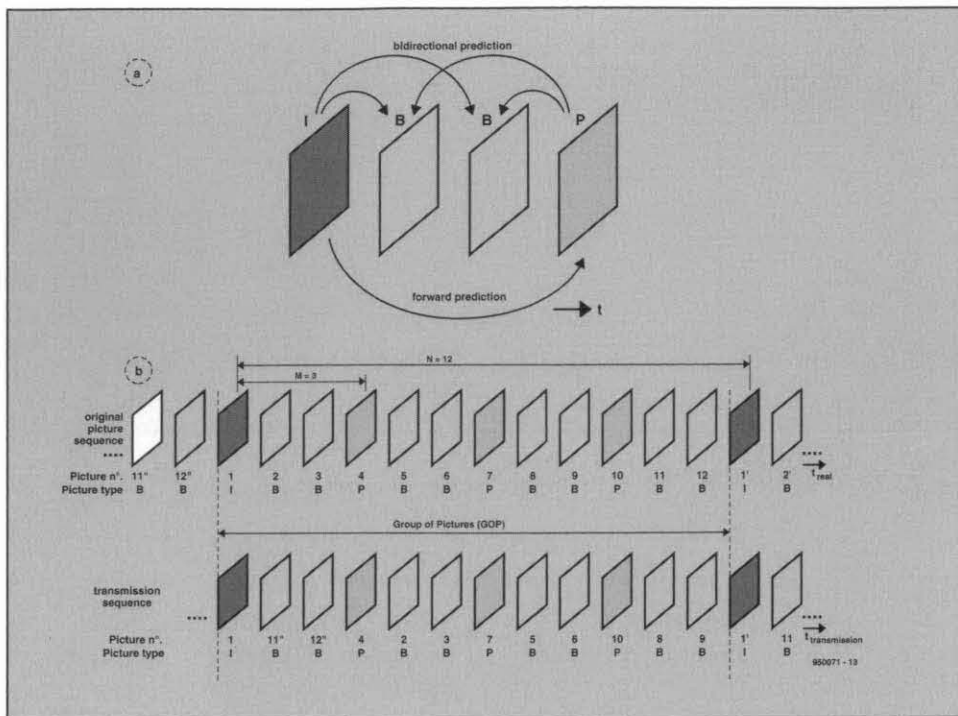


Fig. 3. a) Prediction with P and I pictures; b) I, P and B pictures in normal sequence, and sequence for transmission.

HDTV	1250 lines	16:9	1152 MBit/s
PAL Plus	625 lines	16:9	216 MBit/s
VHS	625 lines	4:3	216 MBit/s

Table 3. Studio data rates.

below). The I pictures keep their positions (but obviously with some off-set caused by the encoder's propagation delay) in the transmission sequence. However, to enable faultless calculation of the B pictures, the framing P pictures should first be applied to the decoder,

which responds by converting the P difference picture and the previous I picture into a complete, normal, picture. Once the I and P picture have been recovered, the data supplied by the successive B pictures may be used to reconstruct their original, complete, structure.

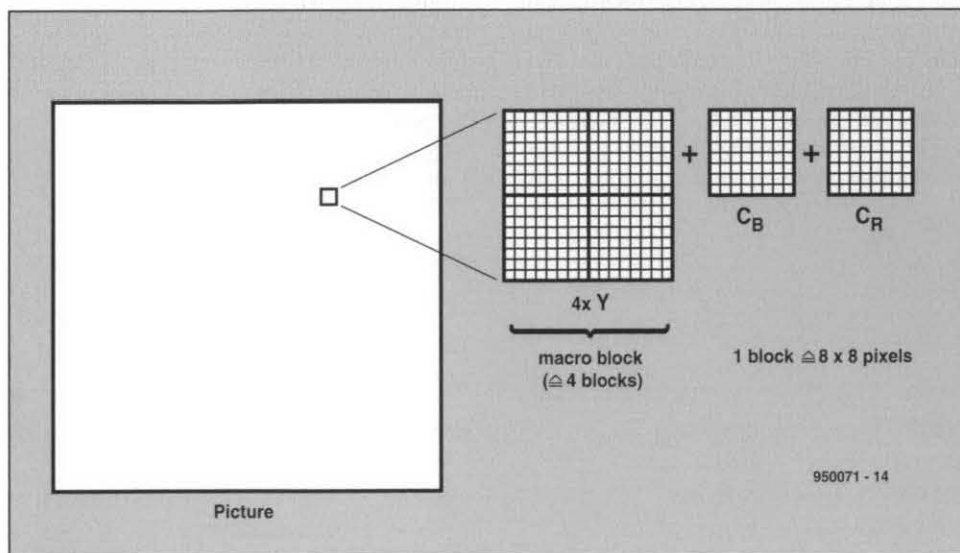


Fig. 4. Picture division in macro blocks and sub-blocks.

In the example of Fig. 3b, the I picture with number 1 is followed by two B pictures, 11'' and 12'', which, as far as the viewer is concerned, should precede the I picture, although their decoding requires the decoder to 'know' the I-picture already. Next comes P-type difference picture number 4, which can be computed entirely with the aid of I picture number 1. These two pictures then enable the two bidirectionally interpolated B-type difference pictures numbers 2 and 3 to be reconstructed. The sequence then continues with groups of one P and two B pictures, until it is time for a complete I picture again.

MPEG-2 encoder

The data processing in an MPEG-2 encoder requires each original picture to be divided into a raster consisting of four macro blocks (Fig. 4). Each macro block consists of four sub-blocks of eight by eight picture elements each. The brightness signal (luminance) and the two colour signals (chrominance) are processed as blocks one after another. Associated with each macro block of 16 times 16 brightness values (Y) are two colour type blocks, C_b and C_r, each consisting of eight times eight colour values. This arrangement is referred to as 4:2:0 format by the experts. The 4:2:2 format of the High Profile (Table 1) is obtained by adding four instead of two colour blocks to each macro block. The result is a better colour resolution. The MPEG encoder described below processes each of these luminance and chrominance individually, and in succession.

The block diagram of a typical MPEG encoder is shown in Fig. 5. After the A-to-D conversion of the analogue video signal follows a pre-processing stage which does filter functions and, if necessary, re-arranging of the lines, in case interlaced half pictures are applied.

A discrete cosine transformation (DCT) stage forms two-dimensional brightness and colour information similar to the familiar Fourier transformation in a video frequency spectrum. In the case of the I picture, the input signal of the DCT is formed by the individual 64-pixel blocks of the full picture, and those of the difference picture with B and P pictures. The DCT itself is reversible, and does not cause data reduction. Not until the subsequent *quantization* is it possible to turn a large part of the DCT values into zeroes. This causes the disappearance of high-frequency components in the picture which the human eye has difficulty perceiving anyway. Next, *variable length coding* (VLC) further reduces the number of bits to be transmitted by assigning a short code to frequently occurring DCT values (Huffmann or entropy encoding). Longer codes also occur. The video data compressed in this way then arrive at a buffer which outputs the

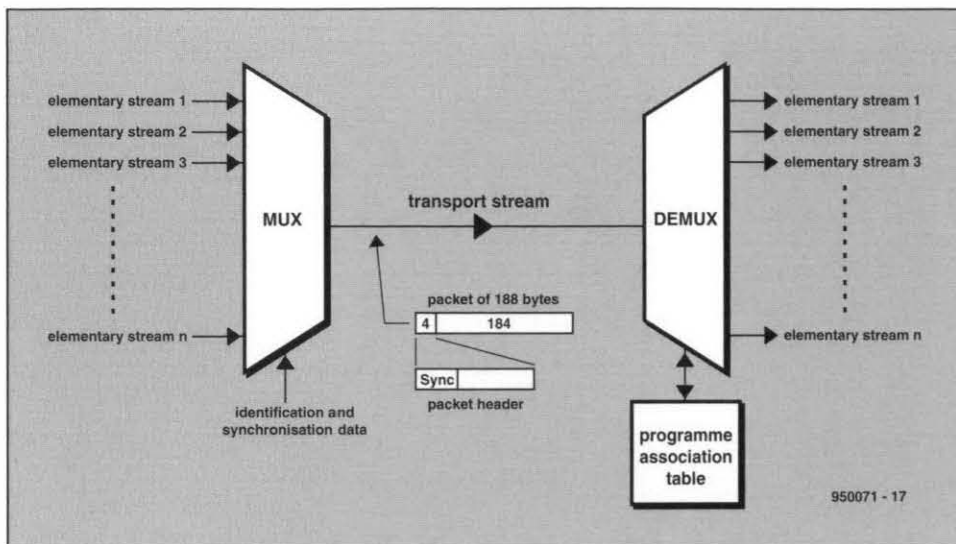


Fig. 7. MPEG-2 programme multiplexer.

human ear. Sounds which are under the *hearing threshold* are not encoded. The system also suppresses soft sounds in the vicinity of loud ones (*co-hearing threshold*). An in-depth discussion of the MUSI-CAM system may be found in Ref. 1.

In the MPEG standard, the complexity of the Musicam data reduction is divided into three downward compatible levels, which are referred to as Layers (Layer I through III), where Layer III is the most complex. An MPEG audio decoder capable of handling, for example, Layer II, should also understand Layer-I encoded data.

MPEG-2 is compatible with several audio sampling rates and several multi-channel sound systems (see **Table 4**). As compared with MPEG-1, there are also halved sampling rates and multi-channel as well as surround sound. The data rate of the compressed audio signals for a stereo channel with ancillary data (e.g., RDS) is 96 kBit/s, 128 kBit/s or 192 kBit/s, depending on the depth of the Musicam encoding.

The MPEG-2 transport stream

The MPEG-2 encoder supplies the video and audio data in the form of packets. These packets start with a header, which, in turn, starts with a synchronization word. The header contains information to tell the system whether video or audio data are involved. With video information, it also indicates the type of picture being transmitted, the structure of the matrix, when the picture has to be presented to the viewer, and more. With the audio data, the header tells the receiver, among other things, the data rate at the non-compressed side, and whether or not multi-channel sound is being used.

This stream of data packets within a single TV channel is referred to as *elementary stream*. Depending on the capacity of the transmission medium (satellite TV transponder or cable TV channel) several elementary datastreams may be bundled into a so-called *transport stream* (**Fig. 7**). The transport stream uses a

fixed packet length of 188 bytes (including the header), and is built from elementary streams by a multiplexer.

At the receiver side, this transport stream arrives at a demultiplexer, which uses the headers to route each packet to its own elementary stream. Furthermore, the multiplexer uses information from the so-called *programme association table* to determine which programmes are being transmitted, as well as their transmission format.

The MPEG-2 decoder

The basic architecture of the video decoder in an MPEG-2 compatible TV set is shown in **Fig. 8**. The compressed video datastream (in packet form) arrives at a header detector, which passes the information extracted from the headers to a control section, and arranges the data acceptance of the buffer. The picture data produced by the buffer then reach a stage which eliminates the variable length coding. An inverse quantization operation transfers the block-arranged picture data (8x8 pixels) to the inverse DCT, which does the re-conversion into real brightness and colour information (but still as digital datawords). The motion compensation with P and B pictures uses the movement vectors to reconstruct a viewable TV picture from the difference picture. The viewable picture is then copied into a picture memory where it is held ready for the picture output control. The content of the picture memory output is then also available for the processing of subsequent P and B difference pictures.

Channel encoding for cable and satellite

As already mentioned, the MPEG-2 standard only discusses the source encoding. It says nothing about the channel encoding for the purpose of bit error protection to be implemented in the transmission

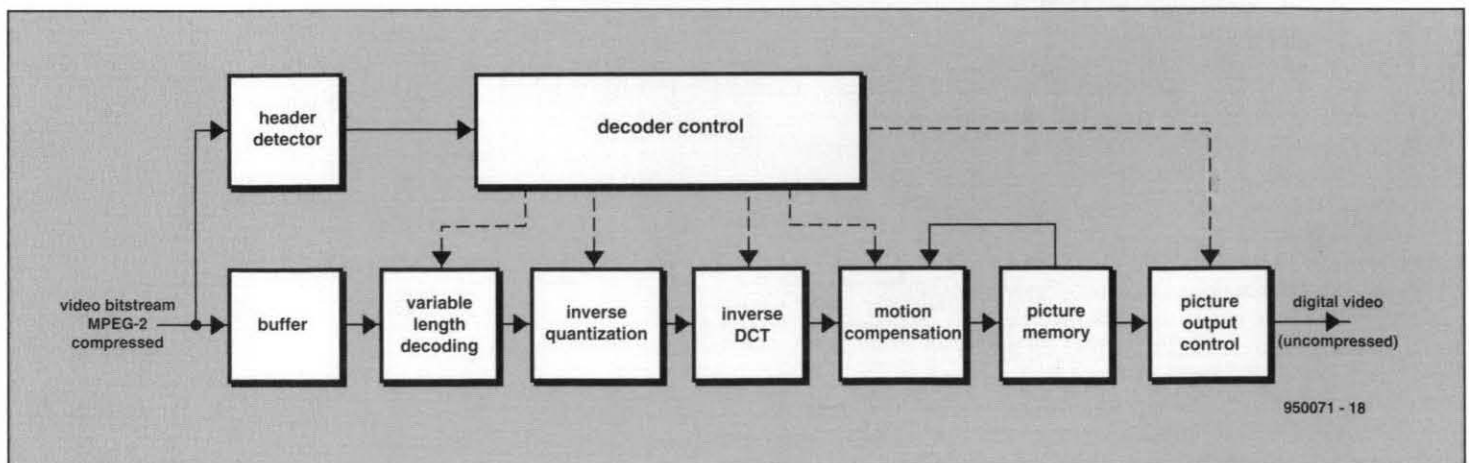


Fig. 8. Block diagram of an MPEG-2 decoder.

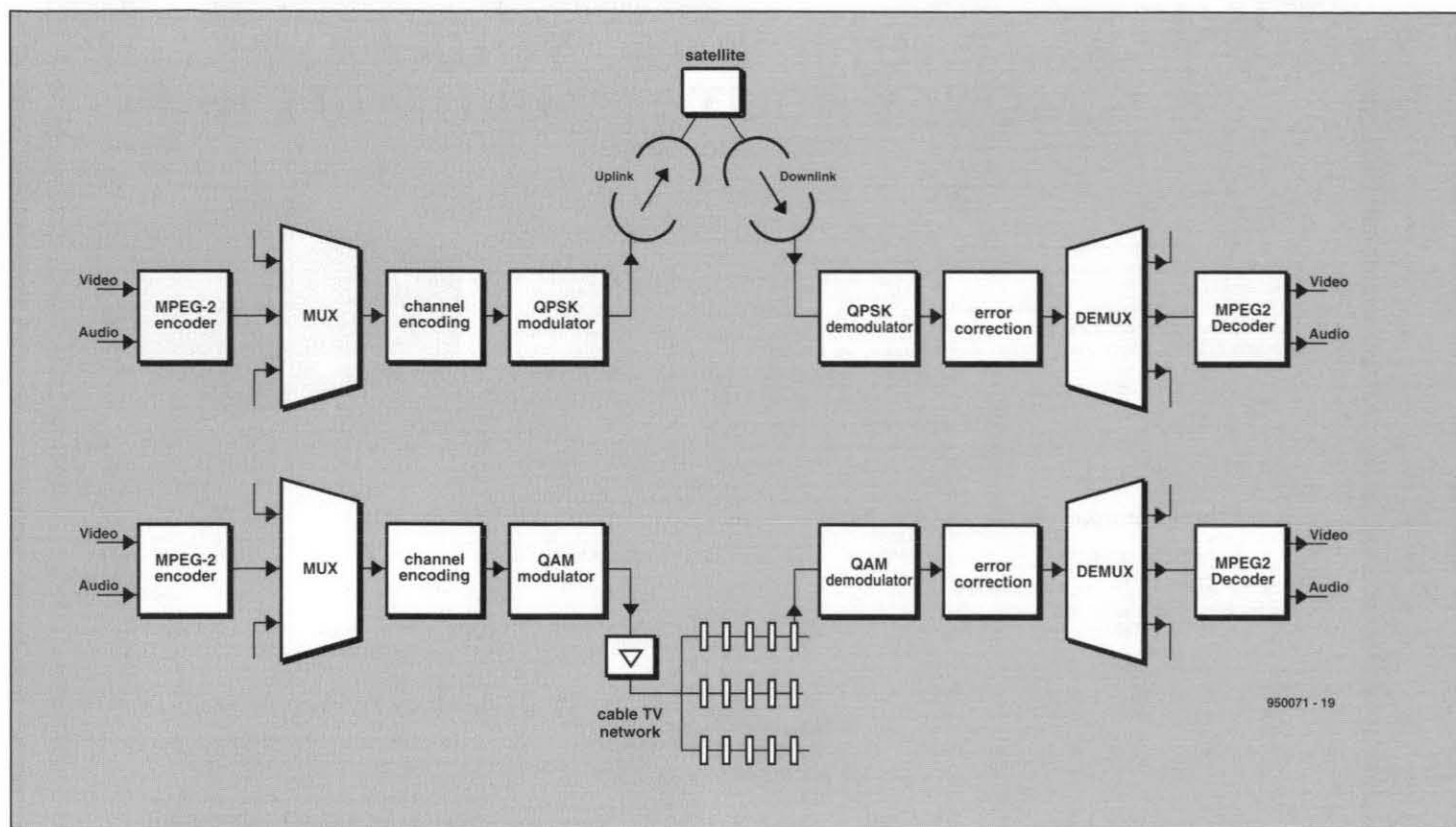


Fig. 9. Channel encoding used on cable network and satellite.

channel. The drawing in **Fig. 9** shows the individual processing blocks with satellite and cable TV systems. After the MPEG-2 source encoding, and the bundling of several programmes follows the channel encoding to achieve error protection. In the case of a satellite link, this is followed by a QPSK modulator, which generates a four-phase RF signal. QPSK modulation is used because of the often poor linearity of satellite TV transponders. In cable networks, on the other hand, very good linearity and signal to noise figures may be expected, so that the use of eight amplitude levels helps to save a lot of bandwidth. Instead of QPSK modulation, QAM is applied on cable TV networks (16-QAM, 32-QAM or 64-QAM). The phase states of the two modulation systems are sketched in **Fig. 8**.

Where the satellite signal is to be put onto a cable network, some dedicated equipment is required for the modulation format conversion. A QPSK demodulator with error correction makes the transport stream available. After a new channel encoding operation and 64-QAM modulation, the signal is ready to be put onto the cable. Because most cable networks are already pretty crowded with analogue PAL signals, digital TV is often transferred to the Hyperband (302 MHz to 446 MHz). In this space, up to eight MPEG-2 programmes may be squeezed into a bandwidth of 8 MHz, depending, of course, on the compression factor, which, in turn, determines the picture quality.

Thus, there is room for up to 144 digital TV programmes in the Hyperband.

In Europe, digital TV programmes will be broadcast via the Astra 1E (1995), Astra 1F (1996), as well as the EutelSat Hot Bird (1994) and Hot Bird Plus (1996). The exact number of digital TV signals which will be available in the near future is difficult to predict. If the quality requirement is relaxed, (see Table 2), up to 12 MPEG-2 programmes may be carried via a single transponder of the 'Astra' type. If all 32 available transponders on Astra 1E and 1F were commissioned for 12-channel digital TV, that would give a staggering total of 384 TV channels!

Computing the hypothetical, maximum, number of TV channels on a cable network or on a satellite is all very well, but bear in mind that rapidly changing pictures (as for example, in sports) require smaller compression factors than, for instance, cartoon films. Not surprisingly, concepts have been drawn up which use variable transponder bandwidth allocation to the different types of program.

Further outlook

With the introduction of the MPEG-2 data reduction process, a means has become available which enables the number of programmes contained in the bandwidth for a traditional TV channel to be multiplied at the cost of the transmission quality. It will be very unlikely

that all these new channels will go to 'traditional broadcasters' because many of these already seem to run into financial trouble if the competition consists of, say, 25 others on a cable TV network. Also, the advertising revenue which can be procured by a broadcaster is not unlimited. New applications of TV channels are therefore bound to occur, including:

- Pay-per-Channel
- Pay-per-View
- Near-Video-on-Demand
- Video-on-Demand
- Teleshopping
- Teleteaching

Apart from TV movie makers, large warehouses and mail order giants have also shown great interest in the channels that will become available to offer their products via Teleshopping, the Electronic Warehouse and the like.

Because MPEG-2 changes TV transmission into data transmission, the acronym is also often mentioned (and the system used!) in relation to today's MultiMedia hype. Indeed, many high-resolution photographs and other artwork is already available on CD-ROM in MPEG format. (950071)

References:

1. Astra Digital Radio, parts 1 and 2, *Elektor Electronics* May and June 1995.

LETTERS

6-V lead-acid battery charger

Dear Editor—I am hoping you can help me with a seemingly simple problem.

My present Lambretta rectifier unit (6 V at 12 A) has packed up and I wish to replace it with a home-made battery charging unit. The power is supplied from a coil on the bike's magneto. As I have been unemployed for the past five years, I cannot afford Lambretta's extortionate price for a replacement unit, so I trust you can supply me with the circuit diagram of a suitable unit.

A. Appley, Bromley, Kent.

As luck would have it, we have just published a design that should meet your present needs exactly: '6 V motive-battery charger' (July/August 1995, p. 92).

[Editor]

Reception of Manx Radio

Dear Editor—For a couple of years now, I have been writing to different radio advertisers: what I would like to do is fit myself up with whatever equipment it takes to receive Manx Radio (1368 kHz). For some reason, I have never ever received any information on what I am asking for. May it is just simply impossible or nobody can explain it to me or they don't know how to do it themselves.

The reason I keep pursuing my quest is that I look at different electronics magazines and I see places like Slovenia, Liechtenstein, Turkey, and so on, being able to be reached by amateur radio. I put on my household radio, scan the waves and it is guaranteed that I find somebody from a foreign country speaking in a foreign language. Surely, the Isle of Man is not too far away.

If I am just plain stupid, then please, please, let somebody tell me or even take a little time to explain why these few (130) miles cannot be bridged.

R.J.R. Michelson, Melton Mowbray

The e.r.p. (effectively radiated power) of Manx Radio is only 2.5 kW; that, together with the hilly countryside between the isle and Melton Mowbray prevents good reception of the station. A directional antenna, such as described in 'Small loop antennas for MW, BCB, LF and VLF' by J. Carr in our June/July 1994 issues, may help you receive Manx Radio.

Suggestions and/or comments from other readers are welcome.

[Editor]

Bat detector

Dear Editor—The electret (condenser) microphone Type ME2500 (from MailTech), used in the 'Bat Detector' *EE* April 1995, p. 62) is NOTHING like the sketch on the circuit diagram.

[The letter continues with many notes and suggestions on the construction of the unit—copies of the complete letter can be obtained on request from our Editorial Office in Dorchester].

Bruce Williamson, Melton Mowbray

Unfortunately, you have misread both the circuit diagram and the parts list: the microphone around which the unit is designed and tested is an MCE2500 from Monacor (which is available from, among others, C-1 Electronics at about £5). If you have trouble in obtaining this, please let us know.

None the less, thank you very much for your interesting and detailed letter.

[Editor]

Figuring it out

Over the past year, there has been correspondence between Mr Ritchie of Fraserburgh, Scotland, and Mr O. Bishop, author of the 20-part series 'Figuring it Out' which ended in our November 1994 issue. The correspondence was protracted owing to Mr Bishop's moving to New Zealand.

The main reason for the correspondence was Mr Ritchie's comment that the derivation of Equation 115 in Part 14 (March 1994) was flawed. Mr Bishop commented to this as follows: "In Part 14 there was an arithmetic error in deriving Eq. 112. The equation should have been $5000C + 50000Ct + 50000 = 400t$. Consequently, the values obtained by applying that equation were incorrect. Now, $C=8 \times 10^{-3}$, $D=-8 \times 10^{-4}$, and Eq. 115 should be $i=0.001913(e^{-10.02t} - e^{-4990t}) + t(8 \times 10^{-3}) - 8 \times 10^{-4}$. The graph of this equation has the same general features as that shown in Fig. 119, rising to about 1 mA as before, though rather faster, then falling slightly before it begins to rise again after about 90 ms. The text describing the graph and the conclusions to be drawn remain unaffected by this correction".

There remains a 'grey' area pertaining to (1) Eq. 112 in Part 14, which Mr Ritchie claims "is based on a fundamentally flawed concept (like Eq. 115)"; (2) Eq. 147 in Part 19, which Mr Ritchie claims "produces a result wherein the energy dissipated is greatly in excess of that stored in the source: a ridiculous situation which could imply that perpetual motion is not only possible, but can be achieved with an extraordinary degree of efficiency"; (3) Mr Ritchie's comment that "the answer given to question no. 2 in Part 20 is wrong and is subject to the same comment as (2) above. Mr Bishop has, however, agreed in principle that the published results quoted were in error and has advised of the correct solutions.

These comments are published here in the interests of other readers. The correspondence on this subject is now closed as far as this magazine is concerned. Any further comments will have to be directed

to the author.

[Editor]

Surround sound processor

I am contemplating the building of the surround-sound processor (*EE* February 1995), but I fear a possible problem with the linking of the processor to an existing sound system (TV or stereo).

The article states that the processor must be connected to the LINE OUT of the TV receiver. I am afraid of a possible snag here. The level of the LINE OUT or SCART output is fixed, since it pertains to a volume-independent signal of $1 V_{pp}$. After the processor has been set up, the sound level of the centre and surround loudspeakers will then also be fixed (independent of the volume setting on the TV). I fear that this will not lead to the pleasant listening we are promised.

What I would like to know, therefore, is: "Would it be possible to make use of the headphone or external speaker outputs? The centre and surround speakers will then follow the volume setting of the main speakers (in the TV). But, how will the surround processor react when the loudspeaker signal is clipped by the zener diodes in the input circuits?"

S. Paternotte

The design is based on a variable line level: the headphone output of a TV receiver is eminently suitable. However, a fixed level, such as that from a SCART socket, can be used if the main speakers are driven via a separate amplifier. The line signal is then fed to a line input on the amplifier.

The surround sound processor is fed from the variable output of the amplifier (or the headphone output of the TV).

The rating of the zener diodes (D_1-D_4) does not make clipping likely: the maximum drive voltage required by the output amplifiers is about 1 V, well below this rating.

[Editor]

Upgrade your car battery charger

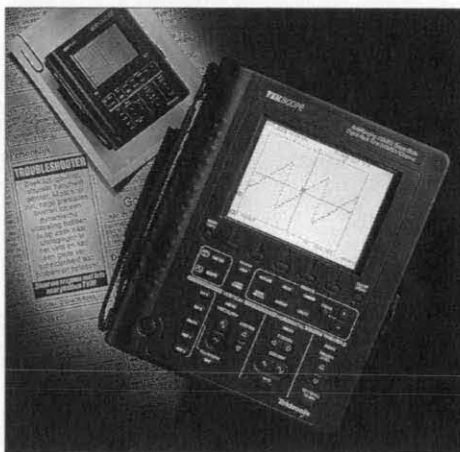
The article on p. 34 in our February 1995 issue stated that the circuit can be set up with a variable load of 2–5 Ω , 100 W. This is, of course, a formidable load, which is quite expensive. It is considerably easier and cheaper to use a number of parallel-connected defect car headlight bulbs (normally, the dimmer filament of these bulbs goes, but the main beam filament remains intact). A flasher light bulb (21 W) and rear light bulb (5 W) may be used for fine adjustment.

DESIGN COMPETITION REVISITED

International 1st prize

After our July/August issue had gone to press, it was decided to award an INTERNATIONAL 1ST PRIZE in addition to the national prizes in the various countries. The additional prize will be awarded for what the judging panel considers the best overall design from anywhere in the world. It does not replace national prizes.

The International 1st Prize, made available by Tektronix, is the new **Type THS720 TekScope**. This attractive test instrument is a complete pocket-size digital, two-channel oscilloscope. The bandwidth of each



channel is 100 MHz; the sampling frequency is 5×10^8 samples sec^{-1} . Test results are displayed on a clear screen; they may also be applied to a personal computer via the integral RS232 interface or printed out on paper. The instrument also provides a fully-fledged multimeter function. It comes complete with all necessary test cables and a protective cover.

CORRECTIONS TO JULY/AUGUST ISSUE

Owing to some last-minute alterations, a few small, but nevertheless annoying errors occurred in our July/August issue. The necessary corrections are detailed here.

The '**AF Power Indicator**' advised in the contents to be on p. 102 was omitted and is given here.

The page number of '**Speed-up for printer buffer**' was shown in the contents as 104, whereas this should have been 102.

The page number of '**Simple r.f.**

signal generator' was given as 30; this should have been 10.

The circuit diagram included with

'**ZN436 replacement**' on p. 109 is incorrect; the correct one is reproduced in column 1.

AF POWER INDICATOR

The indicator is intended primarily for heavy-duty PA (Public Address) loudspeakers. Connected simply to the loudspeaker input terminals, it displays the power applied to the speaker by a row of five LEDs: the larger the power, the more diodes will light. Since the power provided by the output amplifier also influences the total current through the diode array, the brightness with which the LEDs light also increases with increasing power. In this way, only five LEDs give a fairly good indication of the applied power.

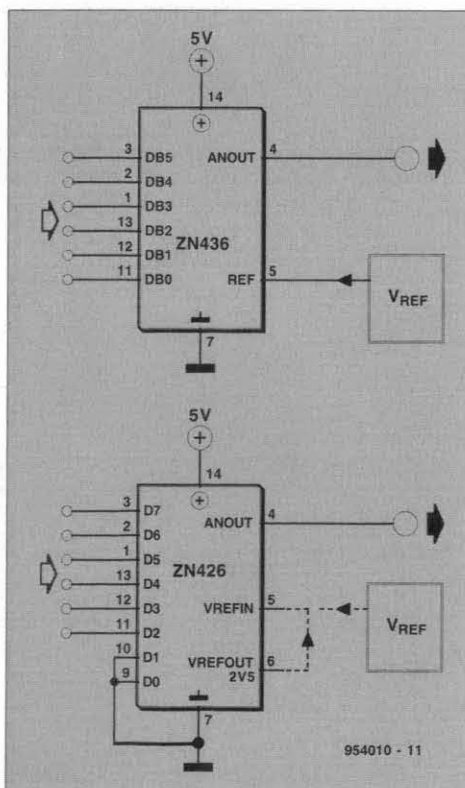
The scale is geared to use with PA systems, where a few watts here and there do not matter. The stated values relate to peak voltages across 8Ω . If the loudspeaker impedance is 4Ω , the values are double the stated ones.

Since a clear display requires that the lighting times of the LEDs are not too short, a single-phase rectifier, R_7 - D_6 - C_1 , is provided at the input. Because the capacitor is discharged each half period via R_6 and the remainder of the circuit, the afterglow lasts for some tenths of a second. Resistor R_7 limits the charging-current peaks to C_1 to about 1 A. The LEDs used are of the low-current type and light clearly at currents as low as 1 mA. Resistor R_6 ensures that at full drive the maximum permissible current through the

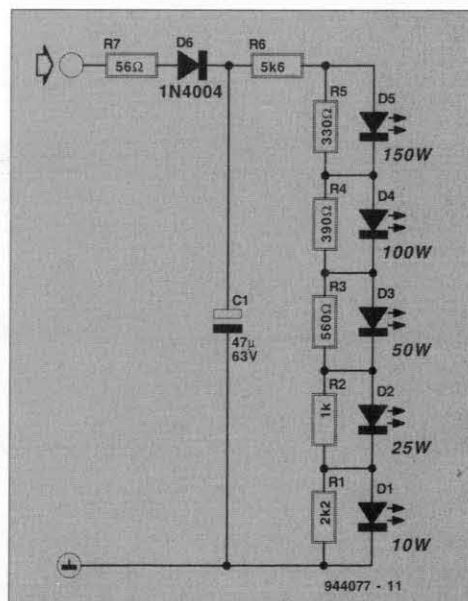
LEDs is not exceeded (7 mA at an a.f. power of 150 W into 8Ω).

If slightly longer afterglow times are required, the value of C_1 may be increased to some extent. However, this results in a power somewhere between peak and continuous values being measured rather than peak values. This is determined by the time constant of network R_7 - C_1 . Some experimenting with this may prove useful.

Design by T. Giesberts
[954077]



ZN436 replacement



MAINS MEASURING AID

The mains voltage level is dangerous, and possibly lethal to touch, so that extreme caution is required whenever you work on wiring or components connected to the mains. None the less, it is sometimes required to investigate the shape of the mains voltage using an oscilloscope, for instance, if you want to measure the mains current consumption of a device, or establish the degree of mains pollution caused by a certain load. The circuit described here reduces the risks of connecting an oscilloscope input to the mains to a minimum.

Design by K. Walraven

THE rule is quite simple: do not carry out direct measurements on the mains unless it is absolutely necessary, and then only you are convinced that the measurement is safe in all respects.

Be that as it may, it is sometimes necessary, or unavoidable, to connect measuring equipment directly to the mains. For instance, if you want to measure the (a.c) current consumption of a certain apparatus, or check if it distorts the mains waveform. The latter is a problem often associated with switched mode power supplies and triac-based dimmers, both of which produce high levels of interference if faulty or improperly designed.

Checking the waveform in particular can be pretty dangerous because it almost invariably requires the use of an oscilloscope, whose metal case is connected to the mains earth and the ground clip with the probe. For obvious reasons, you should make absolutely sure that the ground clip is never connected to the 'live' (L) line of the mains, because that causes (1) an extremely dangerous situation and (2) a blown domestic 13 A fuse, in that order of importance. Possibly, the short-circuit current causes damage to the equipment you are measuring on, as well as to the (expensive) oscilloscope.

Fortunately, the UK-style 3-pin mains plug and socket have an asymmetrical layout which fixes the position of the live (L), neutral (N) and earth (E) pins. Although this reduces to a great extent the chances of accidentally connecting the ground clip of an oscilloscope to the L line, the present circuit gives even greater security by making sure that the connection is always without danger.

Circuit description

The mains measuring aid was designed principally as a protection for oscilloscope measurements on the mains voltage. In addition to this function, the circuit also allows a multimeter to be connected for the purpose of current consumption measurements. Fortunately, this type of measurement is less dangerous in any case because the multimeter is not usually connected to the mains itself.

The circuit consists of two parts:

- an attenuator which reduces the mains voltage to a safe, low, level, together with a fuse and a series resistor for the current measurement;
- an optical indication to ensure that the polarity is correct. As already mentioned, this should not be a problem in the UK. This feature was added however for some continental-style earthed mains plugs (in particular the 'Schuko' type), which are of a symmetrical design and can be inserted in two ways, so you never know where the L and the N are.

The circuit diagram of the mains measuring aid is shown in **Fig. 1**. The circuit is contained in a plastic case which contains a mains socket. The connection to the mains is made via a standard three-wire cable and a 13-A fused plug. In this way, the measuring aid is easily connected between a mains outlet and the load you wish to examine.

The plug and the socket are found back at the top of the schematic. The L (live) and N (neutral) connections are connected straight through. The N (neutral) line, however, is broken to enable the series resistor and the fuse

to be inserted. So, there is an neutral 'in' (N1) and a neutral 'out' (N2). The live and earth through connections are 'tapped' and connected to the actual measurement circuit, together with the N1 and N2 lines. The measurement circuit is shown in the lower half of the schematic. The live and earth wires are connected to socket K₇, while the two neutral wires go to socket K₁. The circuit works as follows.

The 'in' neutral, N1, is connected to the 'out' neutral, N2, via the fuse, F₁, and the series resistor, R₅. The fuse is connected to K₂, and the multimeter (set to alternating voltage measurement!) is connected to the sockets indicated by K₆. For the voltage measurements, a voltage divider is connected between the live and neutral 'in' lines. This voltage divider reduces the mains voltage by a factor of 1,000, and consists of resistors R₁ through R₄. The scope or the multimeter is connected to the sockets indicated by K₅. The high resistance which then exists between K₅ and the live line makes the measurement a lot safer than without the attenuator.

That leaves us with two neon lights, one red and one green, with built-in series resistors. The green light, La₁, is connected between the live and earth line, while the red one, La₂, is connected between neutral and earth. The green neon light will be on when the unit is correctly plugged into the mains outlet. The red light comes on when the live and neutral lines are swapped, for whatever reason. Immediate action is then required to correct this situation, and the help of a qualified electric engineer should be sought. If the circuit is built for continental style mains sockets, the mains measuring aid should be plugged in the other way around.

Practical use

To clear all misunderstanding: the mains measuring aid is intended for earthed mains sockets only. Both neon lights will glow if it is connected to a non-earthed mains outlet (only in some countries). A voltage detector should then be used to check out the sockets linked to K₅ and K₆.

A BNC socket is purposely not used for the scope connection because of the possible reversal of the L and N lines in the mains wall outlet (or in the extension cord, distribution block, etc., you never know). The BNC socket having a large metal screen which is easily touched is then a possible

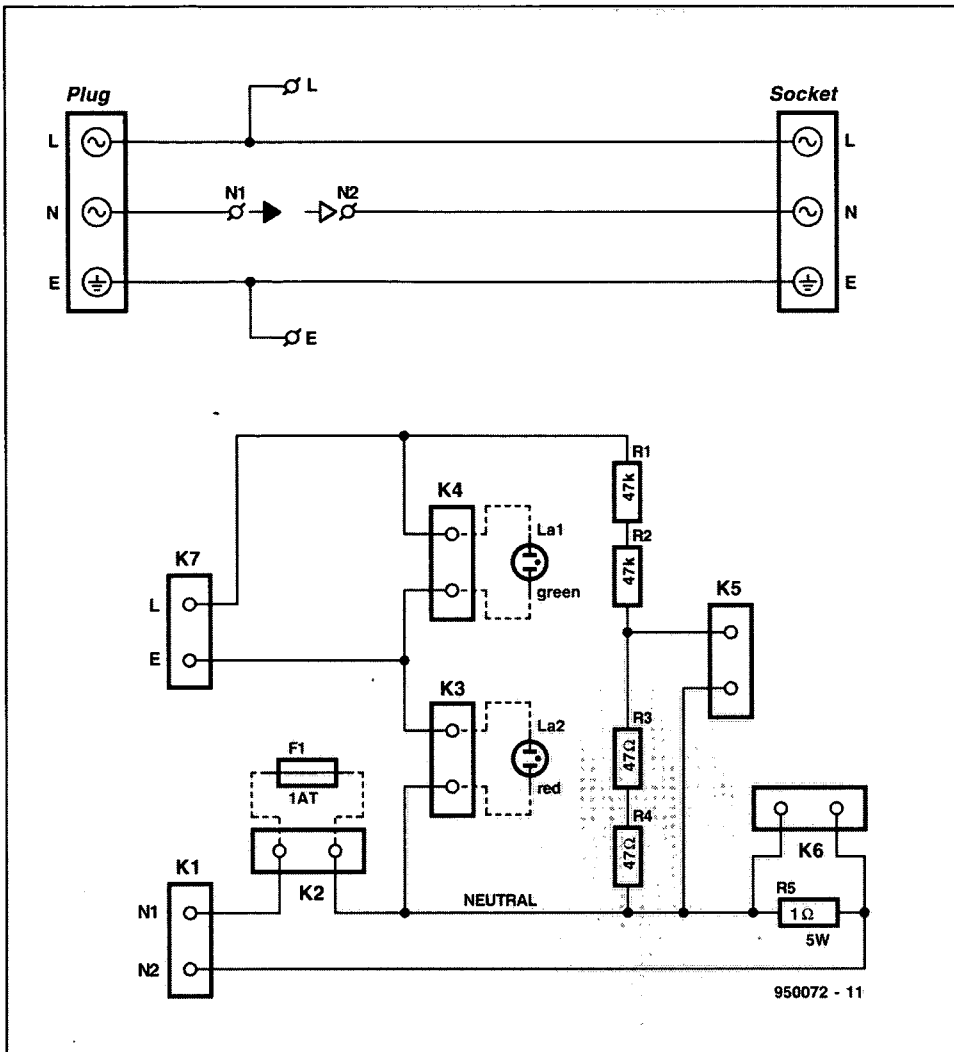


Fig. 1. Circuit diagram of the mains measuring aid. The main purpose of the circuit is to increase safety while performing voltage or current measurements involving the extremely dangerous mains voltage.

source of danger because it is at 'live' potential. Hence, we recommend using miniature banana sockets for the instrument connections, because these have slightly recessed metal parts. The possible reversal of L and N is also why the following connecting-up order **must** be followed:

1. If you wish to do measurements on a load, connect it to the socket on the mains measuring aid.
2. Plug the mains measuring aid into a mains socket. Check that the green light comes on. Do not proceed if the red light comes on, or the green and the red light at the same time, or if the fuse blows.
3. Connect the scope probe to the mains measuring aid.

Never reverse this order. If you do, a mains fuse may blow, the earth current trip detector may be set, and the case of the scope may be at mains potential very briefly.

If the mains measuring aid is connected correctly, the neutral line is

connected to the earth line via the oscilloscope. In theory, these two lines are at the same potential. In practice, however, a small voltage difference may exist, which may manifest itself by a slightly distorted measurement signal. The only safe way to eliminate this distortion is to power the oscilloscope via a 1:1 safety transformer.

Construction

The enclosure used for the mains measuring aid should be an all-ABS type, which is large enough to house the printed circuit board as well as a mains socket. The mains input cable should enter the case through a rubber grommet and a properly rated strain relief. Because the banana sockets, neon lights and the fuse holder should be accessible from the outside, these devices are connected to the circuit via screw-type PCB terminal blocks. Construction of the PCB itself (Fig. 2) is very simple indeed because the parts used are all fairly large. The resistors should be mounted at a dis-

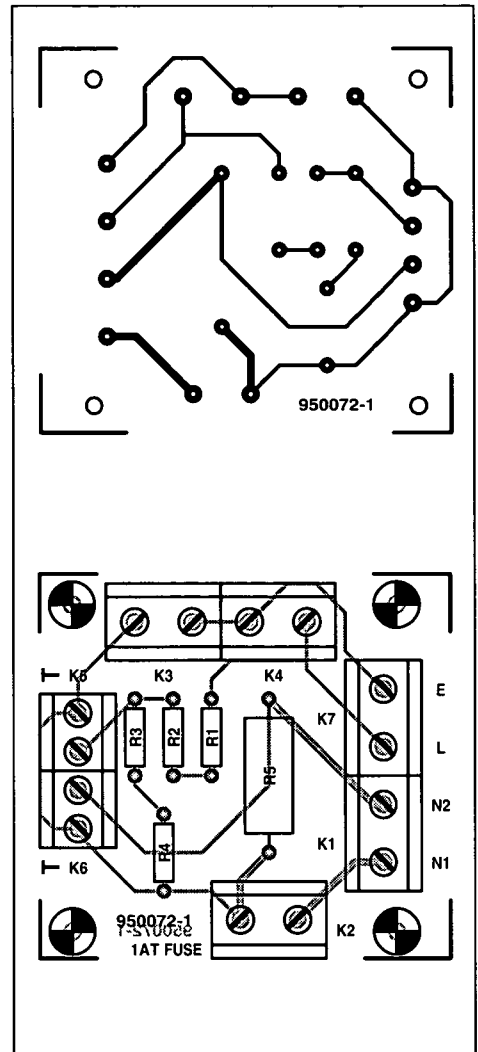


Fig. 2. Printed circuit board design (board not available ready-made through the Readers Service).

COMPONENTS LIST

Resistors:

- R₁; R₂ = 47kΩ
- R₃; R₄ = 47Ω
- R₅ = 1Ω 5W

Miscellaneous:

- K₁-K₄ = 2-way PCB terminal block, pin raster 7.5mm.
- K₅; K₆ = 2-way PCB terminal block, pin raster 5mm.
- F₁ = fuse, 1A, slow, with panel mount holder.
- La₁ = neon light, green, with internal series resistor.
- La₂ = neon light, red, with internal series resistor.
- One ABS enclosure (see text).
- Four miniature banana sockets.
- One 13A mains socket.
- One 13A mains plug, fused.
- 3-wire mains cable, approx. 1 m.
- 0.75mm² csa insulated mains wire.

The schematic capture program **Geswin** (GESECA for Windows™) adds more than a pretty face to **SpiceAge**. Upgrade £100+VAT*

- **Geswin** DDE links with **SpiceAge** to provide instant circuit editing. Because this link enables **SpiceAge** to retain all its simulation settings, the schematic (produced by **Geswin**) is uncluttered so that you can create clean drawings that may be clipboarded into your other Windows applications.
- You can clipboard sections of your netlist from **SpiceAge** back into **Geswin**'s attribute Inspector if you wish to use patches of existing circuits.
- **Geswin** has inherited **GESECA**'s speed and ease of use. You will find it's best-loved "bucket of bits" components' store waiting for your instant use from a special self-replenishing window.
- The **SpiceAge** component library has been expanded and re-drawn into "stubbies". The new symbols allow more components to fit within a given screen area without compromising clarity.
- Multiple windows allow you to scratch pad your designs (simulating as you work) and clipboard them into a fair copy window.
- File compatible with **GESECA**: schematics and components from **GESECA** may be read.
- Comprehensive **HELP** provides reference material; tutorial style manual reassures you of your own intuition.
- **Geswin** automatically invokes (or switches to) **SpiceAge**; you can also invoke **Geswin** from **SpiceAge**.

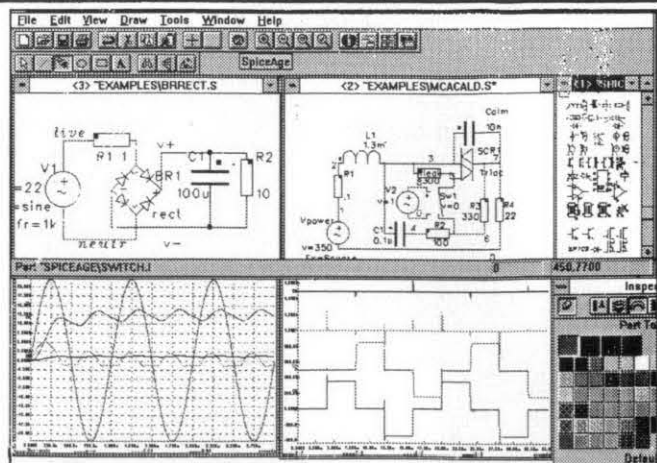
Contact your local representative

Those Engineers Ltd, 31 Birkbeck Road, LONDON NW7 4BP. Tel 0181-906 0155, FAX 0181-906 0969.

Mission Electronics, PO Box 3187, Benoni 1500, South Africa. Tel/FAX 0800 112305 or Tel 083 626 1225

Tatum Labs Inc, 1287 N Silo Ridge, Ann Arbor, MI 48108, USA. Tel 313 663 8810 FAX 313 663 3640

*UK upgrade price from **GESECA**; new price £295 + VAT
prices subject to local variations



Those
Engineers Ltd



tance of about 3 mm above the board to allow for their heat dissipation.

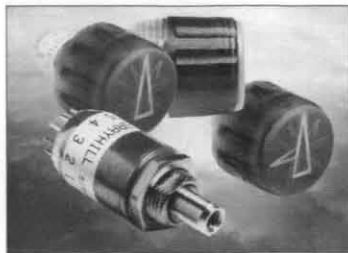
The PCB is secured to the bottom of the case with the aid of four sets of screw, PCB pillar and nut. The wiring should be installed exactly as indicated in Fig. 1. Just to make sure you get it right, here's the story in words. Connect the incoming live and earth wires straight through to the mains output socket, leaving the earth wire a little longer than the live wire. This is done to minimize hazards when the socket is accidentally dislodged from the case. Tap the earth and live connections on the output socket, and connect the wires to the 'L' and 'E' respectively on terminal block K₇. Here, again, leave the earth wire a little longer so that it remains connected in case someone accidentally pulls the wires. The neutral wire of the incoming cable is connected to 'N1' on K₁, and the neutral wire from the output socket is connected to 'N2', also on K₁. Next, connect the green neon light to K₄, the red neon light to K₃, and the fuseholder, to K₂. Use mains-rated, fully isolated wire with a minimum cross-sectional area of 0.75 mm². As regards the neon lights, be sure to purchase types with an internal series

resistor, and a screw or clamp-type fitting.

The banana sockets for the voltage and current measurements are connected to K₅ and K₆ respectively. As already mentioned, banana sockets are recommended because their metal parts are recessed and not easily touched by accident. A further advantage is that they allow easy connection of a multimeter. As a suggestion, make the distance between the banana sockets such that a BNC adaptor can be fitted. To enable the metal parts of the banana sockets to be recessed further than normal, the diameter of the holes drilled for them should be based on the metal part, rather than the plastic bush, as is more usual. Finally, a tip: remove all plastic parts from the socket before soldering. This prevents deforming of the plastic caused by the heat of the soldering iron.

After closing the case, run a final security check on the mains measuring aid. Plug in the input cable, and check that the red light is on. Next, use a voltage detector to check that none of the banana sockets is at live potential. (950072)

Rotary switches offer spring return and isolated positions



Two new facilities have been added to the range of Grayhill rotary switches available in the UK from EAO-Highland.

A spring-return feature provides momentary contact for applications such as 'hold and test' and 'hold-to-calibrate', while isolated positions provide protection against indiscriminate rotation.

Each of the spring-return switches has one or more momentary positions, and maintaining the contact at these positions requires a rotational force. Releasing the force allows the mechanism to return the contact to the normal detent position.

The isolated positions, which cannot be reached by normal rotation, involve an additional pull-to-turn operation. Releasing the shaft locks the switch in that position until the pull action is repeated.

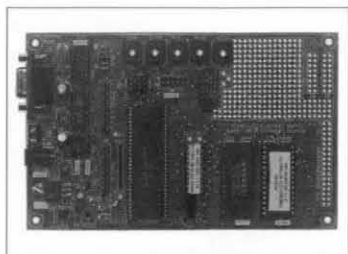
The safety positions provided by the isolation facility can be used for calibration, standby or emergency stop functions.

The switches are available with a choice of configurations, ratings, and internal circuitry. Models are available with from one to six decks, and with up to six poles per deck.

Electrical ratings are from 200 mA to 1 A, depending on the number of decks, and angle of throw may be 30° or 36°.

EAO-Highland Electronics Ltd., Albert Drive, Burgess Hill, West Sussex RH15 9TN. Tel. (01444) 236000, fax (01444) 236641.

Mitsubishi MELPS microcontroller family



Mitsubishi's versatile family of microcontrollers, called MELPS, is available in both 8 bit and 16 bit versions. These devices are 6502 upwards code compatible, and in addition offer a code superset. The 16-bit devices are particu-

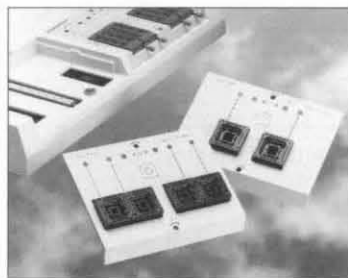
larly interesting as they are hardly more expensive than the 8-bit types, but can run at up to 25 MHz making them very powerful controllers indeed.

Cross assemblers are available from, among others, Pentica and Mitsubishi themselves. To assist programmers developing applications based on MELPS devices, dB Electronic Design offer a development kit which includes a single-Eurocard MELPS-based computer with 32K RAM, 32K ROM, a monitor, RS232 serial link, analogue and digital I/O, a prototyping area, full documentation and a PC-compatible MELPS family cross-assembler.

Applications of the development kit include a low-cost introduction to assembly programming, low-volume embedded control applications, Mitsubishi MELPS family software and hardware development, education, test equipment (e.g., programmable signal generators), data logging, and more!

dB Electronic Design, 347 Ware Road, Hertford SG13 7EL. Tel. (01992) 553903, fax (01992) 505903, e-mail 100407.1174.

Gang programming 68HC711 micros



The L9000 programmer from LLOYD Research Ltd. can now program PLCC versions of the 44 and 52-pin members of the Motorola 68HC711 family. The PL71 module has four PLCC sockets for programming the 68HC711D3. The L9000 mainframe downloads a small program to each micro, and does not rely on Motorola's 'prog' mode function. Two such modules can be fitted so that eight devices can be programmed in parallel.

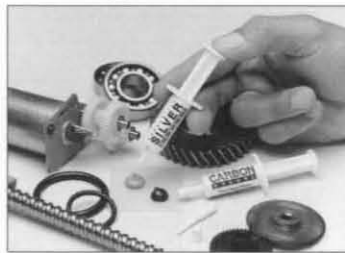
Larger devices such as the 68HC711E9/E20/E32 are accommodated in the PL71E module which has 52-pin PLCC sockets. As the L9000 does not use 'prog' mode, it is also possible to program the EEPROM and configuration register. For volume production, a second module can be fitted.

Other modules in the L9000 range provide for programming Motorola micros such as the 68HC705C8/9 and P9 as well as EPROMs in DIL, PLCC and LCC packages.

The L9000 is believed to offer support for a wider range of microcontrollers than any other comparable programmer.

Lloyd Research Ltd., 7 & 7A Brook Lane, Warsash, Southampton SO31 9FH. Tel. (01489) 574040, fax (01489) 885853.

Conductive silver and carbon greases

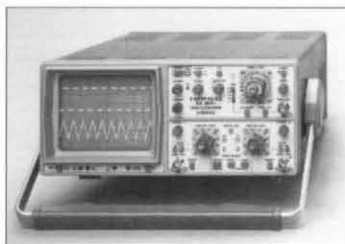


At first glance, new Circuit Works conductive greases do what all greases do, they reduce friction, heat and wear when applied as a surface coating to moving parts. But while traditional greases are insulators, Circuit Works greases are excellent conductors of electrical and thermal (type 7100 silver grease only) energy. In addition, the new greases offer unparalleled protection from moisture, corrosion and other environmental hazards.

These new greases lubricate and protect assemblies while forming conductive pathways, contacts, connection, static drains and grounding. This unusual combination of properties makes Circuit Works conductive greases extraordinarily useful in a wide variety of applications. Available in silver and carbon formulas, these greases can solve many of the most difficult lubrication, electrical and thermal management challenges.

Intertronics, Unit 9, Station Field Industrial Estate, Banbury Road, Kidlington, Oxon OX5 1JD. Tel. (01865) 842842, fax (01865) 842172.

New Hameg HM303 'scope



The new Hameg HM303 standard oscilloscope succeeds the HM203, which sold over 170,000 worldwide. The bandwidth has been extended to 30 MHz, a lighter weight of only 5.6 kgs and a lower panel height reduced by 20 mm has been achieved by incorporating a switch-mode power supply. Another advantage is that the new oscilloscope will work from a mains supply of between 90 and 240 V a.c., without adjustment.

Brief specification:

- Dual channel, d.c. to 30 MHz, 2 mV/div.; overscan indicator.
- Time base: 10 ns to 0.5 s/div.; variable hold-off; x10 magnification.
- Triggering: d.c. to 100 MHz; active TV-sync separator; LED trigger indication.

- Additional features: component tester, 1 kHz/1 MHz calibrator.

The new Hameg HM303 oscilloscope is priced at £392 plus vat, which included two switched probes and a manual. Carriage is free of charge.

BK Electronics, Unit 1, Comet Way, Southend-on-Sea, Essex SS2 6TR. Tel. (01702) 527572. Fax (01702) 420243.

Affordable schematic editor for Windows

New from CRaG Systems is WinDraft, a complete 32-bit schematic design tool designed specifically for Windows. WinDraft is an ideal front-end for the WinBoard PCB layout package and costs just £495.

Some of the unique features available on the easy to learn and use package include: the ability to draw several parallel wires at once by simply pressing the + or - key to increase or decrease the number of wires; automatic insertion of components into existing wires; scaling of components using the + and - keys; automatic junction placement when the user ends a wire on another wire and direct pin name editing from the schematic editor without having to go through the on-line graphical library editor. Forward and backward annotation is provided as well as post processors such as Bill of Materials (BOM) and automatic annotation.

The familiar Windows interface is intuitive, easy to learn and easy to remember. The program starts with the full colour toolbar with easily recognisable icons. A floating toolbar may be selected to provide the user with drawing tools right on the sheet. A single mouse click on an object allows editing and a double mouse click brings up a dialog box to change object parameters. This easy to remember context sensitive editing is the same as provided in the WinBoard PCB layout program. The program offers the convenience of keyboard shortcuts as an alternative to mouse and menu commands.

WinDraft contains a library of over 10,000 analogue and digital parts, including ansi/ieee formats. In addition, the program loads OrCAD SDT 386 files and libraries. The open database and ASCII file formats allow users easily to integrate files with their applications and those of other vendors. The program offers full hierarchical support and when the user creates a hierarchical design, the program automatically sets up the connectors between sheets at the different levels. In addition, WinDraft is Multiple Document Interface (MDI) compliant and includes complete Electrical Rules Checking (ERC) functions. The program comes complete with a printed user manual and context-sensitive on-line help that includes the complete reference manual.

CRaG Systems, 8 Shakespeare Road, Thatcham, Newbury, Berkshire RG18 3FQ. Tel. (01635) 873670, fax (01635) 868557. (955035)