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# **ELEKTOR ELECTRONICS**

THE INTERNATIONAL  
ELECTRONICS MAGAZINE

## **DSP FUNCTION GENERATOR**

**Stepper motor ICs**

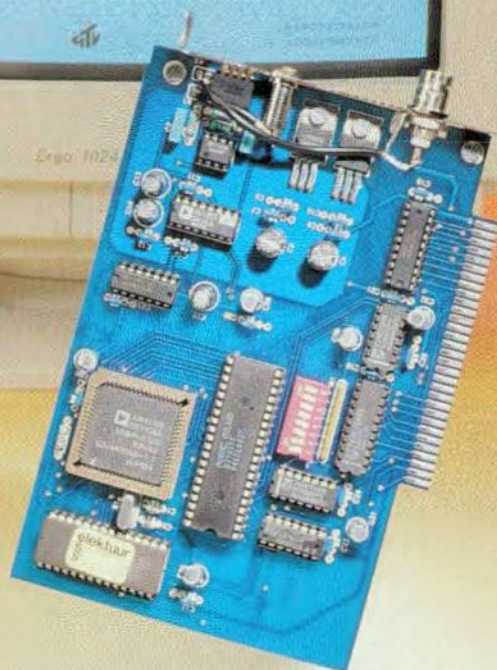
**Wideband active  
loop antenna**

**TDA1560Q: a 30 W  
audio amplifier  
for cars**

**Long-life  
night light**

**Telephone-controlled  
mains switch**

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MICROCONTROLLER  
DEVELOPMENT  
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- Stepper motor control
- Electronic barometer
- Simple function generator
- Bat detector
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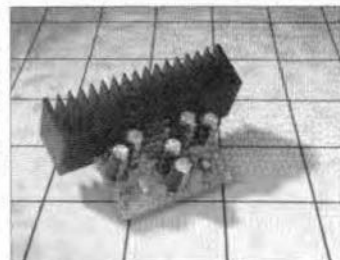
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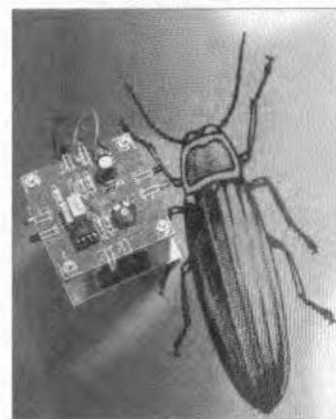
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# 30 W AF AMPLIFIER FOR CARS

Design by T. Giesberts

The power that can be obtained from a standard car radio amplifier operating from a 12 V car battery is 5–6 W, which (for many listeners) is not really enough for satisfactory hi-fi reproduction. It is, of course, possible to boost the 12 V supply with a power inverter, but that is fairly expensive and not always acceptable. Now, a Philips IC enables audio power of about 30 W to be obtained from a 12 V car battery.



Until not so long ago, the Class B output stages of a standard car radio could not deliver more than  $2 \times 5\text{--}6 W_{\text{rms}}$  into  $4 \Omega$  loudspeakers. More was not possible with a single supply line of 12 V. Most modern car radios use bridge amplifiers to boost the output to 12–16 W. Often, each of the four loudspeakers has its own dedicated amplifier. Many car manufacturers do not like the use of power inverters to raise the on-board voltage out of fear that these can cause (embarrassing or even dangerous) interference with the remainder of the electronic systems in the car (of which there can be many). There is also the problem of heat generation in the output stages, which may necessitate forced cooling.

## Class H

Electronics manufacturers have been researching ways and means of obtaining adequate output power without the use of a power inverter, and Philips have come up with the TDA1560Q.

Output amplifiers can be arranged in a number of different configurations, of which most audio enthusiasts only know Class A and Class B. A different one that provides fairly high output power with relatively low dissipation is Class G. In this configuration, use is made of two supply voltages: a fairly low one that is constantly available and a much higher one that becomes available only when the the voltage swing of the output stages can not be sustained by the low supply voltage.

Since in cars only one supply voltage is available, Philips engineers have devised a pseudo Class G configuration in which a number of electrolytic capacitors are charged by the battery voltage. During brief voltage peaks in the output signal, semiconductor switches connect these capacitors in series with the 12 V line so

that the supply voltage to the amplifier is temporarily doubled. Since this is a further development of the Class G technique, it is named Class H. The (temporary) 24 V supply to the amplifier enables (theoretically) a power of 80 W to be delivered into  $4 \Omega$  or 40 W into  $8 \Omega$ .

A simplified diagram of a Class H

output amplifier is shown in **Fig. 1**. It contains two principal circuits: the first is a Class B amplifier,  $T_1\text{--}T_4$ , which is loaded by  $R_1$ , and the second raises the internal supply voltage. The second circuit uses two external capacitors,  $C_1$  and  $C_2$ , which serve as supply buffers.

Since a music signal consists only

## Brief Technical Data

### Class H operation

Low dissipation with music signals

Extensive protection circuits (output current; temperature; load impedance)

Supply voltage 12 V nominal

Quiescent current 100 mA

### Output power

(1 kHz sinusoidal, THD = 0.5%) 30 W r.m.s. into  $8 \Omega$

(music signal) 40 W into  $8 \Omega$

THD + noise (1 W into  $8 \Omega$ )  $\ll 0.01\%$  (1 kHz)

THD + noise (20 W into  $8 \Omega$ )  $\ll 0.05\%$  (20 Hz to 20 kHz)

THD + noise (20 W into  $8 \Omega$ )  $\ll 0.06\%$  (1 kHz)

THD + noise (20 W into  $8 \Omega$ )  $\ll 0.2\%$  (20 Hz to 20 kHz)

Power bandwidth (–3 dB)

5 Hz to 100 kHz

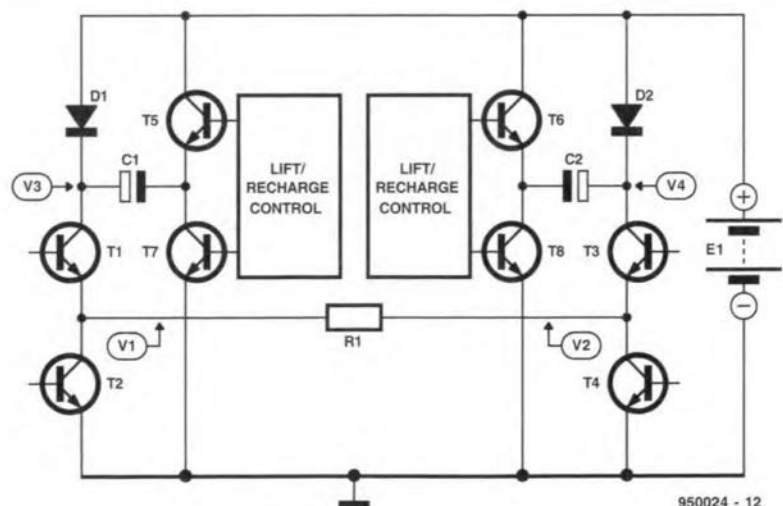


Fig. 1. Diagram of a basic Class H amplifier.

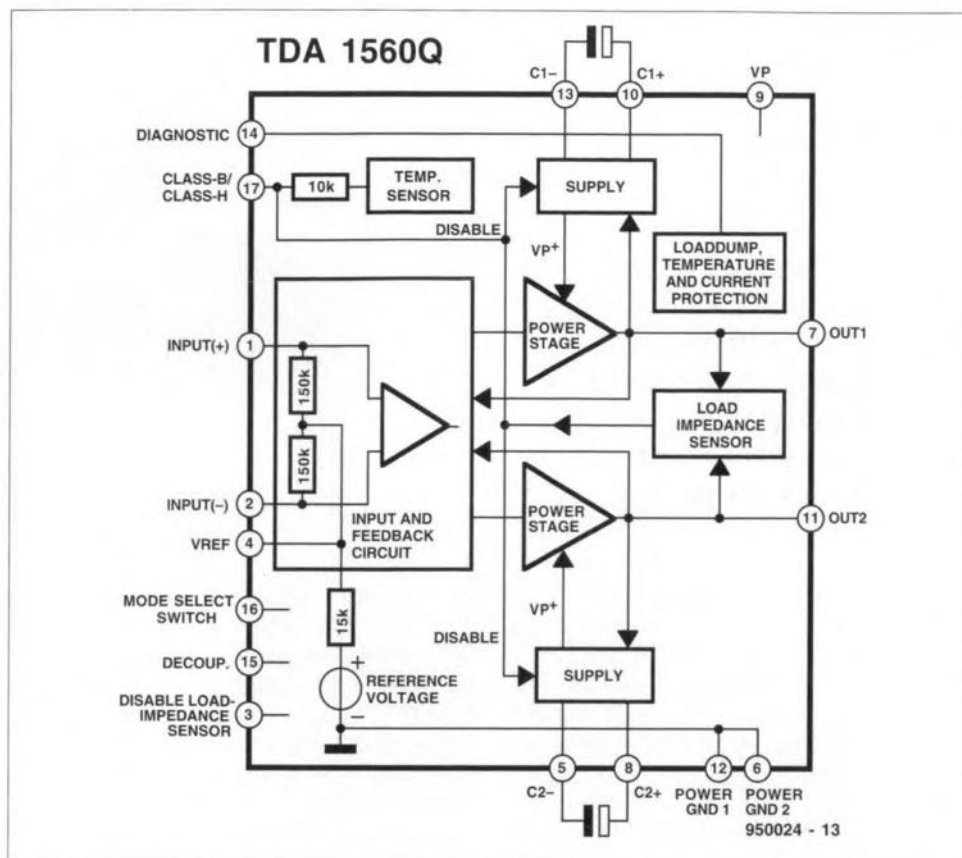


Fig. 2. Block diagram of the TDA1560Q

for a small part of high level components, the supply voltage needs to be raised for a small part of the time only.

Because the supply voltage is raised for short periods of time only, the average dissipated power will be only slightly higher than that of an

amplifier without a voltage-raising circuit, in spite of the fact that the peak output power is appreciably higher.

Capacitors  $C_1$  and  $C_2$  are charged through current sources  $T_7$  and  $T_8$  to a voltage which is nearly equal to the supply voltage,  $E_1$ . When either volt-

age  $V_1$  (or  $V_2$ ) rises and  $T_1$  (or  $T_3$ ) approaches the saturation voltage, the lift control circuit detects this. Lift transistors  $T_5$  and  $T_6$  then conduct, so that the charged capacitors are switched between the collector of  $T_1$  (or  $T_3$ ) and supply voltage  $E_1$ . Diodes  $D_1$  and  $D_2$  prevent the capacitors being discharged via the battery. Voltage  $V_1$  (or  $V_2$ ) can increase to nearly twice the supply voltage. The lift/recharge control circuit ensures that  $T_5$  and  $T_7$ , and  $T_6$  and  $T_8$ , can not conduct simultaneously.

### Inside the TDA1560Q

A block diagram of the TDA1560Q is shown in Fig. 2. A differential input stage in the input and feedback circuit is connected to pins 1 and 2. Because of this stage, the IC is highly insensitive to common-mode interference. The input impedance is 300 k $\Omega$ , so that for a good low-frequency response even small input capacitors are sufficient.

The input and feedback circuit contains circuitry that controls the supply circuits and the power stages.

The control circuitry monitors the input signal and anticipates saturation of the output transistors. As soon as this happens, the supply voltage is raised. Because the input signal is monitored, it is possible to control the lift voltage. To keep the dissipation at a minimum, the supply voltage is raised only to a level where the output will stay below the clipping level.

A current limiter protects the out-

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put stages against being short-circuited to ground or to the supply line. In general, whenever the current drawn exceeds a level of 5.5 A, the output and the power stages are switched off. The protection circuit monitors at short intervals whether the short-circuit has been removed. If so, the output stages are reactivated. This arrangement limits the dissipation in the power stages during short-circuits to a minimum.

There is a dual temperature protection. The first switches off the voltage doublers when the temperature of their cases rises above 120 °C. The amplifier can then operate in Class B only. The second protection uses sensors located close to the output and switching transistors. If these sensors measure a temperature higher than 165 °C, the base current of the associated transistor is lowered.

There is also a circuit that monitors the load impedance. After the amplifier has been switched on, the d.c. resistance of the loudspeaker(s) is determined by passing a current through the speaker coil(s) and measuring the consequent voltage drop across it. Because of the peak current that the power stages can handle, the Class H section is switched off when a 4 Ω loudspeaker is detected. The IC then operates as a Class B amplifier. When the load impedance drops below 0.5 Ω, it is considered a short circuit and the entire IC is disabled. The impedance sensor is very sensitive and may be actuated by spurious pulses (for instance, when a car door gets closed during switch-on: the loudspeakers then act as microphones). The sensor may be disabled by shorting pin 3 to ground.

Finally, the IC contains an internal reference voltage source for the input circuits. This reference is decoupled by a capacitor at pin 4.

## Circuit description

The circuit diagram of the 30 W AF amplifier is shown in **Fig. 3**. The input is connected to the differential input stage (pins 1 and 2) via coupling capacitors  $C_1$  and  $C_2$ . Although the -ve input is linked to earth via wire bridge A-B, the arrangement gives good common-mode rejection in spite of the asymmetrical input. A true symmetrical input is obtained when wire bridge A-B is omitted from the board. Network  $R_1$ - $C_3$  forms a low-pass filter that suppresses HF interference at the input. The input impedance is determined largely by the value of  $R_2$ .

The circuit around darlington  $T_1$  provides a delay at switch-on to suppress switching noise reaching the output stages. This is essential since

the impedance measuring sensor (which normally provides the suppression) has been disabled here (pin 3 to ground).

As soon as the supply voltage is on, a potential of 3 V is applied to pin 16 via  $R_3$  and  $D_1$  to place the IC in the mute mode. Initially, since  $C_{10}$  is discharged,  $T_1$  remains off. However, the capacitor then gets charged via  $R_4$  and within a few seconds the voltage across it has risen to a level at which  $T_1$  begins to conduct. This results in a voltage of 12 V being applied to pin 16, whereupon the power stages operate normally.

Various facilities are open to the user via pin 14. For instance, it may be used to detect whether one of the protection circuits is working. Normally, this pin is at the level of the supply voltage. If its potential is only half that value, one of the protection circuits is actuated. When the pin is linked to ground via jumper  $JP_1$ , the amplifier is muted. When the jumper is connected to +12 V, all protection circuits are disabled. For normal operation, therefore, no jumper should be placed at  $JP_1$ .

Capacitors  $C_{15}$  and  $C_{16}$  buffer the 12 V battery voltage. Capacitors  $C_{11}$ - $C_{12}$  and

$C_{13}$ - $C_{14}$  are required by the lift/control circuit. Two parallel-connected 4700 µF electrolytic capacitors are used in each case, because these take up less space on the board than a single 10,000 µF component. Networks  $R_6$ - $C_6$  and  $R_7$ - $C_7$  are interference suppressors.

A Boucherot network,  $R_8$ - $C_8$  and  $R_9$ - $C_9$ , is provided at each loudspeaker terminal to maintain a 'normal' load at high frequencies (at which the loudspeaker impedance rises appreciably owing to its inductive behaviour).

## Construction

The construction is limited to populating the printed-circuit board shown in **Fig. 4**. The IC must protrude slightly from the board so that it can be fitted flush against the heat sink. An insulating washer between IC and heat sink is a must: apply heat conducting paste to both the base of the IC and the heat sink. The insulating washer may have to be cut to size from a mica T03 washer.

Most constructors will use two amplifiers in one enclosure for a compact stereo setup. It is, however, also possible to use four amplifiers in one case: one for each

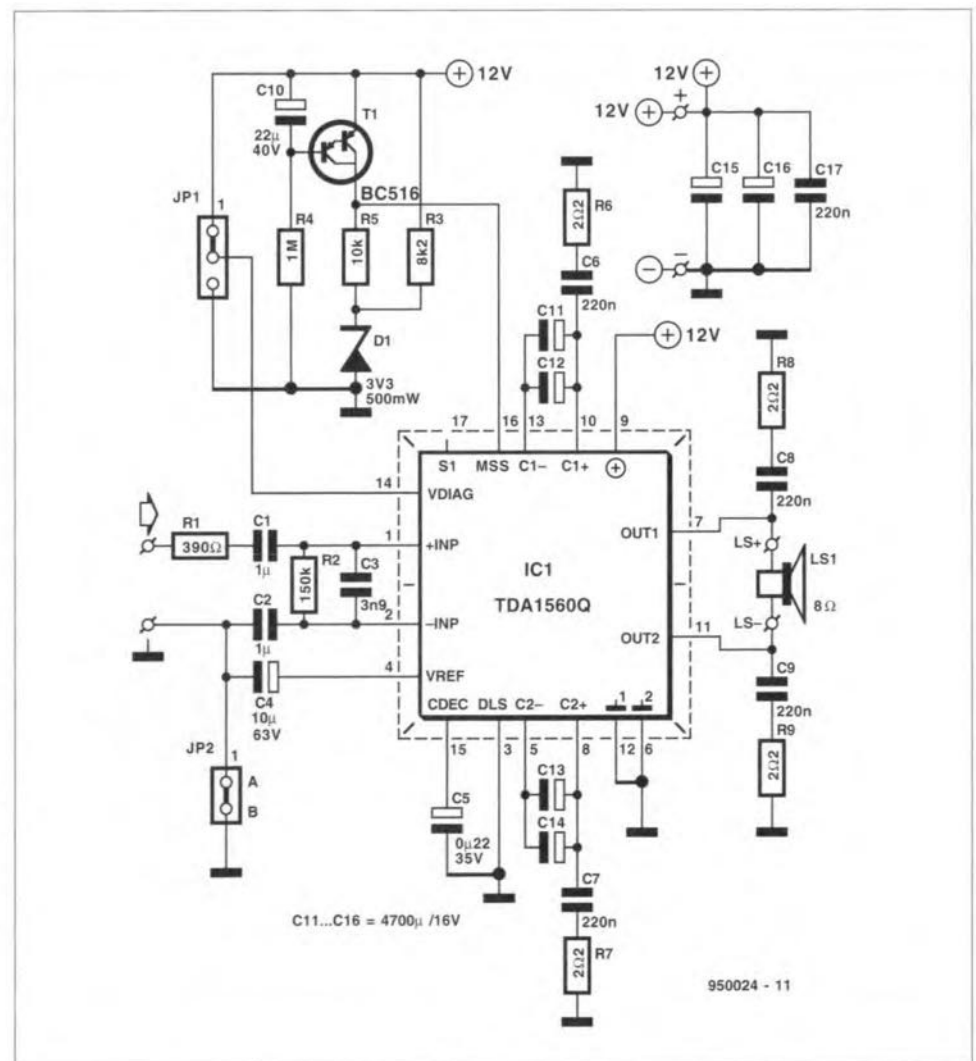


Fig. 3. Circuit diagram of the 30 W AF amplifier for cars.

of the two front and rear speakers. Make sure that none of the loudspeaker cables or terminals can touch the chassis, because that does not do the bridge amplifier any good in the long term in spite of the protection circuits.

## Parts list

### Resistors:

$R_1 = 390 \Omega$   
 $R_2 = 150 \text{ k}\Omega$   
 $R_3 = 8.2 \text{ k}\Omega$   
 $R_4 = 1 \text{ M}\Omega$   
 $R_5 = 10 \text{ k}\Omega$   
 $R_6 - R_9 = 2.2 \Omega$

### Capacitors:

$C_1, C_2 = 1 \mu\text{F}$ , pitch 5 mm  
 $C_3 = 3.9 \text{ nF}$   
 $C_4 = 10 \mu\text{F}$ , 63 V, radial  
 $C_5 = 220 \text{ nF}$ , 35 V, tantalum  
 $C_6 - C_9, C_{17} = 220 \text{ nF}$   
 $C_{10} = 22 \mu\text{F}$ , 40 V, radial  
 $C_{11} - C_{16} = 4700 \mu\text{F}$ , 16 V, radial

### Semiconductors:

$D_1 = \text{zener}$ , 3.3 V, 500 mW  
 $T_1 = \text{BC516}$

### Integrated circuits:

$IC_1 = \text{TDA1560Q}$

### Miscellaneous:

Heat sink for  $IC_1$ ;  $R_{th} \ll 2.5 \text{ K W}^{-1}$   
 PCB Order No. 950024-1

[950024]

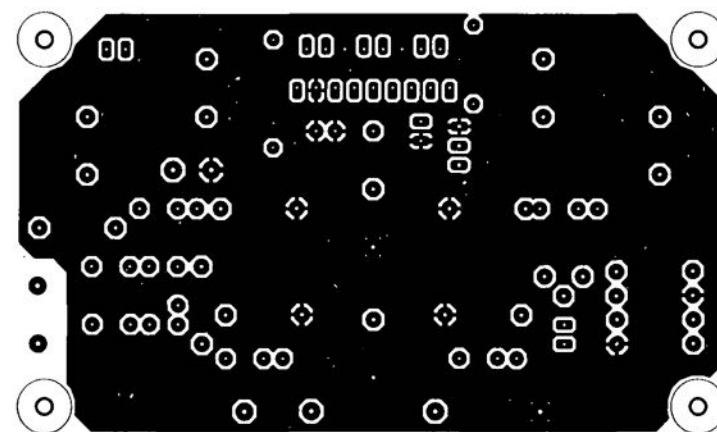
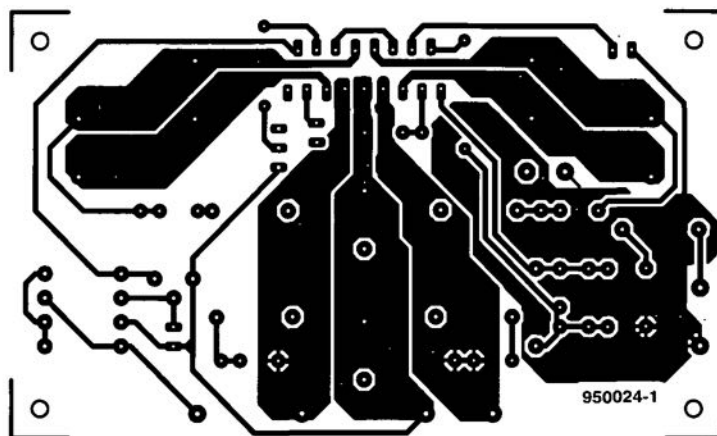
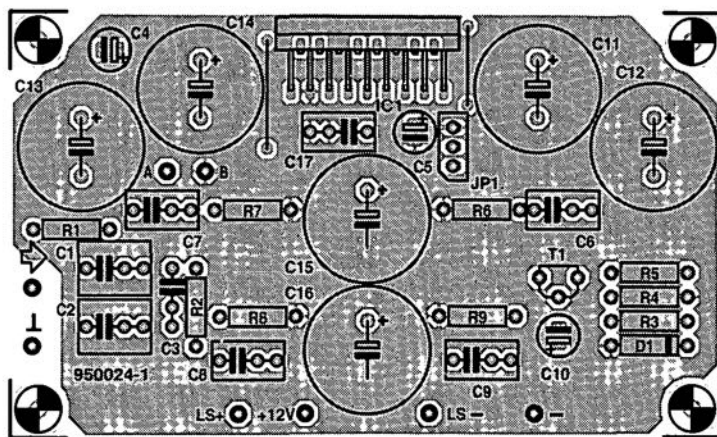


Fig. 4. Printed circuit board for the 30 W AF amplifier for cars.

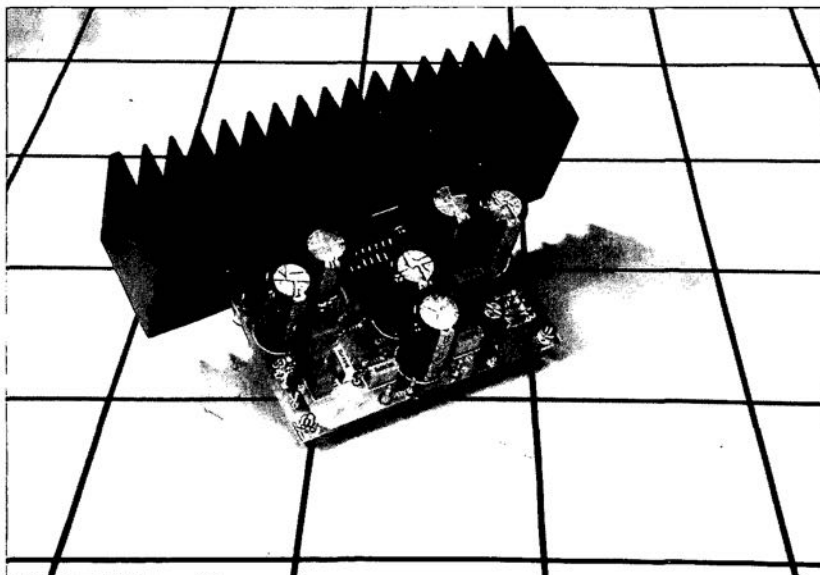


Fig.5. The completed (prototype) 30 W AF amplifier for cars.

# WIDEBAND ACTIVE LOOP ANTENNA

Wideband antenna design is problematic because size and performance are conflicting aspects. The wideband antenna described in this article covers the long, medium and shortwave bands up to about 50 MHz, and achieves excellent efficiency while remaining reasonably sized.



Design by J. Barendrecht

**M**ANY shortwave DXers lack the space to erect a large, tuned, antenna, and have to resort to much smaller alternatives. Not surprisingly, these are nearly always active antennas, which are expected to do 'the impossible' (well, almost). Ideally, they should have a low noise level, good large signal handling, wideband characteristics with a stable output level across the entire frequency range, and, last but not least, they should be usable in areas with a high noise level (i.e., in and around the city). Unfortunately, you can not expect all that from an active antenna. Low noise and a wideband response, for instance, are contending aspects, while immunity against man-made noise is very difficult to achieve. However, if the latter aspect is the most important (and in many cases it will, unless you live in the middle of nowhere), there is

no alternative than to use a rhombic or loop antenna, which (ideally) responds to the magnetic component only of the energy picked up from the transmitter. Because it ignores electric components, this type of antenna keeps out a lot of man-made interference.

However, choosing a loop antenna does not solve all problems because good wideband response is difficult to achieve with this type of antenna. The voltage induced in the antenna drops significantly below the resonance frequency. At higher frequencies, too, problems occur because the induced voltage is in series with the loop's self-inductance. This, in combination with the amplifier's input capacitance, creates a low-pass filter with a roll-off frequency which can be so low that it becomes a troublesome factor. Consequently, it is essential to ensure proper matching between the passive

part of the antenna (i.e., the loop) and the active part (i.e., the amplifier). In all cases, however, the best you will be able to achieve is still a trade-off.

## A MOSFET amplifier

Recapping the above, the active part of the antenna should couple good large signal behaviour with low noise, and in addition present a very low input capacitance.

The circuit diagram shown in **Fig. 1** shows the amplifier sitting between the loop (which will be reverted to) and the phantom power supply. A dual-gate MOSFET,  $T_1$ , is used as a transconductance amplifier to match the impedance of the loop to that of the output coax cable. Transistor  $T_2$  is the actual amplifying device. Some of you may wonder about the use of the BF981 MOSFET, which would appear to be designed for VHF/UHF applications only. However, the specifications of this MOSFET indicate that it also has low noise at lower frequencies, provided its very high input impedance is properly matched.

Input matching is not a problem at relatively low frequencies. The loop antenna used here has a diameter of about 1 m (3 feet), and its low impedance at low frequencies is easily stepped up. Problems occur at higher frequencies, however, because then the self-inductance of the loop (approx. 5  $\mu$ H) is also stepped up, and starts to cause trouble. The BF981 has an input capacitance of about 2 pF, while the capacitance of a regular input transformer lies between 0.5 pF and 1 pF. Some form of damping is, therefore, required to prevent unwanted resonance peaks. Although that can be achieved by the simple addition of a resistor, everything possible has to be done not to attenuate the already weak signals picked up by the antenna. Hence, some means of damping the loop has to be devised which does not unduly attenuate the RF signal.

The problem is not new, of course, and had to be contended with in the design of RF stages in early FM receivers using valves. Triodes offered a lower noise figure than pentodes, but only if neutralizing (or 'neutrodyne') techniques were applied. If that could not be done, there was the grounded grid amplifier to resort to. Not a good alternative, though, because it had a higher noise figure, and offered less gain.

A compromise was found in the  
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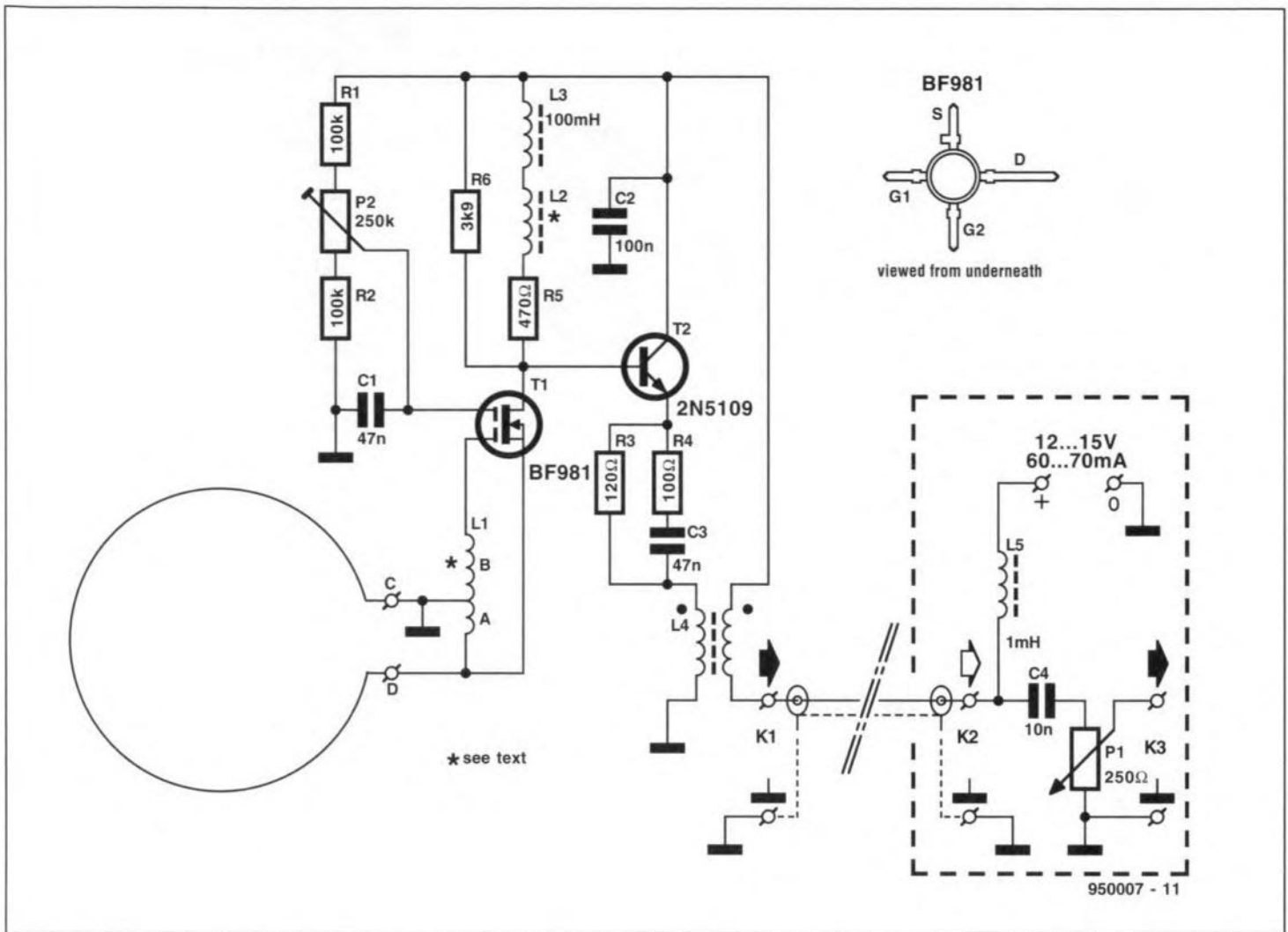


Fig. 1. The heart of the active antenna is formed by dual-gate MOSFET T1, a BF981. The antenna proper consists of a loop with a diameter of about 1 m.

inter-grid or inter-base amplifier. This type of bridge circuit required no neutralizing, and did not degrade the noise figure with respect to the common-cathode amplifier.

The amplifier used here revives the above technology, and may be called an inter-gate type (the electrical behaviour of a MOSFET being very similar to that of a thermionic valve). This circuit is easy to recognize from the fact that the source of the MOSFET is connected to the input transformer rather than to ground, while the tap on the transformer is connected to ground. The amplifier is therefore, best classified between a grounded-gate and a grounded-source circuit.

Here, the choice of an inter-base circuit has nothing to do with avoiding neutralization as in the valve era — the prime design targets are now (1) matching and (2) damping. As already mentioned, there are no problems at relatively low frequencies. The output impedance of T1 (approx. 100 Ω) is then insignificant, and the gate-source voltage is about six times the voltage induced in the loop. From about

3.4 MHz, the source input starts to act as a damping resistance, which eliminates resonance effects while extending the bandwidth of L1. Precisely what we are after!

As a matter of course, the damping reduces the signal level supplied by the loop. The loop output voltage being small already, the MOSFET has to provide considerable gain at higher frequencies also. This has been achieved by inserting an inductor-resistor combination, R5-L2, between the drain of T1 and choke L3. The RL combination ensures a high drain impedance at higher frequencies also, because L3 then has a fairly high capacitive reactance. Resistor R6 keeps the gain of T1 within reasonable limits.

The amplified signal is coupled out via emitter follower T2 and a bifilar output transformer, L4. From there, the signal is fed to the input of the receiver. At the receiver side, a small passive network is fitted. A potentiometer, P1, is available to reduce the input signal when necessary. This control will be particularly useful when the active antenna is used with a re-

ceiver suffering from poor or average large-signal handling.

Choke L5 and capacitor C4 allow the RF signal and the preamplifier's supply voltage to be carried via the same coax cable. In most cases, it will be possible to take the supply voltage from the receiver. If not, the simplest of regulated power supplies is also fine, the current consumption of the preamplifier being modest at between 60 mA and 70 mA.

## The loop antenna

The antenna proper consists of a loop with a diameter of about 1 m. Ideally, the loop should be made from metal tubing with a diameter of about 20 mm. The choice of metal is not so important. Plate material or even rectangular tubing of the same width may be used also. Ordinary copper wire is not suitable because it is too thin.

Those of you who live outside Europe may make the loop much larger to increase the output voltage and the signal-to-noise ratio. In Europe, a diameter of about 1 m is just



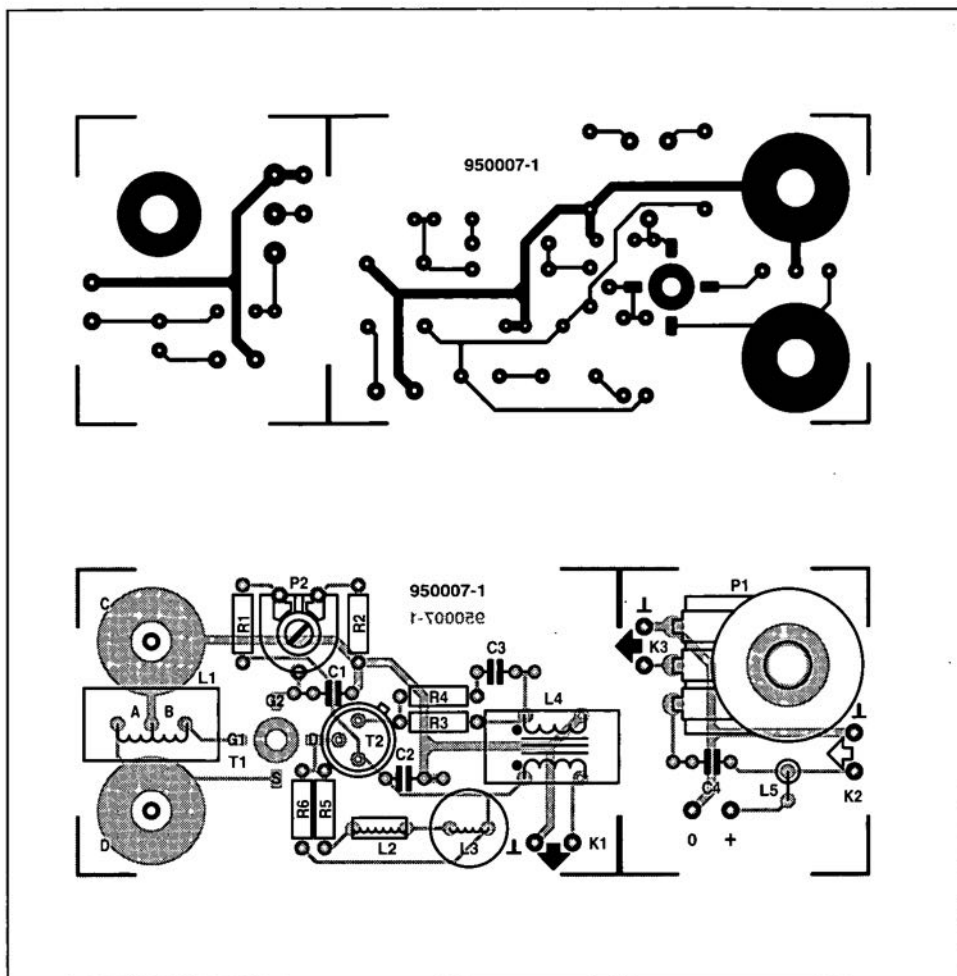


Fig. 2. The printed circuit board consists of two sections, which should be separated before they are populated. The section which has the potentiometer (P1) on it corresponds to the sub-circuit in the dashed box in Fig. 1.

about the maximum because of the very high signal levels which exist as a result of the area being the target of a very large number of short-wave broadcast transmitters. Increasing the loop diameter will, therefore, almost certainly cause input blocking effects in the receiver. A smaller loop is, of course, possible, although that will reduce the performance.

## Construction

The artwork of the printed circuit board designed for the active antenna is shown in Fig. 2. Unfortunately, this board is not available ready-made through our Readers Services, so you will have to make it yourself. Two important points have to be mentioned with respect to this board. The first is that the right-hand section has to be cut off because it holds the sub-circuit which is fitted inside or near the receiver. Secondly, the loop ends must be connected directly to points 'C' and 'D' on the board. In practice, it is best to secure the board between the loop ends.

Populating the board is straightforward with the possible exceptions of

mounting  $T_1$  and making the inductors. The MOSFET,  $T_1$ , is fitted at the **copper** side of the board. Its type number should be legible when looking through the hole in the board from the component side. The longest terminal of the device is the drain (see also the pinout inset in Fig. 1).

The circuit has a total of five inductors. Three of these,  $L_1$ ,  $L_2$  and  $L_4$ , are home-made, while  $L_3$  and  $L_5$  are off-the-shelf chokes.  $L_2$  consists of 20 turns of 0.4-mm dia. enamelled copper wire, and has an internal diameter of 6 mm. No core is used, and the inductor may be wound on, say, a PCB spacer.  $L_1$  and  $L_4$  are both wound on a ferrite ring core type G2.3-FT16.  $L_1$  consists of 24 turns with a tap at 4 turns;  $L_{1A}$  has 4 turns, and  $L_{1B}$ , 20 turns. Use 0.4 mm dia. (28SWG) enamelled copper wire.  $L_4$  is wound with slightly thinner wire (0.3 mm dia, 30SWG), and has two bifilar windings of 4 turns each. Bifilar means that you wind two wires at a time, so that the inductor halves run alongside each other. In all home-made inductors, the wire is close-wound, i.e., it is not spaced.

The prototype of the preamplifier

## COMPONENTS LIST

### Resistors:

$R_1, R_2 = 100k\Omega$   
 $R_3 = 120\Omega$   
 $R_4 = 100\Omega$   
 $R_5 = 470\Omega$   
 $R_6 = 3k\Omega$   
 $P_1 = 250\Omega$   
 $P_2 = 250k\Omega$  preset H

### Capacitors:

$C_1, C_3 = 47nF$  Sibatit (Siemens)  
 $C_2 = 100nF$  Sibatit (Siemens)  
 $C_4 = 10nF$  Sibatit (Siemens)

### Inductors:

$L_1 = 24$  turns 0.4 mm CuL (A = 4 turns, B = 20 turns), on ferrite ring core G2.3-FT16\*.  
 $L_2 = 20$  turns 0.4 mm CuL, no core, diameter 6 mm.  
 $L_3 = 100mH$  (Toko 10RB-181LY-104).  
 $L_4 = 4+4$  turns 0.3 mm CuL, bifilar on ferrite ring core G2.3-FT16\*.  
 $L_5 = 1$  mH (Toko).

### Semiconductors:

$T_1 = BF981$   
 $T_2 = 2N5109$  (SGS Thomson)

### Miscellaneous:

$K_1, K_2, K_3 =$  BNC-socket.  
 PCB not available ready-made through the Readers Services.

\* C-I Electronics, P.O. Box 22089, NL-6360-AB Nuth, The Netherlands. Fax: (+31) 45 241877.

board is shown in Fig. 3. The photograph gives a fair indication of the construction of the home-made inductors.

Finally, a word about fitting the circuit into a case. The case should be a plastic type. If the antenna is installed out of doors, a watertight case should be used. Connectors  $K_1$ ,  $K_2$  and  $K_3$  should be good-quality BNC types.

## Adjustment

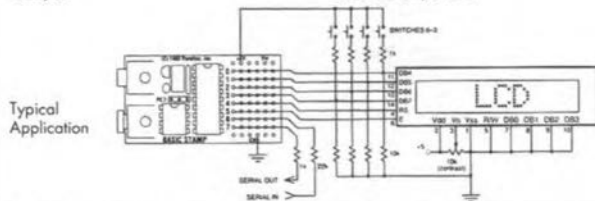
You do not need expensive test equipment to adjust the active antenna. A multimeter, a short-wave receiver and a good sense of hearing are all that is needed.

To begin with, adjust preset  $P_2$  until the voltage at the drain of  $T_1$  is 1 V higher than half the supply voltage, i.e., 7 V if the supply voltage is 12 V, or 8.5 V if the supply voltage is 15 V. Next, check during the evening hours that signals in the 41-m, 31-m and 25-m broadcast bands are sufficiently

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PIC 16C71/84 TrueFlight	•	•	•	•	•	•	•	•	•	•	•	16	
BackDraft 17	•												PLCC
ClearView '5x		•	•	•	•	•	•	•	•	•	•	20	
ClearView 'xx												20	
B.I.O.C Compiler				•	•	•	•	•	•	•	•		
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PIC Prototyping Boards													
Parallax Assembler				•									
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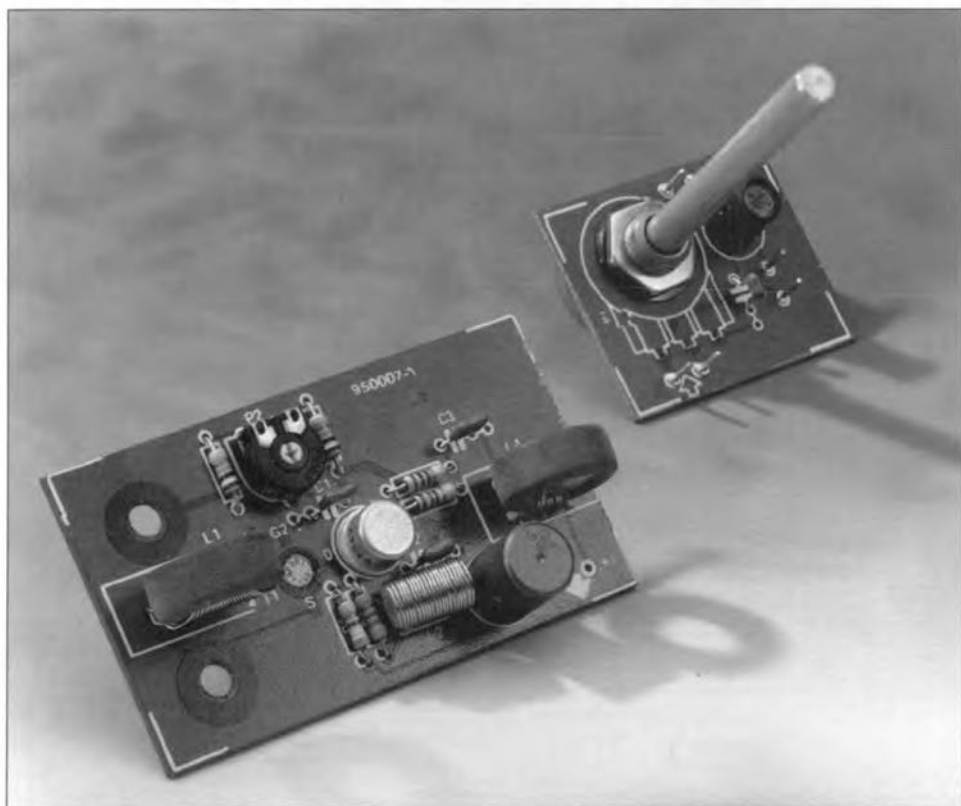


Fig. 3. Although three inductors in the circuit are home made, the circuit is simple to build.

strong. A considerable improvement should be noted over the regular whip antenna. If not, run a thorough check on the complete circuit.

If the antenna appears to work so far, the receiver is tuned between 21 MHz and 21.5 MHz (13-m band). Listen carefully for spurious signals in this band like harmonics, 'birdies', 'whistles' or intermodulation products. If such signals are noted, the receiver is probably overdriven. If the spurious signals do not disappear when the input level is reduced by operating potentiometer P<sub>1</sub>, carefully adjust the preset, P<sub>2</sub>, until a setting is found at which the level of the spurious signals is at a minimum. Next, tune to a weak signal in the 13-m band to check that the new setting does not unduly decrease the signal-to-noise ratio. possibly, a minor adjustment of P<sub>1</sub> brings some improvement.

Finally, the above mentioned time for the adjustment is only valid for the winter months, and in the spring up to the end of April. In the summer months, the adjustment is best done around midnight.

(950007)

# FOCUS ON: CD ROM STANDARDS AND APPLICATIONS

Since the introduction of the audio compact disc (CD) in 1982, this digital information carrier has been the nucleus of many developments. Today, the CD is not only used for music, but also for computer data and video. This article discusses the various CD standards that have evolved over the years. These are world standards which have been defined in the Red Book, Yellow Book, Green Book, Orange Book and White Book.

By our editorial staff

THE Compact Disc was born in Eindhoven, The Netherlands, at the Philips Research Laboratories. There, the concept of optical registration of digital data was developed. In 1980, when Philips N.V. and Sony agreed to promote the CD as a carrier of digital audio, it was difficult to foresee the overwhelming effect the silver disc would have on the music industry. In five years' time, some 30 million CD players were operational, and 450 million CDs sold. The gramophone, Edison's invention, and the most important sound medium for 80-odd years, was dead and buried at 'record' speed.

Since then, there's no stopping the CD. The shining silver disc is used for an increasing number of applications. The White Book, for instance, published in 1994 by Philips and JVC, gives details of the video CD, a CD variant which looks poised to open the attack on the pre-

recorded video tape. In the course of this year, both the computer industry and manufacturers of consumer electronics will introduce various systems which support digital video based on the video CD. This puts the video CD in a position to become accepted just as rapidly as the CD-DA (audio CD).

Today there are so many CD standards that it is difficult to see the wood for the trees. These standards are, therefore, briefly discussed below.

## Red Book, CD-DA

The standard for digital audio, **CD-DA**, may be found in the Red Book, which contains all technical specifications concerning registration and error correction pertaining to the CD. The Red Book has become the basis for later CD standards and developments, which were once beyond the specs laid down in the Red Book

because of high technical demands on the CD.

The information on a CD consists of a spiral-shaped string of holes pressed into a transparent polycarbonate layer. Next, a reflecting aluminium layer is applied which is covered with a transparent protection layer. The space between two holes is called an island. A laser beam scans the spiral from centre of the disc. Because the recording device in the laser drive unit is capable of detecting whether the light is reflected by a hole or an island, it is possible to recover the information pressed on the CD. Variations in the intensity of the reflected light are used to focus the laser via a complex servo system.

The spiral on the CD is divided into three sections: the lead-in, the program (data) and the lead-out. To make the best possible use of the space on the CD, the spiral is scanned at a constant speed. The CD's rotation speed is therefore dependent on the position of the laser. In the program section, the rotation speed can vary between 197 and 539 revolutions per minute. Because a mechanical speed control alone does not enable a constant data flow, the player has a buffer memory which has to be half filled all the time. If less than 50% of the available space is used, the drive speed is increased. If more than 50% is used, the speed is lowered accordingly. The data read by the laser is clocked out of the buffer with the aid of a quartz-controlled oscillator. The buffer/clock system guarantees a perfectly stable datastream into the DAC which follows the CD drive unit.

All data on an audio CD represents sound signals which have been sampled at a frequency of 44.1 KHz. Each sound channel is linearly digitized at a resolution of 16 bits. The result is a datastream with a speed of 1.4112 Mbit per second.

## Yellow Book, CD-ROM

The next standard to appear on the market was defined in the Yellow Book, again produced jointly by Philips and Sony. Once the enormous storage capacity of CDs was fully recognized, the idea of a **CD-ROM** was born. The CD-ROM is marketed as the replacement for magnetic media such as floppy disks and hard disks. It has a number of advantages and disadvantages. The advantages include low cost, large storage capacity, non-volatile character, and reliability. On the down side, a CD-ROM is a read-only medium.

To maintain compatibility with the



CD-DA, the CD-ROM also contains one long spiral. This is in stark contrast with the long-established system of parallel tracks on magnetic media. Because the CD-ROM is also read at constant speed, it has a fairly large random read access time. Any time a file has to be read, the motor speed has to be adjusted until the right reading speed is achieved, and that takes time. Furthermore, the data transfer speed offered by the CD-ROM is relatively low at about 150 KByte per second. Fortunately, double, triple and quadruple speed CD-ROM drives have arrived, and we may see further improvements in the near future.

The information in the Yellow Book does not go much further than a description of the idea to store computer information in the program section. Further, it indicates the types of error correction methods which can be added to the system. The Yellow Book contains neither descriptions of the structure of files and directories as used with computers, nor information on how audio-visual (multi-media) information is to be stored. Consequently, the ISO-9660 and CD-ROM-XA standards were introduced later.

The ISO-9660 standard was initially developed by the High Sierra Group, and taken over by the ISO in 1988. It describes the file structure used with IBM-compatible PCs, and has become the basis for later standards. The UNIX platform uses the RRIP (Rock Ridge Interchange Protocol), while Apple Macintosh users have the HFS (Hierarchical File System) for their CD-ROMs.

## Green Book, CD-i

In 1986, less than a year after the introduction of the CD-ROM, the **CD Interactive** (CD-i) was announced as a multi-media system for the consumer market. The complete system description may be found in the Green Book. Multi-media systems which process audio-visual information are an interesting application area of the CD-ROM. As already mentioned in the description of the CD-DA, audio information is recorded at a speed of 1.4112 MBit/s. Because video information is far more complex than audio information, the amount of data required for digital video will be even greater. Both with audio and video, there is an interaction between the necessary datastream and the quality of the encoded signal. The CD-i specification describes lots of possibilities for the recording of multi-media information such as sound, still-video, animations and video. Moreover, the information is stored in an interleaved pattern, which means that, for instance, audio and video are interwoven in blocks. That allows the CD-i player to read several types of information simultaneously.

The essential difference between CD-i



Fig. 1. The CD-DA (audio CD) was the first CD for a big audience. This Philips CD player was a market hit during the early nineteen-eighties.

and CD-ROM is that the specifications of the former include a complete description of the hardware which is necessary to be able to use the CD-i software. The Green Book also provides information on the structure of the data pressed on a CD-i disc. A marked difference with the Yellow Book, which has nothing on data storage formats.

Chapter 9 of the Green Book describes how MPEG1 full-screen video encoded according to ISO 11172 may be added to CD-i information. This system is called

'digital video on CD-i' and has been added to the CD-i system as an option.

## CD-ROM XA

**CD-ROM XA** (eXtended Architecture) denotes an extension of the CD-ROM standard drawn up to make the medium better suited to multi-media applications. Broadly speaking, the XA standard enables a number of CD-i compatible audio and video formats to be used with CD-ROM also. Furthermore, it intro-



Fig. 2. The CD-ROM drive is on the way to becoming just another standard peripheral in computer land.

duces the possibility of different start directories, which enables you to run a CD under different operating systems. Finally, the CD-ROM-XA standard, like the CD-i, is structurally compatible with the ISO-9660 standard. That makes the CD-ROM-XA suitable for many different computer systems. This type of disc is, however, unsuitable for CD-i players because they often lack the appropriate programs. Despite the fact that the XA standard has been with us for some time, little software has become available so far which utilizes this standard.

## Sector structure

According to the definitions in the Yellow Book, sectors on a CD have a length of 2,352 bytes, and are subdivided into a number of fields to make them accessible to computers. The start of a sector is indicated by a synchronization pattern of 12 bytes. This is followed by a 4-byte header which contains its absolute address in minutes, seconds and sectors, as well as a mode byte. That leaves 2,336 bytes available for data storage in each sector.

All sectors in one track use the same mode. Sectors exist in three different modes. In Mode-0 sectors, all remaining 2,336 bytes are empty, i.e., zero. Mode-1 sectors contain 2,048 bytes of user data, protected by an EDC (error-detecting code) and an ECC (error-correcting code). This error protection is additional to the protection already used for CDs. Although the standard error correction for CDs is application independent, it is not powerful enough for computer applications. This is because small data errors are unacceptable in computer systems, although they may go by unnoticed in audio systems.

In Mode-2, which is the format used for normal CD-ROMs that do not require extra error correction (for instance, digitized audio/video), the remaining 2,336 bytes are available to hold data. The structure of Mode-2 sectors is further detailed in the Green Book to ensure compatibility with the ISO-9660 standard. The extension with Mode-2 is used with CD-i and CD-ROM-XA. It involves the storage of data in sectors by assigning a sub-header to each sector. This sub-header contains a file and channel number coding information for details on the type of data contained in the sector, as well as a sub-mode byte. The file number is used to distinguish between sectors of different, interleaved, files. The channel number is used to support the different channels a file may be composed of. The sub-mode byte contains the end-of-file (EOF) and end-of-record (EOR) bits, an interrupt trigger bit to enable synchronization, and a real-time bit which indicates that the file is used in real time mode.

Finally, three bits follow which indi-

Table 1.

Standard	standard book	system holder	introduction
CD-DA	Red Book	Philips, Sony	1982
CD-ROM	Yellow Book	Philips, Sony	1985
CD-i	Green Book	Philips, Sony	1987
CD-ROM XA		Philips, Sony	1989
CD-ROM MO/CD-WO	Orange Book	Philips, Sony	1990
CD-Bridge		Philips, Sony	1991
Photo CD		Kodak, Philips	1992
Video CD	White Book	JVC, Philips	1994



Fig. 3. A CD-i player is compatible with many different CD formats.

cate the type of data (video, audio, computer, etc.) in the sector. This extension has two options: mode-2/form-1 and mode-2/form-2, where the form bit indicates whether or not the additional error correction used in Mode-1 sectors is employed. Mode-2/form-1 sectors do have this extra error correction (EDC and ECC), while mode-2/form-2 sectors have an EDC block only. The absence of extra error correction is justified if the CD contains audio or video information. With these file types, the absence of the real-time bits (even occasionally) is much more important than small data errors. Because the extra error correction is not used, 280 bytes are available for data storage. With a real-time file stored in a mode-2/form-1 sector, the error detection and correction operations have to be performed in real time also, which makes high demands on the relevant hardware.

The eight space bytes in a Mode-1 sector are usually zero, and used for the header in Mode-2. Consequently, the lo-

cations for the data and the EDC fields are moved by eight bytes. A mode-2/form-2 sector is closed off by a 4-byte EDC field only, which may contain parity bits which serve as quality indicators in the CD production process. These bytes may also be made zero. If they are used, it is recommended to employ the same EDC as with mode-2/form-1 sectors.

## Orange Book, CD-MO and CD-WO

The Compact Disc Magneto-Optical (CD-MO) and Compact Disc Write Once (CD-WO) are specified in the Orange Book. This extension has given the CD an even wider application area, because it specifies how CDs may be produced in small quantities.

The CD-MO enables the information on a CD to be re-written several times. By contrast, the CD-WO system allows data to be written once only. The CD-MO has a magneto-optical layer in which the

information is stored in a completely different manner than with a normal CD. The read section of the laser recognizes a CD-MO disc from a change in the polarization direction of the laser light. A special drive unit is required for the reading and writing of this type of CD.

A CD-WO, *a.k.a.* CD Recordable (CD-R) has three status levels: it is either blank, partly written on, or completely written on. Like the CD-MO, the CD-WO contains a special pre-recorded track with information required for tracking and timing. The CD-WO contains a light absorbing layer of which the reflection characteristics are modified with a special laser during recording. A CD-WO enables CD's to be 'burnt' which are compatible with the Red, Yellow and Green Book. These discs can be played on any conventional CD player or CD-ROM drive.

The CD-WO standard also supports the use of multiple partitions on a single CD ('multi-session'). Each of these partitions has its own lead-in, program and lead-out sections, and is compatible with the standards in the Red, Green or Yellow Book. Such a multi-session CD can only be read by a special multi-session drive. An ordinary CD-ROM drive can only read the data in the first session.

### CD-Bridge

The **CD-Bridge** standard was developed to bridge the CD-i and CD-ROM standards. It is a very open standard with plenty of room for the implementation of the various system specifications. A CD-Bridge disc is a CD-ROM-XA disc which also contains a CD-i program. Consequently, this type of disc may be used in a computer as well as in a CD-ROM-XA drive. The popular photo-CD and Video-CD are examples of CD-Bridge discs.

### Photo-CD

The **Photo-CD** is a CD-Bridge disc of which the standard was designed by Philips and Kodak. This type of CD is intended for the storage of photographs which have been digitized at a very high resolution, and so allows you to view photographs on your TV or computer screen. The relevant file may be processed further on the PC, or printed on paper.

A Photo-CD may be an ordinary CD, produced with conventional means, or a CD-WO. The latter format allows photos to be added to the CD during further sessions. Obviously, pre-recorded Photo-CDs have one session only, and can be read by all types of CD-ROM.

The standard version of the Photo-CD is based on 35-mm photographic negatives which are digitized at a resolution of 3782 x 2048 pixels. The file recorded on the CD consists of five sub-files: Base/16, Base/4, Base, 4xBase and

**Table 2.**

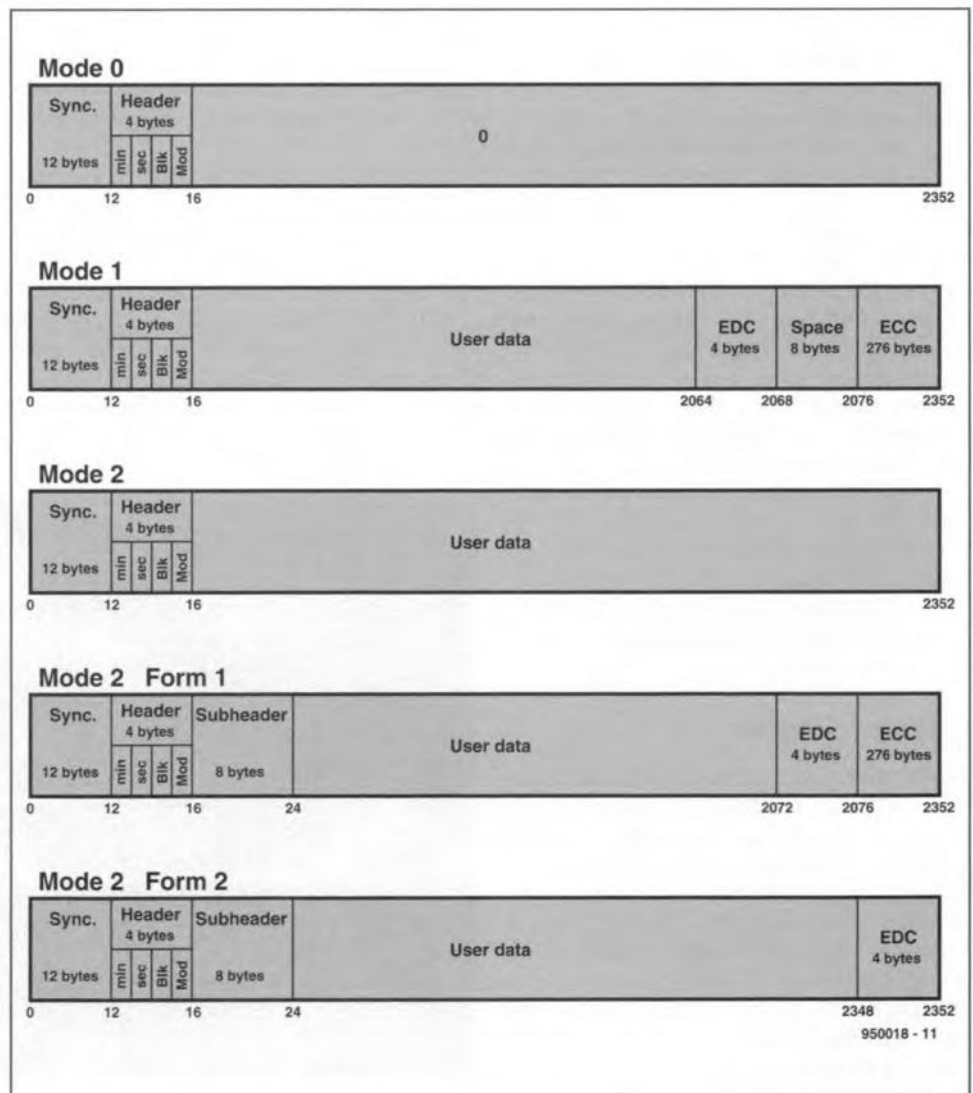
Compatibility between disk format and player.

Disk	player/system					
	CD-DA	CD-ROM	CD-ROM-XA	CD-i	Photo CD	Video CD
CD-DA	x	x	x	x	x	x
CD-ROM	-	x	x	-	-	-
CD-ROM XA	-	-	x	-	-	-
CD-i	-	-	-	x	-	-
CD-Bridge	-	-	x	x	-	-
Photo CD	-	-	x	x	x	-
Video CD	-	-	x	x	-	x

x = compatible  
- = not compatible

16xBase. Thanks to data compression techniques, an ordinary CD can hold more than 100 digitized 35-mm photographs. These days it is also possible to

put larger film formats onto a Photo-CD. This is particularly interesting for professional users of photographic material.



**Fig. 4.** The data structure on a CD-ROM is strongly dependent on the application. This drawing shows the sector structure of the CD-ROM, CD-ROM-XA and Cd-i formats.

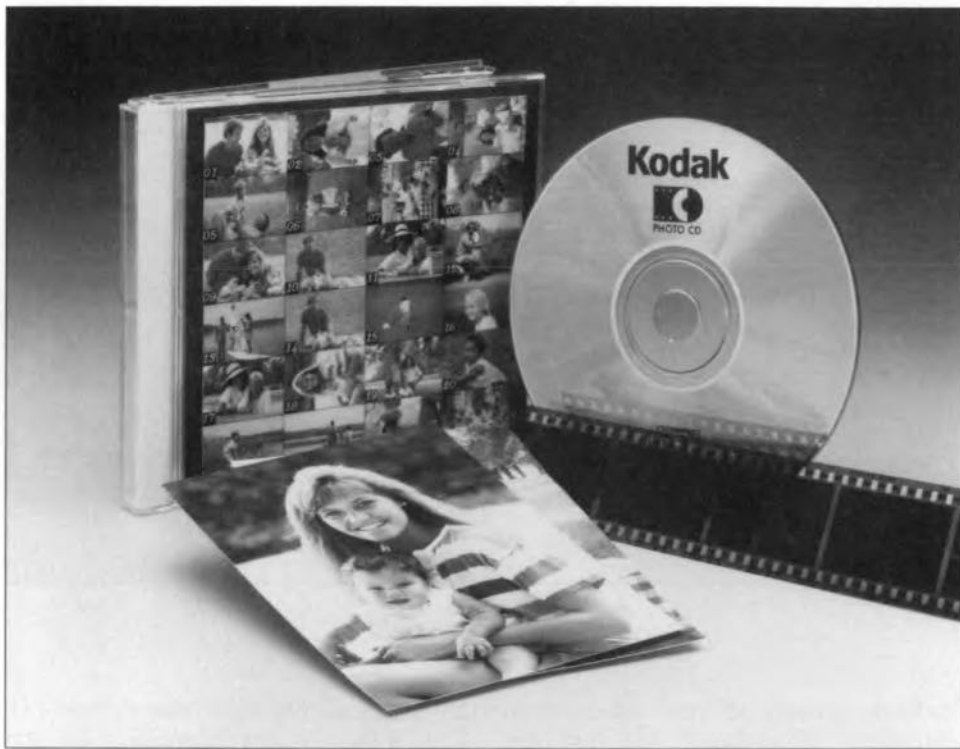


Fig. 5. The Photo-CD format was designed Kodak and Philips. It allows over 100 35-mm negatives to be stored on a single CD without loss of quality.

## White Book, Video-CD

The last CD-Bridge variant discussed in this article is the **Video-CD**. This was developed for the storage of full-motion, full-screen, video, as already described in Chapter 9 of the Green Book (CD-i). The pictures on the CD are encoded to the MPEG-1 standard. A normal 12-cm diameter CD has storage capacity for 74 minutes of digital video. The technical specifications of the Video-CD are described in the White Book. Initially, this version was also known as the Karaoke-CD standard.

To further the acceptance of this medium, the standard explicitly describes the possibility of adding full-motion video decoder to a conventional audio CD player. As a matter of course, that is only possible if the player is modified accordingly.

## Other formats

**CD-Video**, not to be confused with Video-CD, is a CD format which has been in use for some time to record five to six minutes of analogue video on a CD. This format is described as an extension in the Red Book. In addition to the video information, the CD has spare capacity for about 20 minutes of digital audio. After a few false starts, this format soon went into oblivion. Today, it is hardly produced any more.

The CD Background Music (**CD-BGM**) format was developed for background music ('Muzak') systems, and is based on technologies derived from the

CD-i standard. By virtue of the ADPCM encoding used, a single CD can hold up to 20 hours of background music at reasonable quality.

**CD+MIDI** and **CD+G** were also developed on the basis of the audio CD. These formats enable graphics and MIDI data to be put on a CD, together with digital audio.

The last format to be mentioned is called **CD-i Ready**. With these audio CDs, an amount of CD-i software is stored in the background. When the CD

is played on an audio CD player, this extra functionality is not noticed because the disc behaves just like any other music CD. The CD-i software comes to life once the disc is inserted in a CD-I player. Additional functions which are then available include song texts, photographs, discographies, etc. To make sure that the CD-i information does not interfere with the music reproduction, the CD-i player first reads its own information, and stores it in a buffer. Next, the associated audio track is played.

## Finale

A plethora of CD standards is currently in use, and the overall situation is complex enough to look pretty bewildering at first glance. As a general tip, formulate your requirements before you go out and purchase a CD player or a CD-ROM drive. Use the information in **Table 2** to check for yourself which standards are actually required for your particular applications, and then select a player which supports at least those standards.

(950018)

## Source:

*Compact Disc Standards, an Introductory Overview*, by Jan Korst and Verus Pronk, Philips Research Laboratory, Eindhoven, The Netherlands.

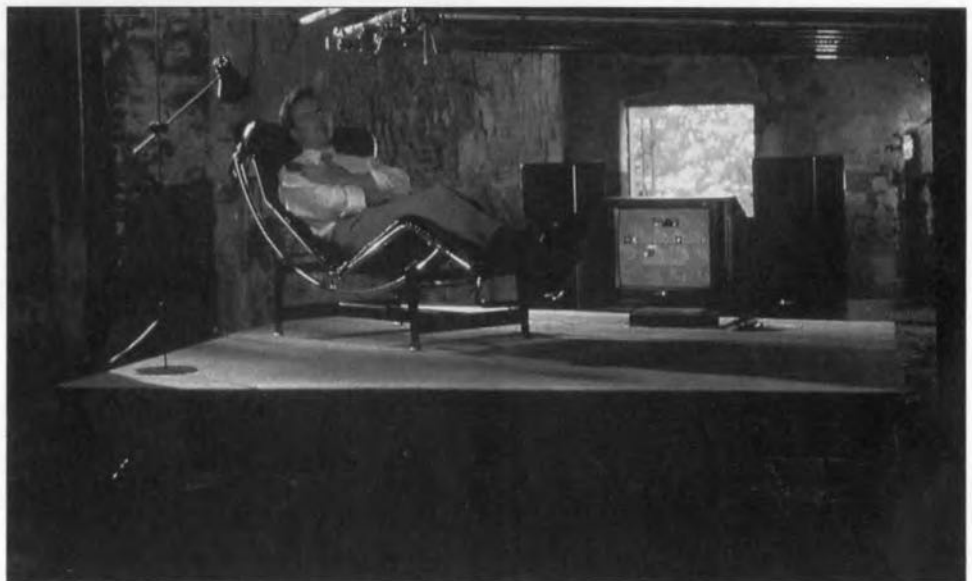


Fig. 6. The Video-CD is expected to take a large market share away from the pre-recorded video tape. Computer users, too, can use this CD format to load and display digitized photos with the aid of an MPEG insertion card.

# DIGITAL SIGNAL PROCESSORS

By L. Lemmens

This article is intended as a brief introduction to digital signal processors (DSPs) and what makes them different from traditional processors and microcontrollers. The description is based on the ADSP-2100 family from Analog Devices, which includes the ADSP-2105 used in the DSP function generator described elsewhere in this issue.

The fundamental theory of DSP is Shannon's Sampling Theorem (1949) which states how often a time-varying signal is to be monitored if it is to be reconstructed exactly from its digital samples. It can be simply stated as follows:

In order to recover the signal function  $f(t)$  exactly, it is necessary to sample  $f(t)$  at a rate greater than twice its highest frequency component.

For instance, an audio signal whose highest frequency is 18 kHz should be sampled at 36 kHz to preserve and recover its waveform exactly.

Sampling a signal at a rate below its highest frequency component results in a phenomenon called *aliasing*. This results in a frequency erroneously taking on the identity of an entirely different frequency when recovered.

## Multi-functionality

In spite of their name, digital signal processors are intended to process analogue signals. However, since they are digital devices, the signal must first be passed through an analogue-to-digital converter. After the signal has been processed, a digital-to-analogue converter (DAC) is needed in many applications. The two conversions are not normally carried out by the DSP but by external devices.

When analogue signals are digitized, their waveform is translated into a digital number at set intervals. The consequent series of numbers is passed through a digital filter (or filters) and their frequency spectrum is then determined by a Discrete Fourier Transform (DFT) or a Fast Fourier Transform (FFT). The power spectrum determination lies at the heart of a range of DSP operations, from speech recognition to the analysis of seismic data.

The mathematics underlying the sampling theory and the Fourier transform are too complex to be discussed in an article of this nature, but can be found in many textbooks. However, in practice, the processes come down to the computation of a series of products. Such a computation consists of (a) fetching two numbers from the mem-

ory; (b) multiplying the numbers; (c) accumulating the result; (d) storing the result in memory.

Apart from the fact that standard processors do not possess a multiplication facility, they would need many cycles to perform one such operation. Digital signal processors can perform several actions in parallel during one cycle and can even do so in real time.

A typical DSP in the ADSP-2100 family operates at 12.5 MHz and executes an instruction in a single 80 ns cycle. Since all instructions are carried out in a single cycle, MIPS (Million Instructions Per Second) = MHz. Its flexible architecture and comprehensive instruction set make possible a number of parallel operations. In one cycle, the ADSP-2100 can

- generate the next program address;
- fetch the next instruction;
- perform one or two data moves;
- update one or two data address pointers;

- perform a computational operation.

## Architecture

Figure 1 is an overall block diagram of the ADSP-2105. The processor contains three independent computational units: the arithmetic logic unit (ALU), the multiplier/accumulator (MAC) and the Shifter. These units process 16-bit data directly and have provisions to support multiprecision computations.

The ALU performs a standard set of arithmetic and logic operations; division primitives are also supported.

The MAC performs single-cycle multiplication, multiplication/addition and multiplication/subtraction operations.

The Shifter performs logical and arithmetic shifts, normalization, denormalization and derive exponent operations. The Shifter can be used to implement efficiently any degree of numeric format control, up to and including full floating point representations.

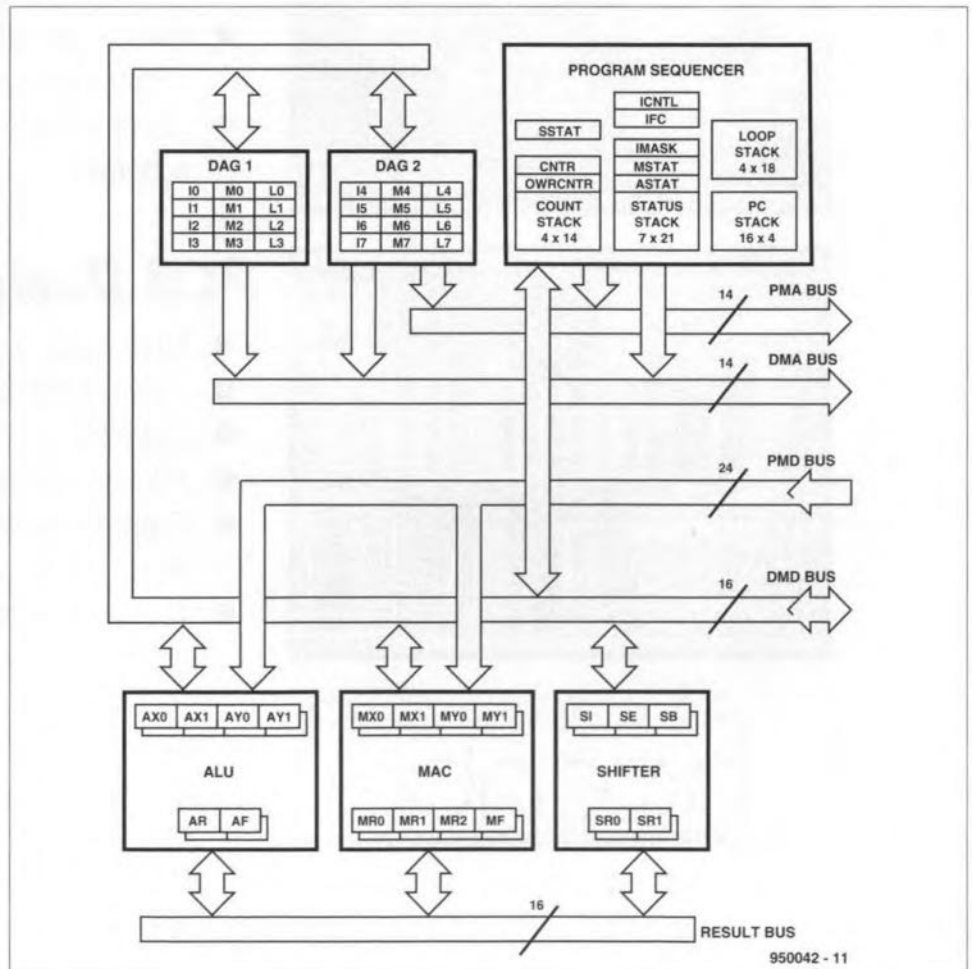
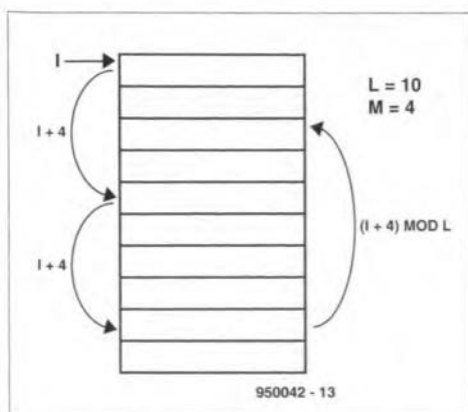


Fig. 1. Block diagram of the ADSP-2105.





**Fig. 2. When a register is scanned and an overflow occurs, the pointer is placed modulo L at the beginning of the register.**

The computational units are arranged side by side instead of serially for flexible operation sequencing. The internal result (R) bus interconnects the units, so that the output of any one of them may be the input of any unit on the next cycle.

A powerful program sequencer and two dedicated data address generators ensure efficient use of these computational units. The program sequencer generates the next instruction address. To minimize overhead cycles, the sequencer supports conditional jumps, subroutine calls and returns in a single cycle. With internal loop counters and loop stacks, the DSP executes looped code with zero overhead; no explicit jump instructions are required to maintain the loop.

The data address generators (DAGs) handle address pointer updates. Each DAG keeps track of up to four address pointers. Whenever the pointer is used to access external data (indirect addressing), it is modified by a prespecified value. A length value may be associated with each pointer to implement automatic modulo addressing for circular buffers. With two independent DAGs, the processor can generate two ad-

resses simultaneously for dual operand fetches.

Efficient data transfer is achieved with the use of five internal buses:

- Program Memory Address (PMA) bus;
- Program Memory Data (PMD) bus;
- Data Memory Address (DMA) bus;
- Data Memory Data (DMD) bus;
- Result (R) bus.

The program memory (PMA, PMD) buses and data memory (DMA, DMD) buses extend off-chip to provide direct connections to external memories.

The DMD bus is the primary bus for routing data internally and to and from external data memory.

The 14-bit DMA bus provides direct addressing of  $16k \times 16$  of external memory. Although the primary function of the program memory is for storing instructions, it can also store data. In this case, the PMD bus provides a path for routing data to and from program memory, permitting dual operand fetches.

The 14-bit PMA bus provides direct addressing of  $16k \times 24$  of external memory, expandable to  $32k \times 24$  by using the program memory data access (PMDA) signal as the 15th address line.

The data address generators provide indirect addressing for data stored in external memories. The processor contains two independent DAGs so that two data operands (one in program memory and one in data memory) can be addressed simultaneously.

The two generators are identical except that DAG1 has a bit reversal option on the output and can only generate data memory addresses, while DAG2 can generate both program and data memory address, but has no bit reversal capability.

There are three register files in each DAG: the modify (MO) register file, the indirect (I) register file, and the length (L) register file. Each of these register files contains four 14-bit register which are readable and loadable from the DMD bus. The

I registers hold the actual addresses used to access external memory.

When the indirect addressing mode is used, the selected I register content is driven on to either the PMA or DMA bus. This value is post-modified by adding the content of the selected M register. The modified address is passed through the modulus logic.

Associated with each I register is an L register which may contain the length of the buffer addressed by the I register. In case of an overflow, the pointer is placed modulo L at the beginning of the register—see Fig. 2. The L register and the modulus logic together enable circular buffer addressing, which is used, for example, in the DSP Function Generator described elsewhere in this issue for Direct Digital Synthesis DDS).

The modulus logic is disabled by setting the length of the associated buffer to zero.

The program sequencer incorporates powerful and flexible mechanisms for program flow control, such as zero-overhead looping, single-cycle branching (both conditional and unconditional) and automatic interrupt processing.

The sequencing logic controls the flow of the program execution. It outputs a program memory address on to the PMA bus from one of four sources: the PC incrementer, PC stack, instruction register or interrupt controller. The next address source selector controls which of these four sources are selected based on the current instruction word and the processor status. A fifth possible source for the next program memory address is provided by DAG2 when a register indirect jump is executed.

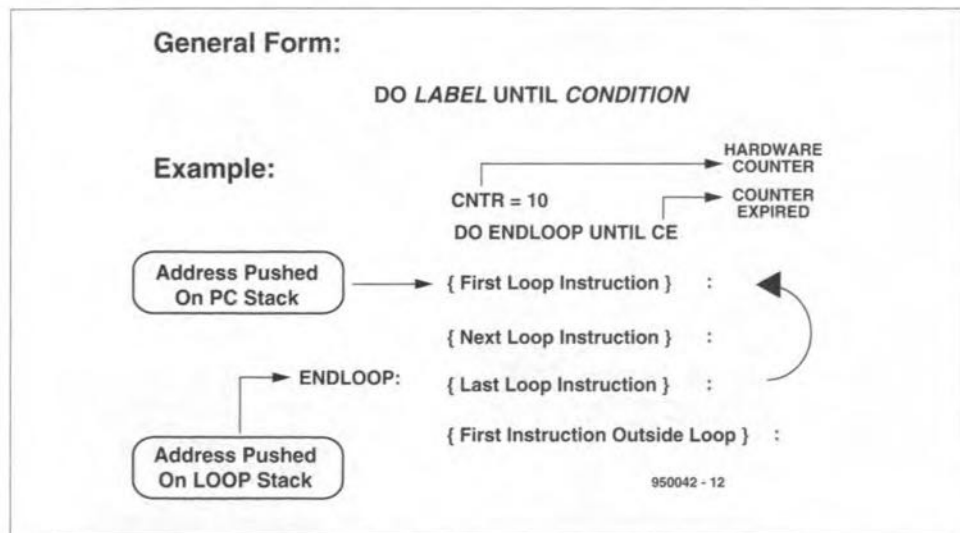
The loop counter is used for DO-UNTIL loops (see Fig. 3); there is thus no variable that needs to be checked by the program, but a register that is automatically decreased and signals when the end condition (CNTR=0) is reached.

When a data fetch from program memory is required, an extra memory cycle is automatically appended to enable the next instruction fetch. To avoid this extra cycle, the device has an internal instruction cache (16 instructions deep) which serves as an alternate source for the next instruction. The cache monitor circuit transparently determines when the cache contents are valid. When the next instruction is in the cache, no extra cycle is necessary.

[950042]

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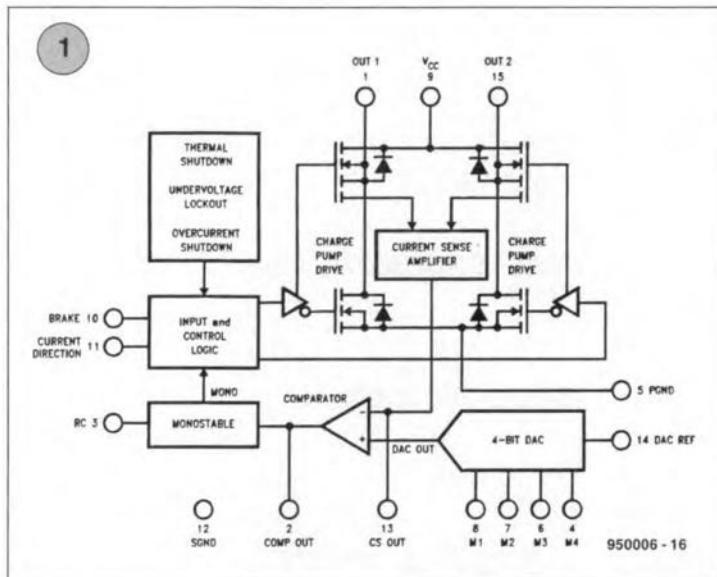
**Fig. 2. Example of a DO-UNTIL loop in a DSP. The processor has a discrete loop counter.**

# APPLICATION NOTE

The content of this article is based on information obtained from manufacturers in the electrical and electronics industries, and does not imply practical experience by *Elektor Electronics* or its consultants.

## LMD18245 3A, 55V DMOS FULL-BRIDGE STEPPER MOTOR DRIVER

Source: National Semiconductor



THE LMD18245 is a full-bridge power amplifier which incorporates all the circuit blocks required to drive and control current in a brushed type d.c. motor, or one phase of a bipolar stepper motor. The multi-technology process used to build the device combines CMOS control and protection circuitry with DMOS power switches on the same monolithic structure. The LMD18245 controls the motor current via a fixed off-time chopper technique.

An all-DMOS H-bridge power stage delivers continuous output currents up to 3 A (6 A peak) at supply voltage up to 55 V. The DMOS power switches feature low  $R_{DS(on)}$  for high efficiency, and a diode intrinsic to the DMOS body structure eliminates the discrete diodes typically required to clamp bipolar power stages. An innovative current sensing method eliminates the power loss associated with a sense

resistor in series with the motor. A four-bit digital-to-analogue converter (DAC) provides a digital path for controlling the motor current, and, by extension, simplifies implementation of full, half and microstep stepper motor drives. For higher resolution applications, an external DAC can be used. The block diagram of the LMD18245 is shown in Fig. 1.

### The current sense amplifier

Many transistor cells in parallel make up the DMOS power switches. The current sense amplifier (Fig. 2) uses a small fraction of the cells of both upper switches to provide a unique, low-loss means for sensing the load current. In practice, each upper switch functions as a  $1\times$  sense device in parallel with a  $4000\times$  power device. The current amplifier forces the voltage at the source of the sense device to equal

that at the source of the power device; thus, the devices share the total drain current in proportion to the 1:4000 cell ratio. Only the current flowing from drain to source, i.e., the forward current, registers at the output of the current sense amplifier. The latter therefore sources 250  $\mu$ A per ampère of total forward current conducted by the upper two switches of the power bridge.

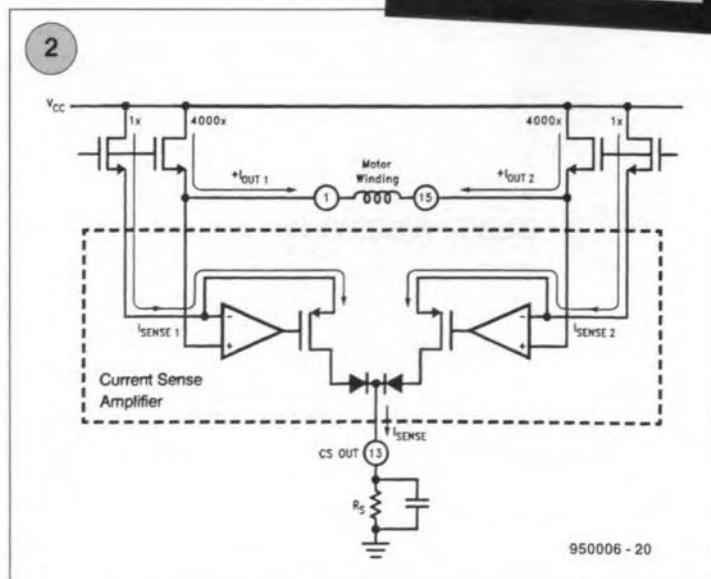
The sense current develops a potential across  $R_s$  that is proportional to the load current; for example, per ampère of load current, the sense current develops 1 V across a 4-k $\Omega$  resistor (the product of 250  $\mu$ A per ampère and 4 k $\Omega$ ). Since chopping the load current occurs as the voltage at CS OUT surpasses the threshold (the DAC output voltage),  $R_s$  sets the gain of the chopper amplifier; for example, a 2-k $\Omega$  resistor sets the gain at 2 A of load current per volt of the threshold (i.e., the reciprocal

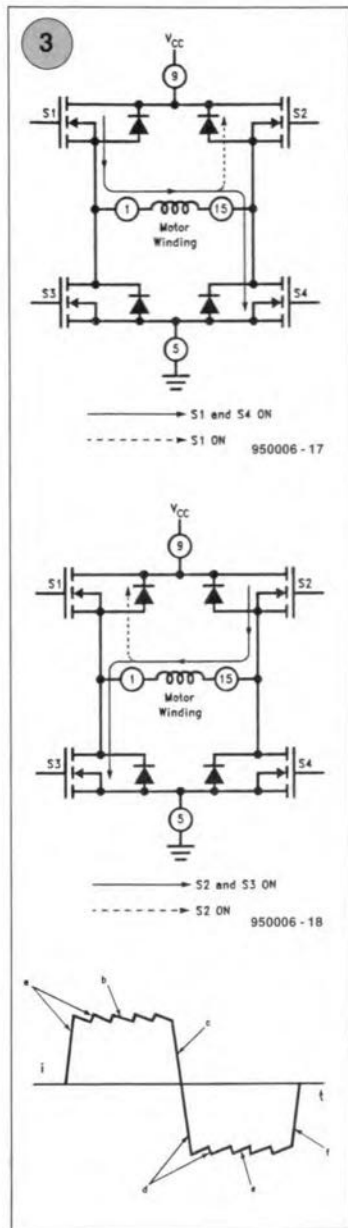
## FEATURES

- » DMOS power stage rated at 55V and 3A continuous
- » Low  $R_{DS(on)}$  of typically 0.3 $\Omega$  per power switch
- » Internal clamp diodes
- » Low-loss current sensing method
- » Digital or analogue control of motor current
- » TTL and CMOS compatible inputs
- » Thermal shutdown (outputs off) at  $T_j=155^\circ\text{C}$
- » Overcurrent protection
- » No shoot-through currents
- » 15-lead TO-220 moulded power package

## APPLICATIONS

- » Full, half and microstep stepper motor drives
- » Stepper motor and brushed d.c. motor servo drives
- » Automated factory, medical and office equipment





of the product of 250  $\mu$ A per A and 2 k $\Omega$ ). The specified operating voltage at the CS OUT pin is 0 to 5 V.

**The digital-to-analogue converter (DAC)**

The DAC sets the threshold for chopping at  $V_{DAC REF} \times D/16$ , where D is the decimal equivalent (0-15) of the binary number applied at the DAC inputs, M4 through M1. M4 is the most-significant bit (MSB). For applications that require higher resolution, an external DAC may be used to drive the DAC REF input. The specified operating voltage range at DAC REF is 0 to 5 V.

**Comparator, monostable and winding current threshold for chopping**

As the voltage at CS OUT surpasses that at the output

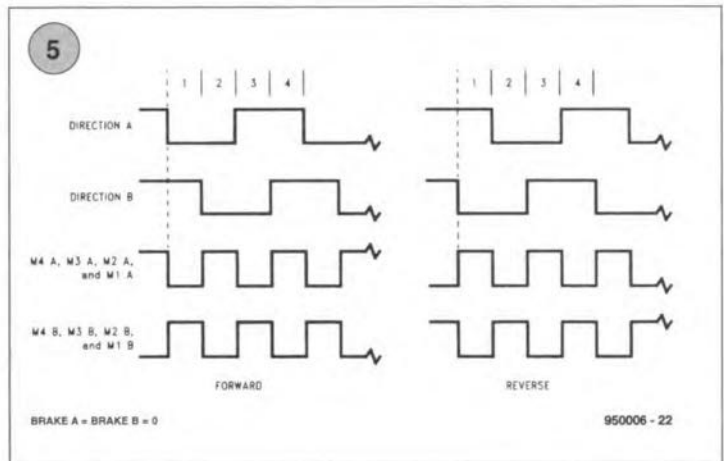
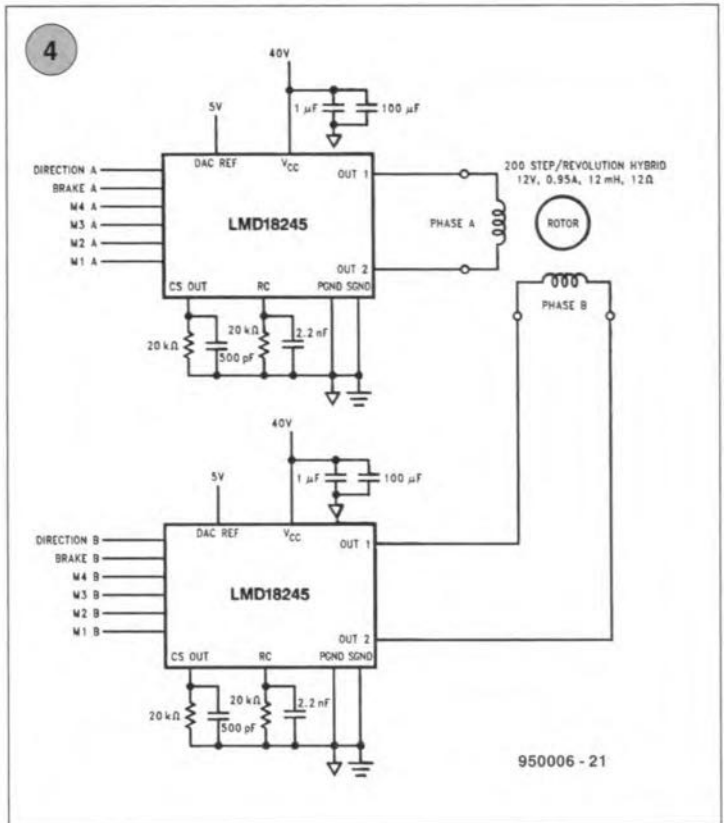
of the DAC, the comparator triggers the monostable. This, once triggered, provides a timing pulse to the control logic. During the timing pulse, the power bridge shorts the motor winding, causing current in the winding to recirculate and decay slowly towards zero. A parallel RC network connected between RC (pin 3) and ground sets the timing pulse, or off-time, to about 1.1RC seconds.

Chopping of the winding current occurs as the voltage at CS OUT exceeds that at the output of the DAC; so chopping occurs at a winding current threshold of about

$$(V_{DAC REF} \times D/16) \div [(250 \times 10^{-6}) \times R_s] \text{ ampères.}$$

Apart from processing the MMV signal, the control logic also interprets the levels applied to the DIRECTION and BRAKE inputs of the IC. The H-bridge is capable of assuming different configurations, as illustrated in Fig. 3. Turning ON a source switch and a sink switch in opposite halves of the bridge forces the full supply voltage less the switch drops across the winding (a). While the bridge remains in this state, the winding current increases exponentially towards a limit dictated by the supply voltage, the switch drops, and the winding resistance. Subsequently turning OFF the sink switch causes a voltage transient that forward biases the body diode of the other source switch. The diode clamps the transient at one diode drop above the supply voltage, and provides an alternative current path. While the bridge remains in this state, it essentially shorts the winding, and the winding current recirculates and decays exponentially towards zero (b). This process is repeated until the DIRECTION signal changes. Both the switches and the body diodes then provide a decay path for the initial winding current, which rapidly drops to zero (c). Next, the control logic re-configures the H-bridge, so that the current

flows through S2, the motor winding and S3. The motor current waveshape is then described by (d), (e) and (f) in the lower drawing.



flows through S2, the motor winding and S3. The motor current waveshape is then described by (d), (e) and (f) in the lower drawing.

**Modes of operation**

A typical application of two LMD18245s driving a stepper motor is shown in Fig. 4. The chopper off-time is set to about 48  $\mu$ s by the 20-k $\Omega$  resistor and 2.2-nF capacitor connected between RC and ground. The chopper gain is set to about 200 mA per volt of the threshold by the 20-k $\Omega$  resistor at the CS OUT pin. Digital signals supplied by a microcontroller govern the thresholds for chopping, the directions of the winding

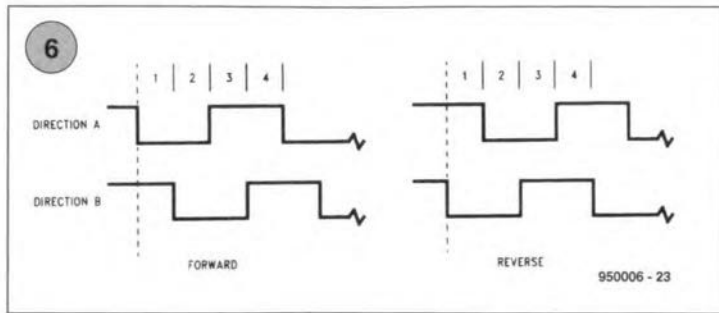
currents, and, by extension, the drive type (full step, half step, etc.).

**Full step drive**

There are two types of full step drive. In one-phase drive (Fig. 5), the motor can be made to take full steps by energizing windings A and B in the sequence

$$A \rightarrow B \rightarrow A' \rightarrow B' \rightarrow A \rightarrow \dots$$

where A and B represent the currents in one direction through the respective windings, and A' and B', the reverse currents. The motor takes one full step each time one winding is de-energized and the other is energized. To make the motor reverse,



the above sequence must be reversed. That is achieved by swapping the levels of the DIRECTION signals.

Two-phase drive (Fig. 6) also results in full steps, and is described by the sequence

$AB \rightarrow A'B \rightarrow A'B' \rightarrow AB' \rightarrow AB \rightarrow \dots$

Because both windings are energized at all times, this sequence produces more torque than with one-phase drive. All DAC inputs are held permanently high.

**Half-step drive without torque compensation**

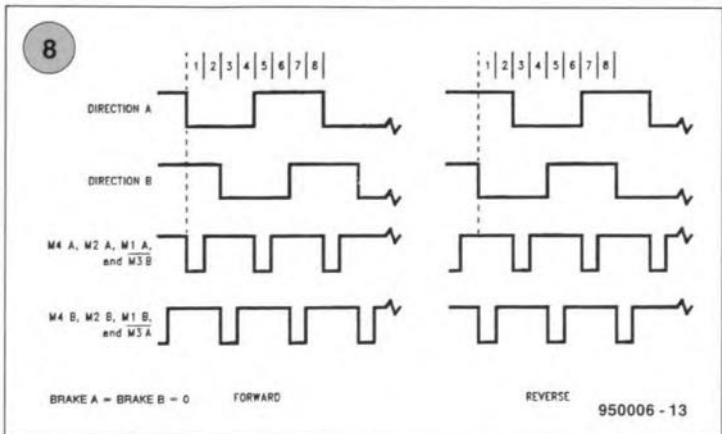
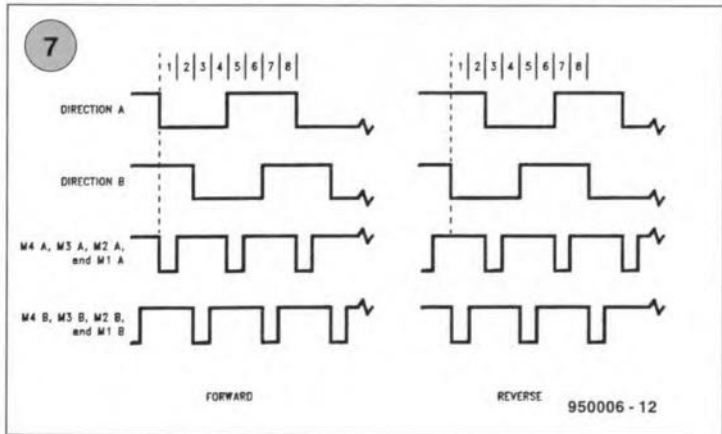
To make the motor take half steps (Fig. 7), windings A and B can be energized in the sequence

$A \rightarrow AB \rightarrow B \rightarrow A'B \rightarrow A' \rightarrow A'B' \rightarrow B' \rightarrow AB' \rightarrow A \rightarrow \dots$

It is important to note that although half stepping doubles the step resolution, changing the number of energized windings from two to one decreases torque by about 40%, resulting in significant torque ripple and possibly noisy operation.

**Half-step drive with torque compensation**

The above problem can be solved by torque compensation (Fig. 8). Essentially, the windings are then energized with sinusoidal currents. Controlling the winding currents in this fashion doubles the step resolution without the significant torque ripple



	$\alpha$	$\cos \alpha$	DAC A	DIR A	$\sin \alpha$	DAC B	DIR B
Reverse $\Rightarrow$	0	1	15	1	0	0	1
	45	0.707	11	1	0.707	11	1
	90	0	0	0	1	15	1
	135	0.707	11	0	0.707	11	1
	180	1	15	0	0	0	0
	225	0.707	11	0	0.707	11	0
	270	0	0	1	1	15	0
Forward $\Leftarrow$	315	0.707	11	1	0.707	11	0
	REPEAT						

Table 1. Lookup table for half-step drive with torque compensation. Note:  $90^\circ$  electrical/full step  $\div$  2 microsteps/full step =  $45^\circ$  electrical/step.

	$\alpha$	$\cos \alpha$	DAC A	DIR A	$\sin \alpha$	DAC B	DIR B
Reverse $\Rightarrow$	0	1	15	1	0	0	1
	22.5	0.924	14	1	0.383	6	1
	45	0.707	11	1	0.707	11	1
	67.5	0.383	6	1	0.924	14	1
	90	0	0	0	1	15	1
	112.5	0.383	6	0	0.924	14	1
	135	0.707	11	0	0.707	11	1
	157.5	0.924	14	0	0.383	6	1
	180	0	15	0	0	0	0
	202.5	0.924	14	0	0.383	6	0
	225	0.707	11	0	0.707	11	0
	247.5	0.383	6	0	0.924	14	0
	270	0	0	1	1	15	0
	292.5	0.383	6	1	0.924	14	0
	315	0.707	11	1	0.707	11	0
	337.5	0.924	14	1	0.383	6	0
Forward $\Leftarrow$	REPEAT						

Table 2. Winding currents and Lookup Table for quarter-step drive with torque compensation. Note:  $90^\circ$  electrical/full step  $\div$  4 microsteps/full step =  $22.5^\circ$  electrical/microstep.

of the prior drive technique. Along with the obvious advantage of increased step resolution, this microstepping reduces both full-step oscillations and resonances that occur as the motor and load combination is driven at its natural resonant frequency, or subharmonics thereof. When compared to full step drive, microstepping makes the motor run smoother and quieter. Table 1 shows the phase angle,  $\alpha$ , and the associated cosine values for winding A, and sine values for winding B, for each of the eight different half steps (each full  $360^\circ$  cycle comprises of four full steps).

**Quarter step drive with torque compensation**

The quarter step drive mode only differs from the half-step mode in respect of the resolution. A  $360^\circ$  cycle is divided into 16 steps. Four microsteps then equal one full step. The relevant control data is shown in Table 2. (950006)

**Source:** LMD18245 data sheet, National Semiconductor.

## LMD18245 Electrical Characteristics

The following specifications apply for  $V_{CC} = +42V$ , unless otherwise stated. **Bold-face limits apply over the temperature range  $-40\text{ }^{\circ}\text{C} \leq T_J \leq +125\text{ }^{\circ}\text{C}$ .** All other limits apply for  $T_A = T_J = 25\text{ }^{\circ}\text{C}$ .

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$I_{CC}$	Quiescent current	DAC REF = 0V, $V_{CC} = +20V$		8	15	mA
<b>POWER OUTPUT STAGE</b>						
$R_{DS(on)}$	Switch ON resistance	$I_{LOAD} = 3A$		0.3	0.4	$\Omega$
					<b>0.6</b>	$\Omega$
		$I_{LOAD} = 6A$		0.3	0.4	$\Omega$
					<b>0.6</b>	$\Omega$
$V_{DIODE}$	Body Diode Forward Voltage	$I_{DIODE} = 3A$	1.0	1.5	V	
$T_{rr}$	Diode Reverse Recovery Time	$I_{DIODE} = 1A$		80		ns
$Q_{rr}$	Diode Reverse Recovery Charge	$I_{DIODE} = 1A$		40		nC
$t_{D(ON)}$	Output Turn ON Delay Time	Sourcing Outputs	$I_{LOAD} = 3A$	5		$\mu\text{s}$
		Sinking Outputs	$I_{LOAD} = 3A$	900		ns
$t_{D(OFF)}$	Output Turn OFF Delay Time	Sourcing Outputs	$I_{LOAD} = 3A$	600		ns
		Sinking Outputs	$I_{LOAD} = 3A$	400		ns
$t_{ON}$	Output Turn ON Switching Time	Sourcing Outputs	$I_{LOAD} = 3A$	40		$\mu\text{s}$
		Sinking Outputs	$I_{LOAD} = 3A$	1		$\mu\text{s}$
$t_{OFF}$	Output Turn OFF Switching Time	Sourcing Outputs	$I_{LOAD} = 3A$	200		ns
		Sinking Outputs	$I_{LOAD} = 3A$	80		ns
$t_{pw}$	Minimum Input Pulse Width	pins 10 and 11		2		$\mu\text{s}$
$t_{DB}$	Minimum Dead Band			40		ns
<b>CURRENT SENSE AMPLIFIER</b>						
	Current Sense Output	$I_{LOAD} = 1A$	200	250	300	$\mu\text{A}$
	Linearity Error	$I_{LOAD} = 0.5\text{-}3A$	175		325	$\mu\text{A}$
	Current Sense Offset	$I_{LOAD} = 0A$		$\pm 6$		%
				5	20	$\mu\text{A}$
<b>DIGITAL-TO-ANALOG CONVERTER (DAC)</b>						
	Resolution		4			Bits
	Monotonicity		4			Bits
	Total Unadjusted Error			0.125	0.25	LSB
	Propagation Delay					<b>0.5</b> LSB
				50		ns
$I_{REF}$	DAC REF input current	DAC REF = +5V		-0.5	$\pm 10$	$\mu\text{A}$
<b>COMPARATOR AND MONOSTABLE</b>						
	Comparator High Output Level			6.27		V
	Comparator Low Output Level			88		mV
	Comparator Output Current	Source		0.2		mA
		Sink		3.2		mA
$t_{DELAY}$	Monostable Turn OFF Delay			1.2	2.0	$\mu\text{s}$
<b>PROTECTION AND PACKAGE THERMAL RESISTANCES</b>						
	Undervoltage Lockout, $V_{CC}$		5		8	V
$T_{JSD}$	Shutdown Temperature, $T_J$			155		$^{\circ}\text{C}$
$\theta_{JC}$	Package Thermal Resistance	Junction-to-Case		1.5		$^{\circ}\text{C}/\text{W}$
$\theta_{JA}$	Package Thermal Resistance	Junction-to-Ambient		35		$^{\circ}\text{C}/\text{W}$
<b>LOGIC INPUTS</b>						
$V_{IL}$	Low Level Input Voltage			-0.1	0.8	V
$V_{IH}$	High Level Input Voltage			2	12	V
$I_{IN}$	Input Current	$V_{IN} = 0V$ or 12V			$\pm 10$	$\mu\text{A}$

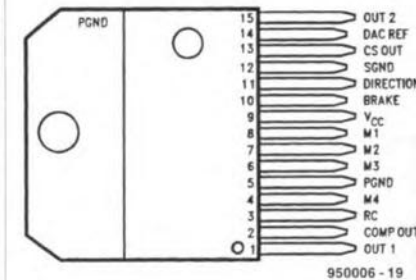
## Absolute Maximum Ratings

d.c. voltage at OUT 1, OUT 2 and VCC	+60 V
d.c. voltage at COMP OUT, RC, Mx, BRAKE, DIRECTION, CS OUT and DAC REF	+12V
d.c. voltage PGND to SGND	$\pm 400\text{mV}$
Continuous Load Current	3A
Peak Load Current	6A
Junction Temperature	+150 $^{\circ}\text{C}$
Power dissipation, $T_A = 25\text{ }^{\circ}\text{C}$ , infinite heatsink	25W
Power dissipation, $T_A = 25\text{ }^{\circ}\text{C}$ , free air	3.5W
ESD susceptibility	1500V
Storage temperature range	-65 to +150 $^{\circ}\text{C}$

## Operating Conditions

Temperature range	-40 to +125 $^{\circ}\text{C}$
Supply Voltage Range	+12 V to +55V
CS OUT Voltage Range	0V to +5V
DAC REF Voltage Range	0V to +5V
MMV pulse width	10 $\mu\text{s}$ to 100 ms

## Pinout Descriptions



**Pin 1, OUT1:** Output node of the first half H-bridge

**Pin 2, COMP OUT:** Output of the comparator. If the voltage at CS OUT exceeds that provided by the DAC, the comparator triggers the monostable.

**Pin 3, RC:** Monostable timing node. A parallel resistor-capacitor network connected between this node and ground sets the monostable timing pulse at about 1.1 RC seconds.

**Pin 5, PGND:** Ground return node of the power bridge. Bond wires (internal) connect PGND to the tab of the TO-220 package.

**Pins 4 and 6 through 8, M4 through M1:** Digital inputs of the DAC. These inputs make up a four-bit binary number with M4 as the most significant bit or MSB. The DAC provides an analogue voltage directly proportional to the binary number applied at M4 through M1.

**Pin 9, Vcc:** Power supply node.

**Pin 10, BRAKE:** Brake logic input. Pulling the BRAKE input logic-high activates both sourcing switches of the power bridge, effectively shorting the load. Shorting the load in this manner forces the load current to recirculate and decay to zero.

**Pin 11, DIRECTION:** Direction logic input. The logic level at this input dictates the direction of the current flow in the load.

**Pin 12, SGND:** Ground return node of all signal level circuits.

**Pin 13, CS OUT:** Output of the current sense amplifier. The current sense amplifier sources 250 $\mu\text{A}$  (typical) per ampere of total forward current conducted by the upper two switches of the power bridge.

**Pin 14, DAC REF:** Voltage reference input of the DAC. The DAC provides an analogue voltage equal to  $V_{DAC\ REF} \times D/16$ , where D is the decimal equivalent (0-15) of the binary number applied to M4 through M1.

**Pin 15, OUT2:** Output node of the second half H-bridge.

# LONG-LIFE NIGHT LIGHT

This article describes an automatically operating night light with two remarkable features. First of all, a light-operated switch turns the lamp on and off automatically depending on ambient light intensity. Secondly, the night light never requires a bulb to be exchanged, simply because there is no bulb inside.

Design by H. Bonekamp

NIGHT lights are often the subject of debates. Either you need one to be able to sleep, or you can not sleep when there is one around in the bedroom. In particular, children often appear to feel much more at ease if a night light is present in their bedroom. The light has a reassuring effect because it appears to function as an orientation aid during periods of light sleep and waking.

Commercially available night lights come in two kinds. The cheap ones have a neon lamp and are on as long as they are plugged into the mains socket. The more expensive types have a small bulb inside, and feature a light-sensitive switch which turns on the light when it gets dark.

Both types have their own advantages and disadvantages. The neon lights are inexpensive and use little power. On the down side, they do

waste energy by remaining on all the time, and often provide insufficient light. The automatic types provide much more light at the cost of a higher current consumption. They also require the (fairly expensive) bulb to be exchanged from time to time. The ideal compromise between the two types would be a version having a light/dark sensor control and an economical lamp with the same life expectancy as a neon light, but a higher light output.

Although these requirements may appear contradictory, the design presented here offers the best of both worlds by exchanging the bulb for a couple of super-luminosity LEDs.

## Profile

Before discussing the design in greater detail, it may be worthwhile to state our *desiderata*. To start with, a reliably operating light/dark switch with adjustable sensitivity is needed to make sure that the on/off switching behaviour is predictable. Furthermore, the circuit should have a reasonable degree of hysteresis to prevent oscillation around the threshold level. Next, the switch should be immune against brief variations of the ambient light intensity. A further wish is to be able to determine the amount of light produced by the night light by fitting one or several 'super-LEDs', without changing the brightness of individual LEDs.

On a different tack, there is, of course, the safety aspect to consider. The night light being used in a children's bedroom, it must be absolutely safe, with complete electrical insulation between the mains voltage and parts which can be touched from the outside. Finally, the night light should be a compact unit which can be plugged straight into a mains socket. No wires, no external controls.

## Four transistors

All requirements mentioned so far are satisfied by a relatively simple circuit. Looking at the circuit diagram in Fig. 1, there are only four transistors, four LEDs and a handful of passive parts.

LEDs D<sub>2</sub> through D<sub>5</sub> at the right-hand side of the diagram supply the light. So-called super-red LEDs with a diameter of 8 mm are used here. These devices come in a diffused-light enclosure with an aperture angle of about 120°, and supply 'soft' light with an intensity of about 500 mCd at 20 mA. Not all of the LEDs shown in the circuit diagram have to be fitted — depending on the desired light intensity, one, two, three or four super LEDs may be fitted without having to change anything in the circuit. This is by virtue of a current source which powers the LEDs. The current source consists of T<sub>4</sub> and surrounding components, of which D<sub>6</sub> and D<sub>7</sub> have a crucial function because they keep the base of T<sub>4</sub> at a constant voltage of about 1.2 V. The voltage across R<sub>8</sub> is, therefore, 0.6 V, which causes a constant emitter current (and collector current) of about 22 mA because R<sub>8</sub> has a value of 27 Ω.

The constant current source is switched on and off by T<sub>3</sub>, which forms the final stage of the light-sensitive switch. This also comprises transistors T<sub>2</sub> and T<sub>1</sub>. The latter is a phototransistor which functions as a sensor for ambient light. The more light it detects, the harder it conducts. Depending on the setting of preset P<sub>1</sub>, a certain amount of ambient light seen by T<sub>1</sub> causes T<sub>2</sub> to be driven. This, in turn, causes the constant current source to be turned on via T<sub>3</sub>, so that the LEDs light at a constant intensity.

Positive feedback via resistor R<sub>4</sub> gives the circuit just the right amount of hysteresis. As long as the current source operates, a part of the positive voltage at the collector of T<sub>3</sub> (approx. 1.2 V) is fed to the base of T<sub>2</sub> via resistor R<sub>4</sub>. Because T<sub>4</sub> is a p-n-p type, the additional voltage pinches the device off a little more, so that the threshold to be overcome by the photocurrent through T<sub>1</sub> is raised a little.

In case T<sub>1</sub> detects an amount of light which causes sufficient conduction, the feedback via R<sub>4</sub> has just the opposite effect. T<sub>2</sub> and T<sub>3</sub> then start to conduct, and the voltage at the collector of T<sub>3</sub> drops considerably. This low level is also fed to the base of T<sub>2</sub> via R<sub>4</sub>,



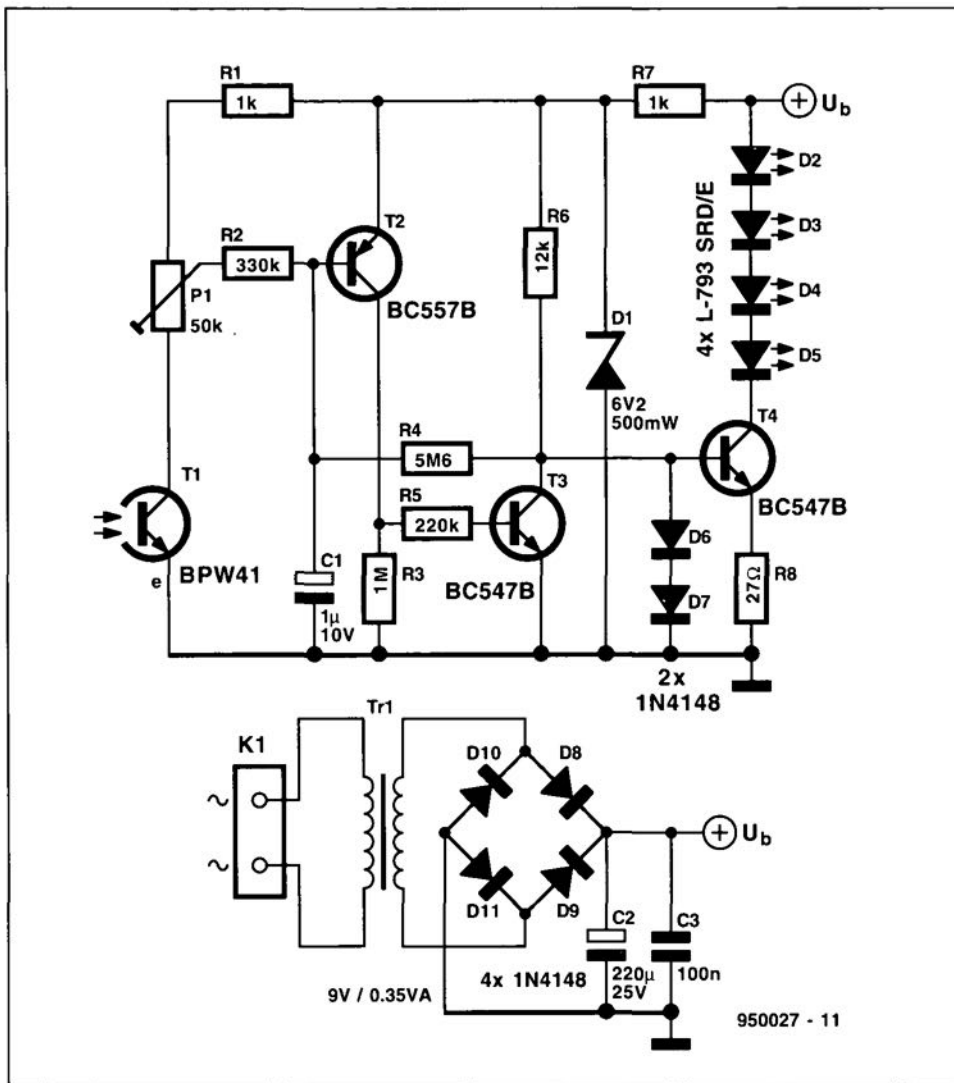


Fig. 1. The circuit may be divided into a light-sensitive switch ( $T_1$ ,  $T_2$  and  $T_3$ ) and a constant-current source ( $T_4$ ) which powers a number of diffused-light super-LEDs.

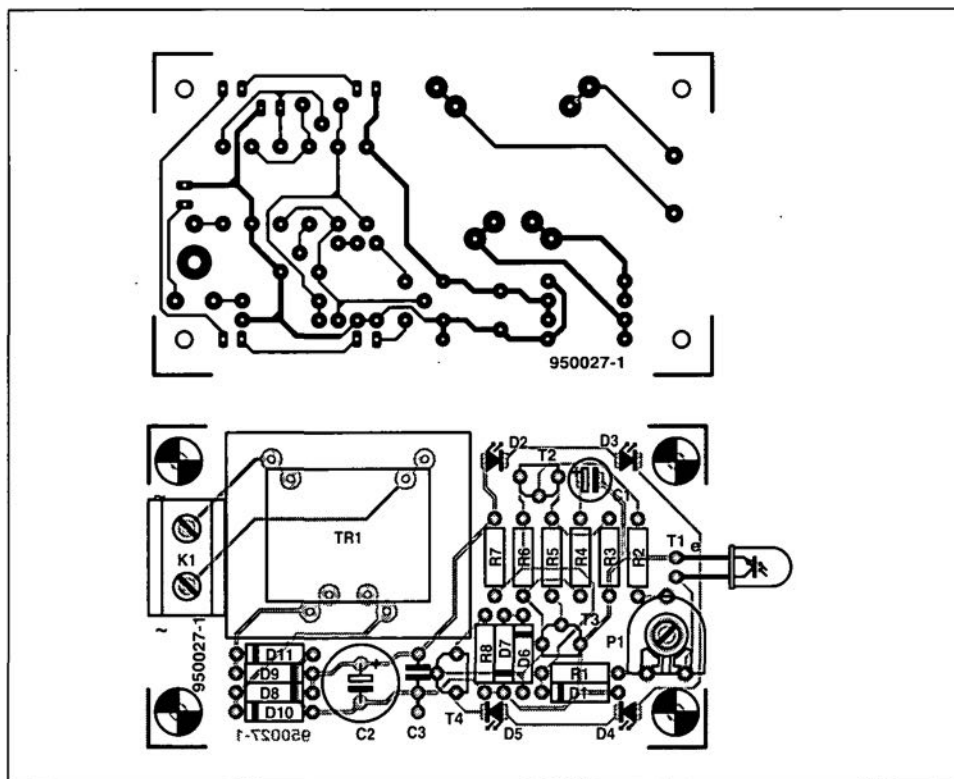


Fig. 2. PCB design (board not available ready-made through the Readers Services).

so that the transistor conducts a little harder. Consequently, a relatively large decrease in photocurrent through  $T_1$  is needed to make the switch toggle again. The voltage feedback via  $R_4$  creates a difference between the 'on' and 'off' levels which is sufficiently large to prevent oscillation around the threshold level.

Capacitor  $C_1$  has been added to prevent the operation of the circuit from being disturbed by brief variations of the ambient light intensity detected by  $T_1$ . Although the capacitor is not too large, it does make the voltage variations at the base of  $T_1$  much slower than those at the wiper of  $P_1$ .

The night light is powered by a classic supply consisting of a transformer, a bridge rectifier and a reservoir electrolytic. Because the circuit draws very little current, the transformer used is a

## COMPONENTS LIST

### Resistors:

- $R_1, R_7 = 1k\Omega$
- $R_2 = 330k\Omega$
- $R_3 = 1M\Omega$
- $R_4 = 5M\Omega$
- $R_5 = 220k\Omega$
- $R_6 = 12k\Omega$
- $R_8 = 27\Omega$
- $P_1 = 50k\Omega$

### Capacitors:

- $C_1 = 1\mu F$  10V radial
- $C_2 = 220\mu F$  25V radial
- $C_3 = 100nF$

### Semiconductors:

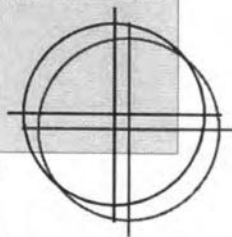
- $D_1 = 6V2$  500 mW zener diode
- $D_2-D_5 = L-793$  SRD/E (Kingbright\*)
- $D_6, D_7-D_{11} = 1N4148$
- $T_1 = BPW41$  (Siemens)
- $T_2 = BC557B$
- $T_3, T_4 = BC547B$

### Miscellaneous:

- $K_1 =$  PCB terminal block, pitch 7.5 mm.
- $Tr_1 =$  PCB mount mains transformer, sec. 9 V/0.35 VA (Hahn, or Monacor type VTR1109, Velleman type 1090018M or Block type VR1109).
- Case, e.g. power supply case with moulded mains plug (approx. size 100x50x40 mm) (Maplin).
- PCB not available ready-made through the Readers Services.

\* Hero Electronics, (01525) 405015.

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pretty small type rated at 9 V, 0.35 VA only. For the same reason, low-current diodes type 1N4148 are used as rectifiers. To keep out the effects of voltage fluctuations, the supply voltage for the electronic switch is separated from the current source, and stabilized at 6.2 V with the aid of a simple zener diode, D<sub>1</sub>.

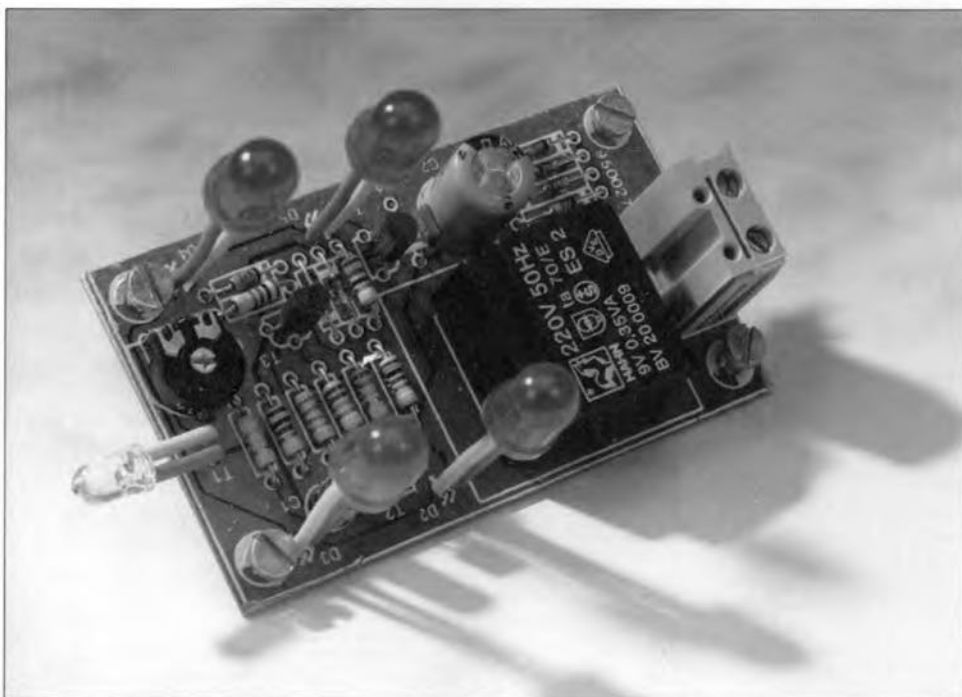
## Construction

The printed circuit board designed for the night light is shown in **Fig. 2**. Unfortunately, this board is not available ready-made through the Readers Services, so you have to make it yourself, or have it made for you. Building

up the board is not expected to cause problems, the parts being few and common. The design of the board allows a number of transformers to be used, while up to four LEDs may be mounted. LEDs not fitted must be replaced by a wire link.

There are two important points about building the circuit into a case. First, T<sub>1</sub> should not be allowed to 'see' the light produced by the LEDs, and, secondly, an electrically safe enclosure should be used. The first point is easy to accomplish by fitting the phototransistor such that it looks upwards, while the LEDs point straight ahead.

Safety need not be a problem if you use a so-called power supply case with a moulded mains plug. To make the night light 'child-proof', consider applying lacquer over the screw heads. Before closing the case, however, the sensitivity preset, P<sub>1</sub>, has to be adjusted. In most cases, it is best to wait until you think it is sufficiently dark, and then adjust P<sub>1</sub> until the light is just switched on. (950027)

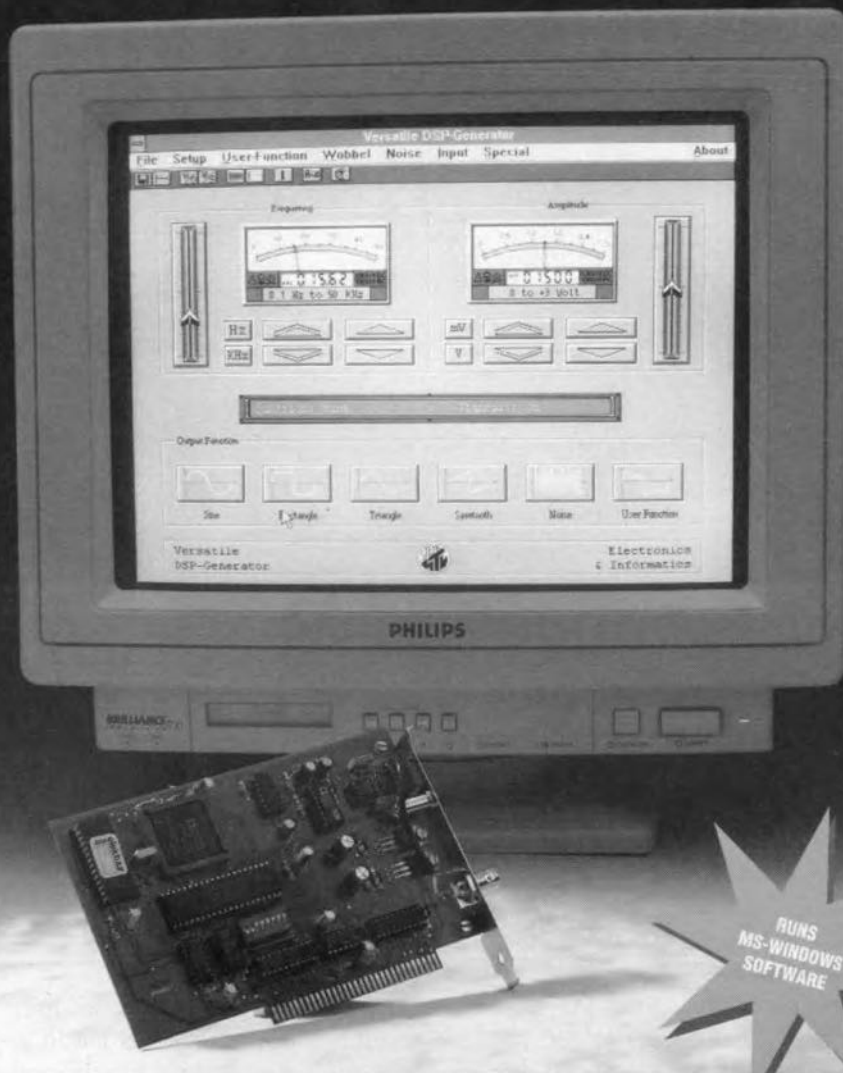




# DSP FUNCTION GENERATOR

## MAIN SPECIFICATIONS

Frequency range:	0.1 Hz to 20 KHz (sinewave, triangle and sawtooth).
Output voltage:	6 V <sub>pp</sub> max.
Waveforms:	sinewave, triangle, rectangular, sawtooth, noise.
Resolution:	16 bits.
Software:	DOS or Windows.
PC bus:	8-bits XT slot.
DSP chip:	ADSP-2105.
Output socket:	BNC or 3.5mm stereo jack.
Output impedance:	47 Ω.



No electronics workshop or laboratory is complete without a function generator. The one described in this article is off the beaten track because it is not a stand-alone box with the usual set of controls on the front panel. Rather, it is an insertion card for PCs, and entirely controlled by software. The heart of the generator is a digital signal processor (DSP) chip from Analog Devices. The card is controlled by a 'plain DOS' or a Windows program supplied to you on disk. The Windows version even allows you to create your own waveshapes!

**Hardware/software design by P. Hackl, M. Haidinger, R. Leeb and F. Reithuber**

DIGITAL signal processors (DSPs) are typically found where digital and analogue electronics meet. A DSP is a special kind of microprocessor which, although a purely digital device, is capable of performing real-time operations on analogue signals 'in

transit'. For example, a DSP uses microprocessor instructions to multiply, amplify, attenuate or filter analogue signals. Likewise, a DSP is capable of adding reverberation to a music signal by delaying the data flow of the digitized audio signal with the aid of a

memory bank, and then adding it again to the main flow. Sure, that can be done with all-analogue electronics, too, for instance, with a bucket brigade memory, but then there is the inevitable noise, distortion, etc., to contend with and keep to a minimum.

The advantage of digital processing is that the quality of the digitized analogue signal is not affected during any operation. By contrast, in analogue circuits, the non-ideal characteristics of subcircuits give rise to distortion, and a decrease in the signal-to-noise ratio.

A DSP, of course, also has its limitations. The maximum frequency of the analogue signal, for instance, is limited by the processor's clock frequency. In practice, therefore, DSPs are best suited to processing low-frequency signals, leaving traditional, discrete, solutions firmly established for high-frequency techniques.

## Circuit description

The complete circuit diagram of the digital function generator is shown in **Fig. 1**. The circuit is connected to the expansion bus of the PC. Consequently, all control is effected via software. An important link between the DSP system and the PC is the 82C55 PPI (programmable peripheral interface). Other key parts in the circuit diagram are the DSP proper (IC<sub>1</sub>, an ADSP-2105), a D-A converter type AD1851 (IC<sub>2</sub>) and a bootstrap EPROM type 27512 (IC<sub>3</sub>). All other components

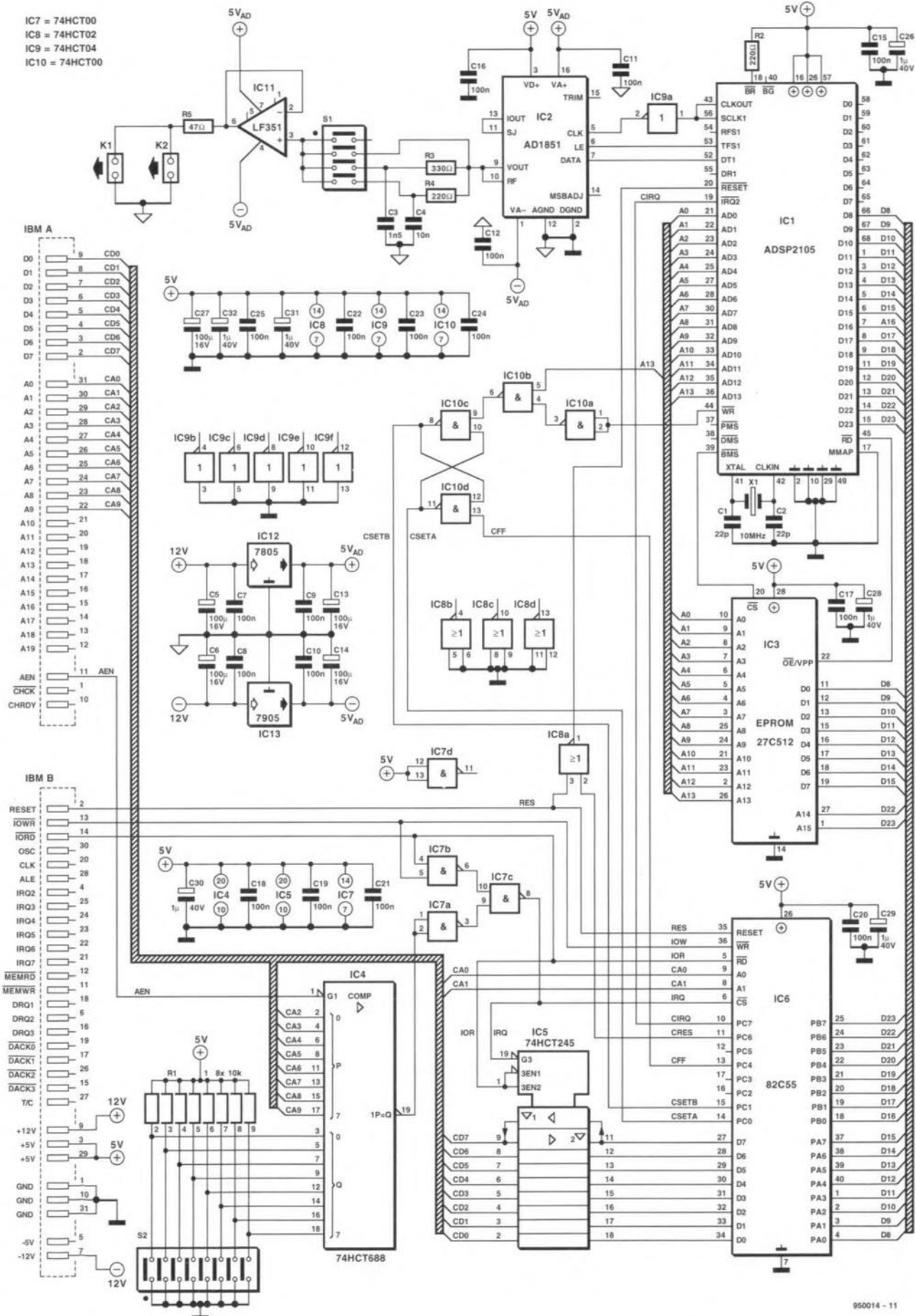


Fig. 1. Circuit diagram of the digital function generator. A digital signal processor (DSP) computes the waveform and sends it to a high-end PCM type D-A converter.

in the circuit are 'glue' between these key elements.

The EPROM, IC<sub>3</sub>, is connected to the DSP only, and directly. The EPROM contains a set of codes which are loaded by the DSP to enable it to start ('boot') at power-on. The fact that the eight data outputs of the EPROM are connected to datalines D<sub>8</sub>-D<sub>15</sub> of the DSP is not a mistake. The same goes for the circumstance that datalines D<sub>0</sub>-D<sub>7</sub> of the DSP are not used. Inside the DSP, three 8-bit wide bytes are converted into a 24-bit word, which is subsequently stored in the program memory.

The block diagram in Fig. 2 shows the structure of a circuit based on the ADSP-2105. The boot EPROM has a width of eight bits; the data memory and the I/O components have a width of 16 bits; and the program memory, a width of 24 bits. The external address bus of the ADSP is reserved for driving the EPROM. In addition, A<sub>13</sub> and  $\overline{WR}$  are used to generate an acknowledge signal via four NAND gates which mimic a bistable. The acknowledge signal is used by the processor to indicate that a command or instruction is understood. The computer can read back the acknowledge signal (CSTEA and CSTE $\overline{B}$ ) via the 8255 PPI. It responds by returning a CFF signal which resets the acknowledge generator (i.e. the NAND-based bistable). Because the EPROM is only required to boot the DSP, there is no link between this memory and the PC's expansion bus. During the boot operation, the DSP fetches the code from the EPROM, and stores it its internal program memory.

The complete address bus, the chip select lines and the databus of the EPROM are connected to the DSP only. After the boot-up operation, the DSP no longer uses the code contained in the EPROM. It then waits until the system has to be started again.

The DSP supplies a serial data signal (DT1 on pin 52), a clock signal (CLKOUT on pin 43) and a flag signal (TFS1 on pin 53). The serial clock signal is applied to the digital-to-analogue converter (DAC), but it is also read back by the ADSP via the SCLK1 input, pin 56.

The DAC used is a type AD1851 PCM audio digitizer from Analog Devices. There is little to say about the DAC proper. The device has a resolution of 16 bits, and is suitable for triple oversampling (a feature which is not used in the present application). The signal to noise ratio is about 96 dB. The AD1851 is specially designed for use in high-end CD players, digital amplifiers, DAT recorders, synthesizers and keyboards. The maximum clock rate for the serial input data is 12.5 MHz. In the present circuit, a clock of 10 MHz is used.

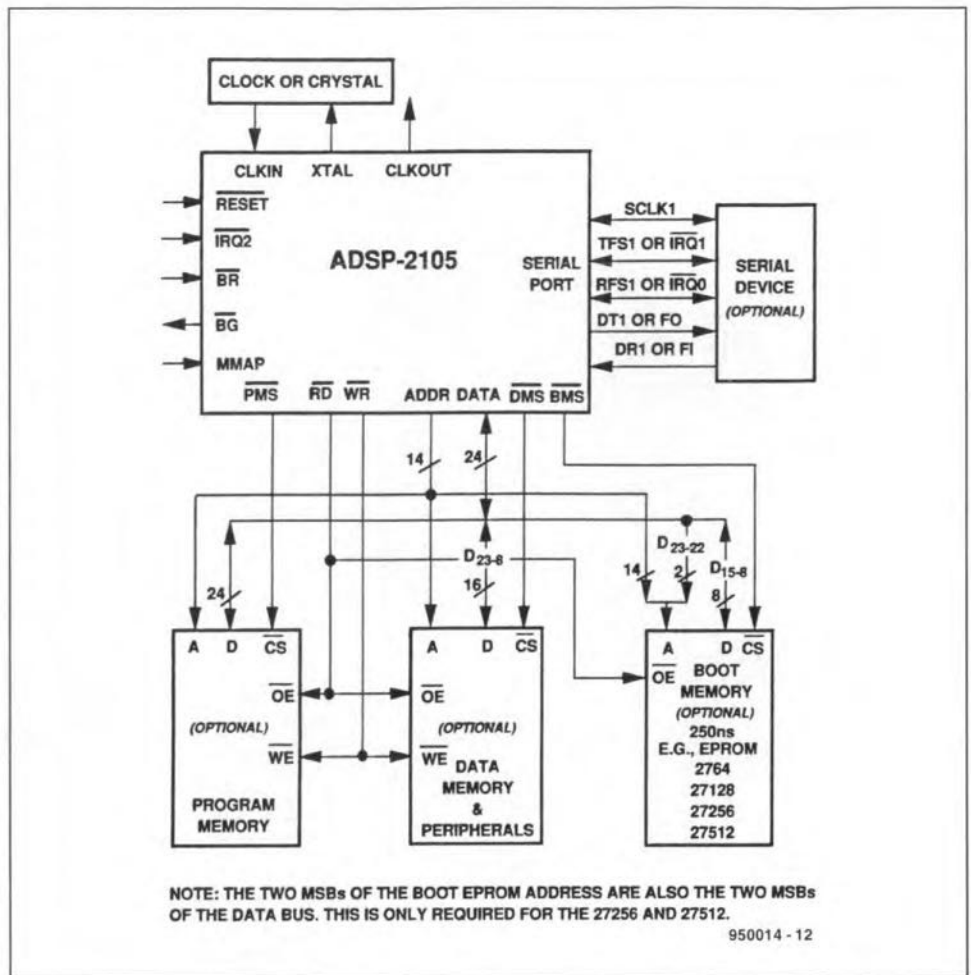


Fig. 2. The ADSP-2105 from Analog Devices uses three different bus widths, 8, 16 and 24-bit, for its memory functions.

The DAC output signal may reach buffer IC<sub>11</sub> via three different routes. DIP switch S<sub>1</sub> enables you to select a direct connection, without any kind of filtering, or the insertion of one of two passive low-pass filters. If the section consisting of R<sub>3</sub> and C<sub>3</sub> is selected, the roll-off frequency of the filter lies at about 320 kHz. If the other section, R<sub>4</sub>-C<sub>4</sub>, is selected, the roll-off frequency becomes 72 kHz. Switching off the filters is useful if noise or rectangular signals are required. The best waveforms are obtained when the 320-kHz roll-off is selected. Only the square waves are then 'rounded' a bit. The other roll-off, 72-kHz, is ideal for a perfect sinewave over the entire audio range. At higher frequencies, however, non-sinusoidal waveshapes are severely distorted by this setting, which is not suitable for generating white noise either.

After buffering by an LF351 opamp (IC<sub>11</sub>), the signal is available on two outputs (K<sub>1</sub> and K<sub>2</sub>) at an output impedance of 47 Ω.

The power supply is based on two integrated regulators, IC<sub>12</sub> for the +12 V line, and IC<sub>13</sub>, for the -5 V line.

The last sections of the circuit to be discussed are the address decoder and

the link between the 8255 and the PC. The address decoder compares the bit pattern set on switch block S<sub>2</sub> with that on address lines A<sub>2</sub>-A<sub>9</sub>. If the patterns match, and AEN is active, output P=Q drops low, and an enable signal is generated via IC<sub>7</sub>. The enable signal is only passed, by the way, if IOR or IOW is active at the same time. When the selection signal is present, IC<sub>6</sub> is switched on, and its databus inputs receive the levels present on the PC's databus. Together with the low-order address lines A<sub>0</sub> and A<sub>1</sub>, these drive signals RES (reset) IOW ( $\overline{WR}$ ) and IOR ( $\overline{RD}$ ), the selection signal enables the PC and the PPI to exchange data. Here, the 8255 takes four memory locations.

## Construction

As already mentioned, the circuit is designed as an insertion card for PCs. The copper track layouts and the component mounting plan of the double-sided through-plated printed circuit board designed for the function generator are shown in Fig. 3. This board is available ready-made through the Readers Services, along with the control software on diskette, and the programmed EPROM.

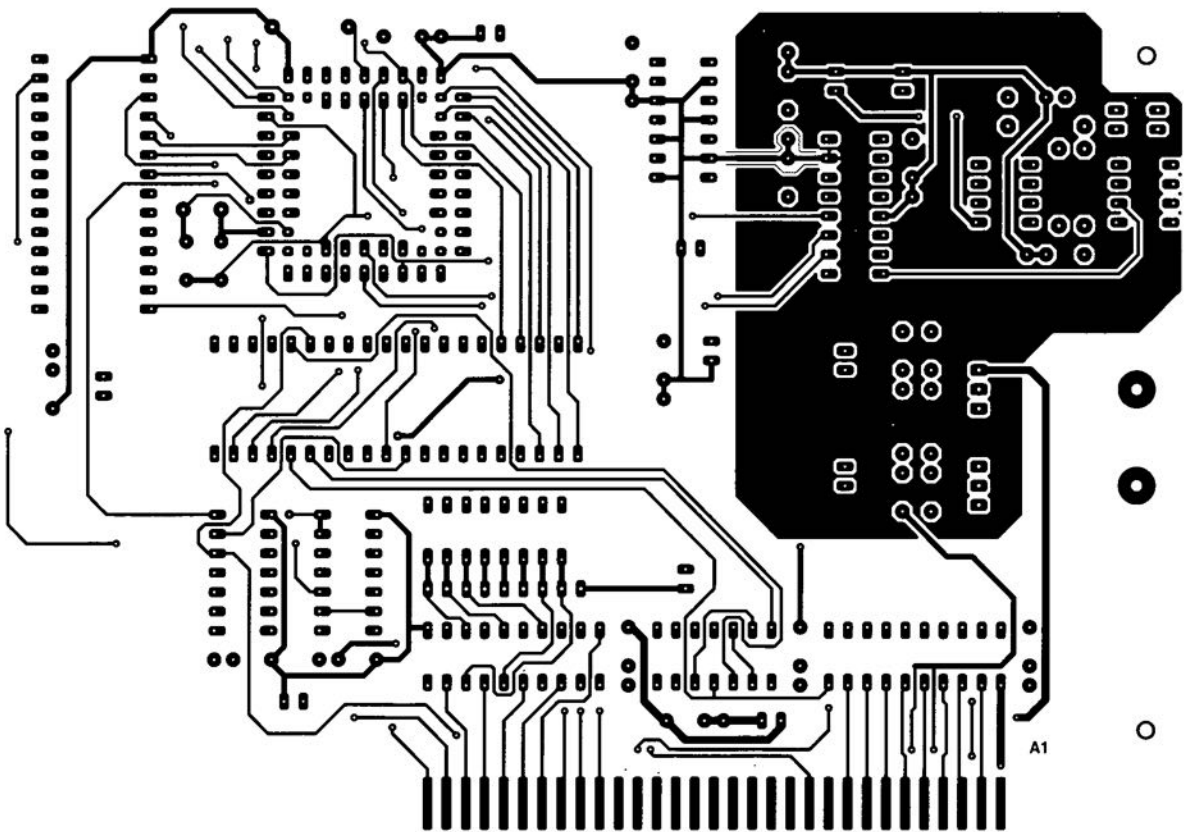
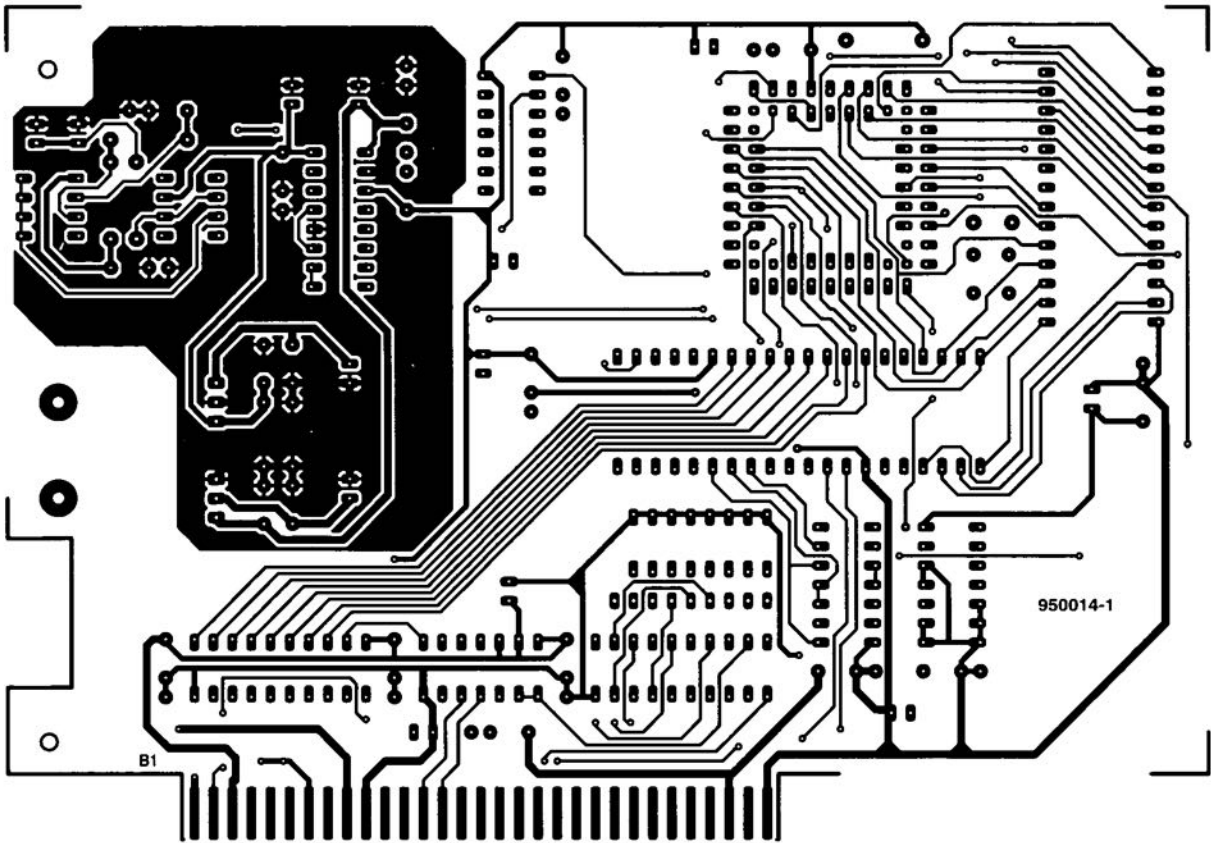


Fig. 3a. Copper track layouts (direct-reading) of the double-sided PCB designed for the function generator. Board available ready-made through the Readers Services (see page 78).

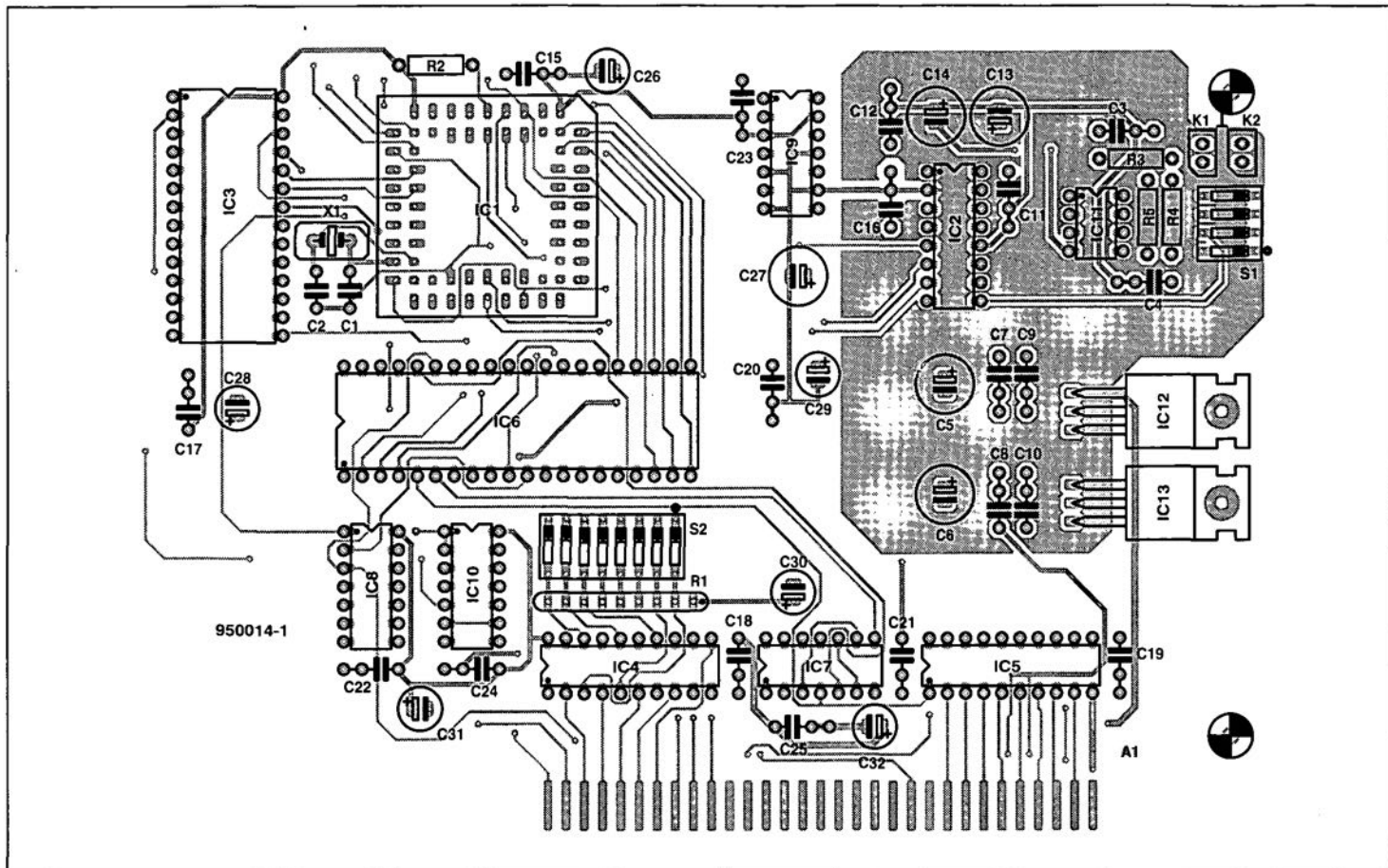


Fig. 3b. Component mounting plan.

Populating the PCB is mostly routine work, and is not expected to cause undue problems. It is recommended to use good-quality sockets for all ICs, except, of course, the two voltage regulators. All electrolytic capacitors are radial types for upright mounting. Make sure of their orientation (polarity!) before soldering these devices in place. The same goes for the ICs, although these are fitted in sockets rather than soldered.

Connectors  $K_1$  and  $K_2$  are mounted on the PC insertion card fixing bracket before this is secured to the PCB. The BNC and 'jack' type sockets require holes to be drilled in the bracket. Some PCB material below the BNC socket has to be removed to leave room for the nut that holds the socket in place. The bracket should also have a rectangular hole through which the levers of DIP switch  $S_1$  can be accessed.

Set the card address before inserting the card into a free expansion bus slot in the PC. The default address setting for this type of card is  $300_H$  ('experimental' according to the IBM I/O standard), which is set with switches 3 through 8 to 'on', and switches 1 and 2 to 'off'. Initially, select no filtering by setting all switches in  $S_1$  to 'off'.

## Control software

Good as the hardware may be, it is

## COMPONENTS LIST

### Resistors:

$R_1$  = SIL array 8x10k $\Omega$   
 $R_2; R_4$  = 220 $\Omega$   
 $R_3$  = 330 $\Omega$   
 $R_5$  = 47 $\Omega$

### Capacitors:

$C_1; C_2$  = 22pF  
 $C_3$  = 1nF5  
 $C_4$  = 10nF  
 $C_5; C_6; C_{13}; C_{14}; C_{27}$  = 100 $\mu$ F 16V radial  
 $C_7-C_{12}; C_{15}-C_{25}$  = 100nF  
 $C_{26}; C_{28}-C_{32}$  = 1 $\mu$ F 40V radial

### Semiconductors:

$IC_1$  = ADSP2105 (Analog Devices)\*  
 $IC_2$  = AD1851N (Analog Devices)\*  
 $IC_3$  = 27C512 EPROM (order code 956501-1, see page 78)  
 $IC_4$  = 74HCT688  
 $IC_5$  = 74HCT245  
 $IC_6$  = 82C55  
 $IC_7; IC_{10}$  = 74HCT00  
 $IC_8$  = 74HCT02  
 $IC_9$  = 74HCT04  
 $IC_{11}$  = LF351  
 $IC_{12}$  = 7805  
 $IC_{13}$  = 7905

### Miscellaneous:

$K_1$  = BNC socket.

$K_2$  = 3.5 mm dia. stereo headphones socket.

$S_1$  = 4-way DIP-switch.

$S_2$  = 8-way DIP-switch.

$X_1$  = quartz crystal 10 MHz.

Fixing bracket for PC insertion card, Vero type 427-59702K.

PCB, EPROM and disk: available as a set, order code: 950014-C (see page 70). Diskette also available separately: order code 956001-1.

\* Analog Devices, Worldwide Headquarters, One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A. Tel. (+1) 617 329-4700, fax (+1) 617 326-8703.

UK distributors: Arrow Electronics Ltd. (01234) 270777; Jermyn Distribution (01732) 743743; Polar Electronics Ltd. (01525) 377093.

Kits for this project available from C-1 Electronics, P.O. Box 22089, NL-6360-AB Nuth, The Netherlands. Fax (+31) 45 241877.

## ADSP-2105 FROM ANALOG DEVICES

The ADSP-2105 is a single-chip microcomputer optimized for digital signal processing (DSP) and other high-speed numeric processing applications. Its instruction set is a fully compatible superset of the ADSP-2100 instruction set. It combines the complete ADSP-2100 architecture (three computational units, data/address generators and a program sequencer) with a serial port, a programmable timer, extensive interrupt capabilities and on-chip program and data memory RAM. The block diagram shows the structure of the processor, and the parts which belong to the basis architecture. The chip has 512 words of (16-bit) data memory RAM and 1 K words of (24-bit) program memory RAM on chip.

The ADSP-2105 is the industry's leading cost/performance DSP. It offers a direct upgrade path to more highly integrated and higher performance DSP processors such as the ADSP-2101 and ADSP-2111. Designers selecting the ADSP-2105 will be able to preserve their investment in ADSP21xx development tools requiring the added features found on the higher-grade DSPs in the 2100 family.

The ADSP-2105 is feature and instruction set compatible with the ADSP-2101. The only differences are the sizes of the on-chip memories (half the size of the ADSP-2101's), the number of serial ports (one instead of two) and the processor speed. The ADSP-2105 serial port (SPORT) is identical to SPORT1 of the ADSP-2101.

The ADSP-2105's flexible architecture and comprehensive instruction set support a high degree of operational parallelism. In one cycle the ADSP-2105 can:

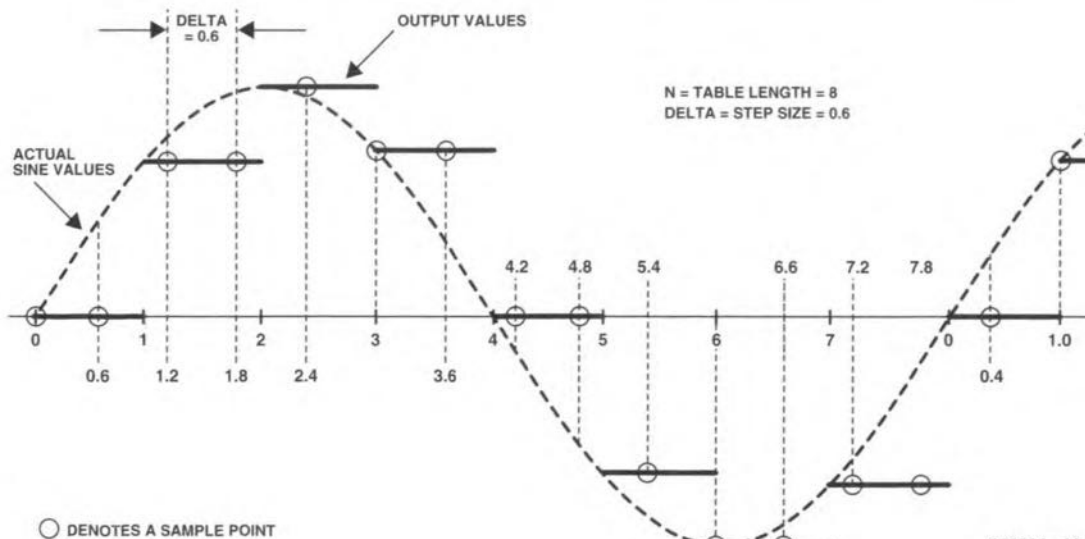
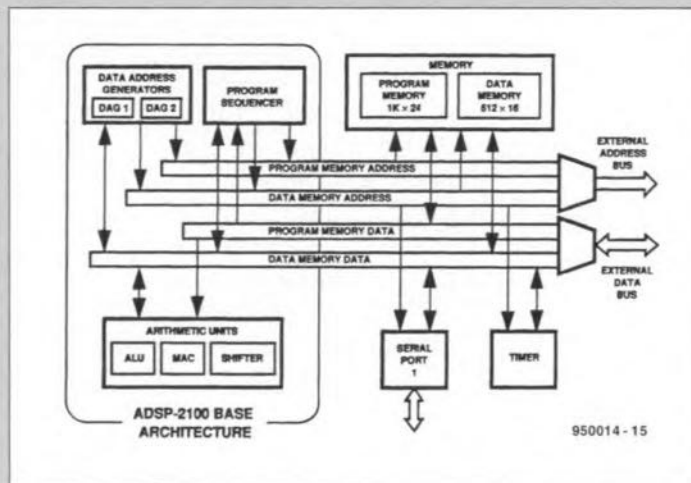
- generate the next program address
- fetch the next instruction
- perform one or two data moves
- update one or two data address pointers
- perform a computational operation
- receive or transmit data via the serial port

Fabricated in a high-speed double-layer metal CMOS process, the ADSP-2105 operates with a 100-ns instruction cycle time. Every instruction executes in one cycle. Fabrication in CMOS results in low dissipation. The ADSP-2105 dissipates less than 1 W under all conditions, and no more than 80 mW under standby conditions.

### Digital signal generation

With periodic signals, samples of one period are stored in memory. Next, the successive values are sent one after one to the DSP's output. The frequency of the output signal may be changed by varying the step size at which data is fetched from a look-up table. The address generators contained in the ADSP-21xx processors allow this to be achieved in a simple way because the table start address, the step size and the table length can be programmed with the aid of individual registers. After fetching a table entry, the processor automatically increases the address by the desired step size. If the length of the table is exceeded, the pointer automatically wraps around to the start of the table. In this way, a cyclic buffer/table may be created, provided each waveform is described by a data from a separate table contained in the memory.

The serial datastream at the DSP's output is converted into an analogue signal by a DAC. The DAC is usually followed by a low-pass filter which removes the steps from the signal. The diagram below shows how a digital sinewave is created.



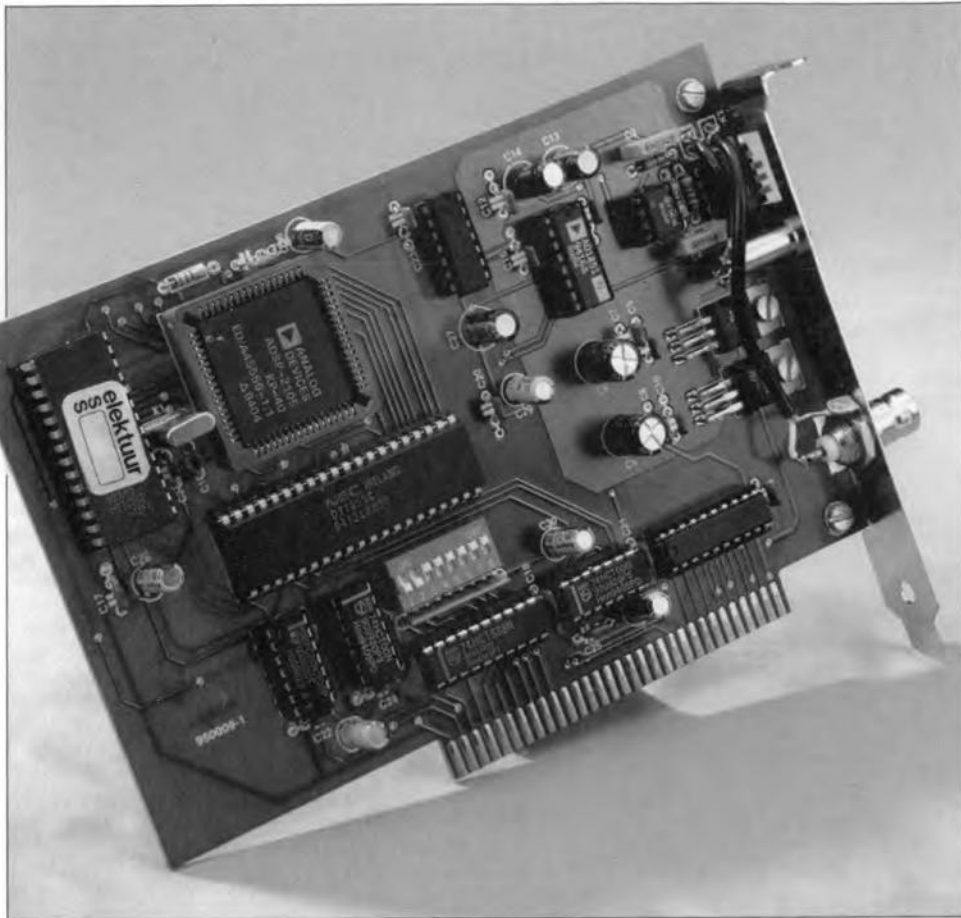


Fig. 4. Finished insertion card. The switches in block S<sub>1</sub> are accessible from the rear of the PC through a hole in the aluminium fixing bracket attached to the card.

useless without the appropriate software. The present project is supported by a couple of programs which allow the function generator to be controlled

from DOS as well as from Windows. The Windows software is much more extensive than the DOS version, and offers extra features such as defining

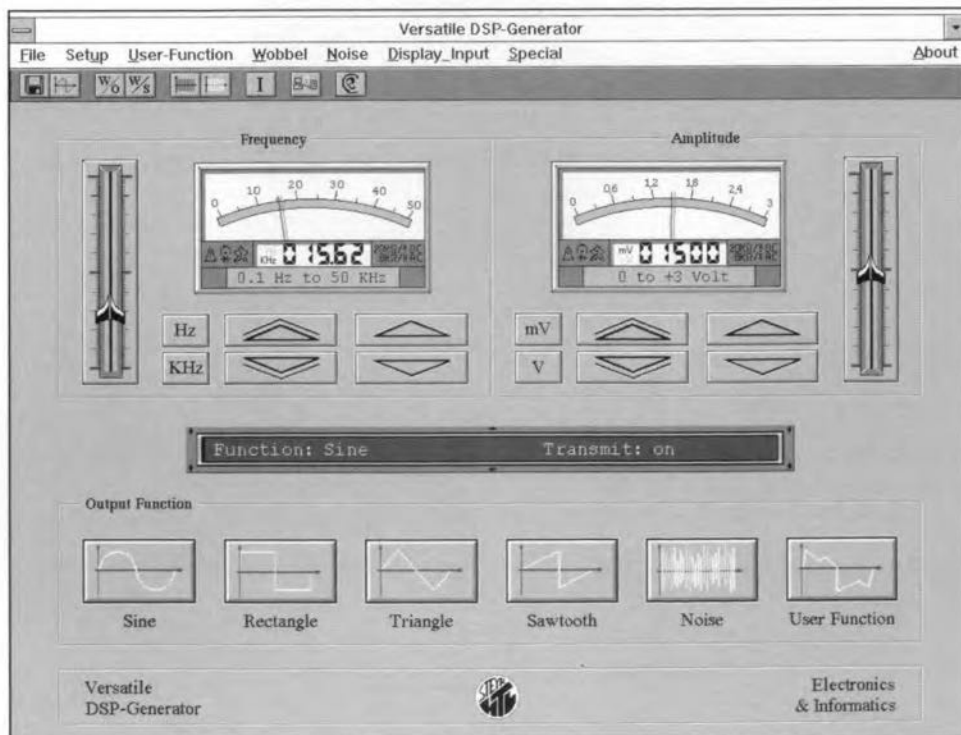


Fig. 5. Screenshot of the Windows program. Note the two panel meters with combined analogue/digital readouts.

an arbitrary waveshape, a hearing test and a sweep (wobbulator) function.

The DOS program, COMGEN, gives the DSP card the functionality of an ordinary, simple function generator for audio signals. It takes its commands and parameters from the DOS command line. Parameters are separated by a comma. When COMGEN is followed by a ? or **Help**, all options are shown on the screen.

The DOS command format is

COMGEN P: A: F: type:

- P:** sets the port address, for instance, 308. The desired address must be entered in hexadecimal after P:. The default address is 300.
- A:** sets the output level (amplitude) in millivolts.
- F:** sets the frequency in hertz.
- type:** SIN for sine wave;  
REC for rectangular wave;  
TRI for triangular wave;  
SAW for sawtooth;  
WHI for white noise;  
PIN for pink noise.

The first time you use COMGEN after a system reset, it must be followed by a LOAD command. This resets the DSP card and starts the DSP program. For example:

COMGEN LOAD A:1000 WHI

causes the generator to supply white noise at an output level of 1 V. The card address is 300<sub>H</sub>.

## For Windows, too

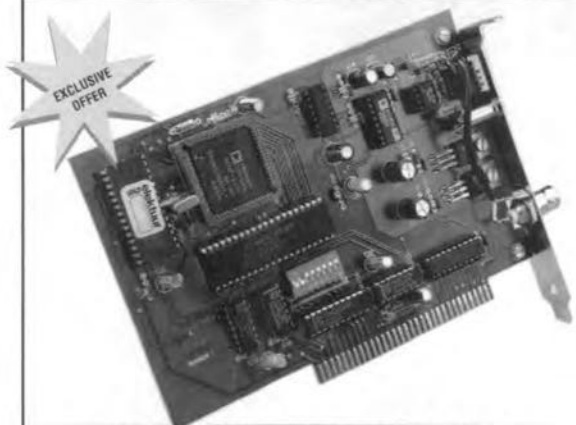
Windows users are treated to the perfect looks of mouse-operated on-screen buttons and pull-down menus, in short, a graphics user interface. The Windows software is on the same diskette as the DOS program.

After installing the Windows version of the program, you are ready to operate the DSP card without bothering to consult the users' guide. The minimum requirements of the program are: Windows 3.1 or later, 2 MBytes free on the hard disk, and a VGA card.

After clicking away the title screen, the generator's control panel appears on the screen. The eye catchers are two large panel meters with combined analogue and digital read-outs. The left-hand meter indicates the set signal frequency, and the left-hand meter, the signal level. Six push-buttons and a slide potentiometer allow the frequency and the level of the generator output signal to be set as desired.

A menu bar at the top of the screen gives access to a number of specific functions including a swept-frequency generator (wobbulator), white or pink noise generator, and a hearing test. The menu bar also takes you into the advanced configuration options. A full-

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74HCT573

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P&P 12.50

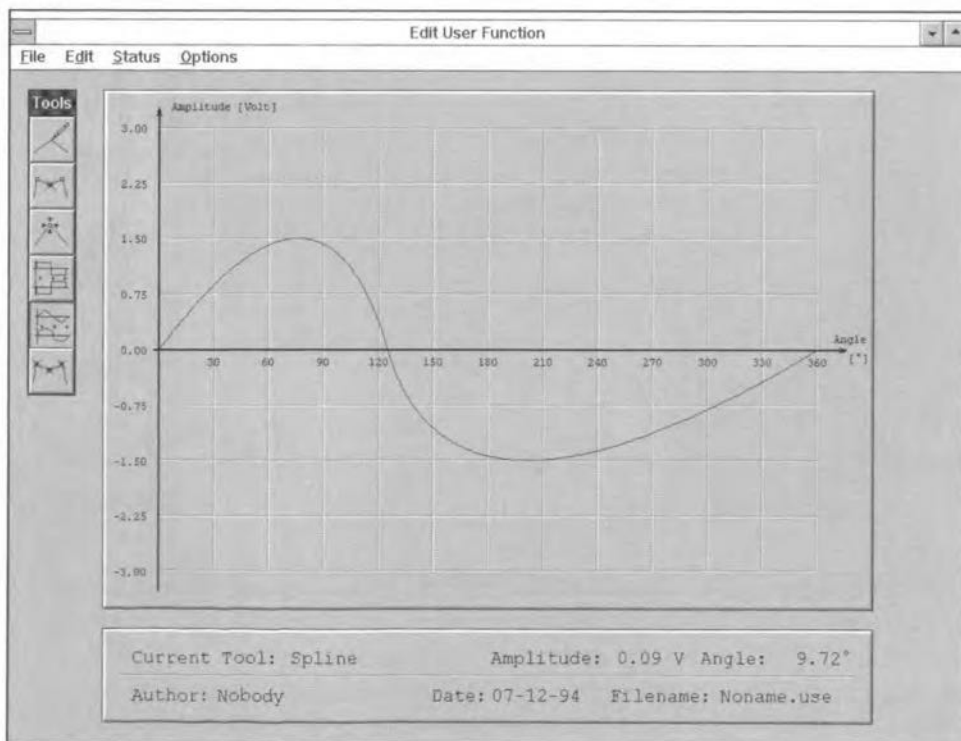
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screen editor is available for the user to compose a waveform.

Six buttons at the bottom of the screen enable the desired waveform to be selected. If the 'user' function is selected, the edit screen for this function has to be opened via the menu bar. The tools are then offered enable just about any waveform to be created — see Fig. 6.

Unfortunately, a full description of all features offered by the Windows software is beyond the scope of this article. However, the structure of the program is so clear that most questions can be answered simply by navigating through the different menus. Furthermore, a 17-page users' manual is available separately, which discusses the operation of the Windows software in great detail. The order code of this 'paperware' is 950014-P.

(950014)

Fig. 6. The Wave Editor in action. Compose your own waveform by drawing it!



# THE DIGITAL SOLUTION

## Part 4 – Analogue to digital

By Owen Bishop

**In this series we look closely at digital electronics, what it is, what it does, how it works, and its promise for the future.**

Last month we saw how binary information may be presented to a digital circuit. Binary information is essentially of the yes/no, true/false, off/on, high/low, variety. It has only two states or two levels. Much of the information we wish to process in a digital circuit is not like this. It is numerical information that can take any value within a given range. For example, we might wish to record digitally the temperature of a room, which may take *any* value within a range of, say, 5° to 35°. Or we may wish to process the rapid changes in air pressure that we call *sound*, or the brightness levels that go to make up a TV image.

The first stage in processing such quantities is to convert them into their electrical analogue values. Usually these values are expressed as voltages. These are not the same as those in a digital circuit, which can have only two values, low and high. Analogue voltages can take any value within a given range, and change smoothly from one value to another. The electrical analogue of a sound wave is a voltage whose changes are analogous to the changes in air pressure of the original sound. Before the analogue voltage can be processed in a digital circuit, we must convert it into its digital equivalent. For this, we use an *analogue-to-digital converter*, known briefly as an *ADC*.

Analogue quantities are represented in the digital circuit as numbers on the binary scale. The individual binary digits (or *bits*) have the value 0 or 1, and these values are represented by a low or high voltage. A binary number of several bits is represented by a number of registers set to 0 or 1, or by the low and high voltages on a set (or *bus*) of data lines. The more precisely we want to express the quantity, the more bits, register or data lines we use.

If we use eight bits, the

range of possible values is from 00000000 to 11111111. This is from 0 to 255 in decimal, so there are 256 ( $=2^8$ ) possible values. If the quantity is a voltage which may range from 0 V to 1 V, there are 256 steps in this range. One step (an increase of the binary value by 1) is equivalent to a value change of  $1/256 = 0.0039$  V. If we wish to express values more precisely than this, we must increase the number of bits. With 12 bits, the range is from 0 to 4095, with 4096 ( $=2^{12}$ ) possible values. The difference between adjacent values is reduced to 0.00024 V. In the circuit we describe below we assume that we are working with eight bits, but the operation of the circuit is the same, irrespective of the number of bits.

There are several distinct ways of converting values from analogue to digital form. We describe the most important techniques and outline their advantages and disadvantages. The circuit diagrams show the converters as a number of functional blocks. In most cases, it would be possible to assemble the converter from these units separately. But normally, the complete converter is available as an integrated circuit, needing perhaps only a few external capacitors and resistors.

### Counter converter

The interesting point about the ADC in Fig. 31 is that it is based on a DAC, a *digital-to-analogue* converter. The action of DACs will be described in a future instalment. For the present, we limit ourselves to saying that a DAC accepts a digital input and produces the

equivalent analogue output within a range extending from 0 V up to a preset maximum. In the figure, the eight digital inputs,  $D_0$  to  $D_7$ , of the DAC are fed from the outputs of an 8-bit counter. To start the conversion, the counter is reset so that all outputs are 0. Resetting and various other operations are performed by a simple control circuit consisting of a number of logic gates. The precise nature of the control circuit is not relevant to the description of the operation of the converter.

The all-zero input to the DAC results in it giving a 0 V output, and we assume that there is a positive voltage at the analogue input terminal. The + input of the comparator is therefore greater than the - input, so its output swings to logic high. A high input on one input of the AND gate causes its output to follow the level on the other input. Pulses from the clock pass through the AND gate and increase the counter.

The increasing output from the counter passes to the DAC and its output rises. If this process is allowed to continue, the voltage from the DAC increases in 256 steps from 0 V up to the maximum. In a typical converter it is arranged that the voltage increases in steps of 0.01 V from 0 V to 2.55 V. For as long as the output from the DAC is less than the analogue input voltage, pulses continue to pass to the counter and the count increases. Eventually, provided the analogue voltage is not greater than 2.55 V, an incremental step takes the DAC output just above the analogue voltage. Instantly, the output of the comparator swings low and stays low. No more pulses pass to the counter, which remains registering the count it has reached.

A signal from the control circuit informs the next stage of the digital circuit that conversion is complete. The eight output lines indicate the binary value corresponding to the analogue voltage. In some converters, this value is held on a series of eight *registers* or *latches*, while the counter is reset and counting begins again to find the new value of the analogue input.

The counter converter is

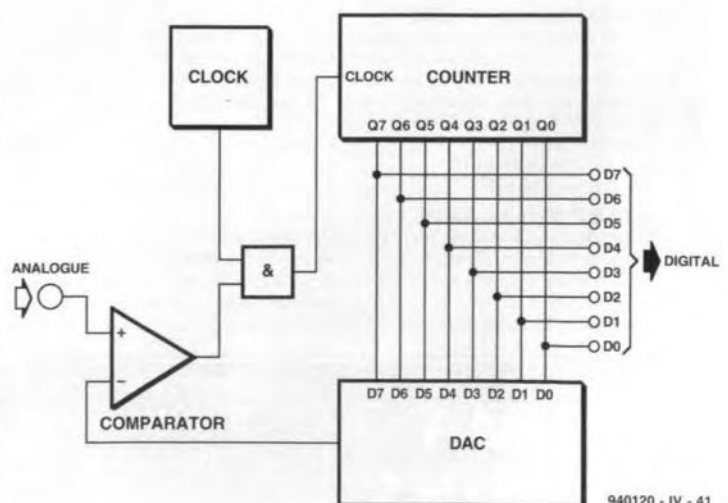


Fig. 31

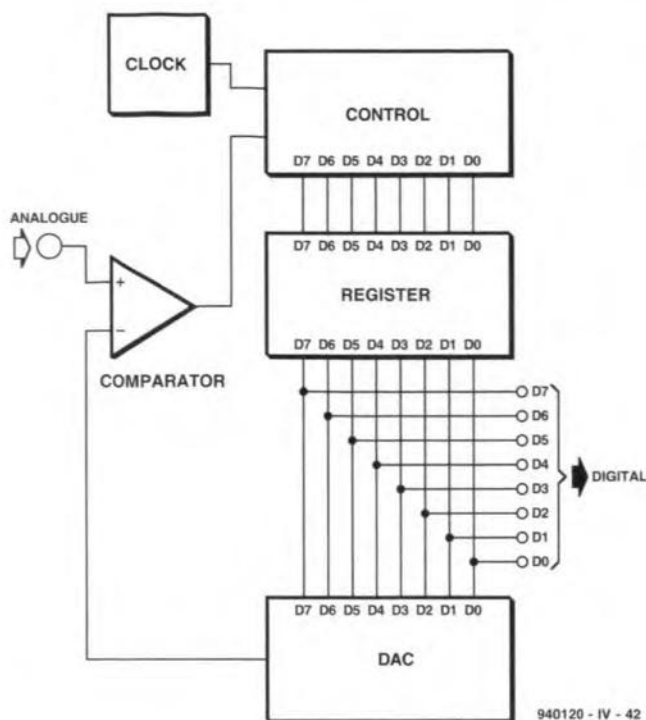


Fig. 32

available as an inexpensive IC, the ZN425E. It is easy to set up and use. One of its disadvantages is that it is slow. A more serious drawback is that the time taken for conversion depends on the analogue voltage. For example, with steps of 0.01 V, an analogue voltage of 0.05 V is matched after only five steps, but it takes 200 steps (40× as long) to match an input of 2 V. This means that a relatively high input voltage is sampled less often than a low input, so rapid changes in the voltages are followed less accurately. Another point is that the input is allowed to change while counting proceeds. Sometimes, the input may be increasing slightly ahead of the count, whereas at other times it may fall to meet the count. As a result of this, the input is converted at irregular intervals.

A variation on the counter type of ADC has the clock pulses going directly to the counter, and there is no AND gate. The counter is an up/down type, with an 'up' input and a 'down' input. The counter is increased on each clock pulse when the 'up' input is high, but decreased when the 'down' input is high. Both inputs are fed from the comparator and there are two situations:

1. analogue input higher than DAC output → comparator output high → counter increased.
2. Analogue input lower than DAC output → comparator input low → counter decreased.

This makes the counter follow the changes in analogue input instead of being reset and having to count up for every conversion. If the analogue input

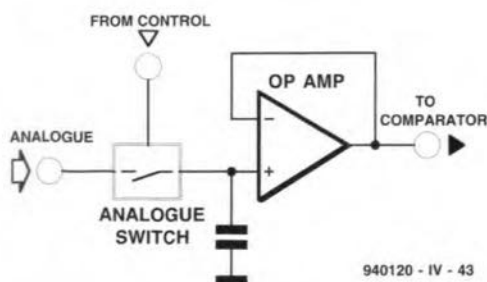


Fig. 33

Control output	DAC output (V)	Comparator output
00000000	0.00	high
<u>1</u> 0000000	1.28	low
0 <u>1</u> 000000	0.64	high
01 <u>1</u> 00000	0.96	high
011 <u>1</u> 0000	1.12	low
0110 <u>1</u> 000	1.04	high
01100 <u>1</u> 00	1.00	low
011001 <u>1</u> 0	1.02	correct; retain the present setting for that digit
011001 <u>1</u> 1	1.03	high
011001 <u>1</u> 0	1.02	correct; conversion complete

Table 1

is varying by fairly small amounts between consecutive conversions, the counter never has far to count to match the DAC output to the analogue input. It may take only a few steps for each conversion, which makes conversion much quicker and more accurate. Also, conversions are completed at more regular intervals.

The main disadvantage of the tracking counter ADC is that, if the input voltage is constant, the counter is made to count up and down alternately at each conversion, which causes its output to oscillate.

### Successive approximation

An ADC using *successive approximation* is shown in Fig. 32. It has some features in common with the counter type: it has a DAC, clock, and comparator, but no counter. Instead of the counter, it has a control circuit which feeds its output to an 8-bit register. The register holds the values it receives from the control, and passes them to the DAC. The clock causes the control to step through its program.

At the beginning of a conversion, the register is set to 00000000 by the control and the output of the DAC is 0 V. The analogue input is greater than this, so the comparator output swings high. This level causes digit D<sub>7</sub> of the control to go high, so that its output is 10000000. This is held in the register and fed to the DAC. The effect of this is to cause the output of the DAC to rise to its half-way value. For example, if the maximum value

is 2.55 V (equivalent to 256 steps, or a count of 11111111), the output is 1.28 V. If the analogue input is *greater* than this, the comparator output remains high and the next digit, D<sub>6</sub>, is made high. The value 11000000 produces a DAC output of 1.92 V. However, if the analogue input is *smaller* than 1.28 V, D<sub>7</sub> is made 0 and D<sub>6</sub> is made 1. The value 01000000 makes the DAC output change to 0.64 V. Suppose that the analogue input is smaller than 1.28 V, but greater than 0.64 V. The range of possible voltages has been narrowed down. At the next clock pulse, the control output is changed to 01100000 (0.96 V) and, assuming this turns out to be too high, to 01010000 (0.80 V). The range has been narrowed to 0.64–0.80 V.

Working along the row of digits, the control circuit cuts the remaining range into two halves at each stage and decides whether the analogue input is in the upper half or lower half of the range. This is the technique of successive approximation. It homes on the correct analogue value in nine clock pulses.

To make the routine clear, follow the sequence as it homes on an analogue input of 1.02 V (see Table 1, in which the newly changed digit is underlined).

The binary search for the correct value, continually halving the range and selecting the appropriate half, is fast. It makes this type of ADC one of the fastest of those described here. There is one slight complication: if the analogue voltage is changing rapidly, the circuit might not home on it

sufficiently quickly. The input might 'slip through the net' and not be found. To guard against this, it is necessary in some high-speed applications to hold the analogue input constant while it is being converted. This is done by the use of a *sample-and-hold* circuit.

A typical sample-and-hold circuit is shown in **Fig. 33**. The analogue switch is a digitally controlled (or electronic) type. Unusually for a digital circuit, its input can take any value between 0 V and the +ve supply voltage, and its output takes the same value as its input. When the control input is low, the input and output are isolated from each other, with a typical leakage current of 1.5 nA. When the control is high, the switch is turned on and has an input-to-output resistance of about 250  $\Omega$ . To sample the analogue voltage, the switch is turned on by a high pulse from the control circuit. During this pulse, the capacitor is charged to the input voltage. When the pulse ends, the switch is turned off and the capacitor holds its charge; it can not leak away through the switch. The operational amplifier has a very high input impedance, so the charge can not leak away in that direction, either. The op amp is wired as a voltage follower, so its output equals the sampled voltage and is converted to digital form by the ADC. The switch is then opened to allow the capacitor to be recharged to the most recent analogue level, ready for the next sampling.

### Dual slope integration

The dual slope integration type of ADC relies on an entirely different principle. It is

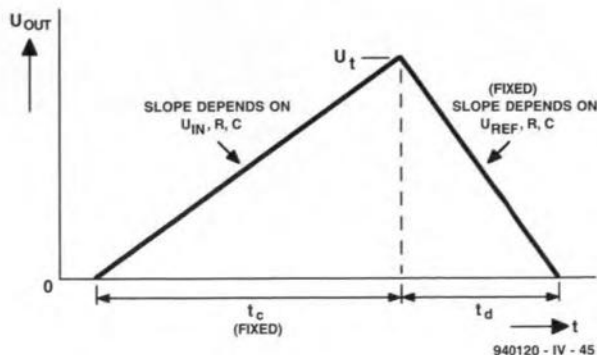


Fig. 35

based on an op amp wired as an integrator as shown in **Fig. 34**. At the beginning of a conversion cycle, the capacitor is discharged, and the counter is reset to zero. The double-throw analogue switch is set to connect the op amp to the incoming analogue voltage. The output of an integrator is a ramp and, assuming the capacitor is discharged to begin with:

$$U_{\text{out}} = (-1/RC) \int_0^{t_c} U_{\text{in}} dt$$

The control lets the output ramp down (or up, if the analogue voltage is negative) for a fixed number of clock pulses. We will assume that the input is negative and that the output voltage ramps up to  $+U_t$ . Then, the analogue switch is changed to connect the op amp to a reference voltage. The reference voltage has the opposite polarity to the analogue input. This is easily arranged, because the comparator will already have informed control of the polarity of the charge during the charging phase.

The discharge phase lasts

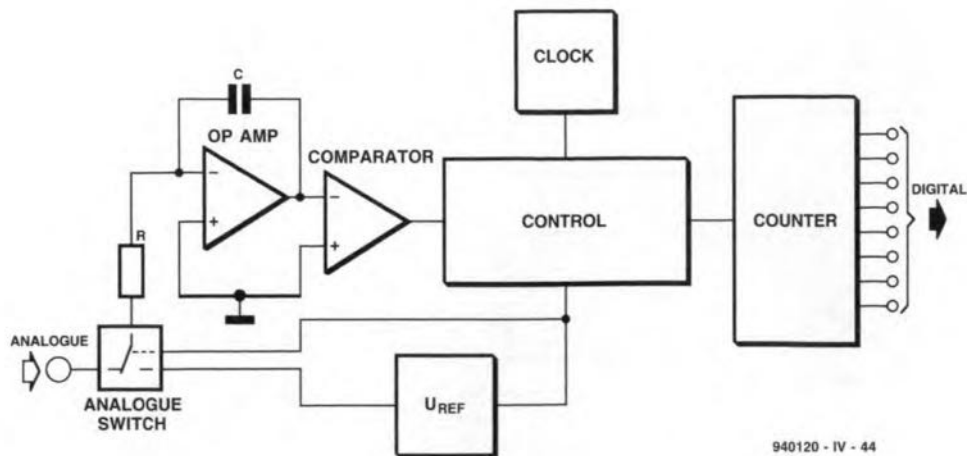


Fig. 34

for as long as it takes the capacitor to become discharged to bring the op amp output back to zero. The length of this phase,  $t_d$ , is measured by counting clock pulses. During the charging phase, the slope of the ramp at any instant depends on the magnitude of the analogue voltage, but the time of charging is fixed. The output voltage reached by the op amp depends on the average ana-

logue input and on  $R$  and  $C$  (see **Fig. 35**). During the discharge phase, the slope of the ramp is fixed. The time taken to reach zero depends on the slope and the output voltage reached at the end of the charging period. Since  $U_t$  is proportional to  $U_{\text{in}}$  and  $t_d$  is proportional to  $U_t$ ,  $t_d$  is proportional to  $U_{\text{in}}$ .  $R$  and  $C$  merely act as scale factors and apply to *both* periods, so their

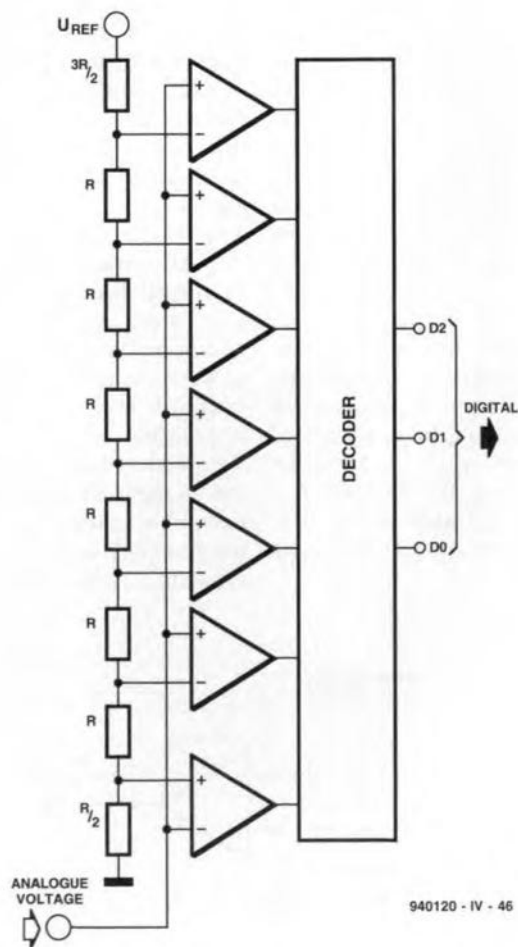


Fig. 36

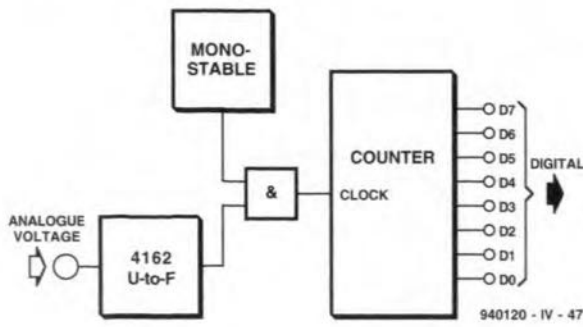


Fig. 37

values cancel out of the calculation. We are left with:

$$U_{in} = -U_{ref} \times t_d/t_c$$

We have already noted that the values of  $R$  and  $C$  do not affect the calculation of  $U_{in}$ . This means that the precision of the conversion does not rely on the use of a high-precision resistor and capacitor. The result is unaffected even if the resistor and capacitor values change over a period of time owing to ageing. In addition, the charging and discharge times appear in the equation as a *ratio*. We need to count only the *numbers* of clock pulses (easy to do digitally), but the precise length of the pulses is unimportant. Finally, the integrating action of the op amp means that it is the average value of  $U_{in}$  that is being measured. Noise on the input is largely ignored. The only critical value in the equation is that of the voltage reference; a high precision reference is essential and is easily provided.

As a result of the factors listed above, the dual slope ADC has high precision and stability. For this reason, it is often used in instrumentation

applications, such as digital voltmeters.

### Flash converter

The converters described so far all rely on counting circuits and an appreciable time is required, therefore, for each conversion. An 8-bit successive approximation converter, for instance, with a typical clock rate of 900 kHz, requires nine clock periods, that is, 10  $\mu$ s. One hundred thousand conversions per second is, however, more than the other types can achieve. Although such a high conversion rate is adequate for most purposes, there are applications where higher rates are essential. For example, conversion of analogue video signals in real time requires several million samples per second, often to at least 12-bit accuracy. For purposes such as this, we use flash conversion which, as its name implies, is very fast. The principle is illustrated in Fig. 36, which shows a 3-bit converter.

For a resolution of  $n$  bits, we have a chain of  $2^n$  resistors, fabricated on a silicon chip, connected between a reference voltage and ground. The result

is a series of tapping points at precisely known and equally spaced voltages. If the resistor value is  $R$ , with the top resistor  $3R/2$  and the bottom resistor  $R/2$ , the voltage across each resistor is  $U_{ref}/2^n$ . The voltage at each tapping point is compared with the input analogue voltage by a series of comparators. We need  $(2^n - 1)$  comparators. For a given input voltage, there will be a number of comparators at the lower end of the chain which have a logic high output because the analogue input voltage is greater than their reference voltage. The remaining comparators will have a logic low output. The outputs of the comparators are decoded by a logic circuit which produces a digital output representing the input voltage. The time taken for conversion is simply that required for a comparator to settle to a stable output level, making it possible to perform ten million or more conversions per second.

The main disadvantage of this type of converter is the large number of comparators required. An 8-bit converter needs 255 comparators. This order of accuracy is not always required in video circuits, so 6-bit converters are made that need only 63 comparators.

### Voltage to frequency

As mentioned earlier, there is a tendency in digital circuitry, especially with the falling cost of microprocessors and microcontrollers, to replace hardware solutions by software solutions. The converters described so far in this article are essentially hardware. Their output is a binary number

which can be used directly by subsequent digital circuits. A *voltage-to-frequency* ( $U$ -to- $f$ ) converter performs only part of the analogue-to-digital process, leaving the final stages to be performed by software.

A  $U$ -to- $f$  converter is a voltage-controlled oscillator with a square-wave output. The VCO found in the 4046 phase-locked loop IC described in an earlier instalment can be used as a simple converter. The difficulty is that its response is not perfectly linear, so it is unsuitable for use in several applications. The 4152 is a VCO with 1% linearity. It generates a square-wave output in which the pulses are of equal length and their frequency is proportional to the input analogue voltage. The output from the IC can be fed to a counter IC as in Fig. 37. All that is needed to complete the circuit is a monostable to feed pulses from the IC to the counter for a fixed length of time. The count is proportional to the analogue voltage.

An alternative technique is to feed the output from the converter directly to an input port of a microcontroller system or microcomputer. Software monitors the input and counts the number of pulses received during a given period of time. Note that it is possible to have a long lead joining the converter to the computer, making this type of converter suitable for remote measurements.

### Voltage to time

Voltage-to-time conversion is another technique that lends itself to software processing. The 507C is a low-cost IC that is able to perform a 7-bit conversion, typically in 1 ms. It is a *single-slope* converter that consists of a counter driven by an external clock and a DAC which produces a descending ramp voltage—see Fig. 38. The ramp voltage is continuously compared with the input analogue voltage. Provided that the input voltage is greater than 200 mV, the output of the IC goes high whenever the ramp voltage exceeds the analogue voltage. Thus, we obtain a series of pulses at a fixed frequency ( $1/64 \times$  the clock frequency) but with a *pulse width* proportional to the input

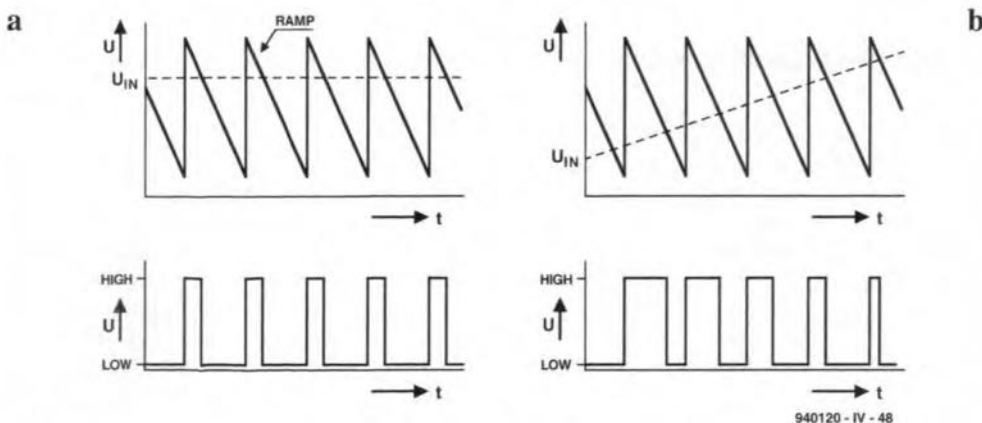


Fig. 38

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voltage. Figure 38b shows the pulse width gradually decreasing as the input voltage increases.

In a digital application, the output of this converter is fed to the input of a digital timing circuit or to a microcontroller system. The length of the high pulses is measured and, from this information, the value of the input analogue voltage is calculated. As in the previous

example, the output is suitable for transmission along a wire and may be used, therefore, for remote sensing. One point to notice is that this is not an analogue-to-digital converter: it converts one analogue quantity, voltage, into another analogue quantity, time. But time is an analogue quantity that is more easily measured by software.

[940120-IV]

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### Test yourself 4

1. Make a table of the successive approximation in an 8-bit ADC (Fig. 32) if the maximum analogue input is 2.55 V and actual input is 0.45 V.
2. A dual slope ADC has  $R = 22 \text{ k}\Omega$ ,  $C = 1 \text{ nF}$ , clock rate = 2 MHz, and  $U_{\text{ref}} = -5 \text{ V}$ . The capacitor takes 400 clock pulses to get charged and 250 clock pulses to become discharged. What is the value of  $U_{\text{in}}$ ?
3. A flash converter has a 4-bit output. How many comparators does it need? If the reference voltage is 5 V, what is the voltage across each of the resistors in the chain?

# TELEPHONE-CONTROLLED SWITCH

Design by H. Kiprowski

**A switch, based on a PIC<sup>1</sup> RISC<sup>2</sup> processor, is described that enables mains-operated equipment, such as a computer, a coffee maker, or the central heating to be switched on and off via a telephone line.**

The 'teleswitch' is operated via a telephone line and can switch the mains on and off as often as required. It is well-protected against unauthorized use and can be switched to manual operation so that it need not be unplugged when the user is at home. Moreover, it does not increase the telephone bill since it reacts to the bell signal: communication need not be established.

The switch is based on a CMOS RISC processor Type PIC16C54LPOTP from Microchip. This processor contains 12 I/O lines that can be programmed individually, its own clock oscillator, programmable internal registers that can serve as RAM, and 512 bytes of ROM.

The letters LP stand for Low Power, indicating that the processor draws a minute current only.

The last three letters in the type coding indicate One Time Programmable. This means that the PIC can be programmed only once: it can not be erased. This type of PIC is significantly less expensive than the types with a window and EPROM that can be programmed and erased many times.

The clock signal may lie between d.c. and 400 kHz. Since in the present application the low-frequency telephone signal is used, an inexpensive 32.768 kHz crystal can be used.

## Circuit description

The circuit—see **Fig. 1**—consists of four distinct sections: power supply, telephone interface, PIC and a relay-operated switch.

The telephone interface is connected to the telephone line via terminals **a** and **b**. Capacitors **C7** and **C8** prevent the direct voltage on the telephone line entering the switch: only the 48 V bell signal is passed by them. This alternating voltage is half-wave rectified by **D2** and limited to a level of  $-0.7$  V to  $+4.7$  V. This voltage is applied to the LED in optoisolator **IC3**, which then lights. Resistor **R5** keeps the current within safe values. When the telephone

bell rings, a rectangular voltage of about 5 V appears on the collector of the optotransistor and thus at input **RB3** of **IC1**.

When the PIC is actuated by a bell signal or manually by **S1** being pressed, its output **RB0** becomes high. This switches on **T1**, which in its turn energizes the relay. Socket **K2** is then connected to the mains via plug **K1**.

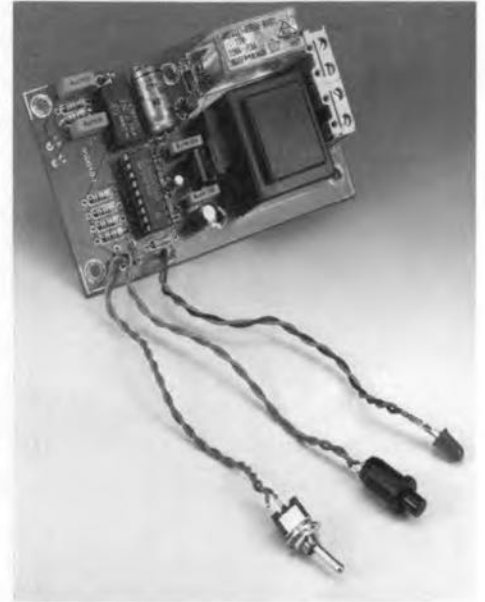
Inputs **RB1** and **RB2** of **IC1** are held high via pull-up resistors **R1** and **R2** when both **S1** and **S2** are open.

The internal clock oscillator is controlled by crystal **X1**.

Diode **D3** is a function indicator.

Both **IC1** and **IC3** are powered by a simple, regulated 5 V supply provided by **B1**, **IC2**, and capacitors **C1**–**C4**.

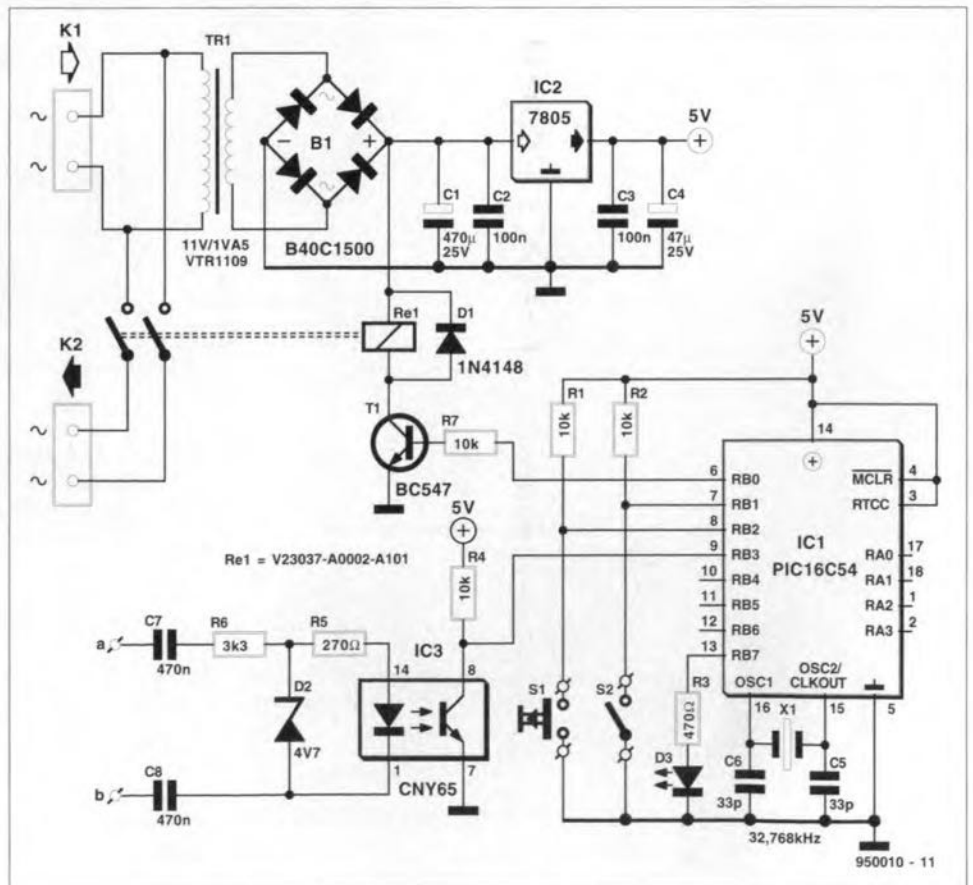
The relay is energized by the unregulated 14 V at the +ve terminal of the bridge rectifier. The relay contacts are rated at 5 A. The constant-power rating of the relay is 1200 VA.



## Program

The program stored in the PIC ensures simple control of the switch. It starts automatically when the switch is connected to the mains and immediately checks whether **S2** is open or closed. If this switch is open, **RB1** is high: the processor is then in manual control mode. In this mode, the switch is operated by pressing **S1**.

The 'teleswitch' acts as a remote



**Fig. 1.** Circuit diagram of the telephone-controlled switch.

<sup>1</sup> = Peripheral Interface Controller

<sup>2</sup> = Reduced Instruction Set Coding

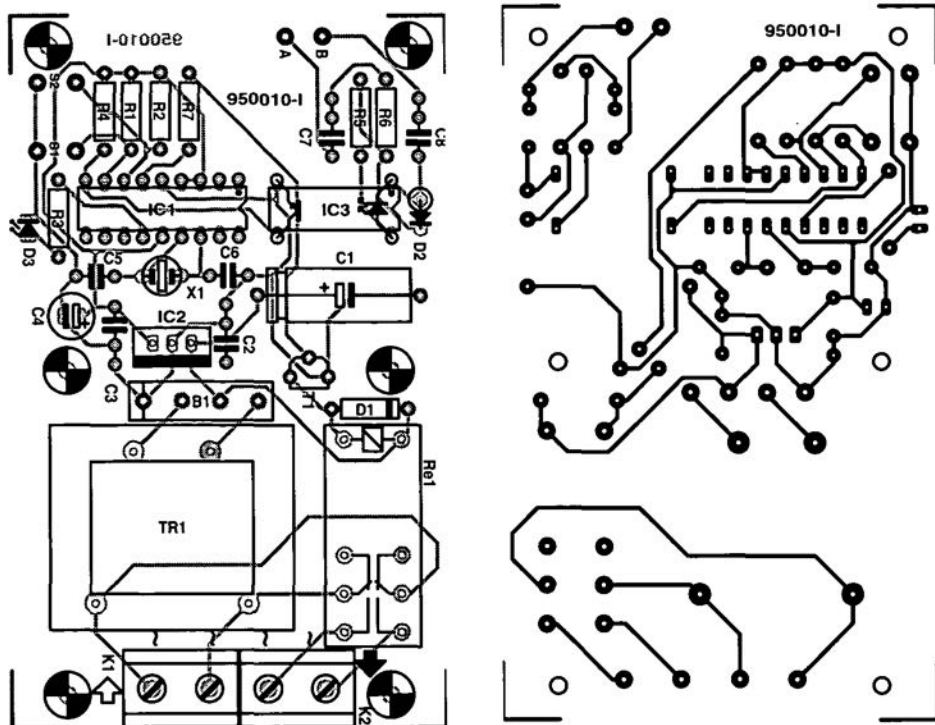


Fig. 2. Printed-circuit board for the telephone-controlled switch.

controlled unit when  $S_2$  is closed; the state of  $S_1$  is then immaterial.

When  $S_2$  is closed, input  $RB_3$  is monitored to ascertain whether a valid bell signal is received. A bell signal is valid only if it consists of one call tone only. Thus, the remote operator dials the number of the telephone, lets it ring once only and then returns the handset to the cradle.

The program waits for seven seconds after the call has been received. If during that time no further bell signal is detected, output  $RB_7$  is actuated, whereupon  $D_3$  lights to indicate that the first part of the input code has been accepted. A second internal counter then enables the caller to re-

peat the call within 50 seconds.

Only if within this period the bell rings once and not again within seven seconds, the total code is accepted as valid. Output  $RB_0$  then changes state, whereupon  $D_3$  goes out to indicate that the switch is in the standby mode.

Since many electronic telephone exchanges generate a short initial call tone, the program is arranged to ignore this first ring if the second follows within two seconds. This means that a bell signal is not valid when the interval between two rings is longer than two and shorter than seven seconds. The program is also interrupted when the interval between two rings is longer than 50 seconds.

When a bell signal has been judged invalid, the switch immediately reverts to its standby mode.

Note that manual operation can be selected with  $S_2$  in either operating mode.

If the switch is used to switch a computer on, an acknowledgment from the computer may be arranged via its modem.

Without PC and modem, a control acknowledgment may be arranged via a (existing) telephone answering machine, which must be connected in parallel with the equipment or device to be switched. In that case, if, on a second call, the answering machine comes on line, it is certain that the equipment or device has been switched on.

## Construction and installation

The 'teleswitch' should be built on the printed-circuit board shown in Fig. 2. The PIC and optoisolator are best fitted

in appropriate sockets to enable them to be changed easily. It is advisable to cut any terminals protruding from the track side of the board as short as possible to prevent them piercing the insulation of the connecting wires running beneath the board. It is, actually, advisable to separate the board from these wires by a thin sheet of perspex or other insulating material.

If possible, fit the board in an enclosure already fitted with a mains plug and socket. Connect  $K_1$  to the plug and  $K_2$  to the socket.

Terminals **a** and **b** of the switch are connected via a length of (two-wire) telephone cable to the relevant pins of an appropriate plug that fits in the telephone socket. Since these sockets vary from country to country, no further information on them can be given. Note by the way that in certain countries it may not be allowed to connect the 'teleswitch' to the public telephone network: seek advice from your local telephone authority. There is, of course, no objection to using it with a private telephone system.

## Parts list

### Resistors:

$R_1, R_2, R_4, R_7 = 10 \text{ k}\Omega$   
 $R_3 = 470 \Omega$   
 $R_5 = 270 \Omega$   
 $R_6 = 3.3 \text{ k}\Omega$

### Capacitors:

$C_1 = 470 \mu\text{F}, 25 \text{ V}$   
 $C_2, C_3 = 100 \text{ nF}$   
 $C_4 = 47 \mu\text{F}, 25 \text{ V (upright)}$   
 $C_5, C_6 = 33 \text{ pF}$   
 $C_7, C_8 = 470 \text{ nF}$

### Semiconductors:

$D_1 = 1\text{N}4148$   
 $D_2 = \text{zener}, 4.7 \text{ V}, 500 \text{ mW}$   
 $D_3 = \text{LED}$   
 $T_1 = \text{BC}547$

### Integrated circuits:

$\text{IC}_1 = \text{see miscellaneous}$   
 $\text{IC}_2 = 7805$   
 $\text{IC}_3 = \text{CNY}65$

### Miscellaneous:

$K_1, K_2 = \text{two-terminal strip, pitch } 7.5 \text{ mm}$   
 $S_1 = \text{press-to-make switch}$   
 $S_2 = \text{single-pole on/off switch}$   
 $B_1 = \text{B}80\text{C}1500 \text{ rectifier}$   
 $X_1 = \text{crystal}, 32.768 \text{ kHz}$   
 $\text{Re}_1 = 12 \text{ V}, 1200 \text{ VA}, 2\text{-contact relay}$   
 $\text{Tr}_1 = \text{Mains transformer}, 9 \text{ V}, 1.5 \text{ VA secondary, e.g. Velleman } 1090018 \text{ (Maplin)}$

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[950010]

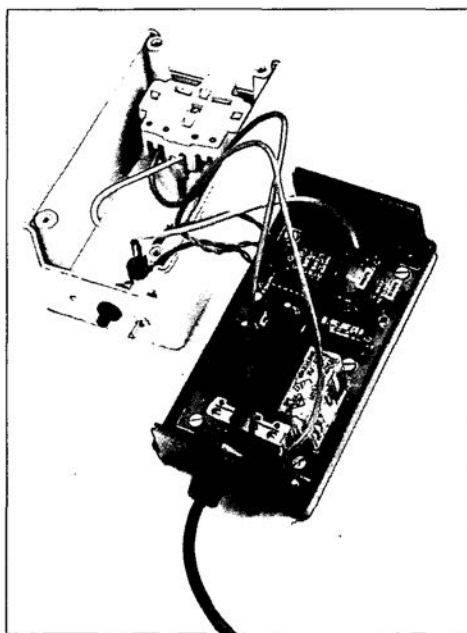
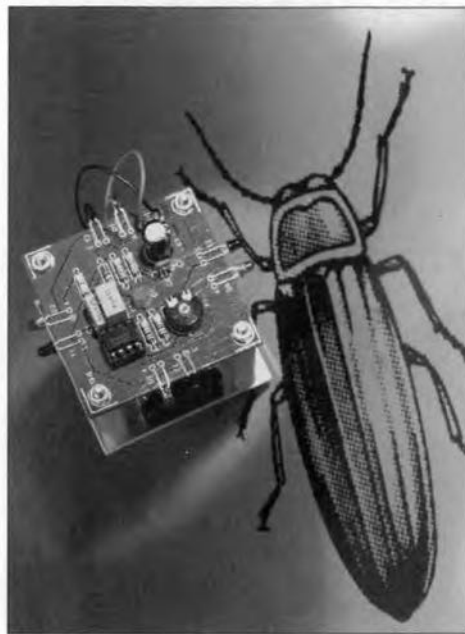


Fig. 3. Completed switch.

# ELECTRONIC FIREFLIES

The circuit described here mimics the behaviour of a firefly, but only if you build more than one. Although it may be a bit bold to speak of group dynamics and conditioned interaction, some very interesting effects can be observed in this cybernetic modelling experiment based on simple electronics. Interested? Then read on.

Design by H. Bonekamp



THE electronic firefly being an example of an artificial animal, it is, strictly speaking, also a cybernetic model with its own, characteristic, behaviour in the presence of members of its species. Since these members communicate via optical means, a group of electronic fireflies really is an opto-cybernetic model in which interactive behaviour may be observed.

Fireflies are beetles emitting phosphorescent light. If you have ever seen the beautiful light patterns produced by a swarm of fireflies, the effect is not unlike synchronous oscillation. In some people, the effect induces deep thoughts, while others are hypnotized, or, in any case, touched by such a wonder of nature.

## From biology to electronics

To be able to mimic positive phototactic behaviour of a firefly you first of all need a small, oscillator-controlled, flashing light which is clearly visible in the dark. Furthermore, some means has to be provided to control the flash rate (in other words, the oscillator frequency), and an optical output signal to be able to control a second oscillator.

The circuit diagram in **Fig. 1** shows that the above requirements are easily realized with practical electronics. The heart of the circuit is the familiar and inexpensive 555 timer. The optical sensors and emitters of the model are

realized by a set of infrared LEDs and phototransistors.

The 555 is wired as an astable multivibrator. The principle is both simple and effective. In the configuration used here, the 555 acts like a switch which closes when the d.c. voltage at the threshold input (pin 6) rises above two-thirds of the supply voltage, and opens again when it drops below one-third of the supply voltage. The threshold input is connected to a capacitor,  $C_2$ , which is charged via  $P_1$ - $R_1$ - $R_4$  as long as the 'switch' formed by the 555 is open. Any time the capacitor voltage rises above the above mentioned threshold level, the capacitor is discharged via pin 7 of the 555, and the Q output (pin 3) drops low. This is used to switch on a LED,  $D_1$ . Since the charging and discharging of  $C_2$  is repeated continuously, LED  $D_1$  flashes at a certain rhythm, and so forms the 'light' of the firefly. The flash rate is determined by  $P_1$ ,  $R_1$  and  $C_2$ , and works out at about 1 Hz. The ratio  $(P_1+R_1)/R_4$  determines the mark/space ratio, (duty factor) of the LED control signal.

So far, the circuit looks like an ordinary flashing LED. The specialty, however, is the addition of  $T_1$ - $T_4$  and  $D_2$ - $D_5$ . The latter are infrared emitting diodes (IREDs) which produce the optical transmitting signal of the firefly. The series-connected IREDs are simply connected in parallel with  $D_1$ , and emit infrared pulses in the same rhythm as the ordinary, visible light LED. The aim is, of course, that the IR pulses

are picked up by another firefly, via transistor  $T_1$ ,  $T_2$ ,  $T_3$  or  $T_4$ . When these phototransistors detect infrared light, they start to conduct, causing the voltage across  $R_5$  to drop. This voltage is used to assist in the charging of  $C_2$ , via diode  $D_6$ , causing the capacitor to be charged a little faster than normal. The result is a brief phase shift of the flashing signal, causing the next flash to occur a little later than normal.

Since the voltage across  $C_2$  never drops below one third of the supply voltage, diode  $D_6$  will not start to conduct until the voltage at the emitter of one of the phototransistors has risen to that level plus the diode's forward drop. The value of  $R_5$  therefore determines the sensitivity of the phototransistors. Because the current through the IREDs is limited by the battery capacity, the distance between the IREDs on one firefly the phototransistors on another should not be more than a few centimetres. As soon as two of these 'creatures' are placed within a small distance of each other, each of them will pick up the infrared light emitted by the other. Provided their flash frequencies are equal, their light pulses will coincide after a while.

## Printed circuit boards

The artwork of the printed circuit board designed for the electronic firefly is shown in **Fig. 2**. Building up should not present problems as there are no special components or construction methods to grapple with. Unfortunately the printed circuit board is not available ready-made through our Readers Services, so you have to make it yourself.

Since each side of the board has one IRED and one phototransistor, the firefly is capable of looking for other members of its species in four directions. Obviously, it makes no sense to build one firefly only. The fun starts at four or so of these little beasts.

All fireflies have to be adjusted for the same flash frequency. Fortunately, that can be achieved without special test instruments. However, to prevent the behaviour of the circuit being influenced, the adjustment should be made at the lowest possible ambient light intensity. The following order is recommended.

1. On one of the fireflies, turn preset  $P_1$  to the centre of its travel, and use this board as the reference.
2. Count the number of flashes in one minute.



## COMPONENTS LIST

## Resistors:

$R_1 = 1\text{M}\Omega$   
 $R_2 = 3\text{k}\Omega$   
 $R_3 = 390\Omega$   
 $R_4 = 10\text{k}\Omega$   
 $R_5 = 22\text{k}\Omega$   
 $P_1 = 500\text{k}\Omega$  preset H

## Capacitors:

$C_1 = 10\text{nF}$   
 $C_2 = 1\mu\text{F}$  MKT  
 $C_3 = 100\mu\text{F}$  16V radial  
 $C_4 = 100\text{nF}$

## Semiconductors:

$D_1 = \text{LED (green) low current}$   
 $D_2\text{--}D_5 = \text{SFH409 (Siemens)}$   
 $D_6 = 1\text{N4148}$   
 $T_1\text{--}T_4 = \text{SFH309F (Siemens)}$   
 $\text{IC}_1 = \text{TLC555}$

## Miscellaneous:

9-V PP3 battery + clip.  
 PCB not available ready-made through the Readers Services.

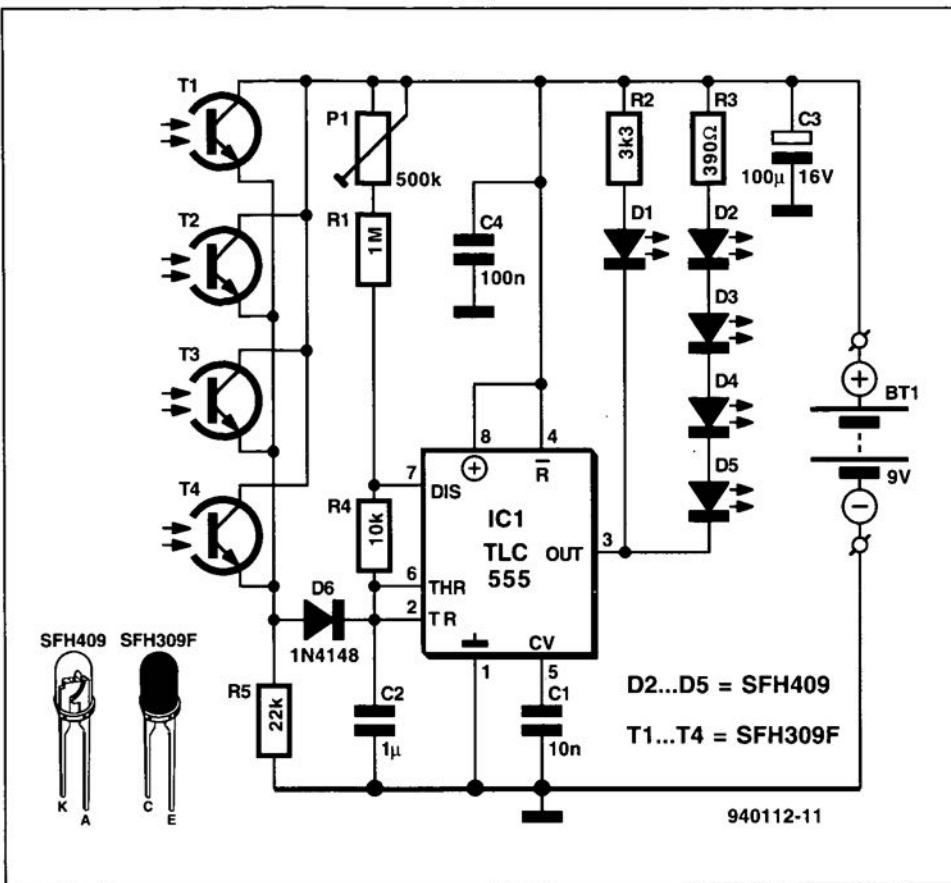


Fig. 1. Circuit diagram of the electronic firefly. This little beast has optical senses.

- Put the reference board away ('out of sight' of the others), and fetch the second board.
- On this board also, set  $P_1$  to the centre of its travel. Next, count the number of flashes in one minute.
- If the number of flashes is greater than that produced by the reference board, turn  $P_1$  anti-clockwise. If the

number of flashes is smaller, turn  $P_1$  clockwise.

- Count the number of flashes per minute again, and adjust  $P_1$  until the frequency is less than or equal to two pulses with respect to the reference. This adjustment is sufficiently accurate for the present purpose.

The other boards are adjusted in the same way. Although this may seem tedious and time-consuming, in practice the correct setting of  $P_1$  is rapidly found.

Next, you can start thinking about a practical and attractive enclosure for the fireflies. Almost anything may be used, provided the view of the photo-

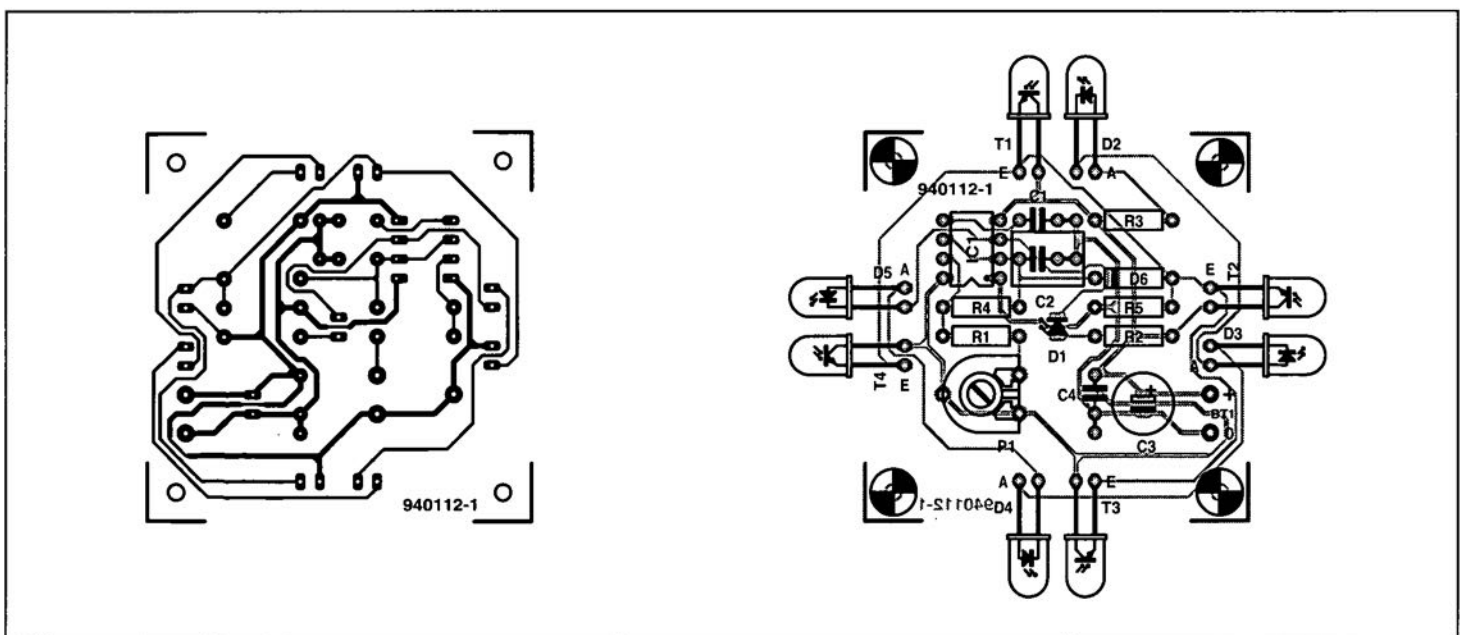


Fig. 2. The PCB design allows the firefly to communicate with other members of its species via all four sides of the board.

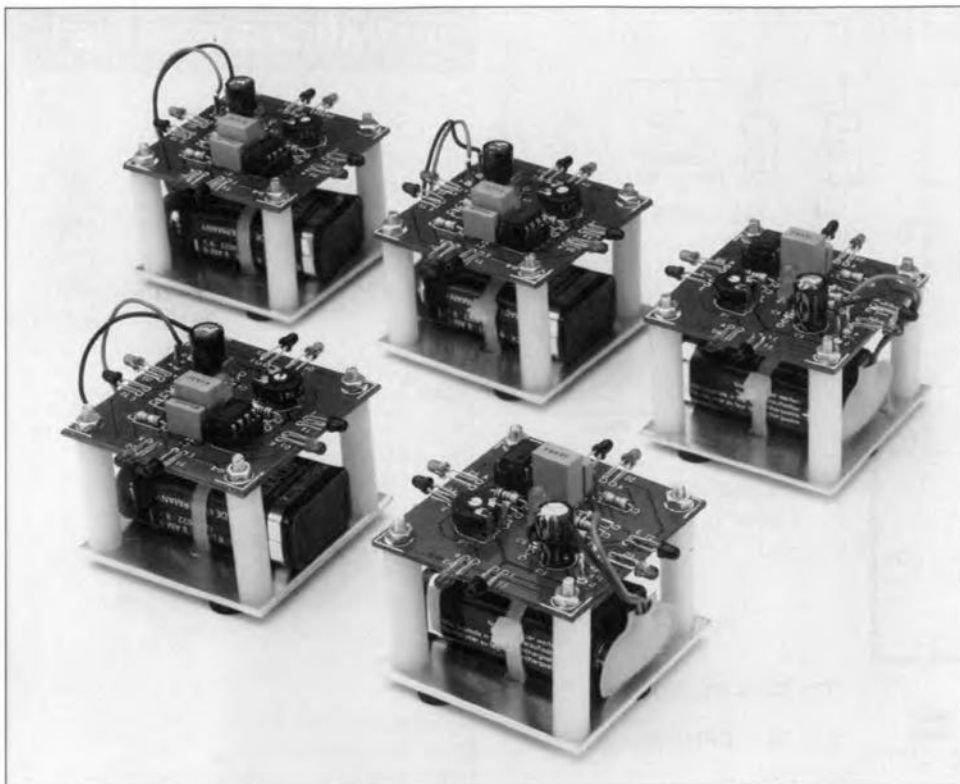


Fig. 3. The fun starts when you build a number of fireflies.

transistors and IREDS is not blocked. As illustrated by the introductory photograph, the prototypes were not mounted in cases at all. Each board was fitted on an aluminium base plate with the aid of four PCB spacers. The base plate serves to hold the 9-V battery, which is held in place by a plastic cable tie. This leaves the fireflies entirely mobile.

## Experiments

When all boards are adjusted as described earlier, it is time to do some experimenting to see if synchronous light effects actually occur. A good impression of the typical behaviour of the circuit, and the optimum distance, is obtained by starting with two fireflies. Although it is not necessary to do the experiment in absolute darkness, ambient light should be kept to a minimum.

Switch on two fireflies, and place them at a distance of about 10 cm. In the rare case of the two already flashing in unison, keep them out of each other's sight for a couple of minutes, and then slowly move them towards each other, ensuring that the optical parts on the boards can see each other. Carefully watch the flashing of the two fireflies. At a certain instant, you will note a steady synchronization between the two flashers.

After moving the fireflies around on the table for a while, it will be noticed that the distance for the quickest syn-

chronization is about three centimetres. When the distance is smaller, the LEDs will remain on all the time.

Next, put a third firefly on the tabletop. Notice that the synchronization of the first two may be disrupted by the third if it is slowly moved into their sight. Here, too, the flashing changes to steady 'on' if the distance between the fireflies becomes too small.

Introducing a fourth member into the group allows a square configuration to be made, which causes a loop in which a kind of positive feedback effect occurs. Here, the distance between the fireflies becomes even more critical than with three members.

In the 'square' arrangement, it is best to start with a distance of about 4 cm between the boards. Next, move them closer a millimetre at a time. If the LEDs light continuously after a while, the distance has to be increased again. If the LEDs do not start to flash again, the 'lock up' situation can be cancelled by inserting a piece of cardboard between two fireflies, which interrupts their optical link. If the lock-up effect occurs again after a while, the distance has to be increased a little again, and the trick with the cardboard is repeated. With a little patience, quite interesting synchronization patterns may be obtained with four fireflies. During some experiments with prototypes, it appeared that heat (IR) radiation emanating from persons close by the fireflies sometimes had an effect on a synchronization pattern.

## FIREFLIES

A firefly is not a fly, but a kind of beetle which is so named because of its ability to emit phosphorescent light. Both males and females have a unique light emitting organ at the rear end of their body. This organ consists of different layers of which the inner one functions as a reflector. The actual production of visible light is caused by a chemical reaction of two substances which are made by the insects themselves. The reaction is started by stimuli from the nervous system.

In general, it is assumed that the light serves to attract members of the opposite sex. The females (who can not fly) usually attach themselves to the top of grass blades, and turn the rear end of their body towards males flying over them. They respond to light signals emitted by an attractive male by boosting their own light intensity. To be able to detect these signals emitted by the females, the males have large hemispheric shaped eyes.

## Finally

To complete the story, a few figures. The flash rate is set to about 1 Hz. The current consumption of the circuit is about 14 mA, of which 2 mA goes to  $D_1$ , and 10 mA to the four IREDS.

If you want to increase the range of these creatures, consider increasing the current through the IREDS. This is best done by lowering the value of  $R_3$ . Note, however, that the minimum value is about 56  $\Omega$ . At this value, the IREDS pass a current of about 100 mA, which will considerably shorten the battery life.

(940112)

# MOCK CAR ALARM

Although it has no detector or alarm actuation device of any kind, the present circuit may still function as a deterrent against car thieves. Actually, a vigilantly flashing LED in your car simulates an armed car alarm which is not there at all.

Design by L. Lemmens

IN this day and age any car owner should be painfully aware that his or her trusted vehicle can be broken into or stolen at almost any time and place. Car burglary and car theft is such a massive problem that it seems to grow beyond the capacity of the police. Not surprisingly, certain cars have to be fitted with an approved alarm system before they can be insured at all. In the car shops, too, shelves are loaded with anti-theft radios, wheel locks, gear lever locks and a wide range of electronic car alarms.

Most locks and clamps are brightly coloured, while the alarm systems usually come with a flashing LED, and a set of bright stickers for fitting on the car windows, warning potential thieves that the car is fitted with an alarm. However, since there is no way of telling whether or not an alarm is actually fitted or not, it is also possible to mount just a flashing LED, which hopefully acts as a deterrent.

## A comparator

In principle, such a mock car alarm consists of only two parts: a flashing LED and a series resistor of about 150  $\Omega$ . Most of you will know perfectly well how to connect and install such a

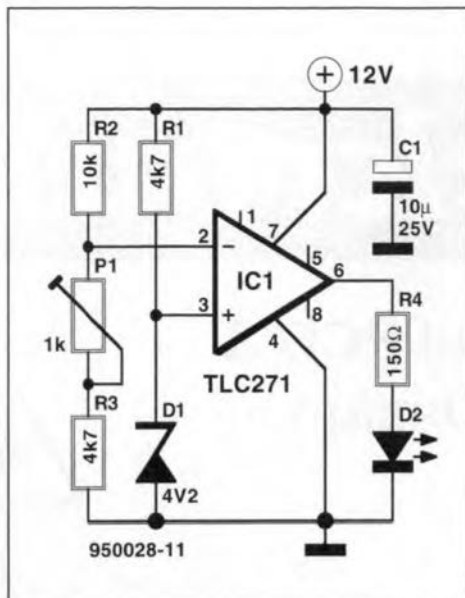


Fig. 1. Circuit diagram of the mock car alarm. No need to switch the flashing LED on and off any time you enter or leave the car, that is done automatically for you by a comparator which monitors the car battery voltage.

mock indicator. The disadvantage of this super-simple solution is that the LED will flash all the time, and that can be dangerous while you drive the car because it has a distracting effect. Obviously, it is possible to add a switch to turn the LED on and off, but that is cumbersome. Ideally, the LED should be on only when the car is parked, and off when it is driven. How that can be achieved without tampering with the car's electrical wiring system is discussed below.

The switching on and off of the flashing LED is controlled by an accurate comparator which measures the car battery voltage. When the engine is running, this voltage will be of the order of 14 V. When the engine is switched off, the battery voltage drops to a value between 12 V and 12.5 V. With the comparator's threshold level set to a value just under 13 V, the LED is switched off automatically when the engine is started, and on, when the engine is switched off.

With reference to the circuit diagram in Fig. 1, opamp IC<sub>1</sub> is wired as a comparator which compares the two voltages applied to its inputs. The comparator output is high (and the LED is switched on) when the voltage at the +input is higher than that at the -input. The voltage at the +input is fixed at +4.2 V with the aid of zener diode D<sub>1</sub> and resistor R<sub>1</sub>. These parts

make the reference level is independent of the car battery voltage. The -input of IC<sub>1</sub> is tied to the junction of an adjustable voltage divider. The voltage at this junction varies along with the battery voltage, and may be set to a value between 3.8 V and 4.4 V when the battery voltage is 12 V, and between 4.5 V and 5.1 V when it is about 14 V.

Preset P<sub>1</sub> is used to adjust the voltage at the -input to a level just under the reference of 4.2 V, when the engine is switched off. The LED then starts to flash, but it will go out the instant the engine runs, because then the -input of the comparator rises above the threshold of 4.2 V, and the comparator output drops from high to low.

## Construction

A printed circuit board is really not needed for such a simple project with so few parts. The circuit is easily built on a piece of veroboard or stripboard, or, even simpler, as a 'flying wire' construction. The latter option may be the smartest because it allows the shape to be matched to the enclosure used. For this, a plug for the cigarette lighter socket in the dashboard is suitable. The flashing LED then protrudes from the cable opening in the plug. Although the plug is a convenient and low-cost solution, it is rather conspicuous as a mock alarm, and will almost certainly fail to deter experienced car thieves. If you want to make the warning device look as authentic as possible, it may be better to fit it in a small box, or in the dashboard.

Finally, Fig. 2 shows a prototype, while the other photograph on this page illustrates how the project may be finished neatly. (950028)

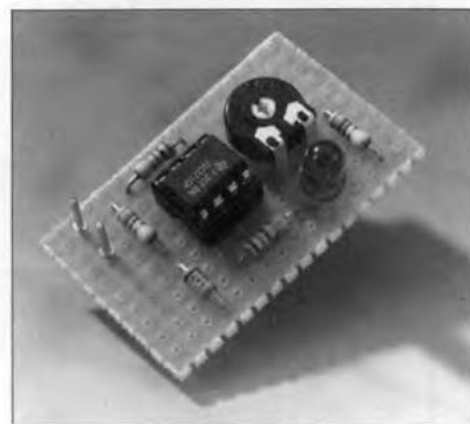


Fig. 2. A simple circuit like this is easily built on a small piece of stripboard.

