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TRANSFORMERS

AUDIO & HI-FI • COMPUTERS & MICROPROCESSORS • DESIGN IDEAS • RADIO, TELEVISION & COMMUNICATIONS • SCIENCE & TECHNOLOGY • TEST & MEASUREMENT

IN-CAR AUDIO AMPLIFIER

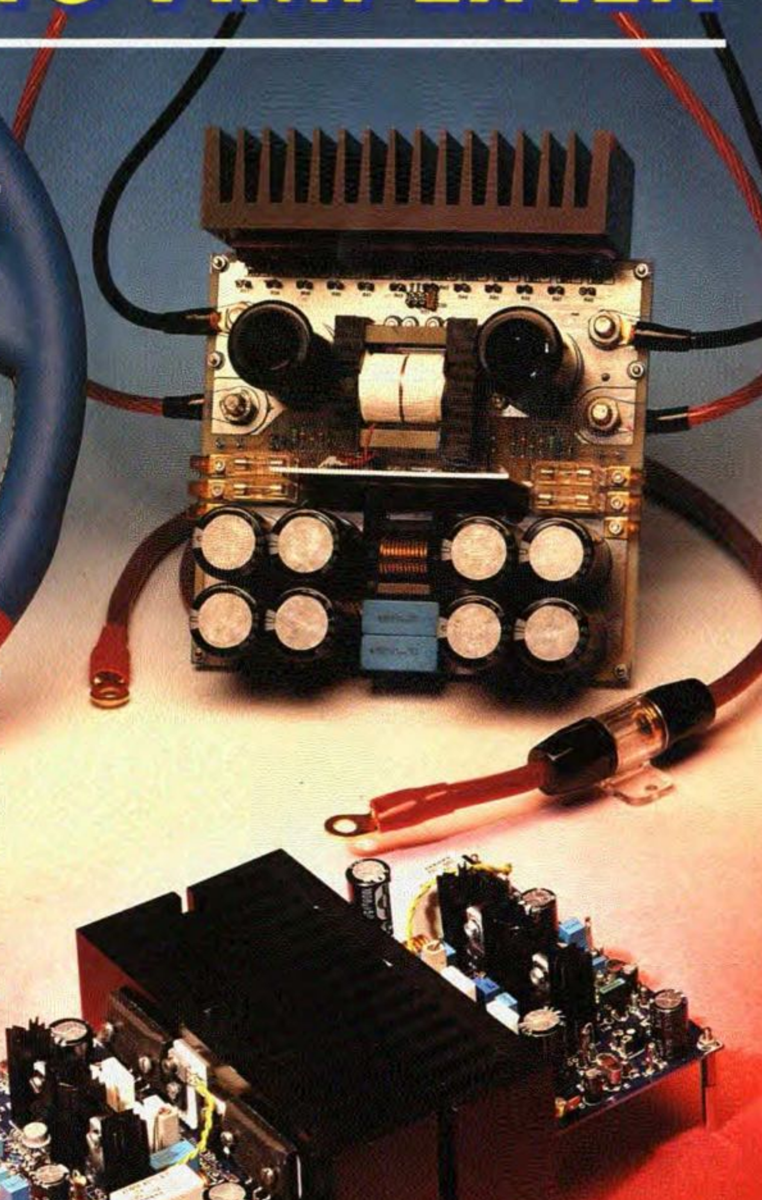
TV line monitor

Stable DC-DC converter

Computer PSU monitor

Infra-red remote-control tester

Voice scrambler



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MOTIVE-BATTERY CHARGER

Design by L. Lemmens

The battery charger is intended primarily for charging, and keeping charged, without supervision, lead-acid batteries of cars and motorcycles that are laid up for lengthy periods, for instance, during the winter.

If a verhicle is laid up for a lengthy period, it is advisable to keep its (lead-acid) battery charged properly during this period as this will extend its life considerably compared to leaving it just in the vehicle and charging it when the vehicle is needed again. Unfortunately, the bulk of vehicle battery chargers is not suitable for unsupervised, continuous charging for long periods.

Self discharge

Even when a lead-acid battery is not in use, its internal chemical action does not stop. Owing to small impurities in the acid, there are always tiny current loops in action, causing self discharge. In new batteries, this does not amount to much, just a few tenths of a per cent per day. Some self discharge also results from the electrochemical reaction between the lead dioxide of the positive plate lattices and the lead alloy of the grid. This is a form of corrosion, which in a fully charged battery is negligible, but can take on alarming dimensions in a neglected (discharged) battery. If the battery becomes totally discharged, the damage may be irreversible. This is because the lead sulphate formed in the plates during the discharge changes in structure: relatively large crystals of lead sulphate are formed which block the lattices in the plates. Both the negative and the positive plates become entirely sulphated and, as they are now composed of identical material, the terminal voltage collapses. The battery is then a write-off.

Charging during layoffs

There is only one way of preventing a battery being destroyed through self-discharge and that is to keep it regularly charged. However, this should be done in an intelligent way, because overcharging a lead-acid battery is just as bad for it as a complete discharge. This means that a charger is required that does not just charge the battery, but also continuously monitors its condition and acts accordingly. Most commercial lead-acid battery chargers have no such facility and are thus totally unsuitable for keeping a battery charged unsupervised.

Charging current & voltage

The state of charge of a lead-acid battery is reflected by its cell voltage. Normally, this is 2 V. However, accurate measurements show that this voltage seldom has its nominal value. The cell voltage of a partly charged battery not in use is 1.9–2.0 V, that of a fully charged battery is 2.05–2.1 V. The charging voltage should be slightly higher, because during charging the cell voltage rises. In general, a battery is fully charged when its cell voltage has risen to 2.2–2.3 V (that is, 13.2–13.8 for a 12 V battery). When the cell voltage reaches 2.35–2.4 V, there is a sharp rise in voltage. Most of the charge is then used in dissociating the water of the sulphuric acid solution into hydrogen and oxygen and the cell begins to gas freely. It is thus advisable to treat 2.4 V as the upper limit of the cell voltage during charging.

There are three different ways of charging a battery: normal (the most common), fast and trickle.

The charging current during normal charging is one tenth to one twentieth of the nominal battery capacity in ampere-hours (Ah). Thus, a 20 Ah battery should be charged with a current of 1–2 A.

Fast charging takes place with a current that is three to five times larger than that used during normal charging. The condition of the battery needs constant monitoring, because the risk of overcharging is high. It is, in any case, advisable to use fast charging only in exceptional cases. Repeated fast charging reduces the useful life of the battery.

Trickle charging is not intended to charge a battery, but rather to keep it in good working condition by countering the effects of self discharge. The charging voltage should not be higher than 2.2 V per cell and the charging current may be limited to $^{1}/_{1000}$ to $^{1}/_{2000}$ of the battery capacity.

Which charging method?

It is clear that for the present battery charger fast charging is not a method worth considering. Strictly speaking, trickle charging should do the trick. With proper design, a trickle charger could be left charging the battery for a whole year. Unfortunately, a trickle charger requires that from the onset the battery is fully charged. If the battery is partly discharged when it is laid up, a trickle charger would not be able to charge it in a year.

Therefore, the present charger uses a combination of normal charging and trickle charging. It is, in fact, a standard charger provided with voltage and current monitoring facilities. The charging current is 0.5 A; it can not rise above that level because of the internal protection circuits.

Since the charger also contains preset voltage limiting, the cell voltage of the battery on charge can not exceed a certain level. When, for instance, the preset voltage of 2.2 V is exceeded, the charging current is interrupted. When

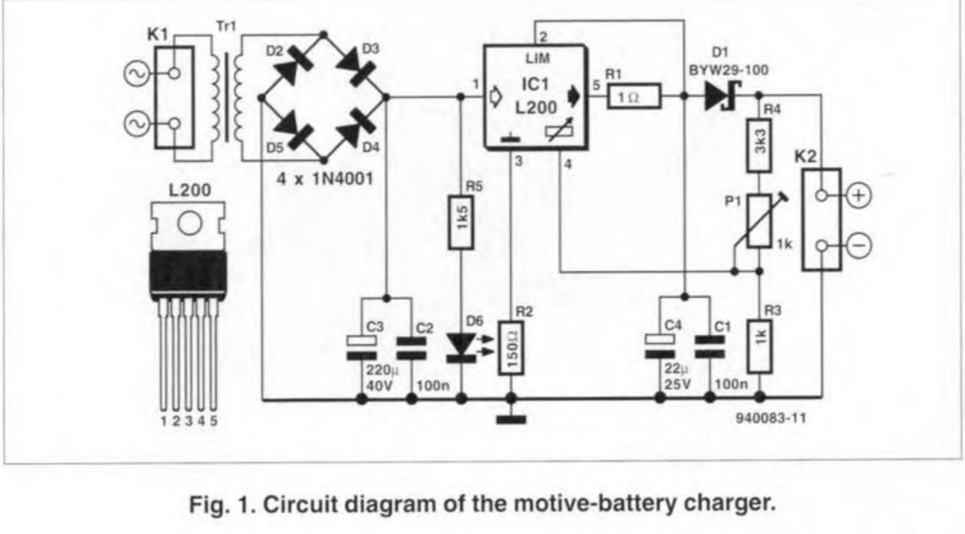


Fig. 1. Circuit diagram of the motive-battery charger.

after a while the voltage has dropped below 2.2 V, the charging current is switched on again.

Circuit description

The mains voltage enters via K_1 (see **Fig. 1**) and the output (charging) voltage is available at K_2. The mains voltage from K_1 is applied to a bridge rectifier, D_2–D_5, via transformer Tr_1. Diode D_6 serves as on/off indicator; C_3 is a buffer capacitor, and C_2 decouples any r.f. noise voltage.

The heart of the circuit is a Type L200, IC_1, from SGS Thomson. It is a programmable voltage and current regulator, housed in a five-pin case, which is reputed to be virtually indestructible. It can handle input voltages up to 40 V, with peaks up to 60 V, provides a current of up to 1.8 A, and is furnished with reliable thermal and short-circuit protection.

The L200 is a general-purpose chip, which in the present circuit is used as a current source that is switched off if the output (that is, charging) voltage exceeds a certain value. This is done by comparing this voltage continuously with the 2.77 V reference potential at pin 4. The switch-off value is set with P_1.

The peak output (charging) current is set by R_1. When the current limiting is actuated, the voltage across R_1, according to the manufacturer, is about 0.45 V, which gives a charging current of 450 mA.

Schottky diode D_1 prevents the battery discharging through IC_1 if there is a mains failure. In that case, the current is limited to that through R_3, R_4 and P_1, which amounts to only 3.5 mA.

Resistor R_2 protects IC_1 against the battery being connected with incorrect polarity. This is, however, only a short-term protection; if the battery remains connected with incorrect polarity, both IC_1 and C_4 will give up the ghost.

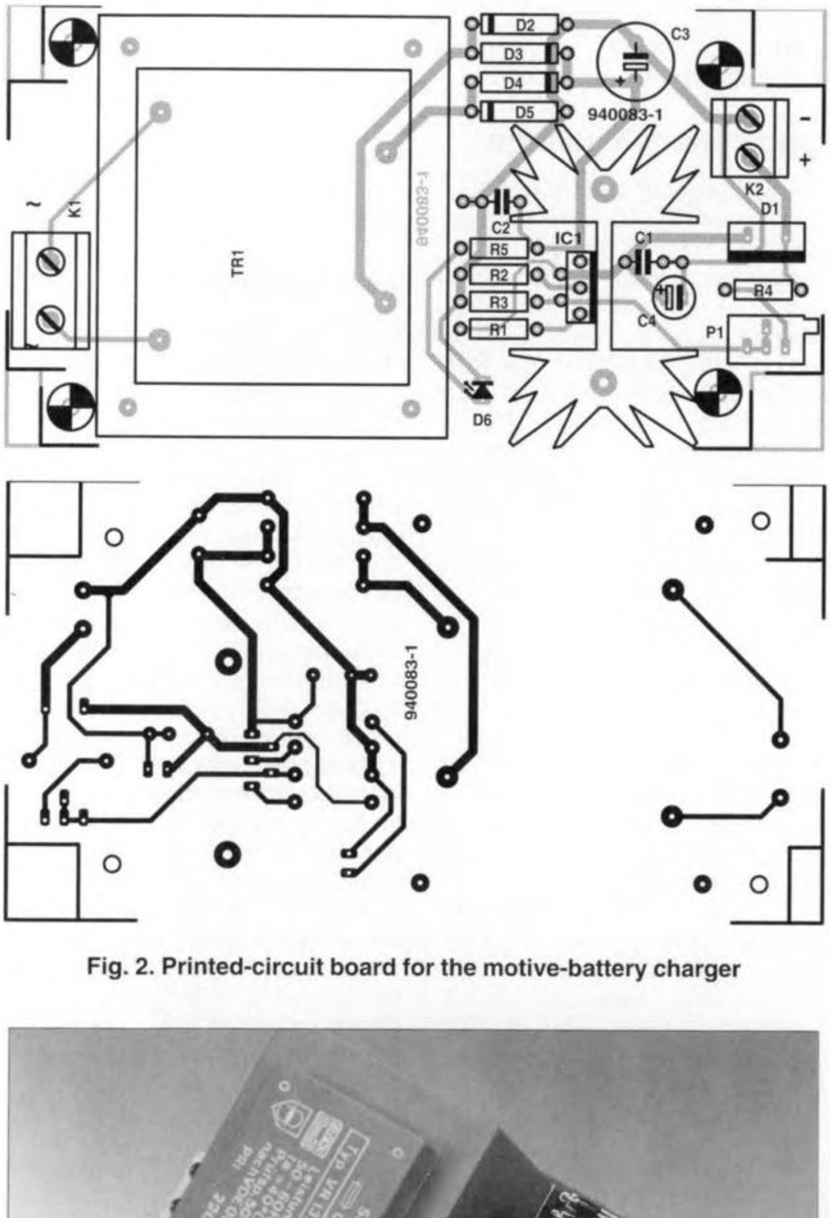


Fig. 2. Printed-circuit board for the motive-battery charger

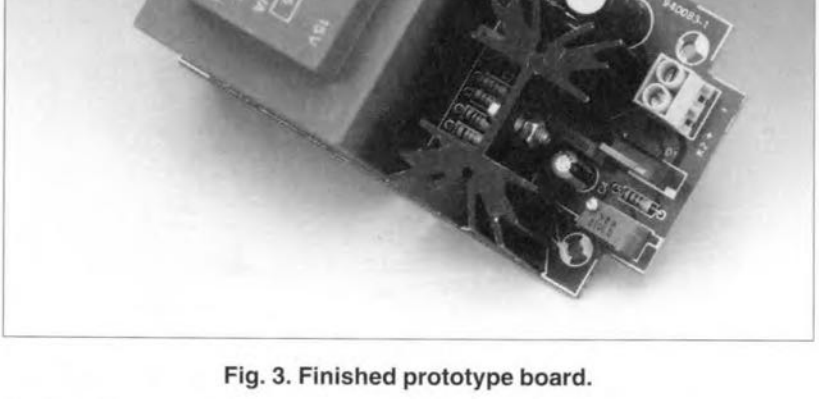


Fig. 3. Finished prototype board.

Construction

The entire circuit, including the mains transformer, is intended to be built on the printed-circuit board in **Fig. 2**. Finishing the board is straightforward.

Note that a large space has been reserved on the board for a heat sink for IC_1, because this chip will dissipate about 3 W. The IC must be electrically insulated from the heat sink with a ceramic washer and heat transfer paste.

When the board has been finished (see **Fig. 3**), it should be fitted in a well-insulated synthetic fibre case.

Alignment

To set P_1 to the required voltage limits, a 12V battery and two multimeters are needed—see **Fig. 4**.

- Connect the charger to the mains and switch it on.
- Connect the battery to the output of the charger, with one of the multimeters (set to 1A d.c. range) in series with the + output terminal.
- Connect the other multimeter (set to 25 V range) across the output of the charger.
- Adjust P_1 for maximum output voltage.
- The battery is now being charged; observe the charging voltage.
- When the charging voltage reaches the desired maximum value, say, 13.5 V, slowly turn P_1 back until the charging current is zero.

If a laboratory power supply unit (PSU) is available, it may be used to simulate a battery by connecting a 27 Ω, 5 W resistor across its output terminals. Set the PSU output to 13.5 V, connect it to the output of the charger and adjust P_1 till the current just drops to zero.

In a rare case, it may happen that the required voltage limits can not be set with P_1. This may be because the internal reference potential of the IC is slightly too high. This may be remedied by lowering the value of R_4 slightly (to, say, 2.2 kΩ).

Finally

Diode D_6 may be fitted outside the enclosure and be connected to the board via two lengths of flexible, insulated circuit wire.

Use flexible, insulated wire of dia. ≥0.75 mm for the connections between the battery and K_2. Use red wire for the +ve line and green or black wire for the –ve line. Suitable clamps can be obtained from car parts dealers or good hardware shops.

When disconnecting the battery, always take off the negative cable first and then the positive one. When connecting the battery, put on the positive cable first and then the negative one. These precautions will prevent a short circuit of the battery if the positive cable terminal accidentally touches the frame of the car or motorcycle.

Parts list

Resistors:
R_1 = 1 Ω
R_2 = 150 Ω
R_3 = 1 kΩ
R_4 = 2.2 kΩ – see text
R_5 = 1.5 kΩ
P_1 = 1 kΩ multiturn preset

Capacitors:
C_1, C_2 = 100 nF
C_3 = 220 µF, 40 V, radial
C_4 = 22 µF, 25 V, radial

Semiconductors:
D_1 = BYW29-100
D_2–D_5 = 1N4001
D_6 = LED, red, 5 mm

Integrated circuits:
IC_1 = L200CV (5-pin)

Miscellaneous:
K_1 = 2-way terminal block, pitch 7.5mm
K_2 = 2-way terminal block, pitch 5 mm
Tr_1 = short-circuit-proof mains transformer, 15 V, 13 VA
Enclosure, synthetic fibre 120×65×65 mm ($4^3/_4$×$2^1/_2$×$2^1/_2$ in)
Heat sink 5 K W^{-1}, complete with fitting/insulating kit
PCB Ref. 940083

[940083]

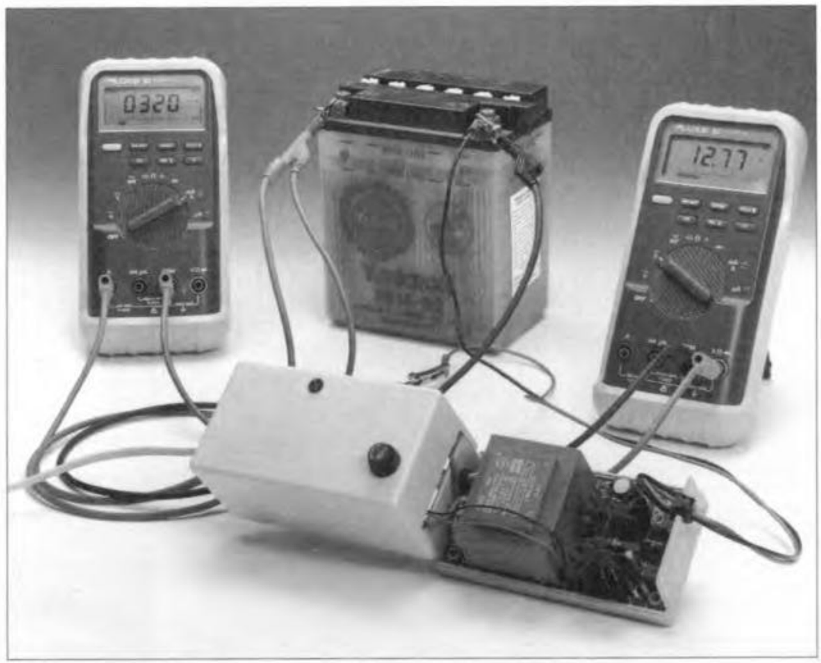
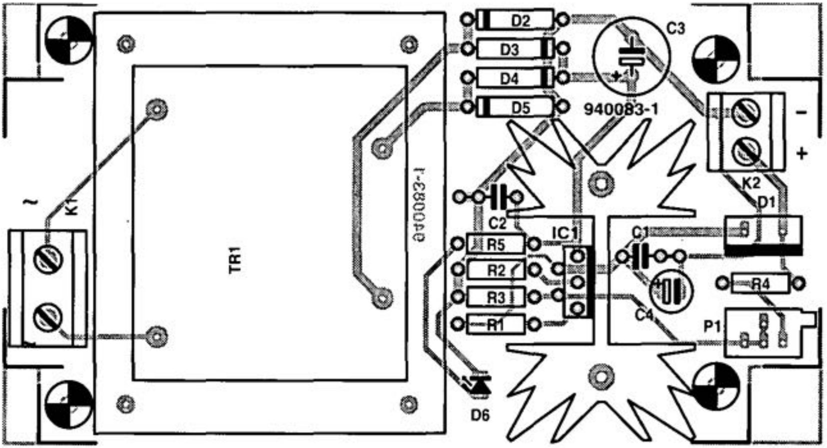


Fig. 4. During alignment, both voltage and current must be monitored.


D2
D3
D4
D5
C3
940083-1
-
+
K2
D1
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D6
TR1
K1
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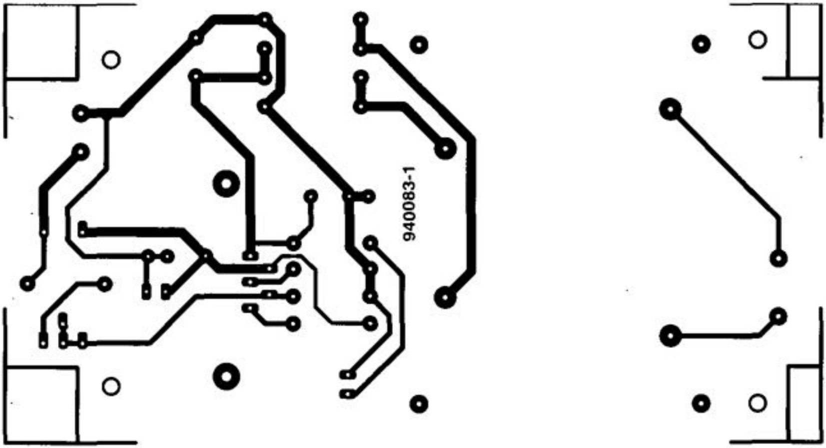
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INTEGRATED A.F. AMPLIFIER - PART 2

Design by T. Giesberts

Construction

The preamplifier section is intended to be built on the printed-circuit board shown in **Fig. 4**. Since the various connectors and controls (except S_1 and S_2) are mounted directly on to the board, the completion of the board should not present any difficulties. Take care, however, not to overlook any of the wire bridges, which should be soldered in place first. Circuits IC_5 and IC_6 are intended to be fitted on a common heat sink, with insulating washers between the chips and the heat sink. The completed board is shown in **Fig. 6**.

The output amplifier is best built on the printed-circuit board shown in **Fig. 7**. Two of these boards are, of course, needed for a stereo version. As usual, start populating the board by soldering the wire bridges and small components in place. Pay particular attention to the polarity of C_{11} and C_{13}. It is advisable to solder R_{19} and R_{20} slightly off the board: this helps the cooling of these components. Use heavy-duty solder pins for all external connections to reduce the resistance to a minimum (remember that very high currents flow).

Mount T_5, T_6 and T_7 on a common heat sink with a thermal rating of 0.6° W^{-1}. Insulate the transistors from one another and from the heat

Main parameters

Sensitivity (all inputs)	300 mV
Signal-to-noise ratio (input short-circuited)	100 dB (1 W into 8 Ω)
(input open-circuited)	80 dB (1 W into 8 Ω)
Input impedance (all inputs)	47 kΩ
Slew rate	100 V μs^{-1}
Line output impedance	100 Ω
Line output	1 V into 100 Ω
Tape output impedance	1 kΩ
Tape output	300 mV into 1 kΩ
Bandwidth (80 W into 4 Ω)	10 Hz – 70 kHz
Harmonic distortion (45 W into 8 Ω at 1 kHz)	0.1%
(85 W into 4 Ω at 1 kHz)	0.2%
Maximum output power	85 W into 4 Ω
	45 W into 8 Ω

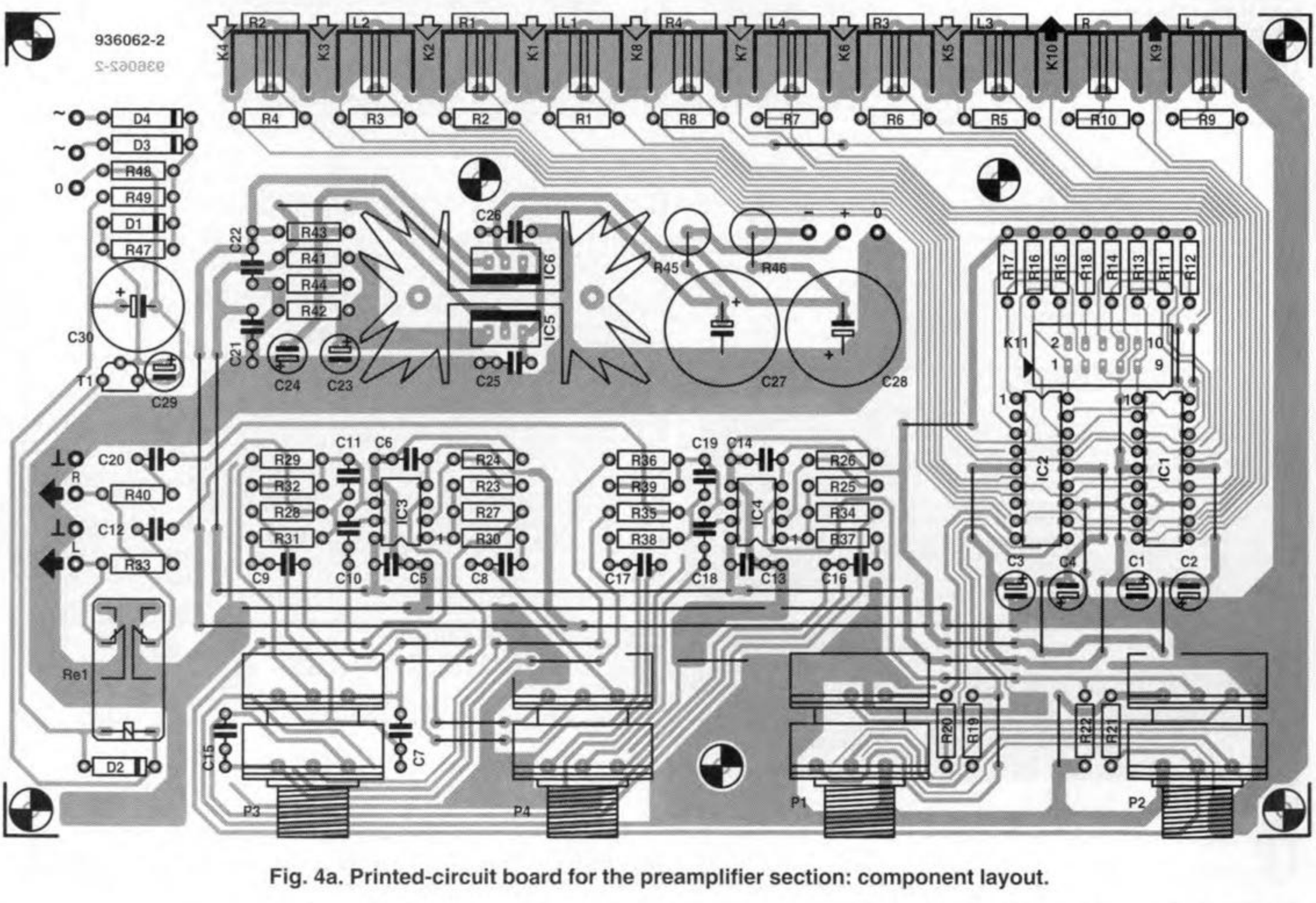


Fig. 4a. Printed-circuit board for the preamplifier section: component layout.

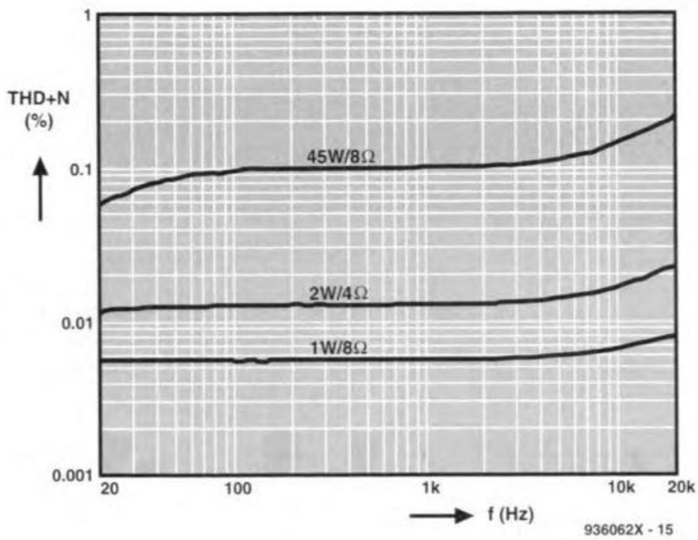


Fig. 5. Distortion plus noise vs frequency characteristic.

sink with ceramic washers (do not use mica or silicon types) and heat transfer paste.

Assembly

Fit he amplifiers and power supply in a standard 19 in. instrument case as shown in **Fig. 11**; the wiring diagram is shown in **Fig. 8**.

Fit the four 10 000 μF capacitors and the eight 0.1 Ω, 5 W, resistors (power supply), and the series resistor for the on-off LED, on a separate piece of prototyping board.

Fix all the boards on insulated spacers to the bottom of the case.

Use insulated wire of at least 1.5 mm^2 diameter for the connections in the power suply and also for the power lines.

Link box header K_{11} to S_1 and S_2 with flatcable (see **Fig. 1**, Part 1).

Calibration

Set P_1 and P_2 on the output amplifier board to the centre of their travel. Short-circuit the input of the output amplifier and switch on the supply voltage. Connect a good-quality millivoltmeter across R_{19} and R_{20} in turn and adjust P_2 for a meter reading of 22 mV. The quiescent current is then around 100 mA. Next, adjust P_1 for an amplifier output of 0 V (or very nearly so). If that can not be achieved, replace T_2 by another transistor which makes it possible.

Parts list

PREAMPLIFIER: Fig. 1 and Fig. 4

Resistors:

R_1–R_8 = 47 kΩ
R_9, R_{10} = 1 kΩ
R_{11}–R_{18}, R_{29}, R_{36} = 10 kΩ
R_{19}, R_{20} = 2.2 kΩ
R_{21}, R_{22}, R_{32}, R_{39} = 1 MΩ
R_{23}, R_{25} = 4.22 kΩ, 1%
R_{24}, R_{26} = 1.0 kΩ, 1%
R_{27}, R_{28}, R_{34}, R_{35} = 2.7 kΩ
R_{30}, R_{31}, R_{37}, R_{38} = 1.8 kΩ
R_{33}, R_{40} = 100 Ω
R_{41}, R_{43} = 1.24 kΩ, 1%
R_{42}, R_{44} = 10.7 kΩ, 1%
R_{45}, R_{46} = 220 Ω, 5 W
R_{47} = 22 MΩ
R_{48} = 4.7 kΩ
R_{49} = 180 Ω
P_1, P_3, P_4 = 10 kΩ, linear, stereo

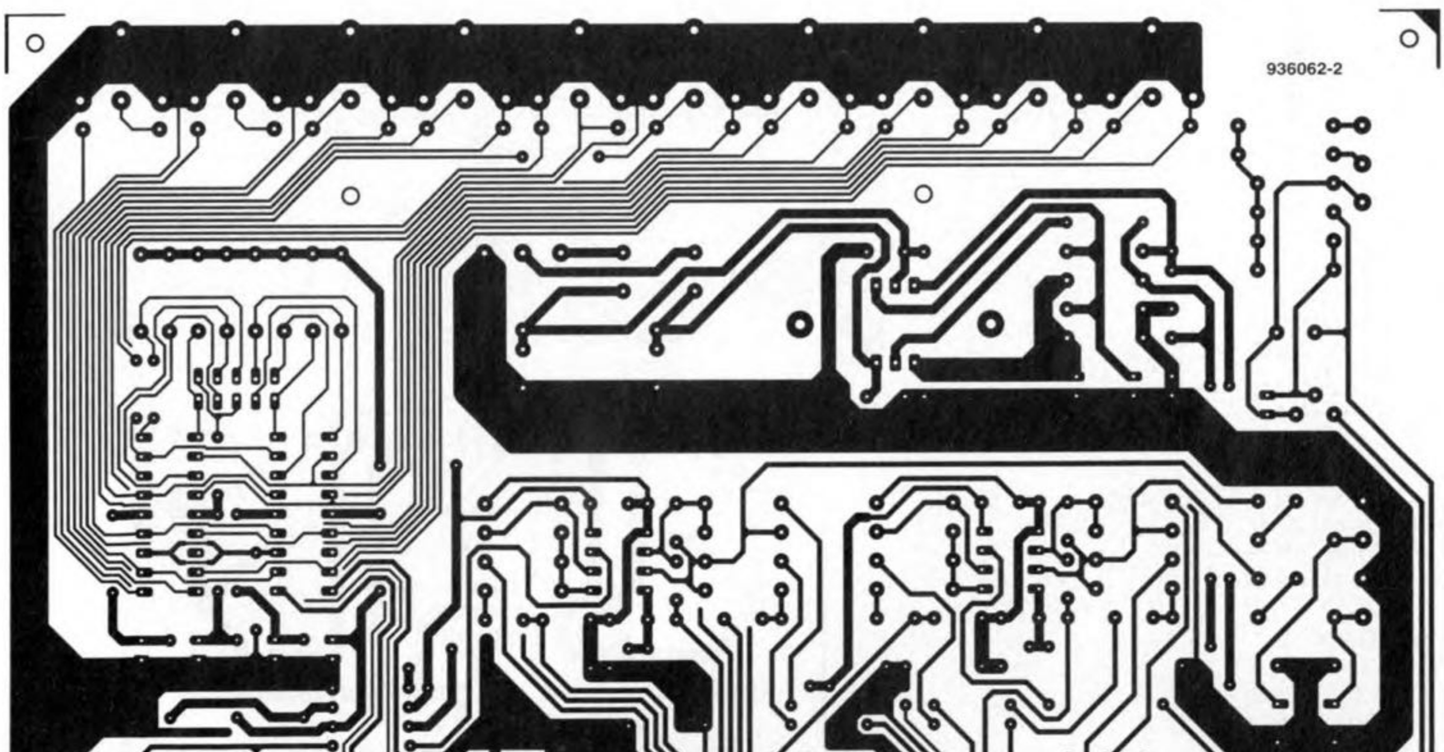


Fig. 4b. Printed-circuit for the preamplifier section: track layout.

P_2 = 10 kΩ, logarithmic, stereo

Capacitors:
C_1–C_4 = 10 μF, 63 V, radial
C_5, C_6, C_{13}, C_{14}, C_{21}, C_{22}, C_{25}, C_{26} = 100 nF
C_7, C_{15} = 180 nF
C_8, C_9, C_{16}, C_{17} = 68 nF
C_{10}, C_{18} = 3.9 nF
C_{11}, C_{19} = 47 pF
C_{12}, C_{20} = 2.2 μF, 50 V, polythene
C_{23}, C_{24} = 22 μF, 25 V, radial
C_{27}, C_{28} = 220 μF, 40 V, radial
C_{29} = 2.2 μF, 63 V, radial
C_{30} = 100 μF, 40 V, radial

Semiconductors:
D_1, D_2 = 1N4148
D_3, D_4 = 1N4003
T_1 = BC517

Integrated circuits:
IC_1, IC_2 = LM1037
IC_3, IC_4 = NE5532
IC_5 = LM317
IC_6 = LM337

Miscellaneous:
K_1–K_{10} = audio socket for PCB mounting
K_{11} = 10-way male box header and female counterpart
S_1, S_2 = 1-pole, 12-position rotary switch
Re_1 = 2-contact change-over relay for PCB mounting
Heat sink (IC_5; IC_6) 4° W^{-1}
Insulating mounting kit for IC_5, IC_6
30 cm (12 in) 10-core flatcable
4 off extension spindle for P_1–P_4
PCB Ref. 936062-2

OUTPUT AMPLIFIER: Fig. 2 and 7

Resistors:
R_1, R_{17} = 1 kΩ
R_2 = 100 kΩ
R_3 = 2.7 kΩ
R_4 = 150 Ω
R_5, R_6 = 470 kΩ
R_7–R_{10} = 2.2 MΩ
R_{11} = 4.7 kΩ
R_{12} = 5.6 kΩ
R_{13}, R_{14} = 560 Ω
R_{15}, R_{16} = 47 Ω
R_{18} = 220 Ω
R_{19}, R_{20} = 0.22 Ω, 5 W
P_1 = 2.5 kΩ preset
P_2 = 250 Ω preset

Capacitors:
C_1 = 1 nF
C_2, C_3, C_9 = 1 μF
C_4 = 100 μF, 10 V, bipolar
C_5, C_6 = 150 nF
C_7, C_8 = 100 pF
C_{10}, C_{12} = 680 nF
C_{11}, C_{13} = 10 000 μF, 40 V, radial

Semiconductors:
T_1 = BC550C
T_2 = BC560C
T_3 = BC640
T_4 = BC639
T_5 = BD139
T_6 = BDV65B
T_7 = BDV64B

Miscellaneous:
Heat sink (T_5–T_7), 0.6 °C W^{-1} (160×75 mm)
Mounting insulating kits for T_5–T_7
PCB Ref. 936062-1

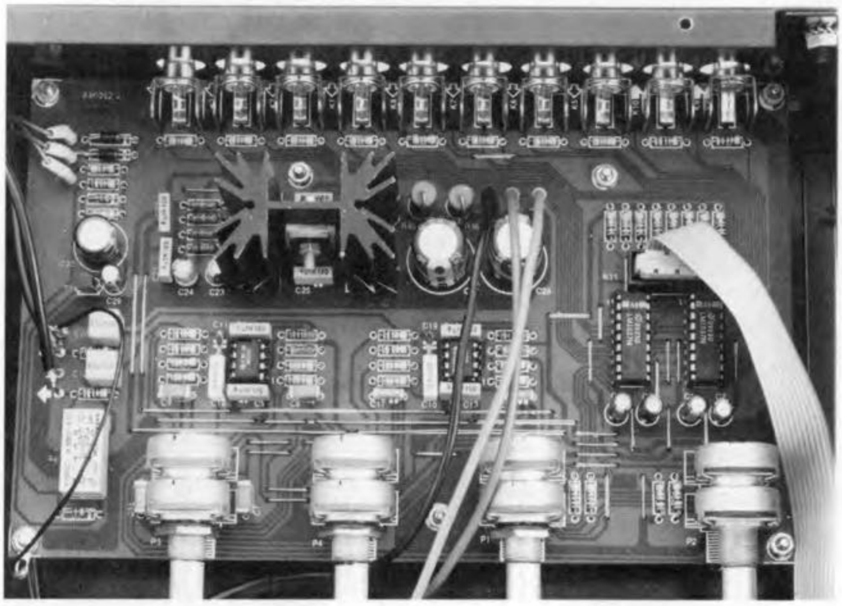


Fig. 6. Completed printed-circuit board for the preamplifier. The potentiometers are fitted with extension spindles.

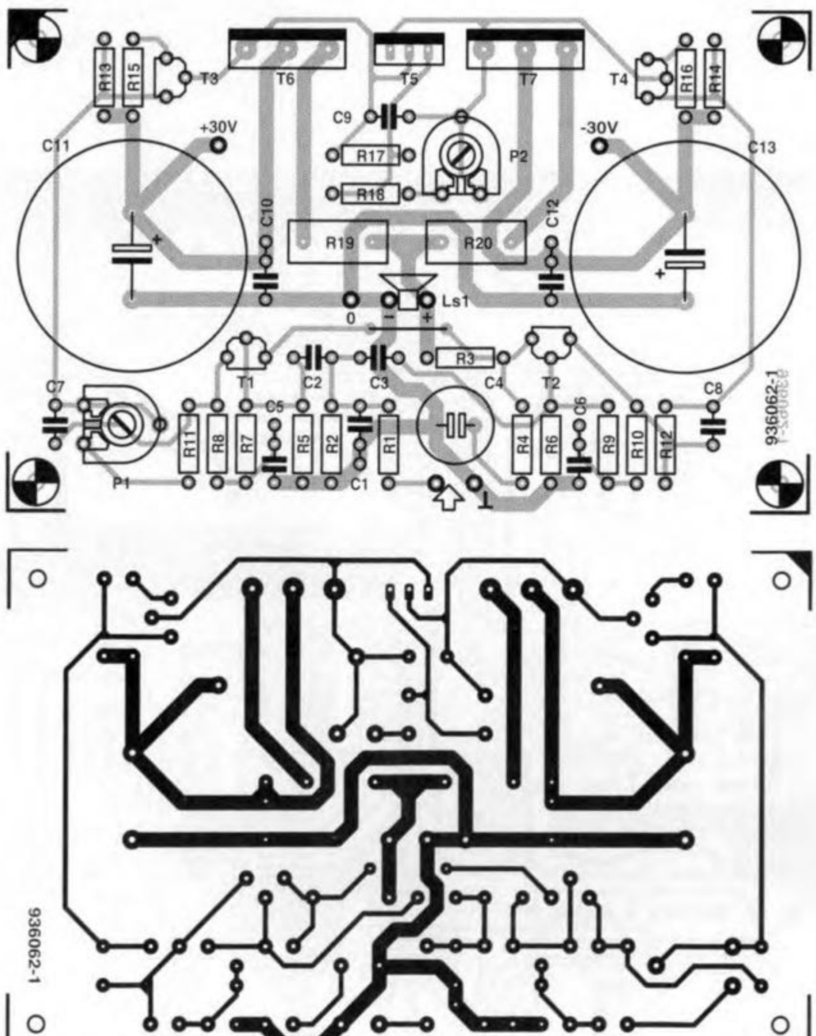


Fig. 7. Printed-circuit board for the output amplifier section.

POWER SUPPLY: Fig. 3

Resistors:

R_1–R_8 = 0.1 Ω, 5 W

R_9 = 10 kΩ

Capacitors:

C_1–C_4 = 10 000 μF, 50 V

Semiconductors:

D_1 = LED, low current

B_1 = bridge rectifier B200C35

Tr_1 = toroidal mains transformer, secondary 2×22 V, 300 VA (mono), 600 VA (stereo)

GENERAL

Standard 19 in, 2-unit high instrument case

Mains entry with integral fusae

Mains on/off switch with integral LED indicator

[936062]

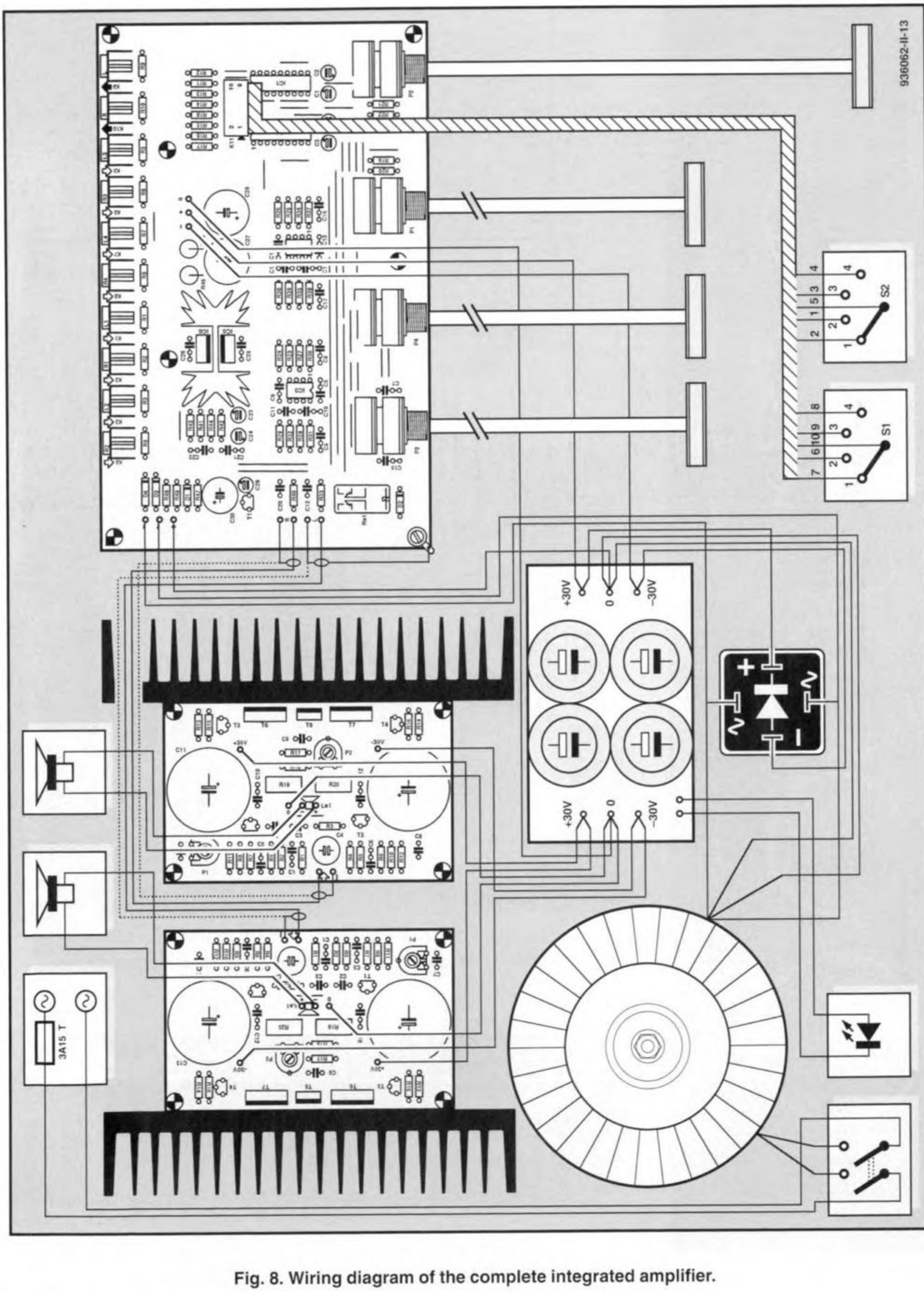


Fig. 8. Wiring diagram of the complete integrated amplifier.

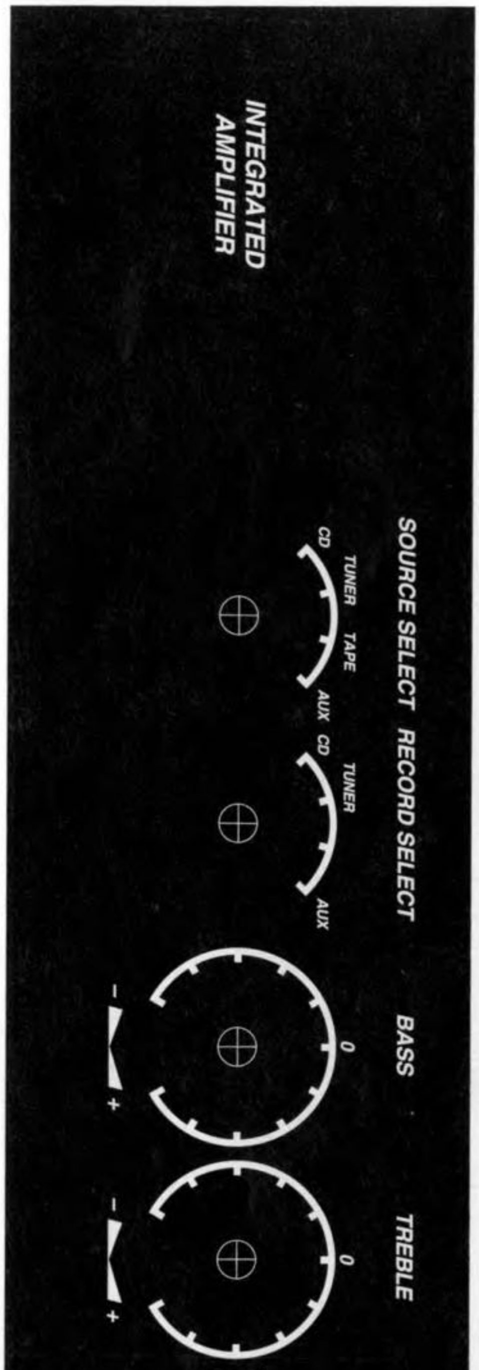


Fig. 9. Suggested front panel.

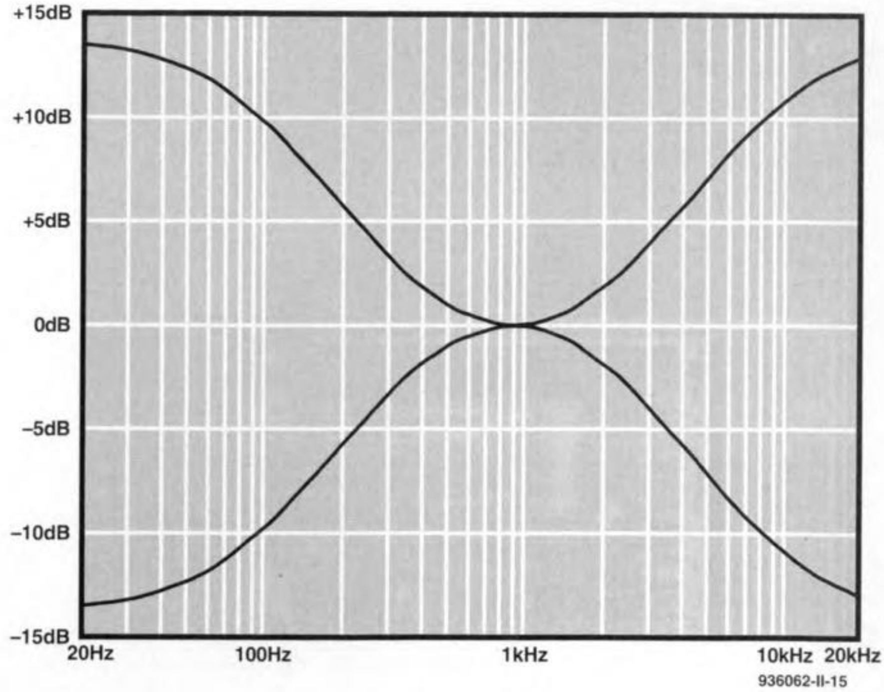


Fig. 10. Frequency characteristics of the amplifier with the tone control at its extreme settings

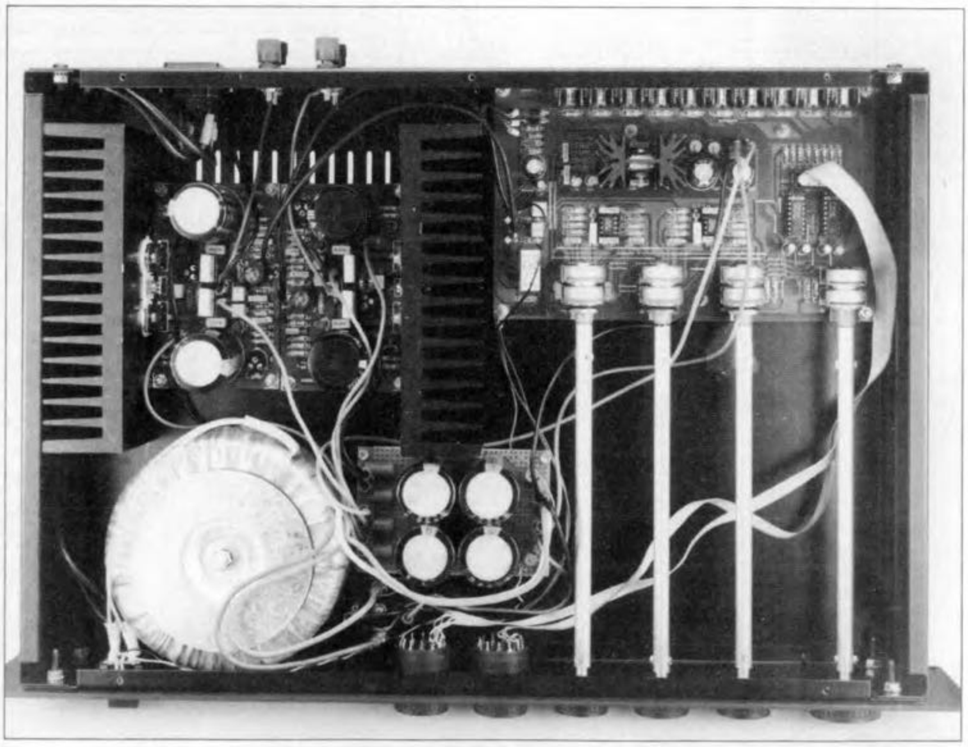


Fig. 11. Inside top view of the completed prototype amplifier.

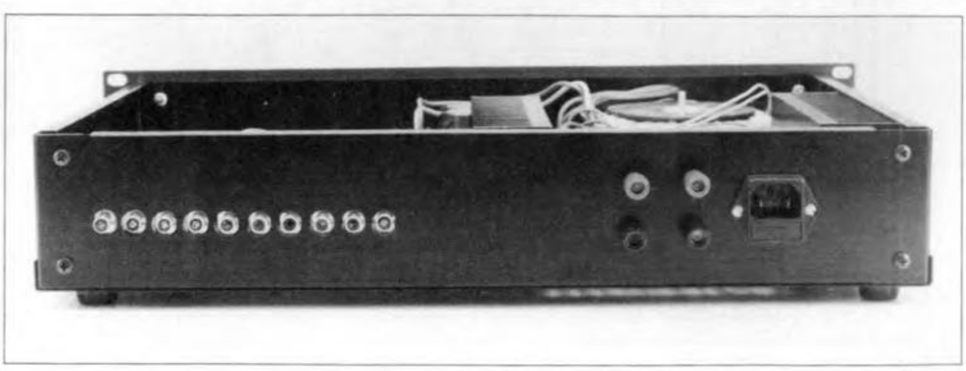
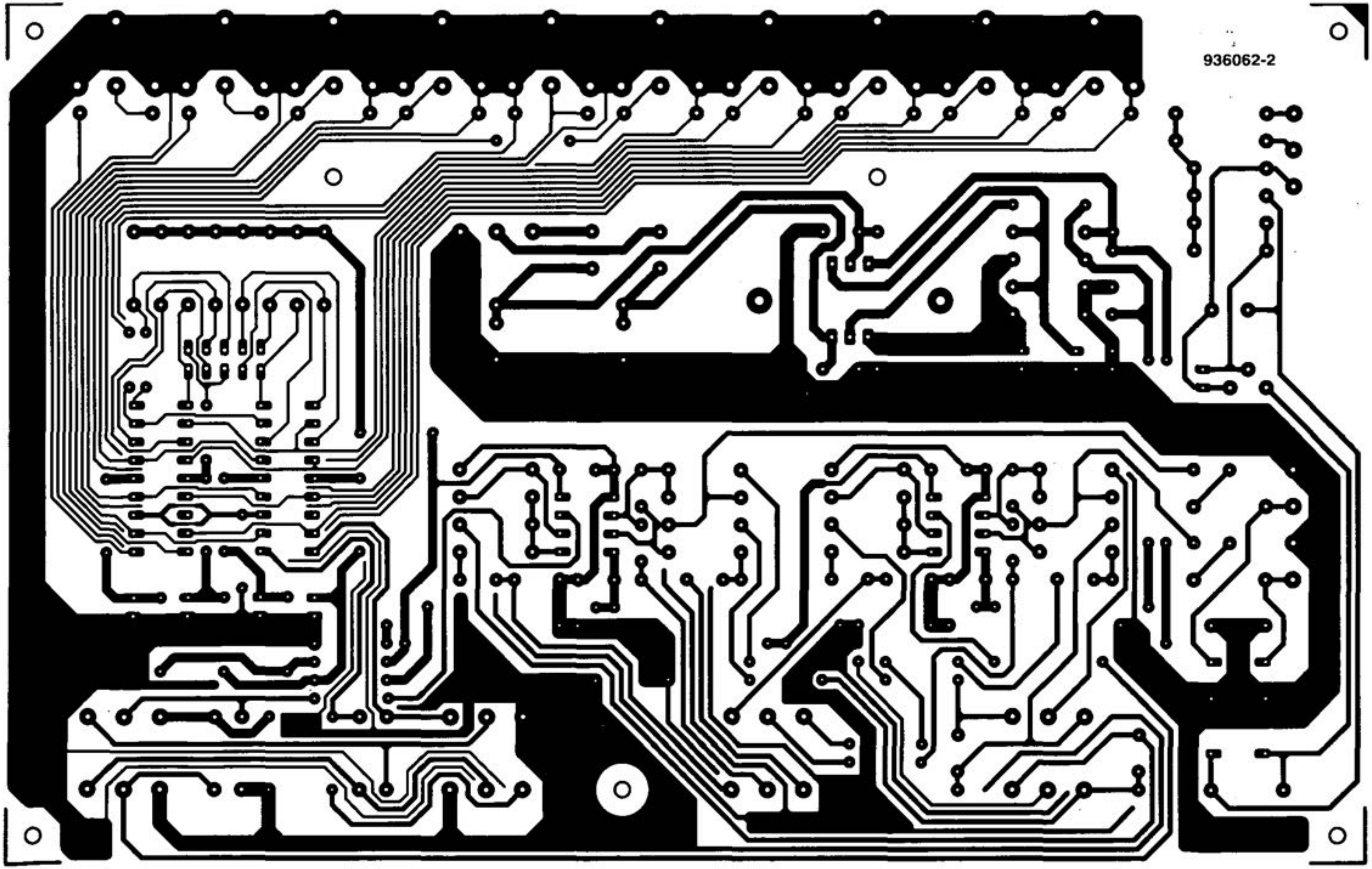


Fig. 12. Rear view of the integrated amplifier.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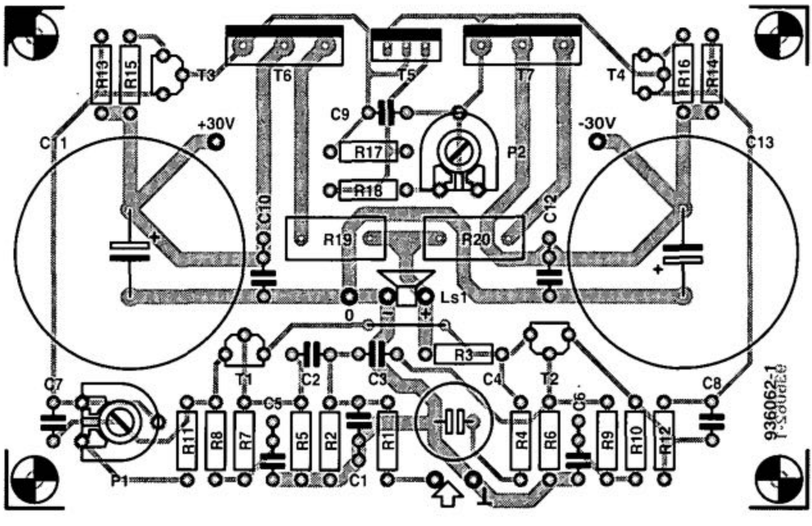
R13
R15
T3
T6
T5
T7
T4
R16
R14
C9
+30V
-30V
C11
C13
R17
P2
R18
C10
C12
R19
R20
Ls1
0
T1
T2
C2
C3
R3
C4
C7
C8
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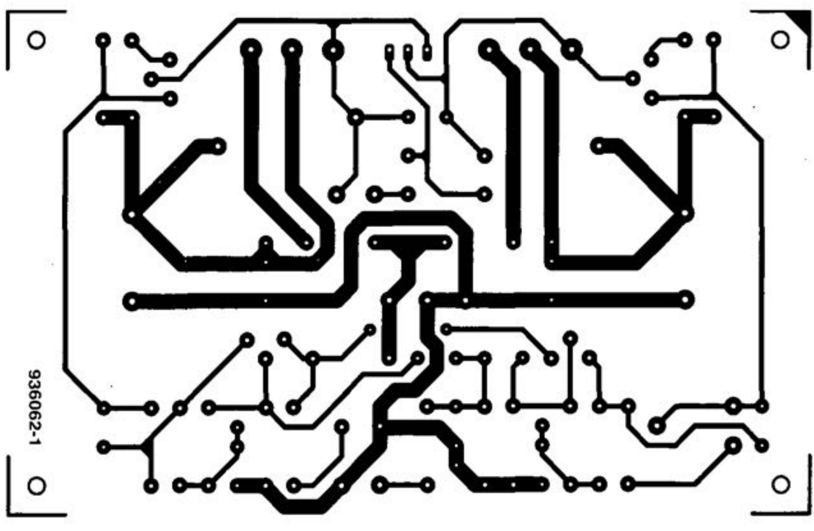
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TESTER FOR INFRA-RED REMOTE CONTROL

Design by A. Rietjens

Modern audio and video systems, virtually without exception, use infra-red remote control. If one day (normally a Sunday) the remote control unit does not elicit a response from the associated equipment, the tester described will quickly establish the cause of failure (hopefully, it is just a flat battery)

Modern domestic remote control units for radio, television and audio systems invariably use infra-red light to pass instructions to the receiver in the associated equipment. The transmitter, housed in a small, handheld box, uses an infra-red transmit diode, while the associated receiver, built in the audio or video equipment, uses an infra-red photo diode. When one of its control buttons is pressed, the transmitter emits a burst of high-frequency signals. Since humans can not see infra-red light, it is impossible for us to observe whether the transmitter does indeed emit signals. The present tester can detect these signals and at the same time give a general indication of their intensity and quality.

How does it work?

Before the tester is detailed, a brief description of how an infra-red remote control works may be useful. The description is based on the frequently used Philips/Sony RC5 coding. Other manufacturers may use different coding techniques, but that does not invalidate the method of operation nor the tester.

Each burst of IR light emitted by the transmitter is 25 ms long and contains a 14-bit code word—see **Fig. 1**. Each burst of light is followed by an interval of about 90 ms. Each bit in the code word is superimposed on to a carrier of 36 kHz. The carrier is not symmetric: its logic '0' period is three times as long as its logic '1' period.

The tester contains an integrated decoder that detects the IR light and converts this into a train of digital bits. This train of data is used to give an indication of the quality of the light signals. This is based on the fact that the IR receiver will not function properly with (very) weak signals: capturing and synchronizing them will take longer than with strong signals. This time difference in processing gives an indication of the quality of the signals.

A full description of the RC5 coding is given in Ref. 1.

Design of tester

The IR detector in the block schematic of the tester in **Fig. 2** is a complete receiver that is able to filter from the IR light it receives only those signals that are associated with IR remote control. This is made possible by the fact that all IR remote control systems make use of a high frequency carrier. Low-frequency signals are filtered out and thus do not appear in the output. The detector output is a TTL signal that indicates whether or not HF. signals are being received. That is, the level at the output varies in rhythm with the HF bursts that reach the photo diode: a high level means there is no h.f. signal, while a low level indicates that an HF signal is present.

The tester works on the principle that the pulses used in the test are

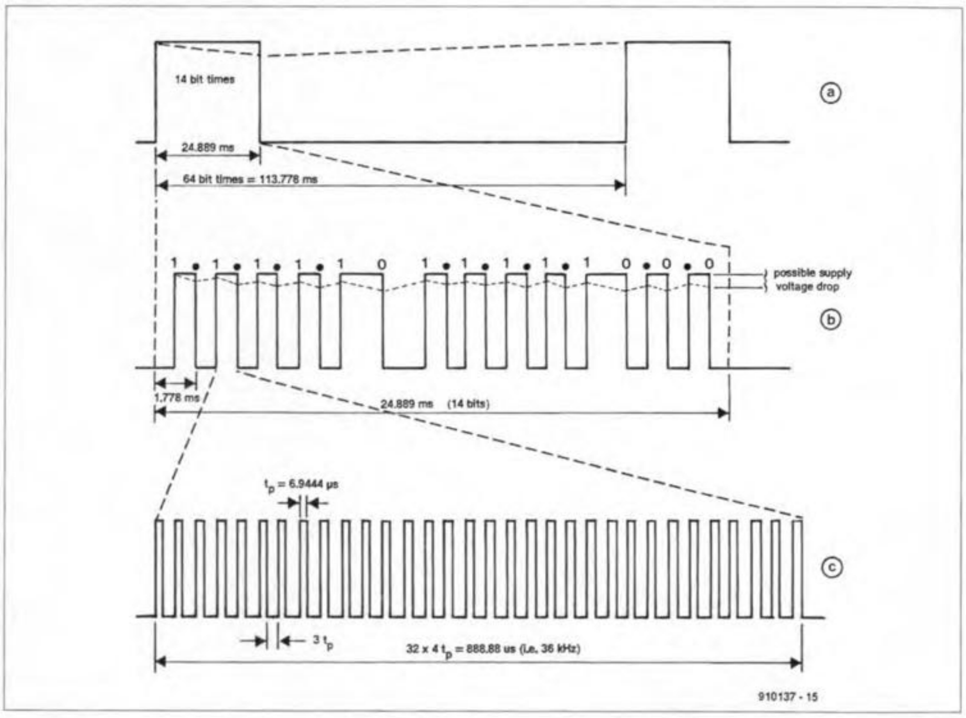


Fig. 1. How an RC5 command is modulated.

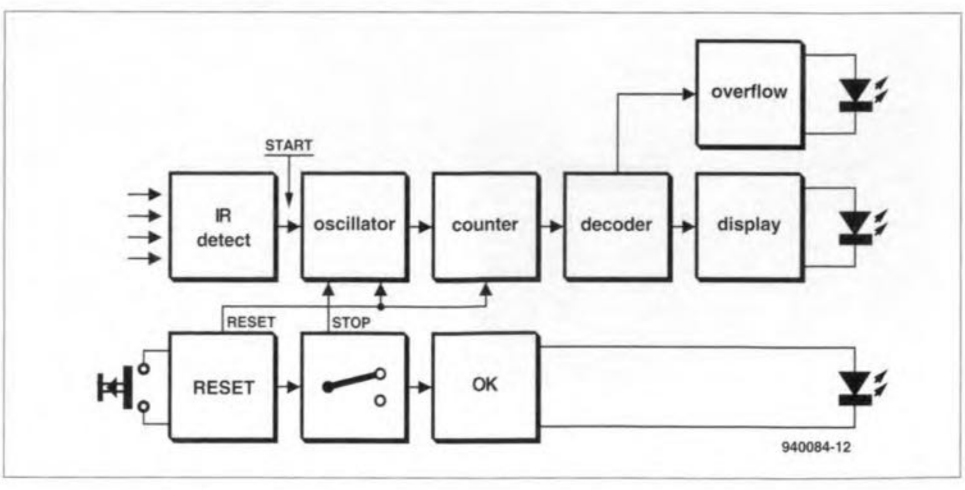


Fig. 2. Block diagram of the remote control tester.

identical. However, not only does the pulse train depend on which button is pressed on the transmitter, but the code varies even when the same button is pressed twice in succession. Fortunately, the header of each instruction is constant, and this is, therefore, used in the tester.

Even then, there is a slight difficulty: in some protocols the first bit is relatively long to enable the transmitter and receiver to synchronize. Because of this, the variation in length caused by poor communication is very small, so that it gives no, or very little, idea of the quality of the signals. To bypass this difficulty, the tester has a change-over switch that enables either the first or the second bit to be selected.

Immediately a pulse train is received, the tester starts an oscillator. The number of pulses counted in the first (or second) bit is read, converted and then made visible on a display (a bar of LEDs).

The LED which indicates that a pulse train has been received also functions as underflow indicator. There is also an overflow indicator. Both LEDs are useful during the calibration of the tester.

Circuit description

To some extent, the circuit, whose diagram is shown in **Fig. 3**, is based on IC_1. This chip contains both the oscillator and counter which are of paramount importance for measuring the

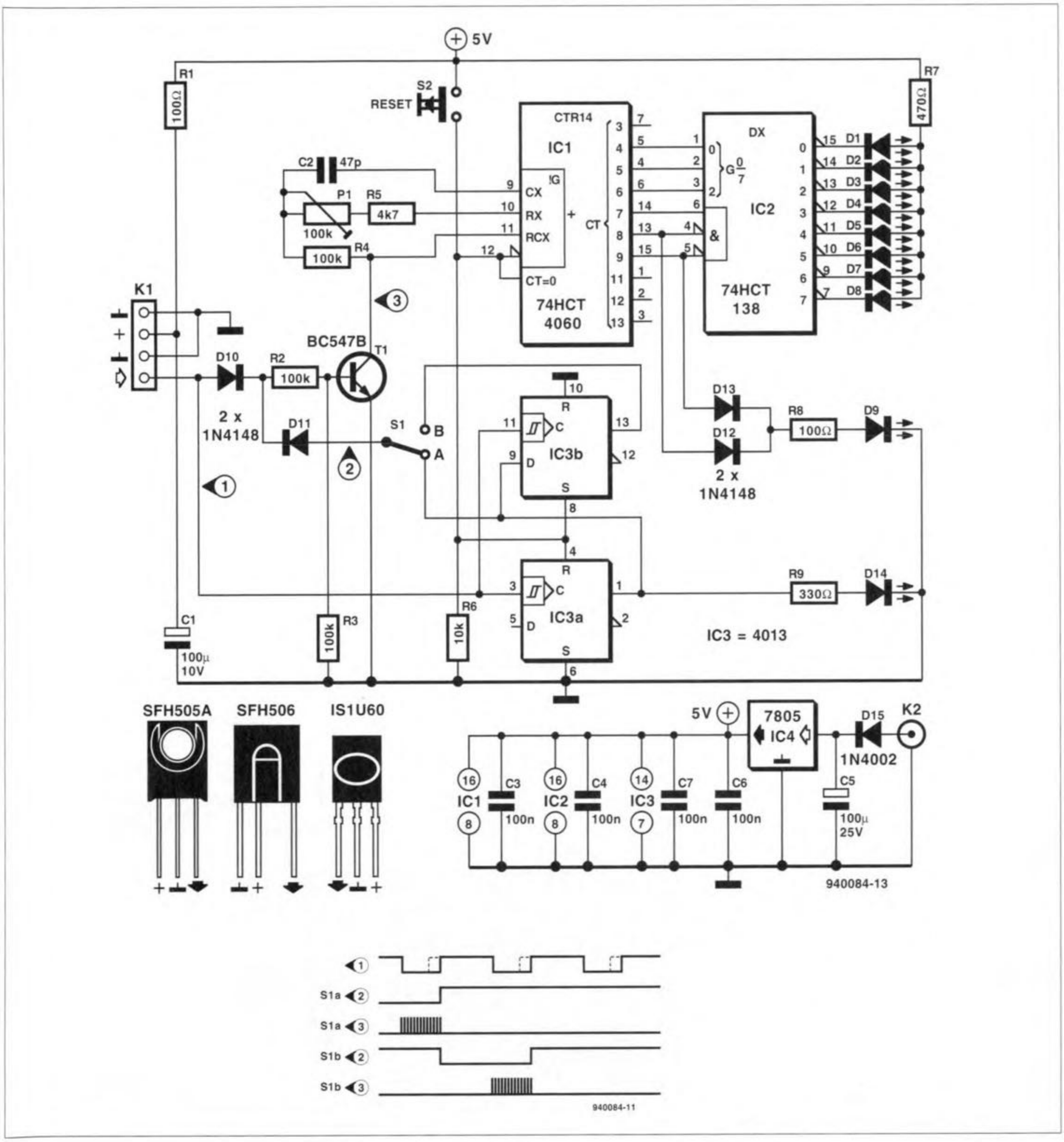


Fig. 3. Circuit diagram of the remote control unit tester.

pulse periods.

The integrated IR photo diode is connected to K_1. The digital code converted from the incoming IR signals is applied to pin 1. A high logic level at this pin, applied to transistor T_1 via D_2 and potential divider R_2-R_3, causes the transistor to conduct. This results in the oscillator input (pin 11) of IC_1 being connected to earth

The two bistables (flip-flops) in IC_3 determine which pulse will be measured. After a reset, the Q output (pin 1) of IC_{3a} is low and that of IC_{3b} (pin 13) is high. The leading edge of the digital input signal gives both bistables a clock pulse, on the receipt of the leading edge of which the level at pin 5 of IC_3 is read and applied to pin 1. After the first clock pulse, pin 1 is high because pin is linked to the +5 V line. Diode D_{14} then lights to indicate that the first data pulse has been received. Pin 13 is kept low because pin 9 is held low by pin 1 at the instant the leading edge of the clock pulse is received. When the second clock pulse is received, pin 9 also goes high, so that from the third clock pulse onward both Q outputs are high.

The oscillator and counter in IC_1 operate only when transistor T_1 is off. This is the case only when the anodes of D_{10} and D_{11} are low. As far as D_{10} is concerned, this is so every time a pulse arrives at pin 1 of K_1. In the case of D_{11}, it depends on the position of jumper S_1. The transistor is off during the first data pulse with the jumper in position A, and during the second data pulse with S_1 in position B. During all subsequent data pulses, the transistor conducts. In the timing diagram in **Fig. 3**, signals 2 and 3 (S_{1a}) are relevant when S_1 is in position A, and signals 2 and 3 (S_{1b}) when the jumper is in position B.

Only outputs Q_4–Q_9 of the counter are used. Pins 4, 5 and 6 are linked to the three inputs of 3-to-8 converter IC_2. This chip is enabled when pin 14 of IC_1 is high and pins 13 and 15 are low. This condition is indicated by one of diodes D_1–D_8 lighting. This arrangement means that measurements take place only during the second half of the period of the data pulse. Pulses that are shorter than half of their original duration are so mutilated that they are unusable. If more than eight clock pulses occur during half the period, the clock frequency is too high and an overflow takes place, whereupon D_9 lights. Either pin 13 or pin 14 or both are then high. This results in IC_2 being disabled and none of D_1–D_8 lights. The oscillator frequency, which is determined by R_5, C_2 and P_1, can be lowered with P_1 to ensure that the requisite number of pulses happen during the measurement period.

Three different types of photo diode may be used; the pinouts of all three are given in **Fig. 3**.

Power is obtained from a 9 V, 250 mA mains adaptor whose output is regulated by IC_4. The circuit is protected against incorrect connection of the mains adaptor by D_{15}.

Construction

The tester is intended to be built on the printed-circuit board shown in **Fig. 4**.

As usual, commence by soldering the five wire bridge in place, followed by the smaller components. The design of the board allows the use of either a digitast switch or a data switch. These are slightly dearer than a standard push button type, but they are more reliable and are easily fitted.

The photo diode is soldered to the holes marked K_1: pin 1 must go the hole nearest the slanting line of the symbol.

Alignment

When the board is finished, connect the mains adaptor to it and set P_1 to maximum resistance: the oscillator then generates its lowest frequency. Set jumper S_1 to position A. When the reset is pressed, all LEDs should be off. Press one button on the remote control transmitter, whereupon at least D_{14} should light. (It is advisable to fit new batteries in the remote control transmitter before calibrating the tester). If it does not, check the power supply and the position of S_1.

If D_{14} lights, one of D_1–D_9 will also light. If D_9 lights or flickers, there is an overflow. In that case, set S_1 to position B, reset the tester and press one of the buttons on the remote control transmitter. If this does not result in D_{14} going out, reset S_1 to position A and replace C_2 by a 470pF capacitor. If this still does not work, there is almost certainly a defect in the circuit, which can only be found by careful checking and rechecking.

Assuming that all works well, hold the tester near the transmitter and adjust P_1 until D_7 or D_8 lights. Holding

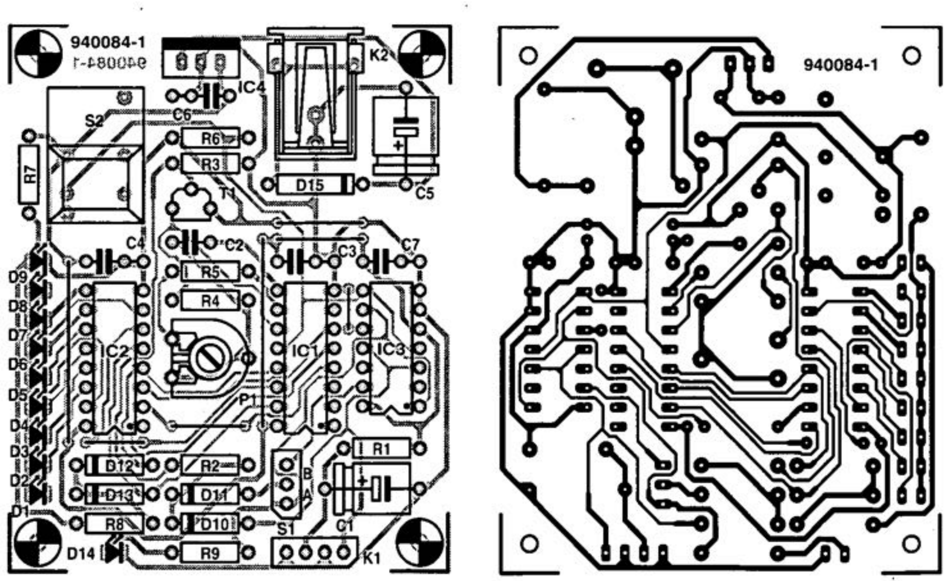


Fig. 4. Printed circuit board for the remote control unit tester.

the tester at greater and greater distances from the transmitter will cause different LEDs to light: this proves that the tester operates correctly. If it gives varying results, set S_1 to position B.

Finally, bear in mind to press the reset button before each measurement.

Parts list

Resistors:
R_1, R_8 = 100 Ω
R_2, R_3 R_4 = 100 kΩ
R_5 = 4.7 kΩ
R_6 = 10 kΩ
R_7 = 470 Ω
R_9 = 330 Ω
P_1 = 100 kΩ preset

Capacitors:
C_1 = 100 µF, 10 V
C_2 = 47 pF
C_3, C_4*, C_6, C_7 = 100 nF
C_5 = =100 µF, 25 V
* see text

Semiconductors:
D_1–D_9, D_{14} = LED, red
D_{10}–D_{13} = 1N4148
D_{15} = 1N4002
T_1 = BC547B
K_1 = Photo diode, SFH505, SFH506-36 or IS1U60

Integrated circuits:
IC_1 = 74HCT4060
IC_2 = 74HCT138
IC = 4013
IC_4 = 7805

Miscellaneous:
K_2 = mains adaptor connector
S_1 = jumper
S_2 = digitast, data switch or push button switch
PCB Ref. 940084

[940084]

Ref. 1: *Elektor Electronics*, January 1992, p. 60

COMPUTER PSU MONITOR

Design by K. Walraven

A circuit is described for continuously monitoring the various power supply lines in computers. It will also detect spikes (other than RF.) on these lines.

The monitor checks that the ±5 V and ±12 V supply voltages to a computer are within ±5% of their nominal value. It will also detect spikes of a couple of hundreds of nanoseconds, but its operational amplifiers are too slow to detect RF interference.

The circuit is housed on a card that is intended to be inserted into one of the free ports of the computer. This has the advantage that it is always present and that the voltages are monitored close to the computer's mother board.

Each supply voltage may be too low, all right, or too high. Each of these states is indicated by an LED. The all right state has a fourth LED which has a memory that registers whether the all right LED has been off at least once after a system reset. If so, there is a spike on the supply line.

The LEDs and the reset control may be brought to the front panel via a length of ribbon cable to enable monitoring to take place at the front rather than at the rear of the computer. The board has been designed to make this a simple modification.

Detector/indicator circuit

The circuit of the monitor (**Fig. 1**) consists of four similar detector circuits, a power supply and 16 indicator LEDs.

To keep the circuit simple, the supply voltages to be monitored are brought down to a standard level of 1.25 V. Reference potentials REF+ and REF– are symmetrically centred on this standard voltage; they differ from it by a margin that is preset with P_1. With component values as specified, this margin is 0–10%.

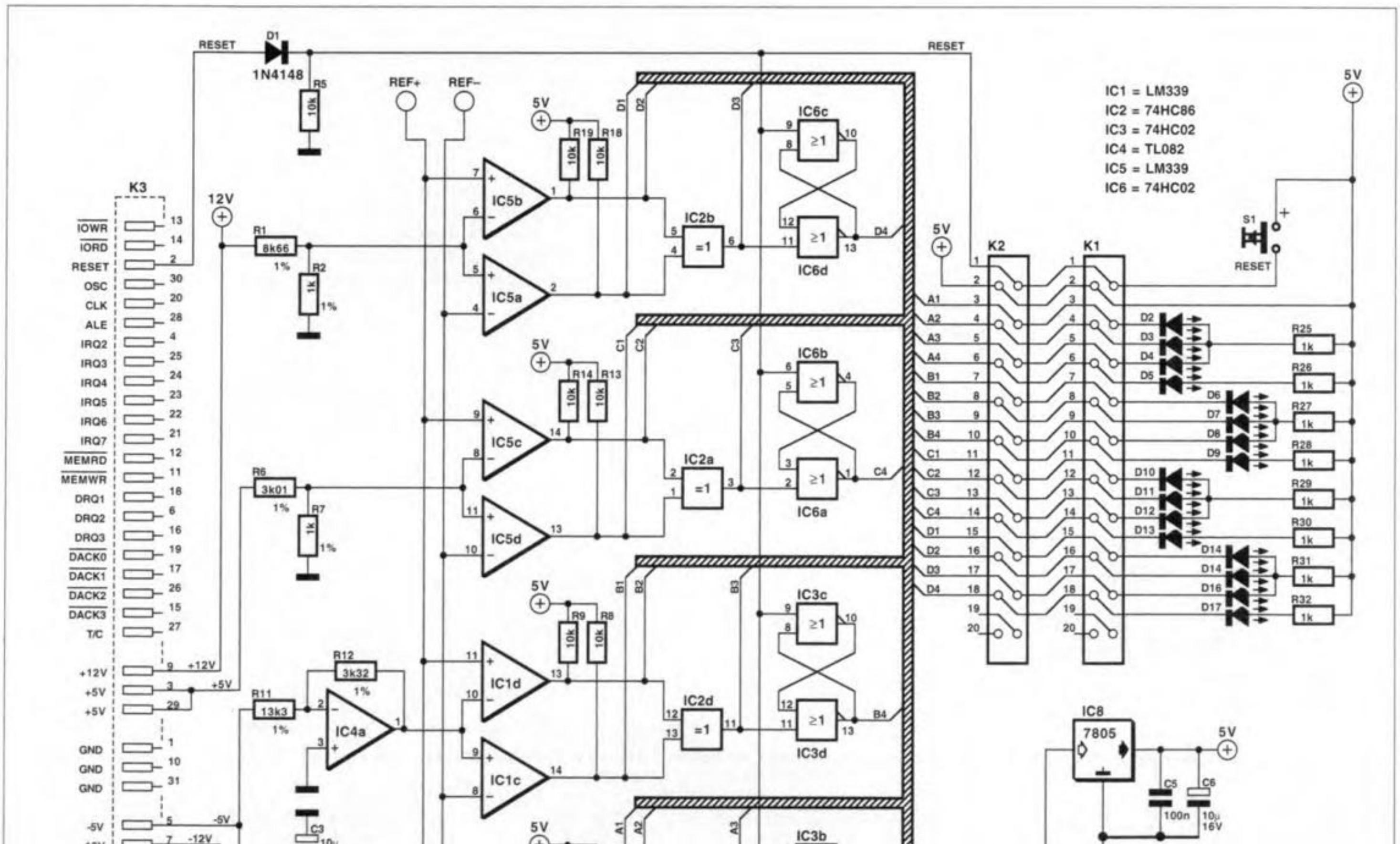


Fig. 1. Circuit diagram of the PSU monitor.

The +5 V and +12 V supply voltages are reduced to 1.25 V by resistors R_6, R_7 and R_1, R_2 respectively. The −5 V and −12 V voltages are lowered by resistors R_{11}, R_{12} and inverter IC_{4a}, and R_{16}, R_{17} and inverter IC_{4b} respectively.

The standard level is compared with reference voltages by two comparators, say, IC_{1a} and IC_{1b}. If the levels correspond, the outputs of the comparators are high and the (red) LEDs connected to the outputs remain off. Since the inputs to the XOR gate, IC_{2c}, following the opamps, are then high, the output of the gate is low, which causes the associated (green) LED to light.

The last stage of each detector circuit is a bistable (flip-flop) formed by two NOR gates (as, for instance, IC_{3a} and IC_{3b}). The bistable is reset by pressing S_1. A system reset of the computer also resets the bistable. The LED connected to the Q output of the bistable goes out after the reset. Diode D_1 prevents a reset of the entire computer when S_1 is pressed.

If the level at the set input of, say, IC_{3a} (pin 2), goes high, possibly because the supply voltage drops or rises briefly, the bistable is set and the fourth (yellow) LED lights. The LED stays on until the next reset. To ensure that all bistables are reset after the computer has been switched on, they are also connected to the reset circuit in the computer.

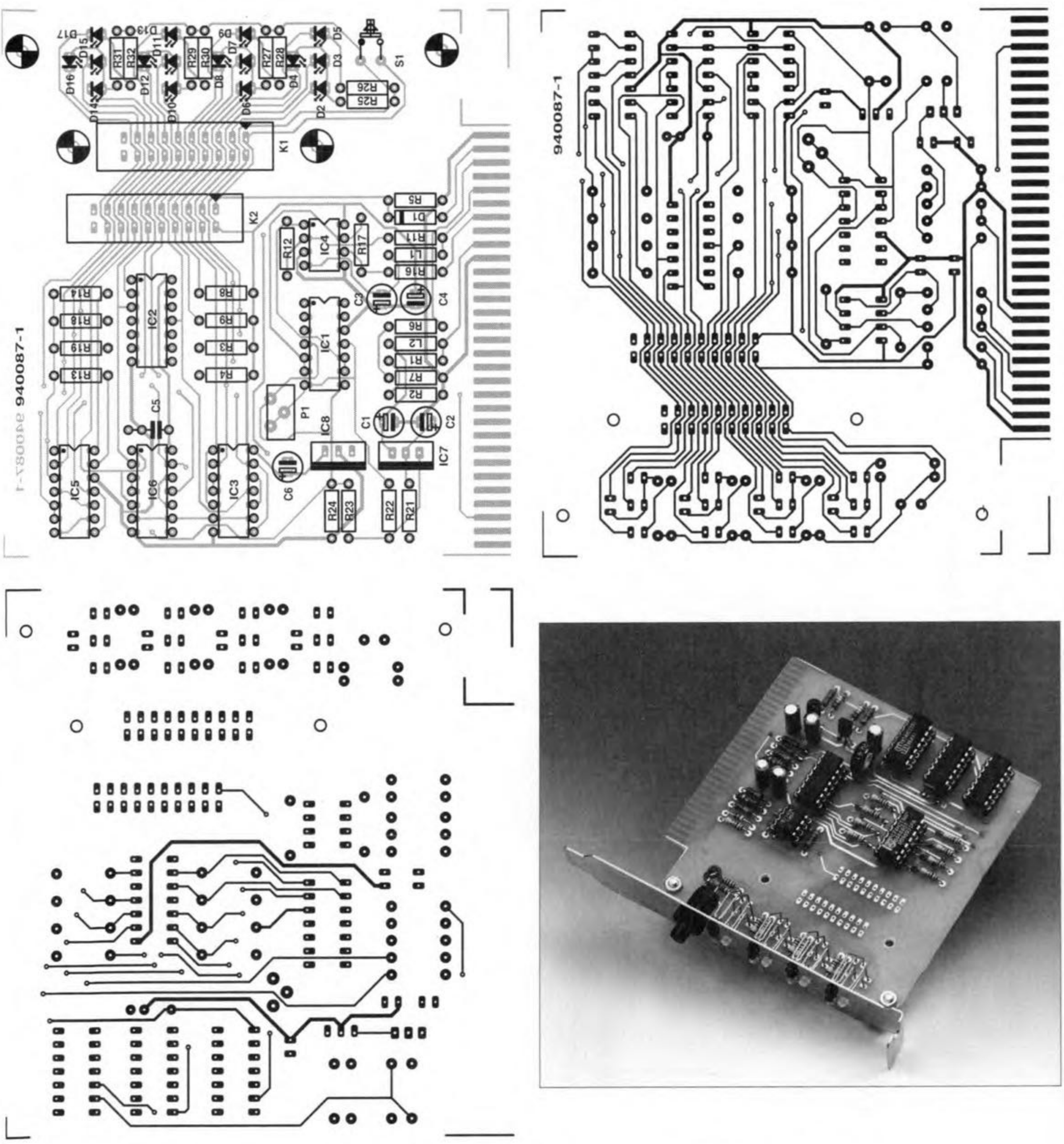


Fig. 2. Printed-circuit board for the PSU monitor. Photograph shows completed prototype.

The 5 V power supply for the monitor is derived from a 12 V source regulated by IC_8. The –5 V supply for IC_4 is derived from the computer. A small inductor, L_1 or L_2, as the case may be, is connected in series with the –5 V and +12 V lines to prevent the buffer capacitors in the power supply suppressing spikes (which would prevent the detectors sensing them).

Regulator IC_7 provides the reference voltages. This IC has an internal reference of 1.25 V, which here is present across R_{21} and R_{22}. Since R_{23} and R_{24} have the same value as R_{21} and R_{22} respectively, the voltage across them is also 1.25 V. When P_1 has a value of 0 Ω, the potential across both R_{21} and R_{24} is 1.25 V. The levels at REF+ and REF– are then the same (1.25 V). When P_1 is set to its maximum value, the potential across R_{21} and R_{24} is 1.13 V. The level at REF+ is then 1.37 V and that at REF– is 1.13 V.

Construction

The monitor is intended to be built on a double-sided printed-circuit board as shown in **Fig. 2** (which is unfortunately not available ready made). A single-sided board proved not feasible, because it would require more than 25 wire bridges. The design of the board ensures that the LEDs (slightly bent) protrude outside after the board has been slotted into the computer. As mentioned earlier, the section of the board on which the LEDs and the reset switch are located may be cut off and brought to the front of the computer via a length of ribbon cable termined in headers. The cut must run in between K_1 and K_2, but the cutting must ensure that the two fixing holes for the support bracket near K_1 remain on the plug-in board. If this option is not used, headers K_1 and K_2 are not required.

When the board has been finished, the monitor is ready for use after P_1 has been adjusted as desired. Normally, the circuits work correctly with a tolerance of 5%, which is set as follows. After the board has been inserted into the computer and this has been switched on, connect a digital multimeter between earth and pin 4 of IC_5 and adjust P_1 for a meter reading of 1.19 V. The potential at pin 7 of IC_5 should then be 1.31 V. If setting these values is not possible, the LM317 used is not sufficiently accurate. In that case, replace it by an LT117 from Linear Technology which has a tolerance of only 1%.

Note that if the set limits are tight, it may happen that after S_1 has been pressed, the yellow LEDs seem to stay on. This is caused by brief supply voltage variations that occur regularly in computers. The reaction of the red LEDs is so fleeting that it appears as if they remain off. Provided the computer functions properly, it is advisable in such a case to set the limits with P_1 rather wider.

Parts list

Resistors:
R_1 = 8.66 kΩ, 1%
R_2, R_7 = 1 kΩ, 1%
R_3–R_5, R_8, R_9, R_{13}, R_{14}, R_{18}, R_{19} = 10 kΩ
R_6 = 3.01 kΩ, 1%
R_{11} = 13.3 kΩ, 1%
R_{12}, R_{17} = 3.32 kΩ, 1%
R_{16} = 31.6 kΩ, 1%
R_{21}, R_{24} = 221 Ω, 1%
R_{22}, R_{23} = 49.9 Ω, 1%
R_{25}–R_{32} = 1 kΩ
P_1 = 100 Ω preset, vertical

Capacitors:
C_1–C_4 = 10 µF, 16 V, radial
C_5 = 100 nF

Inductors:
L_1, L_2 = 1 mH

Semiconductors:
D_1 = 1N 4148
D_2, D_3, D_6, D_7, D_{10}, D_{11}, D_{14}, D_{15} = LED, 3 mm, red*
D_4, D_8, D_{12}, D_{16} = LED, 3 mm, green*
D_5, D_9, D_{13}, D_{17} = LED, 3 mm, yellow*

* high efficiency

Integrated circuits:
IC_1, IC_5 = LM339 or LP339
IC_2 = 74HC86 or HCT86
IC_3, IC_6 = 74HC02 or HCT02
IC_4 = TL082
IC_7 = LM317 or LM317L – see text
IC_8 = 7805 or 78L05

Miscellaneous:
K_1, K_2 = 20-pin straight box header see text
S_1 = press button switch with make contact
PC insertion card support bracket, e.g.,Fisher KHPCL (see **Fig. 3**) or Eurodis No. Spe22833.

[940087]

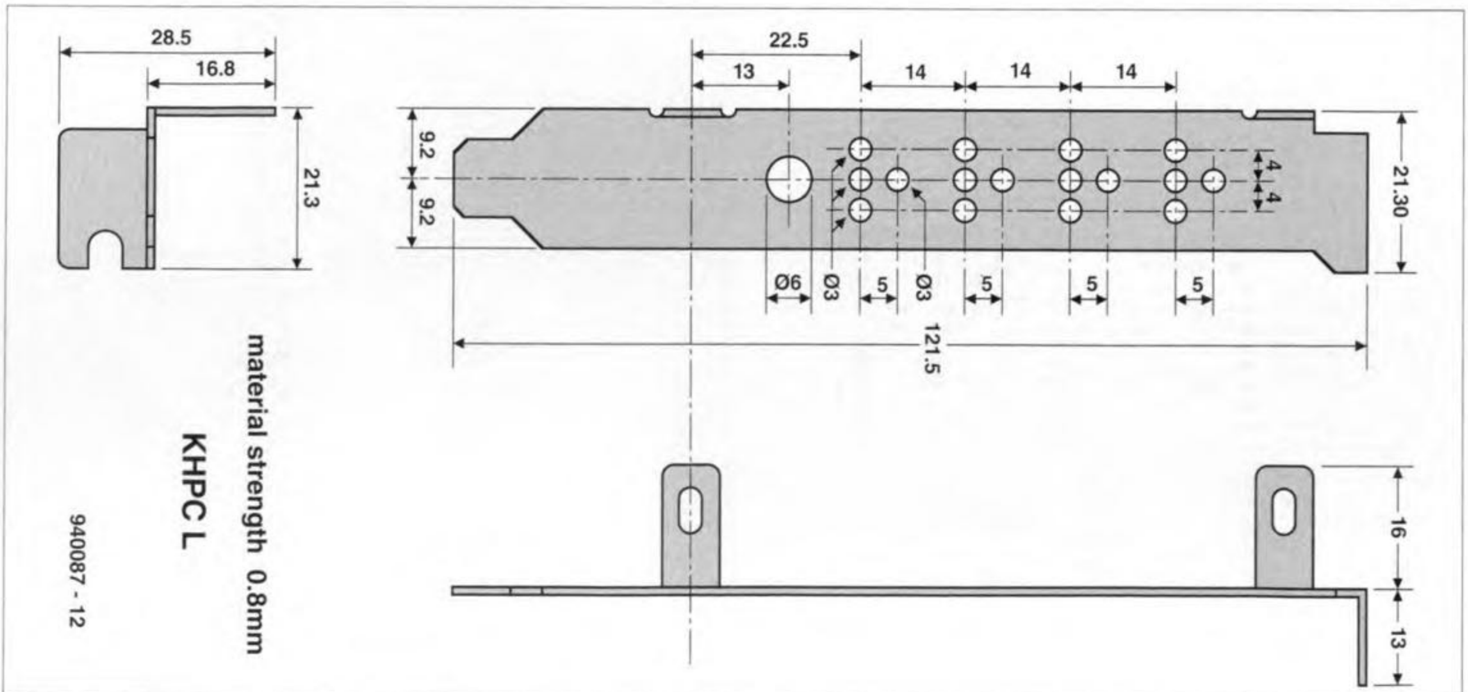
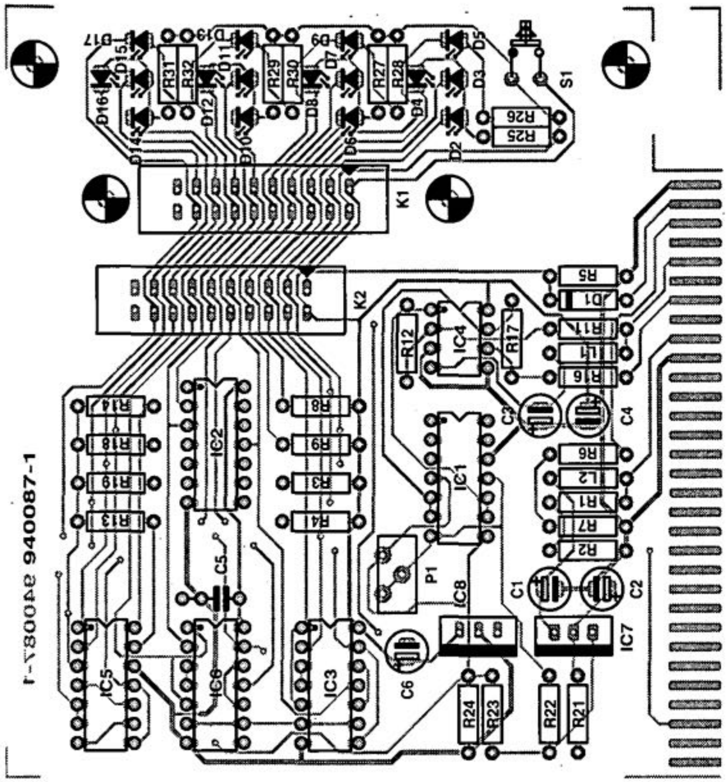


Fig. 3. Template (1:1) of the support bracket showing how the LEDs should be fitted.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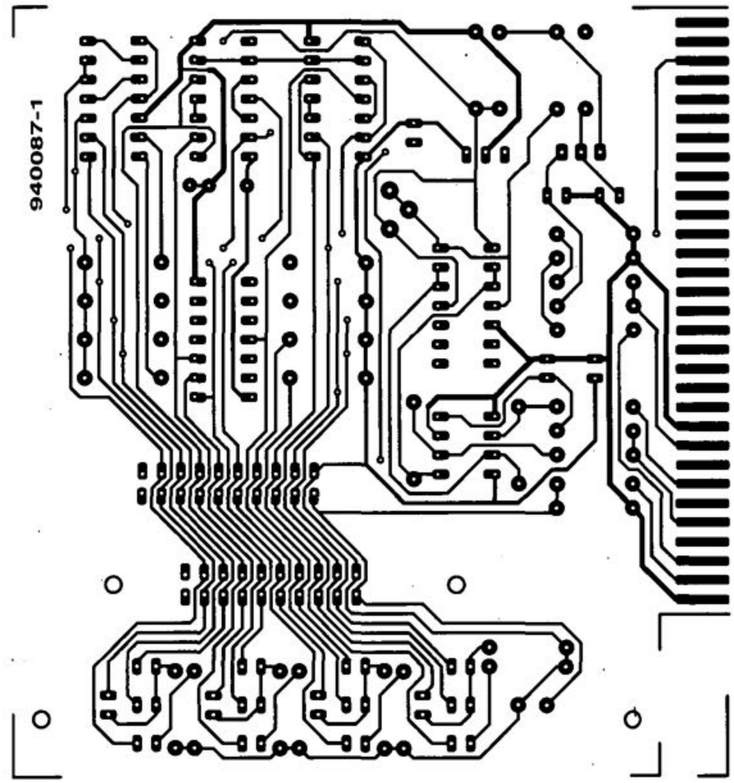
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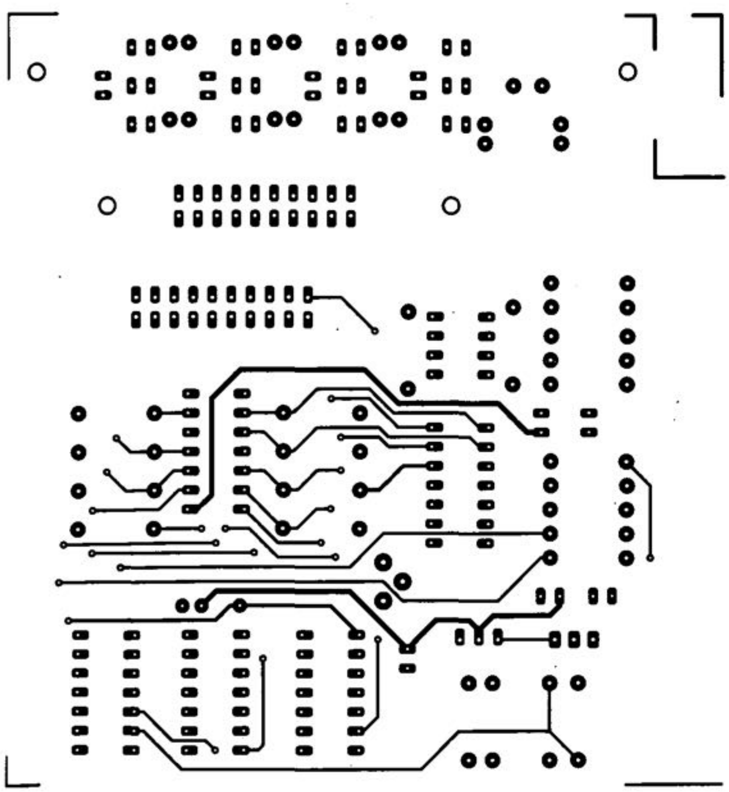
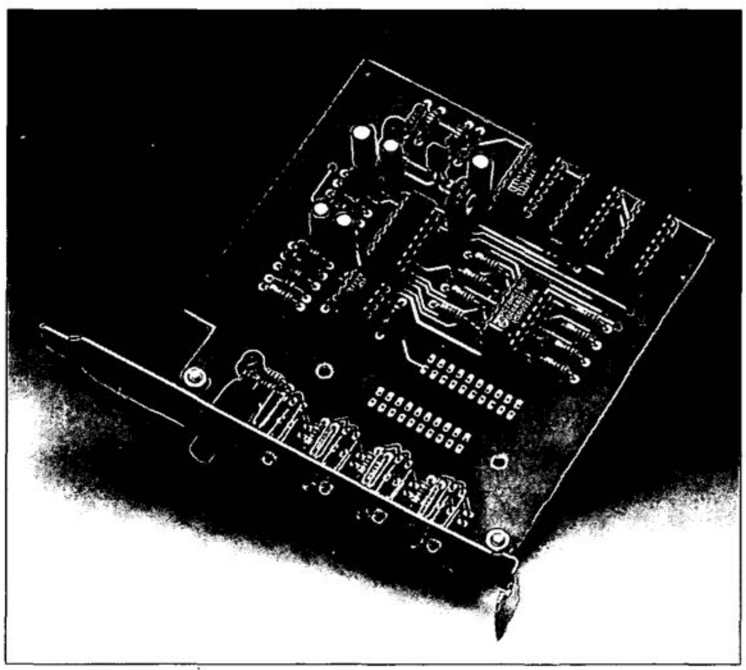



STABLE D.C.-D.C. CONVERTER

Design by L. Lemmens

The very compact converter produces a stable 5 V direct voltage supply from an input of 2.5 V, and is thus eminently suitable for use in portable equipment.

Battery-operated equipment that contains digital circuits often requires a supply voltage of 5 V. If stabilization of the supply is required, the battery voltage needs to be at least 6 V owing to the drop across the regulator. Standard regulators can not be used, of course, since these require an input voltage 3 V higher than the output voltage. Even a low-drop regulator needs a voltage drop of not less than 0.4 V. And then there is the recurring problem of space being limited to no larger than for, say, two HP7 (AA, UM3, Mignon) batteries. There are then two ways the designer can take. One is to be satisfied with a supply of 2–3 V and design the electronics accordingly. This is, however, not always possible. The other way is to use a d.c.-d.c. converter as described in this article.

In spite of its compactness, the converter can supply 100 mA at 5 V from an input of 2.5 V.

MAX660

The converter is based on an IC type MAX660 from Maxim. It operates on the charge pump principle and fulfils two functions: it can convert a positive voltage into a negative one, and it can double the voltage at its input. It is, in fact, a pin-compatible successor to the ICL7660 with the output current uprated to 100 mA. The internal setup of the IC is shown in **Fig. 1**.

The charge pump principle depends on the rapid charging and discharging of a capacitor, and this requires switches and an oscillator.

An oscillator is contained in the MAX660 and it is followed by a binary scaler. The standard oscillator frequency of 10 kHz can be altered via pin 7. This pin is also used if an external oscillator is employed. The internal voltage regulator can be disabled via pin 6 if operation from a very low input voltage is desired.

The (electronic) switches are formed by four MOSFETs. Since the substrates of the FETs on the right always need a negative voltage with respect to the source (to prevent leakage via the substrate), a logic network is provided. In combination with the voltage level translator, this network ensures that the substrate is always at the correct potential.

The action of the pump will be described with reference to **Fig. 2**, in which the FETs have been drawn as normal switches. Note that the connections seem different from those in **Fig. 1**; this is because here pin 5 functions as ground, pin 3 as input and pin 8 as output. Capacitor C_3 functions as pump, while C_1 is the (external) output capacitor.

The oscillator voltage causes switch pairs S_2-S_4 and S_1-S_3 to be opened and closed in turn. When S_2 and S_4 are closed, C_3 is charged very rapidly to the battery voltage. When S_1 and S_3 are closed (S_2 and S_4 are then open), C_3 is connected in series with the battery via S_3. At the same time, C_1 is charged via S_3 to the battery voltage plus the voltage across C_3, that is, twice the battery voltage.

Circuit description

The circuit diagram is shown in **Fig. 3.** As in Fig. 2, C_1 is the output capacitor and C_3 is the pump. The manufacturer recommends that, to ensure that the capacitors can be charged rapidly, they are of a type with low internal impedance. Schottky diode D_1 ensures that im-

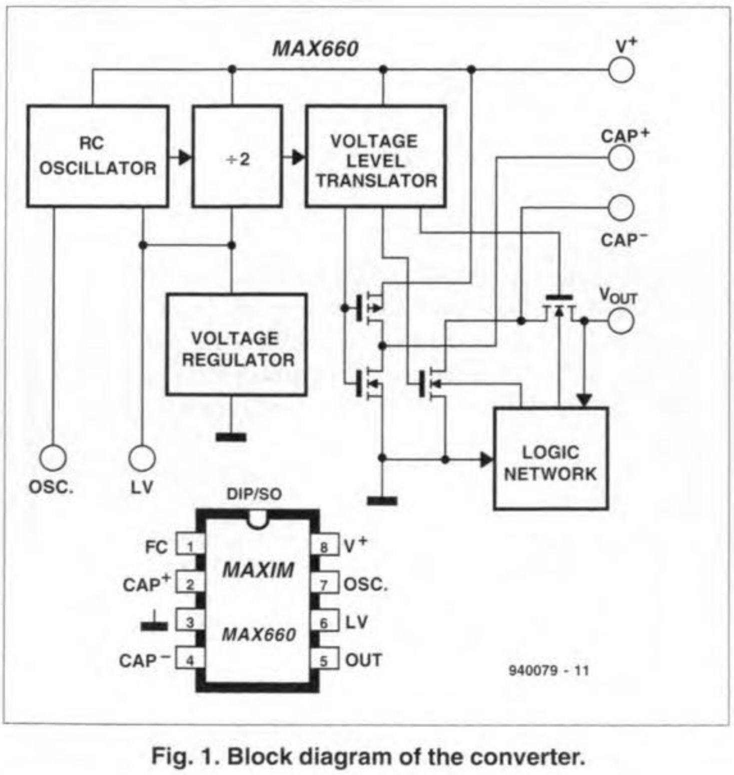


Fig. 1. Block diagram of the converter.

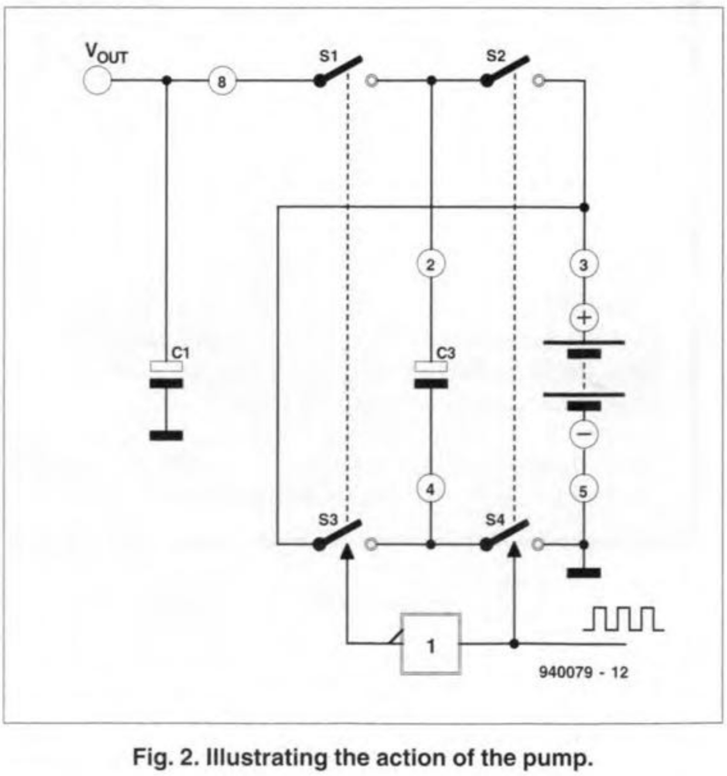
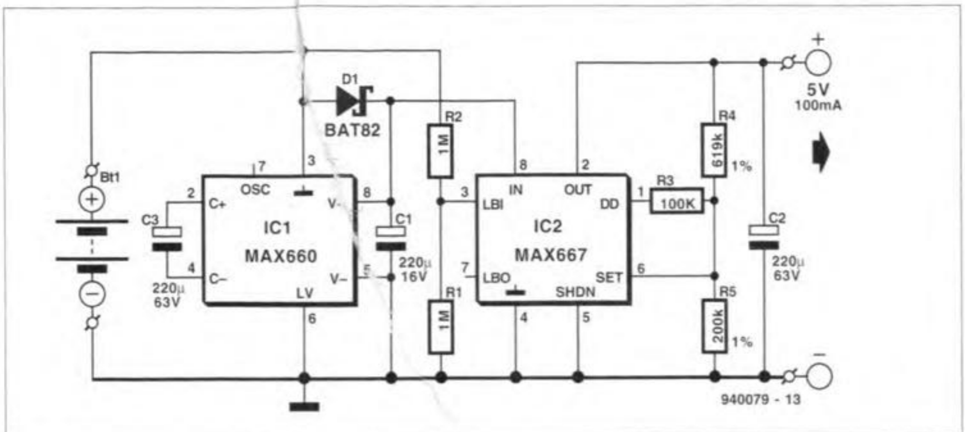


Fig. 2. Illustrating the action of the pump.



mediately after switch-on C_1 gets charged to almost the full battery voltage.

The doubled battery voltage is applied to the input (pin 8) of IC_2. This IC, which has a case identical to that of IC_1, can best be described as low-power, low-drop 5 V voltage regulator. It can handle currents of up to 250 mA and drops only 150 mV at a current of 200 mA. At a current of 100 mA, as in the present converter, the voltage drop is about 100 mV.

The level of the output voltage, U_o, can be set very accurately with potential divider R_4-R_5. Since the internal reference potential, U_{ref}, of the IC is 1.255 V (which is available at pin 6),

$$U_o = (R_4+R_5)/R_5 \times U_{ref} \quad [V].$$

The MAX667 has a low-battery input (pin 3). The potential at this pin is compared with U_{ref}. If it is lower than the reference, the low battery output (pin 7) goes low and this level may be used to control an indicator, for instance, an LED. If pin 7 is connected to a 10 kΩ pull-up resistor, its level may be used to drive a suitable CMOS circuit.

The input to pin 3 is derived from the battery via potential divider R_1-R_2. Since the divider ratio is 1:1, a low battery indication will be given when the battery voltage drops below 2.51 V (that is, $2 \times U_{ref}$). If the low battery option is not needed, R_1 and R_2 may simply be omitted.

Resistor R_3 ensures that the output voltage is cut off when the drop across IC_2 becomes too low for good regulation.

Construction

The converter may be built on the printed-circuit board shown in **Fig. 4** (which is not available ready made) or on a piece of prototyping board.

Once the board has been finished, it is merely a matter of connecting the input voltage and checking with a multimeter that the output voltage is 5 V. It is advisable to recheck the output voltage with a 100 Ω resistor connected in parallel with the meter.

Although it is unlikely that the converter will not work properly, it is advisable to check first whether the regulator or the voltage doubler is at fault. To this end, measure the voltage across C_1; if this is equal to twice the battery voltage, IC_1 fucntions correctly.

In theory, the converter works satisfactorily with input voltages between 2.51 V and 5.5 V. A battery voltage of 5.5 V means that a voltage of 11 V is applied to the regulator, so that this must 'lose' 6 V. At a current of 100 mA, this means a dissipation of 600 mW, which is about the maximum the MAX667 can handle. It is thus advisable not to use such high battery voltages. In any case, is it sensible to double a battery voltage of 5.5 V and then regulate it down to 5 V?

Parts list

Resistors:
R_1, R_2 = 1 MΩ
R_3 = 100 kΩ
R_4 = 619 kΩ, 1%
R_5 = 200 kΩ, 1%

Capacitors:
C_1 = 220 µF, 16 V
C_2, C_3 = 220 µF, 63 V

Semiconductors:
D_1 = BAT82

Integrated circuits:
IC_1 = MAX660 (CPA or EPA)
IC_2 = MAX667 (CPA or EPA)

[940079]

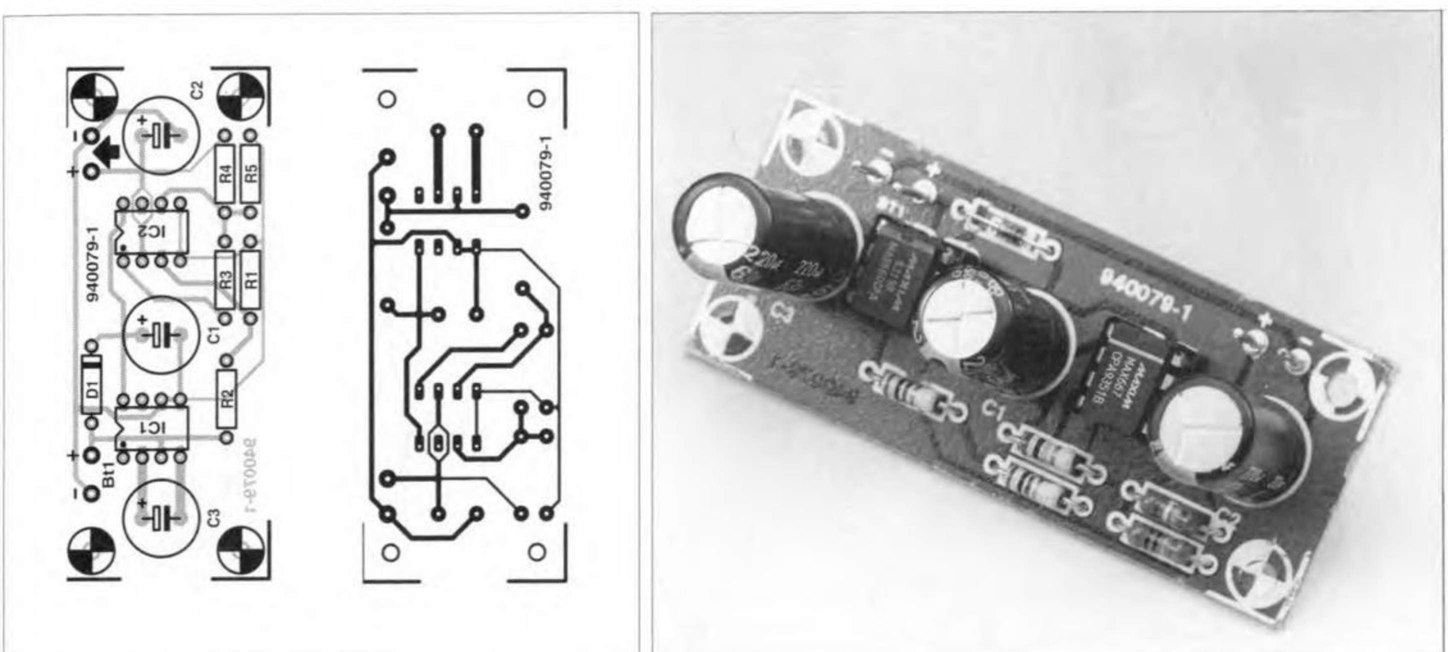
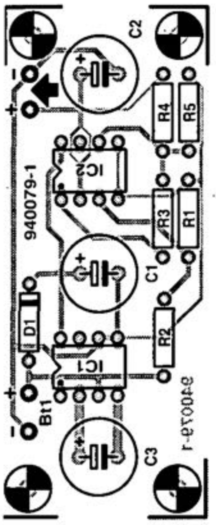


Fig. 4. Printed circuit board of the converter; at the right, the completed prototype.


C2
R4
R5
IC2
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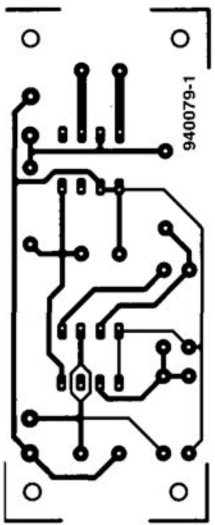
R3
R1
C1
D1
R2
IC1
Bt1
C3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APPLICATION NOTE

The content of this note is based on information received from manufacturers in the electrical and electronics industries, or their representatives, and does not imply practical experience by *Elektor Electronics* or its consultants.

VOICE SCRAMBLERS FX118 AND PCD4440

By G. Kleine

Owing to the vast increase in the number of mobile telephones, there is an equally vast demand (and need) for means of making listening to third-party telephone conversations impossible, or at least difficult. Two such means are introduced here; both are compact and require only low power. One is based on the Type FX118 IC from Consumer Microcircuits Ltd (CML) in England and the other is the PCD4440 from Philips of Holland, which is programmable via an I²C bus.

Both ICs use the principle of frequency inversion. In this, the frequency band of 300–3000 (or 3500) Hz is inverted so that low frequencies become high and vice versa. Where the FX118 provides a simple inversion of the band, the PCD4440 is more sophisticated. This IC splits the speech band into two at a programmed frequency and then inverts both parts independently. Since the programmed frequency can have any one of nine values, this chip offers good protection against eavesdroppers. Even higher protection is possible if the programmed frequencies in the trans-

	FX118	PCD4440
Function	Speech-band scrambler	Split frequency speech band scrambler
Number of speech channels	Scrambler **and** descrambler	Scrambler **or** descrambler
Power supply	3–5.5 V (typ. 3.75 V)	2.8–6.0 V (typ. 5.0 V)
Current drain	4 mA (typ.)	Typ. 13 mA (muted: 2.2 mA)
Input impedance	10 MΩ (typ.)	Typ. 120 kΩ
Output impedance	200 Ω (typ.)	<1 kΩ
Frequency range	300–3000 Hz	300–3500 Hz
Transfer gain	0.5 dB (opamp gain = 0 dB)	0 dB (transparent mode: –3.5 dB)
Spurious signal attenuation	≥40 dB	≥40 dB
Programmable	No	Via I²C bus
Clock	internal 4.433619 (same crystal as colour TV receiver)	External, 3.579 MHz
Packaging	FX118DW: 16 pin SOIC FX118P: 16 pin DIL	8 pin SOIC

Table 1. Main parameters of FX118 and PCD4440 ICs.

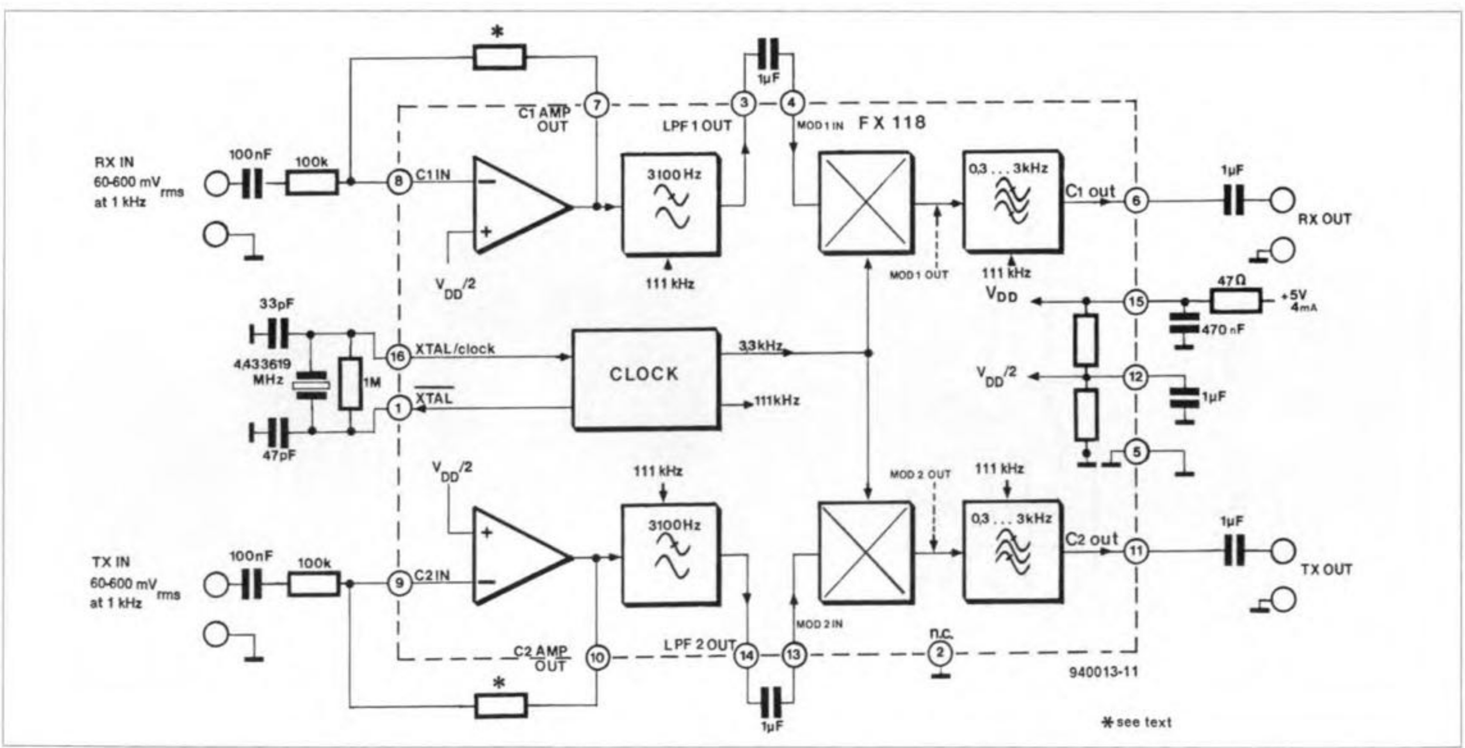

Fig. 1. Combined block and circuit diagram of the Type FX118 circuit.

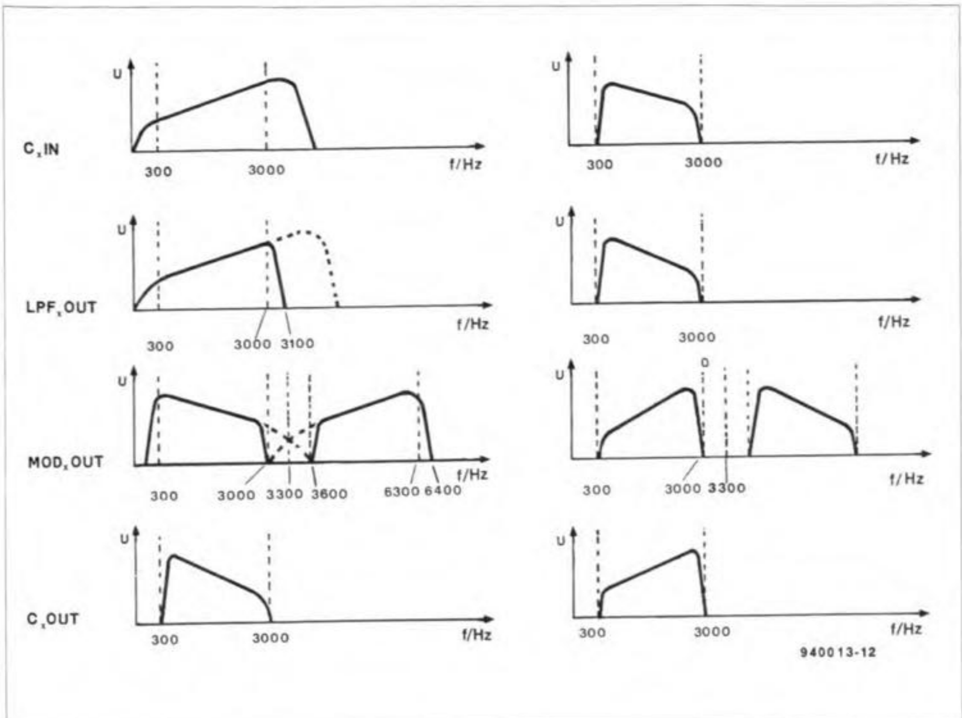

Fig. 2. Mode of operation of the FX118 (x: 1 for channel 1, 2 for channel 2).

mitter and receiver are synchronized. The programmed frequency can be changed ten times per second via the I^{2}C bus.

The filters in both circuits are switched-capacitor (SC) types, that are aligned simply by the application of the correct clock signal to the relevant pin on the circuit. Some parameters of both circuits are given in **Table 1**.

Frequency inverter FX118

A combined block and circuit diagram of duplex frequency inverter Type FX118 is given in **Fig. 1**. The circuit has two identical signal paths for scrambling and descrambling. The central clock, controlled by a 4.431619 MHz crystal, provides all internally required clock frequencies. The crystal has been chosen since it is the same as the inexpensive, easily obtainable one used in colour PAL TV receivers.

There is an amplifier in both signal paths, whose gain can be set by an external resistor. This enables the scrambler to work with input signals of 60–600 mV r.m.s.

The input amplifier is followed by a 3100 Hz low-pass filter. The output of the filter is applied to a frequency changer, which mixes it with a signal of 3300 Hz. This results in a sum and difference frequency band. The difference signal band has the desired inversion and is filtered out by a 300–3000 Hz band-pass filter.

The other signal path which, as already stated, is identical can be used simultaneously for descrambling. This is why the chip is called a duplex frequency inverter. One channel scrambles the outgoing signal, while the other channel descrambles the incoming signal. The mode of operation in scrambling is shown on the hand of the various signals in **Fig. 2a**. The speech signal applied to pin C$_x$IN (C$_1$IN or C$_2$IN) covers a frequency band of 300 Hz to about 5000 Hz. A low-pass filter removes all frequencies above 3100 Hz (LPF$_x$OUT). The resulting signal is mixed with a signal of 3300 Hz (MOD$_x$OUT), whereupon the original band is shifted to above 3300 Hz (sum signal). There is also a mirrored signal below 3300 Hz (difference signal), which has the desired frequency inversion. Because of the choice of 3300 Hz for the mixer frequency, the difference signal lies exactly in the band 300–3000 Hz. The following band-pass filter filters the 300–3000 Hz band from the output signal of the mixer (the sum signal is then eliminated) – C$_x$OUT.

Figure 2b shows how the descrambling of the scrambled signal is carried out.

Figure 3 shows the practical set-up of a radio telephone. Since each FX188 IC provides two signal paths (for scrambling and descrambling respectively), only one chip is required in the bases station and one in the handheld unit: full duplex operation.

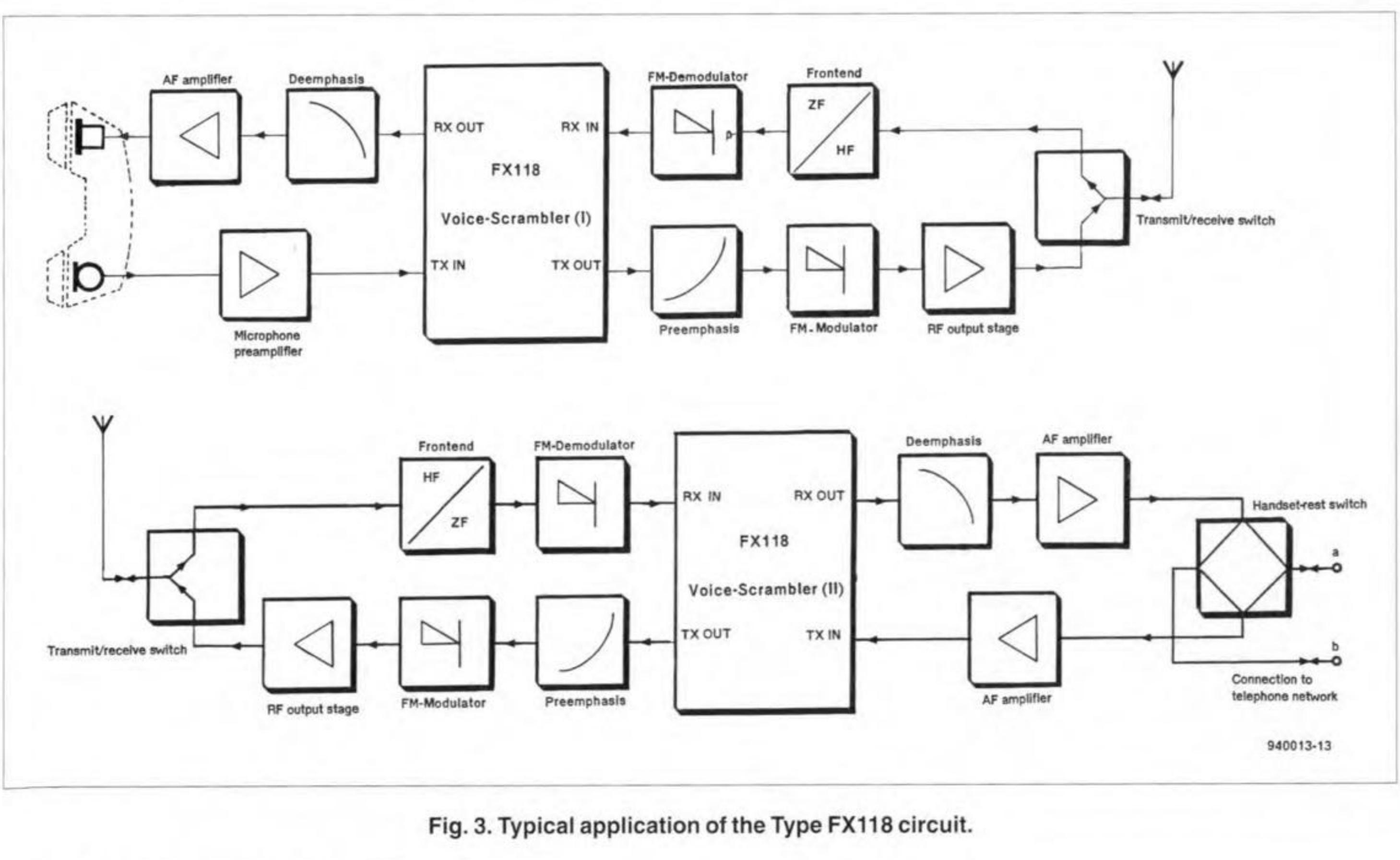

Fig. 3. Typical application of the Type FX118 circuit.

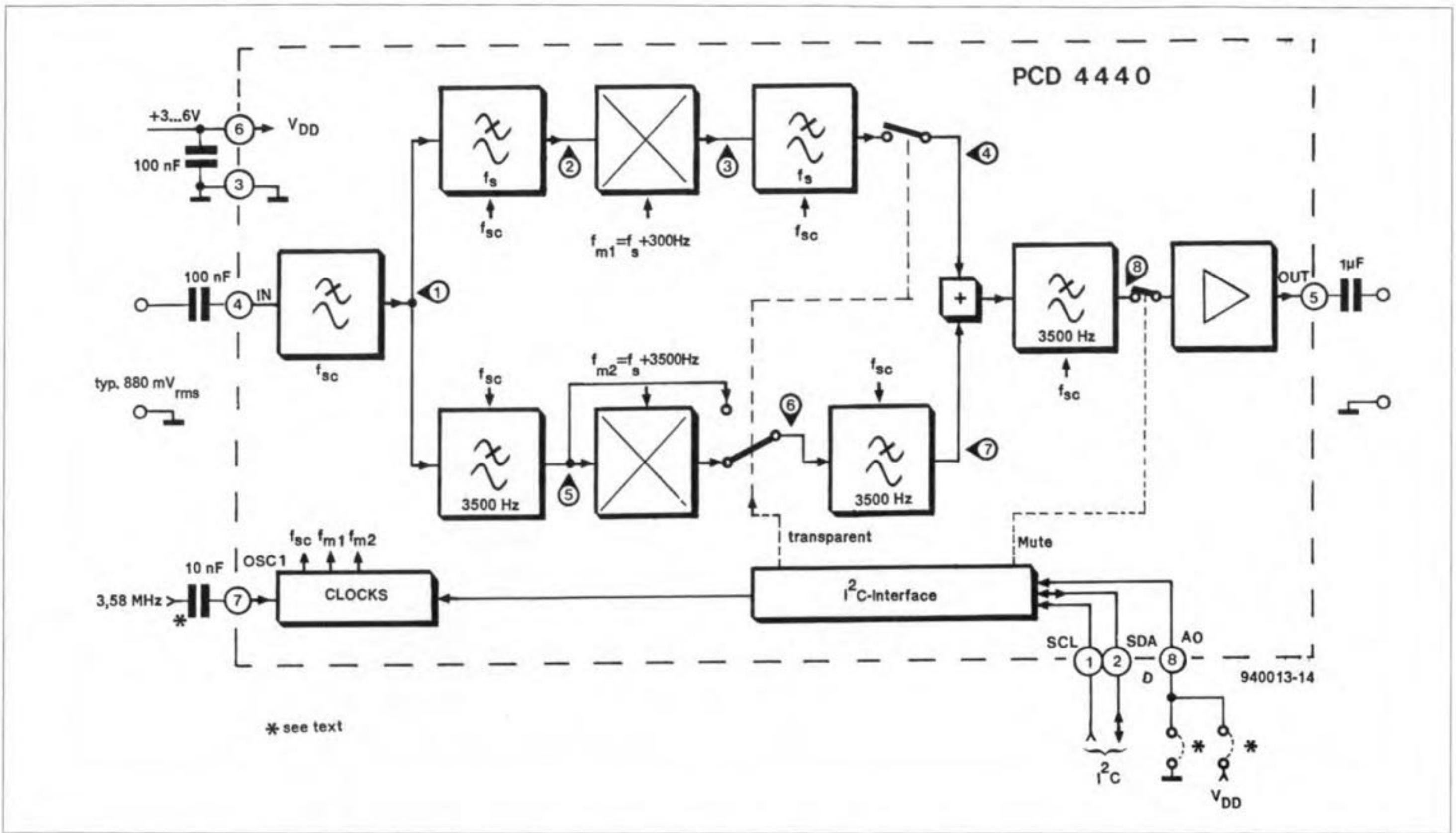

Fig. 4. Combined block and circuit diagram of the Type PCD4440 voice scrambler.

Communication is over two channels and uses frequency modulation. Noise suppression is effected by preamphasis at the transmitter and deemphasis at the receiver. High frequencies are amplified in the preemphasis network and attenuated again by the deemphasis network. Since in FM demodfulation the signal-to-noise ratio deteriorates with higher modulation frequencies, the preamphasis and demphasis networks ensure a level ratio.

Voice scrambler PCD4440

The PCD4440 chip, whose block and circuit diagram is shown in **Fig. 4**, provides only one audio channel. It uses split-frequency operation, in which the speech frequency band is split at a programmable frequency, f_s, after which the two parts are inverted separately. This does, of course, give a higher degree of protection than attainable with the FX118. If then f_s is changed a number of times per second, it becomes virtually impossible to eavesdrop on the communication. Programming of one of up to nine possible frequencies, f_s, takes place via an I²C bus. The chip also has the facilities to pass the speech band transparently, that is, without scrambling and to mute the output. For duplex operation, two PCD4440 chips are needed in both the receiver and the transmitter.

The input (**Fig. 5** ①) is applied to a low-pass filter, whose output is split over two signal paths. The upper path in **Fig. 4** processes the frequency band below f_s. This band is filtered out by a low-pass section whose cut-off frequency is f_s. This range of signals (**Fig. 5** ②) is applied to a frequency changer where it is mixed with a signal, f_{m1} (=f_s+300 Hz) (**Fig. 5** ③). The resulting (inverted) signal (**Fig. 5** ④) is passed through a further low-pass filter to ensure that any residual spurious signals are eliminated.

The upper part of ther speech band is applied to a low-pass filter in the lower signal path in **Fig. 4**, which has a cut-off frequency of 3500 Hz (**Fig.** 5 ⑤). Thereupon it is applied to a frequency changer where it is mixed with a signal, f_{m2} (=f_s+3500 Hz) (**Fig. 5** ⑥). The resulting signal is passed through a low-pass section which has a cut-off frequency of 3500 Hz (**Fig.5** ⑦).

The two (inverted) signals (**Fig. 5** ⑧) are then applied to yet another low-pass filter (cut-off frequency = 3500 Hz) and amplified.

In the transparent mode of operation, the upper signal path is disabled and the frequency changer in the lower path is by-

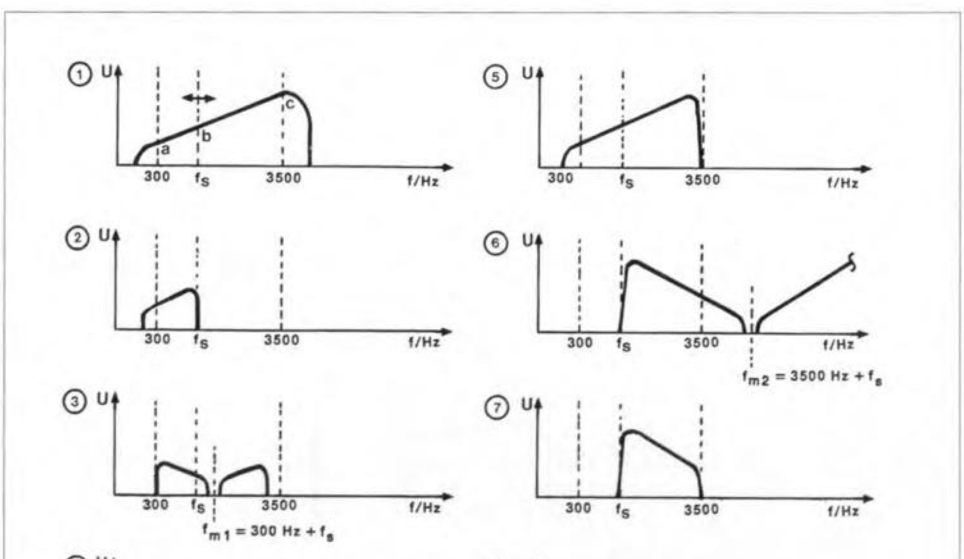

Fig. 5. Mode of operation of the PCD4440.

passed. This ensures that the input signal appears in unchanged form at the output. It is, however, passed through two low-pass sections which remove any residual signals above 3500 Hz.

In muted operation, the output signal is switched off.

The PCD4440 is programmed as follows. **Figure 6** shows two signals, SCL and SDA, which represent the I²C bus. SCL is a clock line that is driven continuously by the I²C transmitter. SDA is the directional data line that is driven by the transmitter or the receiver. In principle, both I²C parties can pull these lines to ground to obviate any short-circuits caused by simultaneous drives. As shown in **Fig. 7**, both lines must be connected to the +5 V supply via external pull-up resistors.

Figure 7 also shows how the PCD4440 is clocked. There is no facility to clock the PCD4440 via an independent crystal. It can, of course, be clocked by an independent, external quartz crystal oscillator.

The control via the I²C bus is always by an address followed by one or more data words. Receipt of each of these words is confirmed by the receiver via an acknowledge pulse. This indicates that the PCD4440 has pulled the SDA line low while the controller generates the SCL clock pulse. Each I²C communication is begun with a start state and ends with a stop state.

The start state (SDA goes low before SCL) is followed by the address of the PCD4440. Depending on the level at pin 8, this is 1101110 (A_0 = 0 V) or 1101111 (A_0 = 1). These addresses are individually allocated to the PCD4440, so that the chip can be combined with other ICs that are controlled via I²C.

The R/W (read/write) bit that follows the address is set to write (R/W = 0).

The acknowledge pulse is followed by a single data word. This data word contains four bits, D_3–D_0, which set the split frequency, f_s, as well as the special modes—see **Table 2**. After f_s has been programmed, the PCD4440 must be enabled by the start instruction (0F hex).

Function	f_s (Hz)	D_3	D_2	D_1	D_0
Mute		0	0	0	1
	2461	0	0	1	0
	1853	0	0	1	1
	1507	0	1	0	0
	1279	0	1	0	1
	1117	0	1	1	0
	1018	0	1	1	1
	899	1	0	0	0
	837	1	0	0	1
	767	1	0	1	0
Transparent		1	0	1	1
Start descramble/ scramble mode		1	1	1	1

Table 2. Programming of the PCD4440.

Summary

Both the FX118 and the PCD4440 circuits enable protection circuits to be designed for mobile telephones or other speech communication systems. Because of the use of switched capacitor (SC) filters, such circuits can be kept very compact; they need no alignment.

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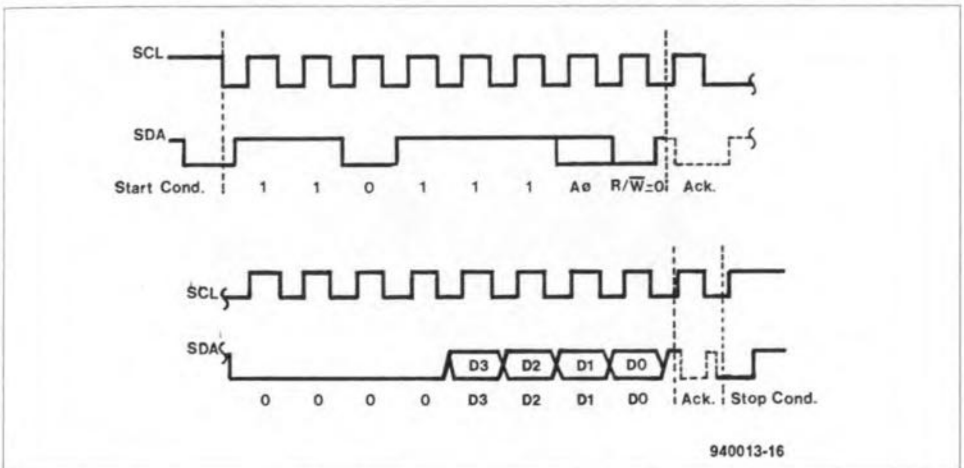

Fig. 6. I²C control of the PCD4440.

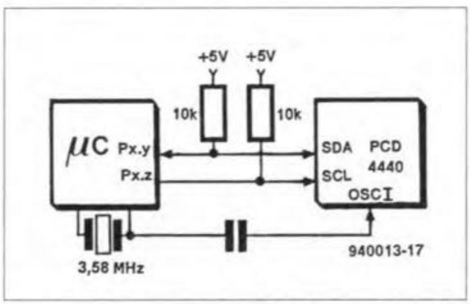

Fig. 7. Linking the PCD4440 to a microcontroller

IN-CAR AUDIO AMPLIFIER - PART 1

Design by T. Giesberts

The in-car audio amplifier is intended for public-minded drivers who not only love their in-car music, but also their hearing (and that of others), which is why they keep the volume of the car's audio system at reasonable volume levels – particularly when the car's windows are open. It is a sad fact that there are some unthinking drivers who do not realise that by having the volume fully up (or nearly so) they are destroying their hearing in a fairly short time (and at the same time, they are a public nuisance). By leaving the volume of your car's audio system at reasonable levels, you will be able to go on listening to your favourite in-car music long after the unthinking few have realised – sadly, too late – that all they can hear is a rushing in their ears – no more.

The aspect of an in-car audio amplifier that makes it so expensive is not the amplifier itself, but the power supply. In domestic or industrial amplifiers, it is possible to obtain any supply voltage we wish from the mains. In a car, however, there is only a 12 V battery and that puts severe limits on the amplifier's power requirements. Roughly, the output power of an amplifier, P, is $P = U_{pp}^2/8R_L$, where U_{pp} is the peak-to-peak supply voltage and R_L is the loudspeaker impedance. Even with 4 Ω loudspeakers and a battery voltage of 13.8 V, the peak power is just about 6 W. A bridge amplifier might increase this to about 20 W. Lowering the load impedance to 2 Ω by shunting loudspeakers, can double this figure to 40 W, but that is all. The only way of obtaining output powers of 100–200 W into 4 Ω is increasing the on-board voltage by a suitable d.c.-d.c. converter, which is the solution chosen for the present amplifier. The amplifier proper will be described this month and the converter next month.

Design considerations

The design of an in-car amplifier is rather different from that of a domestic power amplifier. This is because in the latter the major requirement is the best possible sound quality, which, to most hi-fi enthusiasts means very low distortion, high signal-to-noise ratio and a high slew-rate. In an in-car power amplifier, the main requirements are reliability, solidity, electrical and thermal stability, compactness, and, of course, good sound quality.

Other differences in the design of an in-car amplifier compared with that of a domestic amplifier are sensors for protection against a short-circuit of the output, too high temperatures and direct voltages at the output. Because of the inevitable high ambient temperatures in a car, the cooling of the heat sink mounted output transistors is ensured by an electric fan. Moreover, the output transistors are of a type that can withstand very low loads - down to 1 Ω. Nevertheless, the over-current protection circuit comes into operation at full drive when the load drops below 3 Ω.

Circuit description

Basically, the amplifier consists of a voltage amplifying section, T_1–T_{10}, and a current amplifying section, T_{11}–T_{18} (see **Fig. 2**). The section around T_{19}–T_{22} forms part of the protection circuits.

The signal from the (existing) car radio is applied to the amplifier via C_1. This capacitor is the only one in the signal path and it is, therefore, a good-quality (polypropylene) type. From C_1, the signal passes through a low-pass filter, R_2-C_2, which limits the bandwidth of the signal to a reasonable, practical value.

The input amplifier is a differential one formed by T_{1a} and T_{1b}. The type of transistor used, a MAT02, ensures optimum symmetry and minimal drift. The bandwidth is further limited by R_8-C_3. R_{10}-C_4 is a feedback network.

Zener diodes D_1 and D_2 protect T_1 against too high a collector-emitter potential and thus to a needlessly large dissipation.

The d.c. setting of the differential amplifier is provided by current source T_2. To ensure the highest possible stability, reference diode D_4 is thermally coupled to T_2. The current through the diode is held steady by current source T_3. It is important that the drop across D_4 is exactly 1.8 V, since this ensures the correct level of current through T_1, and thus the voltage drop (3.3 V) across R_6 and R_7. If the drop across D_4 is not exactly 1.8 V, the d.c. setting can

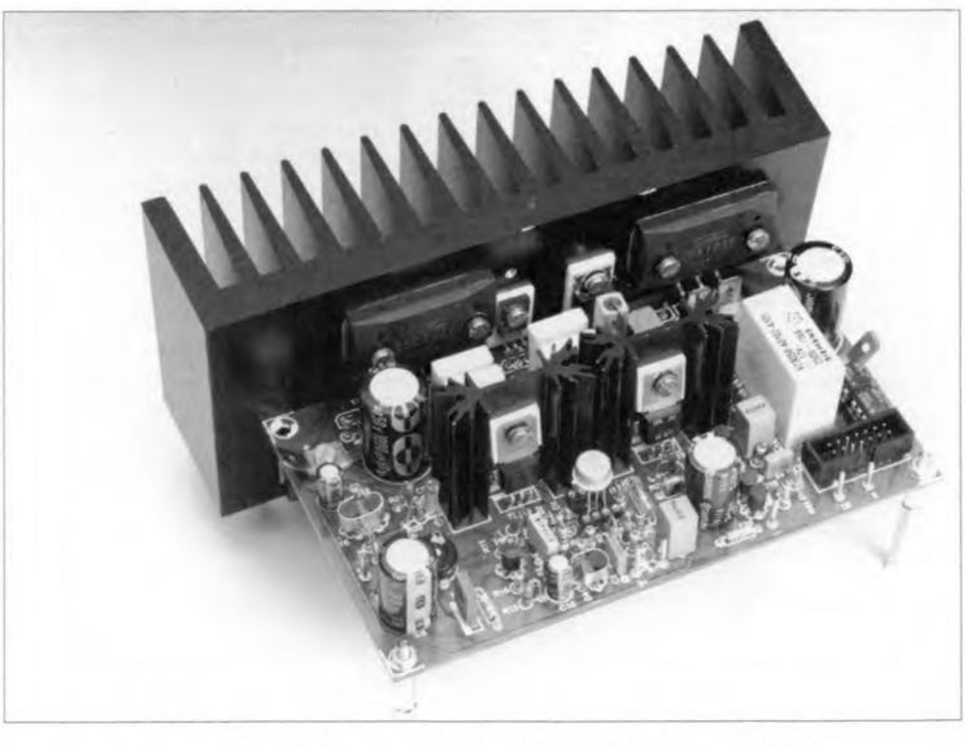

Fig. 1. Completed (mono) prototype amplifier (fan not shown).

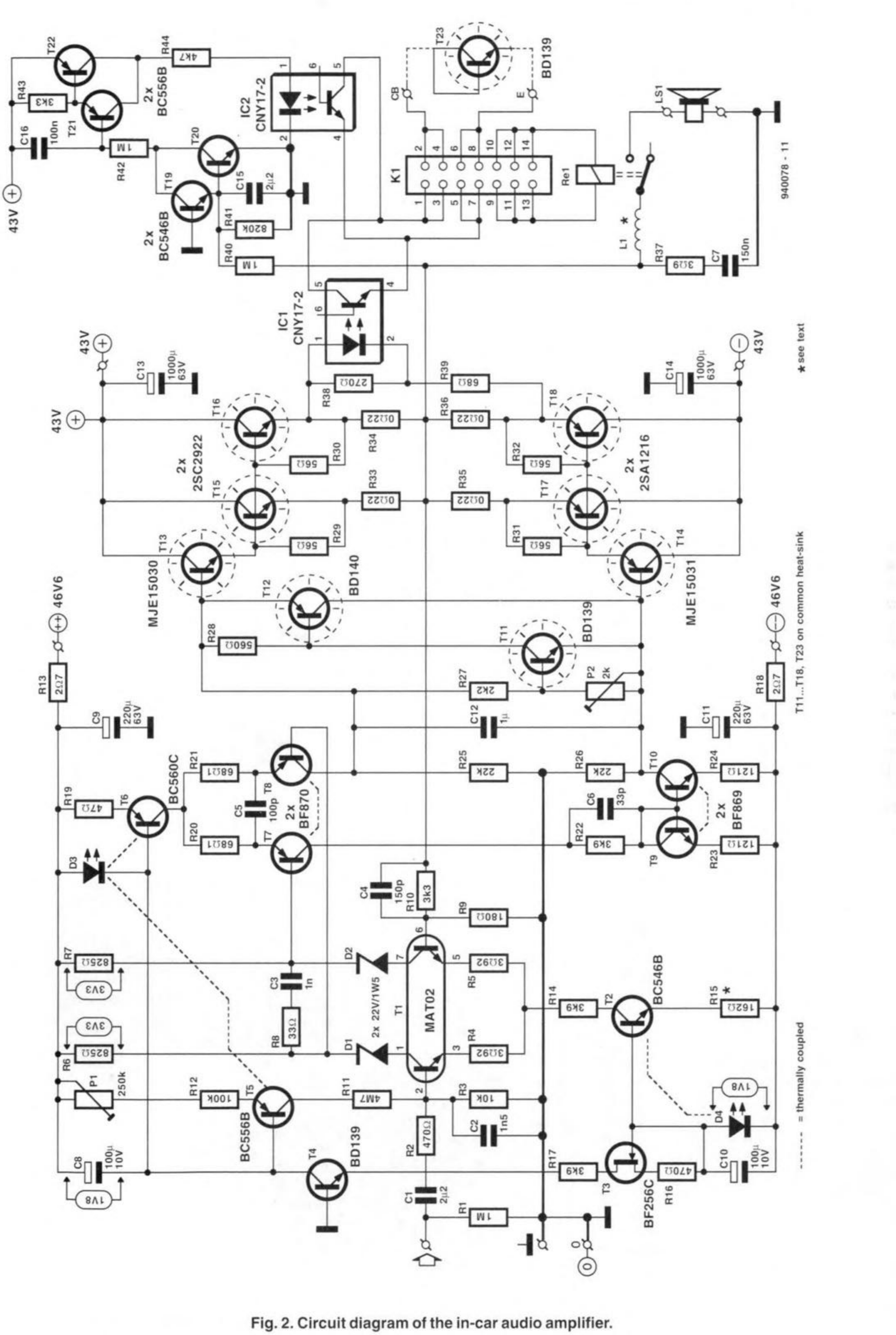

Fig. 2. Circuit diagram of the in-car audio amplifier.

be corrected by (empirically) altering the value of R_{15} slightly.

Current source T_3 also holds the voltage across D_3 constant at 1.8 V. This diode serves as reference for current source T_5 and is also part of another current source, T_6. It is, therefore, thermally coupled to both transistors.

Current source T_5 ensures that the bias current for T_1 is held at a steady level. It also provides, with R_{12} and P_1, a d.c. offset control.

Current source T_6 provides the d.c. operating point of differential amplifier T_7-T_8. This amplifier is augmented by current mirror T_9-T_{10} to ensure a symmetrical drive to the current amplifier. Capacitor C_5 provides frequency correction.

The current amplifier consists of two complementary emitter followers, T_{13} and T_{14}, and parallel-connected power stages T_{15}-T_{16} (n-p-n) and T_{17}-T_{18} (p-n-p). Variable 'zener diode' T_{11}-T_{12} provides precise control of the voltage across T_{13}–T_{18} and R_{33}–R_{36}. This voltage determines the quiescent current through the power transistors. Transistors T_{11}–T_{18} are mounted on a common heat sink to ensure good thermal coupling, so that the quiescent current remains stable even with rising temperature.

The level of the quiescent current (100 mA per transistor) enables the amplifier to process small signals in Class A (0.3 W into 4 Ω).

Capacitors C_{13} and C_{14} ensure sufficient spare current during short signal peaks.

Boucherot network R_{37}-C_7 at the output ensures that the amplifier is loaded even at very high frequencies.

Inductor L_1 limits current peaks that ensue with highly capacitive output loads.

Protection

The supply to the amplifier consists of two different symmetrical voltages: ±43 V for the current amplifier and ±46.6 V for the voltage

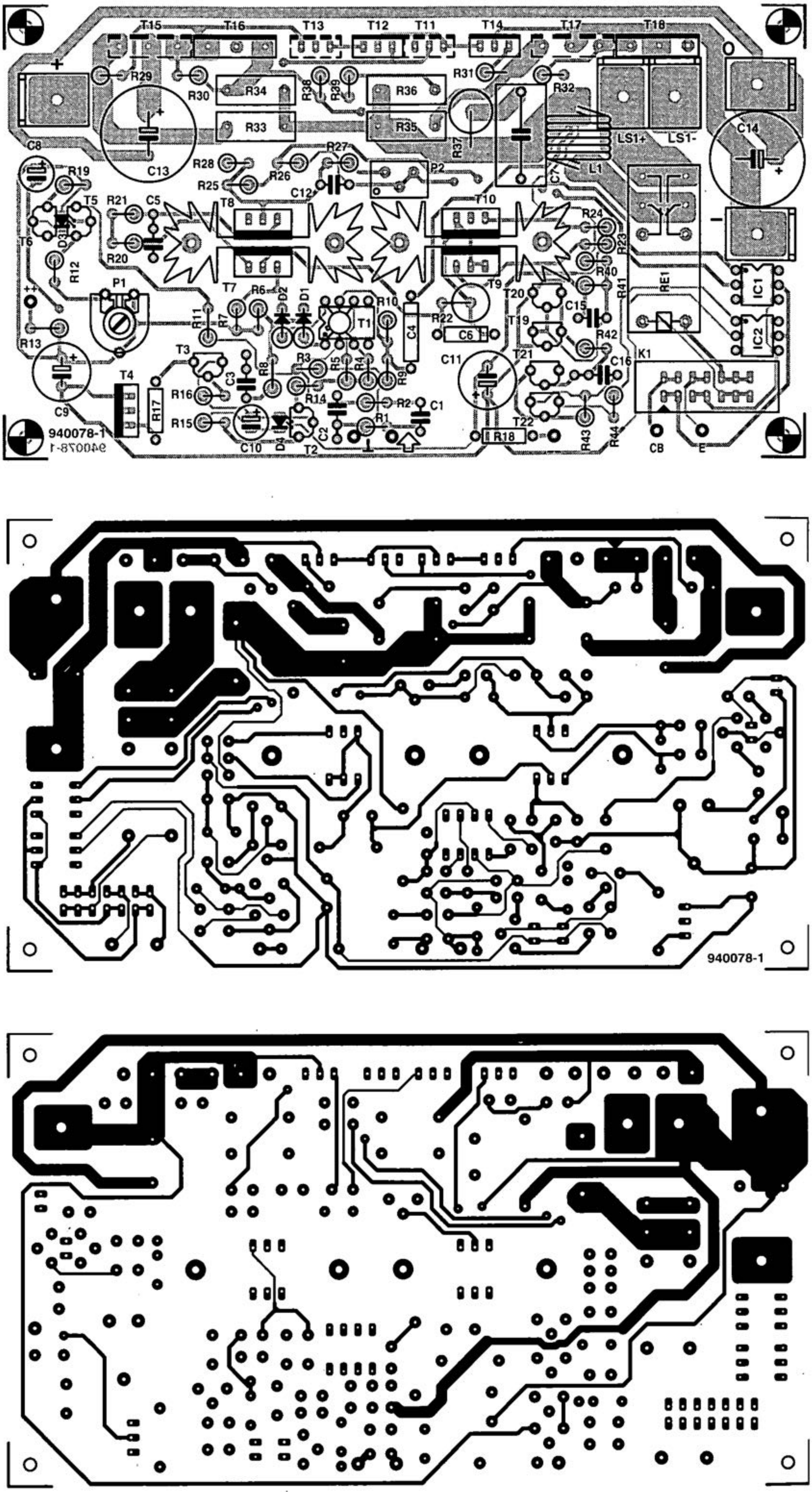

Fig. 3. Printed circuit board for the in-car audio amplifier (2 needed for stereo version).

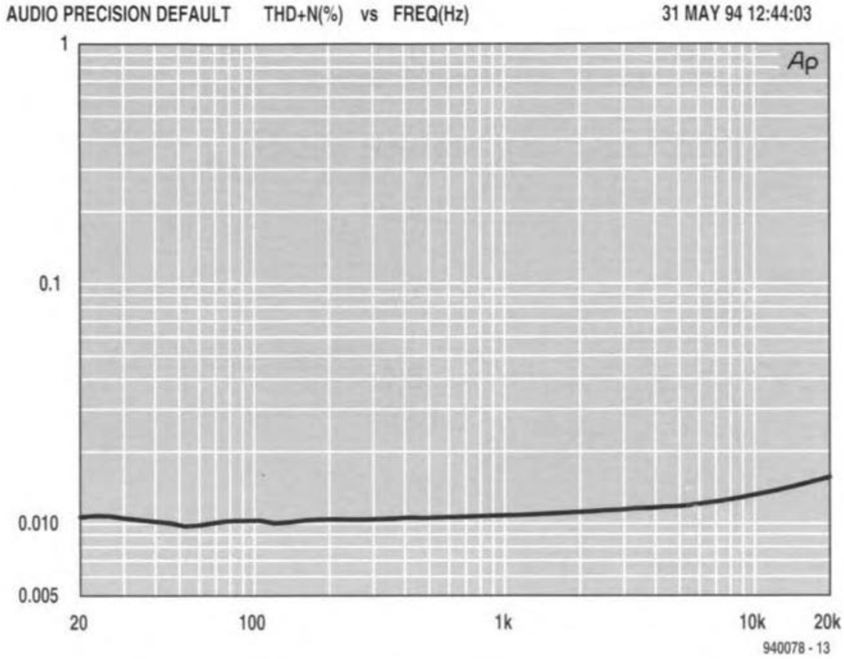

Fig. 4. Harmonic distortion vs frequency characteristic.

amplifier. The slightly higher supply to the voltage amplifier compensates for the inevitable drops, so that the current amplifier can be driven to its maximum supply voltage.

The supply voltages are generated by the converter to be described, together with the complete protection circuits, in Part 2. The sensors for the protection circuits are, however, located on the amplifier board, and these will be briefly discussed here.

In parallel with the emitter resistors of T_{16} and T_{17} is a potential divider, R_{38}-R_{39}, which controls optoisolator IC_1. When the amplifier is overdriven, or the load drops below 3 Ω, or the output is short-circuited, the output current rises above 13.5 A, whereupon the drop across R_{38} will cause the optoisolator to conduct.

The circuit based on T_{19}-T_{20} controls optoisolator IC_2, which is coupled to the amplifier output via R_{40}. When a direct voltage exceeding ±1 V appears on the amplifier output, the optoisolator will be switched on: by T_{20} when the direct voltage is positive, and by T_{19} when the direct voltage is negative.

Transistor T_{23} is a temperature monitor.

The three sensor outputs are taken to the protection circuit via box header K_1. When one of the three sensors is actuated, the associated protection circuit deenergizes relay Re_1, which thereupon disconnects the loudspeaker from the amplifier output.

The protection circuits are electrically isolated from the amplifier to prevent the converter causing possible earth loops between them and the source (car radio)

Construction

The amplifier is best built on the (double-sided) printed-circuit board in **Fig. 3**. Note that this board is for a mono version; for a stereo version two boards are needed.

Most resistors must be mounted upright. Inductor L_1 is self-wound. Close-wind six turns of 1.5 mm diameter enamelled copper wire on an 8 mm dia. former (e.g., a pencil). Clean both ends for soldering and remove the former.

Diode D_4 and transistor T_2, as well as transistors T_5, T_6 and diode D_3 must be sandwiched together (flat side of the diodes against the transistor(s). Clamp the combinations together with a strip of copper or tin plate to ensure good thermal coupling. Note that the LEDs must be types that drop exactly 1.8 V when the current through them is 5 mA (check this with a suitable supply and a series resistor).

The 43 V supply lines ('+', '0', '–'), as well as the loudspeaker leads, must be connected to the board(s) via heavy-duty car-type connectors (rated at 25–30 A). The 46.6 V lines ('++','⊥', and '—') carry only small currents and can thus be soldered to standard solder pins.

The heat sink on which T_7-T_8 and T_9-T_{10} are fixed (insulated with ceramic washers and heat transfer paste) must be soldered at right angles to the board(s) with the aid of solder pins (see **Fig. 1**).

Mount T_{11}, T_{13}, T_{15}, and T_{17} to the track side of the board and T_{12}, T_{14}, T_{16}

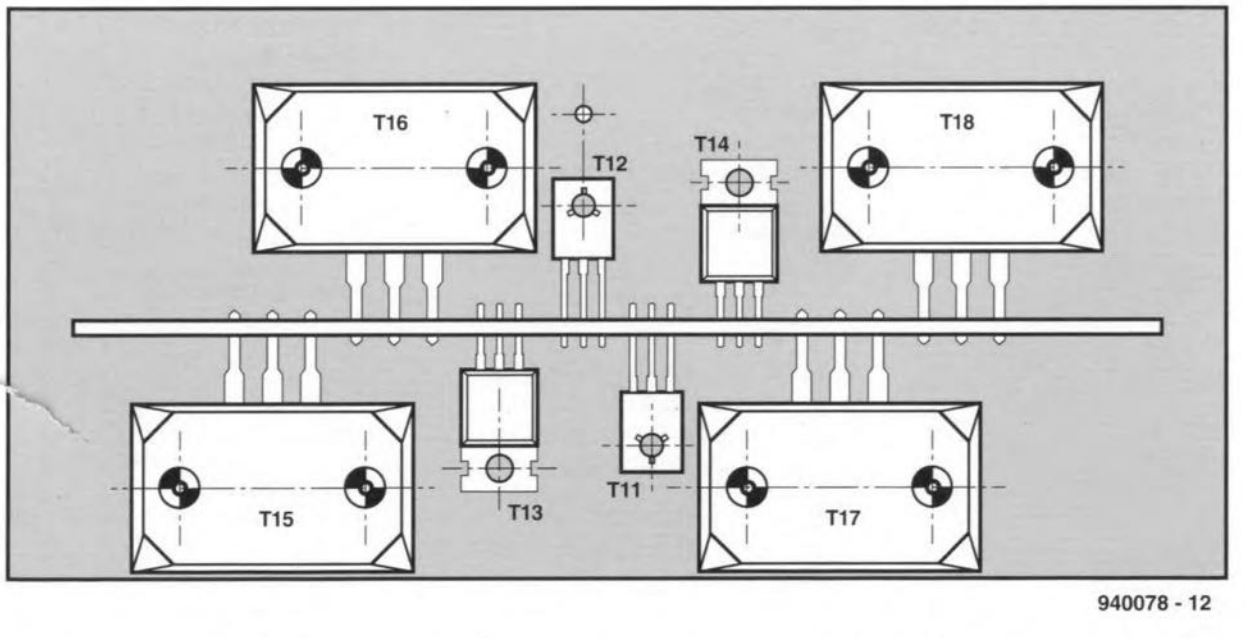

Fig. 5. Template for drilling the heat sink; scale 1:1 (width = 160 mm)

and T_{18} to the component side. Then, attach the board at right angles to the relevant heat sink as shown in **Fig. 1** and **4**. **Figure 4** may also be used as template for drilling the necessary holes. All these transistors must be insulated from the heat sink with ceramic washers and heat transfer paste. It may be difficult or even impossible to obtain ceramic washers for T_{15}–T_{18}; if so, use mica washers. Note that the specified heat sink allows the amplifier to provide an output of not more than 120 W into 4 Ω at an ambient temperature of 30 °C (which is not very high in a car in summer). The full power (200 W into 4 Ω) can only be realised when forced cooling is used.

Parts list

Resistors:

R_1, R_{40}, R_{42} = 1 MΩ
R_2, R_{16} = 470 Ω
R_3 = 10 kΩ
R_4, R_5 = 3.92 Ω, 1%
R_6, R_7 = 825 Ω, 1%
R_8 = 33 Ω
R_9 = 180 Ω
R_{10}, R_{43} = 3.3 kΩ
R_{11} = 4.7 MΩ
R_{12} = 100 kΩ
R_{13}, R_{18} = 2.7 Ω
R_{14}, R_{17} = 3.9 kΩ
R_{15} = 162 Ω, 1% – see text
R_{19} = 47 Ω
R_{20}, R_{21} = 68.1 Ω, 1%
R_{22} = 3.9 kΩ, 1 W
R_{23}, R_{24} = 121 Ω, 1%
R_{25}, R_{26} = 22 kΩ
R_{27} = 2.2 kΩ
R_{28} = 560 Ω
R_{29}–R_{32} = 56 Ω
R_{33}–R_{36} = 0.22 Ω, 5 W, low inductance
R_{37} = 3.9 Ω, 5 W
R_{38} = 270 Ω
R_{39} = 68 Ω
R_{41} = 820 kΩ
R_{44} = 4.7 kΩ
P_1 = 220 (250) kΩ preset
P_2 = 2 kΩ multiturn preset, vertical

Capacitors:

C_1, C_{15} = 2.2 μF, polypropylene, pitch 5 mm
C_2 = 1.5 nF
C_3 = 1 nF
C_4 = 150 pF, 160 V, polystyrene
C_5 = 100 pF, 160 V, polystyrene
C_6 = 33 pF, 160 V, polystyrene
C_7 = 150 nF, 160 V, polypropylene
C_8, C_{10} = 100 μF, 10 v, radial
C_9, C_{11} = 220 μF, 63 V, radial
C_{12} = 1 μF, polypropylene, pitch 5 mm
C_{13}, C_{14} = 1000 μF, 63 V, radial
C_{16} = 100 nF

Semiconductors:

D_1, D_2 = zener, 22 V, 1.5 W
D_3, D_4 = LED, flat, (U_{drop} = 1.8 V)
T_1 = MAT02
T_2, T_{19}, T_{20} = BC546B
T_3 = BF256C
T_4, T_{11}, T_{23} = BD139
T_5, T_{21}, T_{22} = BC556B
T_6 = BC560C
T_7, T_8 = BF870 (BF872)
T_9, T_{10} = BF869 (BF871)
T_{12} = BD140
T_{13} = MJE15030
T_{14} = MJE15031
T_{15}, T_{16} = 2SC2922
T_{17}, T_{18} = 2SA1216

Integrated circuits:

IC_1, IC_2 = CNY17-2

Miscellaneous:

L_1 = see text for winding instructions
K_1 = 14-way straight box header
Re_1 = 12 V, car type relay with two change-over contacts rated at 16 A
Five car-type heavy-duty plug/socket sets(plugs to be screw on type for PCB fitting)
Two off heat sink 11 K W^{-1} (38.1 mm) for T_7-T_8 and T_9-T_{10}
Heat sink 0.5 K W^{-1} (see text)
Two off 12 V, 230 mA fan (Canon CF80-T211N1D or similar)

[940078-I]

ELECTRONIC KNOW-HOW

Transformers – an overview

By K. Schönhoff

The development of transformers is closely connected with the history of alternating voltage. It was the Danish physicist Hans Christian Oersted who discovered in 1820 that a current-carrying conductor produces a magnetic field. Ten years later, the American physicist Josef Henry discovered electromagnetic induction, the 'conversion of magnetism into electricity'. In late 1831, Michael Faraday conducted a series of experiments with a device that consisted of an iron toroid around which two windings of insulated copper wire had been placed (see **Fig. 1**). He connected a battery to one of the windings and hoped that a direct voltage would be inducted in the other winding. But to his surprise, even after two hunded experiments, the only time the galvanometer across winding B deflected was when he connected or disconnected the battery from winding A. It was only after the French instrument maker, Pixii, in 1832, built a hand-operated alternating voltage generator (alternator) that the transformer could be further reasearched and developed.

Early researchers, who applied alternating voltage across an inductance, and measured the consequent voltage and current, discovered that the electrical resistance of a coil changes when an iron rod was inserted into it. This resistance increased further when the iron was formed into a closed circuit. The kind of iron also had an effect on the resistance: this was greatest with soft iron (i.e, iron low in carbon, which is unable to retain magnetism). If a second winding was placed over the iron, but insulated from the first winding, it was found that if an alternating voltage was applied across the first winding, an alternating voltage was induced in the second winding. The secondary voltage was found to be high when the winding consisted of many turns.

Transformer core

The iron core improves the transformer action in two respects. Firstly, it increases the electrical resistance of the winding to an applied alternating voltage. The current in an air-cored coil to which an alternating voltage is applied increases about four times as fast as in an iron-cored coil. Secondly, the iron contains many small magnets which are normally so distributed that their actions cancel one another. They are, however, mobile and can be placed in such a position by an external field that they magnify this field. This magnified field produces a much greater self inductance.

Eddy currents

The iron core of a transformer is an electrical conductor. The outer periphery of the core forms a closed loop and acts thus just like a turn of the winding. This means that a voltage is induced across it and a current flows through it. The core consists of many such closed loops in which small currents, so-called Eddy current, flow. These currents cause power dissipation (loss), which is noticeable by the warming of the transformer during operation.

This power loss is minimized by making the core not of solid iron, but of thin wafers of steel, laminations, which are electrically insulated from one another. Moreover, the electrical resistance of the laminations is increased by the addition of a small amount of silicon to the steel.

The insulation between the laminations consists of a 6–10 μm thick, single-sided layer of varnish, a 2–3 μm thick double-sided coating of phosphate, or a 2–3 μm thick oxide coating.

The space factor, that is, the ratio of the active cross-sectional area to the total area, varies from 0.75 (lamination thickness 0.05 mm) to 0.92 (lamination thickness 0.5 mm).

The diameter of some common

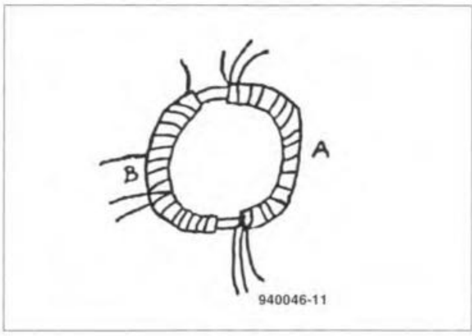

Fig. 1

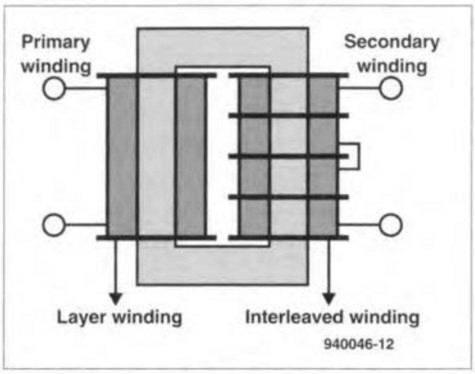

Fig. 2

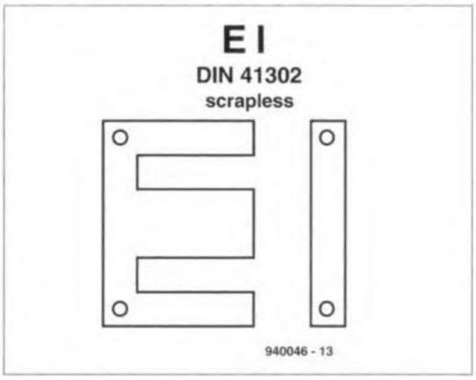

Fig. 3

Insulation		Wire diameter in mm			
		0.1	0.5	1	5
enamel	single	0.011	0.028	0.040	0.060
	double	0.021	0.045	0.065	0.100
rayon	single	0.05	0.06	0.07	
	double	0.09	0.11	0.12	
cotton	single		0.10	0.12	
	double		0.16	0.22	0.40
paper	single		0.12	0.12	0.20
	double		0.22	0.22	0.35

Table 1. Diameter of some commonly encountered winding wire.

Fig. 4.

Fig. 5

Fig. 6

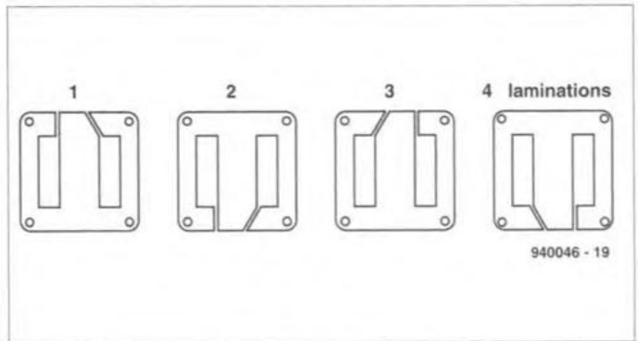

Fig. 7

winding wire is given in Table 1.

Saturation

When the current through the primary winding increases, the field strength and the magnetization of the core also increase. However, at a certain level of current, the magnetization no longer increases: the core is saturated, but the (weak) field around the transformer becomes stronger. This stray field can cause interference in electronic circuits. Moreover, the energy transfer to the secondary winding deteriorates, because not all the lines of force produced by the primary embrace the secondary.

The stray field is particularly bothersome when the primary and secondary are relatively far from each other, as on a UI core. It is not so strong when the windings are adjacent on the same limb of the core, and weaker still when the windings are on top of one another, as in most transformers.

Two properties of the core are particularly important for computing a transformer design: the degree to which it can be magnetized before saturation occurs and the permeability, that is, the degree to which it magnifies an external field. These factors determine the number of turns required for a certain voltage. The higher the magnetizability, the fewer turns are needed in both windings. The number of turns also depends on the cross-sectional area of the core and the form factor of the transformer.

Laminations

Originally, transformers were needed to provide relatively high power for energy supply systems. They used a rectangular core with well separated windings (see **Fig. 2**): this ensured good electrical isolation. The windings invariably consisted of cotton-insulated copper wire. In case of a failure, each of the windings could be removed and repaired or replaced.

When, later, transformers were needed for powering small equipment, their designs started to use so-called shell-type cores—see **Fig. 3**. Shell-type cores are sub-divided into EI, M and F types, according to their shape.

The EI type is particularly suitable for transformers that need a small air gap (down to 10 μm). The output voltage of such transformers is load-dependent, which is, for instance, useful in battery chargers that must deliver a constant current. This type of transformer is also useful in amplifiers. In a single-ended class A output stage flows

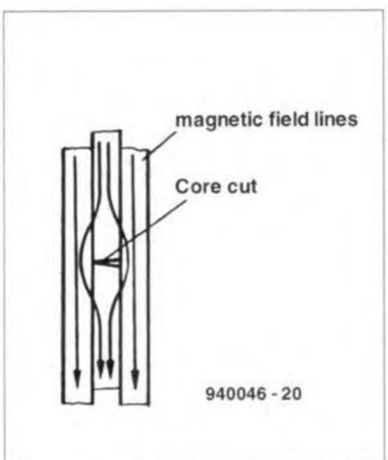

Fig. 8

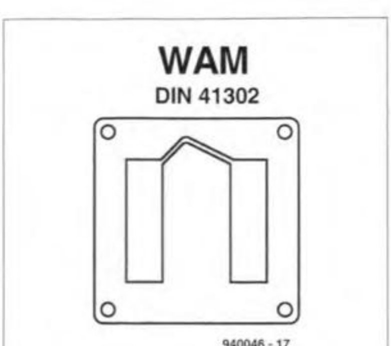

Fig. 9

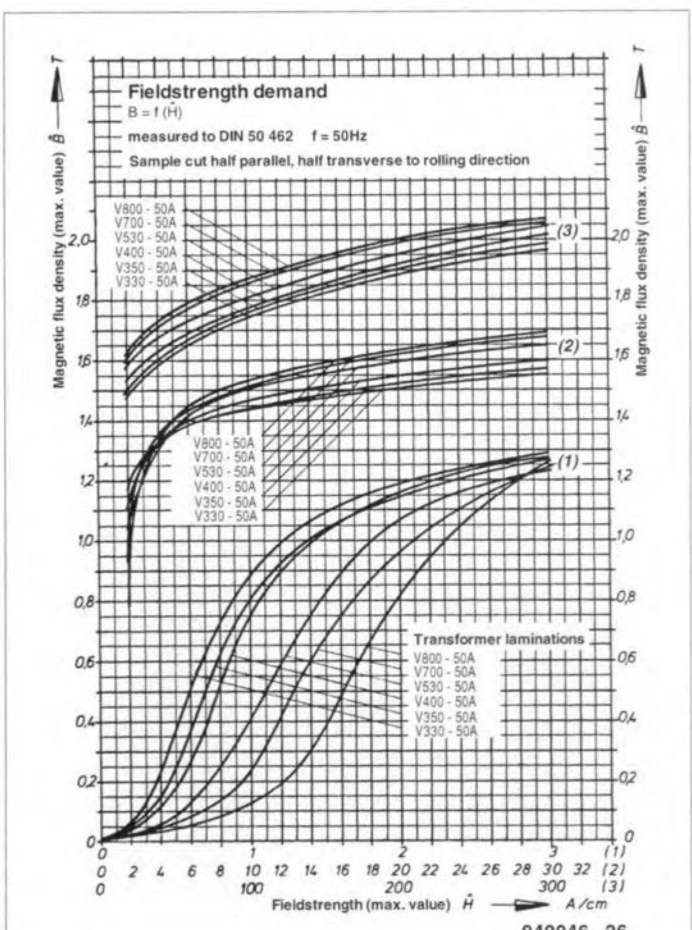

Fig. 10

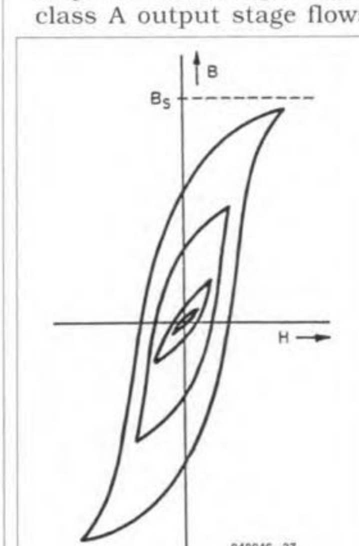

Fig. 11

Table 2. Electrical data for transformers with M and EI cores (EI=scrapless). [Laminations Type V170-50A to DIN 41 302, Part 2 (η = 0.94)]. These are but two of the many tables contained in transformer design books.

Type & size		Secondary poweros cos φ = 1	Magnetic flux $\hat{B}_N$	Current density S_N	Reactive power P_b	Iron losses P_{Fe}	Copper losses P_{Cuw}	Current factor Δ_i	Voltage factor Δ_u	Effective efficiency η_W	Apparent efficiency η_S	Power factor cos φ	Thermal resistance: For copper losses R_{ThCu}	Thermal resistance: For iron losses R_{ThFe}
		W	T	A/mm²	V · A	W	W	–	–	–	–	–	K/W	K/W
M 42		3,94	1,37	6,7	4,31	0,68	3,81	1,365	1,76	0,467	0,416	0,89	22,6	10,8
M 55		15,8	1,38	4,97	11,6	1,78	5,7	1,267	1,301	0,68	0,61	0,89	14,1	6,4
M 65		34,1	1,39	4,1	21,5	3,25	7,6	1,228	1,188	0,76	0,69	0,9	10,2	4,45
M 74		62	1,39	3,51	34,5	5,2	9,3	1,198	1,13	0,81	0,74	0,91	7,9	3,35
M 85	a	82	1,37	3,47	43,2	6,9	10,4	1,189	1,111	0,83	0,76	0,92	6,8	2,8
	b	108	1,33	3,31	51	9,1	10,9	1,17	1,09	0,84	0,78	0,93	6,1	2,5
M 102	a	143	1,42	2,94	67	10,8	13,5	1,163	1,084	0,85	0,79	0,93	5	2,02
	b	198	1,31	2,76	79	14,6	14,1	1,139	1,065	0,87	0,82	0,94	4,45	1,75

Type & size		Secondary power cosφ = 1	Magnetic fluxe $\hat{B}_N$	Current density S_N	Reactive power P_b	Iron losses P_{Fe}	Copper losses P_{Cuw}	Current factor Δ_i	Voltage factor Δ_u	Effective efficiency η_W	Apparent efficiency η_S	Power factor cos φ	Thermal resistance: For copper losses R_{ThCu}	Thermal resistance: For iron lossesr R_{ThFe}
		W	T	A/mm²	V · A	W	W	–	–	–	–	–	K/W	K/W
M 42		4,05	1,38	6,8	4,53	0,51	3,91	1,348	1,76	0,478	0,421	0,88	22,6	10,8
M 55		16,4	1,4	5,1	12,7	1,36	6	1,262	1,301	0,69	0,61	0,88	14,1	6,4
M 65		35,7	1,42	4,21	24,4	2,5	8	1,231	1,188	0,77	0,68	0,88	10,2	4,45
M 74		65	1,43	3,62	40,8	4,06	9,9	1,208	1,129	0,82	0,73	0,89	7,9	3,35
M 85	a	87	1,41	3,6	53	5,5	11,2	1,204	1,109	0,84	0,75	0,89	6,8	2,8
	b	116	1,39	3,44	66	7,5	11,8	1,193	1,087	0,86	0,77	0,9	6,1	2,5
M 102	a	154	1,42	3,05	86	8,7	14,6	1,184	1,083	0,87	0,78	0,9	5	2,02
	b	215	1,39	2,87	111	12,4	15,2	1,169	1,062	0,89	0,81	0,91	4,45	1,75

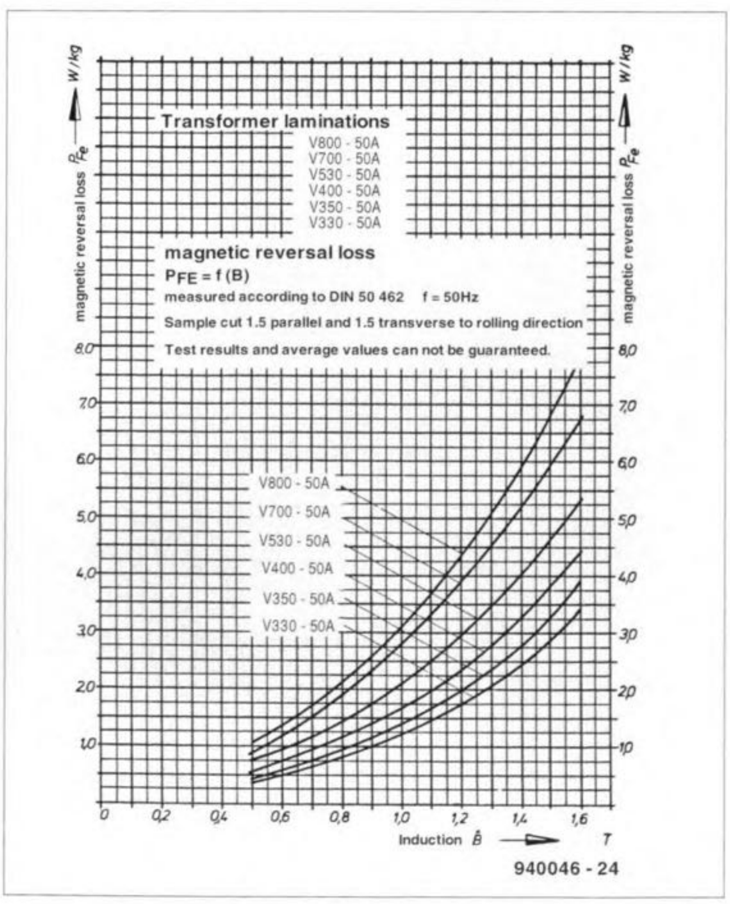

Fig. 12

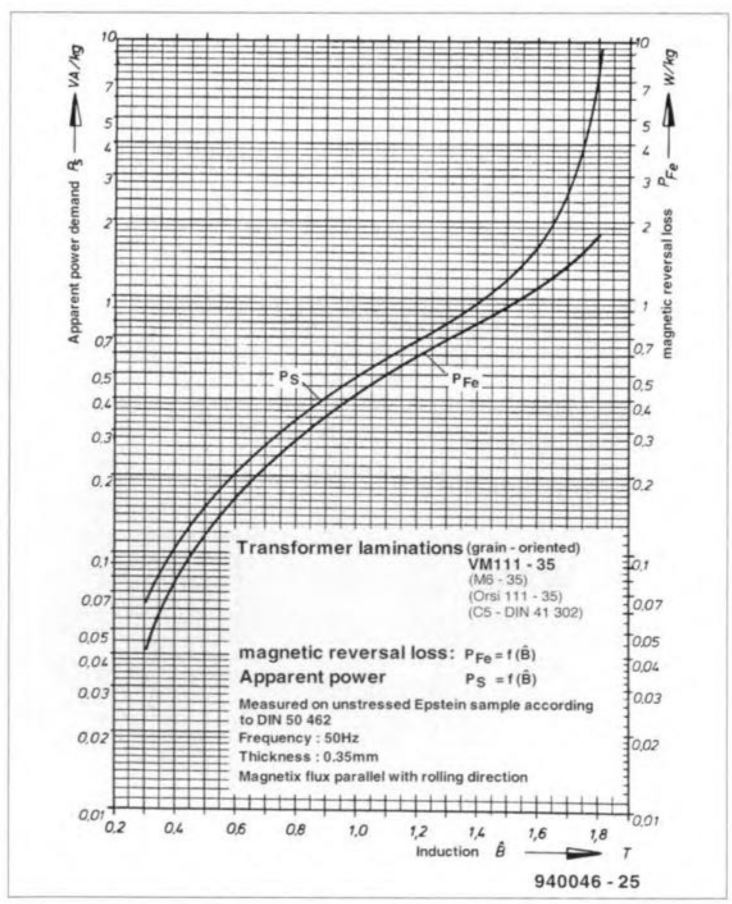

Fig. 13

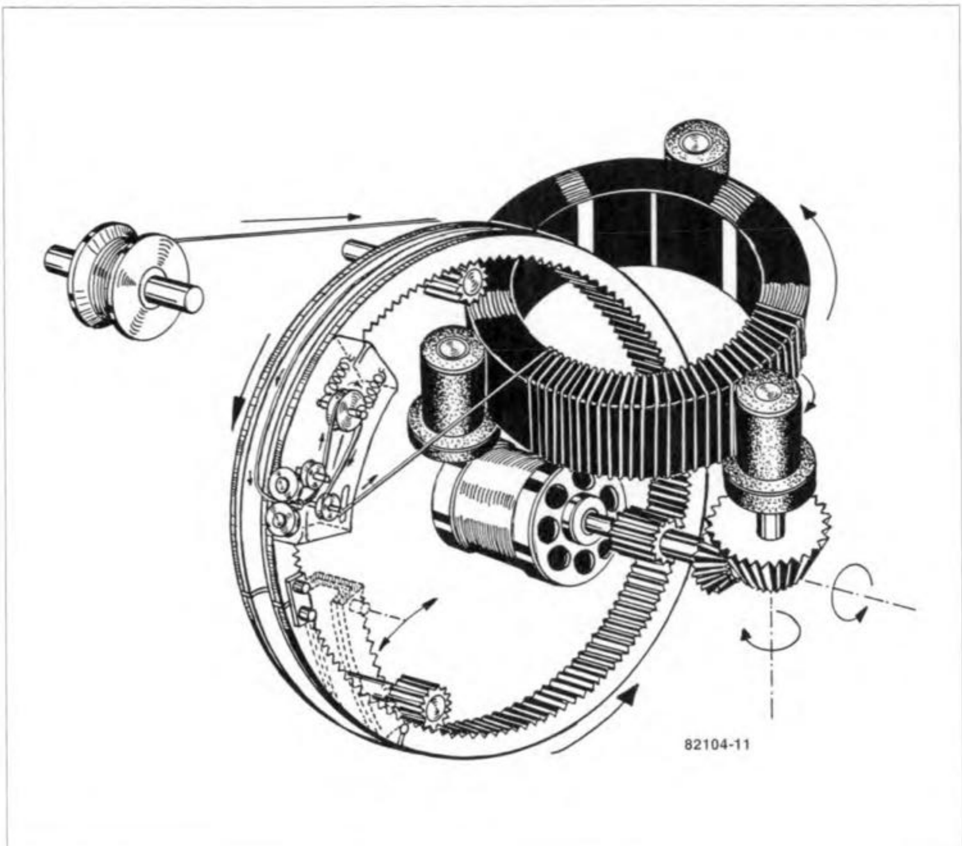

Fig. 14

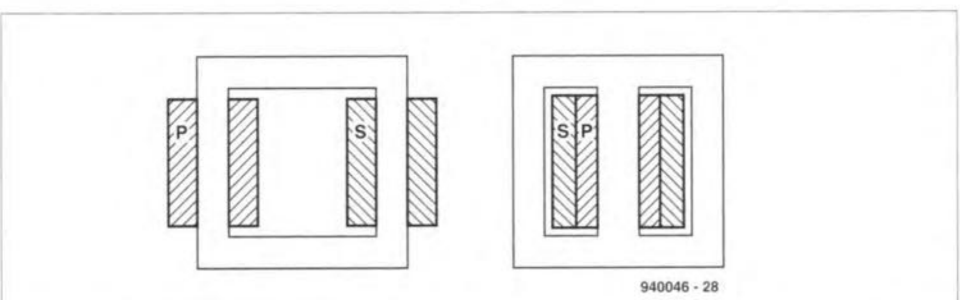

Fig. 15

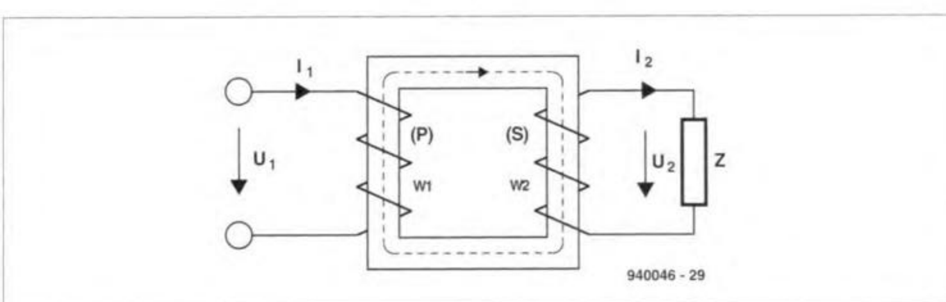

Fig. 16

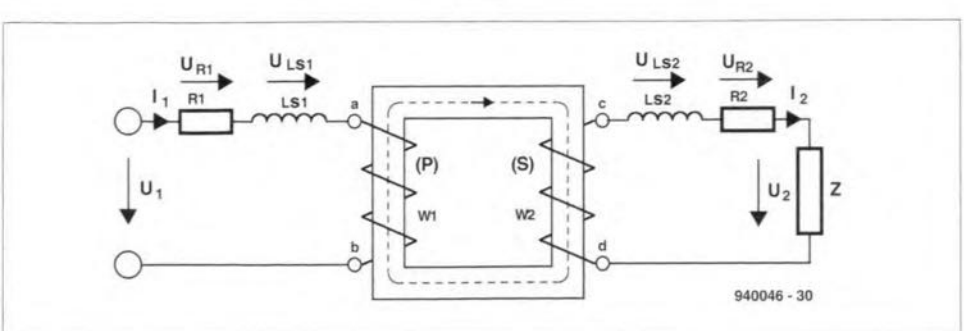

Fig. 17

not only alternating, but also direct current. The air gap prevents the direct current pre-magnetizing the core, which then may become saturated when the alternating current begins to flow or increases.

The M type cored transformer—see **Fig. 4**— is intended mainly for special applications, where its relatively strong stray field does not matter.

Capacity improvement

Special alloys for the laminations coupled with particular rolling processes have improved magnetic properties considerably. In grain-oriented core materials, the grains are oriented by cold rolling of the material. They are aligned in the same direction as the magnetic flux established in the laminations. This improves the parallel, but not the transverse, magnetizability.

In the MD core—see **Fig. 5**—which made its appearance in the 1960s, the transverse magnetizability is also improved. In this core, the effect of the air gap is reduced by aligning the lamination joints in the direction of minimum flux density.

The PM core—see **Fig. 6**—is a further enhancement of the M type. Its improvements include a widening of the outer shell compared with the inner shell, which results in a weaker magnetization of the outer limbs than in the centre limb. Also, strengthening of the limbs results in a smaller magnetic resistance, so that the core can contain more lines of force, which reduces losses. Moreover, the arrangements of the laminations in layers of four—see **Fig. 7**—means that each air gap is flanked at either side by three closed loops (laminations) that act as diversion for the lines of force (see **Fig. 8**). These improvements mean an even better efficiency and weaker stray field than obtainable with the MD core.

A few years ago, the PM core was itself improved by a longitudinal shift of the winding window and optimization of the air gap to raise the efficiency by a further few per cent.

Apart from the standard types, there are several special types from a number of manufacturers, such as that in **Fig. 9**. The manufacturer states that this has the same good properties of the PM types, but the better physical stability of the M type.

Computations

The basic transformer formula is

$$U_1 = 4.44\times10^{-4}\times B\times A_c\times f\times N_1,$$

where

U_1 = primary voltage in V;
B = magnetic flux density in tesla;
A_c = cross-sectional area of the core in

cm^2;
f = mains frequency;
N_1 = number of primary turns.

Assume that a transformer, operating from a 240 V, 50 Hz mains supply is required to deliver a secondary voltage of 24 V. An M65 core (see Table 2) with a cross-sectional area of 4.9 cm^2, which allows a maximum flux density of 1.42 T and a secondary power dissipation of 35.7 W, will be used. How many primary turns will be required?

Rearranging the formula and inserting the specified values gives

$$N_1 = U_1/(4.44\times10^{-4}\times B\times A_c\times f)$$
$$= 240/(4.44\times10^{-4}\times1.42\times4.9\times50)$$
$$= 1553 \text{ turns.}$$

If the mains voltage were 250 V, the flux density would be

$$B = U_1/(4.44\times10^{-4}\times N_1\times A_c\times f)$$
$$=1.48 \text{ T,}$$

which exceeds the permissible maximum, so that the transformer would be driven into saturation. This shows that in these calculations the highest ex-pected primary voltage must be taken into account, which includes mains variations (±5%).

The effective efficiency is read from Table 2 as 77%. If grain-oriented M laminations VM 111-35 had been used, a core of the same dimensions would have allowed a dissipation of 43 W and given an effective efficiency of 81%.

Note in the formulas that B is inversely proportional to the frequency.

Hysteresis

When the frequency of the primary voltage is increased greatly, the losses in the core become so large that laminations can no longer be used. They are replaced by compressed iron-dust cores in which the losses are much smaller. Also in wide use are ferrite cores, which consist of high-resistance magnetic material consisting principally of ferric oxide and one or more other metals. After being powdered and sintered, ferrites exhibit low eddy current losses at high frequencies and thus make ideal core material for RF inductors and switching elements. Other cores for use in RF transformers and inductors are made of ferromagnetic spinels, which are high permeable and resistive ceramic-like materials that exhibit very low eddy current losses and high permeability.

Figure 10 shows typical magnetization curves for laminated cores. **Figure 11** shows typical hysteresis curves of laminated transformers.

Hysteresis is the tendency of a magnetic material to saturate and retain

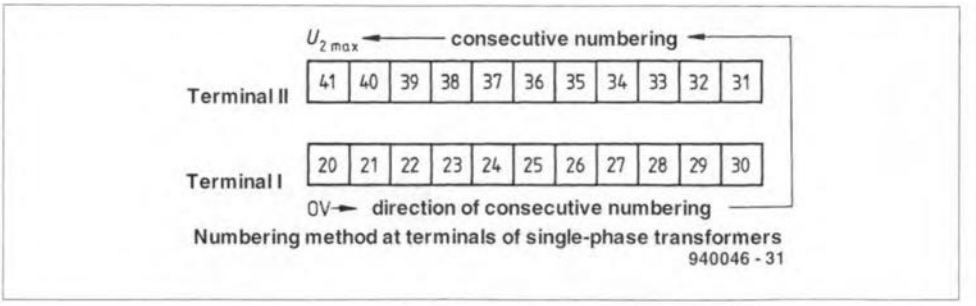

Fig. 18

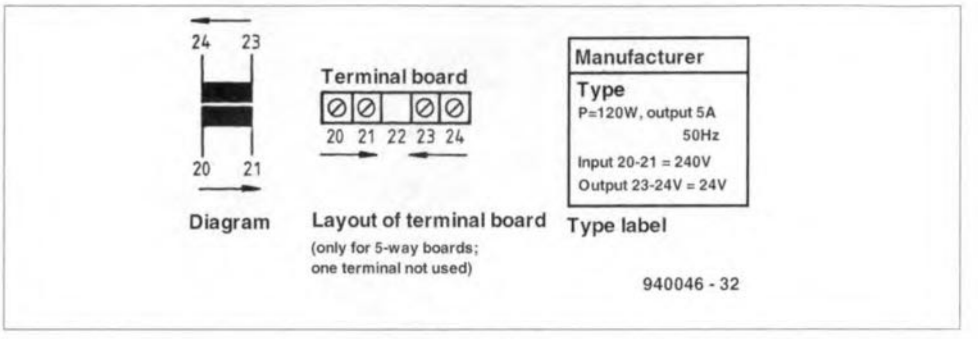

Fig. 19

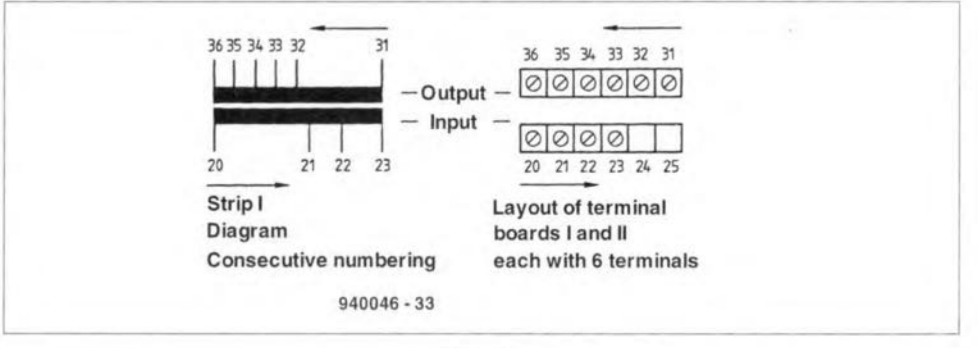

Fig. 20

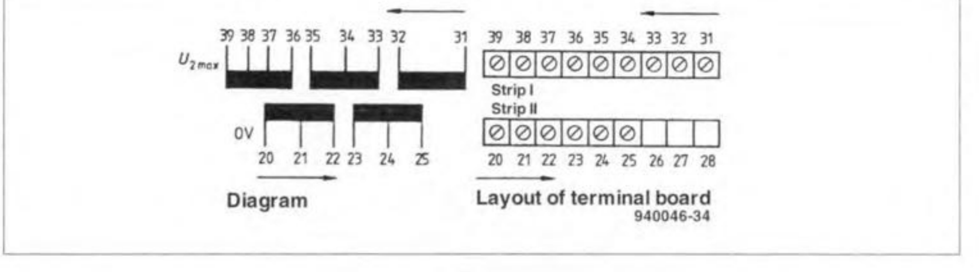

Fig. 21

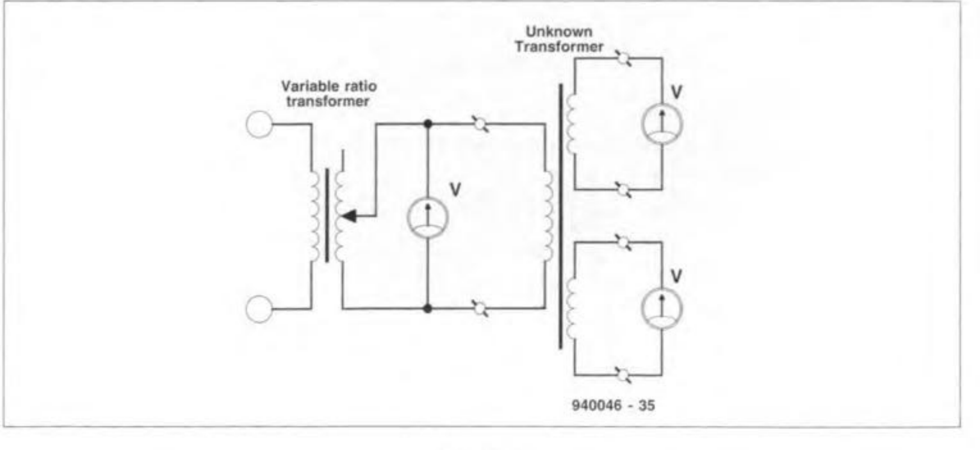

Fig. 22

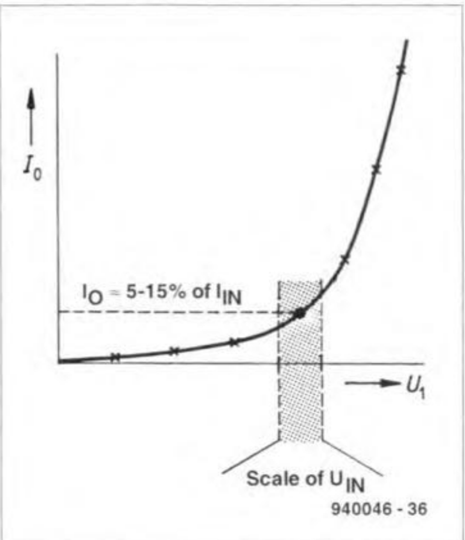

Fig. 23

some of its magnetism after the alternating magnetic field to which it is subjected reverses polarity, thus causing magnetization to lag behind the magnetizing force. The area of the hysteresis loop is a measure of the energy loss at each magnetic reversal. **Figures 12** and **13** give energy loss characteristics for various kinds of lamination at 50 Hz. Hysteresis losses increase rapidly with rising frequency; at a few thousand hertzs, only ferrites exhibit low hysteresis losses.

Toroidal transformers

In toroidal transformers, the core consists of a single long foil of magnetic material that is turned into a toroid. The primary and secondary windings are placed on to this toroid by a special technique—see **Fig. 14**. In these transformers, all lines of force point in the same direction.

The thinner the strip of magnetic material is, the lower the losses in the iron. Therefore, these cores are normally made of very thin foil. It is hard to think of a better closed magnetic loop.

Although the core is entirely surrounded by the windings, so that it tends to get warm, this is offset by the fact that the windings easily radiate heat. In the design of toroidal transformers, this property is used by allowing the copper losses to increase by the use of thin wire. Therefore, the resistance of a toroidal transformer is larger than that of a laminated transformer with the same power handling. Physically, however, the toroidal transformer is smaller.

Some theory

Basically, the operation of a transformer depends on mutual induction. The primary and secondary windings lie in the same magnetic flux. The basic design of a transformer is shown in **Fig. 15**; its circuit diagram in **Fig. 16**.

An alternating current in the primary gives rise to an alternating flux within the core. If the current is sinusoidal and it is assumed that the flux is always directly proportional to the current, then

$$\phi = \phi_m \sin 2\pi f t$$

describes the variation with time of the flux. ϕ is the flux at time t, ϕ_m is the maximum value of the flux and f the frequency with which the current, and thus the flux, alternates. The induced e.m.f. per turn is given by

$$U = -(\mathrm{d}\phi/\mathrm{d}t)$$

$$= -[\mathrm{d}(\phi_m \sin 2\pi f t)/\mathrm{d}t]$$

$$= -2\pi f \phi_m \cos 2\pi f t.$$

The maximum value of this induced e.m.f. per turn, U_m, occurs when the cosine term has its maximum value of 1. Thus,

$$U_m = 2\pi f \phi_m.$$

The r.m.s. value of this e.m.f., U_{rms}, is given by

$$U_{rms} = U_m/\sqrt{2} = 2\pi f \phi_m/\sqrt{2}$$

$$= 4.44 f \phi_m.$$

If the primary has N_1 turns, the r.m.s. value of the primary e.m.f., U_1, is $4.44 N_1 f \phi_m$. If the secondary has N_2 turns, the r.m.s. value of the secondary e.m.f., U_2, is $4.44 N_2 f \phi_m$.

The ratio $U_1{:}U_2 = N_1{:}N_2 = n$ is the turns (or transformation) ratio of the transformer.

When a load is connected across the secondary, a current I_2 flows through it which tends to counter the change in flux. This results in a lowering of the counter-e.m.f. in the primary, so that the primary current, I_1, rises. This rise exactly counters the demagnetizing effect of the secondary current.

So far, the resistance of the primary and secondary windings, as well as any stray fields, have been neglected. In practice, the primary causes a stray flux ϕ_{s1}, which is not linked to the secondary. Similarly, the secondary generates a stray flux, ϕ_{s2}, that is not linked to the primary. These fluxes induce voltages U_{s1} and U_{s2}, which lag the stray fluxes by $\pi/2$.

It may be assumed that, since these stray fluxes exist primarily in the air, they do not depend on the induction. The stray fluxes, and thus U_{s1} and U_{s2}, are directly proportional to I_1 and I_2. For our calculations, it does not matter whether the voltages are induced in the windings or in separate, air-cored coils. The inductances of these imaginary coils are determined by

$$\mathrm{j}\omega L_{s1} = \mathrm{j}X_{s1} = U_{s1}/I_1$$

and

$$\mathrm{j}\omega L_{s2} = \mathrm{j}X_{s2} = U_{s2}/I_2.$$

These coils and the resistance of the windings are shown in **Fig. 17**.

Terminations

Terminations on 'unknown' transformers that are marked by one or two rows of figures between 20 and 99 are almost certainly to DIN 42200. These numbers contain useful information. Most good-quality transformers have two rows of figures: their numbering is as shown in **Fig. 18**:

Terminations rated up to 25 A max.
row 1: starting with 20 up to 60
row 2: starting with 31 up to 60
Terminations rated up to 60 A max.
row 1: starting with 61 up to 99
row 2: starting with 71 up to 99.

For the row with primary terminations the following applies: start with 0 V at termination 20 and then up with increasing potential. See **Fig. 19–21**.

For the row with secondary terminations: start with the highest output voltage at the highest numbered termination and then down with decreasing potential. See **Fig. 19–21**.

The open-circuit voltage of an unknown transformer may be determined with a set-up as in **Fig. 22**. Up to saturation of the transformer, the open-circuit current will be small, about 5–15% of the nominally rated current. It increases in direct proportion to the applied voltage and sharply so when saturation is reached as shown by the curve in **Fig. 23**.

Since very high voltages may arise, the testing of an 'unknown' transformer should be carried out with great care and be started with relatively low applied potentials. The knee of the curve in **Fig. 23** is a measure of the nominally rated voltage of the winding.

[940046]

DESIGNING OSCILLATORS FOR PICs

By A. Rietjens

Peripheral Interface Controllers, PICs®, from Microchip are currently in the centre of attention. In descriptions of these devices an important aspect is seldom mentioned: the design of the clock oscillators. This article aims at putting this right.

Peripheral Interface Controllers contain a general purpose clock oscillator. This oscillator is controlled by an *RC* network, a quartz crystal or a ceramic filter. The clock signal may also be taken from an external generator. In the programming of the EPROM version of the PIC it must be stated which type of oscillator is used. The One Time Programmable (OTP) and QTP versions are available in four different types: RC, LP, XT or HS. Each of these types is suitable for one of the four oscillator variants.

RC oscillators

RC oscillators are an economical design for those applications where accuracy is not too important. When this oscillator is to be used, the RC or EPROM version of the PIC must be purchased. If the EPROM variant is used, the correct bit combination must be selected during programming.

The oscillator frequency depens on four quantities: the voltage, the temperature, the value of the capacitor and the value and type of the resistor. The design of the oscillator is shown in **Fig. 1**. Since at resistance values of >1 MΩ the oscillator becomes vulnerable to noise, temperature variations and humidity, it is advisable to use values of 5–100 kΩ. Values <3 kΩ may cause instability. **Table 1** gives a correlation of the capacitance, resistance and oscillator frequency. The frequency may be 0–4 MHz.

Quartz & ceramic oscillators

Ceramic and crystal oscillator have a number of advantages over *RC* types. Especially their stability and accuracy make them very suitable for circuits that are to be used in a wide variety of conditions. For this type of oscillator, the XT, HS or LP version of the PIC must be purchased. The EPROM version with accurate configuration may also be used. The XT version may be used with crystal frequencies of 0.1–4 MHz, the HS version from 4 MHz to 20 MHz and the LP version from d.c. to 40 kHz. If an external oscillator is used, all these versions can operate down to d.c.

The basic circuit of the oscillator is shown in **Fig. 2**. Sometimes a resistor has to be added to suppress oscillation at overtones. When the HSD version is used, R_S must always be fitted; its value should be between 100 Ω and 1 kΩ. **Table 2** gives the optimum values of C_1 and C_2 if a ceramic resonator is used, while **Table 3** gives these values when a crystal is used.

External oscillator

If a central clock oscillator is used in the processor system, it is convenient if the PIC can also employ this. The external clock signal must then be applied to input OSC1. Output OSC2 remains unused. Only XT, HS, LP and EPROM versions of the PIC can be used for this configuration.

[940106]

RC OSCILLATOR FREQUENCY VARIATION FROM UNIT TO UNIT

Cext	Rext	Average Fosc @ 5V, 25°C	
20pf	3,3k	4,71 Mhz	± 28%
	5k	3,31 Mhz	± 25%
	10k	1,91 Mhz	± 24%
	100k	207,76 Khz	± 39%
100pf	3,3k	1,65 Mhz	± 18%
	5k	1,23 Mhz	± 21%
	10k	711,54 Khz	± 18%
	100k	75,62 Khz	± 28%
300pf	3,3k	672,78 Khz	± 14%
	5k	489,49 Khz	± 13%
	10k	275,73 Khz	± 13%
	100k	28,12 Khz	± 23%

940106 - T1

Table 1.

CAPACITOR SELECTION FOR CERAMIC RESONATORS

Oscillator Type	Resonator Frequency	Capacitor Range C1 = C2
XT	455 KHz	150 - 330 pF
	2,0 MHz	20 - 330 pF
	4,0 MHz	20 - 330 pF
HS	8,0 MHz	20 - 200 pF

940106 - T2

Table 2.

CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

Osc Type	Freq	C1	C2
LP	32 KHz	15 pF	15 pF
XT	100 KHz	15 - 30 pF	200 - 300 pF
	200 KHz	15 - 30 pF	100 - 200 pF
	455 KHz	15 - 30 pF	15 - 100 pF
	1 MHz	15 - 30 pF	15 - 30 pF
	2 MHz	15 pF	15 pF
	4 MHz	15 pF	15 pF
HS	4 MHz	15 pF	15 pF
	8 MHz	15 pF	15 pF
	20 MHz	15 pF	15 pF

940106 - T3

Table 3.

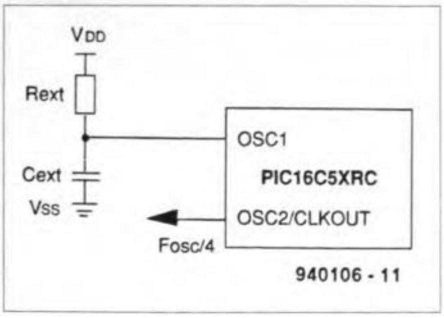

Figure 1.

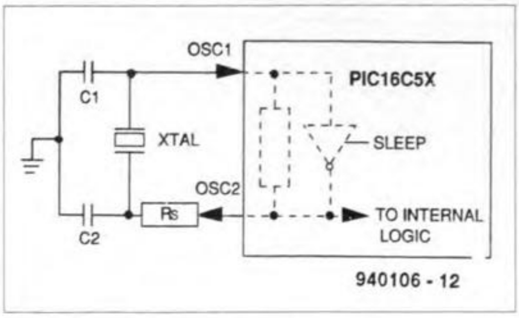

Figure 2.

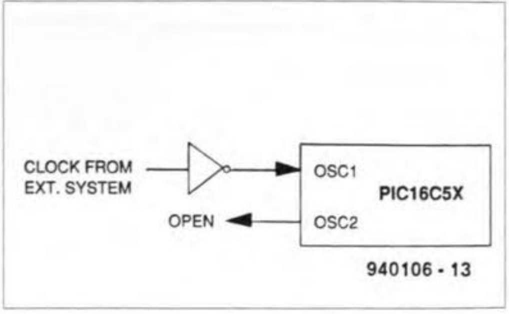

Figure 3.

PIC® PROGRAMMING COURSE

PART 3: INSTRUCTION SET

So far in the course we have been dealing with the hardware structure of the PIC processors. This third instalment, and the one to come, will deal with programming aspects and the PIC instruction set. This instalment also introduces the MPALC assembler for PIC devices, which may be obtained on diskette.

By our editorial staff.

Source: Microchip Technology Inc.

The instructions in the instruction set of most processors usually consist of two parts: an opcode (the instruction proper), and an operand (such as a memory location or a register). The operand is the object of the opcode. Most microprocessors and microcontrollers use one or more bytes for opcodes and operands. Not so with the PIC16C5x processors, which work with 12-bit wide words containing the instruction code and the operands. This approach has advantages as well as disadvantages. For example, the 12-bit structure limits the number of possibilities for the instruction code to 33. On the other hand, it has the advantage of offering very fast instruction processing because all information is fetched in one go.

The instructions used by the PIC16C5x may be divided into three groups:

- byte oriented register file instructions;
- bit oriented register file instructions;
- constants and control instructions.

A marked difference with other processors is noted as regards the byte oriented instructions. Usually, a 'working register' ('W' register in PIC devices; 'accumulator' in most others) is used, for instance, when adding two numbers. With PIC devices, the programmer has the option of storing the result into the W register or into the register file specified in the operand. In the instruction code, the choice is made with the aid of the 'destination bit', d. Unfortunately, Microchip Technology has left the declaration of the d bit to the programmer. Consequently, the 'd' bit has to be declared as follows at the start of every program:

```
           ;rule destination
W equ OH  ;destination = W
F equ 1H  ;destination = f
```

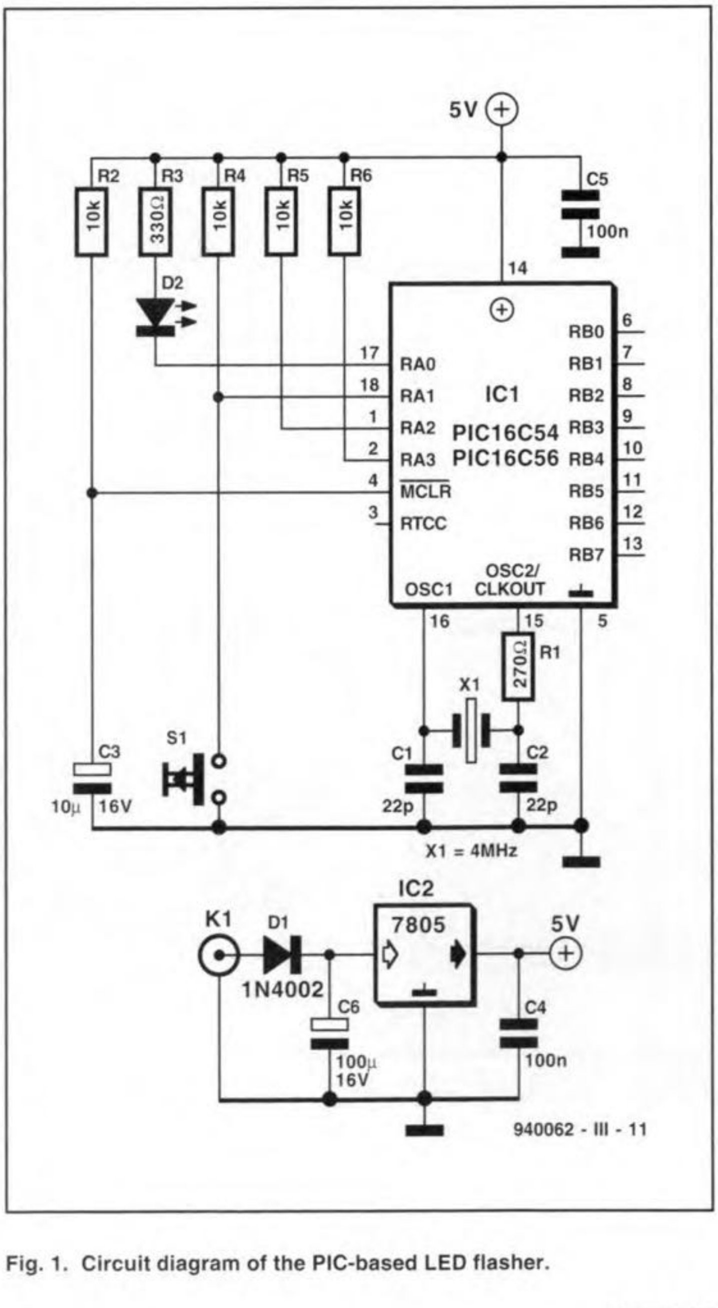

Fig. 1. Circuit diagram of the PIC-based LED flasher.

The PIC instruction set is summarized in **Tables 1, 2 and 3**. The commands and directives used by Microchip's 'MPALC' PIC assembler are listed in **Tables 4, 5, 6 and 7**. A number of these will be discussed further on in this article.

For example: a flashing LED

The outputs of a PIC16C5x processor can drive loads up to 20 mA. However, the maximum current drawn by the PIC device must remain below 50 mA, while the current through the GND (ground) connection must remain smaller than 150 mA.

A programming example, LED_SMPL.ASM (on the course diskette), works in conjunction with the hardware arrangement shown in **Fig. 1**. An LED and a 330-Ω series resistor are connected between the positive supply line (+5 V) and I/O port line RA0. All other I/O pins are strapped to +5 V via 10-kΩ pull-up resistors. A press-key is connected between RA1 and ground. The circuit is built on an experimentation board for PICs described in Ref. 1.

The function of the program is simple: arrange for the LED to start flashing as soon as the press-key is actuated. The example program is assembled as follows:

MPALC LED_SMPL.ASM <RETURN>

While programming the PIC, make sure that the XT (quartz crystal) oscillator option is used.

The operation of the program is easily followed by referring to the listing shown in **Fig. 2**. Lines 1 through 16 contain the assembler instructions which determine the appearance of the listing. The comment with these lines is mostly self-evident. Next, the RESET vectors are declared. The declarations depend on the controller used, and are programmed via a constant called 'controller'. In the present example, 'controller' takes a value of 56. In the subsequent 'if...endif' construction, a second constant, 'Adr_Reset' is defined, which is dependent on the value of 'controller', and serves to enable the assembler to include the reset vectors in the proper locations.

The directive 'list p=16C' is a little unusual. Why the processor type is defined using a 'list' instruction will probably remain a secret kept by the designers of the assembler.

More constants are declared up to line 77. Well-commented declarations are essential to get a good insight into the structure of the program, and are essential for efficient program development and debugging. Also, the declarations may make use of the assembler's computing capabilities, for example,

```
characters/line  equ 80
lines/page       equ 25
characters/page  equ charac-
                 ters/line x
                 lines/page
```

This is the correct approach. By contrast, the following declaration is incorrect:

```
characters/page  equ 2000
```

As already mentioned with the description of the PIC hardware, a CALL instruction can only 'jump' within the first half of a program memory page. It is, therefore, wise to declare all subroutines at the start of the program. The 'ORG' instruction in line 86 tells the assembler to set the internal program counter to the indi-

Table 1. Byte-oriented file register operations

Mnemonic, operand(s)		Name, operation	Status Affected
ADDWF	f, d	Add W and f	C, DC, Z
ANDWF	f, d	AND W and f	Z
CLRF	f	Clear f	Z
CLRW	–	Clear W	Z
COMF	f, d	Complement f	Z
DECF	f, d	Decrement f	Z
DECFSZ	f, d	Decrement f, Skip if zero	–
INCF	f, d	Increment f	Z
INCFSZ	f, d	Increment f, Skip if zero	–
IORWF	f, d	Inclusive OR W and f	Z
MOVF	f, d	Move f	Z
MOVWF	f	Move W to f	–
NOP	–	No Operation	–
RLF	f, d	Rotate left f	C
RRF	f, d	Rotate right f	C
SUBWF	f, d	Subtract W from f	C, DC, Z
SWAPF	f, d	Swap halves f	–
XORWF	f, d	Exclusive OR W and f	Z

Table 2. Bit-oriented file register operations

Mnemonic, operand(s)		Name, operation	Status Affected
BCF	f, b	Bit clear f	–
BSF	f, b	Bit set f	–
BTFSC	f, b	Bit Test f, Skip if Clear	–
BTFSS	f, b	Bit test f, Skip if set	–

Table 3. Literal and control operations

Mnemonic, operand(s)		Name, operation	Status Affected
ANDLW	k	AND literal and W	Z
CALL	k	Call subroutine	–
CLRWD	–	Clear watchdog timer	TO, PD
GOTO	k	Go To address (k = 9 bit)	–
IORLW	k	Inclusive OR Literal and W	Z
MOVLW	k	Move Literal to W	–
OPTION	–	Load OPTION register	–
RETLW	k	Return, place Literal in W	–
SLEEP	–	Go into standby mode	TO, PD
TRIS	f	Tristate port f	–
XORLW	k	Exclusive OR Literal and W	Z

Table 4. Data directives

data	<expr>	Create a 12-bit data value or character string
zero	<mem units>	Initialize with zero <mem units> of program space
set	<label> ... <expr>	Define assembler value
res	<mem units>	Reserve words of program space
equ	<label> ... <expr>	Define an assembler constant
include	"<file_name>"	Include a file into the assembly source flow

Table 5. Listing directives

list	<option>	Set various list control options
page		Force a page eject
title	"title text"	Define a new title for the listing header
subtitl	"subtitle text"	Define a new subtitle for the listing header

PIC16C5x PROGRAMMING

This short course is aimed at providing an introduction into programming and hardware aspects of the PIC16C5x family of microcontrollers manufactured by Microchip Technology Inc.

An **assembler** is offered on disk in support of the course. This assembler is distributed with the permission of Microchip Technology Inc., and supports the PIC16C5x and PIC16Cxx series of controllers. It offers a full featured macro and conditional assembly capacity. It can also generate various object code formats including several hex formats to support Microchip's proprietary development tools as well as third party tools. Also supported are hex (default), decimal and octal source and listing formats. An assembler users manual is available from Microchip Technology distributors for detailed support. The disk also contains a software **simulator**.

The PIC programming course disk may be obtained through the *Elektor Electronics* Readers Services under order number **946196-1**. For price and ordering information, see page 70 of this issue.

The files produced by the assembler can be downloaded to the **PIC programmer** described in *Elektor Electronics* March 1994.

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Table 6. Control directives		
if	<expr>	Start of a conditional assembly block
else		Start of an alternate conditional assembly block
endif		Terminate a conditional assembly block
org	<label> ... <addr>	Set absolute address for following block code
end		Terminate assembly code block

Table 7. Macro directives		
macro	<label> .. [<arg>,[<arg>] ...]	Begin a macro body definition
endm		Terminate macro body definition
local	<label>[,<label>] ...	Define assembler labels as local to macro
exitm		Exit macro

cated address, here, 0000. Immediately after this statement, the subroutine 'Wait_ms' starts. The delay introduced by this subroutine is defined in milliseconds with the aid of a value read from the W register.

Read instructions

The first instruction in the 'Wait ms' subroutine is MOVWF (Table 8). It tells the controller to store the contents of the W register directly at location 'ms'. This location was declared earlier in line 65.

The next instructions (lines 100 and 101) cause a location called 'us' (for microseconds, μs) to be filled with the value 0FEH. Since there is no instruction which enables that to be done directly, an alternative approach is used in which the W register plays an important part. The instruction MOVLW (line 100) puts the constant into the W register.

There are two ways to place the value '0' into the W register: either use MOVLW 000H, or the simpler CLRW instruction. Note, however, that CLRW also sets the Z flag.

Another instruction to clear the contents of a memory location in the register file is 'CLRF'. Like CLRW, CLRF does not make use of the W register, and actuates the Z flag.

A final option is the MOVF instruction, which allows the contents of a memory location to be copied into the W register. Alternatively, this instruction enables the memory location included in the operand, rather than the W register, to act as the 'target'. The result of this instruction is that the contents of a location are simply returned to the same location. This seemingly pointless instruction is useful with, for instance, I/O port operations. One instruction is sufficient to read the logic state of a port, and return the information to the buffer register. The same instruction may also be used to test the contents of a register for the value '0'.

As already mentioned, the subroutine waits the number of milliseconds defined via the W register. This is achieved by using two nested loops. The outer loop (lines 103 through 111) takes exactly 1 ms to complete if a clock frequency of 4 MHz is used. This loop is called as many times as the value contained in the W register, via lines 110 and 111. The number of iterations of the inner loop is not stored as a constant in the 'us' register, but added to the constant of the register. This is done on purpose to allow a correction to be made to compensate for the time needed to start the entire subroutine. The subroutine is finished if location 'us' reaches the value 00H.

Arithmetic instructions

The arithmetic instructions offered by PIC processors are limited to ADDWF and SUBWF, and their derivates INCF and DECF. An application of the ADDWF instruction may be found in

```
1          title "Sample flashing LED"   ; Program title
2          subtitl «Declarations»        ; Program subtitlle
3
4          ; Listing Options for MPALC assembler
5          list c=136                    ; Columns per line
6          list n=60                     ; Lines per page
7          list r=HEX ; [HEX,DEC,OCT]    ; HEX as default
8          list l=ON ; [ON / OFF]        ; Listing ON
9          list x=ON ; [ON / OFF]        ; Macro expansion on
10         list t=ON ; [ON / OFF]        ; Truncate listing lines
1          list e=0 ; [0,1,2,3]          ; 0 = Report all Messages
2                                        ; 1 = Report Warnings,
                                         ; fatals, criticals
3                                        ; 2 = Report fatals, criticals
4                                        ; 3 = Report criticals
5
6          page                          ; New Page
7
8          ; select controller
9 controller   equu     56               ;54: PIC 16C54, 55: PIC 16C55 ...
20
1          if controller == 54 ; PIC 16C54
2              list p=16C54 ;
3              Adr_Reset equ 01FFH ;
4              endif
5          if controller == 55 ; PIC 16C55
6              list p=16C55 ;
7              Adr_Reset equ 01FFH ;
8              endif
9          if controller == 56 ; PIC 16C56
30             list p=16C56 ;
1              Adr_Reset equ 03FFH ;
2              endif
3          if controller == 57 ; PIC 16C57
4              list p=16C57 ;
5              Adr_Reset equ 07FFH ;
6              endif
7
8          ; Main declarations
9
40         ; Destination of Byte-Oriented File Register Operations
1 W             equ      00H             ; Destination is W Register
2 F             equ      01H             ; Destination is F Register
3
4          ; Directions of I/O - Ports
5 Input         equ      01H             ; Input
6 Output        equ      00H             ; Output
7
8 ; ----------------------------------------
9          ; Register file declarations
50
1          ; Operational Register File
2 INDIRECT      equ      00H             ; Indirect Data addressing
3 RTCC          equ      01H             ; Real Time Clock/Counter Reg.
4 PC            equ      02H             ; Program counter
5 STATUS        equ      03H             ; Status Word Register
6 FSR           equ      04H             ; File Select Register
7
8               ; I/O Registers (Ports)
9 Port_A        equ      05H             ;
60 Port_B       equ      06H             ;
1 Port_C        equ      07H             ; PIC 16C55/C57 only
2
3          ; General Purpose Registers, user defined
4 us_Register   equ      009H ;
5 ms_Register   equ      00AH ;
6
7 ; ----------------------------------------
8          ; Hardware declarations
9
70 LED_B        equ      00H             ; LED connected to RA0
1 LED_P         equ      Port_A          ;
2 LED_off_time  equ      000H            ; LED off for 256 ms
3 LED_on_time   equ      000H            ; LED on for 256 ms
4
5 KEY_B         equ      01H             ; KEY connected to RA1
6 KEY_P         equ      Port_A          ;
7
8
9          subtitl "Subroutines"
80         page
1
2 ; ==================================================================
3 ; Subroutines
4 ; ==================================================================
5
6               org      0000H           ; Subroutines only in first half
7                                        ; of page
8
9 ; ----------------------------------------
90 ; Subroutine Wait_ms
1 ;
2 ; Parameter: ms in W Register
3 ; Return value: 000H
4 ;
5 ; Delay time is 1 ms * (W Register) at Fosc = 4Mhz
6 ; Note: W Register = 000H <=> 256 ms
7 ;
8
9 Wait_ms       movwf    ms_Register     ; store ms
100             movlw    0FEH            ; correct call time (incl 1 movlw
1               movwf    us_Register     ; before calling) for first loop
2
3 W_Loop_ms     movlw    0F9H            ; 1 loop 249*W_Loop_us+4 cycles
4               addwf    us_Register,F   ;
5
```

```
W_Loop_us       nop                             ; one loop = 4 cycles
                decfsz  us_Register,F   ; us_register - 1, skip if zero
                goto    W_Loop_us       ;

                decfsz  ms_Register,F   ; ms_register - 1, skip if zero
                goto    W_Loop_ms ;
                nop                     ; correct time of last ms loop


                retlw   000H            ;
;
; ————————————————————————————————————————-

                subtitl "Main program"
                page

; ==================================================================
; Main Program
; ==================================================================
;
Main_Start                              ; Starting after RESET
                movlw   00EH            ; Set RA0, which is connected to
                tris    Port_A          ; LED, as output
                goto    LED_off         ; Initially: LED off

Loop            btfsc   KEY_P, KEY_B    ; Key pressed? (RA1 = 0?)
                goto    Loop            ; No, wait until key pressed

                bcf     LED_P, LED_B    ; LED on
                movlw   LED_on_time     ; wait
                call    Wait_ms         ;

LED_off         bsf LED_P, LED_B        ; LED off
                movlw   LED_off_time    ; wait
                call    Wait_ms         ;

                goto    Loop
;
; ==================================================================
                org     Adr_Reset       ; define reset vector
Reset           goto    Main_Start      ; Start at Main_Start after RST
; ==================================================================
                end
```

Fig. 2. Example program for the hardware shown in Fig. 1. The code shown here may be typed in using any ASCII compatible word processor, and is suitable for the Microchip Technology's MPALC assembler found on the PIC programming course disk. Line numbers are added for reference in this article only; they are NOT included in the LED_SMPL.ASM file on the course disk.

```
; Add two 32-Bit numbers N and Z. Result stored back into N.
;   If N+Z > 2**32 the CARRY flag is set
;
; N_LL, Z_LL: Bit  0.. 7
; N_LH, Z_LH: Bit  8..15
; N_HL, Z_HL: Bit 16..23
; N_HH, Z_HH: Bit 24..31
;
ADD_LL    movf    Z_LL, W    ; Load W with Z_LL
          addwf   N_LL, F    ; ADD N_LL and W, store at N_LL
          btfsc 3,0          ; Skip if Carry = 0
            goto  CARRY_LH   ;

          movf    Z_LH, W    ; Load W with Z_LH
ADD_LH    addwf   N_LH, F    ; ADD N_LH and W, store at N_LH
          btfsc 3,0          ; Skip if Carry = 0
            goto  CARRY_HL   ;

          movf    Z_HL, W    ; Load W with Z_HL
ADD_HL    addwf   N_HL, F    ; ADD N_HL and W, store at N_HL
          btfsc 3,0          ; Skip if Carry = 0
            goto  CARRY_HH   ;

          movf    Z_HH, W    ; Load W with Z_HH
ADD_HH    addwf   N_HH, F    ; ADD N_HH and W, store at N_HH
          retlw   000H       ; Return, load W with 000H

; Ripple carry routine

CARRY_LH  incfcz  Z_LH, W    ; Load W with Z_LH+1, skip if W=0
            goto  ADD_LH
CARRY_HL  incfcz  Z_HL, W    ; Load W with Z_HL+1, skip if W=0
            goto  ADD_HL
CARRY_HH  incfcz  Z_HH, W    ; Load W with Z_HH+1, skip if W=0
            goto  ADD_HH
          setc               ; overflow => carry = 1
          retlw   000H       ; Return, load W with 000H
```

Fig. 3. PIC assembly code for a program which adds two 32-bit numbers.

MOVWF	**Move W to f**		
Syntax	movwf f	**Status bits:**	none
Description	Move data from W register to register f		
Example	*movwf ms_Register*		

MOVLW	**Move Literal to W**		
Syntax	movlw k	**Status bits:**	none
Description	The 8-bit literal k is loaded into W register		
Example	*movlw 0FEH*		

CLRW	**Clear W register**		
Syntax	clrw	**Status bits:**	Z
Description	W register is cleared, Zero bit (Z) is set		
Example	*clrw*		

CLRF	**Clear f and Clear d**		
Syntax	clrf f,d	**Status bits:**	none
Description	Contents of register f are set to 0 d = 0: contents of both data memory location f, and W register are set to 0 d = 1: contents of register f are set to 0		
Example	*clrf ms_Register*		

MOVF	**Move f**		
Syntax	movf f, d	**Status bits:**	Z
Description	d = 0 : move contents of register f, result stored in W d = 1 : move contents of register f, result stored back in f		
Example	*movf Port_B, W*		

ADDWF	**Add W to f**		
Syntax	addwf f, d	**Status bits:**	C, DC, Z
Description	Add contents of the W register to register f d = 0 : result stored in W register d = 1 : result stored back in register f		
Example	*addwf us_Register, F*		

SUBWF	**Subtract W from f**		
Syntax	subwf f, d	**Status bits:**	C, DC, Z
Description	Subtract the W register from register f d = 0 : result stored in W register d = 1 : result stored back in register f		
Note	The subtraction is carried out according to the 2's complement method. The Carry bit is set if the subtraction did not produce an overflow: f > W => C = 1, Z = 0 f = W => C = 1, Z = 1 f < W => C = 0, Z = 0		
Example	*subwf us_Register, F*		

INCF	**increment f**		
Syntax	incf f, d	**Status bits**	Z
Description	Increment contents of register f d = 0 : result stored in W register d = 1 : result stored back in register f		
Example	*incf ms_Register, F*		

DECF	**decrement f**		
Syntax	decf f, d	**Status bits**	Z
Description	Decrement register f d = 0 : result stored in W register d = 1 : result stored back in register f		
Example	*decf ms_Register, F*		

line 104, where a value 0F9H (copied into W in line 103) is added to the contents of location 'us'.

All arithmetic instructions allow either the W register or the f register in the operand to function as the 'target'. That enables a certain value to be added to several 'f' registers in one go.

Unfortunately PIC processors lack instructions of the type 'add with carry' and 'subtract with carry'. Consequently, adding numbers which are wider than 8 bits requires the carry flag to be processed separately. **Figure 3** shows an example of a program in which two 32-bit numbers are added. These numbers are 'Z' and 'N. 'Z' consists of the bytes Z_HH, Z_HL, Z_LH and Z_LL. The same goes for 'N'.

When using the SUBWF instruction, it should be noted that this is performed according to the 'two's complement' method. Consequently, the carry flag is actuated inversely.

The use of the DECF and INCF instructions should be self-evident. These instructions decrease or increase the contents of a memory location by one, respectively. Here, too, the result is stored into the f register stated in the operand, or into the W register. If the result equals 0, the Z flag is actuated.

(940062-3)

Reference:

1. Experimentation board for PICs, *Elektor Electronics* July/August 1994.

Continued in the November 1994 issue.

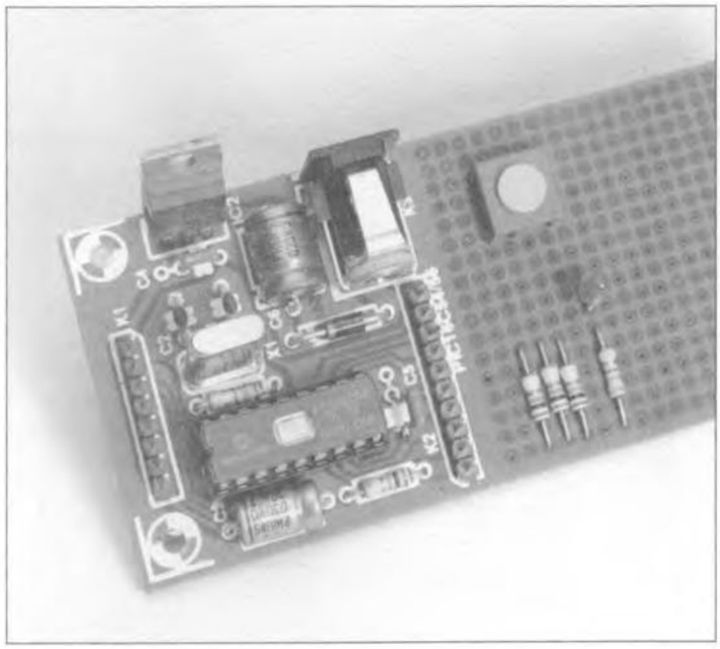


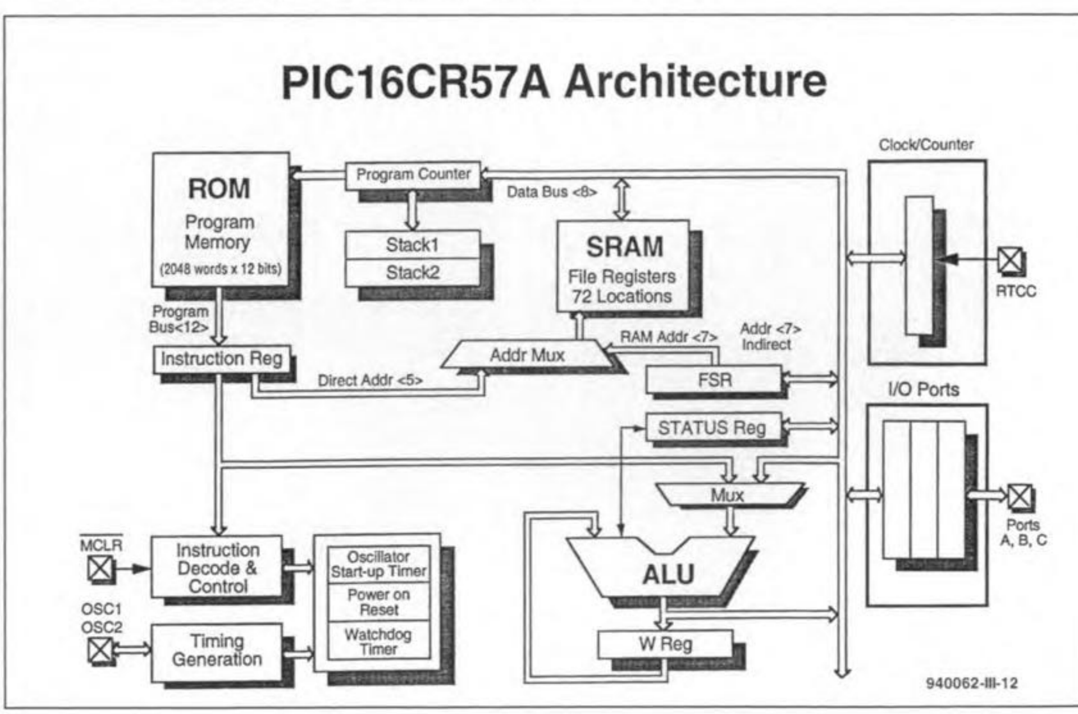
Fig. 4. The PIC-based LED flasher is best built on a PIC experimentation board (Ref. 1).

Microchip announces new PIC16CR57A 8-bit microcontroller

MICROCHIP'S low-cost PIC16CR57A 8-bit microcontroller is ideal for I/O intensive, low-power applications. The new 8-bit ROM-based microcontcontroller uses an advanced 0.9-micron fabrication process to achieve greatly improved electrical performance with lower power consumption and a wider operating voltage range.

Running at up to 20 MHz, with faster instruction execution than any other 8-bit RISC microcontroller in its class, the PIC16CR57A operates from 2.5 to 6.25 V sources and features a power-down (sleep) mode that further reduces power consumption. On-chip memory facilities include 2,048 12-bit wide words of masked ROM for program storage, and 72 bytes of static RAM for data. On-chip peripherals include an 8-bit real-time clock/counter with programmable prescaler, an oscillator start-up timer, a watchdog timer with on-chip RC oscillator and 20 I/O lines with individual directional control. In addition, the PIC16CR57A is socket and software compatible with Microchip's one-time programmable PIC16C57 microcontroller, and 100% code compatible with the 18-pin 16CR54 ROM, providing a simple upgrade path to existing users.

Arizona Microchip Technology Ltd., Unit 3, The Courtyard Meadowbank, Furlong Road, Bourne End, Bucks SL8 5AJ, England.
Tel. (0628) 850303, fax: (0628) 850178.



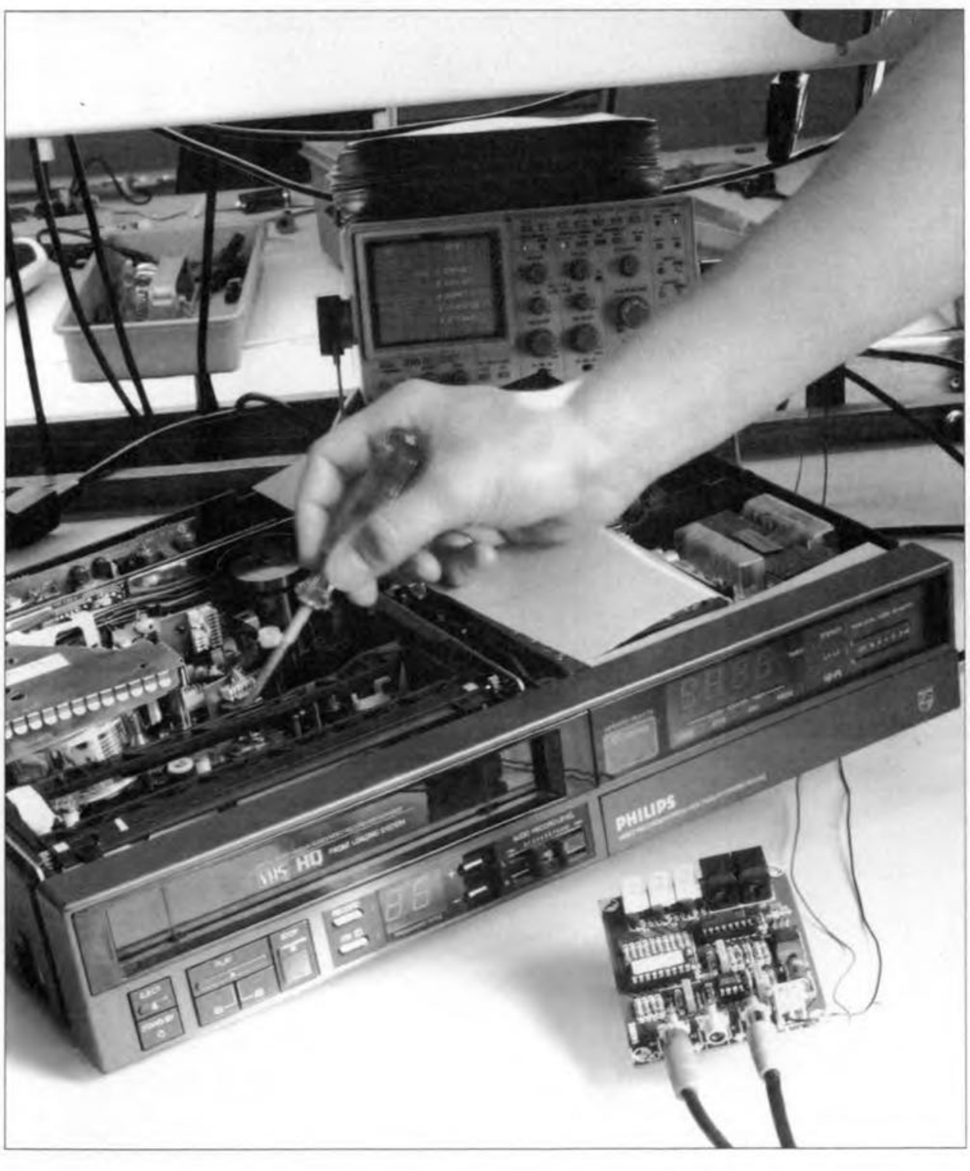
TV LINE MONITOR

Measurements on TV signals are notoriously difficult. Even if you have an oscilloscope with a trigger button marked 'TV' it is practically impossible to select a particular line from the picture signal. That problem is solved once and for all by the TV line monitor described in this article, because it allows any line in the composite video signal to be selected in a simple manner.

Design by J. Matus

FOR a well-founded verdict on the operation of a TV set it is often required to perform measurements on individual lines in the video signal as processed by the set. For this purpose, a number of special test signals (insertion test signals, ITSs) are included in nearly every TV broadcast, whether by satellite or terrestrial. These signals are contained in picture lines which are normally invisible to the viewer, i.e, they fall outside the actually viewed raster. The TV technician, however, views them on an oscilloscope. The basic functions offered by the ITSs will be discussed further on.

The picture line monitor is a handy and multi-functional tool for repairing and adjusting TV sets and other video equipment, such as video recorders (VCRs). The TV line monitor is based on a PIC16C54, a type of microcontroller which has been used on several occasions at the heart of different circuits described in *Elektor Electronics*. The PIC comes ready-programmed through our Readers Services, and reduces the IC count in the circuit to three (well, actually four if you include the voltage regulator). The line monitor enables an oscilloscope to be triggered at the start of the TV line selected by you, the user. The TV line you wish to view on the scope is selected with the aid of two press-keys, and is indicated on a readout consisting of three 7-segment LED displays.



The circuit diagram of the TV line selector is given in **Fig. 1**. Broadly speaking, the circuit consists of two parts: a synchronisation separator and a processor (with LED readout) which acts as a general control. The composite video signal (CVBS) is applied to the circuit via socket K_1. To keep the loop-through connection to the oscilloscope as simple as possible, the CVBS signal re-appears on K_2. A simple *RC* filter, R_{17}-C_2, removes spurious pulses and other noise from the video signal. The 'clean' signal reaches the CVBS input of IC_1, an LM1881, via coupling capacitor C_3. The LM1881 from National Semiconductor is designed specially to unravel composite video signals. The four outputs of this IC supply (1) the composite synchronisation signal, (2) the vertical synchronisation pulses, (3) a colour burst marker and (4) an odd/even field marker. These signals provide all the information necessary to determine the timing of a composite video signal. The TV line monitor only uses the composite and the vertical synchronisation signals. The position of the colour burst is of no consequence to the circuit. Likewise, the odd/even field signal is less suitable for use here, mainly because it tends to be erratic if the video signal contains noise. This was considered an important drawback for a test instrument.

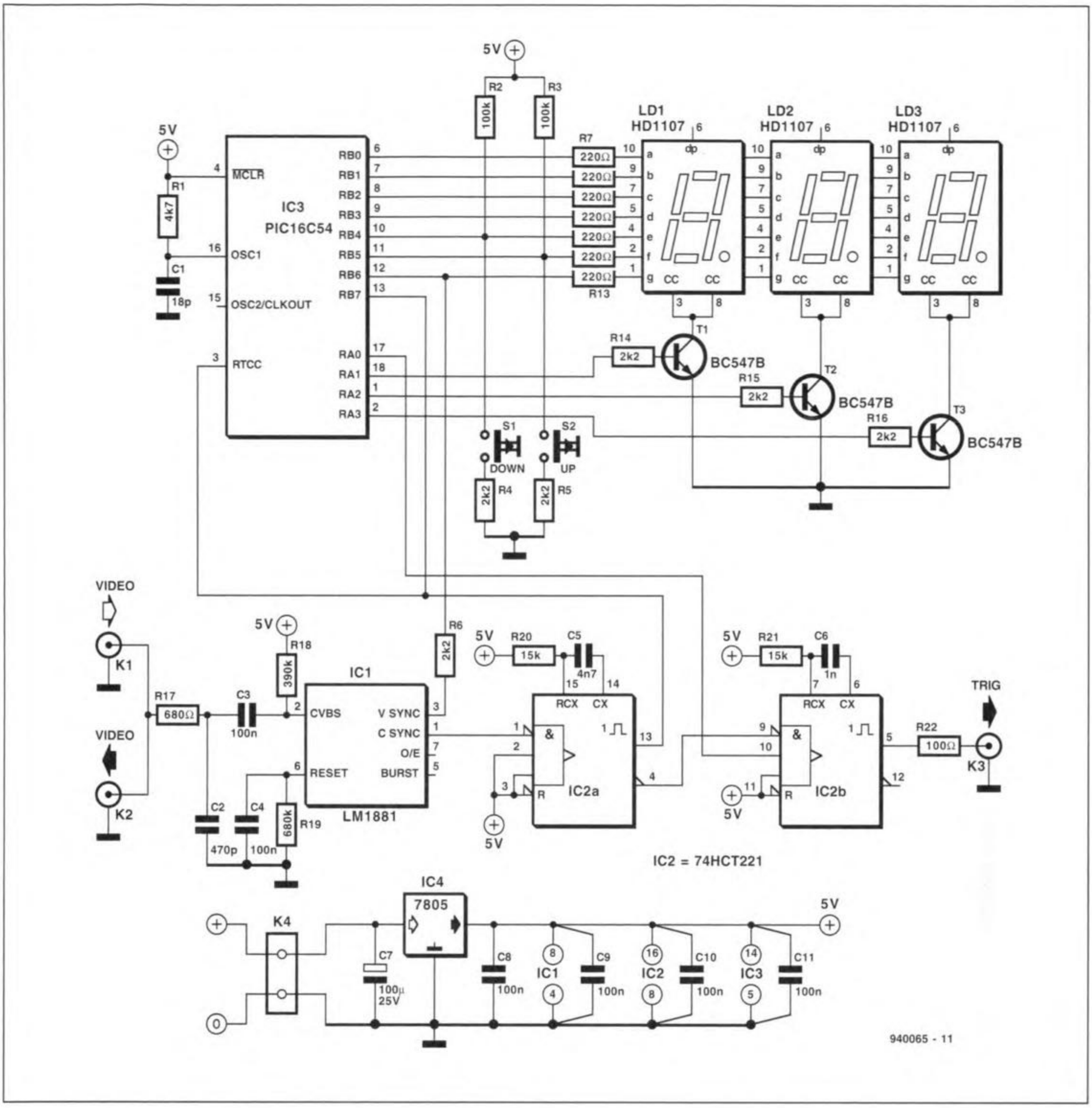


Fig. 1. Circuit diagram of the TV line monitor. The PIC processor, IC3, is supplied ready-programmed.

The composite sync signal is applied to monostable multivibrator IC2a, whose monotime equals about three quarters of a picture line. This time is used to suppress the half-line pulses which occur during the field flyback period. The output of the monostable supplies a clean horizontal sync signal, which can be used straight away by the processor.

The timing diagram in **Fig. 2** shows how the odd/even field changeover is usually marked in the signal. During the field flyback period, a number of extra sync pulses are inserted into the horizontal synchronisation signal, half-way the line period.

Since it is essential for the TV line monitor to detect the field changeover, the processor has to restore the relevant signal from the vertical and horizontal synchronisation pulses (remember, the odd/even field signal supplied by the LM1881 is not used). Figure 2 also indicates a delay of half a line period in the vertical synchronisation signal. This time has to be compensated to make sure that the trigger pulse for the oscilloscope is properly timed.

MAIN SPECIFICATIONS

Video standard:	PAL
Line number display:	3 x 7-segment LED
Processor:	PIC16C54
Controls:	two press-keys
Field:	selectable, odd or even
Picture line:	selectable, 1 through 625
Output:	digital trigger pulse
Detection:	no or bad input signal

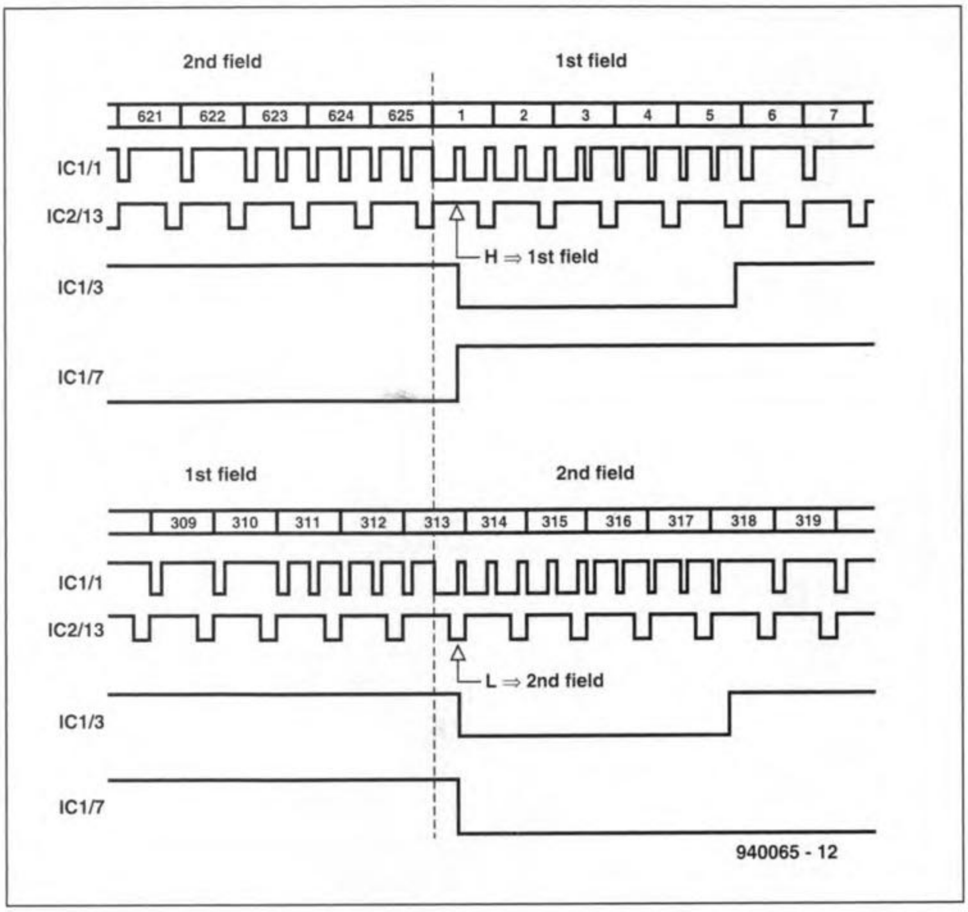


Fig. 2. The change from an odd-numbered to an even-numbered field in an interlaced TV picture is marked by extra horizontal synchronisation pulses which are inserted at about halfway the line period. These pulses appear around the vertical sync pulse.

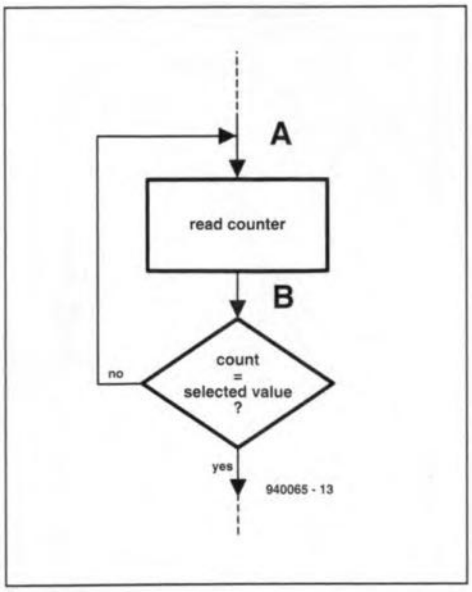


Fig. 3. Polling may cause large variations in the time needed by the processor to respond to a counter state match. This flow diagram shows how the delay is introduced.

The processor: heart of the circuit

As already mentioned, a PIC processor is used for all computing and control functions in the circuit. These functions are:

- driving the display in multiplex mode;
- scanning the press-keys for activity;
- counting the picture lines;
- enabling the trigger pulse.

All functions are carried out by a clever piece of software and the PIC's on-board 8-bit timer. A problem with the PIC processor used is that it can not handle interrupts. Consequently, the software must use 'polling', i.e., very frequent checking whether the desired picture line is already present at the input. Polling is an acceptable alternative if interrupts are not available, but it does take time. As illustrated in **Fig. 3**, it can lead to a large timing error. Obviously, the fastest processor response is obtained if the desired counter state is reached at point 'A'. If the state is reached at point 'B', a considerable delay is introduced because the comparator has to wait for the next polling cycle. This delay would cause an amount of jitter in the trigger pulse that can not be tolerated in a test instrument. Hence, a trick had to be devised to prevent gross timing errors. The solution is simple as well as ingenious: instead of generating a trigger pulse, the processor only enables a monostable (IC_{2b}) which does so. The monostable is started without any delay by the horizontal synchronisation pulse. The timing is illustrated in **Fig. 4**. The 'only' task of the software is to enable the monostable in time. That does, however, create some exacting demands on the speed of the processor, and the compactness of the program executed. Provided it is well written, the software should work reliably despite fairly large variations of the clock frequency. The present circuit works well at clock frequencies between 3 MHz and 5 MHz, allowing the inexpensive *RC* oscillator variant of the PIC processor

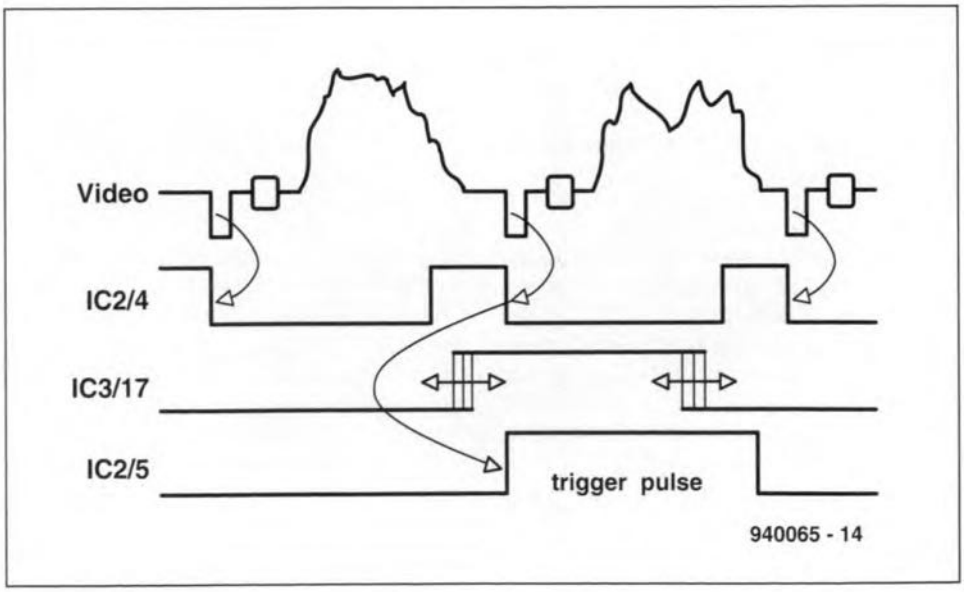


Fig. 4. After the monostable has been enabled, the horizontal sync pulse causes the scope trigger pulse to be generated.

to be used without reducing the repeatability of the circuit.

Ease of use

The TV line monitor is controlled with the aid of two press-keys marked '+' (up) and '–' (down). The picture line number selected in this way appears on a bright LED display. Any time a key is pressed, the line number is increased (+) or decreased (–) by one. If you keep a key pressed, the line number will step up or down automatically at a rate of two per second. If you keep the key pressed longer than 2.5 s, the auto-step speed goes up to 25 lines per second. The other field is selected by pressing both keys at the same time. If a suitable video signal is not present at the input, the circuit shows a moving bar which travels round the outer display segments.

Finally, note that the circuit is only capable of recognising both fields in a picture if the input signal meets the PAL standard as regards interlacing.

Action!

Having dealt with the design background of the circuit, it is time to discuss more practical things, i.e., the construction and use of the TV line monitor.

The artwork of the single-sided printed circuit board designed for the instrument is shown in **Fig. 5**. All components, including the three displays, the three 'RCA' sockets and the two keys, are accommodated on the board.

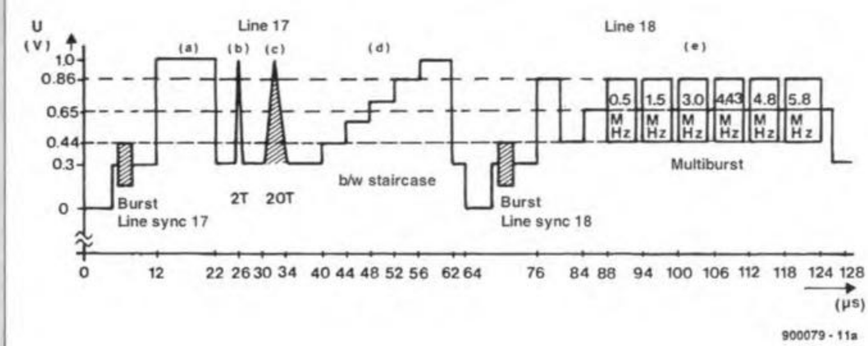
Start the construction by fitting the five wire links. Next, fit all passive components at the proper locations (refer to the component overlay on the board and as shown in Fig. 5). Finally, mount the active parts, the sockets and the PCB terminal block. That completes the construction. Since there are no adjustment points, the circuit is then ready for use.

Connect the circuit to a mains adapter capable of supplying an output voltage of about 8 V d.c. at a current of at least 100 mA. Connect a composite video signal (PAL standard) to socket K_1. Connect the input of the oscilloscope to K_2. Next, connect K_3 to the external trigger input of the oscilloscope. Select external triggering on the scope, and set it for a sensitivity of 0.5 V/div., d.c. coupled.

Switch on the line monitor, and check that the LED display reads '1'. The contents of the same line should be visible on the oscilloscope screen. Depending on the timebase setting, successive lines may also appear on the screen. If an unsuitable video signal is applied to the circuit, the outer segments of display LD_1 will go on and

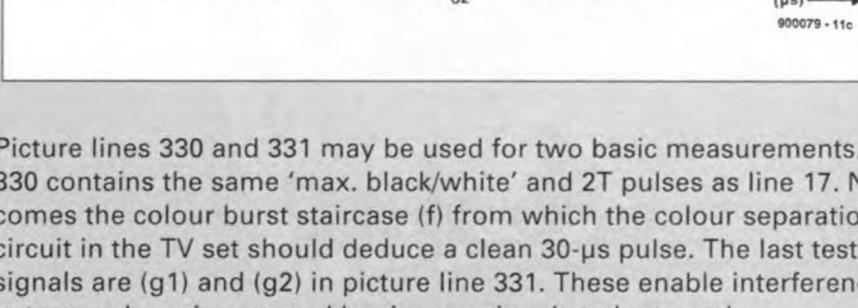
INSERTION TEST SIGNALS

Although the vast majority of TV viewers will never notice, nearly every TV picture contains a large number of special measurement signals transmitted in two pairs of successive lines, 17-18 and 330-331. The structure and function of these insertion test signals (ITSs) is usually based on CCIR recommendation 473-3.



Picture lines 17 and 18 may be used by the TV technician to test a large number of receiver functions. The black/white bar (a) is a reference to establish the maximum black and white levels. The 2T pulse (b) is test signal with sine-shaped edges and a total duration of 0.2 µs. It is used to determine the picture resolution. An attenuation of 20% is still tolerable. The 20T pulse (c) is used to test the response of amplifiers to luminance and chrominance signals. The next test signal is a monochrome staircase consisting of 140-mV steps. Finally, test signal (e) contains a sequence of fixed frequency bursts ranging from 500 kHz to 5.8 MHz. This 'multi-burst' signal serves to ascertain the frequency-dependent behaviour of the video amplifiers.

Picture line 22 is usually empty, i.e., it contains no video information. It has a function, though, enabling the total noise contribution of the receiver to be checked.



Picture lines 330 and 331 may be used for two basic measurements. Line 330 contains the same 'max. black/white' and 2T pulses as line 17. Next comes the colour burst staircase (f) from which the colour separation circuit in the TV set should deduce a clean 30-µs pulse. The last test signals are (g1) and (g2) in picture line 331. These enable interference between chrominance and luminance signals to be traced.

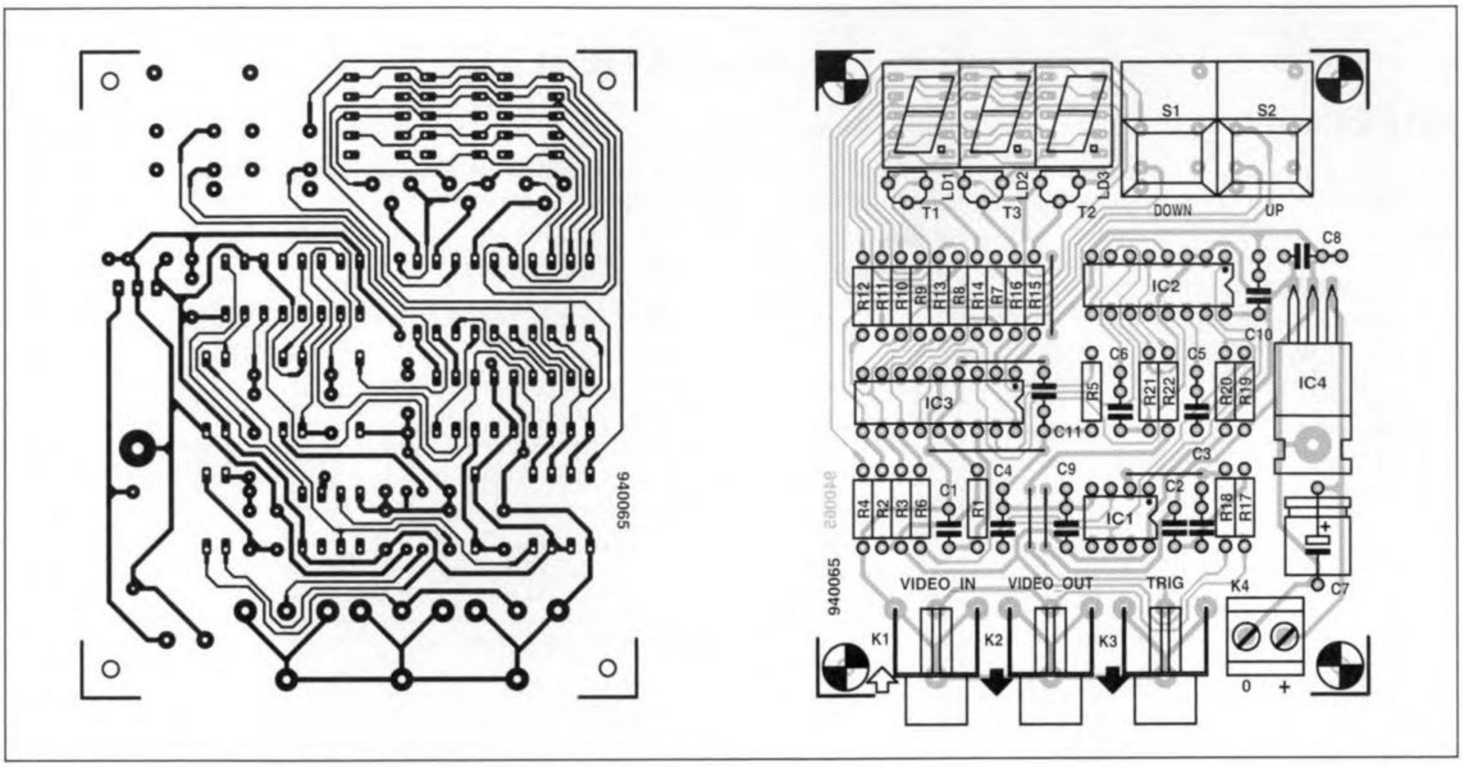


Fig. 5. Component mounting plan and track layout of the PCB designed for the circuit.

off describing a circle. If a correct signal is applied, however, and the circuit is fully functional, any line number can be selected very quickly by pressing the '+' and '–' keys and watching the LED display. (940065)

For further reading:

Colour television, by Geoffrey Hutson, Peter Shepherd and James Brice. McGraw-Hill Book Company. ISBN 0-07-084199-3.

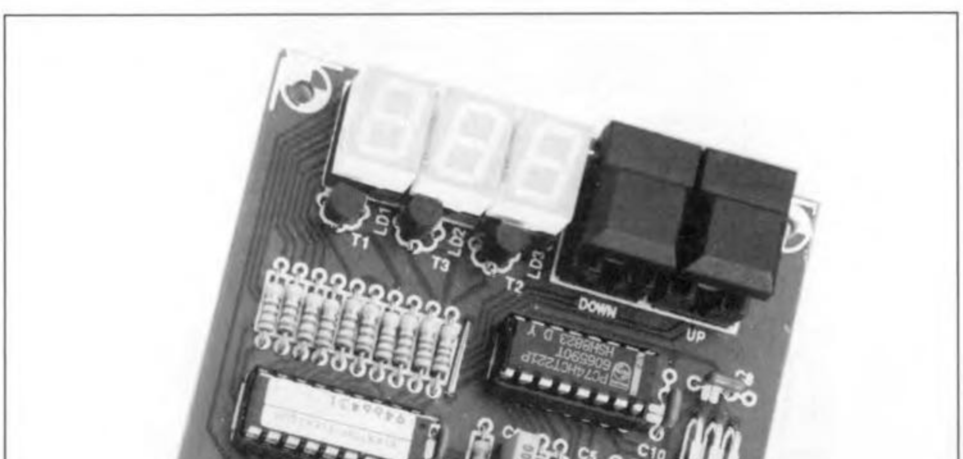


Fig. 6. Completed prototype. Note the compactness of the circuit.

COMPONENTS LIST

Resistors:

R1 = 4kΩ7
R2;R3 = 100kΩ
R4;R5;R6;R14;R15;R16 = 2kΩ2
R7-R13 = 220Ω
R17 = 680Ω
R18 = 390kΩ
R20;R21 = 15kΩ
R22 = 100Ω

Capacitors:

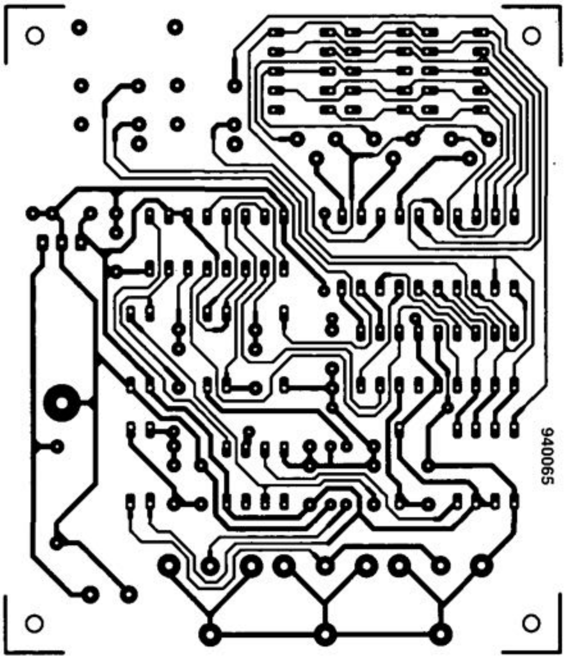
C1 = 18pF
C2 = 470pF
C3;C4;C8-C11 = 100nF
C5 = 4nF7
C6 = 1nF
C7 = 100µF 25V

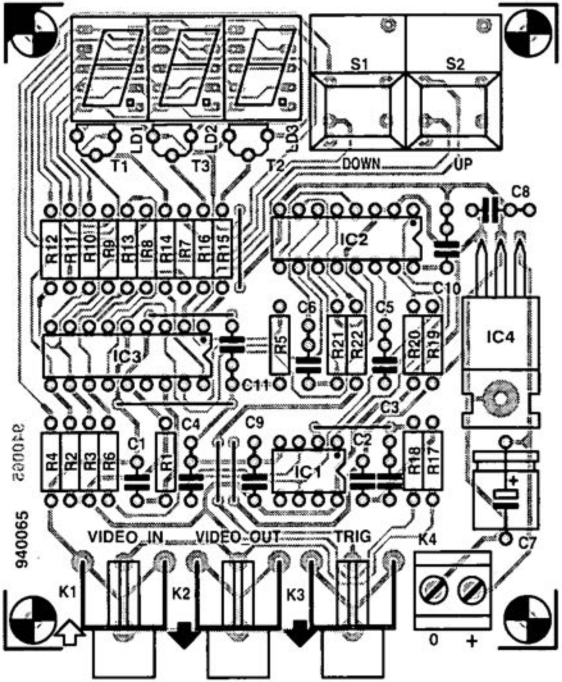
Semiconductors:

T1;T2;T3 = BC547B
IC1 = LM1881 (National Semiconductor)
IC2 = 74HCT221
IC3 = PIC16C54 (programmed; see below)
IC4 = 7805
LD1;LD2;LD3 = HD1107O (orange)

Miscellaneous:

K1;K2;K3 = PCB mount line socket.
K4 = 2-way PCB terminal block, raster 5mm.
S1;S2 = Digitast presskey w. 12mm cap.
Printed circuit board plus programmed PIC (IC3); set order code 940065 (page 70). The PIC is also available separately as order code 946643-1 (page 70).


940065


LD1
LD2
LD3
T1
T3
T2
S1
S2
DOWN
UP
C8
IC2
R12
R11
R10
R9
R13
R8
R14
R7
R16
R15
C10
C6
C5
R21
R22
R20
R19
R5
IC3
IC4
C11
C3
C4
C9
C1
C2
IC1
R4
R2
R3
R6
R1
R18
R17
940065
VIDEO_IN
VIDEO_OUT
TRIG
K4
C7
K1
K2
K3
0
+

COMPONENTS SELECT

New circuit protectors

Raychem has introduced new versions of its resettable surface-mount Polyswitch circuit protection devices for electronic applications, including computer interface ports and peripherals. Current ratings from 300 mA to 2.5 A, voltage ratings 15–69 V and resistance ratings as low as 100 mΩ.

Raychem Ltd, Faraday Road, Dorcan, Swindon SN3 5HH. Telephone 01793 528 171 Fax 01793 572 276.

70 ns sample-and-hold

A monolithic sample-and-hold amplifier that can enhance analogue-to-digital conversion total harmonic distortion by 5–10 dB to let designers use lower cost ADCs and stiull meet system pereformance objectives is now available from

Harris Semiconductor, Riverside Way, Camberley GU15 3YQ Telephone 01276 686 886 Fax 01276 682 323

Reed relays

Reliable switching is provided by Series 182A and Series 182C moulded reed relays that are available with 5 V, 12 V and 24 V d.c. nominal coil voltages and 2000 V coil/contact breakdown voltage. Switch ratings for Series 182A are 240 V a.c., 300 V d.c., 500 mA, 10 W; for Series 182C: 200 V d.c., 250 mA, 3 W. The max. initial contact resistance is 200 mΩ in both series.

AX Electronic Component Distribution, Unit 22, Lawson Hunt Industrial Park, Guildford Road, Broadbridge Heath, Horsham RH12 3JR. Phone 01403 240 055. Fax 01403 255 657.

New range of controllers

A new micromodule, 16/32 bit, 68 k controller measuring 100×118 mm contains a prototyping area on which users can add their own circuitry for those special jobs. Applications are developed on a PC, down loaded to the module and tested in RAM or EEROM memory. Up to 1 Mbyte propgram space is available on board with up to 512 k SRAM. This product will be of particular interest to all 8 bit users who may be running out of power or memory. The one off price is £95.

Cambridge Microprocessor Systems Ltd, Unit 17–18 Zone 'D', Chelmsford Road Ind. Estate, Great Dummow, Essex CM6 1XG. Telephone 01371 875 644. Fax 01371 876 077.

Intelligent multi-function digital panel meters

New panel meters from ITT, the DPM Series, are available in 24 mm and 48 mm high versdions. Each has 34 standard ranges for the measurement of voltage, current and temperature.

ITT Instruments, Jays Close, Viables Estate, Basingstoke RG22 4BW. Phone 01256 311 877. Fax 01256 23659.

New control knobs

A range of new control knobs is available from Rendar, including both plain and graduated types.

Rendar Ltd, Durban Road, South Bersted, Bognor Regis PO22 9RL. Telephone 01243 866 741. Fax 01243 841 486.

New SMD crystal

A new surface-mount crystal, Type CX89F, from ACT has a low profile body that is ≤1.8 mm high. It provides up to 0.5 mW drive and is available in the frequency range 12–100 MHz.

Advanced Crystal Technology, 9 Kingfisher Court, Hambridge Road, Newbury RG14 5SJ. Telephone 01635 528 520 Fax 01635 528 443.

Low charge HEXFETs

International Rectifier has announced a development in its power MOSFET process technology that has reduced the gate charge by up to 40% and the Miller capacitance of its HEXFET power transistors by up to 85%. The new low-charge HEXFETs® offer designers of power switching equipment a lower cost and simpler method for driving transistors at a given frequency. Moreover, this improvement has been achieved without any effect on other device parameters and at no extra cost.

International Rectifier, Holland Road, Hurst Green, Oxted RH8 9BB. Telephone 01883 713215. Fax 01883 714234.