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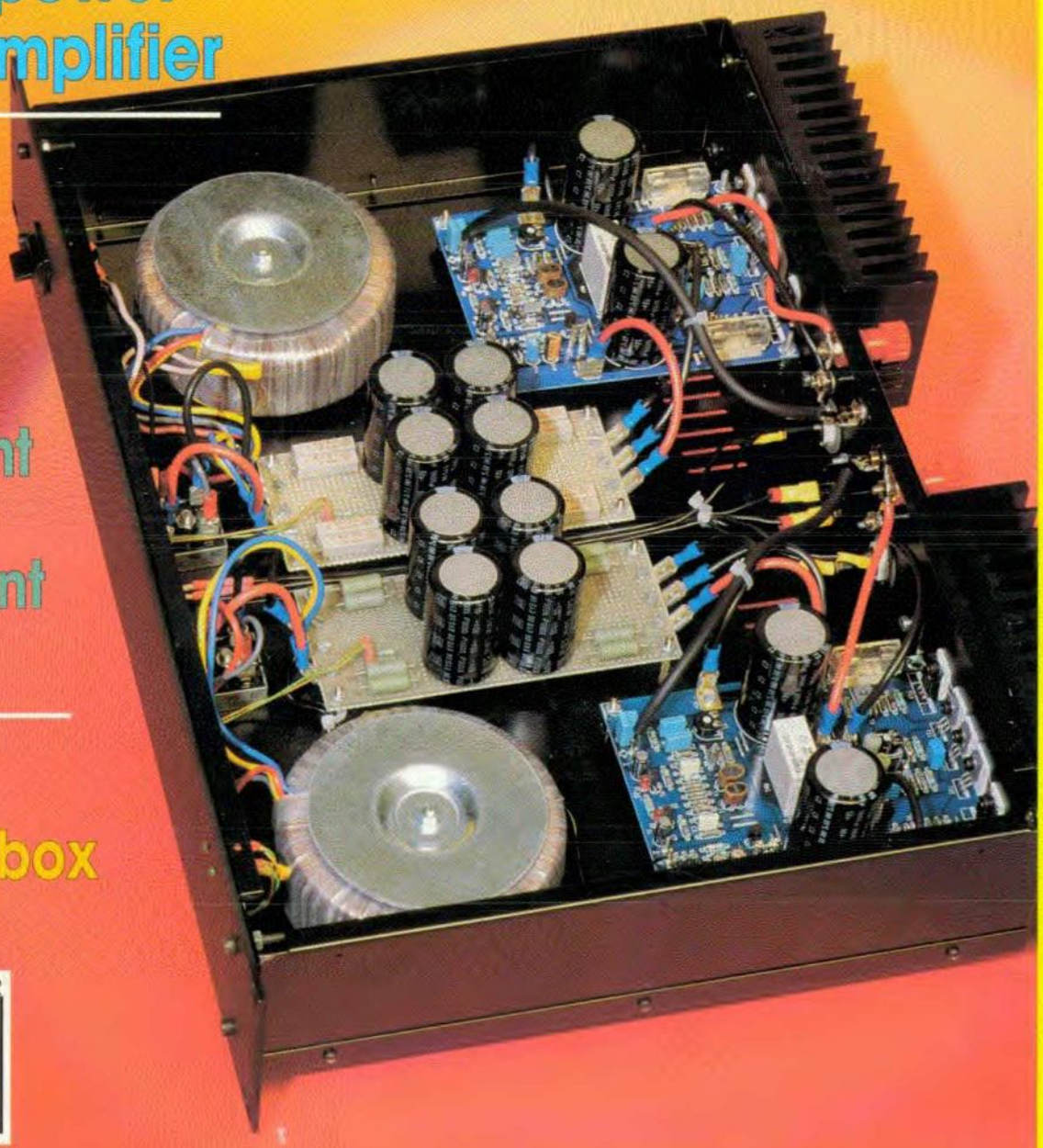
Medium power HEXFET amplifier



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MEDIUM POWER HEXFET AMPLIFIER

Design by T. Giesberts

In spite of their relatively modest TO220 case, the International Rectifier HEXFETs used in the present 60-watt output amplifier can cope with fairly large voltages and currents. The amplifier is absolutely symmetrical from input to output. Its mechanical design is such that it can be accommodated on a fairly small printed-circuit board, including the electrolytic capacitors of the power supply.

The design objective was to arrive at a not too complex unit that nevertheless offered excellent performance, was fairly simple to build and could be reproduced relatively easily. The result is a straightforward amplifier without any unnecessary gimmicks.

A bipolar transistor may be considered a current-amplifying device that enables a (relatively) large current to be controlled by a much smaller one. A field-effect transistor (FET) behaves differently: it is a sort of variable resistance whose conduction is controlled by a voltage. It follows that the drives of these devices is quite different: an important consideration in the design of an output amplifier. A bipolar transistor needs a base current before it can function, whereas a FET can be driven almost without any energy. All it needs is a control voltage; the current it draws is negligible. When power FETs first came on to the market, many designers thought that they would simplify the design of output amplifiers beyond belief. That quickly proved to be not so, however, because power FETs have a fairly large capacitance between the gate and the drain/source channel (sometimes of the order of a few nanofards). This means that at high audio frequencies the driver stages need to deliver fairly large transfer currents to keep the bandwidth sufficiently large.

It may well be asked what advantage(s) aFET offers. In a bipolar power transistor, it is difficult to combine high voltage, large current, and wide bandwidth, because its operation must remain within the Safe Operating Area—SOA. It is not enough to just look at the peak voltage and current in the relevant data sheet. By virtue of modern production techniques, FETs can be fabricated that can handle high voltages (100 V and more) and, in spite of their modest dimensions, large currents. It is, therefore, much simpler to design an output amplifier with reasonable power output with power FETs than with power transistors. Of course, there are other requirements as well, such as slew rate and matching of complementary semiconductors ...

The circuit

A symmetrical design has the advantage that it minimizes problems with distortion, particularly that associated with even harmonics. Therefore, the input stages consist of two differential amplifiers, T_1-T_2 and T_3-T_4. These use discrete transistors, not expensive dual devices, to keep the cost down. Performance is excellent, particularly if the transistors are matched.

A differential amplifier is one of the best means of combining two electrical signals: here, the input signal and the feedback signal. The amplification of the stage is determined mainly by the ratio of the collector and emitter resistances (in the case of T_1-T_2 these are R_9, R_{10}, R_{11} and R_{12}). These form a sort of local feedback: limiting the amplification reduces the distortion.

Two *RC* networks (R_3-C_3 and R_4-C_4) limit the bandwidth of the differential amplifiers and these determine, to a degree, the open-loop bandwidth of the entire amplifier (which is 6.5 kHz).

Brief technical data

Input sensitivity	1 V r.m.s.
Input impedance	48 kΩ
Power output (1 kHz, 0.1% THD)	63 W into 8 Ω
	105 W into 4 Ω
Music power (500 Hz burst, 5 cycles on 5 cycles off)	68 W into 8 Ω
	120 W into 4 Ω
Power bandwidth (35 W into 8 Ω)	1.5 Hz–125 kHz (+0 dB, –3 dB)
Slew rate	20 V μs^{-1} (with input filter)
Signal-to-noise ratio (1 W into 8 Ω)	>99 dB (A-weighted)
Harmonic distortion (1 W into 8 Ω)	<0.006% (1 kHz)
(60 W into 8 Ω)	<0.005% (1 kHz)
	<0.05% (20 Hz–20 kHz)
Intermodulation distortion (50 Hz : 7 kHz; 4 : 1)	<0.008% (35 W into 8 Ω)
Dynamic intermodulation distortion rectangular 3.15 kHz + sine wave 15 kHz)	<0.003% (35 W into 8 Ω)
Damping factor (at 8 Ω)	>160 (20 Hz–20 kHz)
Supply voltage	±35 V
Quiescent current (T_{12} and T_{13})	200 mA

The d.c. operating point of the differential amplifiers is provided by two current sources. Transistor T_6, in conjunction with R_{18} and D_2, provides a constant current of about 2 mA for T_1-T_2. Transistor T_5, with R_{17} and D_1, provides a similar current for T_3-T_4. The combination of a transistor and an LED creates a current source that is largely independent of temperature, since the temperature coefficients of the LED and the transistor are virtually the same. It is, however, necessary that these two components are thermally coupled (or nearly so) and they are, therefore, located side by side on the printed-circuit board.

In the input stage, C_1 is followed by a low-pass section, R_1-C_2, which limits the bandwidth of the input to a value that the amplifier can handle. Resistor R_2 is the base resistor of T_1 and T_3. So far, this is all pretty normal. Network P_1-R_7-R_8 is somewhat out of the ordinary, however. It forms an offset control to adjust the direct voltage at the output of the amplifier to zero. Such a control is normally found **after** the input stage. The advantage of putting it before that stage is that the inputs of the differential amplifiers are exactly at earth potential, which means that the noise contribution of their base resistors is negligible.

The signals at the collectors of T_1 and T_3 are fed to pre-drivers T_8 and T_9. Between these transistors is a 'variable zener' formed by T_7 which, in conjunction with P_2, serves to set the quiescent current of the output FETs.

The output of the pre-drivers is applied to T_{10} and T_{11}, which drive HEXFETs T_{12} and T_{13}. This power section has local feedback (R_{30}-R_{31}).

The design of T_{10}–T_{13} is a kind of compound output stage, since the drain of the power FETs is connected to the output terminal. Note that T_{12} is a p-channel FET and T_{13} an n-channel type. Therefore, the stage provides current amplification as well as voltage amplification. The voltage amplification is limited to ×3 by the local feedback resistors (R_{30}-R_{31}). Here again, this feedback serves to reduce the distortion. The overall feedback of the amplifier is provided by R_5-R-C_5.

Fuses are provided in the source lines of the HEXFETs. Power FETs have an inherent current limitation by virtue of their positive temperature coefficient: when the device gets hot, its drain-source resistance rises and this reduces the current through it. The fuses and this property pro-

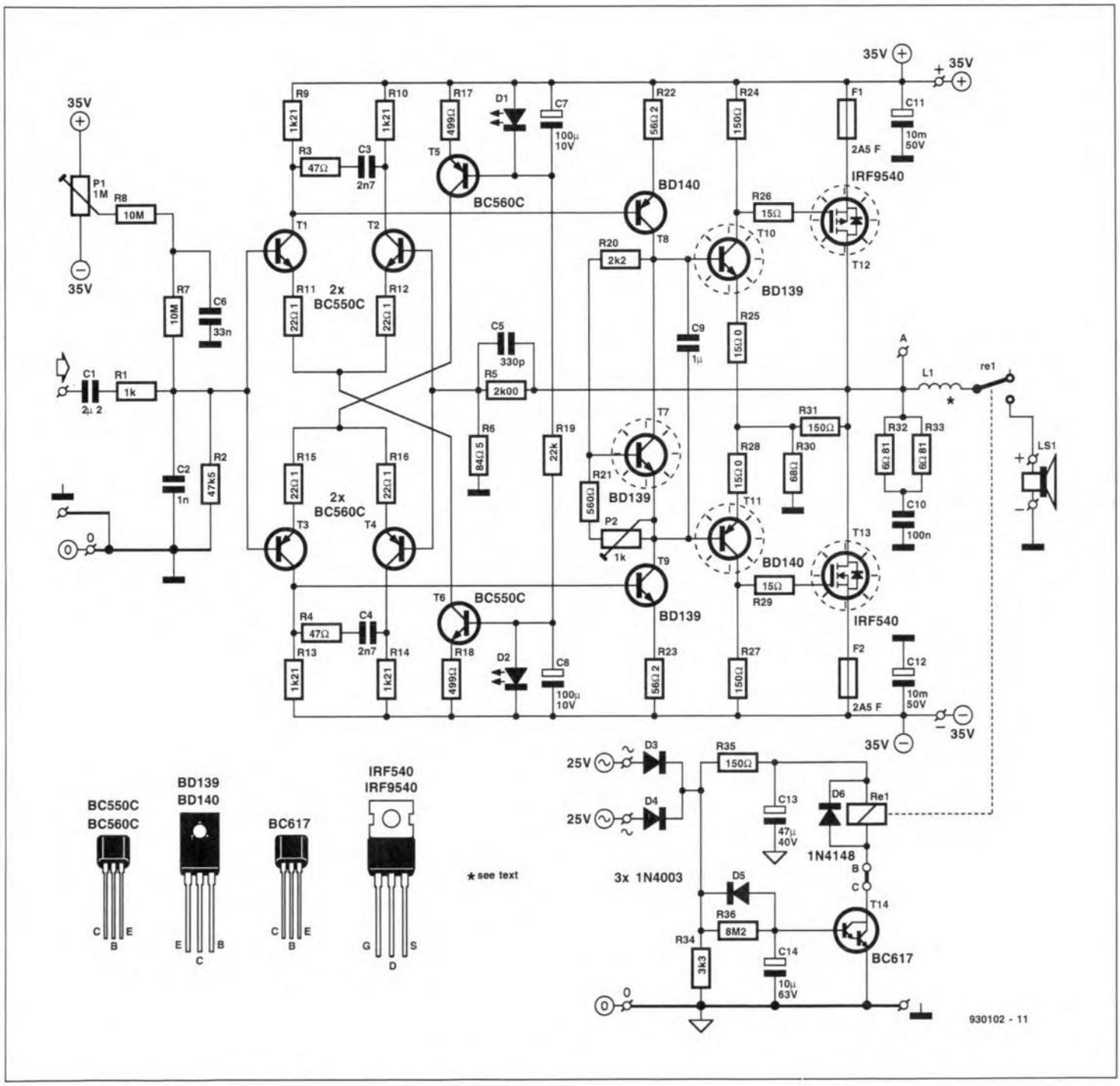


Fig. 1. Circuit diagram of the medium power HEXFET amplifier.

vide adequate protection against brief short-circuits. Note that the HEXFETs used can handle peak currents of up to 75 A. Electrolytic capacitors C_{11} and C_{12} (10,000 µF each and part of the power supply) are located close to the FETs, so that the heavy currents have only a short path to follow.

At the output is a Boucherot network, R_{32}-R_{33}-C_{10}, that ensures an adequate load on the amplifier at high frequencies, since the impedance of the loudspeaker, because of its inductive character, is fairly high at high frequencies.

Inductor L_1 limits any current peaks that may arise with capacitive loads.

The signal is finally applied to the loudspeaker, LS_1, via relay contact Re_1. The relay is not energized for a few seconds after the power is switched on to obviate any plops from the loudspeaker. Such plops are caused by brief variations in the direct supply voltage arising in the short period that the amplifier needs to reach its correct operating level.

The supply voltage for the relay is derived directly from the mains transformer via D_3 and D_4. This has the advantage that the relay is deactuated, by virtue of the low value of C_{13}, immediately the supply voltage fails. The delay in energizing the relay is provided by T_{14} in conjunction with R_{36} and C_{14}. It takes a few second before the potential across C_{14} has risen to a value at which T_{14} switches on. This darlington transistor requires a base voltage of not less than 1.2 V before it can conduct.

The power supply—see **Fig. 2**—is traditional, apart from the resistors, R_5–R_8 in the power lines. These limit, to some degree, the very large peak charging currents to electrolytic capacitors C_{11} and C_{12}. Moreover, together with these capacitors, they form a filter that prevents most spurious voltages from reaching the amplifier. Measurements on the prototype showed that this was particularly evident at frequencies below 500 Hz.

Construction

The design of the printed-circuit board for the amplifier (**Fig. 4**) takes good account of the large currents that flow in the amplifier. This has given rise to a couple of tracks being paralleled instead of combined, so that the effect of currents in the power section on the input stages is minimal.

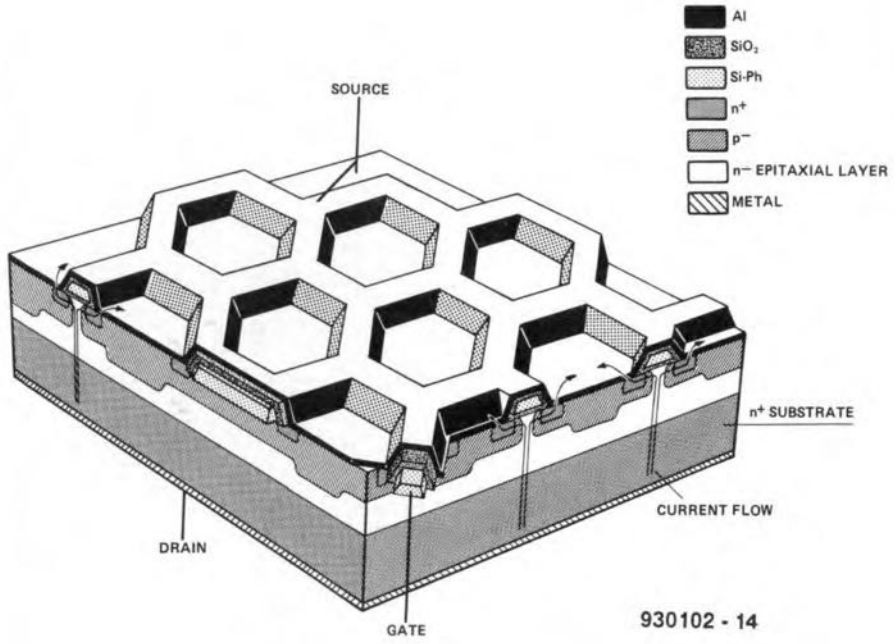
Populating the board is straightforward. Although not strictly necessary, it is advisable to match the transistors used in the differential amplifiers. This may be done conveniently on an h_{fe} tester by measuring the amplification at a collector current of about 1 mA. If such a tester is not available, use a base resistor that results in a collector current of about 1 mA measured with a multimeter. With the same resistor, test a number of other transistors and note the collector currents. Mount the selected pairs on the board and pack them closely together with a 5 mm wide

The HEXFET structure

As implied, the HEXFET structure involves an hexagonal device geometry. At the core is a radically new hexagonal, cellular structure as illustrated. It is this hexagonal geometry, along with advanced MOS processing, that gives the HEXFET an on-state resistance, R_{DSon}, one-third of that possible with the best previous MOSFET technology, in a given die size.

A planar, non-V-groove structure, the HEXFET conducts current vertically. For high packaging density, it uses a silicon-gate structure. The density of the hexagonal source cells on the top surface of the silicon die is over half a million cells per square inch. Electrons flow from a source cell through the channel which is around the periphery of that cell and then into the drain body. The bottom surface of the drain body is in electrical and thermal contact with the holder.

The efficient hexagonal source pattern, the silicon gate, and advanced MOS processing techniques combine to produce the HEXFET's unique performance.



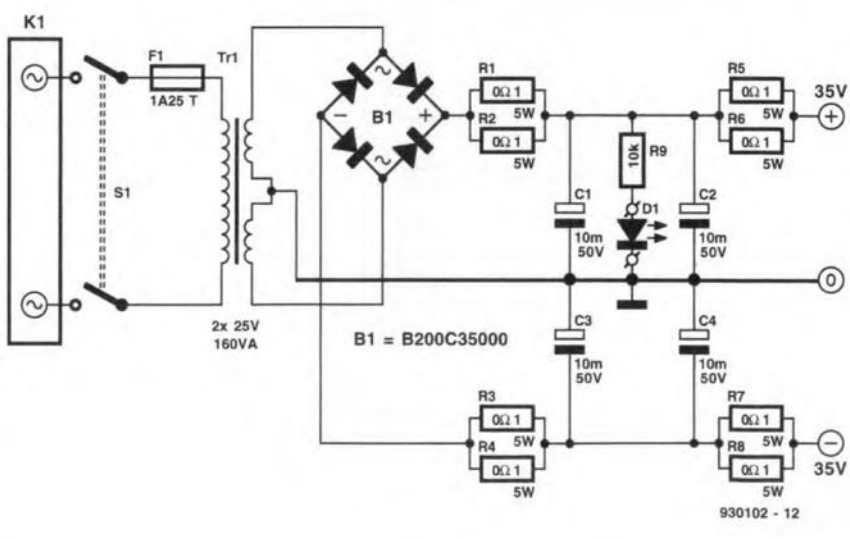


Fig. 2. Circuit diagram of the power supply for the HEXFET amplifier.

copper ring (made from a piece of 12 mm copper water pipe) as shown in **Fig. 5**.

Inductor L_1 consists of six turns, inner diameter 16 mm ($^5/_8$ in), of insulated copper wire 1.5 mm ($^1/_{16}$ in) thick.

The large transistors are located on one side of the board, so that they can be fixed directly to the heat sink. They must be insulated with the aid of ceramic washers.

The two sizes indicated on the board for T_{12} and T_{13} may be ignored: they are a precaution for possible different types of transistor at a later stage.

Connections from the power supply and to the loudspeaker are by means of terminal blocks that can be screwed on to the board.

Mount the two amplifier boards, mains

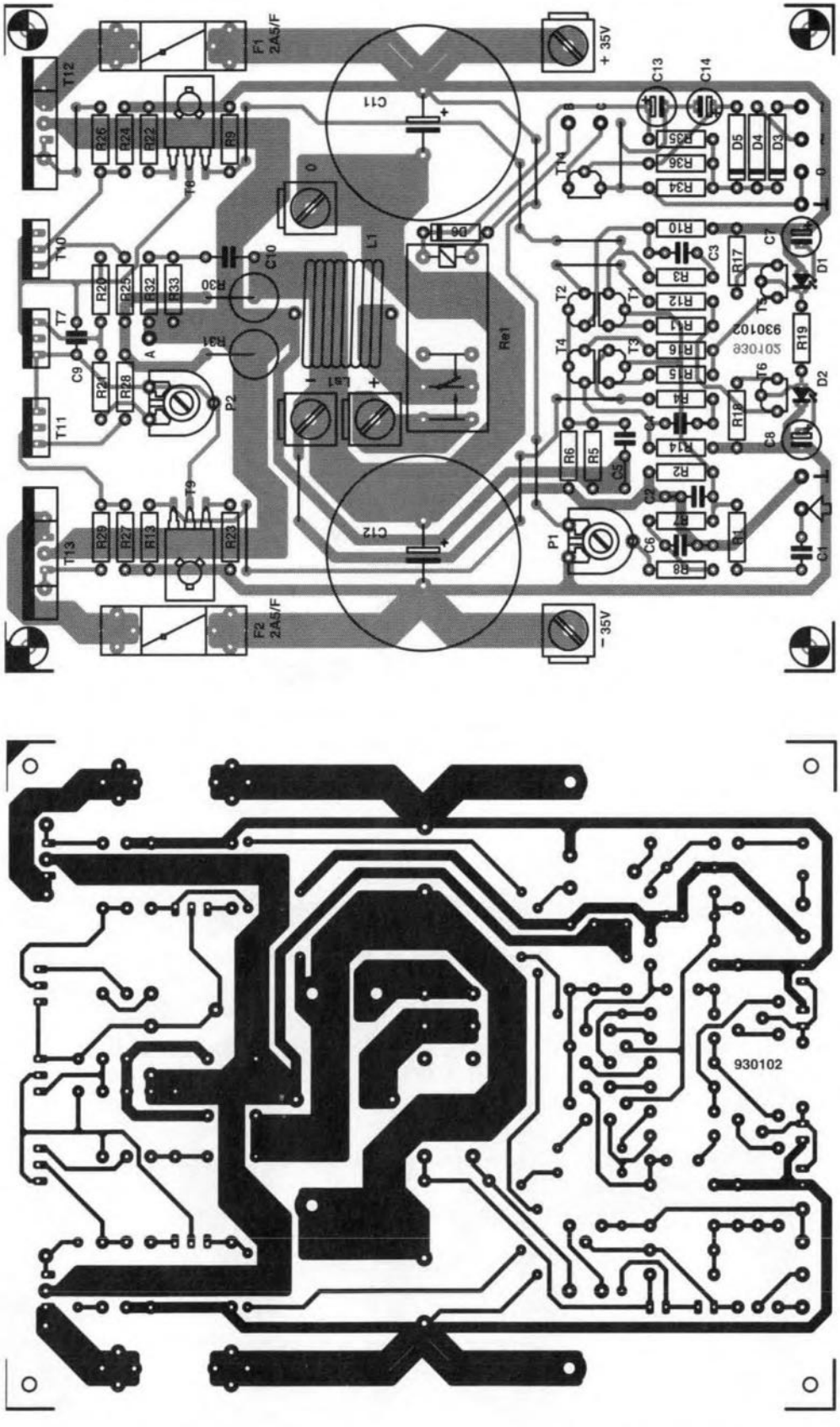


Fig. 3. Printed-circuit board for the medium power HEXFET amplifier.

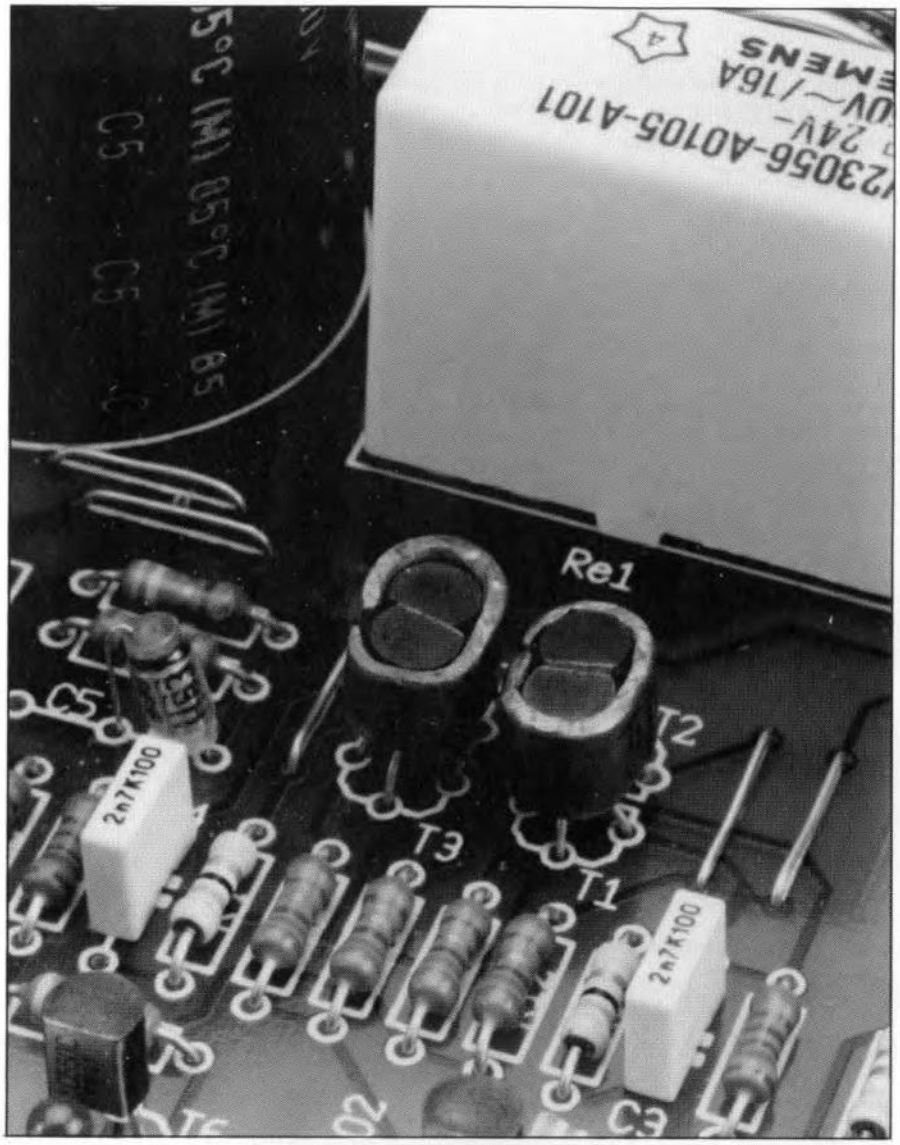


Fig. 4. The differential amplifiers are clamped together with a (DIY) copper ring.

transformers and electrolytic capacitors in a suitable enclosure. The wiring diagram for one channel is given in **Fig. 6**.

It is advisable to measure the supply voltages before they are connected to the amplifiers. Also, turn P_2 to maximum (wiper towards R_{33}) before connecting the power supply to the amplifiers. Set input presets P_1 to the centre of their travel. A few seconds after the supply has been switched on, the relay should come on. Connect a multimeter (1 V direct voltage range) and adjust P_1 until the meter reads zero (both channels!).

Switch the supply off again and insert a multimeter (1 A d.c. range) in one of the supply lines; **do not** substitute it for one of the fuses, since that would affect the operating point of the relevant power FET. Switch the supply on again, wait 5–10 minutes (when the current has stabilized) and adjust P_2 for a meter reading of 330 mA. After about half an hour, the current will remain steady at about 230 mA. The quiescent current through the output transistors is then around 200 mA. Switch off the supply, remove the meter from the supply line and repeat the above procedure with the other channel.

Finally, recheck the direct voltages at the outputs of the amplifiers and, if necessary, readjust P_1 slightly.

The loudspeakers must be 4-ohm or 8-ohm types, whose impedance must not drop below 3 Ω. It is not permissible to connect two 4-ohm units in parallel to the amplifier, because that would give problems when large drive signals are applied to the FETs.

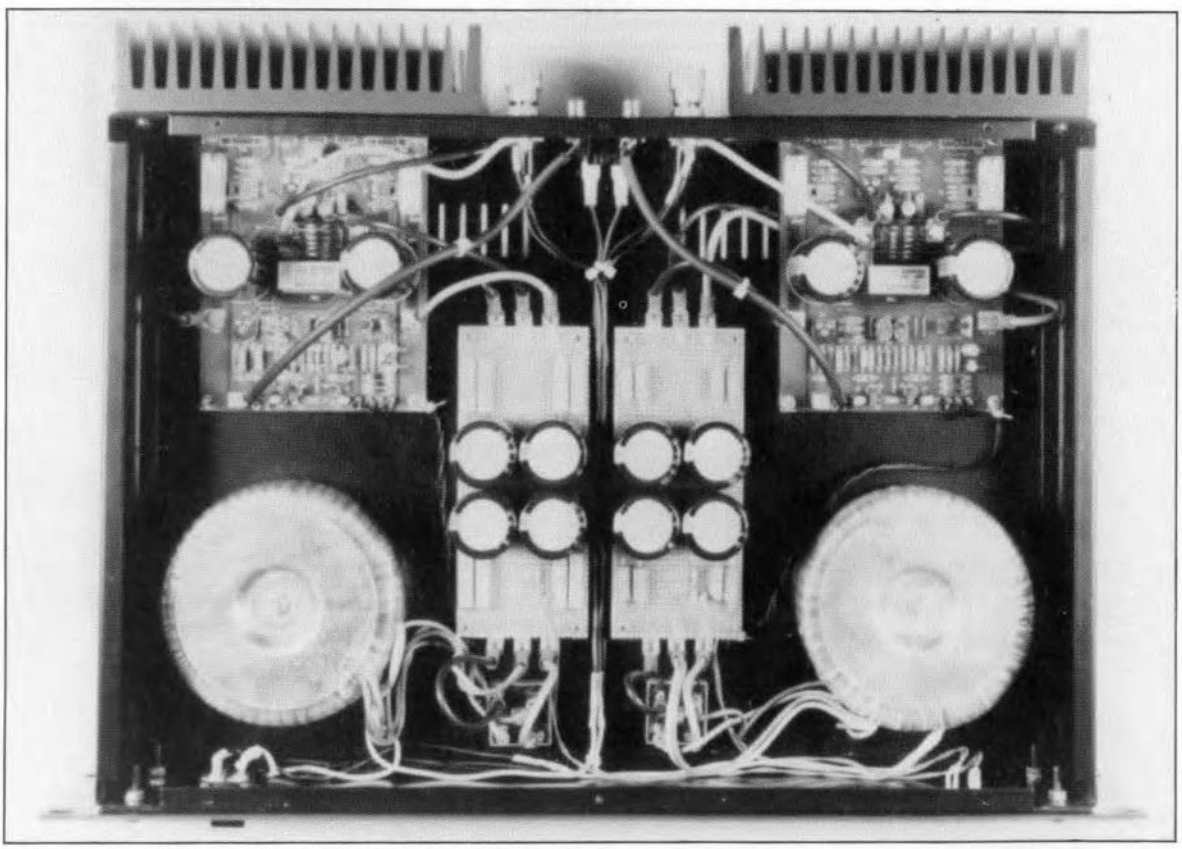


Fig. 5. Top view of the completed amplifier with the enclosure removed.

Parts list (one channel)

Resistors:
R_1 = 1 kΩ
R_2 = 47.5 kΩ, 1%
R_3, R_4 = 47 Ω
R_5 = 2.0 kΩ, 1%
R_6 = 84.5 Ω, 1%
R_7, R_8 = 10 MΩ
R_9, R_{10}, R_{13}, R_{14} = 1.21 kΩ, 1%
R_{11}, R_{12}, R_{15}, R_{16} = 22.1 Ω, 1%
R_{17}, R_{18} = 499 Ω, 1%
R_{19} = 22 kΩ
R_{20} = 2.2 kΩ
R_{21} = 560 Ω
R_{22}, R_{23} = 56.2 Ω, 1%
R_{24}, R_{27} = 150 Ω, 1%
R_{25}, R_{28} = 15.0 Ω, 1%
R_{26}, R_{29} = 15 Ω
R_{30} = 68 Ω, 5 W
R_{31} = 150 Ω, 5 W
R_{32}, R_{33} = 6.81 Ω, 0.6 W, 1%
R_{34} = 3.3 kΩ
R_{35} = 150 Ω
R_{36} = 8.2 MΩ
P_1 = 1 MΩ preset
P_2 = 1 kΩ preset

Capacitors:
C_1 = 2.2 µF, 50 V, MKT
C_2 = 1 nF
C_3, C_4 = 2.7 nF
C_5 = 330 pF, polystyrene, axial
C_6 = 33 nF
C_7, C_8 = 100 µF, 10 V, radial
C_9 = 1 µF
C_{10} = 100 nF
C_{11}, C_{12} = 10,000 µF, 50 V, radial, for PCB mounting
C_{13} = 47 µF, 40 V, radial
C_{14} = 10 µF, 63 V, radial

Inductors:
L_1 = air-core, 0.1 mH (see text)

Semiconductors:
D_1, D_2 = 3 mm LED, red (1.6 V drop at 3 mA)
D_3–D_5 = 1N4003
D_6 = 1N4148
T_1, T_2, T_6 = BC550C
T_3–T_5 = BC560C
T_7, T_9, T_{10} = BD139
T_8, T_{11} = BD140
T_{12} = IRF9540
T_{13} = IRF540
T_{14} = BC617

Miscellaneous:
Re_1 = relay, 24 V, 1 make contact (e.g., Siemens V23056-A0105-A101*)
F_1, F_2 = fuse, 2.5 A, fast, with holder for PCB mounting
Ceramic washers (5) for T_7, T_{10}–T_{13}
Terminal block (5) (see text)
Heat sink, 0.6 K W^{-1} (e.g., Fischer SK85**)
PCB No. 930102 (see p. 110)

Power supply:
Mains transformer, 2 × 25 V, 160 VA
Mains on-off switch with indicator
Fuse 1.25 A, slow with holder
Bridge rectifier Type B200C35000
Electrolytic capacitor (4), 10,000 µF, 50 V
Resistor (8) 0.1 Ω, 5 W

* ElectroValue, 3 Central Trading Estate, Staines, TW18 4UX, L (0784) 442 253. Private customers welcome.

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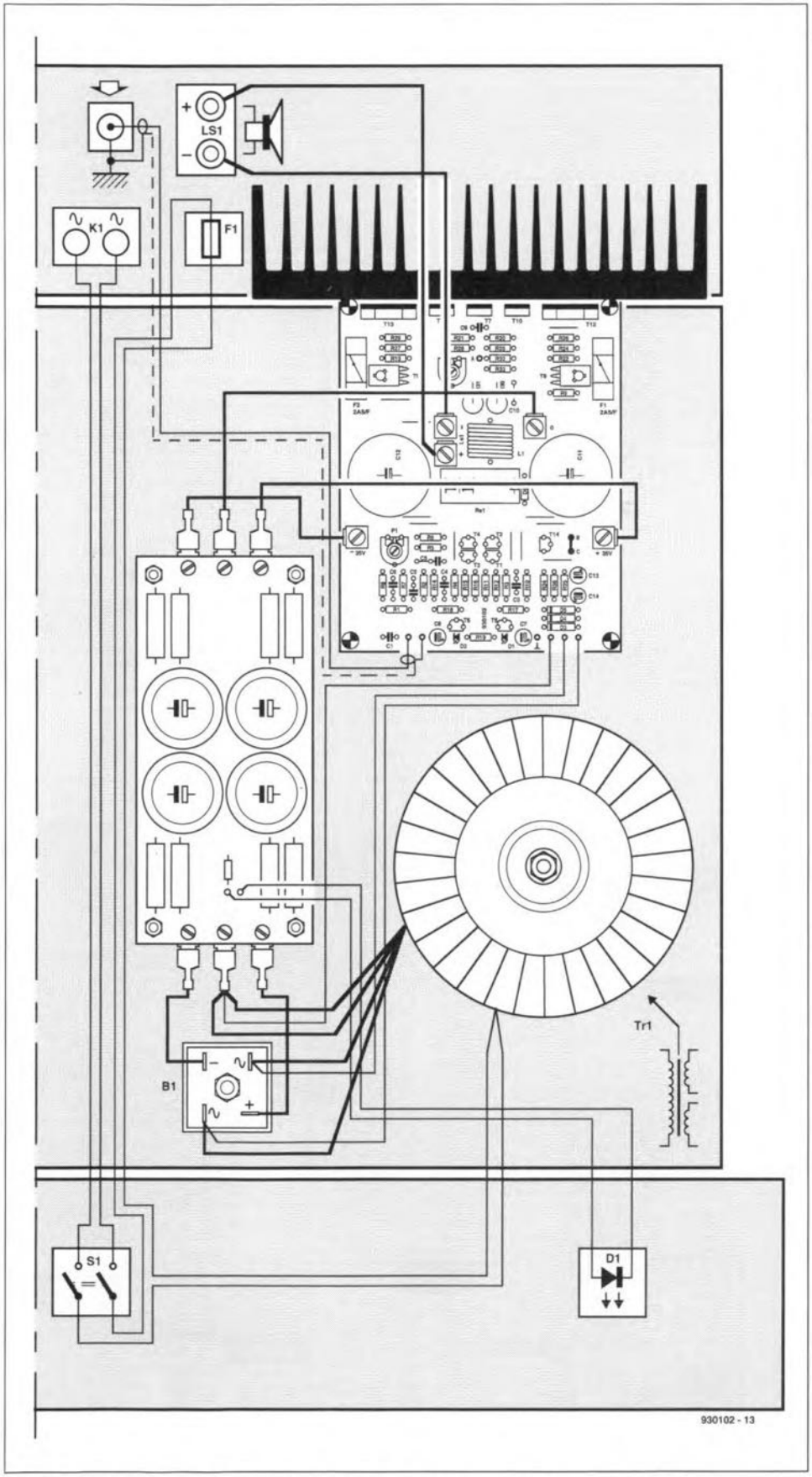
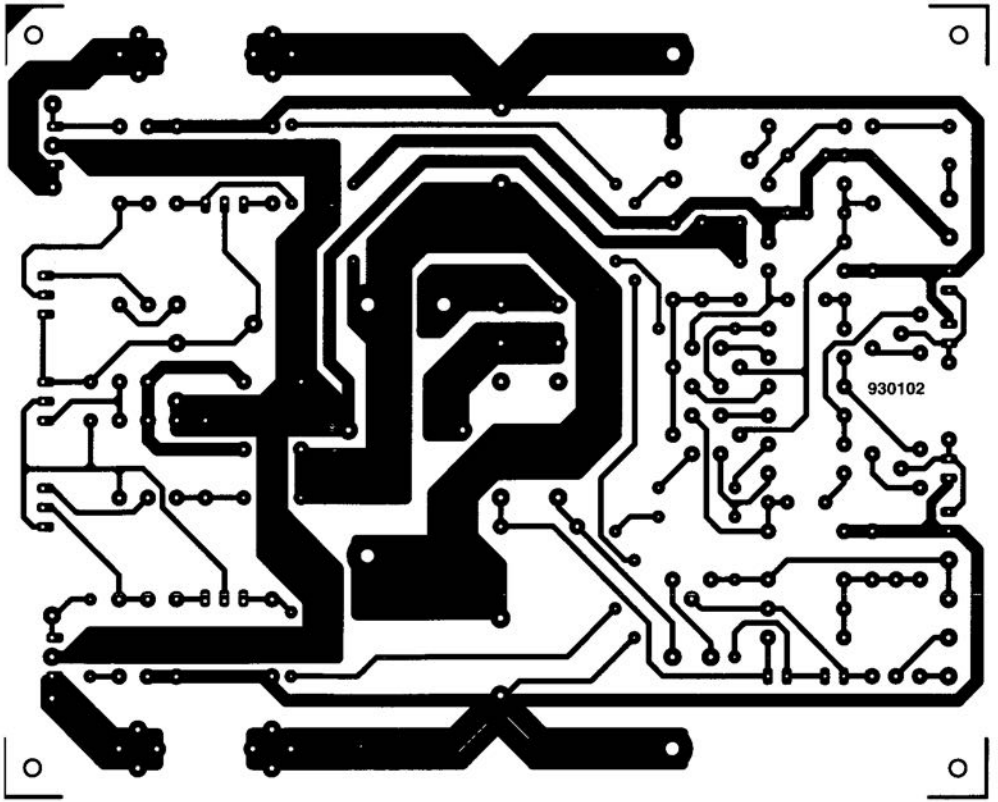


Fig. 6. Wiring diagram of one channel of the medium power HEXFET amplifier.


930102

535 CARD WITH EPROM EMULATOR (PART 2)

Although there is also a signal on the $\overline{\text{ACK}}$ line of the Centronics interface in emulator mode (unless JP6 is swapped), this of little consequence because the BUSY line is held high permanently in run mode. If you use P4.0 as an input, make sure that the line does not short-circuit the output of your application when 'emulator' mode is used. It is, therefore, recommended to drive P4.0 from an open-collector or open-drain output. This avoids the risk of short-circuits, while a pull-up resistor is not required because it is already contained in the controller.

If you want to use the Centronics input in an application, do remember that the circuit is switched to emulator

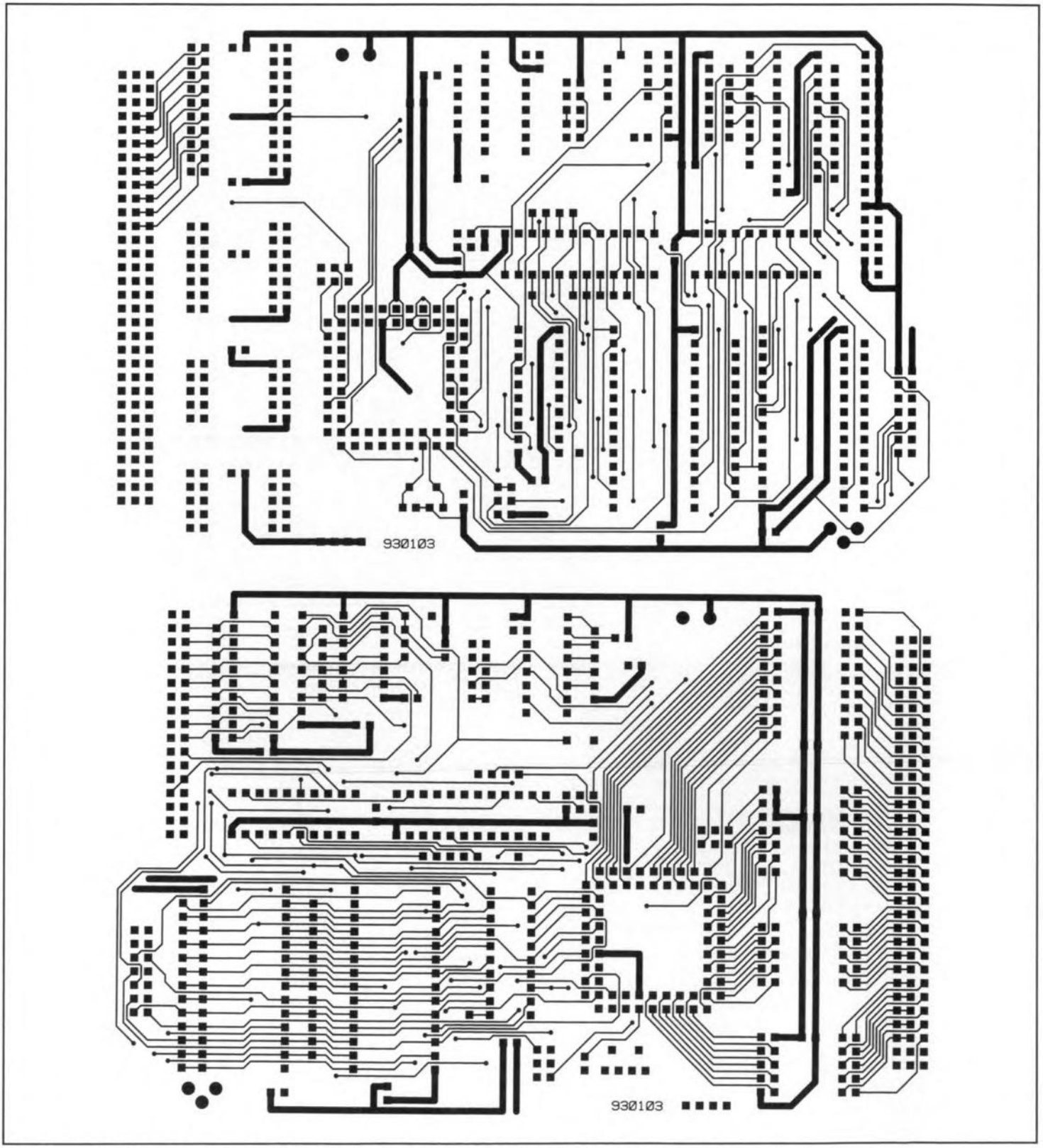


Fig. 3a. Track layouts of the double-sided through-plated printed circuit board designed for the 535 system.

mode when a strobe pulse is received. Since it not normally possible to copy data into the data latch without making use of the strobe pulse, the jumper shown in the block diagram must be swapped to enable a program to be tested. Once that is done, the GAL can no longer switch the circuit to emulator mode. The same jumper is also swapped if EPROM instead of RAM is used for the program memory.

The 535 system

The circuit diagram of the 535 system, **Fig. 2**, is basically a worked out copy of the block diagram, with only a few extra details that require explanations. Among these details are the test points marked with 'P's and the signal name.

The 535 board may be built in two versions: with emulator or without emulator. The version with emulator is typically used to test software for applications of the 535 board. Once the test and debugging phases have been completed successfully, the software may be burned into EPROM for use on a 535 system without an emulator function. The difference between the two versions is, of course, the presence of the parts required for the emulator function. In a system without emulator function, components U5, U8, U9, RP1, ST6, R2, R5 and C24 may be omitted, while pins 8 and 9 of the socket for U9 are interconnected. Note, however, that the GAL (U5) and the PROM (U6) for this project are always supplied as a set, i.e., these parts can not be ordered separately.

As a consequence of the user being able to configure the system with or with an emulator function, provision must be made to use RAM or (EP)ROM respectively for the program memory. Because there are two differences in the pin order of 32-kByte RAMs and

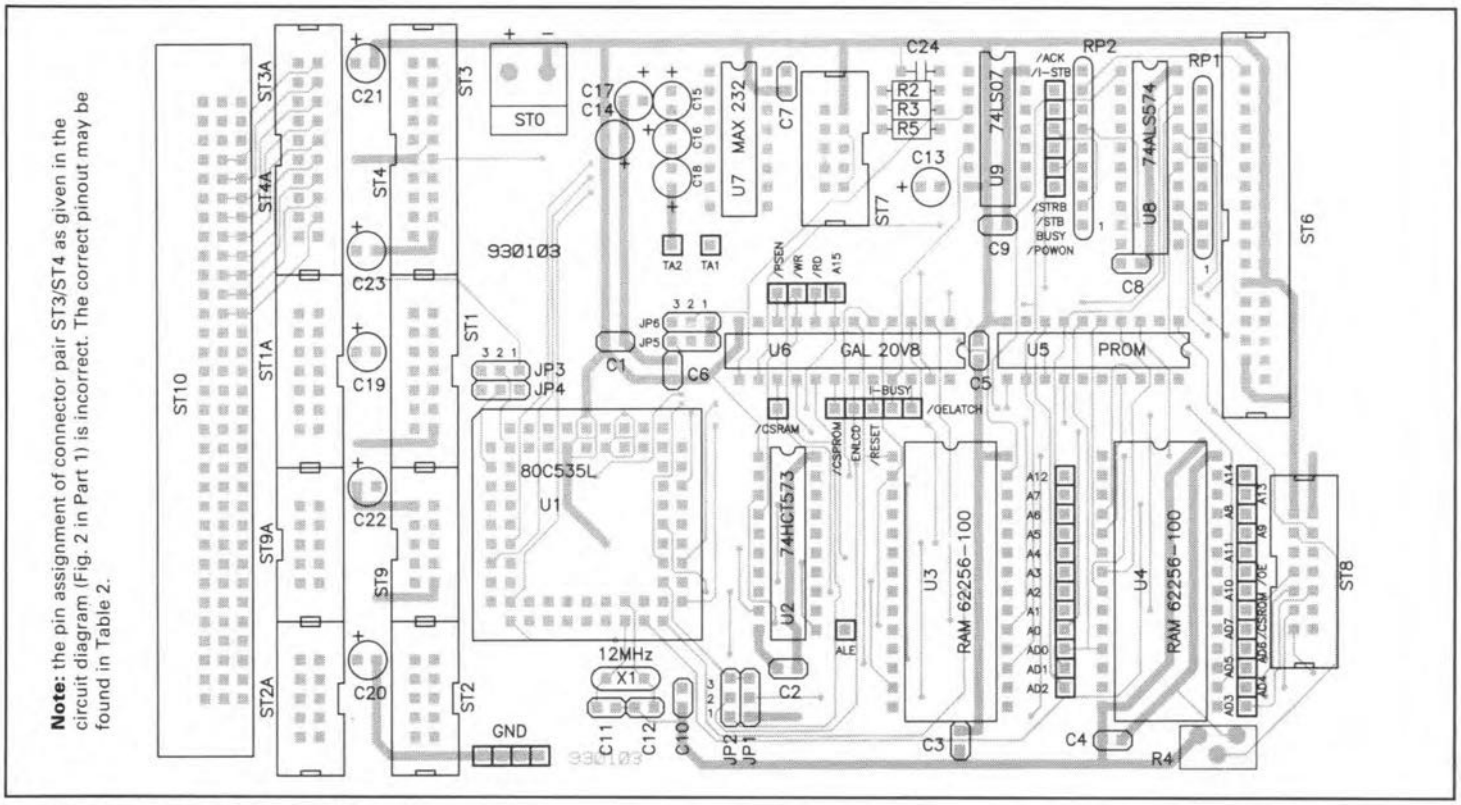


Fig. 3b. Component mounting plan.

COMPONENTS LIST

Resistors:

1	2kΩ2	R2
1	10kΩ	R3
1	10kΩ preset H	R4
1	10Ω	R5
2	8-way 10kΩ SIL array	RP1;RP2

Capacitors:

10	100nF	C1-C10
2	27pF	C11;C12
1	10µF 6V3 tantalum	C13
3	10µF 6V3	C14;C15;C17
2	10µF 16V	C16;C18
5	1µF 6V3	C19-C23
1	4nF7	C24

Semiconductors:

1	SAB80C535L	U1
1	74HCT573	U2
2	RAM 62256-100	U3;U4
1	PROM TBP28L22*	U5
1	GAL 20V8-15*	U6
1	MAX232	U7
1	74LS574	U8
1	74LS07	U9

IC-sockets:

1	68-pin PLCC	
2	28-pin	
1	24-pin, 0.3" wide	
3	20-pin	
1	16-pin	
1	14-pin	

Miscellaneous:

6	3-way pin header with jumper	JP1-JP6
1	12MHz quartz crystal	X1
1	2-way PCB terminal block, pitch 5mm	ST0
5	10-way boxheader	ST2;ST2A; ST7;ST9;ST9A
3	14-way boxheader	ST1;ST1A;ST8
4	20-way boxheader	ST3;ST3A;ST4; ST4A
1	96-way DIN41612 connector (a-b or a-c row)	ST10
1	Press-key, make contact (reset)	
1	Printed circuit board 930103*	

* PROM U5, GAL U6 and the PCB for this project are available as a set under order code 930103. The PROM and GAL are also available separately under order code 6311. Price and ordering information on page 110.

Options:

LCD-module, e.g., LM093LN (Hitachi) or compatible type.
MCS51 assembler course software:
1661 MSDOS version
1681 Atari version

```
        segment code

;-------------------------------------------------------------------------------

LCD_Base equ 8800h
LCD_IWR  equ LCD_Base+0
LCD_DWR  equ LCD_Base+1
LCD_IRD  equ LCD_Base+2
LCD_DRD  equ LCD_Base+3

;-------------------------------------------------------------------------------

LCD_Wait        macro

        mov     DPTR, #LCD_IRD
Busy:   movx    A, @DPTR
        jb      ACC.7, Busy

                endm

;-------------------------------------------------------------------------------
; *****************************************************************************
; LCD_Init
;
; Initiated the LC-Display
;
; Call without parameter at the beginning of the program
; *****************************************************************************

LCD_Init:
        push DPH
        push DPL
        push ACC

        mov   DPH, #01Eh                ; wait > 15ms
        mov   DPL, #000H
LCD_K_wait0:
        djnz  DPL, $
        djnz  DPH, LCD_K_wait0
        mov   DPTR, #LCD_IWR
        mov   A, #00111000b             ; Function Set
        movx  @DPTR, A

        mov   DPH, #008h                ; wait > 4,1ms
        mov   DPL, #000H

LCD_K_wait1:
        djnz  DPL, $
        djnz  DPH, LCD_K_wait1
        mov   DPTR, #LCD_IWR
        mov   A, #00111000b             ;Function Set
        movx  @DPTR, A

        mov   DPH, #001H                ; wait > 100us
        mov   DPL, #033H
LCD_K_wait2:
        djnz  DPL, $
        djnz  DPH, LCD_K_wait2
        mov   DPTR, #LCD_IWR
        mov   A, #00111000b             ;Function Set
        movx  @DPTR, A

        LCD_Wait                        ;LCD busy?
        mov   A, #00000110b             ;Entry Mode Set
        mov   DPTR, #LCD_IWR            ;Instruction Write
        movx  @DPTR, A                  ;
        LCD_Wait                        ;LCD busy?
        mov   A, #00001100b             ;Display ON/OFF
        mov   DPTR, #LCD_IWR            ;Instruction Write
        movx  @DPTR, A                  ;
        LCD_Wait                        ;LCD busy?
        mov   A, #00000001b             ;Clear Display
        mov   DPTR, #LCD_IWR            ;Instruction Write
        movx  @DPTR, A                  ;
        LCD_Wait                        ;LCD busy?
        mov   A, #10000000b             ;Set DD RAM Address
        mov   DPTR, #LCD_IWR            ;Instruction Write
        movx  @DPTR, A                  ;

        pop ACC
        pop DPL
        pop DPH
        ret

; *****************************************************************************
; LCD_Write_Char
;
; Writes a Character on the LC-Display
;
; Call with Parameter (Character) in ACC
; *****************************************************************************

LCD_Write_Char:
        push DPH
        push DPL

        push ACC
        LCD_Wait                        ;LCD busy?
        pop  ACC
        mov  DPTR,#LCD_DWR              ;Data Write
        movx @DPTR,A                    ;

        pop DPL
        pop DPH
        ret
```

930103 - 13

Fig. 4. Example of an LCD driver for the 535 controller.

EPROMs, jumpers JP1 and JP2 are added. These jumpers may be set to RAM or EPROM, just like JP5 and JP6.

The use of the Centronics interface for the emulator function leaves the controller's serial interface free for your own applications. Note, however, that the controller is capable of receiving and generating TTL level signals only. A MAX232 single-chip TTL/RS232 level converter is, therefore, used to allow the controller to be connected to a standard RS232 port on a PC.

Apart from digital I/O ports, the SAB80C535 also has eight analogue inputs, which are connected to an on-board 12-bit A-D (analogue-to-digital) converter. Jumpers JP3 and JP4 enable you to select either the supply voltage or an external voltage (max. 5 V; via ST1) as the ADC reference.

Finally, preset R4 acts as a contrast control for the LC display, which is connected to ST8.

Construction

The complete circuit is easily accommodated on a single Eurocard-size (100×160 mm) printed circuit board, which is double-sided and through plated. This board is available ready-made through our Readers Services, together with the programmed GAL and PAL. The artwork for the 535 board is given in Fig. 3. Connectors ST1-ST4 are 'twins', while ST10 is fitted alongside the edge of the board to enable this to be fitted in a 19-inch case, or to be connected to another board. Connectors ST1A to ST4A enable the connection of ST1-ST4 and ST9 to ST10 to be 'tailored' to requirements. This is useful when the card is to be connected to an existing system. If you are not bound by an existing system, simply make the connection go straight across the board using two press-on (IDC) sockets and a length of flatcable. The relevant pin connections are given in **Table 2**.

If it is desired to fit the board into a 19-inch enclosure, special attention should be given to connectors ST0, ST2(A), ST3(A), ST8, and resistor R4. These parts are located close to the board edge, and make it impossible to use the card guides normally present in 19-inch racks. You may just be lucky with ST8 and R4, but lacking space for the boxes, ST2(A) and ST3(A) will have to be changed into normal pin headers. Also, PCB terminal block ST0 may have to be turned 180° to enable the supply wires to be inserted from the centre of the board.

The connection order of 34-way boxheader ST8 is identical to that of the Centronics connector, with the exception of two missing pins (36-way

box headers do not exist). This does not cause problems if you use a length of flatcable between ST8 and the Centronics connector, making sure that pin 1 on one connector goes to pin 1 of the other (use the single coloured wire on one side of the flatcable for this purpose). Pins 18 and 36 of the Centronics connector are not used. Also, remember that there is no pin-for-pin correspondence between the Centronics connector at the side of the 535 system and the 25-way sub-D connector at the side of the PC. Therefore keep in mind that some wires will have to be crossed if you use a flatcable to establish the connection between ST8 and the PC's printer port. The best way to avoid all problems in this regard is to use a ready-made IBM PC parallel printer cable, which is often cheaper than two connectors and a length of flatcable.

Software

Like many other microcontroller boards, the present 535 system board is not more than the basis of a larger circuit designed to perform a certain function in conjunction with dedicated software. An example of a circuit based on a 80C535 microcontroller core is the Watt-hour meter (Ref. 2).

As already mentioned, you will need an assembler to be able to produce software for the 535 board. Fortunately, MCS51 assemblers come in a wide variety of levels and capabilities. If you are on a tight budget, do consider the assembler contained on the '8051/80C32 assembler course' diskette (Ref. 3), which is good value for money. Note, however, that the examples on this course disk may require small modifications because of the different memory structure of the 535 board.

A programming example specifically written for the present 535 board is given in **Fig. 4**. This is the listing of an LCD driver, which may be used to write messages on to the LCD that tell you what has happened during the course of a program under development. Alternately, such messages many be written to the PC via the RS232 interface on the 535 board. The routine shown in **Fig. 4** has been written with a so-called macro assembler, which enables frequently called, small, program chunks to be defined only once. An example of such a macro is found at the top of the listing. Unfortunately, the assembler mentioned above does not support the use of macros. Consequently, the three individual instructions that make up the macro (LCD_Wait) must be repeated at every location this macro appears in the program. ■

References:

1. I^2C alphanumerical display. Elektor Elec*tronics* September 1993.

2. Watt-hour meter. *Elektor Electronics* February 1993.

3. 8051/8032 assembler course. *Elektor Electronics* February through November 1992. Disk/EPROM order code: 1661 (see page 70).

signal	pin		signal		pin					pin	signal
					row a	ST10				row b/c	
					1					1	
					2					2	
	ST2					ST2A					
P1.0	2	1	+5V		3	2	1			3	+5V
P1.2	4	3	P1.1		4	4	3			4	P1.1
P1.4	6	5	P1.3		5	6	5			5	P1.3
P1.6	8	7	P1.5		6	8	7			6	P1.5
GND	10	9	P1.7		7	10	9			7	P1.7
	ST9					ST9A					
P3.7	9	10	GND		8	9	10			8	GND
P3.5	7	8	P3.6		9	7	8			9	P3.6
P3.3	5	6	P3.4		10	5	6			10	P3.4
P3.1	3	4	P3.2		11	3	4			11	P3.2
+5V	1	2	P3.0		12	1	2			12	P3.0
	ST1					ST1A					
AN0	2	1	+5V		13	2	1			13	+5V
AN2	4	3	AN1		14	4	3			14	AN1
AN4	6	5	AN3		15	6	5			15	AN3
AN6	8	7	AN5		16	8	7			16	AN5
GND	10	9	AN7		17	10	9			17	AN7
GND	12	11	VAGND		18	12	11			18	VAGND
GND	14	13	VAREF		19	14	13			19	VAREF
	ST3/ST4					ST3A/ST4A					
P4.7	19	20	GND		20	19	20			20	GND
P4.5	17	18	P4.6		21	17	18			21	P4.6
P4.3	15	16	P4.4		22	15	16			22	P4.4
P4.1	13	14	P4.2		23	13	14			23	P4.2
+5V	11	12	P4.0		24	11	12			24	P4.0
P5.0	9	10	+5V		25	9	10			25	+5V
P5.2	7	8	P5.1		26	7	8			26	P5.1
P5.4	5	6	P5.3		27	5	6			27	P5.3
P5.6	3	4	P5.5		28	3	4			28	P5.5
GND	1	2	P5.7		29	1	2			29	P5.7
					30					30	
					31					31	
					32					32	

Table 2. Connector pinning overview to help you find signals on the board.

USER INSTRUCTIONS

Load emulator RAM:

1. Connect the printer port on your PC to the Centronics input on the 535 board.
2. Switch on the 535 board, which then waits for the first program to be downloaded.
3. On the PC, type
   COPY <file> PRN: /b
   to print the program to the 535 board in the form of a binary file. The /b switch prevents the COPY command from interpreting the value $1A_H$ as an end-of-file code.
4. The emulator program on the 535 board automatically loads the received data into the program memory, starting at 0000_H.
5. One second after the last received byte, the processor is reset, and the downloaded program is started from 0000_H.
6. The running program is interrupted by a reset when the PC sends new data. Next, the emulator program (downloader) contained in PROM is started again. Steps 3, 4 and 5 follow.
7. The effect of pressing the reset button depends on the program executed by the controller. With the emulator program (downloader) running, the Centronics BUSY signal is reset, and the load routine is initialized. Loading will continue from address 0000_H. With the controller running the program contained in the program memory, pressing the reset key causes a normal system reset. The processor is reset, and the execution of the program starts at 0000_H.

Hardware options:

535 board with emulator

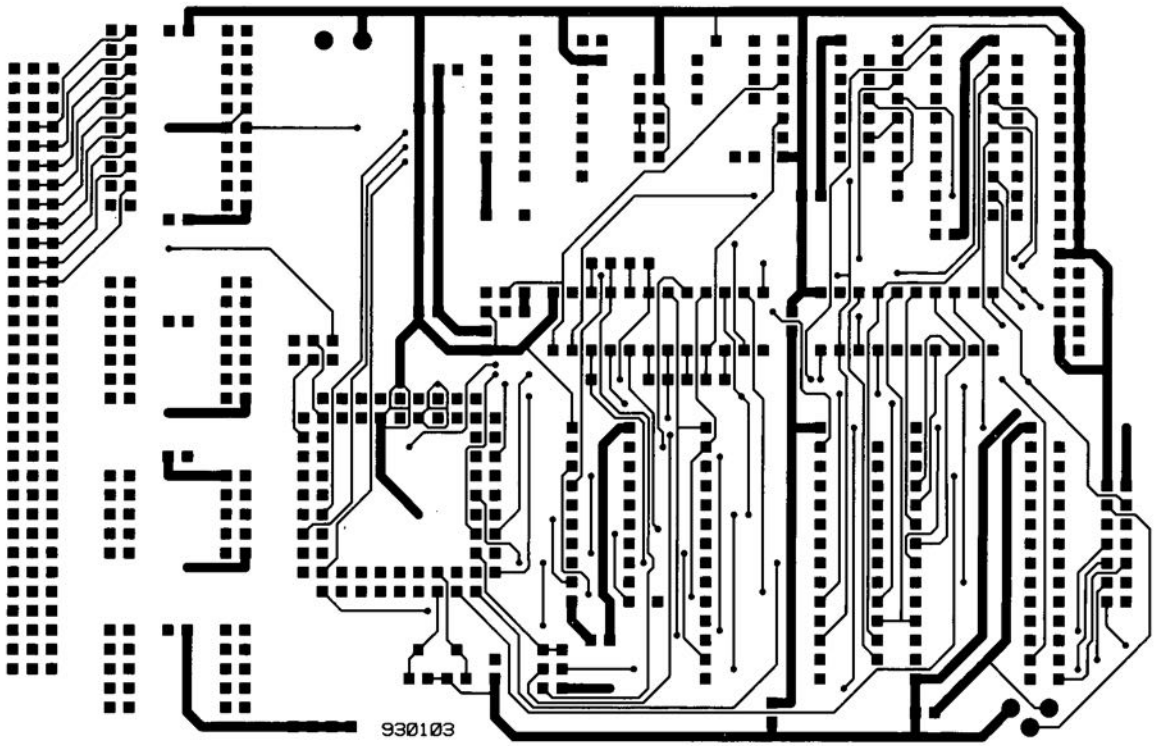
1. IC position U4 has a RAM type 62256.
2. Jumper settings: JP2: 1-2; JP1, JP5 and JP6: 2-3.

535 board with EPROM

1. IC position U4 has an EPROM type 27256.
2. Jumper settings: JP2: 2-3; JP1, JP5 and JP6: 1-2
3. Only if the board is used with a program in EPROM: omit U5, U8, U9, RP2 and ST6. Interconnect pins 8 and 9 of IC socket U9.

Analogue reference voltage

Internally (5 V): JP3, JP4: 1-2.
Externally (max. 5 V): JP3, JP4: 2-3.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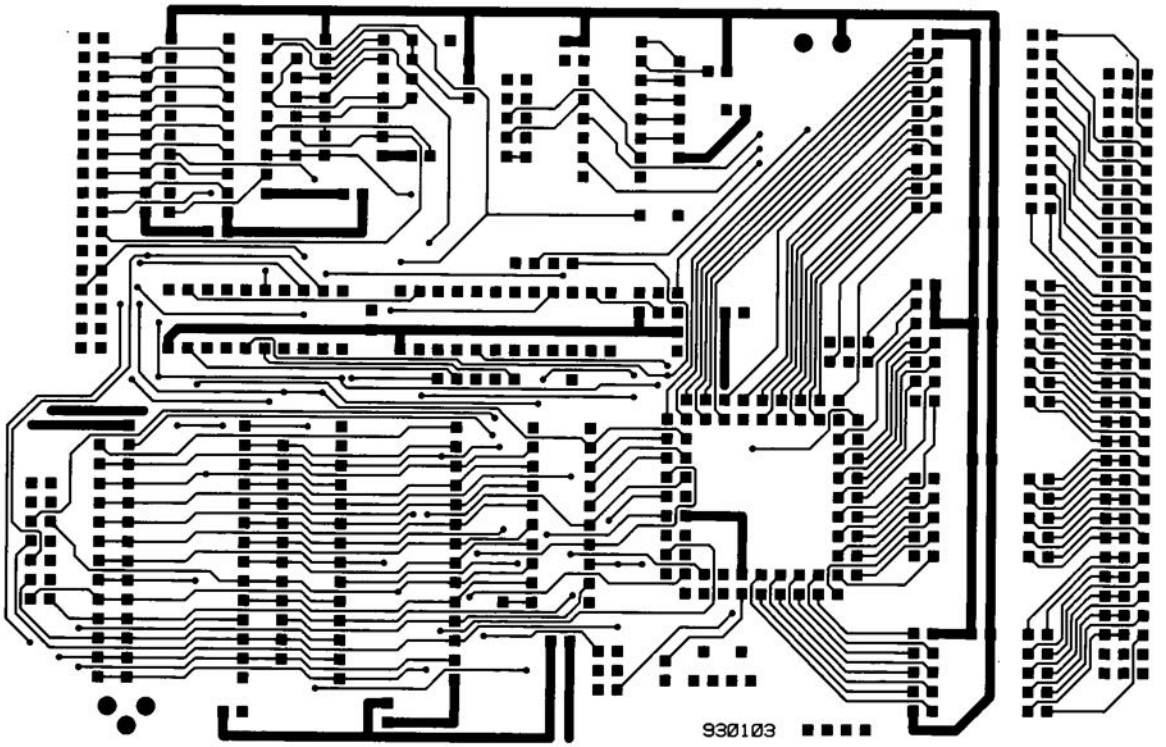
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VIEWS OF THE BRIDGE

Part 1: Power rectification

By Bryan Hart

The diode-quad bridge network is a familiar component in power-supply design. However, the discussion of its operation in the technical literature generally, and in electronics textbooks in particular, is often superficial and a reader can easily get the feeling that 'something is missing' from the explanations. This feeling is intensified in attempting to explain oscilloscope traces of observed circuit waveforms. This article takes a fresh look at the bridge. Part 1 supplies a fuller account of its operation in power rectification than is normally given and Part 2 discusses the wider applicability of this versatile component assembly in the field of instrumentation.

Bridge construction

Figure 1(a) shows two series-connected diodes, D_1 and D_2, arranged in parallel with a similarly connected pair, D_3 and D_4. Note that at this stage all the diodes 'point the same way'. If we now imagine the junction points **A** and **B** to be pulled out in the directions indicated by the arrows, then we arrive at the 'square' (or 'diamond') shape shown in **Fig. 1(b)**. In this more usual form, which we will use from now on, this diode-quad connection is frequently referred to as a 'bridge' by analogy with the well-known Wheatstone bridge component arrangement. An alternative drawing, used in older texts, is shown for completeness in **Fig. 1(c)**. This figure-of-eight representation is not so popular nowadays. Certainly, the diode polarity is not so easily remembered as it is for **Fig. 1b**.

The diode bridge can be purchased as an encapsulated module for power-rectification applications or be constructed from signal diodes, such as the popular general-purpose Type 1N4148, for miscellaneous low-power applications. The intended application determines which of the points **A**, **B**, **X**, **Y** are used as input terminals and which are used as output terminals.

To understand circuit operation, it is sensible engineering practice to assume, initially, that all the components used have ideal characteristics. Thus, the diode of **Fig. 2(a)** is considered 'ideal' if its voltage-current characteristic is described by two straight line sections, (i) and (ii) in **Fig. 2(b)**. As indicated in **Fig. 2(c)**, (i) represents an open circuit, or the open state of that switch. A slightly more realistic model is that giving sections (ii) and (iii) in **Fig. 2(b)**. These can be represented by the switch-battery combination in **Fig. 2(c)**. The battery, U_D, represents the forward voltage drop, assumed constant, of the diode when it conducts. Its value is about 1 V for high-power diodes and 0.7 V for low-power diodes.

Rectifier with resistive load

A basic full-wave power rectifier setup is shown in **Fig. 3(a)**. The input, from the secondary winding of a mains transformer, is connected to points **A** and **B**, and the load, in this case resistor R, is connected between points **X** and **Y**.

The transformer provides d.c. isolation, for safety, and, via the choice of the secondary/primary turns ratio, a means of stepping down the mains voltage without significant power loss.

As indicated in **Fig. 3(b)**, the 50 Hz sinusoidal secondary voltage is assumed to have a peak value of 15 V. At point **J**, $U_{AB} = +10$ V, corresponding to $t_1 = 2.3$ ms; at **K**, $t_2 = 12.3$ ms and $U_{AB} = -10$ V. As the usual assumption of a 'floating' output can be quite puzzling in an explanation of circuit operation for beginners, we will assume that **Y** is connected to a d.c. reference potential, U_r, and, in particular, that $U_r = +5$ V.

Referring to **Fig. 4**, the operation for ideal diodes and $U_{AB} > 0$ is as follows. Diodes D_2 and D_4 in opposite arms of the bridge conduct while D_1 and D_3 are cut off. Conduction in D_4 causes **B** to be held at U_r, so all the variations in secondary voltage appears at **A** and U_X follows U_A. Point J_1 on waveform

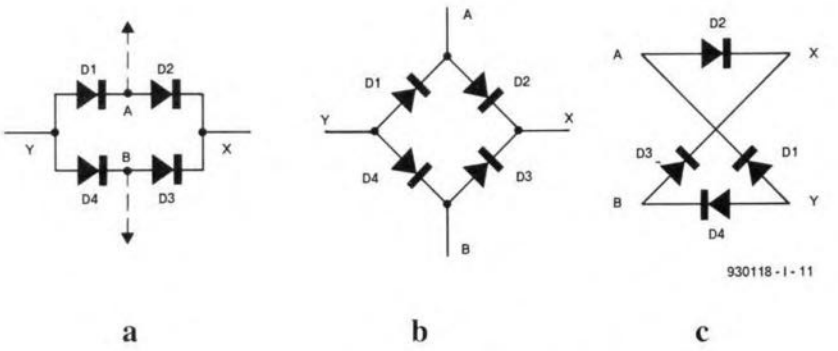


Fig. 1. (a) Bridge representation emphasizing diode polarity; (b) conventional pattern; (c) older 'figure-of-eight' pattern.

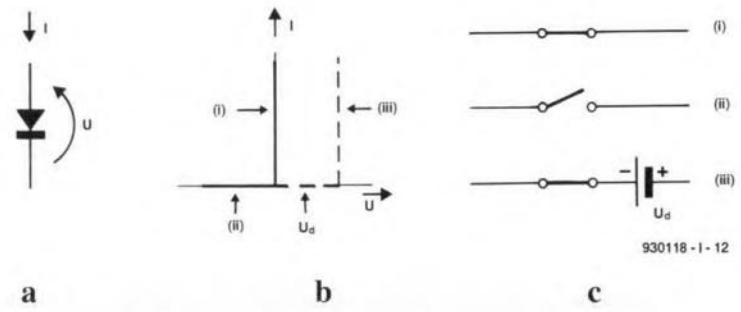


Fig. 2. Diode representation: (a) symbol; (b) current-voltage characteristic; (c) switch equivalents for (b).

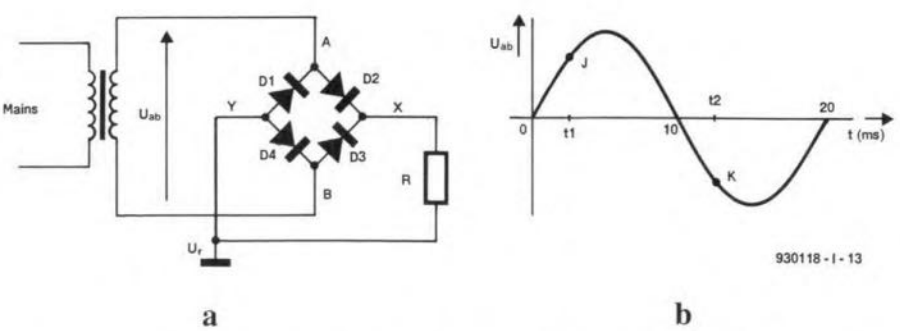


Fig. 3. (a) Bridge rectifier with resistive load; U_r = reference voltage; (b) waveform of transformer secondary voltage.

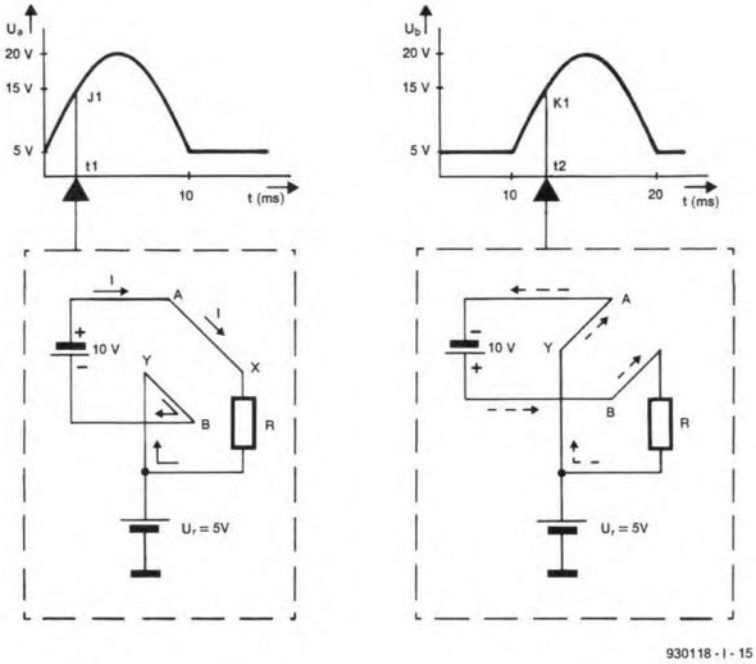


Fig. 4. Waveform for U_A. Boxed section shows instantaneous equivalent circuit at $t = t_1 = 2.3$ ms.

Fig. 5. Waveform for U_B. Boxed section shows instantaneous equivalent circuit at $t = t_2 = 12.3$ ms.

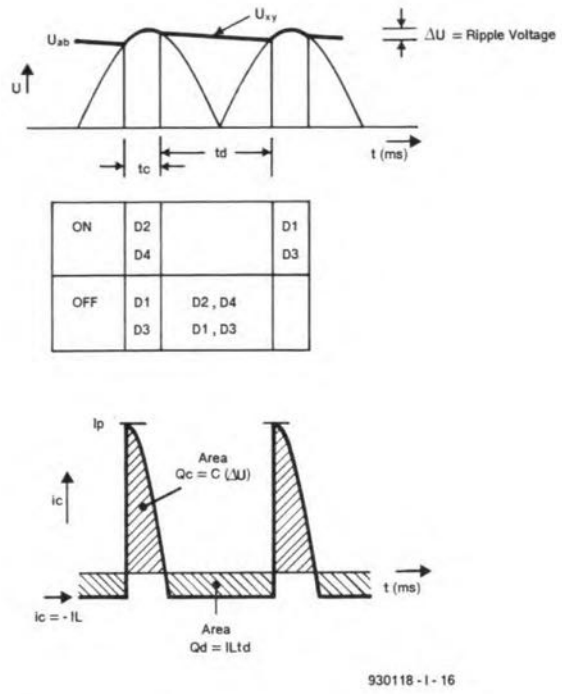


Fig. 6. Rectifier operation with a reservoir capacitor, C, in parallel with R; i_C = current flowing into C.

U_A corresponds to **J** —see **Fig. 3(b)**. An equivalent circuit for instantaneous circuit conditions at t_1 is shown in the boxed section of the diagram in **Fig. 4**. The arrows show the direction of current flow around the circuit. The peak inverse voltage (PIV) rating of each diode must exceed the peak input voltage, 15 V in this case.

Circuit operation for $U_{AB} < 0$ closely mirrors that for $U_{AB} > 0$ and is summarized in **Fig. 5**. In this case, D_1 and D_3 conduct while D_2 and D_4 are cut off; the direction of current flow is shown by the arrows on the broken lines. Conduction in D_4 now holds **A** at +5 V, while U_X follows U_B. Waveforms U_A and U_B are **not** sine waves and, with the present arbitrary choice of U_r = +5 V, neither has a negative section. However, U_{AB} ($= U_A - U_B$) **is** a sine wave. From the waveforms for U_X and U_Y in **Fig. 7(a)** and **7(b)**, we obtain U_{XY} ($= U_X - U_Y$) in **Fig. 7(c)**. The dotted lines show the output obtained when the voltage drop of practical diodes is taken into account.

Although U_X and U_Y in **Fig. 7(a)** and **7(b)** are dependent on U_r, it is significant that U_{XY} in **Fig. 7(c)** is not. Thus, the presence of U_r, introduced for explanatory purposes, is not fundamentally necessary for the production of U_{XY} in practice and can be dispensed with. In that case, the output is said to be 'floating'. More will be said about this later.

Use of a reservoir capacitor

The bold line in **Fig. 6** shows what happens to U_{XY} of **Fig. 7(c)** when a large reservoir capacitor, C, is connected across load resistor R. Waveform U_{XY} is that of U_{AB} with the gaps between the peaks almost filled in. There is only a 'ripple voltage', ΔU, which is normally small compared with the peak value, U_p. Current does not flow in opposite pairs of bridge diodes for half cycles of U_{AB}, but is limited to short intervals t_C in the vicinity of the peaks. During these intervals, the diodes supply a charge $Q_C = C\Delta U$ to C. Conduction ceases when U_{XY} is not able to fall as fast as U_{AB} when C is supplying the full load current, I_L, to R. The magnitude of the charge lost by C in intervals t_D is $Q_D = I_L t_D$. Since $t_D << T/2$, we can write $Q_D = I_L T/2$. Diode conduction recommences when the rising U_{AB} exceeds $U_p - \Delta U$.

After initial switch-on, a state of equilibrium as shown in **Fig. 6** exists when $Q_C = Q_D$.

Voltage ΔU decreases as C is made larger. However, larges values of C mean smaller values of t_C, higher amplitude current pulses and the requirement for more expensive diodes to cater for this.

For equipment design purposes, maximum values of (electrolytic) capacitor C are given in component catalogues that specify the rectification characteristics of bridge asemblies. As an example, consider a bridge rectifier for operation at 50 Hz and a load current that can range from 100 mA to 1 A. The maximum capacitance value is specified as 4700 µF. From these figures, we deduce that

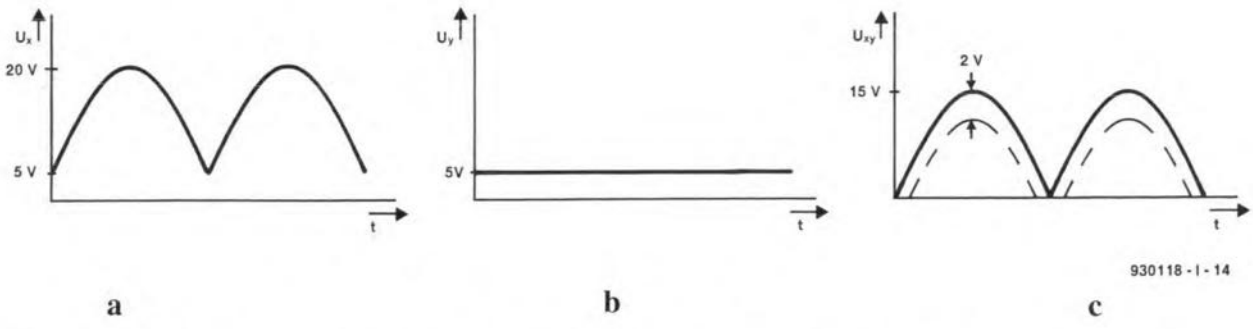


Fig. 7. Other circuit waveforms: (a) U_X; (b) U_Y; (c) U_{XY}. Dotted lines show U_{XY} for finite diode drops.

$Q_{D(max)}$ = 10 (ms) × 1 (A) = 10 mC and $Q_C = 4700\,(\mu F) \times \Delta U = (4700\,\Delta U)\,\mu C$, where ΔU is expressed in V. Equating Q_C and Q_D gives $\Delta U = 2.1$ V (approx). This is the worst ripple case; for I_L = 100 mA, it is 0.21 V.

The simple hydraulic system in **Fig. 8** provides a graphic analogy for rectifier operation with a reservoir capacitor. The tank storing water is similar to the capacitor storing charge and the output pipe fulfils the role of the resistor. A human operator with a bucket, which can be refilled with water as required, plays the part of the transformer and diodes.

A quantity of water, Q_0, flows from the tank through the pipe as the liquid level falls from h_p to $h_p - \Delta h$. When the operator sees that the lower level is reached, he tips a quantity of water, Q_I, from the bucket into the tank. To restore the level to its original value, so that the process can be repeated continually, it is obviously necessary that $Q_I = Q_0$. To make the analogy with bridge operation closer, we should, of course, imagine two human operators with buckets who take it in turn to top up the tank!

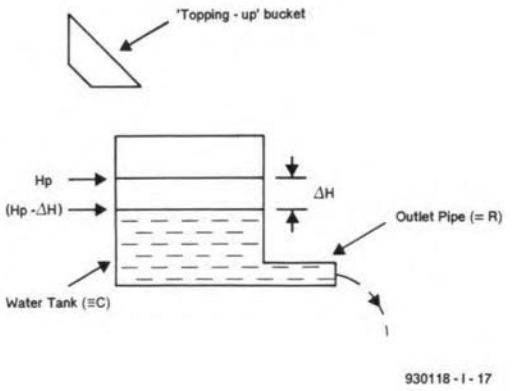


Fig. 8. Hydraulic analogy for Fig. 7.

Application in power supplies

In modern power supply units (PSUs), the bridge rectifier - reservoir capacitor combination is followed by a voltage regulator, a standard catalogue item, as shown in **Fig. 8**. Resistor R is no longer required: its role is taken over by the input circuit of the regulator. The function of the regulator is to reduce the ripple voltage to a negligible value and to produce a d.c. output voltage, U_{cc}, that does not vary by more than a few millivolts when its output current, I_L, changes from zero to its rated maximum value.

For correct operation, the regulator requires to operate above a specified minimum value of $U_{XY} - U_{cc}$, for instance, 3 V. Capacitance C_2, typically a parallel combination of a 10 µF electrolytic capacitor and a 0.1 µF disc capacitor, is used to supply current for load surges.

In **Fig. 8**, U_{cc} is 'floating' in the same sense that the battery voltage for powering a torch is floating. Thus, the potential difference between the terminals of the battery is fixed, but the potential difference between either of its terminals and earth is not.

A third terminal (E) is available on the instrument panel of the PSU in **Fig. 9**. It is connected, for instance via the metal of the casing, to the earth terminal of the mains socket. When used, it takes on the role of U_r discussed earlier. User options, for a single supply and two supplies, are shown in **Fig. 10**. Two PSU outputs may be stacked to produce a higher output voltage than is possible from a single supply. Note that not all commercially available low-cost PSUs have a floating output facility.

The advantages of a bridge rectifier over a conventional two-diode, full-wave rectifier setup are that the transformer is used more efficiently and does not need to have a centre tap. If a centre tap is available, the dual-polarity supply of **Fig. 11** makes a useful circuit arrangement for powering oper-

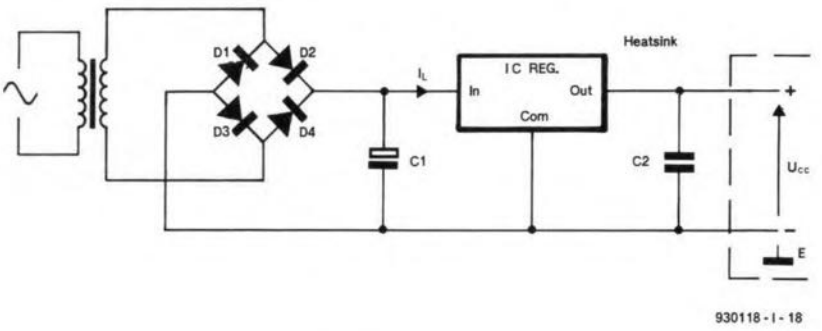


Fig. 9. A regulated PSU with 'floating' output.

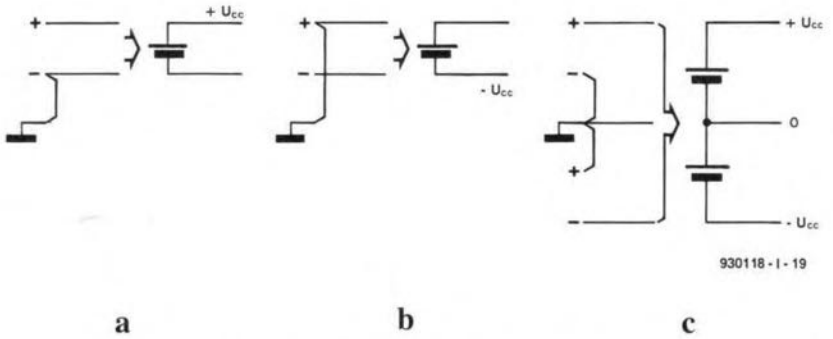


Fig. 10. User options for Fig. 9: (a) positive output; (b) negative output; (c) dual-polarity output with the use of two PSUs.

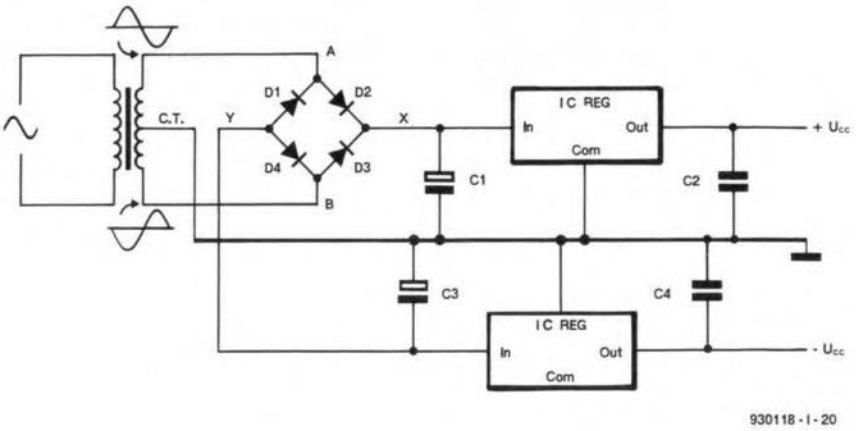


Fig. 11. Dual output PSU using a centre-tap transformer.

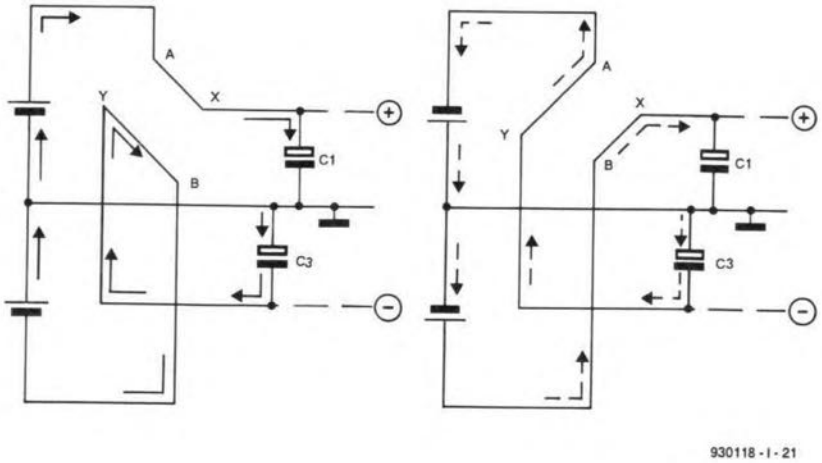


Fig. 12. Instantaneous equivalent circuits for U_{XY} near a peak: (a) $U_{AB} > 0$; (b) $U_{AB} < 0$.

ational amplifiers.

Figure 12(a) shows an instantaneous equivalent circuit, analogous to that of **Fig. 4**, for $U_{AB} > 0$ and near its peak. Similarly, **Fig. 12(b)** is an instantaneous equivalent circuit, analogous to **Fig. 5**, for $U_{AB} < 0$ and near its peak.

In leaving the topic of power rectification, we note that finite voltage drops present no real problems. We can always obtain a higher secondary output voltage from the transformer to compensate from them as shown in the following example. Suppose:

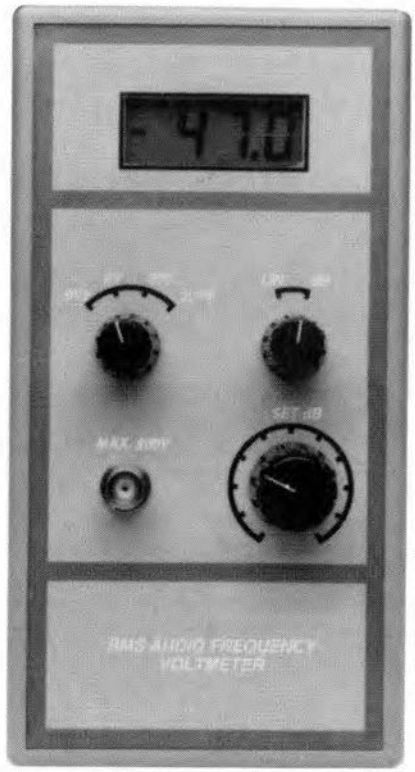
$U_{cc} = 15$ V;
$U_{XY} - U_{cc} \geq 3$ V;
$\Delta U = 1$ V;
$U_D = 1$ V.

Then, taking into account two diode drops, the peak value of U_{AB} must exceed 22 V. A secondary winding providing 20 V_{rms}, corresponding to 28 V_{peak}, is appropriate.

In Part 2, we will consider instrument applications of the diode bridge. In such cases, it is usually constructed from discrete signal diodes.

RMS AF VOLTMETER

Design by F. Hueber



Since measuring alternating voltages and currents is not a straightforward matter, it is not to be wondered at that errors occur frequently. Non-sinusoidal measurands (quantities to be measured) in particular demand a fair knowledge and experience from the test engineer/technician. Most of the difficulties are caused by the fact that measuring instruments invariably only have a simple rectifier at their input. This is reasonably all right at very low frequencies, but even then, it does not take account of the shape of the measurand. Alternating voltages can be measured accurately only by a true-r.m.s. voltmeter, which unfortunately is a fairly expensive instrument. The instrument desribed in this article offers a viable and inexpensive alternative.

It is important to define precisely what has to be measured. The definition of the r.m.s. (root-mean-square) value of an alternating voltage is that value which in a resistive load produces the same amount of heat as a direct voltage of that value. For instance, an alternating voltage of 240 V_{rms} causes a lamp to light as brightly as a direct voltage of 240 V. The waveform of the alternating voltage is not important. A sinusoidal voltage of 240 V_{rms} has the same effect as a sawtooth-shaped, triangular or rectangular voltage of 240 V_{rms}. This means that the peak value of the alternating voltage is always higher than the r.m.s. value, except in the case of a square-wave voltage, whose r.m.s. value is equal to its peak value. Of a sinusoidal voltage, the ratio of the peak value to the r.m.s. value (called the **peak factor**) is $\sqrt{2}$ (= 1.414). Each and every shape of alternating voltage produces a different peak factor as shown in **Table 1**.

Since in most cases the r.m.s. value of a sinusoidal voltage is to be determined, in a standard multimeter a simple rectifier converts the alternating voltage into a direct voltage. The measured value is corrected by a **form factor** (1.11), and the result is shown on the meter. The form factor is the ratio of the r.m.s. value and the average value of the alternating voltage.

Since most multimeters are calibrated for sinusoidal voltages, an error will occur when a non-sinusoidal voltage is measured. These errors and some other information for a number of standard waveshapes are shown in **Table 1**. These data enable the true value of the measurand to be determined, but this neither very convenient nor, in many cases, precise.

Measuring true-r.m.s. values

True-r.m.s. meters use a special converter which makes complex arithmetical routines in the multimeter superfluous. The meaurand is applied to the converter, whose output is then a direct voltage that is representative of the r.m.s. value of the measurand. In other words, the IC assumes the entire complex conversion.

The output of the converter is calculated by sampling the input signal continuously. The value of the samples is squared and the average of the squared values over

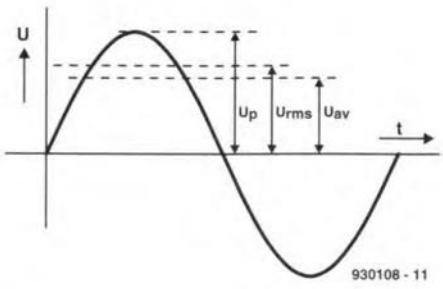


Fig. 1. A sinusoidal signal has three important values: p(eak), r.m.s. and av(erage).

Waveform U_{peak} = 1 V	Peak factor U_{peak} / U_{rms}	RMS value (V)	Reading on multimeter* (V)	Error with multimeter*(%)
sinusoidal	1.414	0.707	0.707	0
triangular	1,73	0.508	0.555	–2
white noise	3	0.333	0.266	–20.2
rectangular (d.f.† 1:1)	1	1.00	1.11	+11
rectangular (d.f.† 33:100)	2	0.25	0.25	–50
rectangular (d.f.† 1:100)	10	0.10	0.01	–99
sawtooth (d.f.† 1:1)	2	0.495	0.354	–28
sawtooth (d.f.† 1:4)	4.7	0.212	0.150	–30

†= duty factor
*= calibrated for sine waves

Table 1. Correlation between waveshapes and the ratios of their peak, r.m.s. and average values.

a certain period is computed. The root taken from this result is the true-r.m.s. value. This procedure is reliable as long as the period over which the average is calculated is long compared with the period of the measurand.

The converter used in the present meter is the AD636JH from Analog Devices. This inexpensive model in the range has a maximum error of 1%. A more accurate model is the AD636K (0.5%) but this is much more expensive.

True-RMS to d.c. conversion

Thermal r.m.s. to d.c. conversion

In theory, thermal conversion is a simple method; yet, in practice, it is difficult and expensive to implement. It involves comparing the heating value of an **unknown** a.c. signal to the heating value of a **known** calibrated d.c. reference voltage—see **Fig. 2**. When the calibrated voltage reference is adjusted to null the temperature difference between the reference resistor, R_2, and the signal resistor, R_1, the power dissipated in these two matched resistors will be equal. Therefore, by the basic definition of r.m.s., the value of the d.c. reference voltage will equal the r.m.s. value of the unknown signal voltage.

Each thermal unit contains a stable, low temperature coefficient resistor, R_1 and R_2, which is in thermal contact with a linear temperature-to-voltage converter, S_1 and S_2, an example of which would be a thermocouple. The output voltage of S_1 (S_2) varies in proportion to the mean square of V_{in}; the first order temperature/voltage ratio will vary as $K V_{in}/R_1$.

The circuit in **Fig. 2** typically has a very low error (about 1%) as wellas awide bandwidth. However, the fixed time constant of the thermal unit, R_1, S_1, R_2, S_2, limits the low-frequency effectiveness of this r.m.s. computational scheme.

In addition to the basic types discussed, there are also variable gain thermal converters available which can overcome the dynamic range limitations of fixed gain converters at the expense of increased complexity and cost.

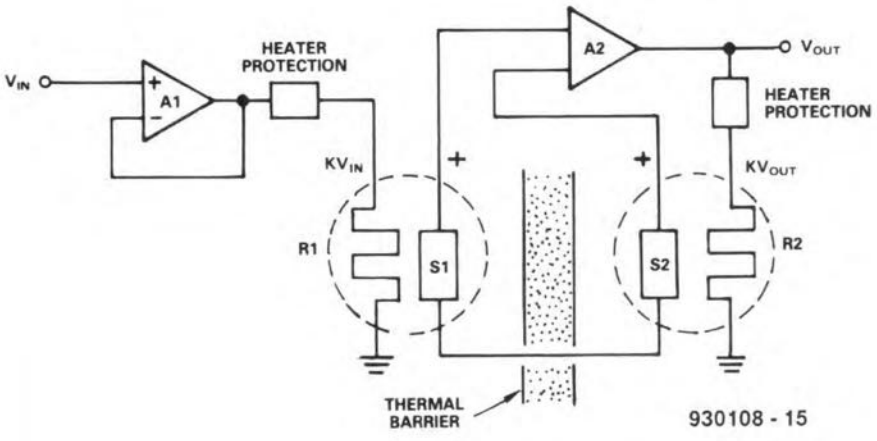


Figure 2.

Direct or explicit computation

The most obvious method of computing r.m.s. value is to perform the functions of squaring, averaging and taking the square root in a straighforward manner with multipliers and operational amplifiers. The direct or explicit method of computation (see **Fig. 3**) has a limited dynamic range because the stages following the squarer must try to deal with a signal that varies enormously in amplitude. For example, an input signal that varies over a 100:1 dynamic range (10 mV to 1 V) would have a dynamic range of 10,000:1 at the output of the squarer (squarer output = 1 mV to 10 V). These practical limitations restrict this method to inputs that have a maximum dynamic range of about 10:1. The system error may be as little as ±0.1% of full scale when a high-quality multiplier and square rooter are used. Excellent bandwidth and high-speed accuracy can also be achieved with this method.

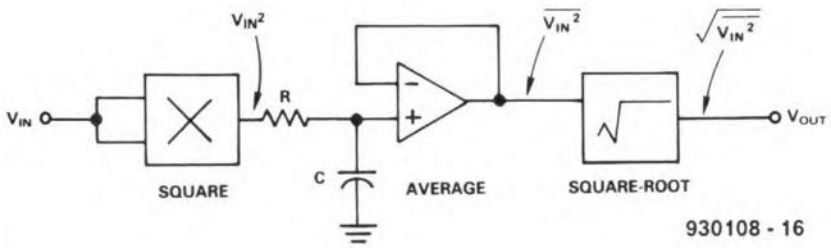


Figure 3

Indirect or implicit method

A generally better computing scheme uses feedback to perform the square root function implicitly or indirectly at the input of the circuit in **Fig. 4**. Divided by the average of the output, the **average** signal levels now vary **linearly** (instead of as the **square**) with the r.m.s. level of the input.This considerably increases the dynamic range of the implicit circuit as compared with explicit r.m.s. circuits.

Some advantages of implicit r.m.s. computation over other methods are fewer components, greater dynamic range, and generally lower cost. A disadvantage of this method is that it generally has a narrower bandwidth than either thermal or explicit computation. An implicit computing scheme may use direct multiplication and division (by multipliers), or it may use any of several log-antilog circuit techniques.

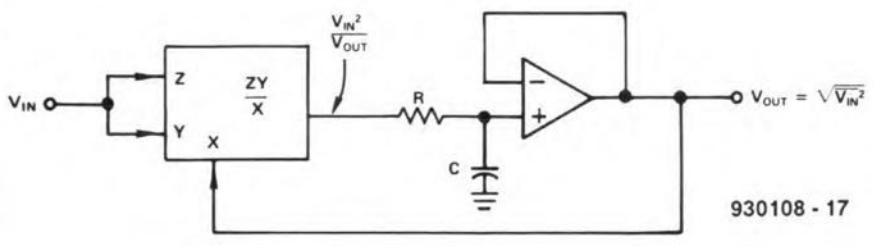


Figure 4

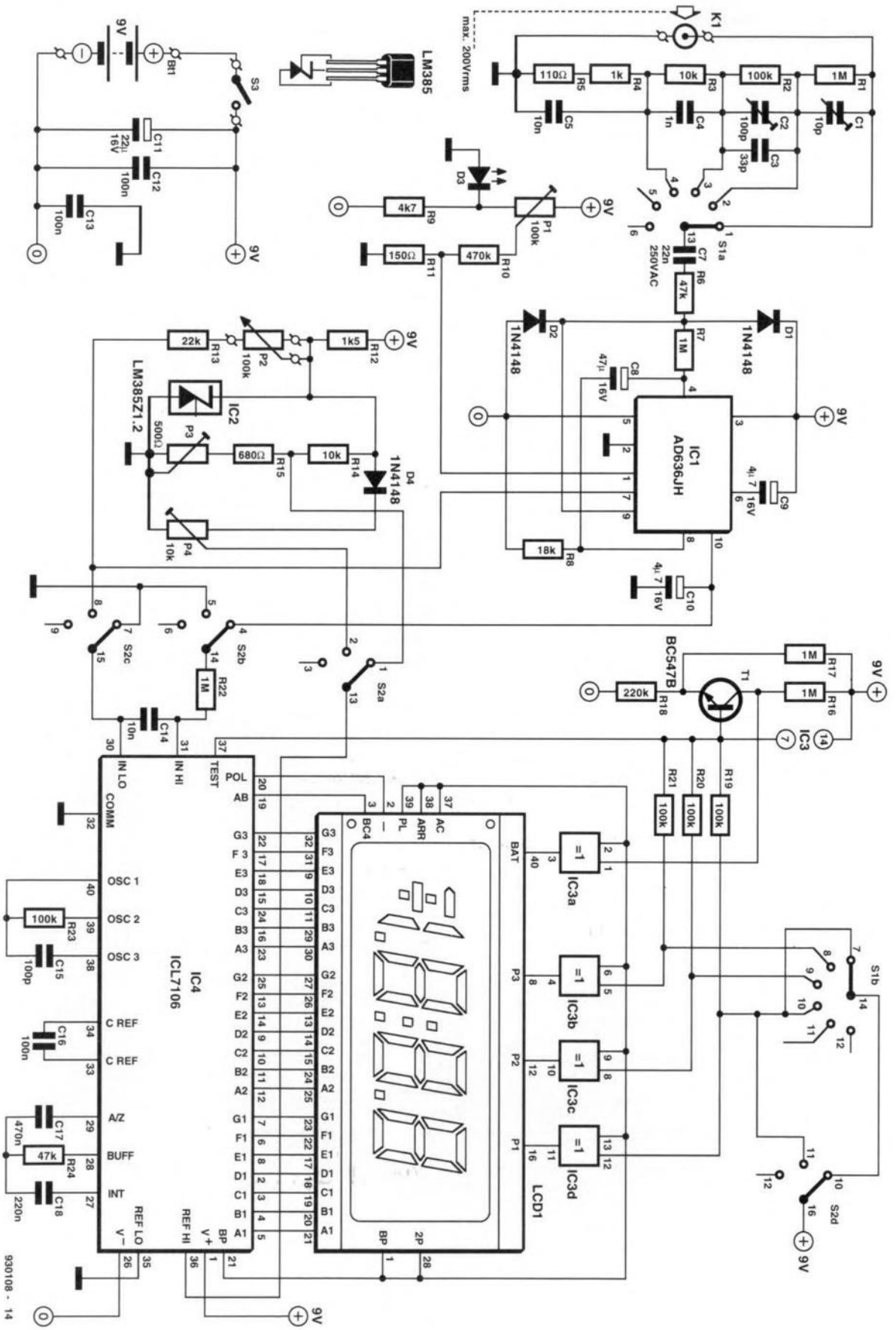


Fig. 5. Circuit diagram of the r.m.s. a.f. voltmeter.

The internal circuit of the AD636JH is shown in **Fig. 6**. The buffer operational amplifier may be used to lower the output impedance of the converter.

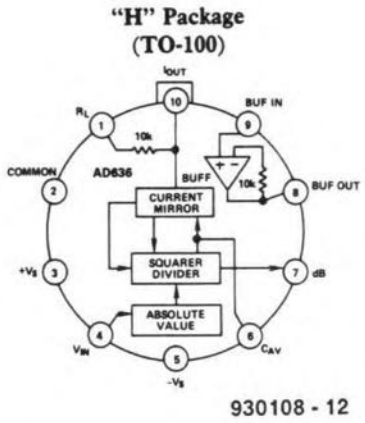


Fig. 6. Internal circuit diagram of the AD636.

The circuit

The measurand is applied to the input stages via socket K_1—see **Fig. 5**. A frequency-compensated step attenuator, R_1–R_5, C_1–C_5, makes the level measurand suitable for the meter. It has four ranges: 200 mV; 2 V; 20 V; and 200 V.

The attenuated signal is applied to IC_1 via C_7 and a protection circuit consisting of R_6, D_1, and D_2. It is imperative that the rating of C_7 is as specified: a lower rating may cause the capacitor to be destroyed with all the consequences of this.

The buffer amplifier in IC_1 is used as an impedance inverter for the input signal, because the low resistance of the actual input (pin 4) at ±7 kΩ would load the attenuator too heavily.

Since the input impedance of A-D converter IC_4 is fairly high, the output signal of IC_1 can be taken directly to IC_4.

Capacitor C_9 aids the determination of the average voltage by IC_1.

Capacitor C_{10} smooths any ripples in the output signal of the converter. It is essential for the correct operation of the meter that C_8, C_9, and C_{10} are good-quality, low-leakage, preferably tantalum or **new** electrolytic, types.

The converter operates from a quasi-symmetrical supply. The common (pin 32) of IC_4, which is held at 2.8 V by an integral zener diode, is used as ground. The offset voltage at the output of IC_1 is compensated with P_1. Thus, when, after calibration, the input of the meter is short-circuited, the display will read 0.00 V. To prevent insufficient compensation when the battery is flat or nearly so, it is important that a stable voltage is used for the compensation. This is achieved by the use of a common red LED as a voltage source. If the battery voltage drops, the current through D_3 also drops, but the potential across it will not vary much. In any case, the current through the diode is so tiny, that it will hardly light.

Also required for correct operation is a stable reference voltage and this is provided by IC_2, a highly stable and temperature-compensated zener circuit. The reference voltage is 1.23 V which is brought down to 100 mV by R_{14}, R_{15}, and P_3. This voltage is applied to pin 36 of IC_4.

dB measurements

Often, for instance, for measurements on a.f. circuits (amplifiers, filters) there is a need for a logarithmic meter calibrated in dB rather than a linear meter. In antiquated test instruments that option was fairly simply implemented by adding a logarithmic scale to the display meter. In modern, electronic units this is not always so simple, Fortunately, IC_1 has a logarithmic output, pin 7. The voltage, $-\log U_{in}$, is derived from a transistor in the multiplier. This facility makes the conversion from a linear scale to a logarithmic one a simple matter. During logarithmic measurements, the display can be nulled as required with P_2. When the input level changes, the display instantly shows the measured value in dB with respect to the set level.

The circuit is switched from linear to logarithmic measurement with S_2. Since the logarithmic voltage is negative, the **b** and **c** sections of the switch are used to invert the polarity of the measurand with respect to IC_4. The **a** section provides a matched reference voltage at pin 36 of the A-D converter. The **d** section ensures that the decimal point of the display is in the correct position.

Since the logarithmic output voltage of IC_1 is temperature-dependent, the reference voltage must be compensated accordingly, which is effected with D_4. The reference voltage at P_5 is, therefore, also dependent on the ambient temperature.

The dB measurements are possible in each range of the meter between +10 dB and –40 dB. For instance, in the 2 V range, the measurand varies between 6.32 V (+10 dB) and 0.02 V (–40 dB). Note that the sign in this range changes.

Frequency range

The calculation of the r.m.s. values of the measurand is carried out with the aid of an arithmetical circuit which makes use of logarithmic signals. As in all logarithmic circuits, the bandwidth is proportional to the signal level. The upper curve in **Fig. 7** (1 V_{rms} input) shows the near-ideal behaviour of the r.m.s. converter. The dashed lines show the upper frequency limits for 1%, 10% and ±3 dB of reading additional error. For example, note that a 1 V_{rms} signal will produce less than 1% of reading additional error up to 220 kHz. A 10 mV_{rms} signal can be measured with 1% of reading additional error (100 µV) up to 14 kHz. This means that the level of high-frequency measurands should be as high as possible. At the lower limit, linearity is guaranteed to about 30 Hz; if a small error is acceptable, even down to 10 Hz. At very low frequencies, the bootstrap circuit keeps the measuring error down to about 0.2% or ±0.2 dB.

Construction

The display is a standard application of the ICL7106. The 'low battery' indicator, provided by T_1, becomes active when the volt-

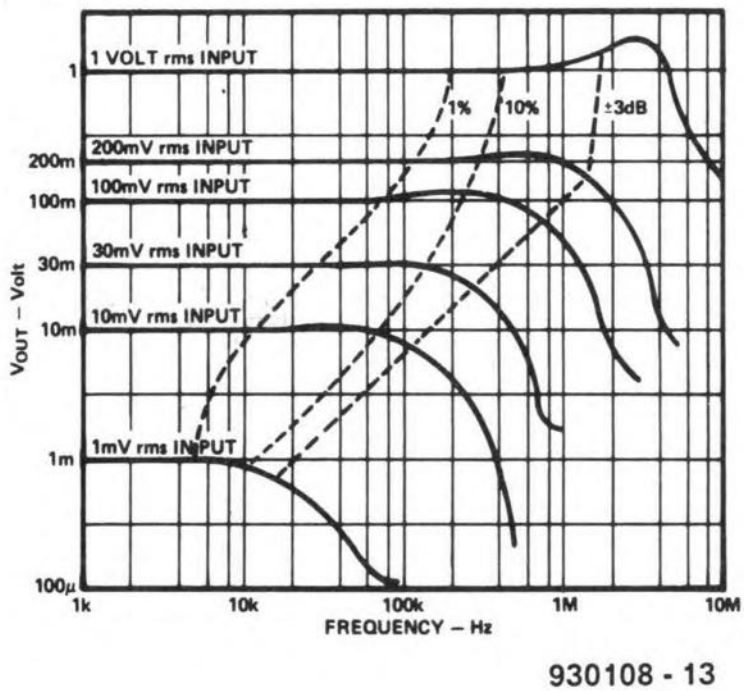


Fig. 7. The bandwidth of the converter is proportional to the level of the input signal.

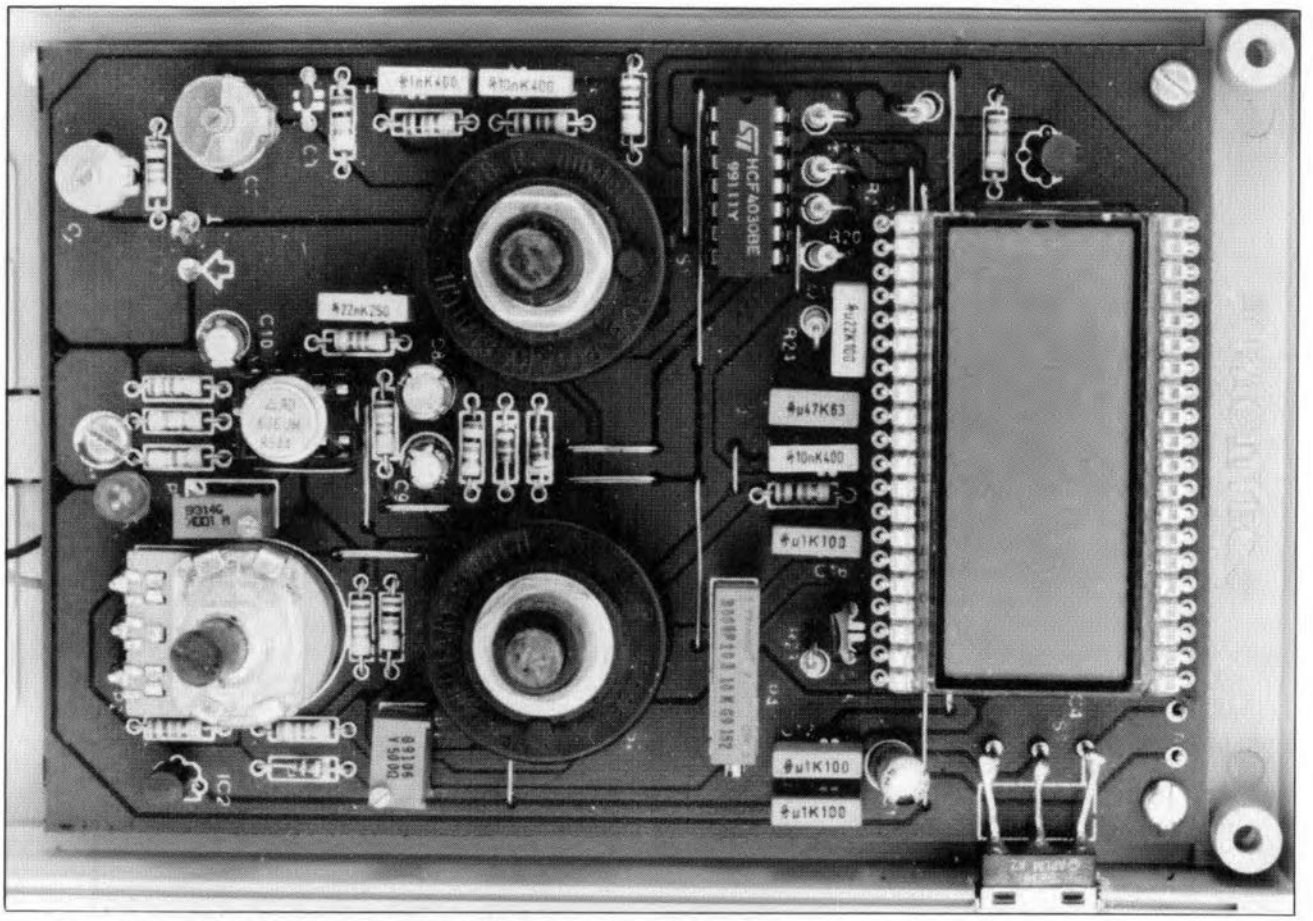


Fig. 8. Inside view of the completed r.m.s. a.f. voltmeter.

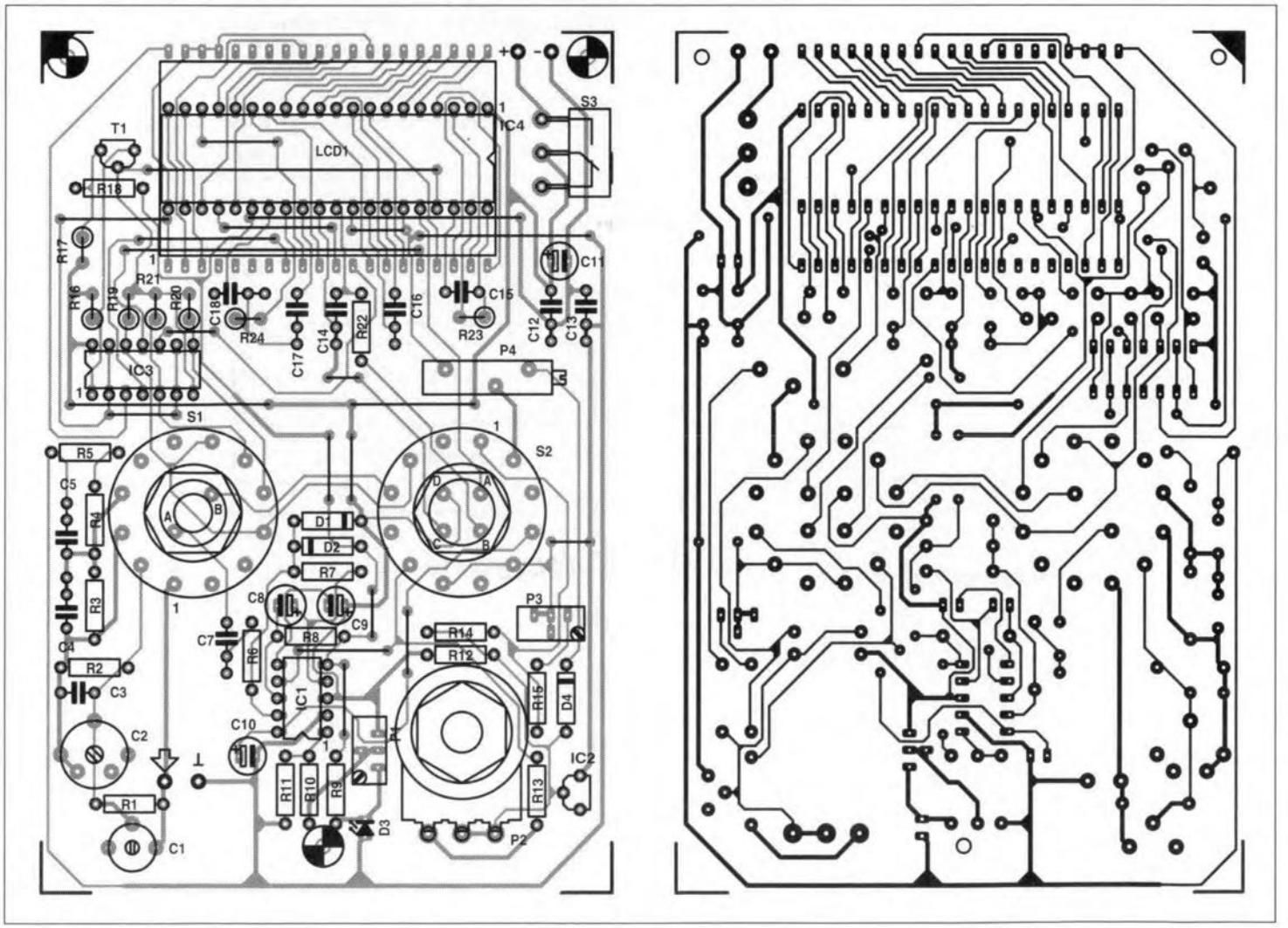


Fig. 8. Printed-circuit board for the r.m.s. a.f. voltmeter.

age drops to 6.5–7 V. Since the entire circuit draws only about 3 mA, a 9 V battery will last quite a time.

The meter is best built on the single-sided printed-circuit board shown in **Fig. 8**. Apart from the BNC input socket and the battery, all components are housed on the board.

Start construction by laying the many wire bridges. The LCD is located above IC_4, and it should therefore be fitted in a good-quality socket. In case of trouble, IC_4 will then remain accessible.

Switch S_3 is a right-angle slide type so that its knob is located at the side of the meter.

Mount rotary switches S_1 and S_2 directly on to the board: these controls must be supported by the lid of the housing to prevent undue mechanical stress on the board. This means that the holes through which the spindles protrude must be a tight fit. Make sure that the rings that determine the number of positions are in the correct position, otherwise the switch may be set to an undefined position.

It is important that the specified resistors and capacitors are used for the voltage divider. Different types may cause trouble when high voltages are applied to the attenuator.

Also important is that the connection between the BNC socket and the board is made from medium-duty cable. Should this cable be too thin, flash-over may occur when the input voltage rises to 200 V_{rms}.

Testing & calibration

Set S_2 to position LIN(ear) and S_1 to the 2 V range. Short-circuit the input. Adjust P_1 till the display reads '000'.

Apply a sinusoidal signal of about 80 Hz at a level of 1.8 V_{rms} both to the input of the meter and to that of a (good-quality) multimeter. The two instrument should give the same reading. If not, adjust P_3 until the two readings are identical.

Next, increase the signal frequency to 20 kHz and adjust C_1 until the two readings are the same again.

Then, set S_1 to the 20 V range and carry out the same tests as above. The reading in this case should be $^1/_{10}$ of the input, that is, 180 mV_{rms}. If the meter readings are different at 20 kHz, adjust C_2 till they are the same again. Since the settings of C_1 and C_2 affect one another, it is necessary for the foregoing tests to be repeated a couple of times.

Set S_2 to position dB and S_1 to position 2 V. Apply an alternating signal at a level of 2 V to K_1 and adjust P_2 until the display reads '000'. Then, set S_1 to position 20 V and adjust P_4 until the display reads –20 dB. This completes the calibration.

Parts list

Resistors:
R_1 = 1 MΩ, 1%
R_2 = 100 kΩ, 1%
R_3 = 10 kΩ, 1%
R_4 = 1 kΩ, 1%
R_5 = 110 Ω, 1%
R_6, R_{24} = 47 kΩ
R_7, R_{16}, R_{17}, R_{22} = 1 MΩ
R_8 = 18 kΩ
R_9 = 4.7 kΩ
R_{10} = 470 kΩ
R_{11} = 150 Ω
R_{12} = 1.5 kΩ
R_{13} = 22 kΩ
R_{14} = 10 kΩ
R_{15} = 680 Ω
R_{18} = 220 kΩ
R_{19}, R_{20}, R_{21}, R_{23} = 100 kΩ
P_1 = 100 kΩ preset, upright type
P_2 = 100 kΩ preset
P_3 = 50 Ω preset, upright type
P_4 = 10 kΩ preset, horizontal type

Capacitors:
C_1 = 10 pF trimmer
C_2 = 100 pF trimmer
C_3 = 33 pF
C_4 = 1 nF
C_5, C_{14} = 10 nF
C_7 = 22 nF, 250 V a.c.
C_8 = 47 µF, 16 V, radial
C_9, C_{10} = 4.7 µF, 16 V, radial
C_{11} = 22 µF, 16 V, radial
C_{12}, C_{13}, C_{16} = 100 nF
C_{15} = 100 pF
C_{17} = 470 nF
C_{18} = 220 nF

Semiconductors:
D_1, D_2, D_4 = 1N4148
D_3 = 5 mm LED, red
T_1 = BC547B

Integrated circuits:
IC_1 = AD636JH
IC_2 = LM385Z1.2
IC_3 = 4030
IC_4 = 7106

Miscellaneous:
K_1 = BNC socket for PCB mounting
S_1 = 2-pole, 6-position rotary switch
S_2 = 4-pole, 2-position rotary switch
S_3 = shift switch, right-angle, for PCB mounting
LCD_1 = $3^1/_2$ digit LCD Type LTD221F12
Bt_1 = 9 V battery with clip
Enclosure Pac-Tec Type HPL9VB (available from OK Industries, Unit 1 Deacon Trading Estate, Eastleigh SO5 5RR. Telephone (0703) 619 841.
PCB No. 930108, see p. 110
Front panel foil No. 930108F (p. 110)

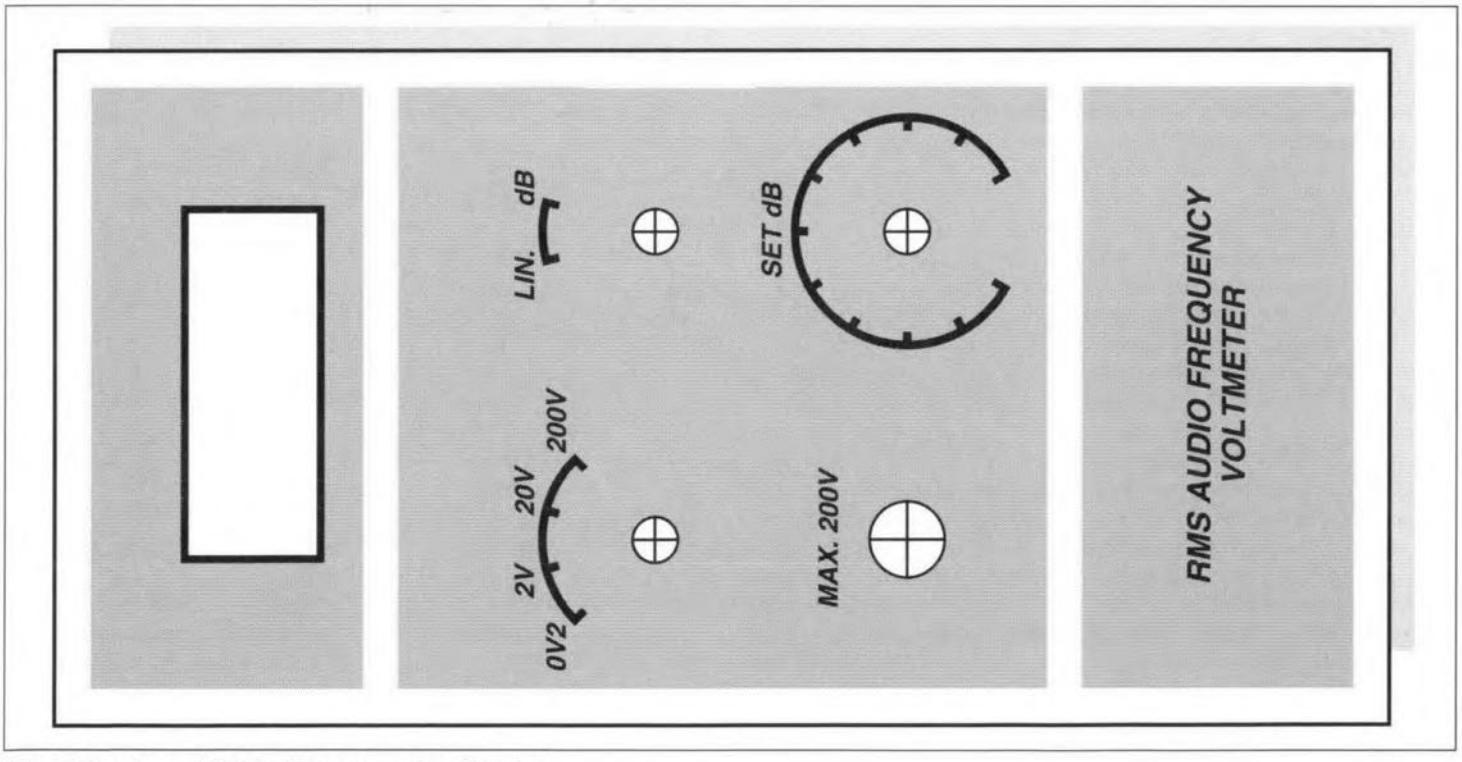


Fig. 9. Front panel foil for the r.m.s. a.f. voltmeter.

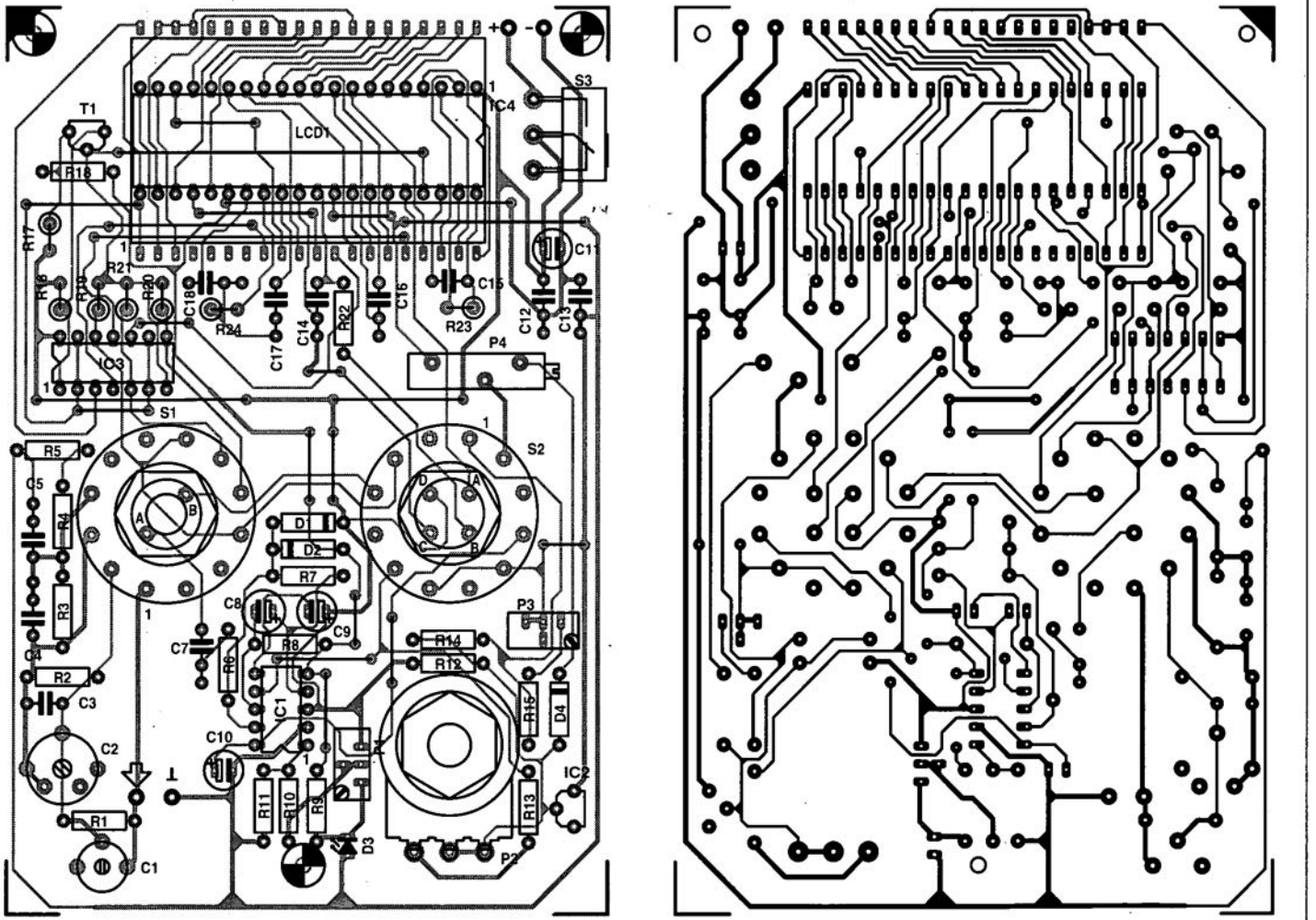


Fig. 8. Printed-circuit board for the r.m.s. a.f. voltmeter.

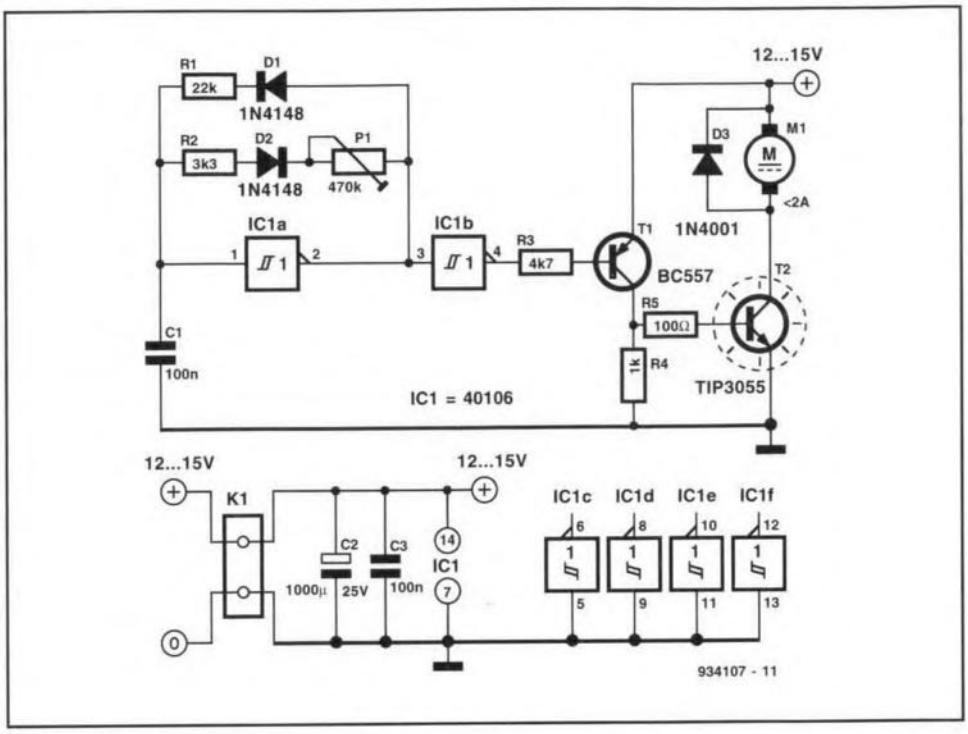
PWM MOTOR CONTROL

Pulse width modulation (PWM) is ideal for controlling small electric PCB drills that draw currents of up to 2 A. Larger currents are possible if T_2 gets addtional cooling and the value of C_2 is increased. The design also makes use of the fact that the drill works with a small d.c. motor whose rotary speed is a fucntion of the voltage across it.

The design is based on a Type 40106 astable multivibrator, IC_{1a}, whose output is low for a period determined by R_1 and high for a period set by R_2 and P_1.

When C_1 is discharged, the level at the input of IC_{1a} is below the lower threshold, so that the output of this stage (pin 2) is high. The capacitor is then charged rapidly via D_1 and R_1, and reaches the upper threshold in about 1.5 ms. The output of IC_{1a} then goes low, whereupon C_1 discharges via D_2, R_2 and P_1. In the prototype, the discharge time could be set between 0.2 ms and 25 ms. This means that the duty factor of the output signal may be varied between 5% and 90%.

The signal is inverted again and then applied to the base of T_1. Transistors T_1 and T_2 are switched on, and the motor is energized, during the negative period of the output pulse of IC_{1b} (pin 4). When the resistance of P_1 is at a minimum, the rotary speed of the drill motor is at a maximum.



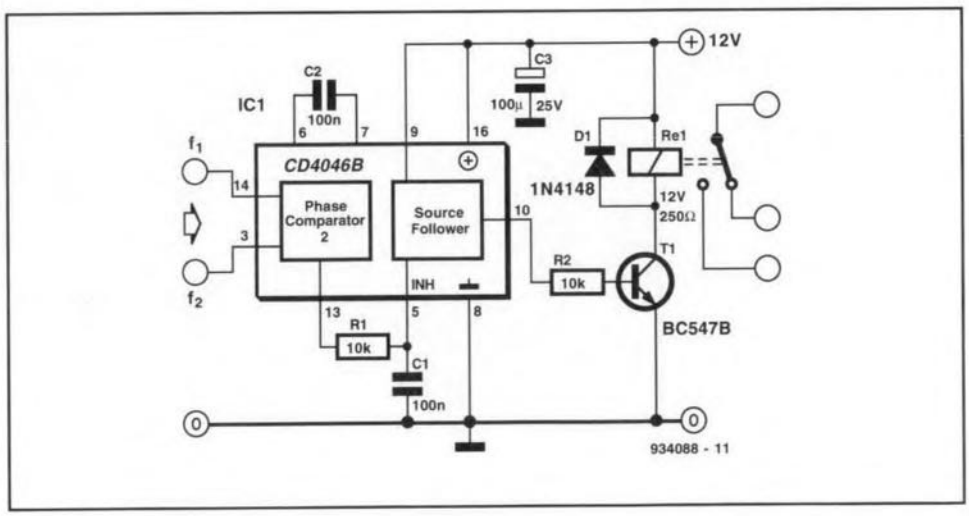
[Amrit bir Tiwana - 934107]

FREQUENCY-OPERATED SWITCH

Voltage-operated switches are fairly commonplace, but frequency-operated ones are still rare. The one described here is based on a 4046, a PLL (phase-locked loop) that, internally, is largely digital.

The two frequencies that are to be compared are applied to pins 3 and 14 of IC_1. They must be rectangular with an amplitude equal to the supply voltage of 3–5 V. Their duty factor is not important, since the IC reacts only to leading transitions (edges). If f_1 is lower than f_2, the output goes low. If $f_1 = f_2$, a rectangular voltage, whose duty factor is stable and determined by the phase difference of the two signals, is present at pin 13. This voltage is converted into a direct voltage by R_1 and C_1, which is then applied to switching transistor T_1 via the source follower. If the voltage level is high enough, T_1 will switch on and energize the relay.

In theory, the error rate of the switch is 0, but in practice 0.1% must be allowed. The time constant R_1-C_1 must be about 10 times as long as the period of the input signal. Higher ratios delay the operation unnecessarily.



When the frequencies are almost identical, it may, in the worst case, take one period of the difference frequency before the circuit is enabled.

The circuit is suitable for operation from 3–15 V supplies, but make sure that the supply and relay voltages are the same. Transistor T_1 can switch up to 100 mA. The current drawn is about 0.5 mA plus the relay current.

[I.M. Nagarajan - 934088]

WINDSCREEN WIPER CONTROL

The circuit and the associated software form a quasi-intelligent windscreen wiper interval for cars. Although intended for the 80C32 single-board computer described in **Ref. 1**, the hardware and software should be usable with any 8051 or 8032 based microcontroller system.

The hardware consists basically of a press-key, S_1, and three transistor drivers — two to drive the LEDs, and one to drive the windscreen wiper relay fitted in the car. D_2 is the wiper control on/off indicator, and D_3 the wiper motor on /off indicator.

After the control has been switched on, the LED and relay control bits, P1.0 and P1.1, are cleared, and the processor enters a wait loop after a 130 ms delay. This delay serves to debounce the press-key, which is connected to port line P1.1. As soon as the key is pressed, the on/off bit, P1.0, is set, and D_2 lights. If the key is pressed for less than 1 s, the program defaults to a wiper interval of 6.5 s (32H×130 ms). If the key is pressed for longer than about 1 s, the wiper interval takes the 'key pressed' time as the new interval time.

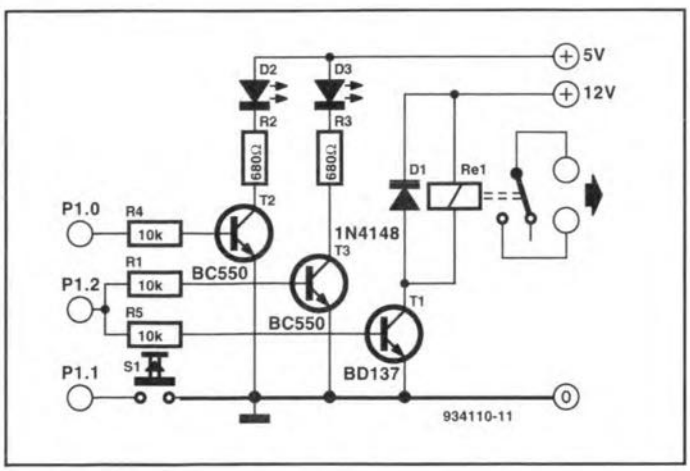
Once a key action has been detected (KEY0 loop), the accumulator value is increased from 0 in 0.13 s steps until the key is released, whereupon the counter value is written to register R7. Next, the accumulator value is compared (by subtraction) with a preprogrammed value of about 1 s (8×0.13 s). If it is smaller, the carry flag is set, and the accumulator is loaded with the value contained in R6. This results in a (default) wiper interval of about 6.5 seconds.

When the key is pressed for longer than 1 s, R6 is loaded with the stored value via R7 and the accumulator (NEW TIME). The new interval then corresponds roughly to the time the key was held pressed. When the key is pressed again, the program reverts to start. If the key action is short (<1 s), one last wiper action takes place in the previously programmed interval time. If the key action is long (>1 s), this is taken to mean a new interval time. In this way, the wiper interval may be adapted quickly to the amount of rain on the windscreen.

(J. Borm – 934110)

Reference:

1. Radio data system (RDS) decoder. *Elektor Electronics* February 1991.




```
; Wiper interval
; press-key connected to P1.1
; on/off LED        to P1.0
; relay             to P1.2 (buffered)

; definitions of SFR's
A          EQU    0E0H
R0         EQU    000H
R1         EQU    001H
R2         EQU    002H
R7         EQU    007H
R6         EQU    006H
P1         EQU    090H

; definition of port pins
LED        EQU    090H
KEY        EQU    091H
RELAY      EQU    092H
           ORG    00H

; Store default interval in R6 (approx. 10 seconds)
           MOV    R6, #32H

; Initialize accumulator and hardware
START      MOV    A, #0
           CLR    LED
           CLR    RELAY

; software debounce of switch approx. 130ms
           MOV    R0, #0H
TIME0      MOV    R1, #0H
TIME1      DJNZ   R1, TIME1
           DJNZ   R0, TIME0

; wait until key pressed i.e. KEY=0
KEY0       JB     KEY, KEY0

; key pressed, power LED on
           SETB   LED

; start counting until key released (measurement interval)
KEY1       INC    A
; time loop 130ms
           MOV    R0, #0H
TIME2      MOV    R1, #0H
TIME3      DJNZ   R1, TIME3
           DJNZ   R0, TIME2
; key released?
           JNB    KEY, KEY1

; store value (A x 130ms) in R7
           MOV    R7, A
           CLR    C

; compare value with minimum interval time (approx. 1s)
           SUBB   A, #08H      ; 8 x 130ms
           JNC    NEW_TIME     ; >1s, new value, else default
WIPE       MOV    A, R6
PULSE      MOV    R0, #0H
TIME4      MOV    R1, #0H
; keep checking if key pressed (i.e. wiper off)
           JNB    KEY, START1
TIME5      DJNZ   R1, TIME5
           JNB    KEY, START1
           DJNZ   R0, TIME4
           JNB    KEY, START1
           DEC    A
           JNZ    PULSE
; switch on relay (fixed interval)
           SETB   RELAY
           MOV    R0, #8
TIME6      MOV    R1, #0H
TIME7      MOV    R2, #0H
           JNB    KEY, START1
TIME8      DJNZ   R2, TIME8
           JNB    KEY, START1
           DJNZ   R1, TIME7
           JNB    KEY, START1
           DJNZ   R0, TIME6
; switch off relay
           CLR    RELAY

           JB     KEY, WIPE
START1     JNB    KEY, START1
           AJMP   START

; update interval time
NEW_TIME   ADD    A,#08
           MOV    A, R7
           MOV    R6, A
           SJMP   WIPE

           END                 934110-12
```

BICYCLE LIGHT WITH AFTERGLOW

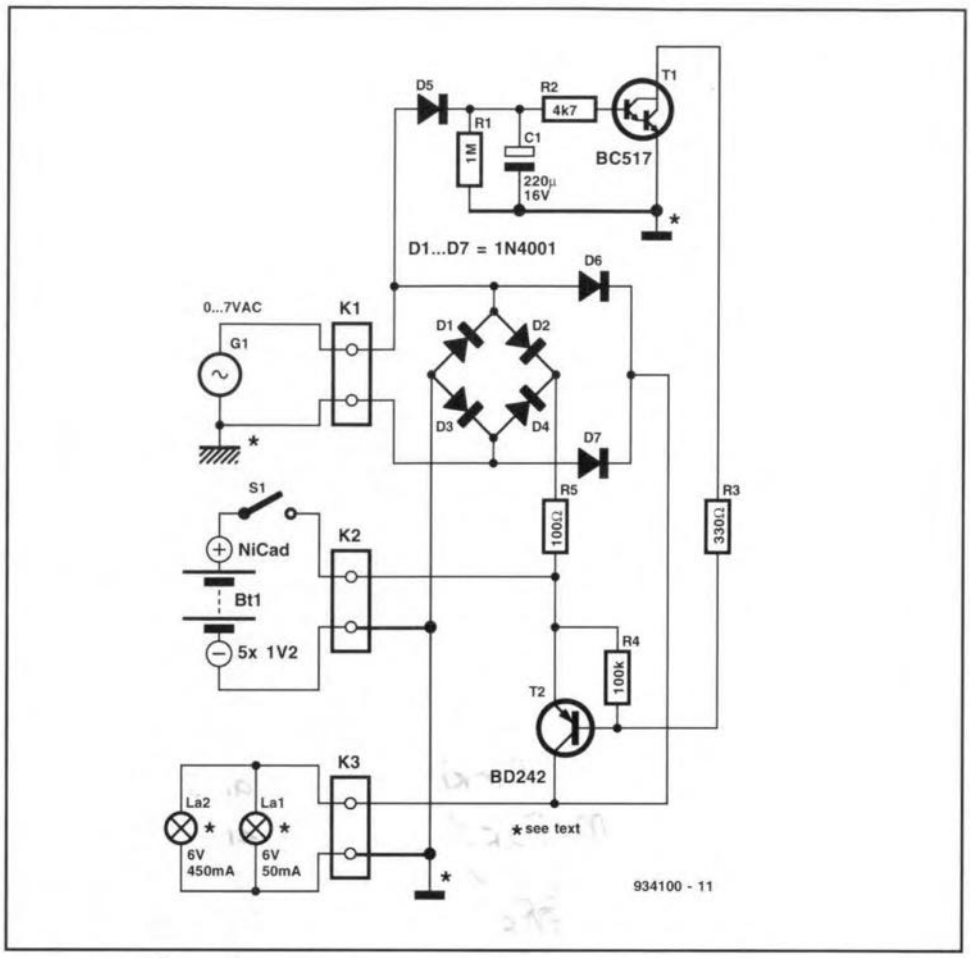
The circuit presented here ensures that bicycle lights remain on for a little while after the bicycle (and thus the dynamo) has come to a standstill. It has the disadvantage that the frame of the bike cannot be used as the common return: a separate wire has to be run for this. This is because use is made of a bridge rectifier to provide full-wave rectification of the dynamo voltage. Consequently, the alternating and direct voltages must float with respect to one another.

Actually, bridge rectifiers are used that have one half in common. Diodes D_1–D_4 constitute the bridge via which (and R_5) the NiCd battery is charged when the bicycle is moving (and the dynamo is connected). Diodes D_1, D_3, D_6, and D_7 form the bridge via which the bicycle lights are powered when the dynamo voltage is sufficiently high.

When the dynamo is driven, C_1 is charged via D_5, which causes T_1 to conduct. If T_1 is on and the dynamo output drops below a certain level, T_2 is switched on, whereupon the bicycle lights are powered by the NiCd battery.

When the bicycle is at a standstill and the dynamo is no longer driven, C_1 is no longer charged. Because of this, T_1 will gradually stop conducting and this will also switch off T_2. The bicycle lights will then go out.

Switch S_1 serves to prevent the NiCd battery slowly discharging via the circuit when the bicycle is not used. The switch should then be opened.



If the afterglow time is found too short, it may be lengthened by increasing the value of C_1.

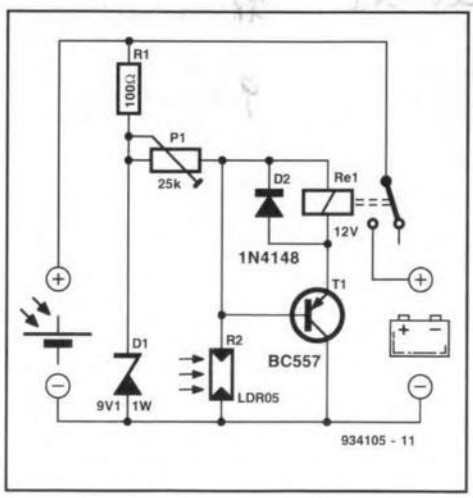
[L. Pijpers - 934100]

SOLAR PANEL SWITCH

When a battery is charged by a solar panel during the day, it may discharge via that panel after sunset. This may, of course, be prevented by a diode, but that has the drawback of a forward voltage drop of 0.7 V or, in the case of a Schottky diode, 0.4 V. In many applications, this is not acceptable.

The present circuit replaces the diode and connects the solar panel to the battery via a relay contact. It is powered by the solar panel. When the supply voltage is too low, the relay is not energized so that the battery is not connected to the solar panel.

When the panel output is sufficient to energize the relay and the LDR (R_2) receives enough light to cause T_1 to conduct, the relay is energized and the battery will be charged.



Owing to its inherent hysteresis, the relay will remain energized even if the potential across the panel drops somewhat. A connected and charged battery cannot actuate the relay when the light begins to fail, because the LDR will then switch off T_1. At what brightness that occurs may be preset with P_1.

Since the current drain is determined primarily by the relay, it is important that this is a miniature type with a high coil resistance, which can nevertheless switch up to 10 A (for instance, Siemens Type V23037-A0002-A101*).

[L. Lemmens - 934105]

* Siemens product. Available from ElectroValue, Unit 3, Central Trading Estate, Staines, Middx TW18 4UX. Telephone: (0784) 442253. Fax: (0784) 460320.

I²C EEPROM

XICOR's X2404 or Philips' PCF8582 EEPROM with integral I²C interface can be connected to the I²C interface published last year[1] via a 6-way PCB mount mini DIN socket.

The bus address of IC_1 (see **Fig. 1**) may be preset with the aid of jumpers A0, A1 and A2. The complete binary address of the PCF8582 is

1 0 1 0 A2 A1-A0 R/W>.

With the jumpers positioned as shown, the address is $A0_{HEX}$.

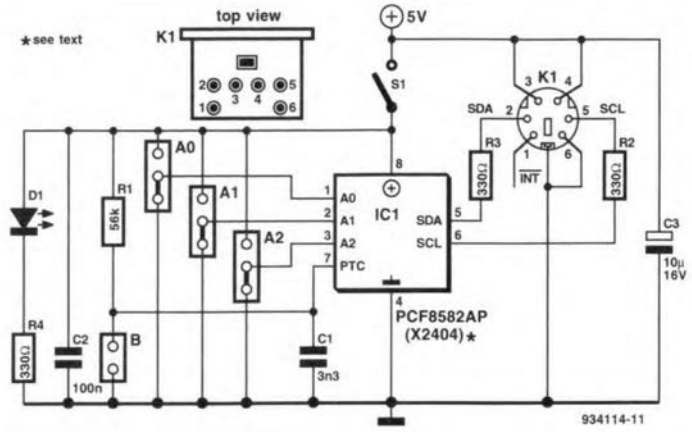
The X2404 is pin compatible with the PCF8582 but has twice its memory: two pages of 256 bytes each. Pages are selected by the software with the aid of the P bit in the I²C address:

1 0 1 0 A2 A1 P R/W>.

When the X2404 is used, jumper A0 must always be connected to earth. With the jumpers positioned as shown, the address for the first page is $A0_{HEX}$ and that for the second page, $A2_{HEX}$.

Before new data can be stored in the EEPROM, the internal oscillator needs to be actuated by connecting network R_1C_1 to the TEST input (not necessary with the X2404, whose pin 7 should be connected to earth: close jumper B). The erase/write time, T_{ew}, is not greater than 10 ms with the X2404, and about 30 ms (R_1C_1) with the PCF8582. The current drawn by IC_1 during erase/write operations may go up to 30 mA (X2404) or 2 mA (PCF8582). In the

1



2

```
unit PCF8582;
(**********)

{ Library to control the PCF8582 I2C EEPROM (256 * 8 bits).}

{ Requirements:
        MS-DOS r 3.3
        I2CDRIV2.SYS added to CONFIG.SYS
        Elektor I|C PC hardware interface
        PCF8582 (compatible) I|C EEPROM
        Special unit: I2C2.TPU

    Source..... PCF8582.PAS
    Executable..... -
    Language..... Turbo Pascal 5.5
    Version..... 1.0
    Date..... 26-03-1993
    Written by..... P. J. Ruiters.
    Copyright..... Elektor Electronics / Elektuur (c) 1993
    Order information.... ESS182x (diskette 5, inch 360 K: I2CDRIV2 & I2C2)
}

{ Compiler directives.      } {$R-,S-,I-,F-,O-,A-,V+,B-,N-,E+,D-,L-}

INTERFACE
{=========================================================================
=======}

{-------------------------------}uses
{ Used units.                 } I2C2,crt;
{-------------------------------}const
{ Erase/write cycle time of the } Tew=50;
{ EEPROM (milli seconds).     }
{-------------------------------}var
{ I|C definition} Bus:I2Cfile;
{ I|C address of PCF8582 EEPROM.} PromAddr:byte;
{-------------------------------}

procedure WriteByteProm(PromDataAddr,PromData:byte);

procedure ReadByteProm(PromDataAddr:byte; var PromData:byte);

IMPLEMENTATION
{=========================================================================
=======}

{
WriteByteProm-
                Store PromData into the EEPROM at address PromDataAddr.
}
procedure WriteByteProm(PromDataAddr,PromData:byte);
{-------------------------------}begin(* WriteByteProm *)
{ Generate start condition on} if Start(Bus)<>0
{ I|C bus.}   then
{}     begin
{} writeln('I|C error (start).');
{} halt;
{}     end;
{ Address I|C EEPROM.} if Address(PromAddr)<>0
{}   then
{}     begin
{}       writeln('I|C error (address).');
{}       halt;
{}     end;
{ Write data byte to EEPROM.} write(Bus,PromDataAddr,PromData);
{ Generate stop condition on   } close(Bus);
{-------------------------------}end; (* WriteByteProm *)

{
ReadByteProm-
                Read the contents of the EEPROM at address PromDataAddr.
                The result
                is returned via PromData.
}
procedure ReadByteProm(PromDataAddr:byte; var PromData:byte);
{-------------------------------}begin (* ReadByteProm *)
{ Generate start condition on } if Start(Bus)<>0
{ I|C bus.}   then
{}     begin
{} writeln('I|C error (start).');
{} halt;
{}     end;
{ Address I|C EEPROM.} if Address(PromAddr)<>0
{}   then
{}     begin
{}       writeln('I|C error (address).');
{}       halt;
{}     end;
{ Set EEPROM location to read.}  write(Bus,PromDataAddr);
{ Read data byte from EEPROM.  }  read(Bus,PromData);
{ Generate stop condition on}   close(Bus);
{ I|C bus.}
{-------------------------------}end; (* ReadByteProm *)

{-------------------------------}begin (* PCF8582 *)
{-------------------------------}end. (* PCF8582 *)
```

3

```
{ I2C bus.                    }
{ Wait until erase/write cycle } delay(Tew);
{ time elapsed.}
{-------------------------------}end; (* WriteByteProm *)

{
ReadByteProm-
                Read the contents of the EEPROM at address PromDataAddr.
                The result
                is returned via PromData.
}
procedure ReadByteProm(PromDataAddr:byte; var PromData:byte);
{-------------------------------}begin (* ReadByteProm *)
{ Generate start condition on } if Start(Bus)<>0
{ I|C bus.}   then
{}     begin
{} writeln('I|C error (start).');
{} halt;
{}     end;
{ Address I|C EEPROM.} if Address(PromAddr)<>0
{}   then
{}     begin
{}       writeln('I|C error (address).');
{}       halt;
{}     end;
{ Set EEPROM location to read.}  write(Bus,PromDataAddr);
{ Read data byte from EEPROM.  }  read(Bus,PromData);
{ Generate stop condition on}   close(Bus);
{ I|C bus.}
{-------------------------------}end; (* ReadByteProm *)

{-------------------------------}begin (* PCF8582 *)
{-------------------------------}end. (* PCF8582 *)
```

standby mode and during read operations, the current is appreciable lower. The overall current drain is then almost entirely that through D_1, that is, 10 mA.

The Pascal unit in **Fig. 2** contains procedures for programming and reading the EEPROM. With WriteByteProm data may be stored byte by byte. Via PromDataAddr access may be had to each address; this is also true for the ReadByteProm read procedure. To use the unit, 'PCF8582' or 'X2404' must be added to the USES command in the source code of the application program in use.

[J. Ruiters - 934114]

[1] *Elektor Electronics*, February 1992, page 36.

NOTE: After this article had been written, it was learned that the PCF8582AP has been superseded by the PCF8582E-2P.

SMALL POWER CONVERTER

The converter enables an existing positive supply voltage to be raised, to be lowered, or to be changed into a negative potential.

The new voltage is electrically isolated from the source by a DIY transformer wound on a G2-3FT12 toroid. The primary winding consists of 30 turns. The number of secondary turns is calculated from

$$n = 30U_o / U_i,$$

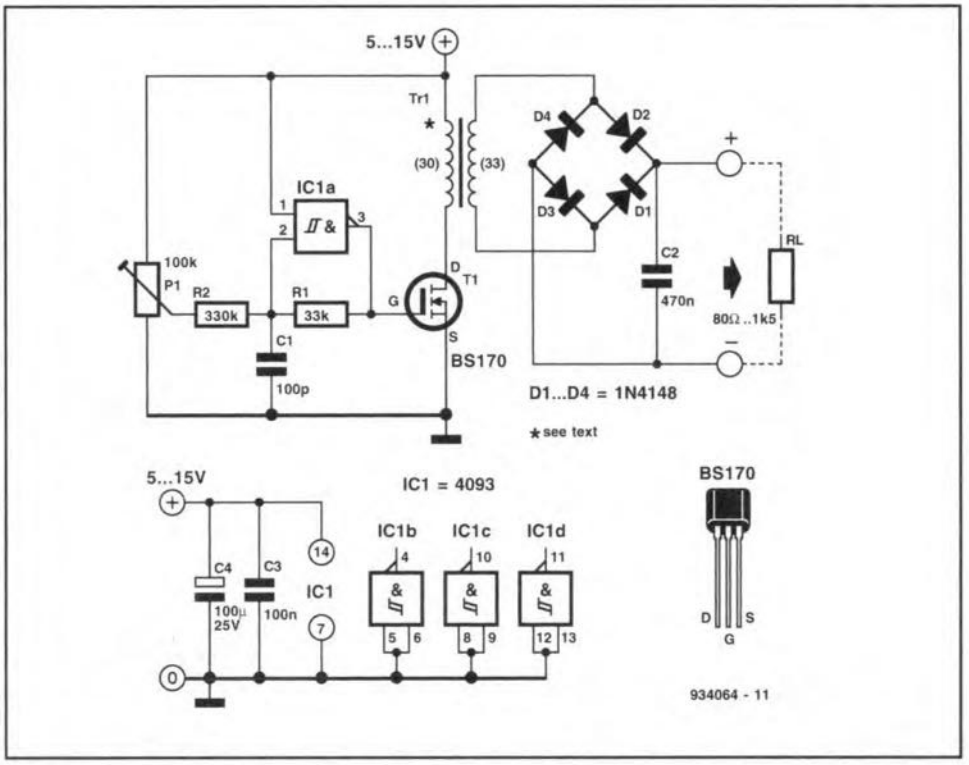
where U_o is the wanted voltage and U_i is the input voltage. Increase the number of turns so found by 10–20 to compensate for losses. If the output voltage is somewhat too large, it can always be reduced with P_1. Both windings must be wound with 0.3 mm dia. enamelled copper wire. Make sure that the turns of both are evenly distributed along the core.

The transformer is driven by a CMOS Schmitt trigger NAND gate that has been converted to a rectangular-wave generator by R_1 and C_1. MOSFET T_1 serves as output stage. Additional charging current for C_1 is provided via R_2 and P_1, which control the duty factor of the rectangular signal. The frequency of this signal is about 220 kHz and its duty factor must be smaller than 0.5.

When T_1 is switched on, some energy is transferred to the secondary winding and some is stored in the magnetic field. When T_1 stops conducting, the energy in the magnetic field is transferred to the secondary winding.

The idea is to make the duty factor small enough to ensure that all energy stored in the field is transferred before T_1 switches on again. If not, there is the risk that the residual magnetic field becomes stronger and stronger, which causes the core to become saturated and this in turn lowers the efficiency. Also, owing to the reduced inductance at the primary side, the current through T_1 will rise appreciably, which means the end of the transistor.

The current through T_1 will also rise dangerously when the secondary load is too heavy. The average current through the primary should not exceed 150 mA (the peak current may be several times larger). From the turns ratio it is easily calculated what the maximum secondary load current should be. With the ratio shown in the drawing (10% extra turns at the secondary side), the secondary load should be not smaller than 80 Ω.



Apart from a heavy load, no load is also to be avoided. In that case, the energy stored in the magnetic field can only move to C_2 where it is stored in the electric field. This means that the charge on C_2, and thus the voltage across it, increases to a level where it can have a serious effect on the circuit to which the converter will be connected. As a rule of thumb (just as with the maximum load current), the indicated value of 1.5 kΩ is directly proportional to the turns ratio.

The Type 1N4148 rectifier diodes are fast enough to cope with the frequency of 220 kHz (1N400x types are not). These diodes can stand a constant current of 200 mA (400 mA peak).

The efficiency of the convertor with a supply voltage of 15 V is about 65%. When the load current is small, this drops to about 50%. The efficiency also drops when the supply voltage is lower than indicated.

The maximum input voltage is 15 V, since the supply to neither IC_1 nor T_1 must exceed this value. The current drawn from a 15 V source and a load of 80 Ω is about 165 mA.

The prototype worked fine with the wiper of P_1 turned completely to **+**; it may even be possible to lower the value of R_2 slightly.

If necessary, the duty factor of the rectangular voltage may be increased somewhat with P_1. When this is being done, the current through T_1 should be watched carefully, preferably on an oscilloscope. If the current suddenly rises too fast, the core is becoming saturated and this means that P_1 must be turned back slightly. Bear in mind that when P_1 is set to a critical position, a slight change in load can drive the core into saturation, with all the consequences of this.

[T. Giesberts - 934064]

SOLID-STATE VOICE RECORDER

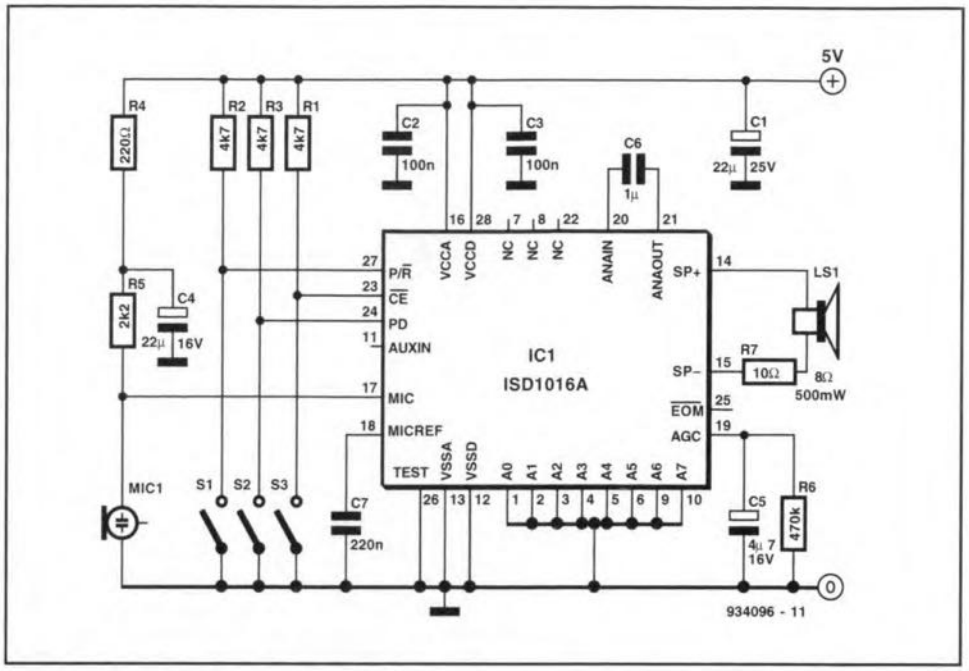
Integrated circuits ISD1012, ISD1016, and ISD1020 from chip maker ISD enable sounds to be recorded and played back. The final two digits in the type coding show the length of a sound message in seconds. The difference in recording and play back time is caused by the sampling frequency, which is highest (10.6 kHz) for the shortest time.

The circuits have a non-volatile memory that can store the recorded sound for not less than ten years without any supply voltage. The circuits also contain a microphone amplifier and an output amplifier.

The drawing shows the simplest circuit for using one of these ICs: an electret microphone, a loudspeaker, three operating switches and a power supply.

Switch S_1 is the recording/playback switch: for recording, it must be closed.

Switch S_2, when open, sets the IC to the power-down mode. The larger part of the circuit is then switched off, which reduces the current drain. Switching to power down also serves as a reset when, for instance, during recording an overflow occurs (message too long). The IC indicates this by making the end-of-message (EOM) output low during the recording.



Recording or playback is started by closing S_3. This switch must remain closed during recording and should preferably be a push-button type.

The circuit is kept simple, although it is possible to connect several ICs in cascade if longer messages, or a number of short ones, are to be recorded.

The bandwidth of the circuits is similar to that of telephones: ISD1012 – 4.5 kHz; ISD1016 – 3.4 kHz; ISD1020 – 2.7 kHz. The current drain during playback is about 25 mA.

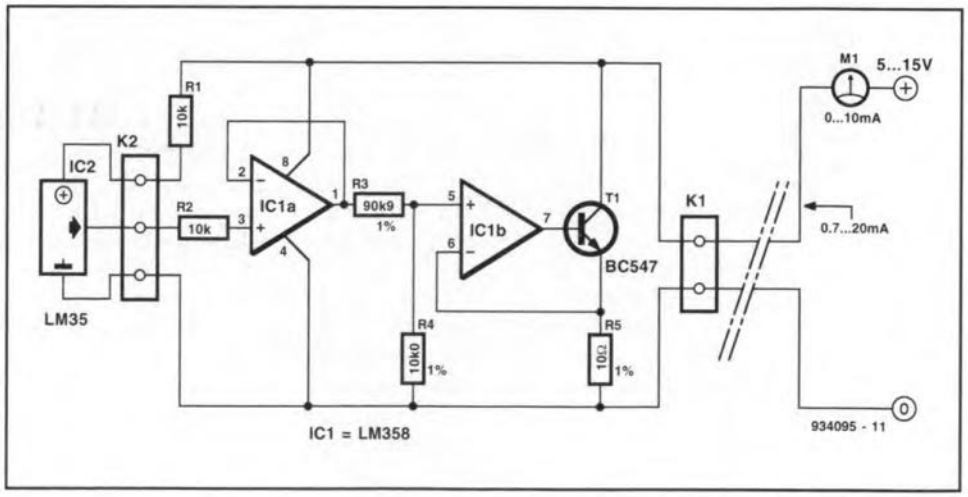
[L. Lemmens - 934096]

ACTIVE TWO-WIRE TEMPERATURE SENSOR

When a physical quantity (measurand) has to be measured at a distance, it is normally necessary to provide the sensor proper with an amplifier. This amplifier needs a power supply, which means that a third wire has to be taken to the sensor. In the present circuit, the measurand and the power supply use the same two lines. To that end, the measurand, buffered by IC_{1a}, is converted into an additional supply current drawn from current source IC_{1b}. In other words, the magnitude of the input voltage may be gauged from the level of the supply current (which, of course, also consists of the current drawn by the opamp and, possibly, the sensor).

When the specified sensor and opamp are used, the current is about 0.7 mA (0.65 mA with a supply voltage of 5 V; 0.7 mA at 10 V; and 0.77 mA at 15 V). With a ful-scale deflection (FSD) of 10 mA, this is a deviation of about 7%, which is, however, easily compensated.

The circuit design is such that when the temperature at the sensor varies from 0 °C to 100 °C, the supply current changes from 0.7 mA to 10.7 mA. Thus, a moving coil ammeter in the supply line enables the temperature to be read quite simply; the supply current to the opamp (0.7 mA) is nullified with the adjustment screw on the meter.



Note that the voltage drop across long lines must be compensated by a higher supply voltage to prevent that IC_1 and IC_2 are under-powered (they must get at least 5 V).

[L. Pijpers - 934095]

STEREO PWM OUTPUT AMPLIFIER

The most remarkable feature of this small stereo amplifier is the use of a stepper motor bridge driver IC as a stereo power output stage. The circuit diagram shows a three-stage pulse-width modulation (PWM) converter/amplifier for each channel. The left (L) and right (R) audio input signals are first converted into triangular waveforms by opamps IC_1 and IC_2, which are wired as integrators, with feedback from the power output stage via resistors R_7 and R_{11}. Next, the triangular waveforms are converted into rectangular signals with a variable pulsewidth by opamps IC_3 and IC_4, which drive the digital inputs of the bridge power amplifier, IC5.

The L6203 from SGS-Thomson is actually a full bridge driver for motor control applications. Its DMOS output transistors have an $R_{D\text{-}S(on)}$ resistance of only 0.3 Ω, which results in low dissipation and, consequently, high efficiency. Each channel (half bridge) of the device is controlled by a separate logic input, while a common 'enable' (pin 11) is available to switch both channels on and off. In the present application, the channels are enabled by a +5.1 V level derived from the IC's voltage reference output. Although the L6203 contains a bridge circuit, the loudspeakers are connected single-ended for a stereo output arrangement.

The test results obtained with a prototype of the amplifier are not spectacular but none the less worth mentioning.

With a supply voltage of 12 V and an input frequency of 1 kHz, a maximum output power of 2 W was supplied into a load of 4 Ω. The nominal input level required for this output power was 2 V_{rms}. A damping factor of 20 was measured, while the distortion was about 1.5%.

These figures change slightly when the supply voltage is increased to 14.4 V. Maximum output power, for instance, increases to about 2.8 W with a distortion of about 1.5%. The input drive level required for this output power is 2.25 V_{rms}. With full drive, the amplifier achieves an efficiency of about 73%, with PWM clock intermodulation products down to –40 dB.

At lower input signal levels, the distortion of the amplifier remains around 0.3%, and the noise level at about –80 dB.

(SGS-Thomson application — 934076)

Parts list

Resistors:
R_1, R_2 = 47 kΩ
R_3, R_4 = 33 kΩ
R_5, R_6 = 2.2 kΩ
R_7, R_{11} = 18 kΩ
R_8, R_{12} = 22 kΩ
R_9, R_{13} = 100 kΩ
R_{10}, R_{14} = 470 Ω
R_{15}, R_{16} = 10 kΩ
R_{17}, R_{18} = 1 kΩ

Capacitors:
C_1 = 10 µF, 25 V
C_2 = 10 µF, 25 V radial
C_3 = 100 µF, 25 V radial
C_4, C_5 = 560 pF, polystyrene
C_6 = 220 µF, 25 V radial
C_7, C_8 = 22 nF
C_9 = 220 nF
C_{10}, C_{11} = 470 nF
C_{12}, C_{13} = 2200 µF, 25 V, radial

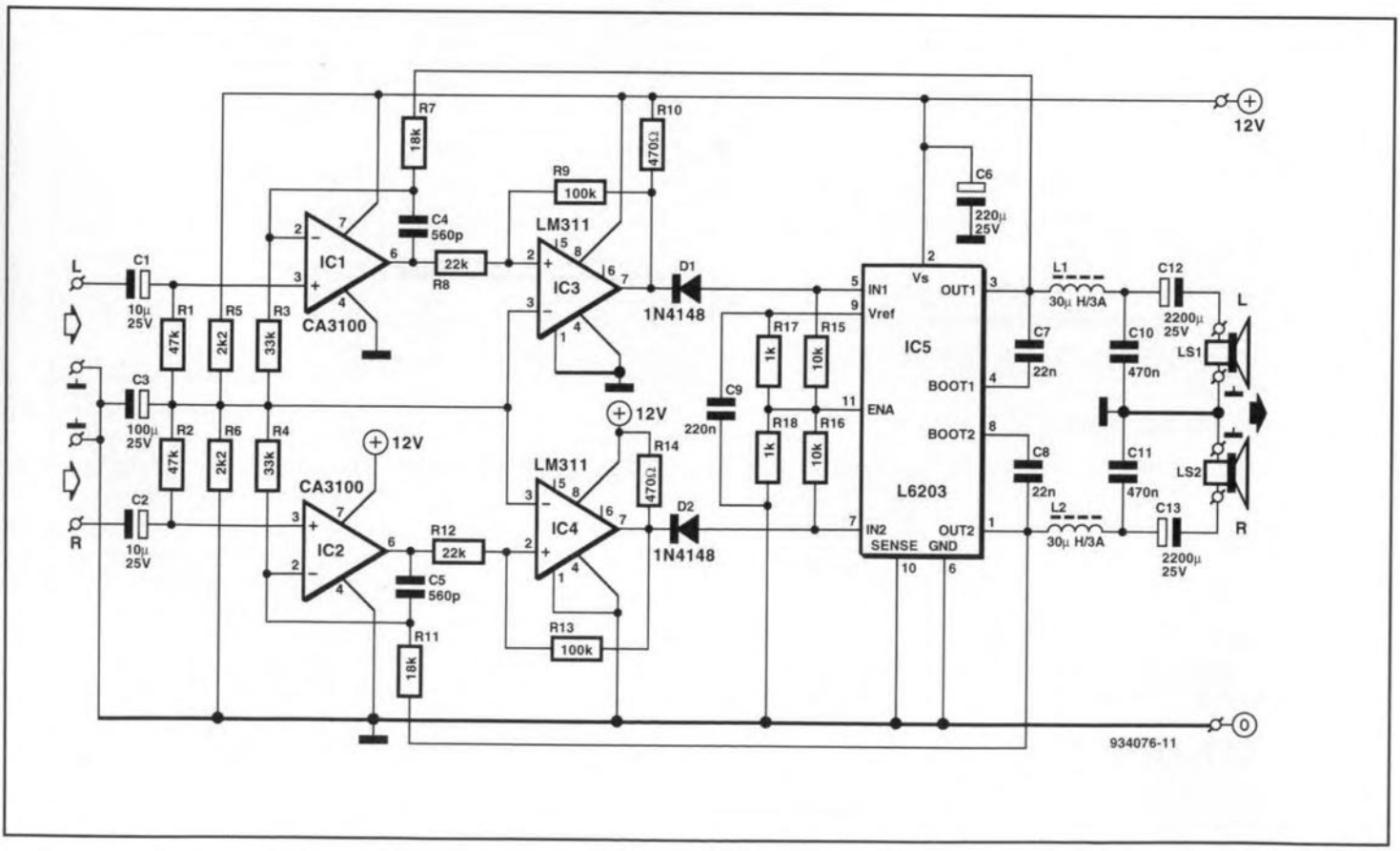
Inductors:
L_1, L_2 = 30 µH/3 A toroid choke

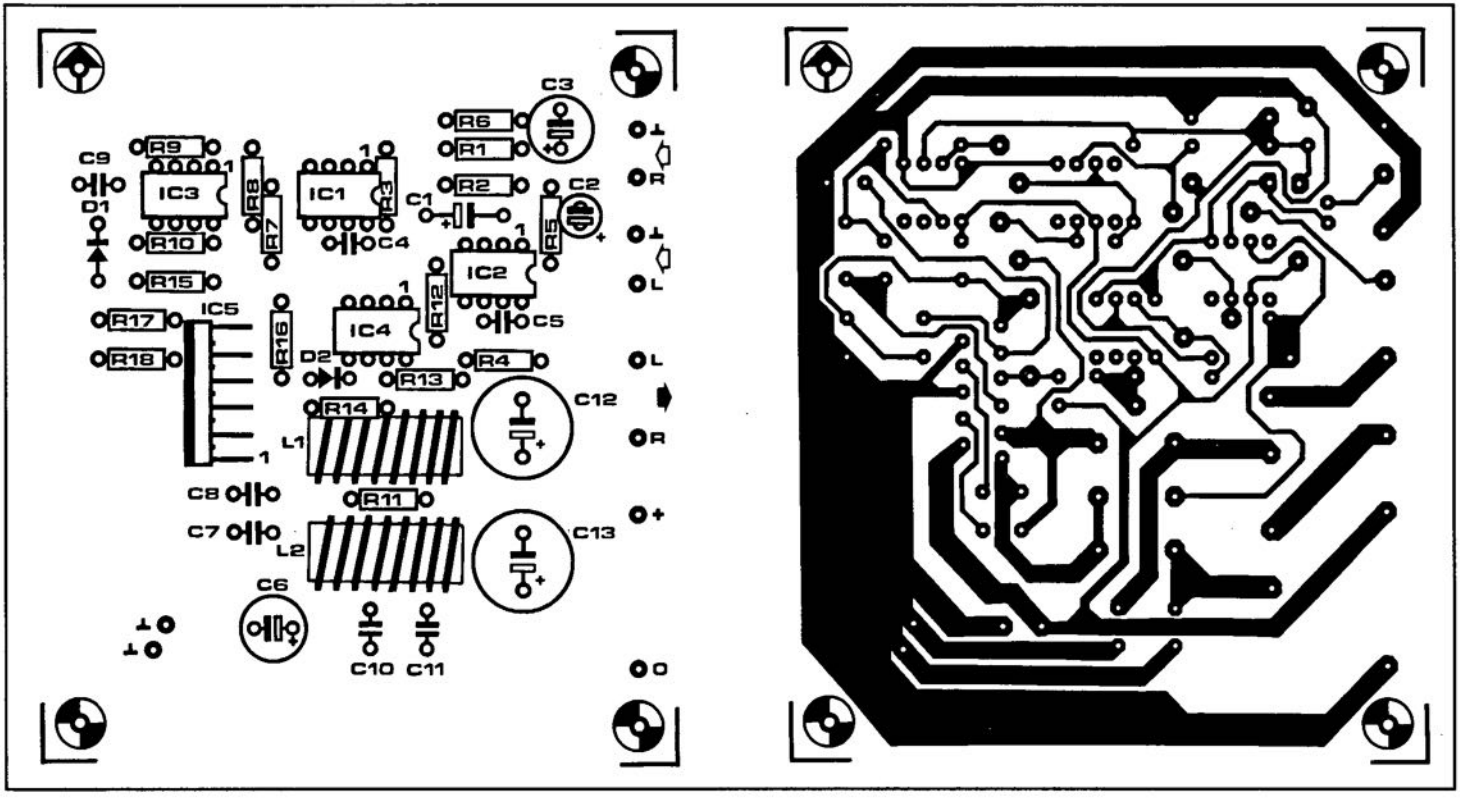
Semiconductors:
D_1, D_2 = 1N4148

Integrated circuits:
IC_1, IC_2 = CA3100*
IC_3, IC_4 = LM311N
IC_5 = L6203**

* Harris Semiconductor UK distributors: Farnell Electronic Components Ltd. (0532) 636311; Thame Components Ltd. (0844) 261188.

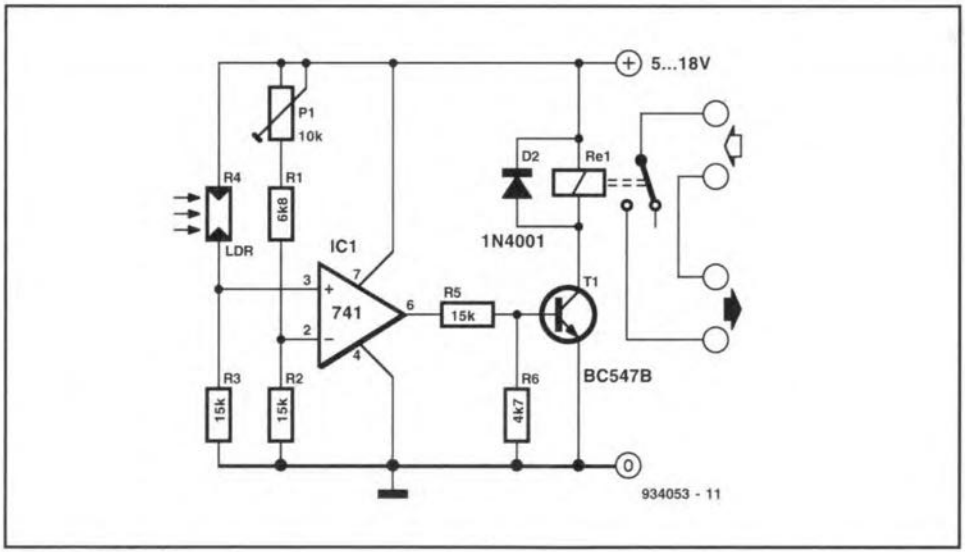
** SGS Thomson Microelectronics UK distributors (among others): Abacus Electronics Ltd. (0635) 33311; Access Electronic Comp. Ltd. (0462) 480888; Farnell Electronic Components Ltd. (0532) 636311.




C3
R6
R1
C9
R9
IC3
R8
R7
IC1
R3
C1
R2
C2
R5
D1
R10
C4
IC2
R15
C5
R12
IC5
R17
IC4
R16
R18
D2
R13
R4
R14
C12
L1
C8
R11
C7
L2
C13
C6
C10
C11
T
R
T
L
L
R
+
O

OPTICAL SQUELCH

Many of the less expensive shortwave receivers have no squelch circuit and continue to emanate noise when no usable signal is coming in. Fortunately, they normally have an LED which lights to indicate that the level of an incoming signal is at or above a predetermined limit. This LED can be used to control a light dependent resistor (LDR). The potential across the LDR can serve to actuate a circuit that switches the loudspeaker or headphones off in the absence of a suitable signal. This is possible without any work in the receiver itself by connecting an external loudspeaker to the headphone output. Inserting the plug into this socket automatically switches off the internal loudspeaker. The connection to the external loudspeaker is via the contact of relay Re_1.



The circuit is based on comparator IC_1. P_1, R_1 and R_2 provide the reference voltage at the inverting input of the opamp, which in the quiescent state (when no light falls on to R_4, which then has a high resistance) is higher than the potential at the non-inverting input. When light falls on to R_4, its resistance decreases, whereupon the level at the non-inverting input of the comparator becomes higher than that at the –ve input. The output of the comparator then changes state and switches on T_1, whereupon the relay is energized. The relay contact then connects the loudspeaker to the headphone output.

During construction it should be borne in mind that the less ambient light falls on to the LDR, the better the squelch will perform.

Preset P_1 should be adjusted so that the relay is not energized when the LED is out, but is actuated as soon as the diode lights. If difficulties arise in the setting of P_1, they are probably caused by the LDR having an incorrect value. In the diagram, the values of R_1, R_2 and P_1 are suitable for use with an LDR that has a resistance when light falls on to it of about 6 kΩ. Measure this resistance with a multimeter; the value of R_1 should be made (about) equal to this, and that of P_1 about twice as high. The value of R_2 and R_3 should be roughly the sum of the values of P_1 and R_1.

The power supply may be taken from the receiver; if that is not possible, a separate mains adaptor should be used. The circuit draws a current of about 5 mA plus the relay current.

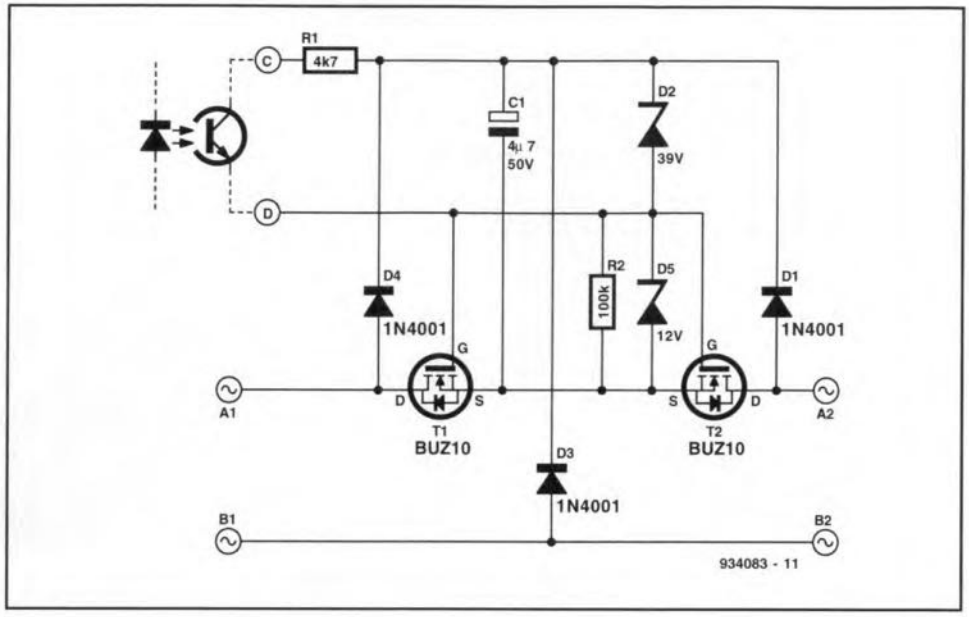
[K. Walraven - 934053]

LOW-DROP A.C. SWITCH

FOR 12 V HALOGEN LIGHTS

Because of their inertia, power consumption, contact wear, and often size, relays are not really suitable for switching alternating voltages. Moreover, they cannot be used in phase control circuits. Replacing them by triacs may give problems owing to the forward voltage drop across these devices.

A much better solution is the use of anti-series-connected SIPMOS transistors. Unfortunately, these need a control voltage that is isolated from the alternating voltage to be switched. This difficulty is, however, overcome by making use of the inverse diodes of the transistors as shown in the diagram.



In the off condition, when the optoisolator does not conduct, C_1 is charged during the negative half period (A positive, B negative) via D_3 and one of the inverse SIPMOS diodes. If the output is terminated, the capacitor will also be charged during the positive half period either via D_4 and the inverse diode of T_2 (load between A2 and B2), or via D_4 and the inverse diode of T_1 (load between A1 and B1).

The circuit is switched on by making the optoisolator conduct, whereupon the voltage across C_1 is connected to the gates of T_1 and T_2 via R_1 and the transistor in the optoisolator. Diode D_5 prevents the gate voltage becoming too high. When the circuit is on, C_1 continues to be charged during the negative half periods via D_3 and one of the SIPMOS transistors.

Diode D_2, in conjunction with D_1 and D_4, suppresses current peaks caused by the switching of inductive loads.

The circuit can switch alternating voltages of up to 45 V. Without a heat sink for the SIPMOS transistors, the maximum current should not exceed 3 A. For larger currents or when large inductive loads are switched regularly, a small heat sink should be used.

[B.C. Zschocke - 934083]

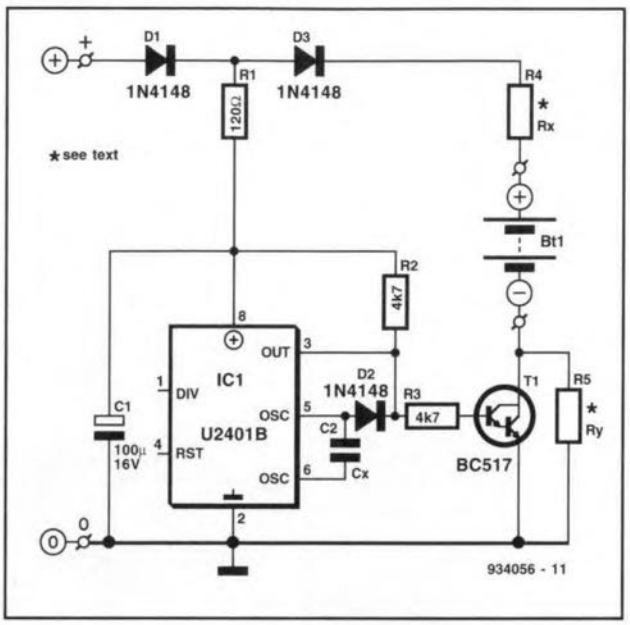
BUTTON-CELL CHARGER

In miniature circuits, the trend is away from expensive dry button cells and to NiCd button types. These batteries are easy to maintain: they may be charged with a constant current for a certain, fixed period, normally 14–16 hours.

The usual NiCd battery chargers are generally not suitable for charging button cells, as their minimum charging current is too high for these cells. The charger described here operates from a 9-V mains adaptor and can charge from one to five button cells.

D_1 is a protection diode, while R_1 and C_1 decouple the supply line to charging processor IC_1, an economy model of the well-known U2400B. D_3 is a safeguard against polarity reversal of the button cells. R_4 limits the charging current to 5 mA. During trickle charging, a current of 0.5 mA flows through R_4 and R_5. The value of C_2 determines the charging time. After the mains adaptor is plugged in, the cells are charged at full current for a period shown in the table (T_1 is on); after that period, trickle charging takes place (T_1 off). The trickle charging current is always $^1/_{10}$ of the full charging current.

[J. Heine - 934056]



C_2 (nF)	Charging time
15	0:58
18	1:10
22	1:26
27	1:46
33	2:09
39	2:33
47	3:04
56	3:40
68	4:27
82	5:22
100	6:33
120	7:51
150	9:49
180	11:47
220	14:25
270	17:41

Table 1

Capacity (mAh)	Charging Current (mA)	R_4 (kΩ) for number of cells 1	2	3	4
8	0.5	15	12	8.2	4.7
15	1.0	6.8	5.6	3.9	2.7
18	1.5	4.7	3.9	2.7	1.8
36	2.0	3.6	2.7	2.2	1.2
75	2.5	2.7	2.2	1.8	1.0
120	5.0	1.5	1.2	0.82	0.47
190	10	0.68	0.56	0.39	0.27
230	15	0.47	0.39	0.27	0.18
310	25	0.36	0.27	0.22	0.12

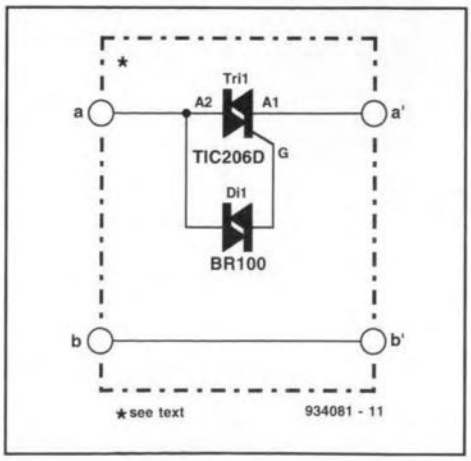
$R_5 = 0.1R_4$

Table 2

PRIVACY PHONE

Undesired listening-in to telephone conversations may be prevented by the present circuit, which requires only two components to protect a telephone.

In each telephone to be protected, a triac is inserted in series with the *a* line. A diac is connected between the anode and the gate of the triac. The trip voltage of the diac is about 25 V, which is appreciably lower than the line voltage of about 50 V, and considerably higher than the potential across a telephone set that is in use (5–12 V). Thus, the triac is switched only if the receivers of all the parallel telephones are on the hook. As soon as a receiver is lifted, the voltage across all sets drops from about 50 V to at most 12 V, so that no diac can be tripped. If, after the receiver has been lifted, the polarity of the line voltage reverse, the diac is not affected. When a call signal is received, all triacs conduct, so that the bell on each telephone will ring.



An added advantage of the present circuit is that it suppresses the parallel tinkling of telephones when a number is dialled on one of them (this happens only where older telephone exchanges are still in use).

The circuit is small enough to be built into the telephone line outlet box.

[L. Lemmens - 934081]

INFRA-RED CONTROLLED REMOTE SWITCH

Nowadays, several manufacturers produce ICs that combine an infra-red receive LED with associate amplifier and demodulator. The Type SFH505A from Siemens, used in the present circuit, has in addition a band-pass filter to minimize any interference. It is best used in conjunction with the infra-red transmitter in the next article.

The output of IC_1 is limited to a maximum pulse width. This is used to advantage by the associated transmitter to span as long a distance as possible. Most commercial remote controls use modulated data transfer, in which the pulse width is smaller than IC_1 can handle. The difference is easily detected by an integrator, R_2-C_2, and a Schmitt trigger, formed by the –T input of monostable IC_{2a}. The time constant is just short enough to ensure that at the maximum pulse width of IC_1 the voltage across C_2 is just under the trigger threshold of IC_{2a} (IC_1 has an active low output, which is why it is connected to the negative trigger input of IC_{2a}). Note that remote control units of, for instance, Sony or Philips, have no effect on the present circuit.

The monostable is retriggerable, so that any bounce at the transmitter does not affect the wanted state of the circuit. The mono time has been set at about half a second. The circuit cannot, therefore, switch on and off rapidly. If nevertheless several or repeated pulses arrive at the trigger input, they cause a lengthening of the output pulse, but the state of the circuit gets changed only once.

The output at pin 7 of IC_{2a} clocks D-type bistable IC_{3a} at the last transition (trailing edge). The bistable is arranged as a binary scaler, so that the circuit can be switched on and off by repeated transmissions.

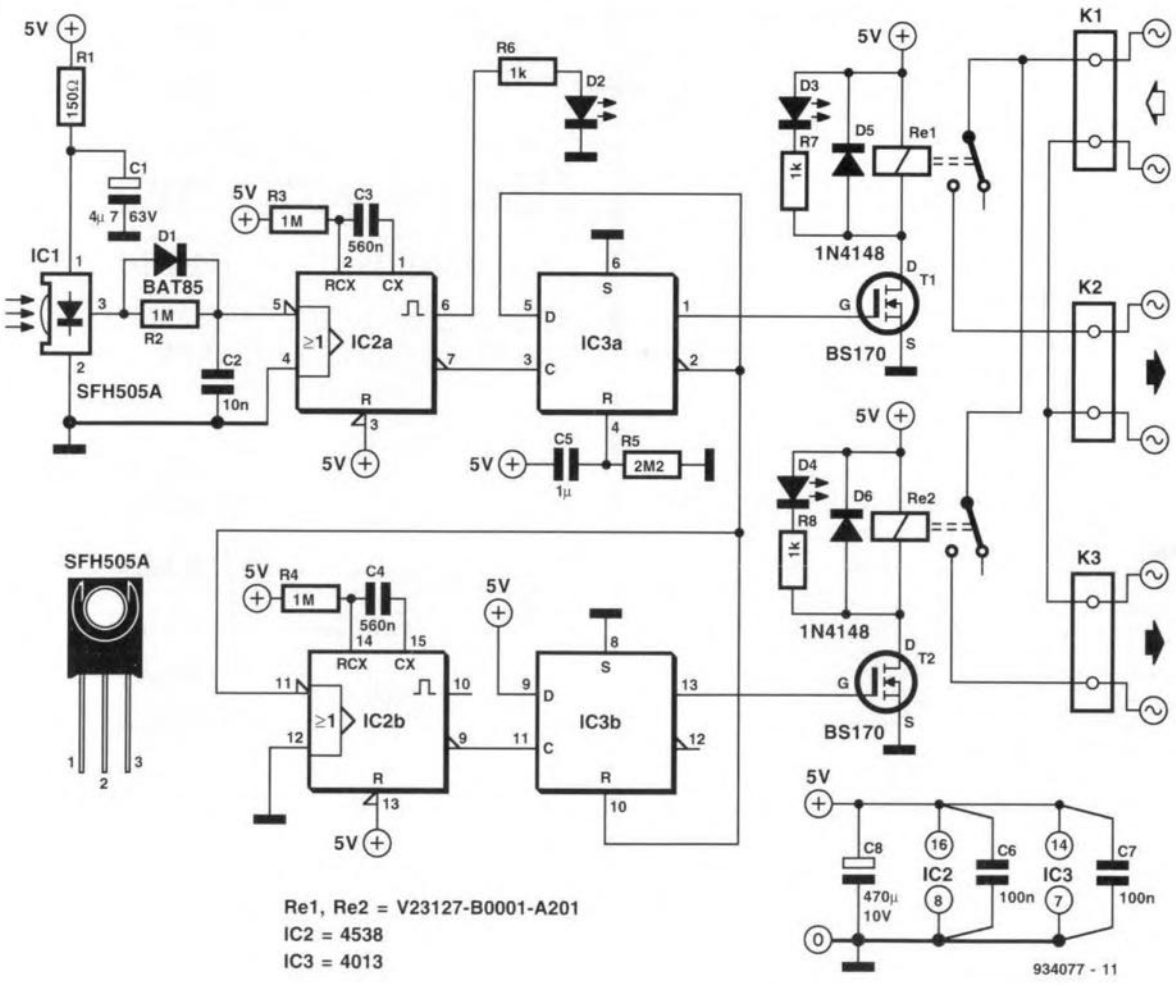
Diode D_2 indicates that IC_{2a} has received a trigger pulse. If interference is experienced from other remote controls, this is indicated by D_2.

The output of IC_{3a} energizes one of the relays via T_1. At the same time, it triggers monostable IC_{2b}, which energizes the second relay via IC_{3b} and T_2. In this way, the second relay is energized a good half a second after the first. This enables several apparatuses to be switched on in two steps. Diodes D_3 and D_4 indicate when the relays are actuated. The relays can switch up to 2000 VA (8 A).

The switch-on current of an equipment may be limited by first switching on the mains voltage with one relay via a series resistor and use the second relay to short out the series resistor.

The circuit draws a current of about 0.6 mA when the relays are unenergized and the LEDs are out. When the relays are actuated and the LEDs light, this increases to 125 mA.

[T. Giesberts - 934077]



Re1, Re2 = V23127-B0001-A201
IC2 = 4538
IC3 = 4013

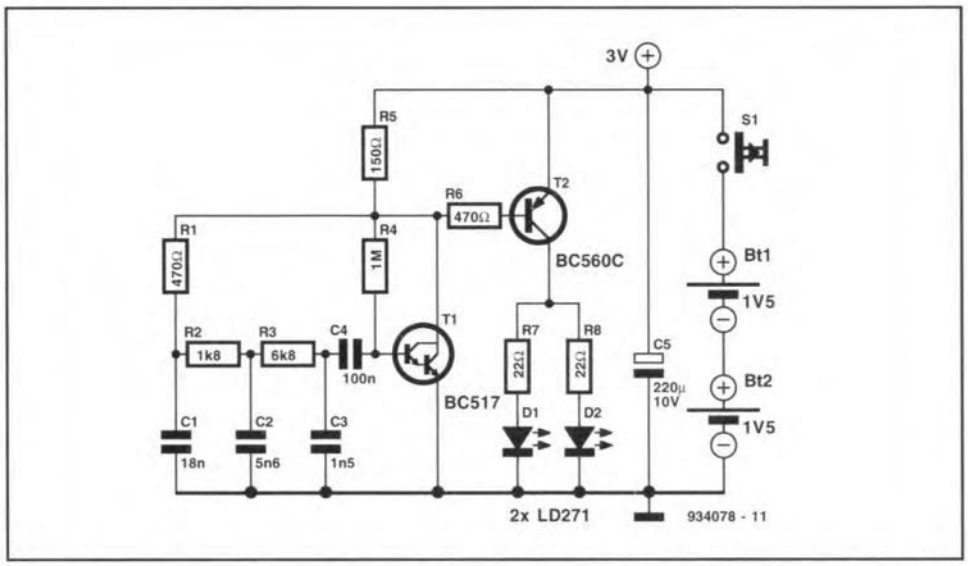
BASIC INFRA-RED TRANSMITTER

The transmitter is intended primarily for use with the receiver in the preceding article. It works from two small 1.5 V dry batteries or one 3 V lithium battery. To make the unit compact and yet have reasonable frequency stability, the design uses a phase-shift oscillator, T_1, which provides good frequency stability. To ensure that the transistor has sufficient amplification at the low supply voltage, it is a darlington.

Each of the branches of phase-shift network, R_1-C_1-R_2-C_2-R_3-C_3 has roughly the same time constant. To ensure that the branches do not affect each other unduly, $R_2 \approx 3.8 R_1$, and $R_3 \approx 3.8 R_2$. Because of this mutual influence, the gain of the amplifier is somewhat higher than the theoretical value of 18 dB.

The value of R_5 is a compromise. It needs to be low so as not to affect the phase-shift network (the output impedance of T_1 also affects the oscillator frequency). At the same time, it must not be too low, because that would increase the current and reduce the gain.

To lessen the influence of the base-emitter resistance of buffer T_2, this transistor is driven by T_1 via an independent resistor, R_6. The buffer is necessary to provide sufficient current for the LEDs. Owing to the low supply voltage, these diodes cannot be connected in series, and they are, therefore, driven independently via their own series resistor, R_7 and R_8.



The transmitter is switched on and off by connecting or disconnecting the supply voltage with S_1. A drawback of this is that current continues to flow as long as S_1 is pressed. Briefly pressing of S_1 is, however, sufficient to switch the receiver on or off.

The current drawn by the circuit depends on the supply voltage and on how long S_1 is pressed. When $U_b = 2$ V, the frequency is 29.3 kHz, the peak current through each of the LEDs is 25 mA, and the total current drain is 27 mA. When $U_b = 3.2$ V, the frequency is 30.4 kHz, the peak current through each of the LEDs is 64 mA, and the total current drain is 63 mA.. At this supply voltage, the range between the prototype transmitter and receiver was 13 m (43 ft).

The current drain may be reduced by connecting in series with S_1 a parallel *RC* network ($R = 10$ kΩ; $C = 1000$ µF, 6.3 V). When S_1 is then pressed, only a brief current pulse ensues; even if S_1 is held down, the current does not rise above about 300 µA.

[T. Giesberts - 934078]

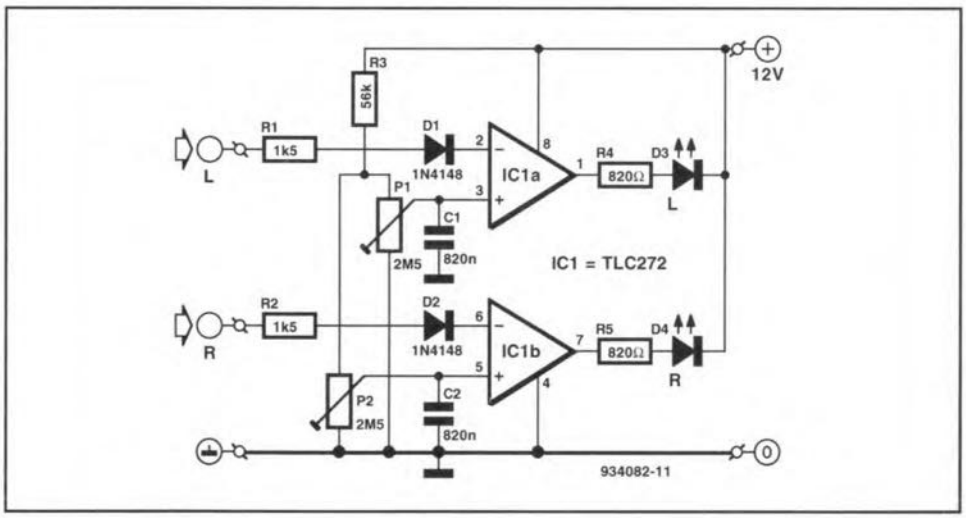
PEAK LEVEL INDICATOR

The indicator shows by means of two LEDs when the signal level in either channel of a stereo audio system exceeds a preset value.

In the diagram, IC_{1a} and IC_{1b} function as comparators. A reference voltage of 0–11 V is applied to their non-inverting inputs by P_1 and P_2 respectively. Resistor R_3 ensures that the reference voltage cannot exceed the common mode range of the opamps.

The signals from the two channels are rectified (half-wave) by D_1 and D_2 and the resulting direct voltage is applied to the inverting inputs of the opamps. Since the input impedance is high, the drop across the diodes is only 200–300 mV. Resistors R_1 and R_2 serve to limit the input current if the drive levels exceed the common mode range.

When the peak value of the input signal rises above the reference voltage less the drop across the diode, the output of the relevant opamp changes state (goes low), whereupon the associated LED lights.



The circuit may be used at frequencies up to 20 kHz (allowing for variations in peak levels of ±0.25 dB).

The indicator draws a current of only 0.25 mA when the LEDs are out and of 24 mA when both LEDs light. This drain may be reduced by the use of high-efficiency LEDs (which draw only 2–3 mA). The value of R_4 and R_5 should then be increased to 3.3 kΩ.

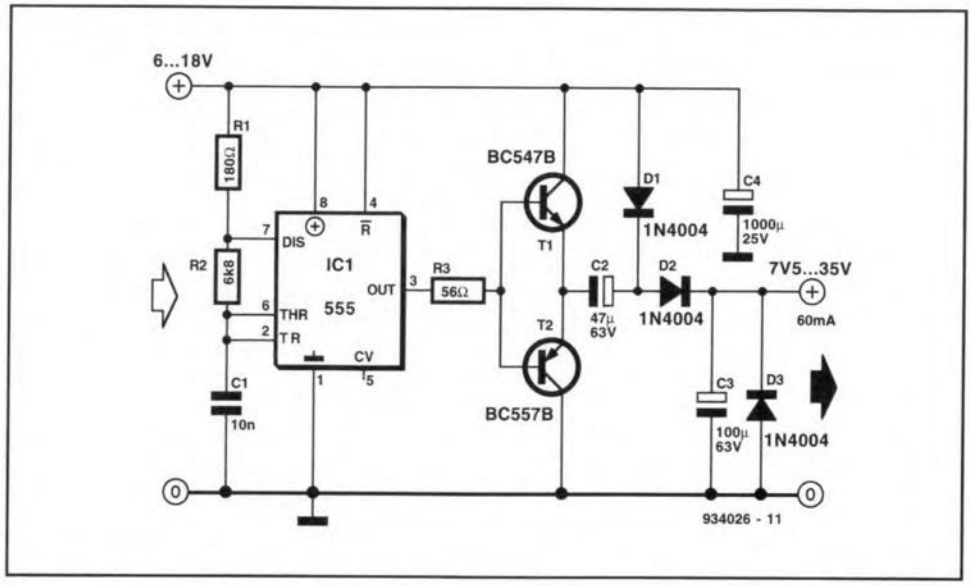
[Amrit bir Tiwana - 934082]

SIMPLE DC TO DC CONVERTER

To keep the converter simple, it contains no preset controls, which means that the level of the output voltage is dependent to some degree on the load. In theory, the output level is twice the level of the input voltage, but, owing to losses in the converter, that level cannot be attained. The main losses occur at the semiconductor junctions of the transistors and the rectifier diodes. Since the drop at these junctions is constant at about 0.6 V, the losses are proportionally larger with an input voltage of 6 V than with one of 18 V.

Oscillator IC_1 generates a signal at a frequency of about 10 kHz. Depending on the output level of the IC, either T_1 or T_2 is switched on. This results in C_2 being charged during one half period; during the other half period, the charge of C_2 is transferred to C_3. This results in the output voltage being twice the input voltage less the losses mentioned.

The circuit contains no critical components; IC_1 may be any version of the 555, bipolar or CMOS, while the transistors may be inexpensive LF types.



Although the present circuit uses 1N4004 diodes, Types 1N4001 will do just as well.

Although the switching frequency is of the order of 10 kHz, and the diodes are designed for lower frequencies, no problems were experienced in the prototype, primarily because the voltages and currents are relatively small.

The converter draws a current of 5 mA (555) plus twice the output current.

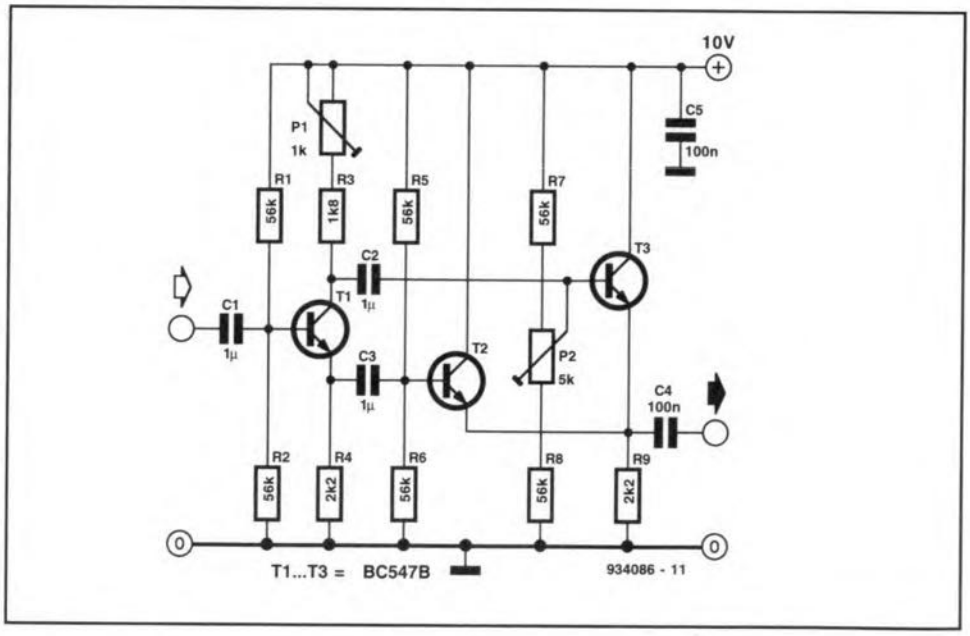
[Amrit Bir Tiwana - 934026]

FREQUENCY DOUBLER

The circuit of the frequency doubler may be looked at from different angles. With input signals ≥1 V, T_2 and T_3 operate as full-wave rectifiers. This means that the fundamental frequency of the input signal is automatically doubled. With input signals <1 V, the two antiphase signals produced by T_1 from the input signal are applied to the emitters of T_2 and T_3 and summed. This means that the fundamental frequency will virtually disappear, so that, because of nonlinearities, only the harmonics remain: the first harmonic will then become the new fundamental frequency in the output signal. This means, of course, that the signal strength reduces appreciably: of an input of 25 mV, only 6 mV remain.

Assuming that the input is sinusoidal, the suppression of the fundamental frequency is optimized with P_1. The operating point of T_3 should be set with P_2 for as near a sinusoidal output as possible. In the protype, the output signal showed a distortion of 5.5% with an input signal frequency of 1 kHz.

The input frequency range is 80 Hz to well over 100 kHz.



Any tendency of T_2 or T_3 to oscillate may be suppressed by soldering a small ceramic capacitor (about 56 pF) between the base and collector of the transistor.

The circuit draws a current of about 4 mA.

[Amrit Bir Tiwana - 934086]

WIND DIRECTION INDICATOR

The indicator shows eight wind directions by means of LEDs. The sensors are reed contacts powered by a permanent magnet. The mechanical construction must be such that it is impossible for more than one reed contact to be closed at any one time.

At the instant a reed contact closes, a leading transition (edge) is applied to the clock inputs of D-bistables (flip-flops) IC_2 and IC_3 via an OR gate in IC_1. This results in the outputs of the bistables assuming the status of the D inputs, so that only the LED associated with the closed reed contact lights.

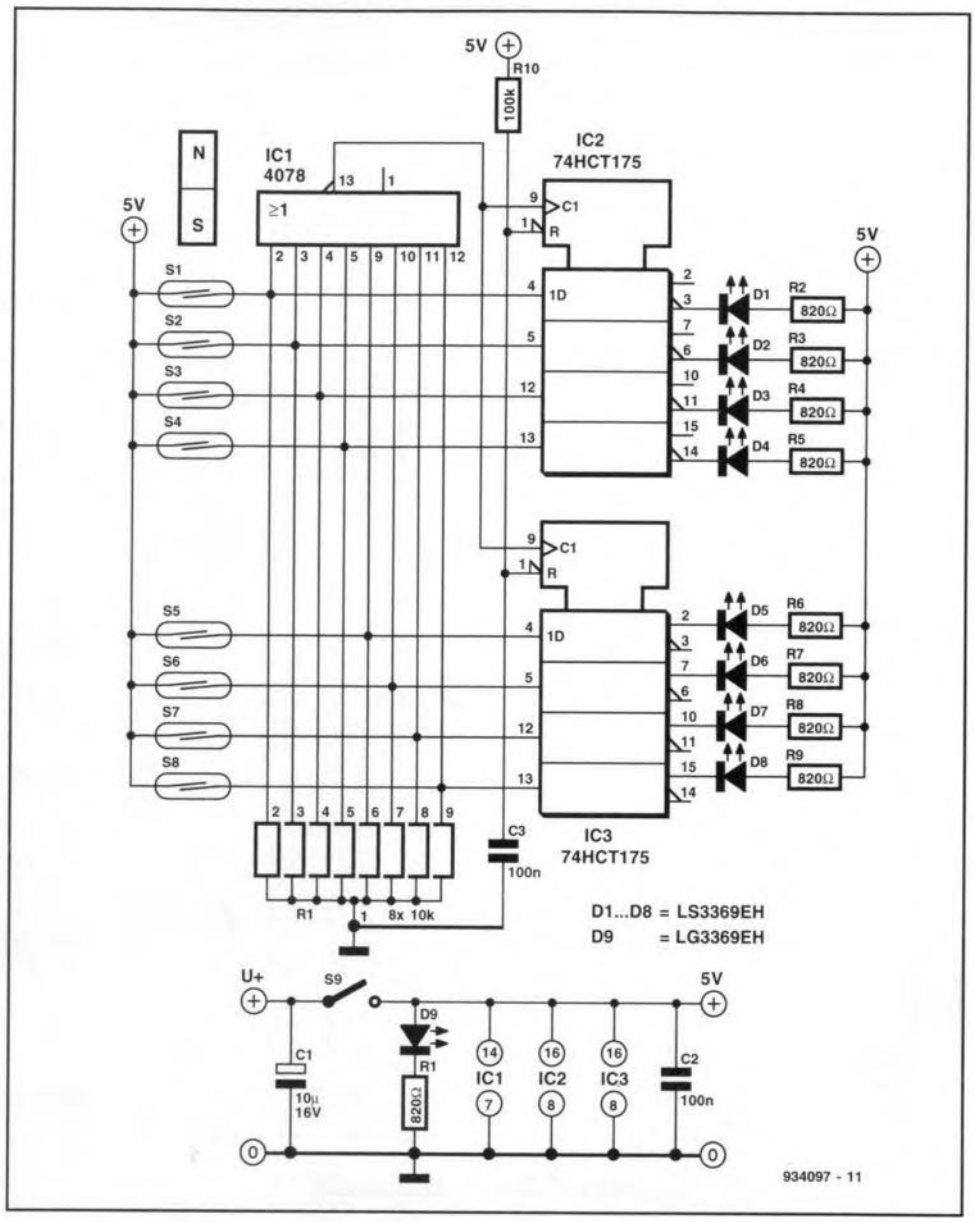
If the wind changes direction slightly, and the reed contact opens, then, owing to the bistable construction, the LED will continue to light. Only when the wind has changed direction so much that another reed contact closes will a different LED light.

When the supply voltage is switched on (S_1), only D_9 will light owing to the power-on reset via R_{10} and C_3. Only when one of the reed contacts has caused a leading transition (edge) at the clock inputs will one of the direction LEDs (D_1–D_8) light.

The indicator needs to be supplied by a regulated 5 V source. It draws a current of not more than 10 mA.

The LEDs are low-current Siemens types.

[J. Ruiters - 934097]



REGULATOR SHORT-CIRCUIT INDICATOR

Modern integrated voltage regulators are protected against short circuits, but do not give an indication when a short circuit occurs. In the case of regulators with fixed output (78xx) a short-circuit indicator is easily arranged by connecting an LED and series resistor across the regulator output. The LED will light only during normal operation, that is, input available and output not short-circuited.

If this sort of indicator is used with regulators with a variable output, such as the LM317, the brightness of the LED will vary with the set output. To make the brightness constant, the current through the LED must become independent of the output voltage. The LED current must then not be limited by a series resistor but by a current source. Such a source can be made with only one extra component: T_1 in the circuit diagram.

The design makes use of the available reference voltage across R_1. This voltage is generated by the LM317 and serves in the first instance, in conjunction with R_1, R_2 and P_1, to regulate the output voltage.

In the present circuit, the reference voltage is used to keep the drop across R_3 constant:

$U_{R3} = 1.25 - U_{eb} = 1.25 - 0.65 = 0.6$ V.

The current through D_3 is then 0.6/180 = 3.3 mA, which is more than ample for the low-current LED used here.

On the prototype, the LED current remains constant with output voltages from 3 V to 25 V. In other words, over that range of voltages, the LED lights with constant brightness.

The base current of T_1 is only 15 µA, so that the operation of the regulator is not affected by the branching off of the reference voltage.

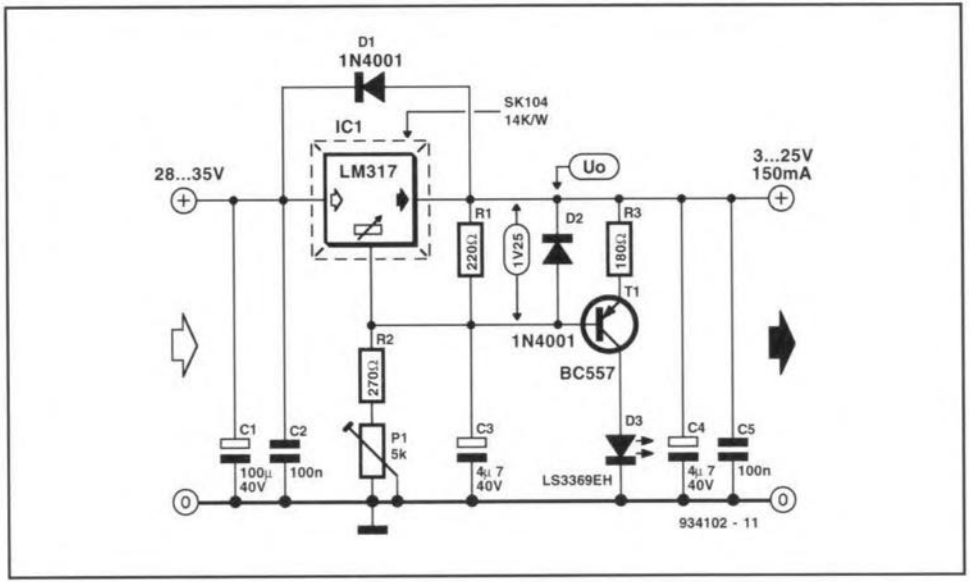
In the present circuit, T_1 dissipates only 100 mW when the collector-emitter voltage is 25 V. Since this transistor can dissipate up to 500 mW (with heat sink), overheating is highly unlikely. Also, its

collector-emitter voltage of 25 V is well below the maximum permissible 45 V. These limits should be borne in mind, however, if the power supply provides higher output voltages.

Capacitor C_3 increases the ripple suppression from 65 dB to 80 dB. Diode D_2 protects IC_1 and T_1 against too high a discharge current from C_3 and too high a base-emitter reverse bias (max. 5 V) when the regulator is short-circuited.

Diode D_1 protects the regulator against discharge currents from C_4 and any electrolytic capacitors in the circuit being supplied). Without this diode, these capacitors would discharge through the regulator should the input of this IC be short-circuited or be connected to a lower voltage.

The quiescent current of the indicator circuit is about 10 mA, while the peak current may rise to 1.5 A. At maximum input voltage (35 V) and minimum output voltage (3 V), the circuit can provide a constant current of about 150 mA.



[J. Ruiters - 934102]

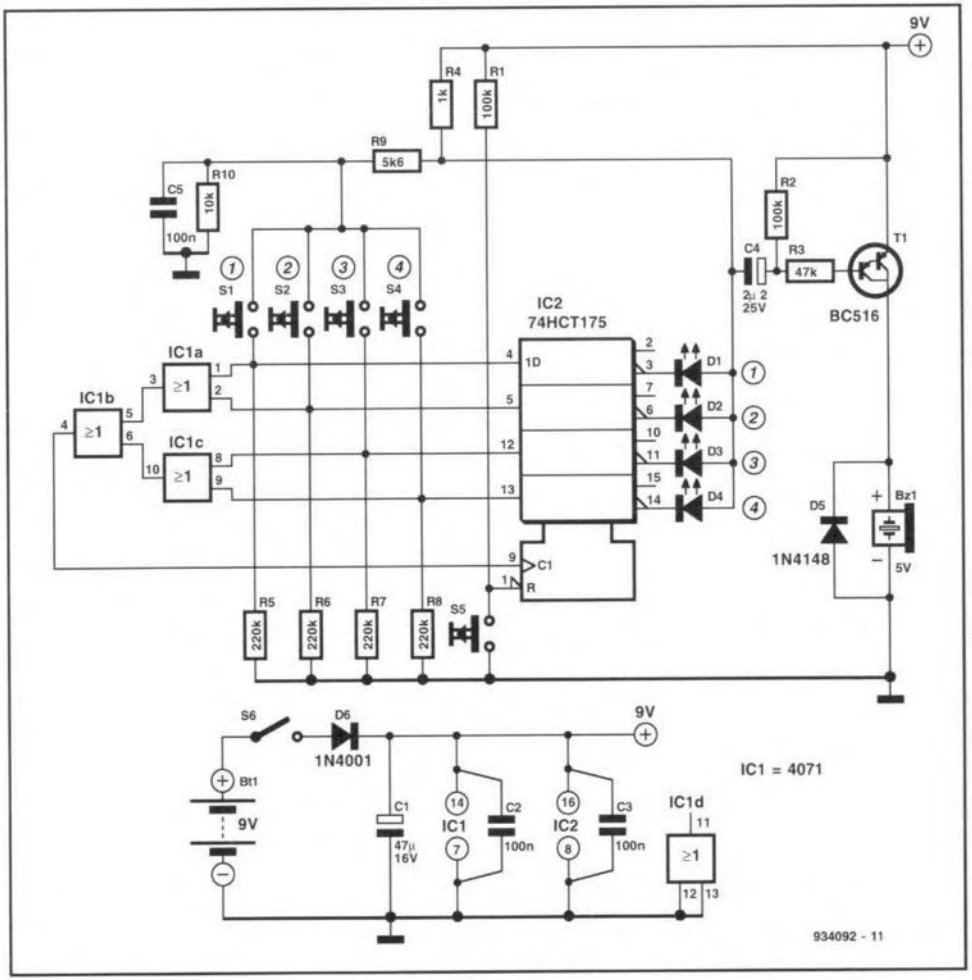
PRECEDENCE DETECTOR

The detector was designed primarily for use with quiz games. It indicates who has first pressed a push button by the sounding of a buzzer and the lighting of an LED. The quiz master can then reset the detector.

In the diagram, the four push buttons, S_1–S_4, are connected to the D inputs of four bistables contained in IC_2. They are also connected to the clock input of IC_2 via OR gates IC_{1a}, IC_{1b} and IC_{1c}. The Q outputs of the bistables drive D_1–D_4.

After the bistables have been reset with S_5 (which briefly makes the CLR input low), all Q outputs are high, so that the LEDs are out. If one of the push-buttons, say S_1, is pressed, a high level ensues at the associated D input. This high level is applied to the clock input of all bistables, whereupon the existing levels at the D inputs of the bistables are stored and applied to the outputs; D_1 will then light

Since the switches and the LEDs are connected to the supply line via a common resistor, R_4, the voltage at points after R_4 will drop to about 2 V owing to the lighting of D_1. Because of potential divider R_9-R_{10}, the voltage across the switches will be only about 1 V. If then one of the switches, other than S_1, is pressed, the voltage at the associated D input(s), as well as at the clock input, will be too low for the IC to react. In this way, the circuit is disabled after one of the switches has been pressed.



Darlington T_1 drives the d.c. buzzer. The base of T_1 is connected to the anodes of the LEDs via R_3 and C_4. At the instant one of the LEDs lights, C_1 passes this low level to T_1, which then energizes the buzzer. After about 0.5 s, C_4 is recharged via R_2 and R_3, so that T_1 is switched off.

The circuit draws a current of about 5 mA when the LEDs are out. When one of the LEDs lights and the buzzer sounds, the current rises to some 50 mA.

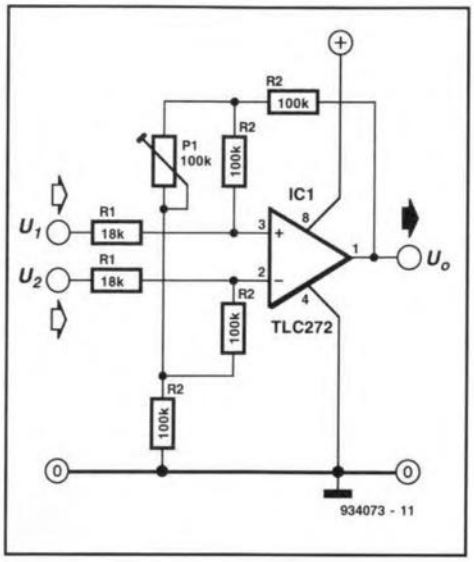
[D. Ibrahim - 934092]

VARIABLE DIFFERENTIAL AMPLIFIER

In a traditional differential amplifier with feedback to the –ve (inverting) input of an operational amplifier and a potential divider at the +ve (non-inverting) input, it is tricky to make the amplification variable. This is because the feedback network and the potential divider need to be each other's image to ensure satisfactory suppression of the common-mode signals (common-mode rejection ratio – CMRR). This means that there must be two variable resistors and these must at all times be equal.

This is not necessary with the present circuit in which one preset can arrange the amplification without affecting the CMRR. It has the following transfer function:

$$U_o = 2R_2/R_1(1+R_2/P_1)(U_2-U_1) \qquad [V]$$



It is clear from this that only P_1 affects the difference voltage $U_2–U_1$. The common-mode signal does not appear in the function. This is partly because P_1 has no effect on it and partly because the resistors with the same circuit reference also have the same value. In theory, that gives total rejection of common-mode signals; in practice, tolerances of the components used will determine the CMRR. To calculate that, however, the formula will have to be expanded appreciably.

[L. Lemmens - 934073]

TEMPERATURE MONITOR

The monitor is intended for use in relatively small spaces (like living rooms). The sensor is a readily available LM335 from National Semiconductor. This gives an output voltage of 10 mV °C^{-1}. This voltage is compared in IC_{1a} and IC_{1b} with two reference voltages. One of these is preset with P_1 and the other with P_2. The output of the comparators is used to switch D_2, D_3 and D_5.

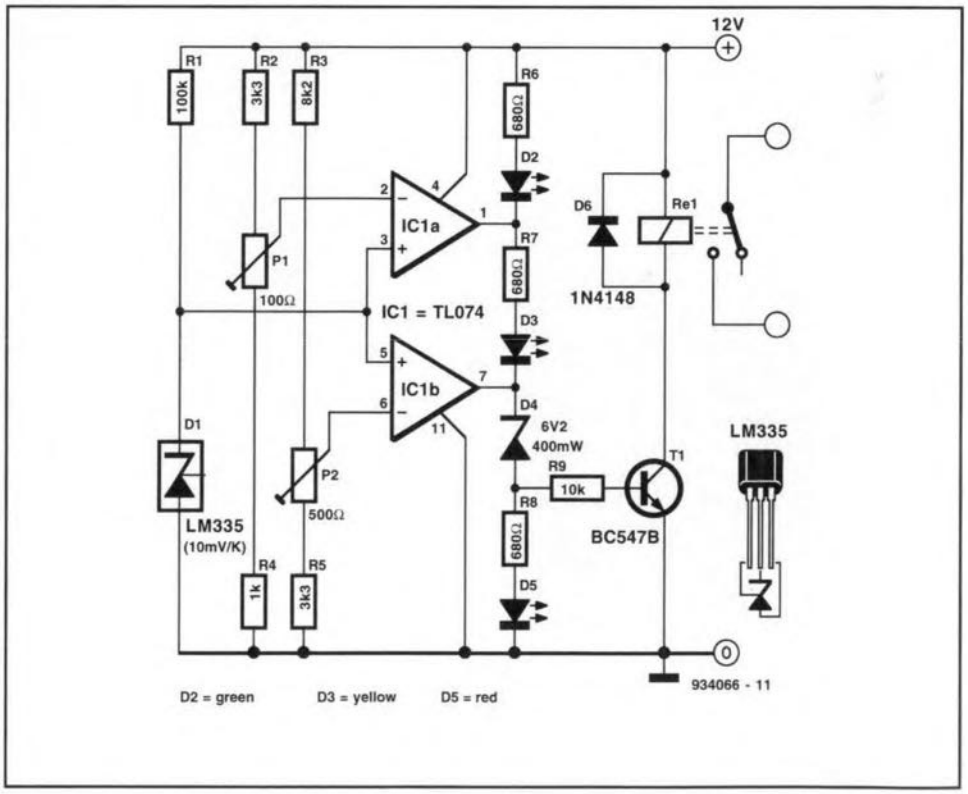
When the voltage produced by D_1 is smaller than either of the reference potentials, the outputs of IC_{1a} and IC_{1b} are low: D_2 will then light.

When the ambient temperature rises, the output of D_1 rises proportionally. When the level of the sensor output lies between the two reference levels, the output of IC_{1a} is high and that of IC_{1b} is low. Diode D_3 will then light, showing that the critical temperature has been reached.

At even higher temperatures, the output of IC_{1b} will also go high and D_5 lights, while the other two LEDs go out. At the same time, the relay will be energized via T_1. The relay contact may then actuate an external load (e.g., a buzzer).

Zener diode D_4 ensures that T_1 does not come on when D_3 lights (since the output voltage of IC_{1b} then rises slightly owing to the current through this IC).

The temperature at which the LEDs should light may be set with P_1 and P_2. Bear in mind, however, that the monitor is intended for 'normal' temperatures between 25 °C and 100 °C.



The monitor draws a current of about 20 mA; when the relay is energized, this rises to about 50 mA.

[M. Stehouwer - 934066]

SPECIAL BAND-STOP FILTER

Double T filters are used in many circuits. This type of filter can be made into a perfect band-stop filter, at least in theory. In the present circuit (**Fig. 1**), a double T filter is used in a different manner. It can have the characteristic of the combination of either a band-stop filter and a low-pass filter (switch S_1 in position 1) or a high-pass filter and a band-stop filter (S_1 in position 2). The characteristic curves are given in **Fig. 2** and **3** respectively.

The variable K in **Fig. 2** and **3** is determined by the setting of P_1. Variable M depends on the setting of P_2, and determines the Q factor.

A drawback of the present design is that the maximum suppression is diminished slightly. At $M = 0.75$, maximum attenuation is (calculated) 50 dB. With components values as in **Fig. 1**, the frequency at that attenuation is 1 kHz. Other frequencies can be computed easily. The band-stop frequency, f_{bs}, with S_1 in position 1 is

$$f_{bs} = 1/2\pi RCK. \quad [Hz]$$

With S_1 in position 2,

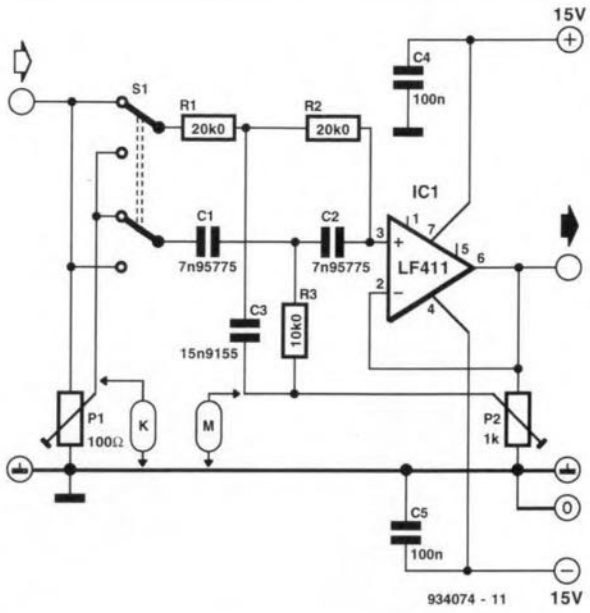
$$f_{bs} = K/2\pi RC. \quad [Hz]$$

In all cases, $0 \leq K \leq 1$; C is in farad and R is in ohms. Various types of IC may be used for the operational amplifier.

The current drawn by the circuit is around 2 mA.

[A. v.d. Veene - 934074]

1



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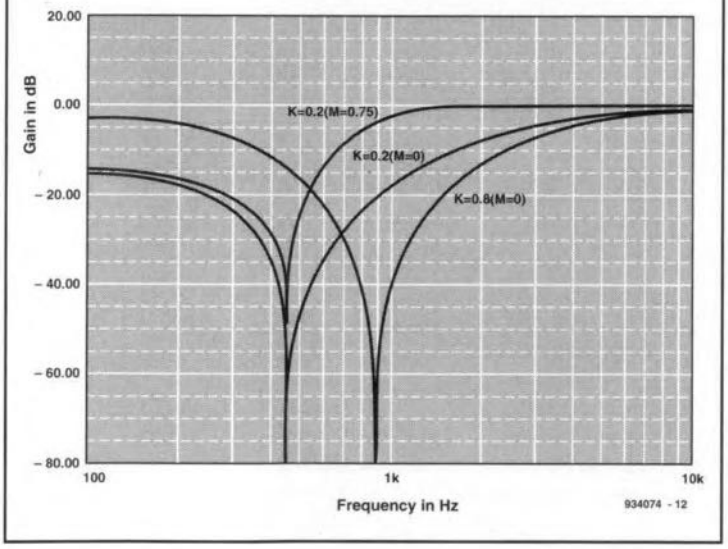

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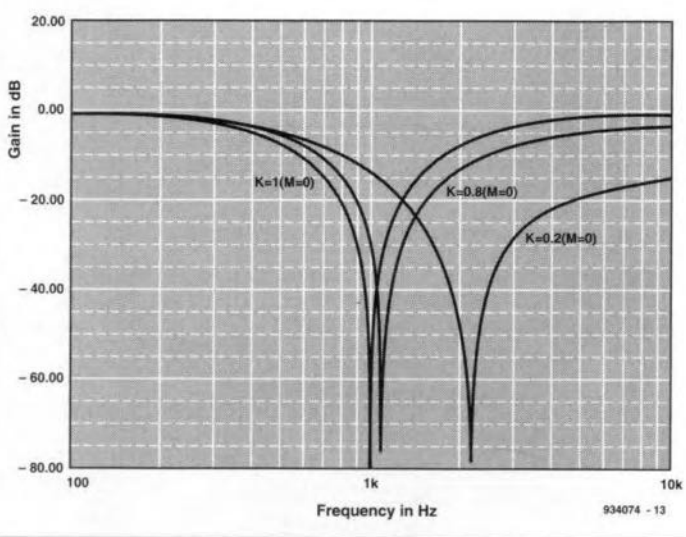


RC-5 INFRA-RED RECEIVER FOR 80C32 COMPUTER

RC-5 is the Philips/Sony standard for infra-red [IR] remote control of audio /video equipment (**Ref. 1**). The circuit and the listing given enable the 80C32 single-board computer (**Ref. 2**) to receive and process IR command signals sent by an RC-5 compatible IR remote control unit.

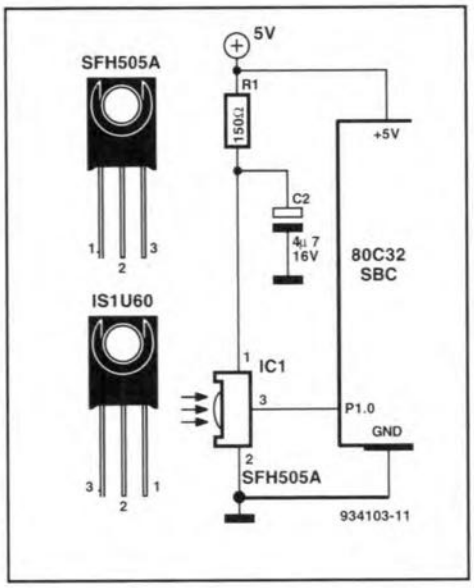
The hardware consists of a Siemens SFH505A IR detector connected directly to the P1.0 port line of the 80C32 microcontroller. The Sharp Type IS1U60 IR detector may be used as an alternative to the SFH505A, with the advantage of higher sensitivity thanks to a pass-band that is better 'tuned' to RC-5 signals*. Note, however, that the SFH505A and the IS1U60 have different pin connections. The IR detector supplies an inverted output signal (high level when no IR signal is detected), which has certain ramifications for the software.

The program (see listing) makes use of the EMON51 monitor program (**Ref. 3**).

Since all timings are based on software, it is essential that the 80C32 computer runs at a clock speed of 12 MHz. It should also be connected to a PC or a terminal, and have the EMON51 system monitor in EPROM. The LOOP routine ensures that the decoding always begins at the start of a new code. COUNT is the count loop proper. If P1.0 goes low during the wait time, R_6 is reset, and the waiting starts again.

Next, a number of registers are initialized to prepare for the reception of a new code, and the software waits for the first high-to-low transition. Note, however, that a half bit time of the new word has already elapsed when this H-to-L transition is actually detected. This means that $^1/_4$ bit time of the second start bit has elapsed after waiting $^3/_4$ bit time. Next, the level at P1.0 is monitored twice every bit time — first at $^1/_4$, and again at $^3/_4$ of the bit time. The bi-phase modulation used allows the microprocessor to determine if a '0' or a '1' is meant.

Actually, it is sufficient if a 'check' is carried out only once every bit time. If the synchronization is all right, and the check is made at $^1/_4$ of the bit time, the correct value is established automatically (remember that the input signal is inverted). Checking two times during every bit period, however, enables the software to flag receive errors.



The received bits are shifted into a 16-bit register formed by R4 (low) and R5 (high). The second start bit becomes the MSB. When the received word is complete, the two lowest system address bits are moved from R4 to the LSBs of R5, which leaves the six databits in R4, and the system address bits in the lowest five bits of R5.

Routine CTRL checks if the check bit has changed since the last decoding action. If so, the software decides that a new key has been pressed, or the same key has been pressed again, whereupon the RC-5 system address (that is, the equipment identification number) and the data (that is, the control action required) are sent to the PC. If not, the program jumps back to the start. By omitting the JZ LOOP instruction, the address and data are transmitted on every received code ('auto repeat').

(K.D. Gens — 934103)

References:

1. Universal RC5 code infrared receiver. *Elektor Electronics* January 1992

2. 8051/80C32 single-board computer. *Elektor Electronics* May 1991.

3. 8051/8032 Assembler course (8 instalments). *Elektor Electronics* February to November 1992.

* The IS1U60 detector is available from Hero Electronics Limited, Dunstable Street, Ampthill, Beds MK45 2JS. Telephone: (0525) 405015. Fax: (0525) 402383.

```
; 8032 RC5 decoder using EMON51

; SFR addresses
ACC             EQU             00E0H
B       EQU             00F0H
P1      EQU             0090H

; EMON51 routines
ccCHR           EQU             0001H           ; send character
to PC
ccBYTE  EQU             0003H           ; send byte to PC
command EQU             0030H           ; EMON51 command register
MON             EQU             0200H           ;EMON51 jumpad-
dress

        ORG             4100H           ; program start address

; LOOP waits for 1.5 bit times HIGH signal to ensure that the
; received RC5 signal starts at the start bits. SFR R6 is reset
; if a LOW level is received during this wait cycle.
LOOP            MOV             R6,#0           ; 255 x 14 µsec
COUNT           MOV             A,P1
        ANL             A,#1
        JZ              LOOP            ; no RC5 code received
        MUL             AB              ; wait 4 cycles
        MUL             AB              ; wait 4 cycles
        DJNZ            R6,COUNT

; Receiver ready to detect and decode an incoming RC5 signal

; count 13 bits, ignore first start bit
WORD            MOV             R7,#13
        MOV             R5,#0           ; reset address
        MOV             R4,#0           ; and data register
; H-to-L edge detected after the first bit half of the start
bit.
HIGH            JB              P1.0,HIGH   ; wait for H-to-L edge
        MOV             A,#110      ; wait 1/4th bit time
        LCALL           WAIT
        MOV             A,#220      ; wait 1/2 bit time
        LCALL           WAIT
NXTBIT  MOV             A,P1            ; input 1st half 2nd bit
        ANL             A,#1            ; mask bit 0 (=P1.0)
        MOV             R6,A            ; store bit
        MOV             A,#220      ; wait 1/2 bit time
        LCALL           WAIT
        MOV             A,P1            ; input 2nd half 2nd bit
        ANL             A,#1

        CLR             C
; Compare first and second half bit:
;       L-to-H change = HIGH-bit
;       H-to-L change = LOW-bit
        SUBB            A,R6

; if 1st and 2nd bit halves are equal: ERROR!!
        JZ              LOOP
        MOV             A,R4            ; get data register
        RLC             A               ; carry to data register
        MOV             R4,A            ; store data
        MOV             A,R5            ; get address register
        RLC             A               ; shift and
        MOV             R5,A            ; store
        MOV             A,#218      ; wait 1/2 bit time
        LCALL           WAIT
        DJNZ            R7,NXTBIT   ; next bit or end of word
; data is only 6 bit, shift two MSB's into address register
        MOV             R7,#2
SHIFT           MOV             A,R4
        RLC             A               ; shift data
        MOV             R4,A
        MOV             A,R5
        RLC             A               ; shift carry to address
        MOV             R5,A
        DJNZ            R7,SHIFT
        MOV             A,R4            ; shift back data
        RR              A
        RR              A
        MOV             R4,A
; skip the next part if auto repeat is required
CTRL            MOV             A,R5
; check control bit (bit 5 in address register)
        ANL             A,#20H
        MOV             B,A             ; control bit in B
        XRL             A,R3            ; compare with last value
        MOV             R3,B            ; store control bit
; If the control bit has changed, send new address and data to
; PC, otherwise go to start of program and wait for new code.
        JZ              LOOP

; Send the result to the PC, two subsequent codes separated by
; a SPACE character.
SNDBYT  MOV             A,R5            ; read address + ctrl bit
        ANL             A,#1FH      ; mask three MSB's
        MOV             command,#ccBYTE
        LCALL           MON             ; send byte to PC
        MOV             A,R4            ; read data byte
        LCALL           MON             ; send byte to PC
        MOV             A,#20H      ; ASCII value of SPACE
        MOV             command,#ccCHR
        LCALL           MON             ; send space character
        LJMP            LOOP            ; start again

; Waste some time ((ACC x 4 + 4)µs)
WAIT            NOP
        NOP
        DJNZ            ACC,WAIT
        RET

        END
934103-12
```

COMPACT A-D CONVERTER

Although good and inexpensive integrated analogue-to-digital (A-D) converters are now readily available, it may be instructive to build one from discrete components.

The present convertor is based on a Type TLC274 IC, which contains four comparators. The outputs of these stages also form the output of the converter.

The problem with designing A-D converters is producing a correctly tracking reference voltage. In fact, each bit requires a small digital-to-analogue (D-A) converter to generate the needed reference. This problem is usually solved by assigning the MSB comparator half the supply voltage as reference: this is produced by potential divider R_1-R_2. For each subsequent bit, the preceding bits are then added to the reference voltage, which requires a few resistors. In case of bit B, this means that bits C and D are used; for bit A, bits B, C and D are used. The translating of the level of these bits is effected by IC_2 and R_1–R_{14}.

The regulated 5-V supply voltage forms the basis for the reference voltage. The levels at the outputs of the buffers should ideally be 5 V (logic 1) or 0 V (logic 0). The resistors in the potential divider should be close tolerance types to ensure good linearity. The higher the resolution (the more bits) of the A-D converter, the more accurate the resistors need to be. It should also be borne in mind that the output level of the buffers in IC_2 deviates more and more from the ideal the greater the current that must be provided. In other words, the value of the resistors must be relatively high. The problem is further minimized by connecting two non-inverting gates in parallel to increase fan-out. With values as shown, the voltage drop at the MSB output buffer (that which provides the largest current) was 6 mV in the prototype. Compared with the value of the LSB of 312.5 mV, this is negligible.

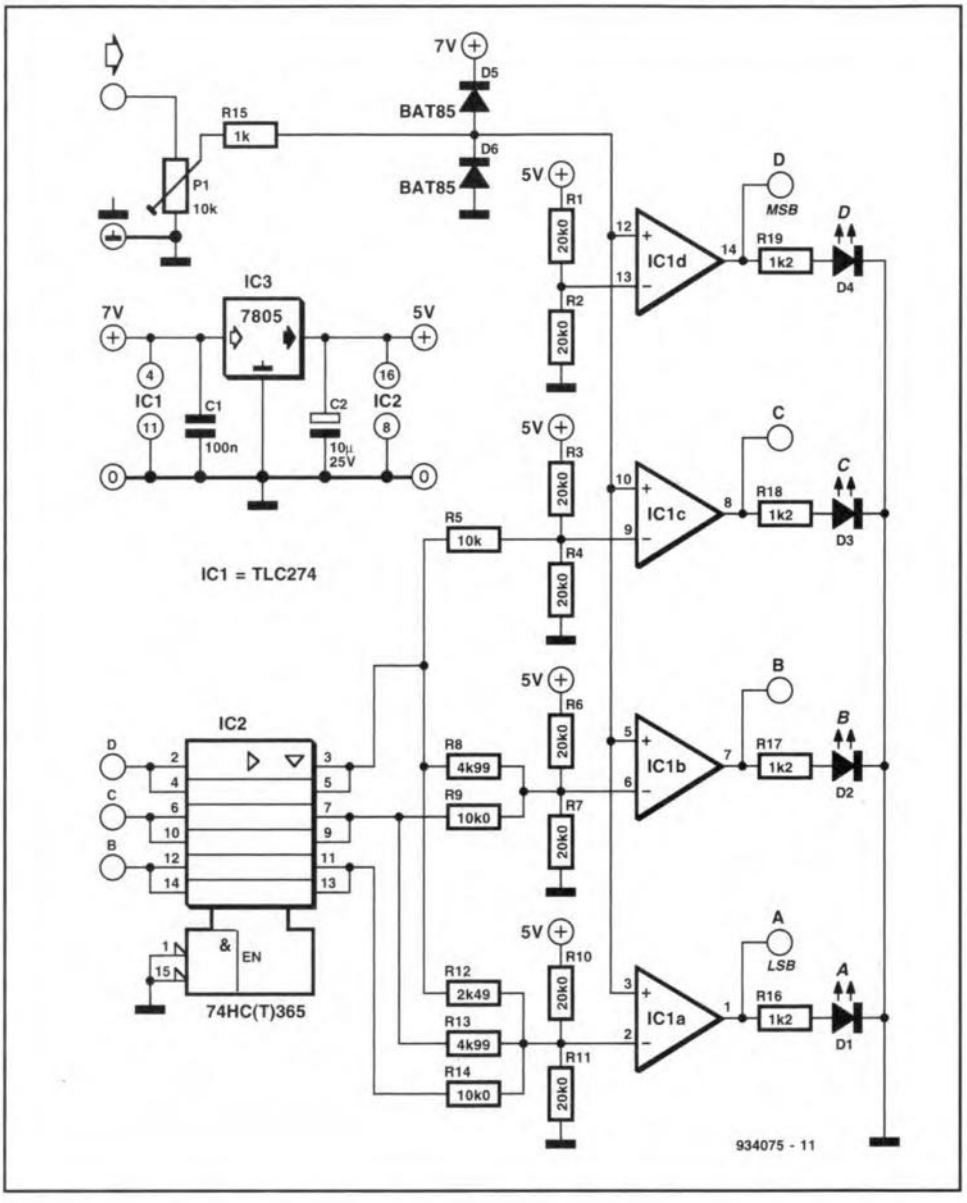
The conversion speed depends on the propagation times of the comparators and buffers. Although the TLC274 performs acceptably, for optimum results true comparators should be used.

The input sensitivity of the circuit is set with P_1.

Diodes D_5 and D_6 protect the opamp inputs against too high potentials.

The current drawn with all LEDs off is about 7 mA; with all four LEDs on, this rises to about 20 mA.

[T. Giesberts - 934075]



BATTERY CHARGING REGULATOR

Philips' IC Type TEA1100 uses the delta-peak principle* to charge NiCd and NiM_3 batteries fast and effectively. The ask of the delta-peak battery charging regulator is to ascertain and evaluate the **change** in the battery voltage: if the voltage at pin 7 drops 1% or more below the average maximum, charging is discontinued. The voltage at pin 7, according to the manufacturers' data sheet, must be 0.385–3.85 V. Potential divider R_4-R_5 ensures that the battery e.m.f. corresponds with this range. The values of these resistors are given by:

$R_4/(R_4+R_5)\cdot n\cdot 1.8 < 3.85$;

$R_4/(R_4+R_5) < 2.14n$;

$R_4/(R_4+R_5)\cdot n\cdot 1.1 > 0.385$;

$R_4/(R_4+R_5) > 0.35n$.

The charging current, I_c, is given by:

$I_c = 1.25R_{sense}/R_{shunt}\cdot R_{ref}$,

where R_{sense} is R_{10}; R_{shunt} is R_8 in paral-

lel with R_9; and R_{ref} is R_2.

Timeout, TO, is a safety facility of the IC. If, for whatever reason, no maximum can be detected, the IC stops the charging after the timeout. This time constant is given by

$$TO = 2^{26} \cdot 0.93 \cdot R_{ref} \cdot C_{osc},$$

where $C_{osc} = C_3$. Note that both timeout **and** charging current are influenced by R_2. When the charging current and timeout are being determined, the value of R_2 must therfore be fixed and that of C_3 must be variable.

When the battery is fully charged, the TEA1100 switches to the 'maintain charge' mode. In this mode, during $^1/_{10}$ of the normal charging time $^1/_2$ of the usual charging current flows (in other words, the battery is trickle-charged at $^1/_{20}$ of the normal charging current). This trickle-charge current may be altered on the basis of the following formula:

$$I_{trickle} = 1.25R_{sense} / 10R_{shunt}R_N.$$

The current is determined from the drop across the shunt resistor and switched by the transistors via pin 2 of IC_1.

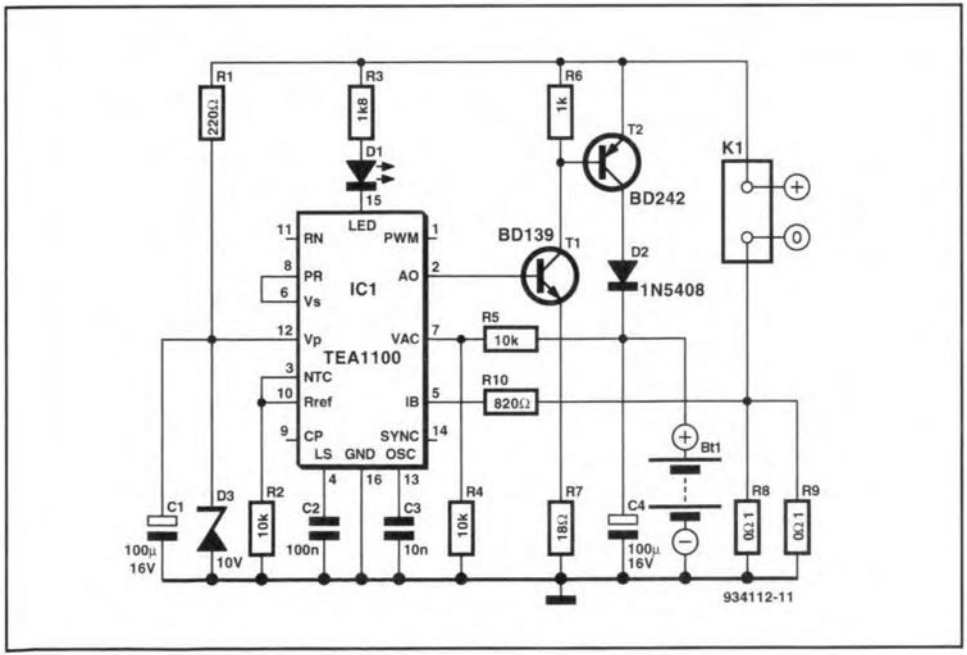
Stability of the circuit is ensured by capacitor C_2.

When no battery is connected to K_1 or when a battery is being trickle-charged, D_1 flashes; when the voltage at pin 7 drops, the LED lights continuously.

The supply voltage at pin 12 must be 5.65–11.5 V. The quiescent current (when the outputs are all off) is some 4 mA.

This IC enables many other applications: a number of these are given in Philips' Data Sheet TEA1100 & TEA1100T.

[A. Rietjens-934112]



The delta-peak principle was described in detail in the December 1992 issue (p. 86) of this magazine.

MULTI-COLOUR-LED

It had to come: an LED that can produce all visible colours. It is the Everlight Type 339-1 VRKGBBW. In fact, it consists of four LEDs in one case: one red, one green, and two blue.When these LEDs are driven into varying brightnesses, all visible colours and white can be produced. The circuit described makes the LEDs light in all colours in any given order.

The circuit consists of an integrator followed by a Schmitt trigger. Together these form an oscillator that produces a triangular voltage with an amplitude of about 1.5 V_{pp} at its pin 1. This signal is applied to one of the LEDs via T_1 and current limiting resistor R_5.

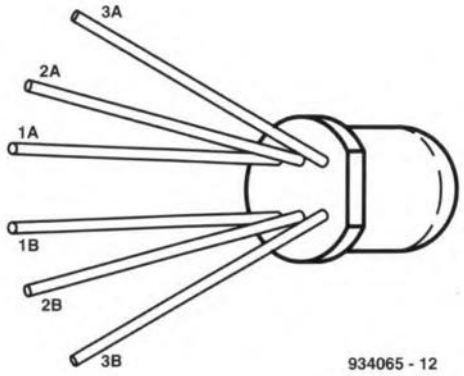
Three of these circuits should be built: one for the red, one for the green, and one for the two blue LEDs. Each circuit should, however, have a different value C_1, say, 470 nF, 330 nF, and 220 nF. Each of the blue LEDs, although connected to the same circuit, should have its own series resistor.

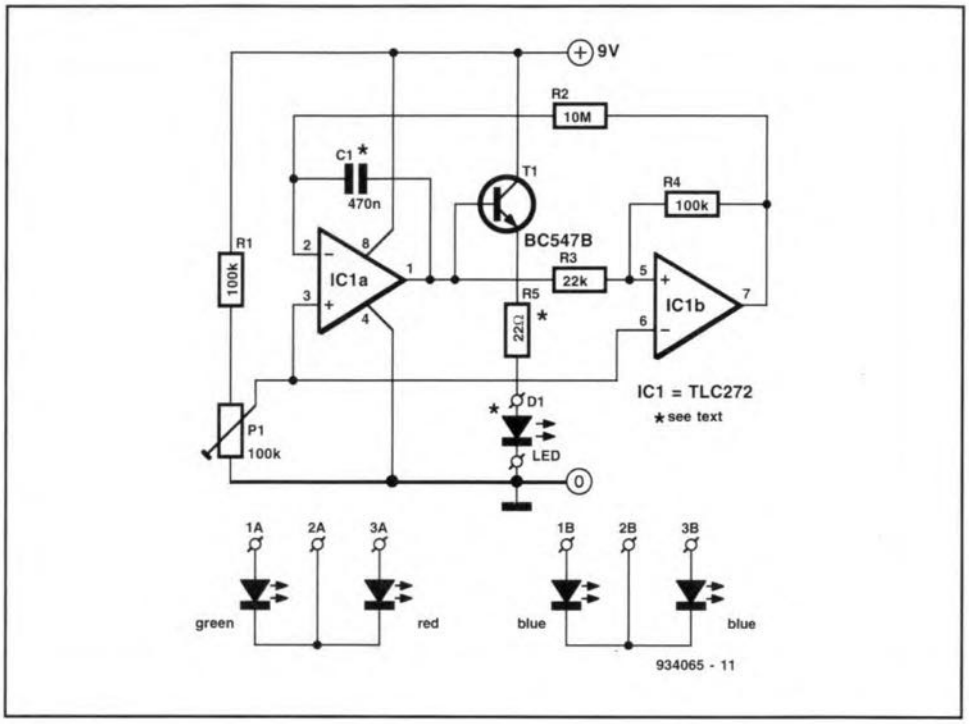
The direct voltage level of the triangular signal may be shifted with P_1. Start with the wiper at earth, and then turn the control very slowly till the LED just begins to light. The best setting is when the LED lights for two thirds of the time and is off for one third.

The value of the series resistors is low, because the sensitivity, especially of the blue LEDs, is low.

Do not turn P_1 too far, but take care that the current through the red and green LEDs remains below 30 mA; the blue ones can draw up to 40 mA. The average current drawn by the circuit is then about 70 mA.

[K. Walraven - 934065]

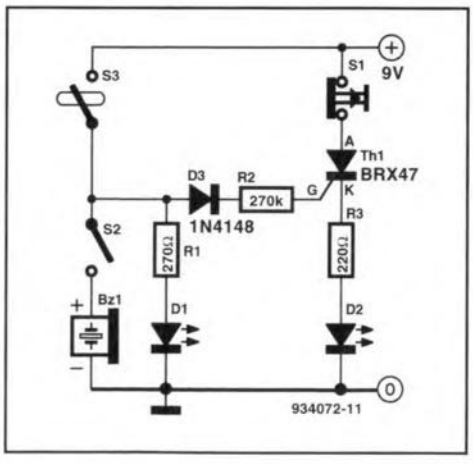




ANGLER'S BAIT INDICATOR

The indicator shows when a fish has taken the bait. Until that happy moment (at least for the angler), the bite sensor is open, so that both LEDs are out. When a fish has been hooked, the sensor closes the current loop, whereupon both LEDs light. In addition to these diodes, a buzzer may be used to give an audible signal. D_2 continues to light, even when the sensor has been reopened, for as long as the thyristor has no hold current. In this way, each tug on the hook line is indicated by D_1.

The circuit draws a current of 20–60 mA, depending on the type of LED and whether a buzzer is used.



The sensor is made from a mercury switch, cast, half a metre of stranded wire and a 3.5 mm mono jack socket. The cast is placed in the line directly under the reel. When the line is tightened, the indicator is actuated.

[F. Roth - 934072]

TELEPHONE MONITOR

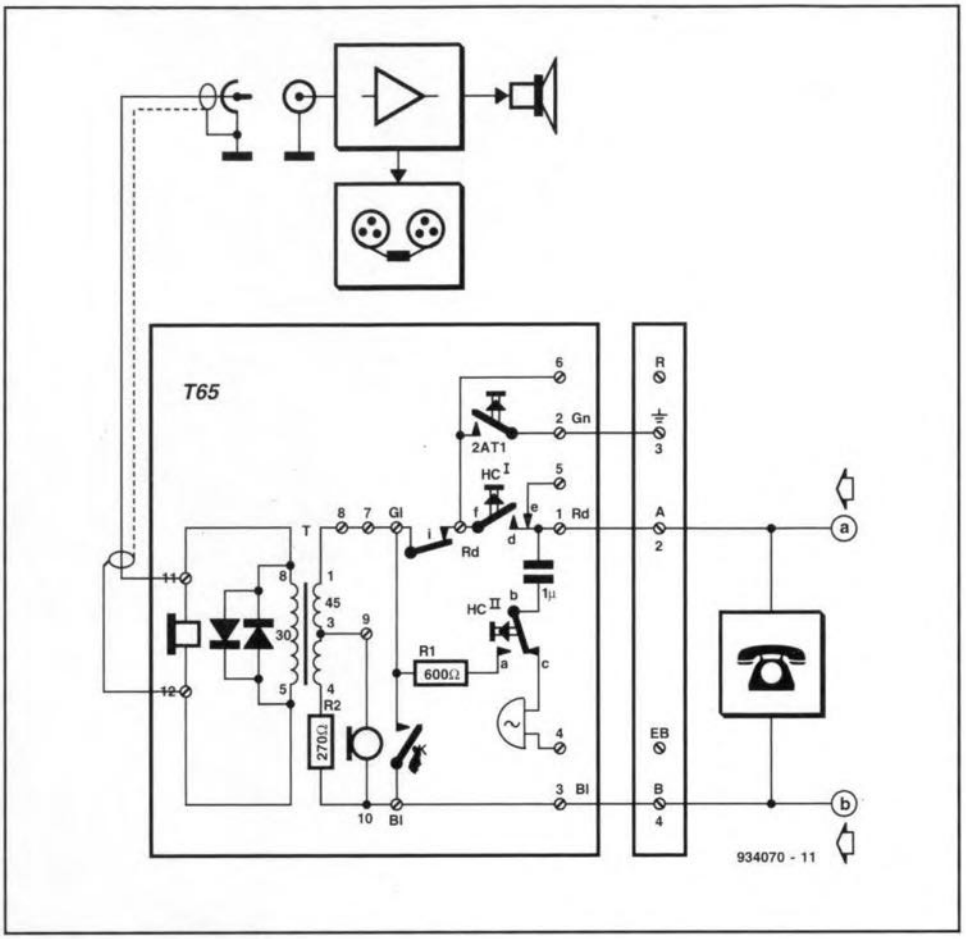
It is sometimes necessary to make a telephone conversation audible to more than one person at either end or to make a tape recording of it (as in many businesses). Often, this is done with the aid of a microphone fitted with a suction cup. This does not work very well, though, whence the present circuit.

Use an old, but still serviceable, telephone set connected across the telephone line in parallel with the receiver to be monitored. Connect a length of screened audio cable across the receiver inset and to an amplifier or tape recorder, as the case may be. As soon as a conversation has to be recorded or amplified, take the receiver from the hook and adjust the input level of the amplifier or recorder as required. Do not set the amplifier gain too high, because this may give rise to howling.

The hook contact of the additional telephone set prevents the bell voltage (50 V or more) reaching the audio equipment. Furthermore, the audio equipment is electrically isolated from the telephone line by the 1:1 telephone transformer, T.

In most west European countries it is now allowed for telephone sets to be connected in parallel, in spite of the resulting paucity of the signal quality (primarily caused by the reduced echo attenuation).

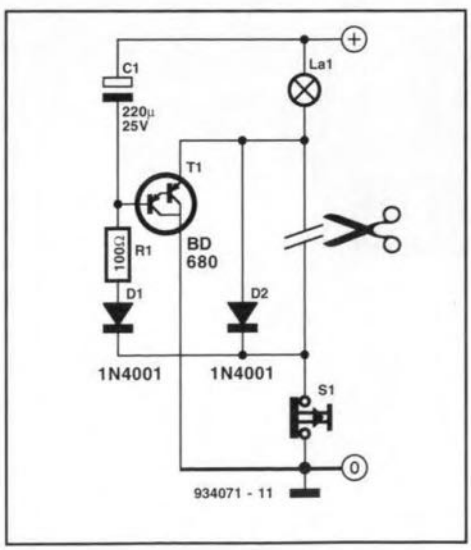
[L. Lemmens - 934070]



CAR INTERIOR LIGHT DELAY

The delay circuit ensures that a car's interior light remains on for about five seconds after all the doors have been closed. This enables the ignition lock to be found easily in the dark (many modern cars have an illuminated ignition lock as standard).

When one of the front doors of the car is opened, the door switch (here, S_1) closes. A current will then flow through interior light L_1 via S_1 and D_2. At the same time, capacitor C_1 is charged rapidly via R_1, D_1 and S_1. When the door is closed, S_1 opens. At the same instant, T_1 is switched on by the low level at the –ve terminal of C_1. After a little while, depending on the value of C_1 and the base current of T_1, the base voltage of T_1 has risen to a level where the transistor ceases to conduct, so that L_1 goes out.



[A. Rietjens - 934071]

Note. In quite a few modern cars, the circuit described (or one like it) is a standard fitting. [Editor]

LOW POWER NBFM TRANSMITTER

The transmitters is a crystal-controlled, battery-powered, one-chip narrow-band FM (NBFM) model for operation in the 27-MHz band, primarily as a wireless microphone*.

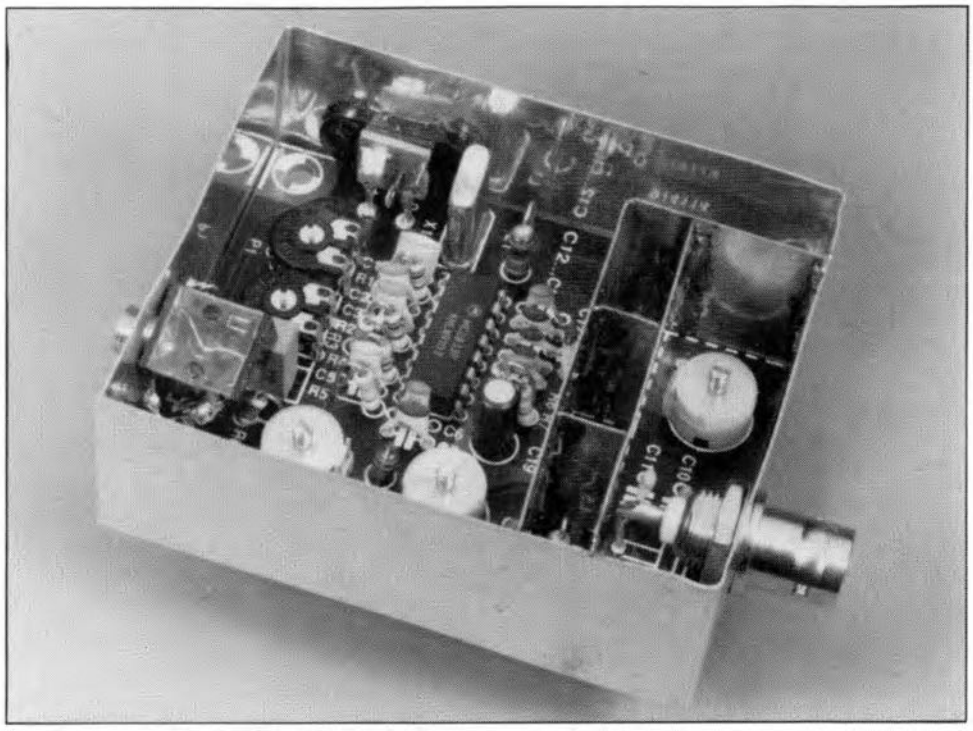
The circuit is an application of Motorola's MC2833 single-chip VHF narrowband FM transmitter IC, designed to work in the 27-MHz band. The transmitter output power is about 10 mW (+10 dBm), which, owing to the expected low efficiency of the antenna used, will result in a typical effective radiated power (ERP) of less than 1 mW. The range of the transmitter, therefore, is limited to 10–20 metres (33–66 ft).

The active circuitry contained in the MC2833 includes a microphone amplifier, a voltage controlled oscillator, and two auxiliary transistors which are used for frequency multiplication or RF amplification, depending on the desired output frequency.

Preset P_1 is used to adjust the microphone gain, and preset P_2 to adjust the deviation. Remember, the transmitter will produce NBFM only, with a maximum deviation of 5 kHz. This means that a narrow-band receiver (such as a typical 27 MHz CB unit) is required for sufficient audio output.

The quartz crystal, X_1, resonates in fundamental mode (here, 9 MHz), calibrated for parallel resonance with a 32 pF load. The final output frequency is generated by frequency multiplication (here, ×3) within the MC2833.

Construction of the transmitter follows the rules of RF design: keep all component leads as short as possible, fit the screening as indicated on the printed circuit board, and do not use an IC socket for IC_1.



The transmitter is fairly simple to adjust: simply peak the three trimmers, C_8, C_9 and C_{18}, for maximum output power delivered to a 50 Ω dummy load. Alternatively, connect the antenna and an oscilloscope to the transmitter output, and adjust the trimmers for maximum RF voltage. Next, listen to the transmitted signal on a 27 MHz receiver, and adjust the two presets until the best possible modulation is achieved. Do not set the microphone gain too high, since this will easily cause clipping.

If the transmitter is used as a wireless microphone, the antenna will typically be a piece of flexible wire with a length of about 1 m. The transmitter draws a current of about 7 mA, so it is good practice to keep an eye on the state of the battery.

(J. Barendrecht — 914114)

* This transmitter is not licensable as a wireless microphone in the UK.

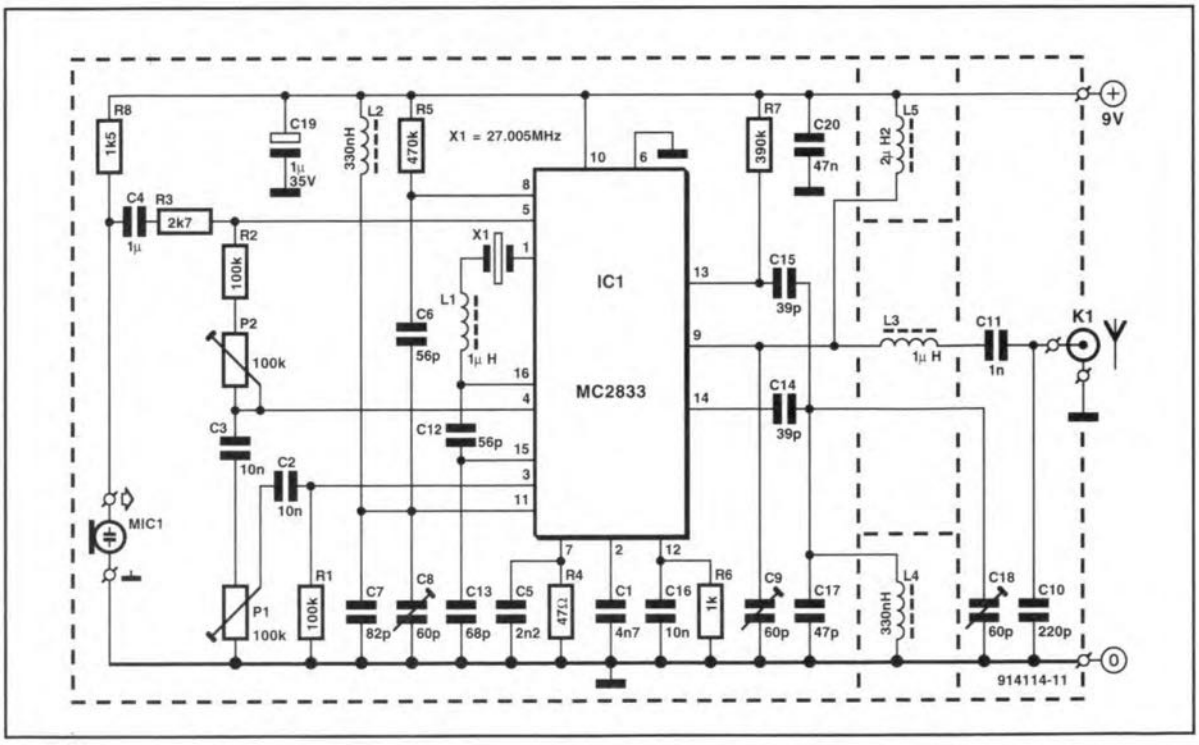


Fig. 1. Circuit diagram of the NBFM transmitter.

PARTS LIST

Resistors:
R_1, R_2 = 100 kΩ
R_3 = 2.7 kΩ
R_4 = 47 Ω
R_5 = 470 kΩ
R_6 = 1 kΩ
R_7 = 390 kΩ
R_8 = 1.5 kΩ
P_1, P_2 = 100 kΩ preset, H

Capacitors:
All fixed capacitors are ceramic, unless otherwise indicated
C_1 = 4.7 nF
C_2, C_3, C_{16} = 10 nF
C_4 = 1 µF MKT
C_5 = 2.2 nF
C_6, C_{12} = 56 pF
C_7 = 82 pF
C_8, C_9, C_{18} = 60 pF foil trimmer
C_{10} = 220 pF
C_{11} = 1 nF
C_{14}, C_{15} = 39 pF
C_{17} = 47 pF
C_{19} = 1 µF, tantalum
C_{20} = 47 nF

Inductors:
L_1, L_2 = 1 µH
L_3, L_4 = 330 nH
L_5 = 2.2 µH

Integrated circuits:
IC_1 = MC2833P (Motorola)

Miscellaneous:
K_1 = BNC socket
X_1 = crystal, 27.005 MHz
MIC_1 = Electret microphone

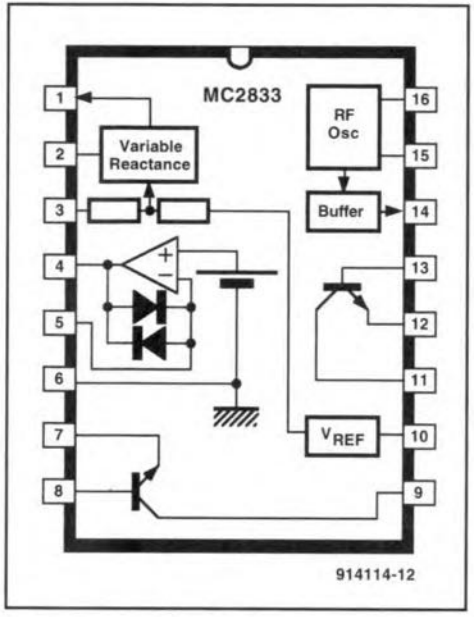


Fig. 2. Block diagram of the MC2833P

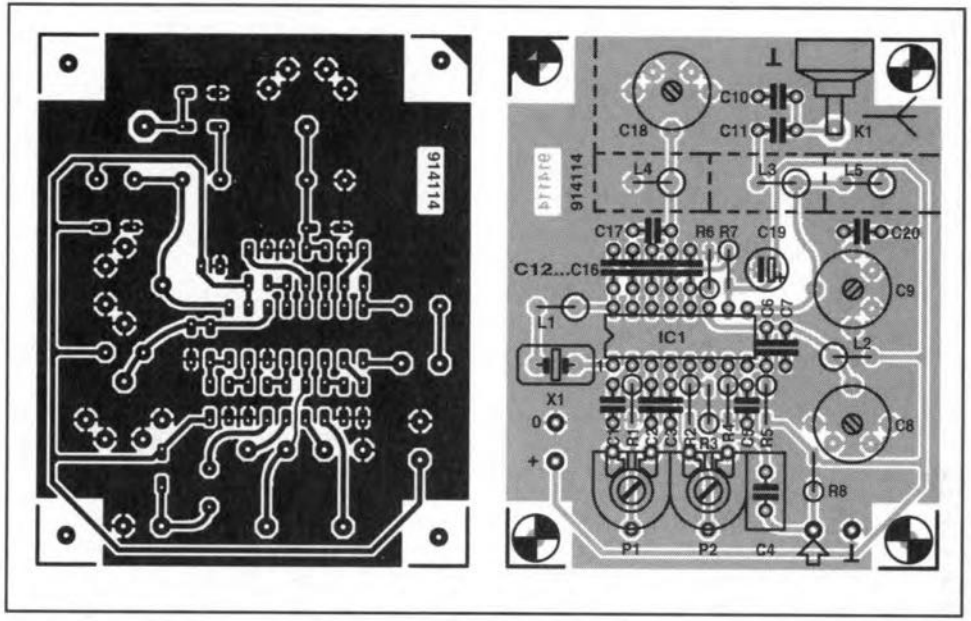


Fig. 3. The printed circuit for the NBFM transmitter (not available ready made).

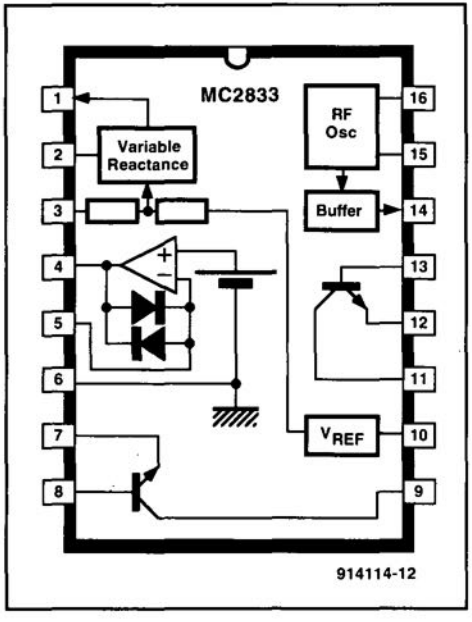


Fig. 2. Block diagram of the MC2833P

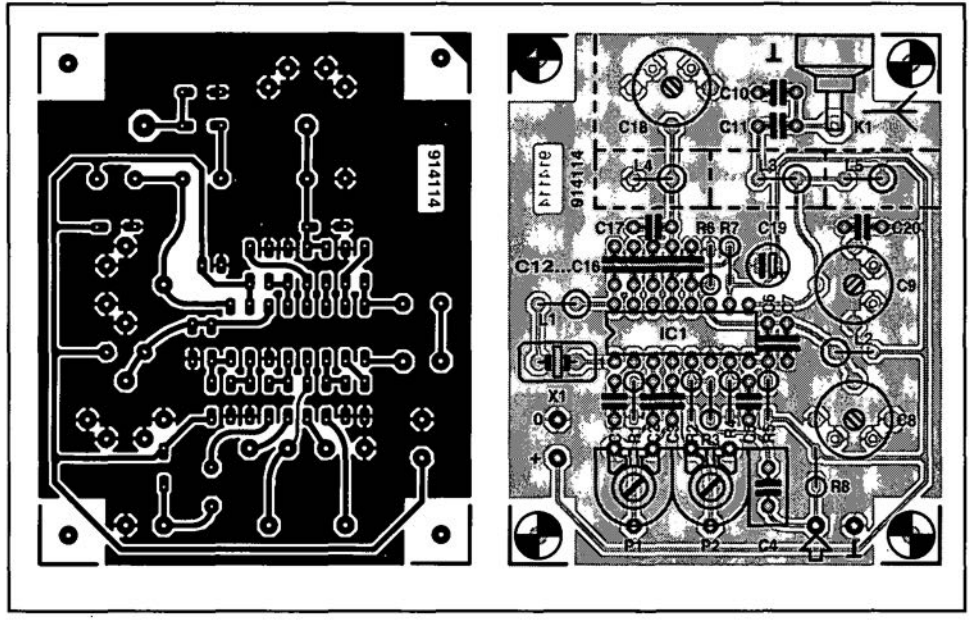
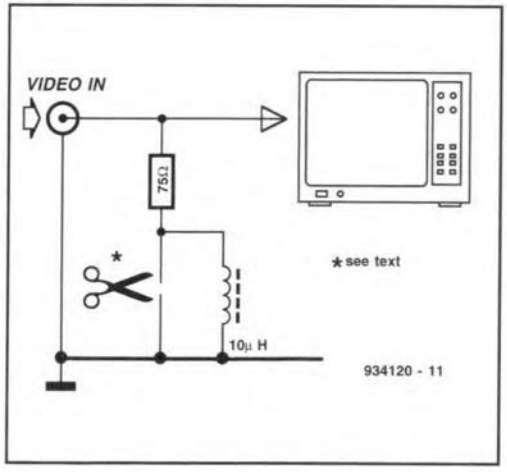


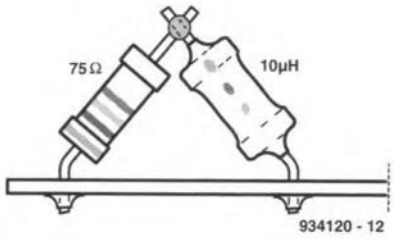
Fig. 3. The printed circuit for the NBFM transmitter (not available ready made).

INEXPENSIVE VIDEO ENHANCER

Often, a video signal applied to the TV receiver via the SCART or AV input appears rather less well-defined than a signal applied directly from the antenna socket. A considerable improvement may be ontained by connecting an inductor of about 10 µH in series with the input resistor of the SCART or AV socket (this resistor is normally 75 Ω or 82 Ω). The inductor raises the input impedance at higher frequencies, so that these are attenuated less than the lower frequencies. The improvement is particularly noticeable with signals of limited bandwidth (such as from a video cassette recorder): the picture is sharper and the colours are fuller.

[J. Bodewes - 934120]





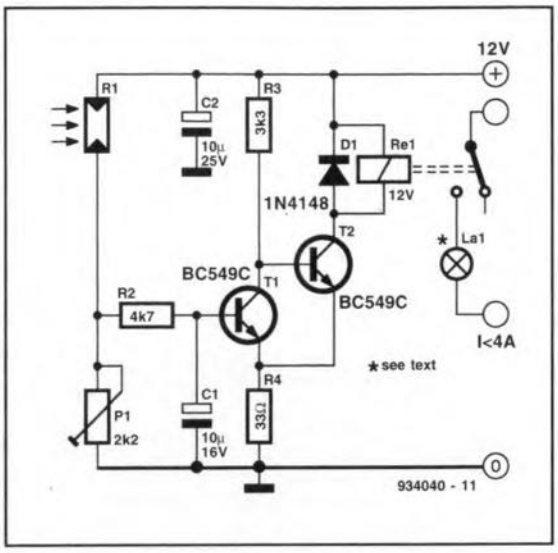
AUTOMATIC TWILIGHT SWITCH

This is one of the simplest twilight switches ever published in this magazine. When it gets dark, the value of light-sensitive resistor R_1 increases, whereupon T_1 switches off. Transistor T_2 then switches on and this energizes relay Re_1. At the same time a voltage drop of about 1 V develops across R_4: this is the hysteresis of the switch.

Capacitor C_1 serves to make the switch insensitive to brief changes in ambient darkness, such as caused by a passing car with its headlights blazing.

The only requirement on the transistors is high current amplification, which means the use of C types.

The varistor is a new type (Piher) that is environment-friendly (since it contains no cadmium) and very small: about twice the size of the head of a match. If another type is used, its day-light resistance should be of the order of a few hundred ohms; this should increase to about 10 kΩ at twilight. In any case, the value of P_1 may be increased (within reason).



During calibration, unsolder C_1 from earth: the circuit then reacts faster.

The relay should be a 12 V type that needs an energizing current ≤50 mA.; its contact should be able to switch 8 A. The load current, however, should not exceed 4 A. When they are switched on, most lamps, and certainly halogen types, draw a very large current. Keeping the load current down ensures a long life of the relay contacts.

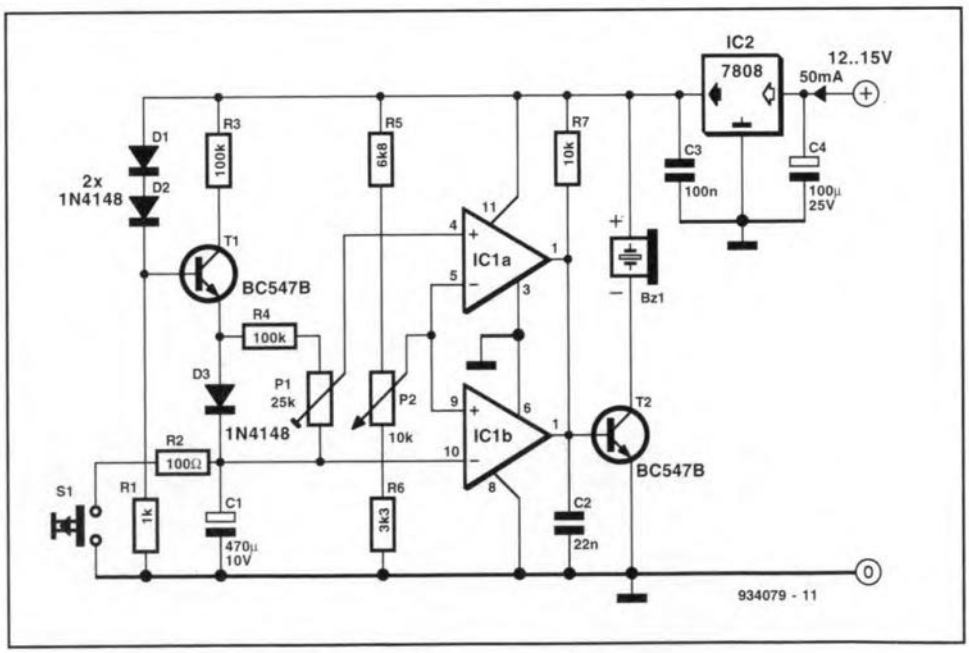
The circuit draws a current of not more than 5 mA plus the relay current.

[K. Walraven - 934040]

BASIC TIMER (I)

The time-determining element in the present circuit is capacitor C_1, which is charged via a current source based on T_1. The voltage across the capacitor is, therefore, a ramp. A comparison of this ramp with a preset voltage gives a fairly accurate time indication. With values shown in the present circuit, that time lies between 1 and 10 minutes.

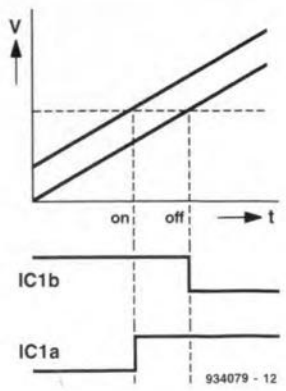
The ramp and reference voltage are compared by IC_{1a} and IC_{1b}, both open-collector output types. Ignoring IC_{1a} for a moment, the output transistor of IC_{1b} will be off as long as the set voltage is higher than the potential across C_1. If that potential becomes higher than the reference voltage, the output transistor in IC_{1b} switches on and T_2 goes off. In practice, this would mean that the buzzer sounds until the set voltage level is exceeded: not exactly ideal. Since the intention is that the buzzer sounds only briefly when the set level is exceeded, IC_{1a} is needed. This comparator evaluates the reference voltage with a potential that is slightly higher than that across C_1. This off-set is provided by R_4-P_1-D_3. The result is that IC_{1a} reacts in a different way from IC_{1b}: the output transistor in IC_{1a} is on when the potential across C_1 plus that at the wiper of P_1 is lower than the reference voltage, and is switched off when the reference voltage is exceeded. Thus, this comparator starts the buzzer sounding for an infinitely long period just before the set time has elapsed.



Summing up the action: one output actuates the buzzer after a certain period of time has elapsed, while the other output switches the buzzer off again after a slightly longer period of time has elapsed. Thus, the buzzer sounds only during the short overlap of these two periods. The length of this overlap is set with P_1. The time period before the buzzer is actuated is set with P_2.

The timer is started when S_1 is pressed.

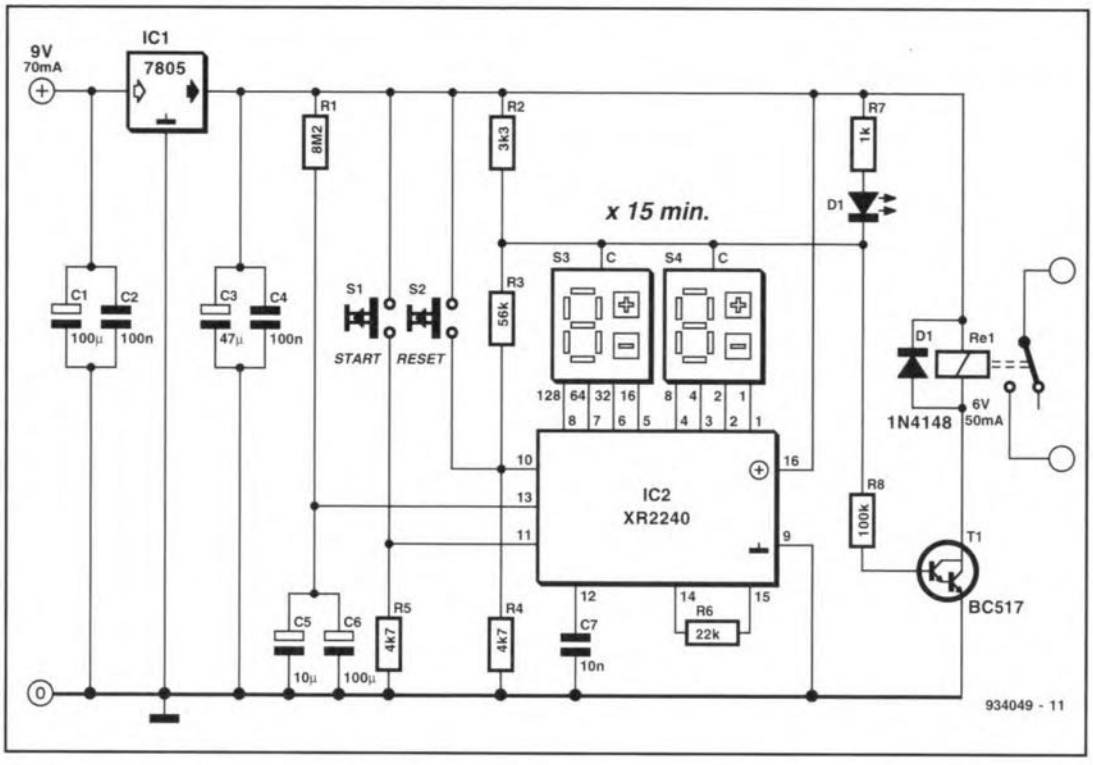
[A. Rietjens - 934079]



LONG-DURATION TIMER

The timer, based on EXAR's Type XR2240, is intended for use in photographic and printed-circuit departments, as a standby switch for TV and radio equipment, as a battery charging monitor, and similar applications. The timing can be set between 15 minutes and 24 hours 45 minutes with two BCD (binary coded decimal) switches.

The timing is programmed in steps, *T*, which are determined by the time constant $R_1 (C_5 + C_6) = 15$ minutes. The BCD switches allow up to 255 such periods to be selected. The timer functions are controlled by an internal bistable (flip-flop) and switches S_1 and S_2. To keep the period accurate, C_5 and C_6 must be carefully selected.



Diode D_1 lights when the timer is switched on. The voltage at junction D_1-R_2-R_3-R_8 is then so low that T_1 remains off. When the set time has elapsed, pin 10 of IC_2 becomes logic high, whereupon the supply voltage exists at the junction. The LED then goes out, T_1 conducts and relay Re_1 is energized, so that its contact changes over.

The supply voltage to the timer is stabilized by regulator IC_1. Capacitors C_1–C_4 smooth the supply voltage to prevent the timer being triggered by pulses on this voltage.

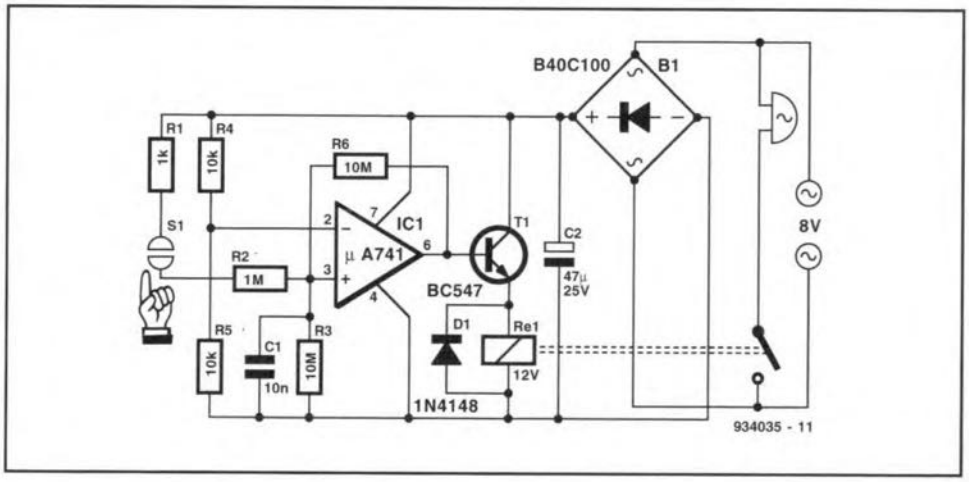
[G. Geißler - 934049]

ELECTRONIC BELL-PUSH

A solid-state bell-push is far more robust than the usual mechanical type. The touch contact may be made from an audio socket, which has a high insulation resistance and is practically indestructible.

The inverting (–) input of IC_1 is at half the supply voltage via R_4-R_5, while the non-inverting input is at earth potential via R_3. When the contact is touched (less than 10 MΩ, a light touch is fine), the output of the opamp goes high and the relay (a 9-V or 12-V type) is energized. The relay contact then actuates the (existing) bell. Resistor R_1 and capacitor C_1 ensure that the bell cannot be actuated accidentally.

The circuit is powered by the rectified bell transformer voltage (or a second bell transformer – for safety's sake, do not use a different type of transformer). A bell transformer can normally provide a current of 1 A, so the first solution is almost always possible.



The circuit draws a (quiescent) current of only 5 mA if a 741 is used and only 0.5 mA if a TLC271 is used. When the relay is energized, this rises by 30 mA.

[J. Bosman - 934035]

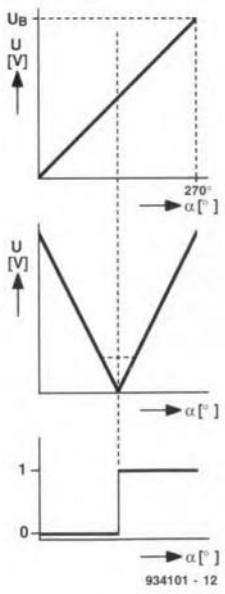
PCB DRILL CONTROL

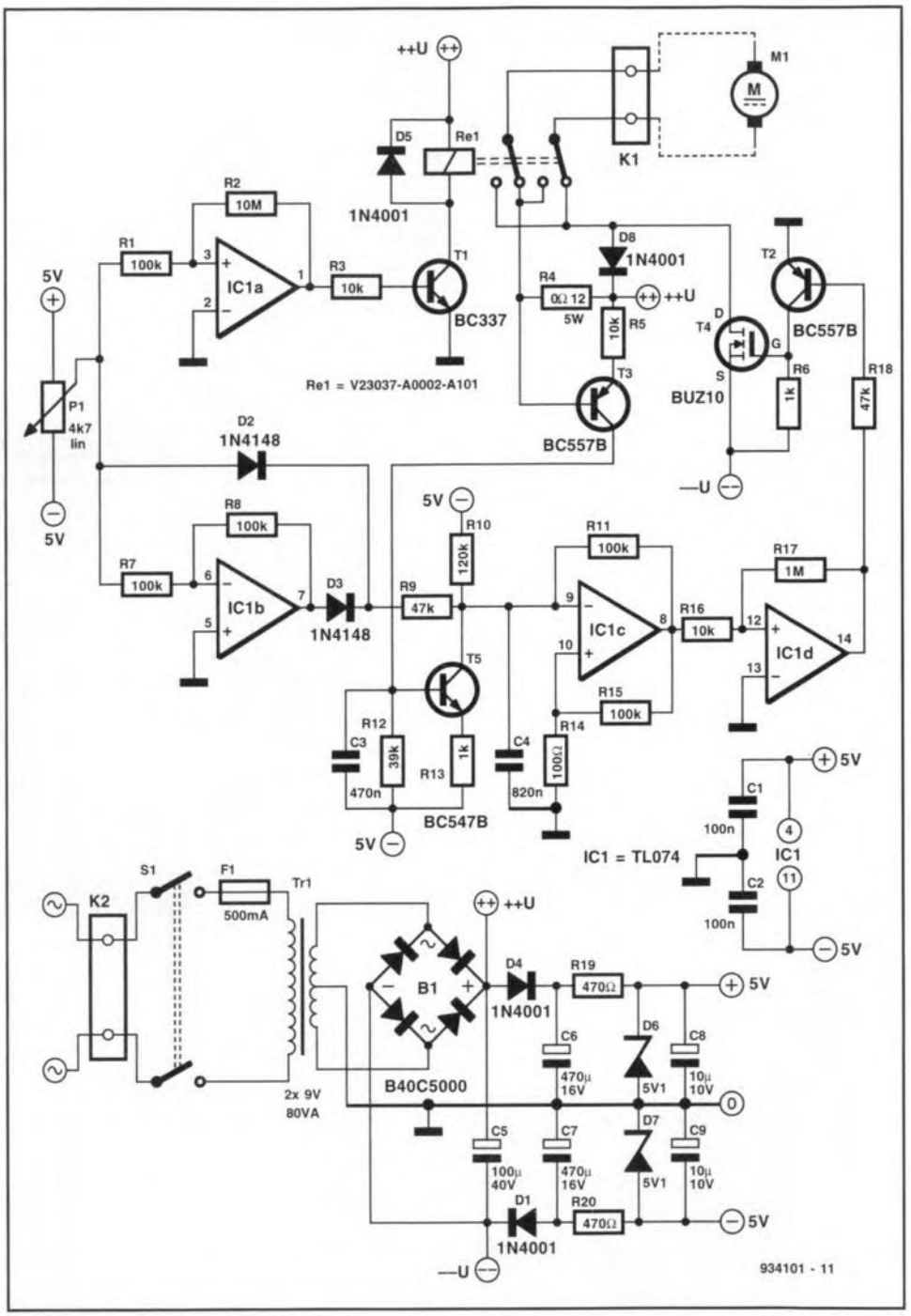
The circuit in the diagram enables the speed of an electric PCB drill to be controlled with only one preset. As an aside, the rotary direction of the drill may be reversed. When the preset is at the centre of its travel, the drill stops.

The power supply delivers (immediately after the bridge rectifier) a voltage of about 12 V for the drill, and, by means of resistors R_{19} and R_{20},and zener diodes D_6 and D_7, a symmetrical voltage of ±5 V for the electronic circuits. The ±5 V voltage is smoothed by C_6 and C_7. Diodes D_4 and D_5 prevent the motor of the drill being connected to the ±5 V section.

Speed control is effected with P_1, while rotary direction is determined by comparator IC_{1a}. This opamp ascertains whether the preset is to the left or to the right of its centre. On the basis of this, relay Re_1 is energized via T_1 or not, and this decides whether the drill turns clockwise or anti-clockwise.

The speed control operates with pulse width modulation. The control (direct)





voltage set with P_1 is applied to D_2 and IC_{1b}-D_3. This latter combination functions as a rectifier. Whether the voltage at the wiper of P_1 is negative or positive, it will appear as a positive potential (minus the 0.6 V forward bias of the diode) at the junction of D_2 and D_3.

The modulator is formed by IC_{1c}. This stage is designed as a rectangular-wave generator, which causes C_4 to be charged and discharged continuously via R_{11}. The setting of P_1 determines (via R_9) in conjunction with R_{10} how much additional direct voltage is applied to C_4, and thus the pulse/spacing ratio at the output of IC_1. Inverter IC_{1d} enhances the transitions (edges) of the signal, which are thereupon used to switch the power FET (T_4) via T_1.

When the drop across R_4, which is in series with the drill motor, rises to slightly more than 0.6 V (that is, when the current through the motor is about 5 A), T_3 will switch on, whereupon T_5 will reduce the pulse width slightly.

[H. Bonekamp - 934101]

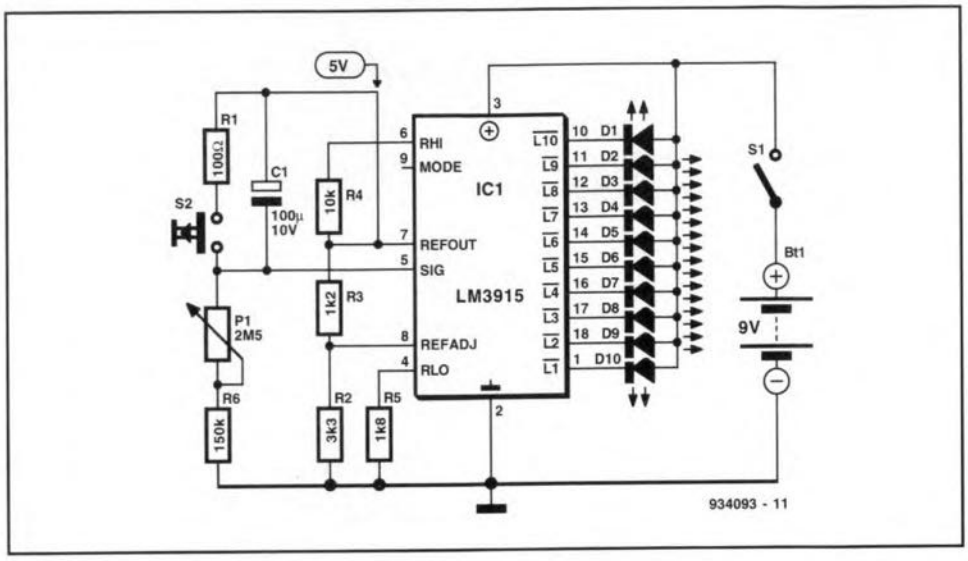
BASIC TIMER (II)

The timer is based on the well-known display driver LM3915, which has a logarithmic scale. This may seem strange, but is not because a simple *RC* network is used for time measurements. The voltage across this network, R_6-P_1-C_1, has, while C_1 is being charged, an exponential character ($U = U_{ref} \cdot e^{-t/RC}$). When this is applied to IC_1, which takes its logarithm, the time is shown linearly on the display. The values of P_1 and R_6 have been chosen to enable the timer showing periods of 1–15 minutes.

The timer is reset (C_1 is discharged) when S_2 is closed. Resistor R_1 limits the peak value of the discharge current from C_1 to an acceptable value for the switch contacts.

Resistor R_5 compensates the leakage currents of the electrolytic capacitors to obviate the risk of D_{10} going out.

If pin 9 of IC_1 is left open, the display is in the dot mode. The elapsing of time is then shown by only one LED lighting. After a reset, D_1 will light first and then, sequentially, all the other LEDs.



The total current drawn by the timer is 20 mA, so that battery supply is possible.

When pin 9 is connected to pin 3 (+ve supply line), the display is in the bar mode. After a reset, all LEDs will light and then go out in turn, starting with D_1. In this mode, battery supply is not recommended.

[H. Bonenkamp - 934093]

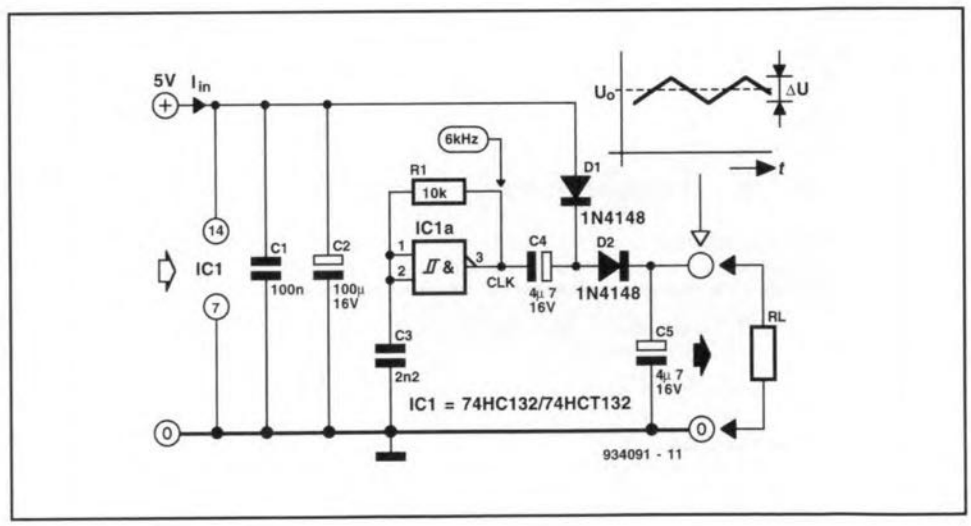
INEXPENSIVE VOLTAGE DOUBLER

Voltage doublers are frequently encountered in electronic circuits. The present one is a variation that is of interest since most digital circuits already have a buffered clock (CLK) available or have a spare Schmitt trigger gate. Since in those cases no new IC is needed, the cost of the doubler is much reduced.

If a buffered CLK signal is available, only four components, C_4, C_5, D_1 and D_2, are required to produce a voltage of 10 V from the 5 V supply. If an oscillator needs to be built from a spare gate, two further components are needed: R_1 and C_3.

The most important parameters of the circuit are given in the table. Note that, owing to tolerances in the clock circuit, these data may be slightly different.

[J. Ruiters - 934091]



R_L [Ω]	U_0 [V]	ΔU [mV_{pp}]	I_{in} [mA]	n [%]
--	9.4	0	2.4	--
2200	8.0	15	20.0	29
780	7.0	40	28.3	45
460	6.0	80	37.6	41

SYMMETRICAL POWER SUPPLY

A symmetrical power supply may be designed from two standard opamps, but it can only provide a small current (of the order of a few mA).

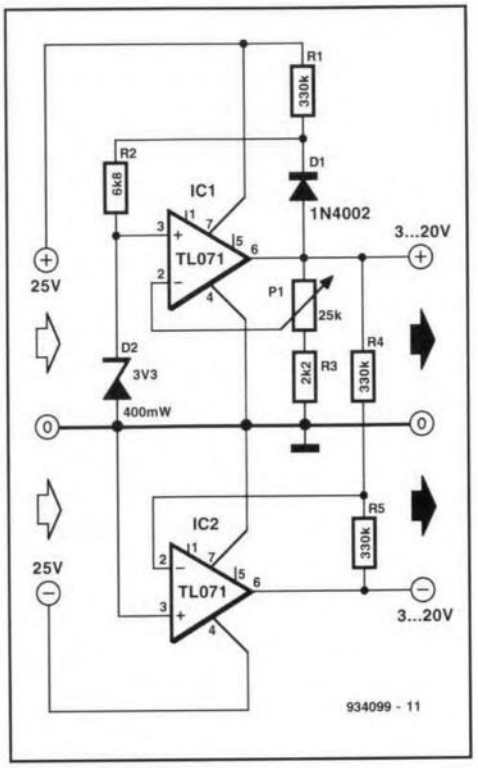
In the diagram, the upper half provides the positive voltage. A 3.3 v zener diode, connected to the non-inverting (+) input of opamp IC_1, serves as reference. To ensure correct starting of the circuit, the diode is initially powered via R_1 and when the output voltage is sufficiently high via D_1. Part of the output voltage is fed back to the inverting (–) input of IC_1 via P_1. The lower the feedback voltage, the higher the output.

The supply voltage for the TL071 may be 36 V maximum, so that the output voltage can go up to about 30 V. It is, however, safer to make the supply to the opamp rather lower and accept a slightly lower output voltage.

The lower part of the diagram is a mirror of the upper part: it provides the negative output. Opamp IC_2 needs an additional (negative) supply voltage.

The output voltages may be made more stable by connecting a 10 µF electrolytic capacitor across each of the outputs.

[Amrit Bir Tiwana - 934099]



VIDEO DATA CHANGE DETECTOR

The circuit detects a change in video information and uses this to switch on an alarm in a closed-circuit television guard system or a video recorder.

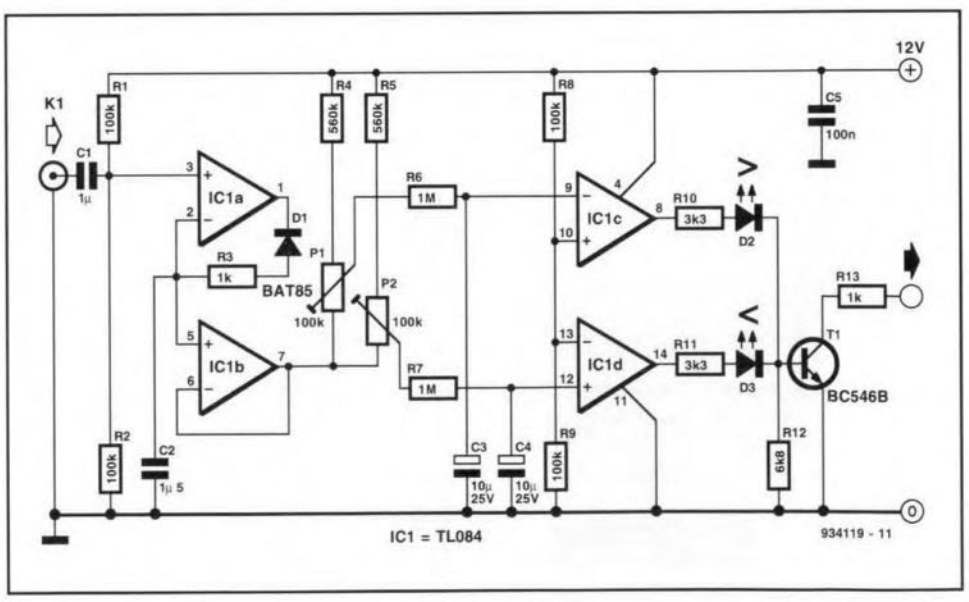
The circuit is usable only where the same picture is shown on the TV monitor for some time. When the picture changes, the average brightness alters and this is detected by a window comparator.

Capacitor C_1 prevents any d.c. component in the video signal reaching the circuit. Opamp IC_{1a} clamps the signal. On average, the potential at pin 3 of IC_{1a} is always equal to half the supply voltage.

The potential across C_2 is buffered by IC_{1b}. The output signal of this opamp is applied to window comparator IC_{1c}-IC_{1d} via presets P_1 and P_2.

The reference voltage for the comparator is held at half the supply voltage ($^1/_2\ U_b$) by R_8-R_9. Preset P_1 is adjusted to make the potential at its wiper slightly higher than $^1/_2\ U_b$, and P_2 to make its wiper voltage slightly lower than $^1/_2\ U_b$. The potentials at the wipers of P_1 and P_2 are applied to the comparator via fairly long (>10 s) time constants (R_6-C_3 and R_7-C_4). The smaller the set window, the faster the reactor will change state.

When the level of the input signal rises, the potential across C_2 decreases, whereupon the levels across P_1 and P_2 also drop. When the voltage at pin 9 of IC_{1c} drops below $^1/_2\ U_b$, the output of this stage goes high. This change of state, indicated by the lighting of D_2, is used to give an external apparatus a trigger or start pulse of up to 65 V via the open collector output of T_1. Resistor R_{13} serves as a current limiter.



When the level of the input signal decreases, a similar action follows, but in this case IC_{1d} changes state, which is indicated by the lighting of D_3.

When there is no change in the average input signal, T_1 remains off.

The circuit draws a current of about 12 mA.

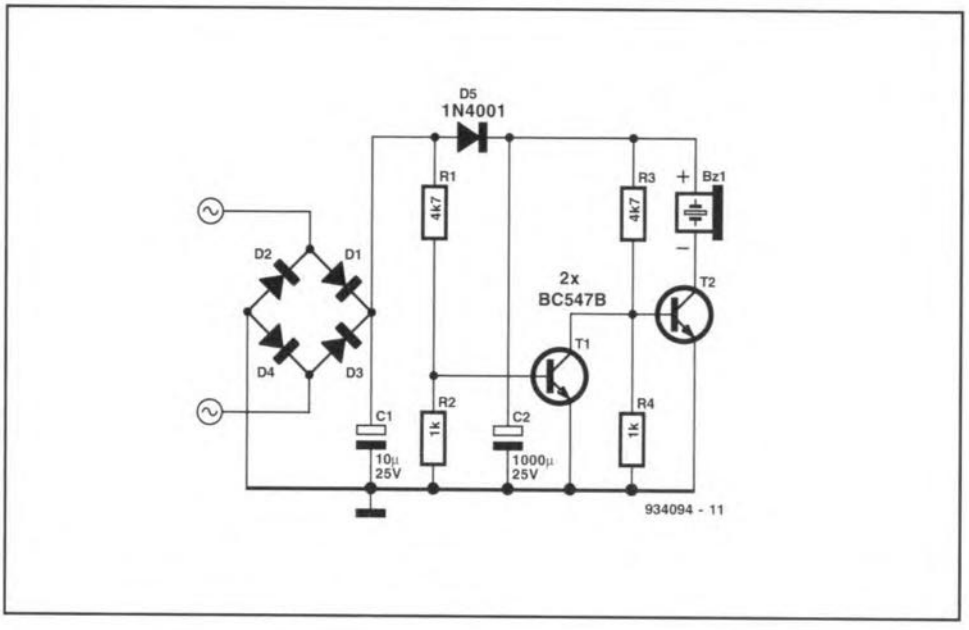
[T. Giesberts - 934119)

COMPLEMENTARY DOORBELL

It is often not possible to put a second bell in parallel to the existing one, because the bell transformer is normally already fully loaded. The circuit proposed here offers a solution to this problem.

The buzzer sounds **after** the bell-push has been released, The energy for this is stored in capacitor C_2 while the bell-push is pressed. This causes only a small (and brief) additional load on the bell transformer. At the same time, T_1 ensures that T_2 is off. When the bell-push is released, T_1 is switched off and T_2 begins to conduct. As long as the charge on C_2 lasts, the buzzer will sound. The length of the sound depends on the value of C_2 (the higher the value, the longer the sound). Since all the energy is supplied by C_2, the buzzer cannot be replaced by a normal bell or gong, since these draw far too large a current.

[A. Rietjens - 934094]



STORAGE OSCILLOSCOPE TESTER

The tester generates two different signals for checking a digital storage oscilloscope. The first is a stepped voltage on to which glitches are superimposed; the second is a rectangular 2 kHz signal on to which a 15 Hz analogue signal is superimposed.

The first signal quickly shows whether the oscilloscope eliminates the glitches during signal processing. If it does, the measurements cannot be fully trusted. It can also be used to check the trigger function; if this is poor, it will not be able to cope with the signal properly.

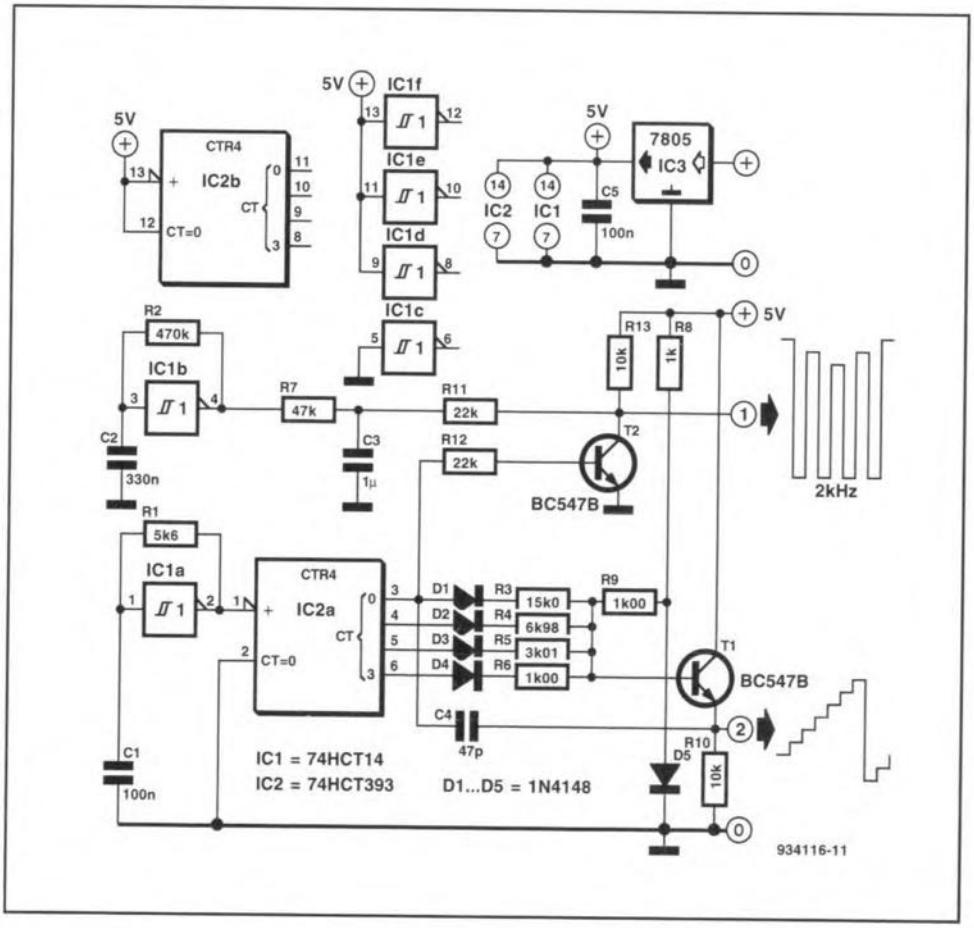
The second signal shows whether at a given setting low-frequency signals remain clearly visible (they should).

The stepped voltage is generated by oscillator IC_{1a} and a digital-to-analogue converter (DAC)—see diagram. The converter consists of IC_2, D_1–D_4, R_3–R_6, and R_9. The signal is buffered by T_1. Diode D_5 compensates the forward bias of the base-emitter junction of T_1. The spikes are introduced by C_4.

The second signal is produced by switching T_2 in rhythm with the 2 kHz signal and changing the collector voltage with the 15 Hz signal generated by oscillator IC_{1b}.

The circuit needs a supply voltage of 9–15 V and draws a current of about 50 mA.

[A. Rietjens - 934116]



HEXADECIMAL DISPLAY DECODER

The byte-to-hex display decoder was designed because nibble-to-hex decoders are no longer produced commercially. In principle, it is of, course, not difficult to decode a nibble, but from byte to hex is generally more practical and requires fewer ICs. The decoder uses a GAL Type 22V10. This type has an adequate number of inputs and outputs for the present application and may be programmed with the 'GAL programmer' (incl. the extension) published in this magazine[1]. The listing and programming data shown are written in the format that is accepted by the National Semiconductor software and may be converted to a JEDDIC file with the EQN2JED option. Note that although a warning is generated that in the define statements an OR term is used, this is a false alarm, since in the present circuit no fewer than eight OR terms are produced.

The circuit has a drawback in that it requires an external clock. Fortunately, this signal can often be derived from the circuit to which the display is connected. The frequency may be between 100 Hz and 100 kHz.

Apart from clocking the bistables at the outputs of the GAL, the clock also serves the multiplexing of the two displays.

Schottky diodes D_1 and D_2 ensure that T_1 and T_2 switch off fast, so that the transistors are on in turn without any overlap. This prevents 'ghost' segments arising at clock frequencies above 1 kHz.

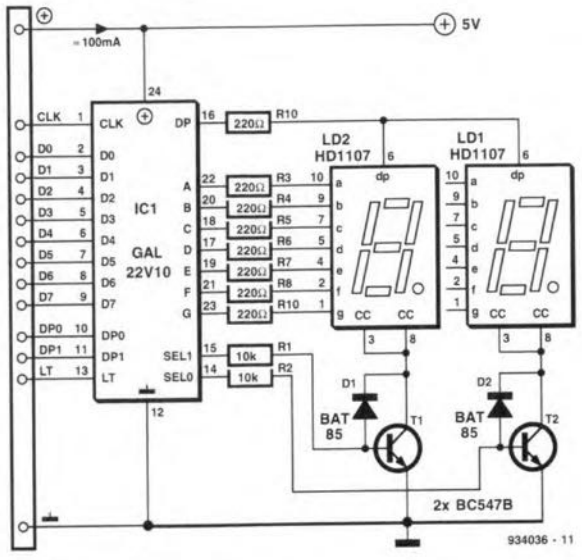
LT is a lamp-test input with which all segments are controlled. A '1' at input DP0 or DP1 causes the relevant decimal point on the displays to light.

The decoder may serve as an example for the design of a special decoder for another application.

[A. Rietjens – 934036]

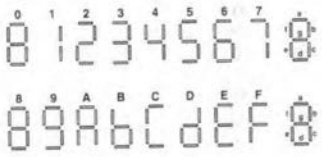
[1] May 1992.

1



2

```
        Hex Decoder / 7-Segment LED Driver
        GAL file for OPAL Junior

CHIP hex_7seg gal22v10

clk d0   d1   d2 d3 d4 d5 d6 d7 dp0 dp1 gnd
lt  sel0 sel1 dp d  c  e  b  f  a   g   vcc

;define product terms for each value and each display

        @define zero      "/d7*/d6*/d5*/d4*/lt*sel0+/d3*/d2*/d1*/d0*/lt*sel1"
        @define one       "/d7*/d6*/d5* d4*/lt*sel0+/d3*/d2*/d1* d0*/lt*sel1"
        @define two       "/d7*/d6* d5*/d4*/lt*sel0+/d3*/d2* d1*/d0*/lt*sel1"
        @define three     "/d7*/d6* d5* d4*/lt*sel0+/d3*/d2* d1* d0*/lt*sel1"
        @define four      "/d7* d6*/d5*/d4*/lt*sel0+/d3* d2*/d1*/d0*/lt*sel1"
        @define five      "/d7* d6*/d5* d4*/lt*sel0+/d3* d2*/d1* d0*/lt*sel1"
        @define six       "/d7* d6* d5*/d4*/lt*sel0+/d3* d2* d1*/d0*/lt*sel1"
        @define seven     "/d7* d6* d5* d4*/lt*sel0+/d3* d2* d1* d0*/lt*sel1"
        @define eight     " d7*/d6*/d5*/d4*/lt*sel0+ d3*/d2*/d1*/d0*/lt*sel1"
        @define nine      " d7*/d6*/d5* d4*/lt*sel0+ d3*/d2*/d1* d0*/lt*sel1"
        @define ten       " d7*/d6* d5*/d4*/lt*sel0+ d3*/d2* d1*/d0*/lt*sel1"
        @define eleven    " d7*/d6* d5* d4*/lt*sel0+ d3*/d2* d1* d0*/lt*sel1"
        @define twelve    " d7* d6*/d5*/d4*/lt*sel0+ d3* d2*/d1*/d0*/lt*sel1"
        @define thirteen  " d7* d6*/d5* d4*/lt*sel0+ d3* d2*/d1* d0*/lt*sel1"
        @define fourteen  " d7* d6* d5*/d4*/lt*sel0+ d3* d2* d1*/d0*/lt*sel1"
        @define fifteen   " d7* d6* d5* d4*/lt*sel0+ d3* d2* d1* d0*/lt*sel1"

;define combined productterms to minimize the total number of terms

        @define or14or15 " d7* d6* d5*/lt*sel0+ d3* d2* d1*/lt*sel1"
        @define or11or15 " d7* d5* d4*/lt*sel0+ d3* d1* d0*/lt*sel1"
        @define or12or14 " d7* d6*/d4*/lt*sel0+ d3* d2*/d0*/lt*sel1"
        @define or2or3    "/d7*/d6* d5*/lt*sel0+/d3*/d2* d1*/lt*sel1"
        @define or4or5    "/d7* d6*/d5*/lt*sel0+/d3* d2*/d1*/lt*sel1"
        @define or7or15   " d6* d5* d4*/lt*sel0+ d2* d1* d0*/lt*sel1"
        @define or1or9    "/d6*/d5* d4*/lt*sel0+/d2*/d1* d0*/lt*sel1"
```




```
        EQUATIONS

;To minimize product terms the segment selection is done by using
;the one's that are off, and several options, like 'one+nine', are combined
;into one product term, resulting in one term 'or1or9'.
;All outputs are registered and the multiplex frequency is determined by
;the supllied clock frequency

/a:= one    + four   + eleven   + thirteen
/b:= five   + six    + or11or15 + or12or14
/c:= two    + twelve + or14or15
/d:= four   + one    + ten      + or7or15
/e:= or1or9 + three  + or4or5   + seven
/f:= one    + or2or3 + seven    + thirteen
/g:= zero   + one    + seven    + twelve

sel0 := sel1
sel1 := /sel1

dp:= dp0*sel1 + dp1*sel0
```

934036 - 12

8-CHANNEL A-D CONVERTER

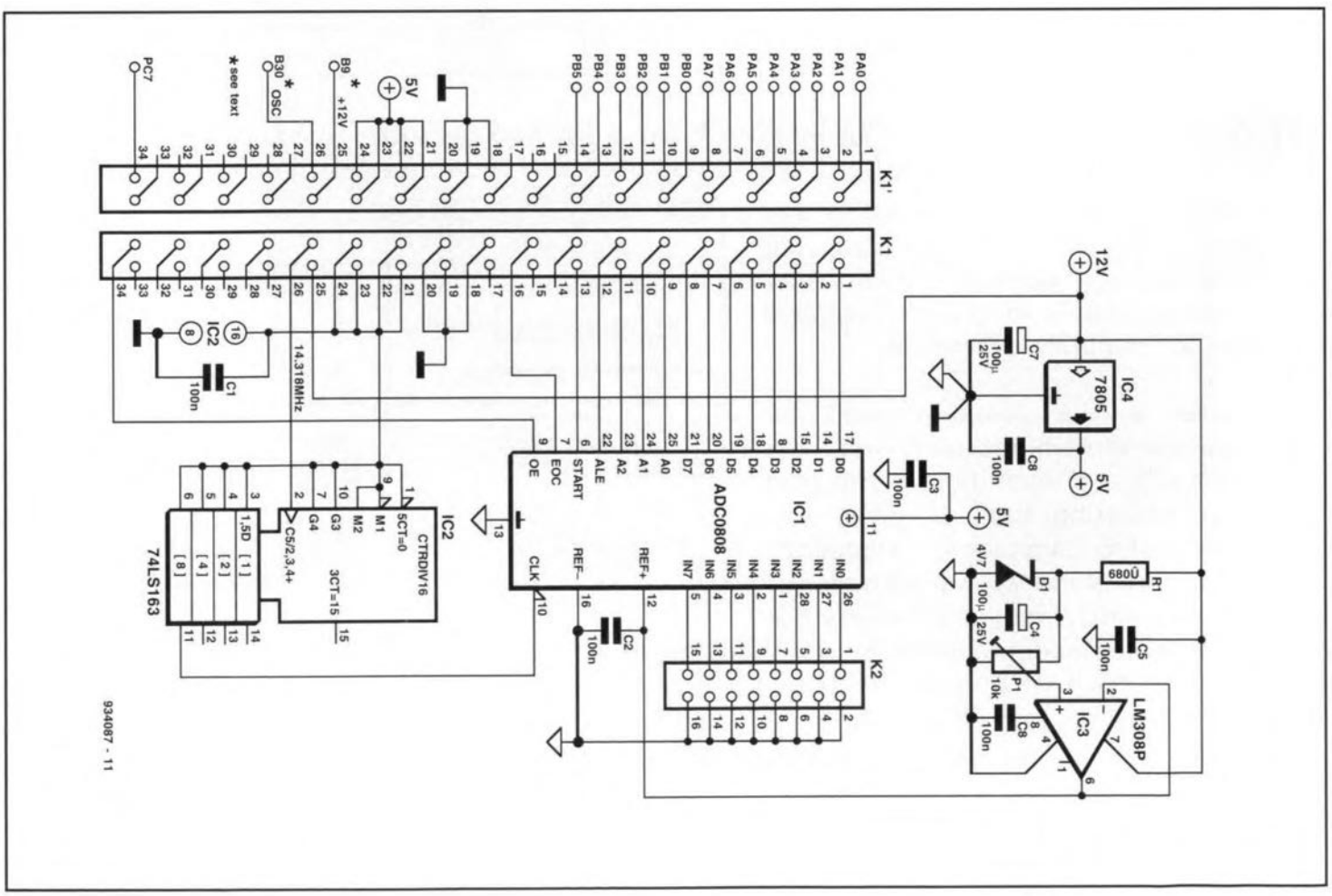
The converter described is controlled by a small I/O card that has an adequate number of inputs and outputs. It may be built on small piece of prototyping board and connected to the I/O board via K_1. The 12 V supply and the clock (OSC = 14.318 MHz) which, divided by 16, is used to clock the converter, are derived from the I/O card. The clock may also be drived from a PC, but that on the I/O card is independent of the computer.

How the converter is operated is shown in the BASIC program, except for one action. The EOC output (which goes high at the end of a conversion) needs a minimum of 0 clock pulses and a maximum of eight clock pulses plus 2 µs after the leading transition (edge) of the start pulse to go low. This means that with compiled software or machine language routines EOC must be checked in the correct manner (that is looking on line 200 whether EOC is high).

[S. Mitra - 934087]

```
10 CLS
20 CTRLWRD = &H99:      'Port A is input, B is output, C is input
30 BASEADDR = &H300:    'base address of 8255
40 PORTA = BASEADDR
50 PORTB = BASEADDR + 1
60 PORTC = BASEADDR + 2
70 CTRLADDR = BASEADDR + 3
80 CHANNEL = 0
90 '
100 OUT CTRLADDR, CTRLWRD:  'initialize 8255
110 '
120 OUT PORTB, CHANNEL:                 'set input channel address
130 OUT PORTB, (CHANNEL  OR &H8):       'B3 HIGH enable address latch
140 OUT PORTB, (CHANNEL AND &HF7):      'B3 LOW
150 '
160 OUT PORTB, (CHANNEL  OR &H10):      'B4 HIGH start conversion
170 OUT PORTB, (CHANNEL AND &HEF):      'B4 LOW
180 '
190 EOC = 0:                            'wait for End Of Conversion
200 WHILE EOC<> &H80 : EOC = INP(PORTC) AND &H80: WEND
210 '
220 OUT PORTB, (CHANNEL  OR &H27):      'B5 HIGH enable ADC outputs
230 LOCATE 1,1:PRINT "Channel ";CHANNEL;" : ";INP (PORTA);"    "
240 OUT PORTB, (CHANNEL AND &HDF):      'B5 LOW disable ADC outputs
250 '
260 PRINT : PRINT "Press N for next channel or S to stop"
270 A$=INKEY$
280 IF (A$="N" OR A$="n") THEN GOTO 310
290 IF (A$="s" OR A$="S") THEN END
300 GOTO 150
310 '
320 CHANNEL = CHANNEL + 1
330 IF CHANNEL = 8 THEN CHANNEL = 0
340 GOTO 110
```

934087 - 12



BATTERY DISCHARGER

When batteries are charged rapidly, the manufacturer usually recommends that after every fifth fast charge there is a 'normal' charge, that is, one at 0.1 C(apacity). That can, however, be done only if the battery is discharged. At the same time, the individual cells must not be discharged too much. If, for instance, one cell is flat and the others are still charged or nearly so, the polarity of the flat cell reverses and that must be prevented to save the battery. As a rule of thumb, a battery should be discharged to an average of 1 V per cell.

The diagram shows a circuit that is suitable for discharging nickel-cadmium (NiCd) as well as nickel-metal-hydride (NiMH) batteries. It is simple and inexpensive, but the components must be matched to the number of cells the battery contains.

As long as D_2 lights, the battery is discharged via R_4 and T_1. When the battery voltage drops below a value set with P_1, T_1 no longer gets a base current. The LED will then go out and the discharge circuit may be removed. The battery can then be charged.

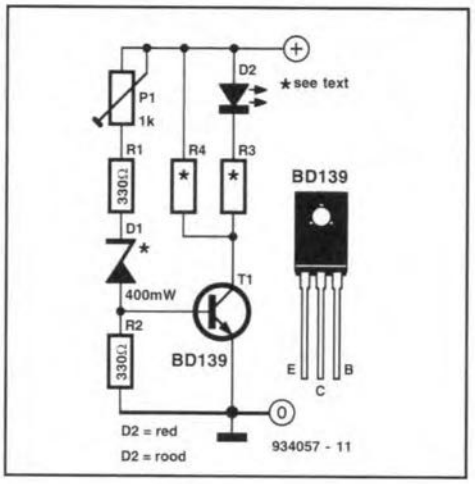
The circuit may be tested with the aid of a variable power supply with current limiting. Connect the discharger to the power supply: R_4 may be omitted. Set the output of the supply to the wanted level, whereupon T_1 should switch off. Adjust P_1 till D_2 lights dimly. This sets the voltage to which a battery may be discharged.

Since the gain is not very high, there is an area where D_2 diminishes gradually and where, therefore, the discharge current decreases gradually. This does not affect the circuit, however.

If the range is too small, the value of the zener diode should be reduced or increased.

The value of R_4 is calculated for a discharge current of about 0.5 A. This value is not critical. That is, if a resistor of 6.8 Ω proves difficult to obtain, a 4.7 Ω or 10 Ω resistor may be used without detriment. Since the voltage of the cells is monitored, it is not necessary to stabilize the discharge current.

[K. Walraven – 934057]



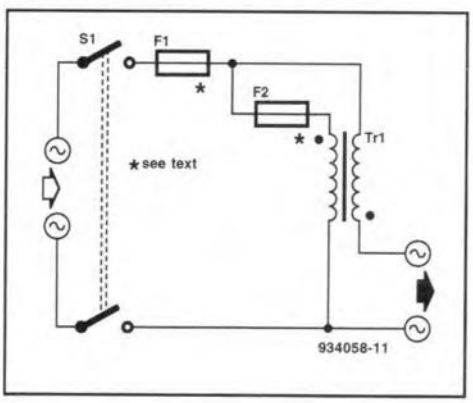
No. of cells	D_1 [V]	R_3 [Ω]	R_4 [Ω]
3	1.2 [2 diodes]	150	6.8 [5 W]
4	2.4 [3 diodes]	270	10 [5 W]
5	3.3	330	12 [5 W]
6	3.9	470	15 [10 W]
7	4.7	560	15 [10 W]
8	5.6	680	18 [10 W]
9	6.8	680	22 [10 W]
10	8.2	820	22 [10 W]

POWER BOOSTER FOR SLIDE PROJECTORS

The lamp in slide projectors is normally controlled with the aid of a triac in series with it. This method reduces the brightness of the lamp appreciably, since the triac drops about 1.5 V, which is more than 6% of the nominal lamp voltage. To compensate this loss, the mains voltage to the projector should be increased by that percentage. The transformer and ventilator can cope easily with that kind of increase, and so can any electronic circuits, since these are invariably powered via a regulator.

The a.c. voltage to the projector may be increased by connecting the secondary winding of a mains transformer in the live wire of the mains. The voltage developed across this winding is then added to the mains voltage (provided that the transformer is connected correctly as regards phase).

The voltage the secondary winding must deliver is calculated as follows. The current through the winding depends on the number of projectors and their rating.



Assuming there are four, each rated at 250 W (power consumption: 300 W), the total power consumption during normal operation is 1200 W. With a mains voltage of 240 V, the current will be 5 A. Since the projectors do not all use full power simultaneously, the secondary winding may be rated at 6 A. The secondary voltage, U_s, should be the ratio of the loss across the triac and the nominal lamp voltage times the mains voltage, that is,

$$U_s = 1.5/24 \cdot 240 = 15 \text{ V}.$$

Fuse F_1 should be rated at 1.25×the maximum current of all projectors. Assuming the earlier stated values, that is,

$$I_{fuse1} = 1.25 \cdot 1200/240 = 6.25 \text{ A},$$

or, rounded off to the next standard value, 6.3 A (delayed action). The rating of fuse F_2 is calculated from

$$I_{fuse2} = 1.25 \cdot U_s \cdot I_s/240 = 487 \text{ mA},$$

or, rounded off upwards, 500 mA.

The circuit should preferably be fitted in a man-made fibre enclosure.

If the output voltage is lower, rather than higher, than the mains voltage, the connections to either the pirmary or the secondary of the additional transformer must be interchanged.

[A. Rietjens - 934058]

NiMH BATTERY CHARGER

Nickel-metal-hydride (NiMH) batteries have now become widely available. A typical one is the 120AAH, which has a capacity of 1.2 Ah in size AA (MN1500; LR6). This type does not lose more than 45% of its capacity through self-discharge over a period of 25 days at a temperature of 20 °C. Recommended fast charging instructions are charging with a current of 0.3C for not more than 2.5 hours, or until the cell voltage has risen to 1.49 V, or until the cell temperature rises above 40 °C. The cell is then charged up to 75% of its capacity, after which it should be charged with a current of 0.1C, which it can stand for long periods. The circuit shown enables these instructions to be adhered to.

Output CT13 of IC_2 goes high after $2^1/_2$ hours, whereupon charging stops. At the same time, the output of IC_{1a} goes high when the battery voltage rises above 1.49 V per cell. This output then toggles, which also stops the charging.

The number of cells contained in the battery to be charged is set with the value of R_{14}: for 1 cell, the resistor is omitted; its value for 2 cells is 100 kΩ; for 3 cells, 2×100 kΩ in parallel (= 50 kΩ); for 3 cells, 3×100 kΩ in parallel; and so on.

The third way of ending the charging is by means of the temperature measured with IC_5. When the temperature rises above 40 °C, IC_{1b} terminates the charging.

The three charging outputs are formed into OR gates by D_2–D_4. Since these are low-current LEDs, it is immediately visible on what basis charging has been discontinued.

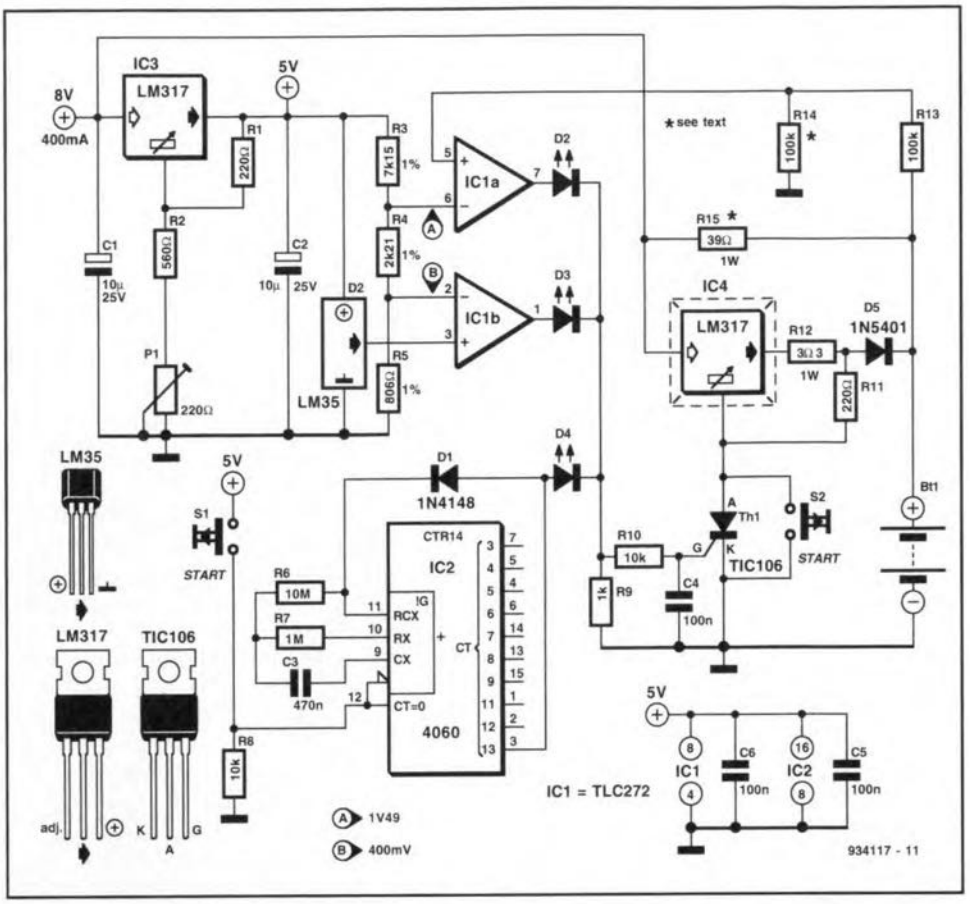
The charger is switched from 0.3 C to 0.1 C (that is, off), te control input of current source IC_4 is connected to earth via thyristor Th_1. The output potential of IC_4 can then not rise above 1.2 V. Since this is lower than the battery voltage, D_5 will be reverse-biased. Further charging of the battery is then via R_{15}. The value of this series resistor (in Ω) is obtained by dividing the difference (in V) between the supply voltage and the battery voltage by 0.12. The quotient should be rounded off to the nearest standard value (the exact value is not terribly important).

The level of the supply voltage depends on the number of cells contained in the battery to be charged. Its minimum value is 4 V plus the number of cells times 1.5 V.

It is necessary to mount IC_4 on a small (10 K W^{-1}) heat sink.

Two keys must be pressed to switch the charger on: S_1 resets timer IC_1 and S_2 switches off thyristor Th_1. These switches could be combined, but double-pole key switches are not generally available.

[K. Walraven - 934117]



BATTERY VOLTAGE MONITOR

Philips' IC Type TEA1041T is intended primarily for monitoring the voltage of 1.8–4.0 V batteries. Internal trigger and timing logic prevent a circuit from reacting to brief breaks in the supply voltage caused by pulses on the load current. One or two LEDs may be used to indicate when the voltage drops below a preset level.

A circuit with two LEDs is shown in **Fig. 1**. Potential divider R_1-R_2 determines the voltage level below which the LEDs indicate that the battery is charged. The divider should give a voltage of exactly 1.25 V at pin 1. Give R_2 a value between 1 kΩ and 100 kΩ and calculate R_1 from

$$R_1 = R_2(U_{th}/1.25-1) \quad [\Omega],$$

where U_{th} is the wanted voltage level. The values of R_3 and R_4 are 100–220 Ω, depending on the battery voltage.

The TEA1041T is enabled when pin 3 is at ground level. If the voltage at pin 1 drops below 1.25 V, a digital counter runs for about 2 s. If the level at pin 1 remains <1.25 V, the IC goes into the alarm state: D_1 lights and continues to do so even when the voltage at pin 1 reaches 1.25 V again. If in this condition S_1 is opened, both LEDs flash for about 4 s. After that, the IC reverts to the standby state, in which it draws a current of about 10 µA, which constitutes only a minute a load on the battery.

Figure 2 shows how the IC can be incorporated in an existing apparatus: D_2 is omitted and pin 3 is permanently at ground level. The monitor is connected across the load as long as S_1 is closed. The IC performs as described earlier, but the LED does not flash after the reset.

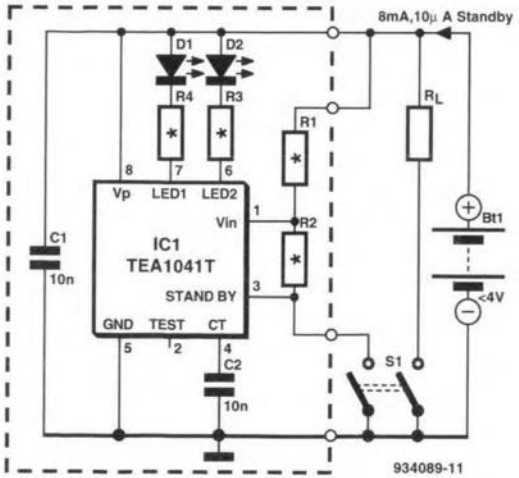
If the supply voltage is higher than 4 V,

connections must be made as shown by the dashed lines in **Fig. 2** (R_1 to R_5 and D_3 and C_3 to earth). The supply voltage is then lowered to 3.3 V by D_3. The potential divider is connected across the full supply voltage.

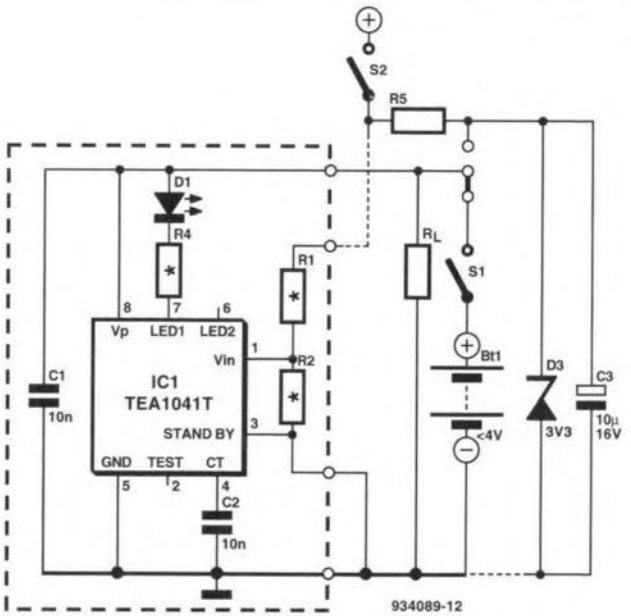
Source: Philips Data Sheet TEA1041T: Battery Low-level Indicator.

[G. Kleine - 934089]

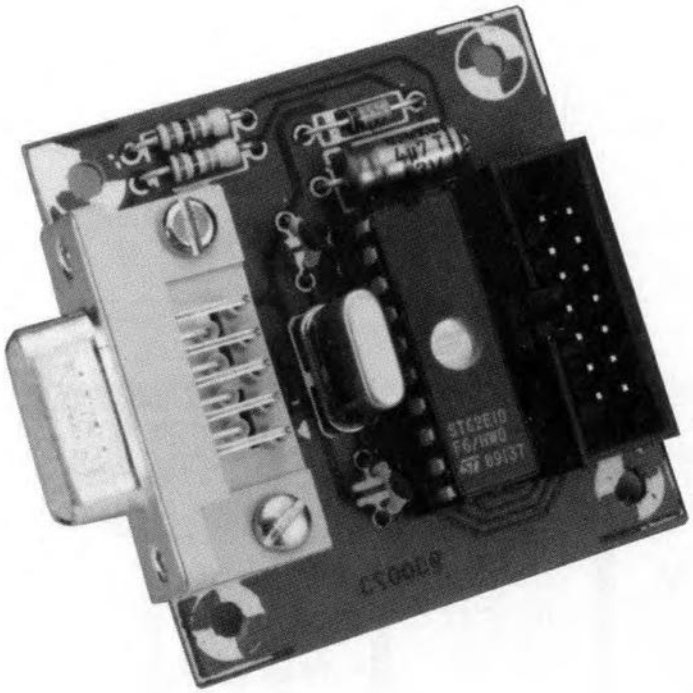
1



2



MICROCONTROLLER-DRIVEN UART



This project demonstrates how a microcontroller fills the bill when it comes to reducing the size and component count of complex digital circuits. Here, one such circuit, the otherwise awesome UART (universal asynchronous receiver/transmitter), is formed by an ST62E10 8-bit controller and a handful of passive parts.

Design by B. Kainka

MANY computer links require serial-to-parallel or parallel-to-series conversion of data formats. Traditionally, this function is performed by a universal asynchronous receiver/transmitter (UART), the best known of which is the AY-3-1015. Unfortunately, this device is not easily programmed from a computer system, since it requires quite a few DIP switches to set up the communication protocol, handshaking, etc. By contrast, the microcontroller used here, an ST62E10 from SGS-Thomson, has a number of registers that allow the PC to use 10 parallel lines as digital inputs or outputs, analogue inputs, or even a mix of these. This 'intelligent' UART is controlled by the PC via the RS232 port, with the registers acting as the software equivalent of DIP switches.

The use of the 20-pin version of the ST62xx microcontroller allows the number of external components to be kept to a minimum, while the current consumption remains limited to a modest 2 mA or so. The extra I/O capacity (8 lines) of the next larger controller in the family, the 28-pin ST62x5, is tempting, but not really required for the present application.

Introducing the ST6210

Considering that it would be too easy, on the one hand, to treat the microcontroller in the circuit as a black box, while, on the other hand, a full description of all the bells and whistles of the device is beyond the scope of this article, a short description is given of the ST6210 architecture, with reference to **Fig. 1**.

The ST62xx family of microcontrollers is based on a so-called macro cell structure, which consists basically of a central unit, ROM or EPROM, RAM, and some peripheral circuitry. The latter comprises:

- a timer with an 8-bit counter and a 7-bit programmable prescaler;
- 8 or 16 digital input/output lines, or analogue input lines;
- a digital watchdog (DWD).

The only difference between the ST621x and the ST622x is the size of the ROM, which is 2 KByte in the ST621x, or 4 KByte in the ST622x. On both controllers, 220 bytes of the ROM space is reserved for the system.

A detailed diagram of the 8-bit core of the ST62xx controller is given in **Fig. 2**. Here, you find the classic ingredients of modern microcontrollers: CPU, ROM, RAM, etc.
The ST62Exx is the family member with EPROM instead of ROM. The advantage of EPROM over conventional ROM is that the memory is erasable and re-programmable, which for the obvious reason of easier debugging, makes it just the thing for application developers. To complete the ST62xx family picture, we should mention the one-time programmable (OTP) version, designated ST62Pxx.

The difference between the 'T' and 'E' version of the ST62xx controller is that two memory areas, 0800H to 087FH, and 0FA0H to 0FEFH, are not usable (reserved) in the 'T' device, while they are available in the 'E' device. In many cases, these 200-odd bytes come in handy to the programmer.

Mixed I/O use is allowed on the microcontroller's port lines, i.e., lines may be programmed individually to function as an input or an output. The input or output function is programmed via the command register contained in the RAM area of the processor. This register is externally programmable, giving full control over all the features offered by the microcontroller. This allows device parameters such as the I/O lines definition, to be held externally (for instance, on a PC), for writing into the ST62xx, while the microcontroller runs a 'fixed' program, reading the parameters from its RAM area as required.

The ST62E10 is connected to a PC via an RS232 link, which keeps the number of I/O lines used down to two. Since the microcontroller proper does not contain an RS232 interface, this function is realized in software, i.e., by appropriate routines that arrange the data transfer to and from the PC.
Port line A0 functions as a the TxD (transmitted data) input, and port line

A1, as the RxD (received data) output. Since the UART we are about to describe belongs functionally in the DTE (data terminal equipment) class, TxD is an input, and RxD, an output.

Circuit description

If you like simple circuits, this one is for you, because the circuit diagram in **Fig. 4** shows only one integrated circuit and seven passive parts. Not surprisingly, this simplicity can be achieved only by a certain amount of 'intelligence' which, you guessed it, resides in the microcontroller. Actually, the intelligence is formed by a chunk of machine code program held in the on-board EPROM.

The microcontroller is clocked by its on-board oscillator, which operates with an external 4-MHz quartz crystal, X1, as the frequency determining component. The controller's port lines are connected to two sockets, K1 for the computer link, and K2 for the parallel equipment. Zener diode D1 keeps the swing of the signal received on port line PA0 within safe limits. Capacitor C1 decouples the microcontroller's supply voltage, while resistors R1 and R2 act as current limiters on the PA0 and PA1 port lines.

It will be noted that the interface does not contain buffers. The baud rate is fixed at 19,200, and determined by the 4-MHz quartz crystal. The baud rate may be doubled to 38.4 Kbaud simply by fitting an 8-MHz quartz crystal. Similarly, a 2-MHz crystal gives a baud rate of 9,600.

Software considerations

Since the microcontroller's clock frequency is divided internally by 13, a maximum of 16 machine cycles is available for each bit. For example, at a clock of 4 MHz:

4,000 kHz / 13 = 307.692 kHz
307.692 kHz / 16 = 19,231 bits/s

Because the length of the processor instructions varies between two and five machine cycles, a bit on the serial link must be recognized or generated in no more than 4 instructions (typically). This means that the programmer can not make use of loops to create serial (RS232) signals. Consequently, each of the 8 bits transmitted has its own set of instructions. Similarly, the instructions that form the 'receive' routine must be in keeping with the chronological order dictated by the 16 machine cycles, irrespective of whether the received information is a 0 or a 1. This is achieved by inserting 'dummy' instructions where necessary. The same goes for the 'transmit' routine.

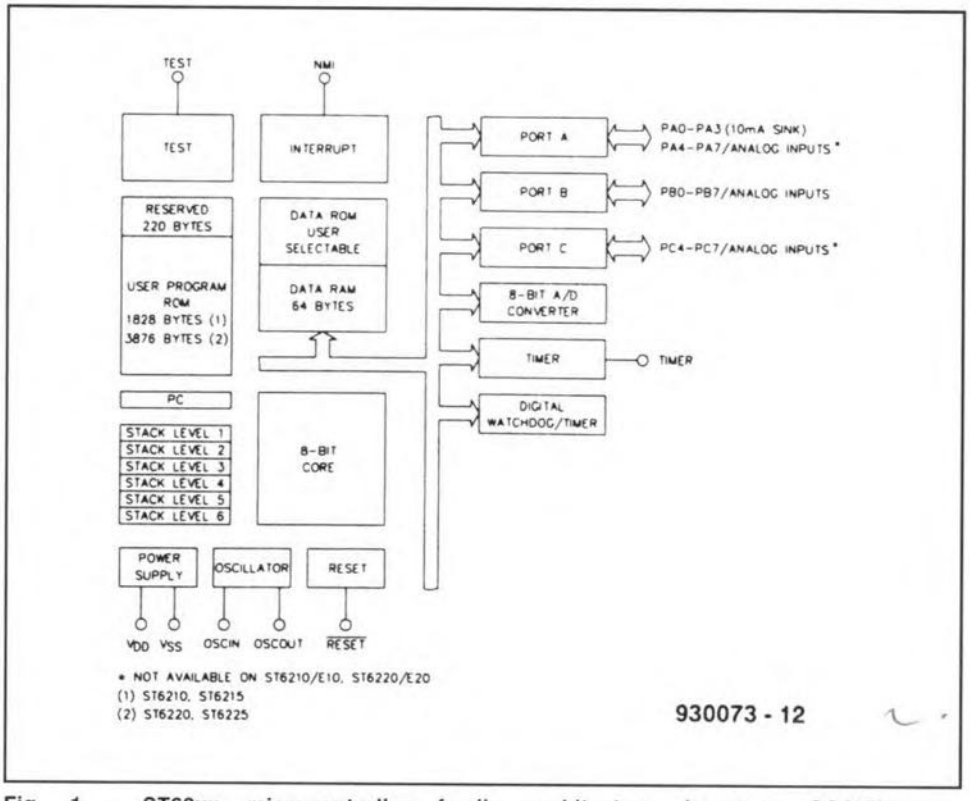


Fig. 1. ST62xx microcontroller family architecture (courtesy SGS-Thomson Microelectronics).

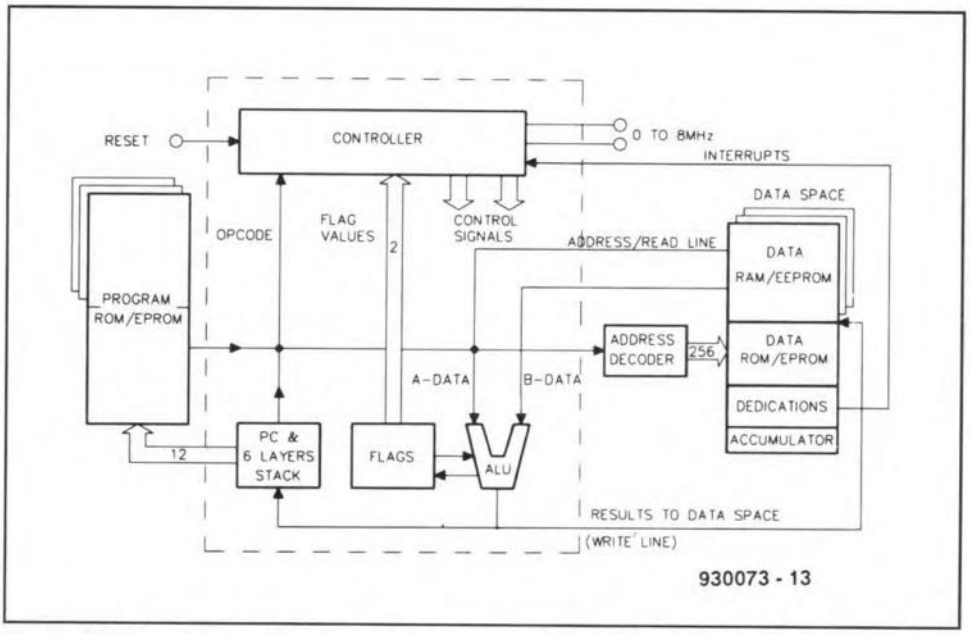


Fig. 2. ST62xx microcontroller core architecture (courtesy SGS-Thomson Microelectronics).

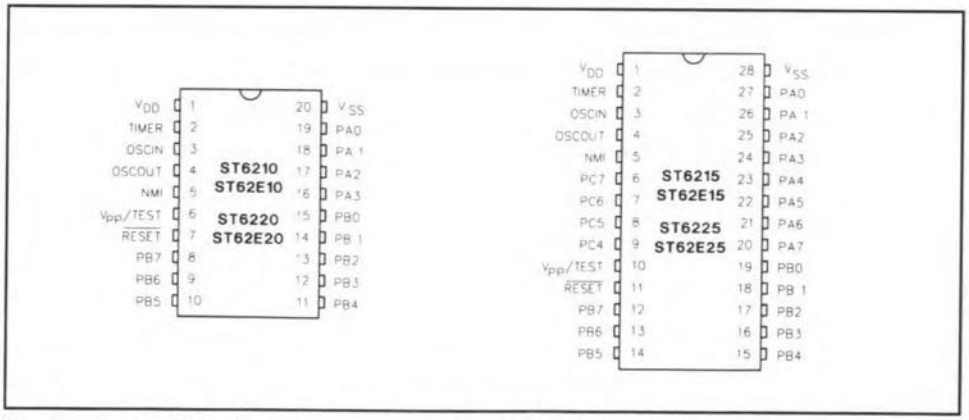


Fig. 3. Pinouts of the devices in the ST62xx family of microcontrollers.

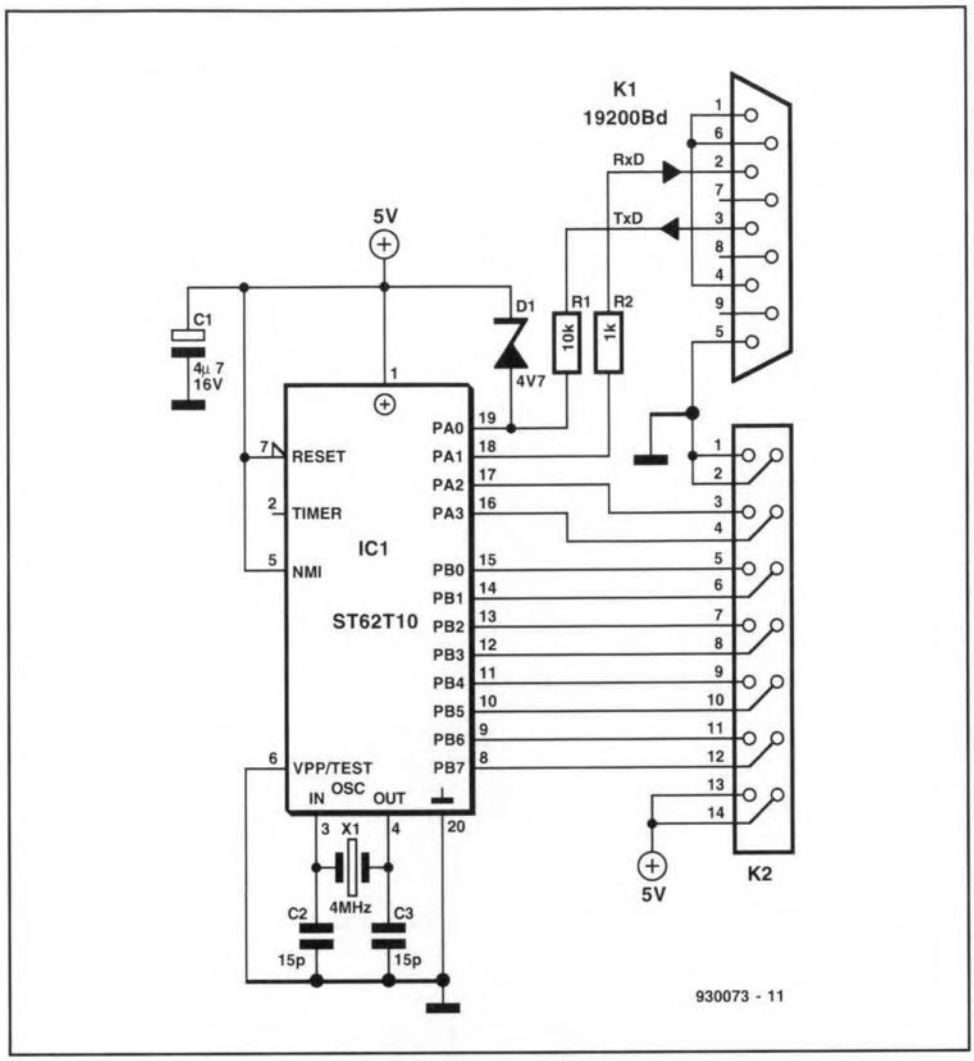


Fig. 4. Circuit diagram of the microcontroller-driven UART.

The main program contains a loop in which data is received, interpreted and processed further. To enable this to be done, the following protocol has been set up: to read the contents of a register, the PC transmits the register address (between 128 and 255), whereupon the microcontroller reads the byte contained at this address, and transmits the information back to the PC. To be able to write to an address, bit 7 must be made 0, i.e. the write addresses of the registers are 0 through 127. The databyte that follows the 'write' address is written into the register. The databyte should come within a certain period after the register 'write' address. If not, the watchdog is alerted, and causes the ST62E10 to be reset.

The interface can be used only if the functions of certain registers in the microcontroller are known. The function of the I/O lines is defined by the following registers: 'ddr' (data direction register), 'ior' (interrupt option register) and 'dr' (data register). Each of the ports A, B and C (ST62x5 only) has its own set of ddr, ior and dr registers. The table below gives the most frequently used options. As already mentioned, each port line can be programmed individually.

ddr	ior	dr	function
0	0	0	input with pull-up
0	0	1	input without pull-up
0	1	1	analogue input, except for PA0-PA3 and PC0-PC3
1	0	x	open-drain output
1	1	x	push-pull output

The microcontroller used in this project is available ready-programmed through our Readers Services under order code 7151.

Interface driver demo

The listing in **Fig. 6** shows a Turbo Pascal program to demonstrate the operation of the UART. The addresses of the most important registers are set up in the 'declarations' preamble of the

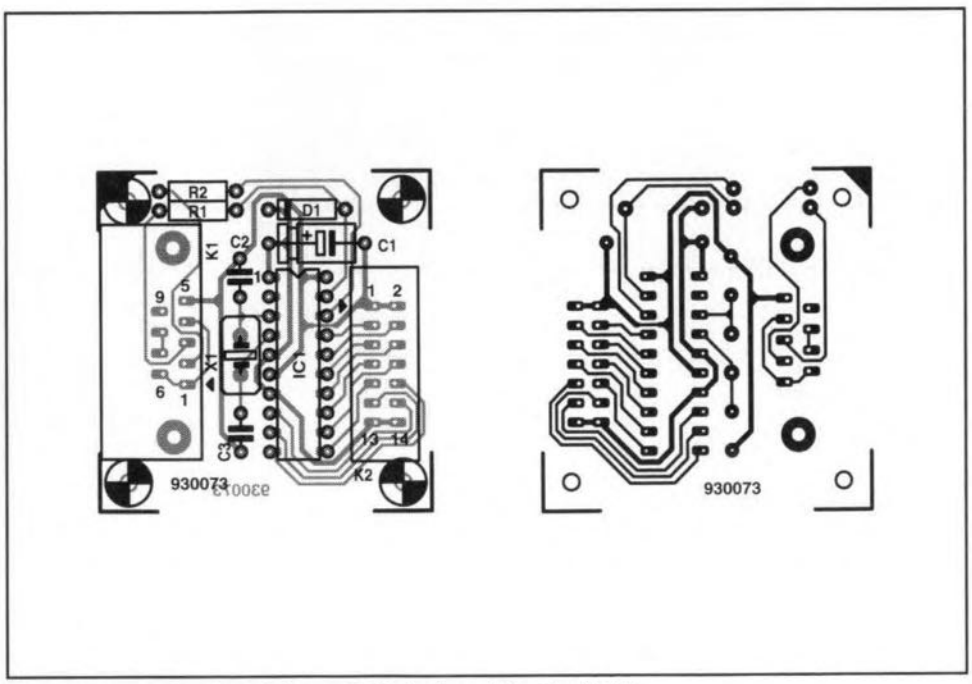


Fig. 5. Artwork for the miniature PCB designed for the UART.

COMPONENTS LIST

Resistors:

1	10kΩ	R1
1	1kΩ	R2

Capacitors:

1	4µF7/16V	C1
1	15pF	C2,C3

Semiconductors:

1	zener 4V7/500mW	D1
1	ST62T10 (order code 7151; see page 110)	IC1

Miscellanaeous:

1	4MHz quartz crystal	X1
1	PCB mount 9-way sub-D socket	K1
1	2x7 pin header	K2
1	Printed circuit board 930073 (see page 110).	

```
program st6_Register;
uses Crt    ;
const ddra = $C4;    { direction register a..c }
      ddrb = $C5;
      ddrc = $C6;
      ora  = $CC;    { option register a..c }
      orb  = $CD;
      orc  = $CE;
      dra  = $C0;    { data register a..c }
      drb  = $C1;
      drc  = $C2;
      adcr = $D1;    { A/D control register }
      adr  = $D0;    { A/D data register }

var   N, BA : Integer;

procedure Transmit (charact :Byte);
begin
  while (Port[BA+5] And 32) = 0 do;  { Transmit register empty? }
  Port[BA]:=charact;                 { 32 or 64 or even 96??? }
end;

function Receive :Byte;
var  i :Word;
begin
  i:=0;
  while ((Port[BA+5] And 1)=0) And (i<3200) DO Inc(i);
  if i < 3200
  then Receive:=Port[BA]
  else begin
         Delay(10);
         Receive := 0;
  end;
end;


procedure Init;
var  i :Word;
begin
  BA:=$2F8; { $3F8 = COM1, $2F8 = COM2 }
  Port[BA+3]:=128;
  Port[BA+0]:=6; { 6 for 19200 Baud, 3 for 38400 Baud }
  Port[BA+1]:=0;
  Port[BA+3]:=7; { 8-Bit, n-Parity, 1 Stopbit }
  Port[BA+1]:=0; { no Interrupts }
  Port[BA+4]:=3; { DTR = 1, CTS = 1 }
  i:=Port[BA];      { Input buffer empty }
  Transmit (0);
  Transmit (0);
end;

procedure RegOut (Address,Datum : Byte);
   begin
     Transmit (Address AND 127);
     Transmit (Datum);
   end;

function RegIn (Address : Byte): Byte;
   begin
     Transmit  (Address);
     Regin := Receive;
   end;

{ 1st Example: Transmit and read back digital Data from Port B }

begin
  Init;
  RegOut (ddrb,$FF);    { Port B: Output }
  RegOut (orb,$FF);     { Push-pull }
  repeat
    for n:= 1 to 255 do begin
      RegOut (drb,n);
      if RegIn (drb) <> n then writeln ('Error');
      write (RegIn(drb));
    end;
  until keypressed
end.

{ 2nd Example: Analogue Input to Port B0 }

begin
  Init;
  RegOut (ddrb,$00);    { Port B: Input }
  RegOut (orb,$FF);     { analogue }
  RegOut (drb,$01);     { B0 is present input }
  repeat
    RegOut (adcr,$30);       { Start measuring }
    writeln (RegIn (adr));  { Read measured value }
    delay (100);
  until keypressed
end.
```

Fig. 6. An interface demo written in Turbo Pascal.

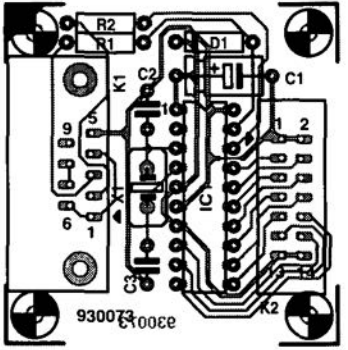
program. The function of each port line must be indicated when the ports are used for digital input or output. Next, it is possible to program a continuous exchange of data between the data register and the relevant port.

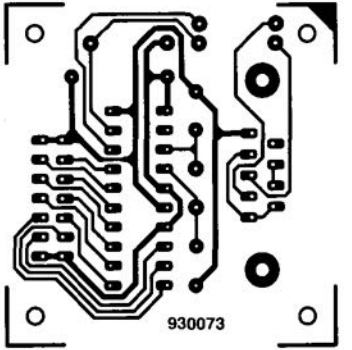
To be able to use the analogue-to-digital converter (ADC) contained in the microcontroller, it is necessary to first program one of the port lines as an input. This is achieved via the port register. The actual conversion is started via the ADC command register. The conversion is pretty fast at only 140 µs, after which the result may be read from the ADC data register.

Construction

The artwork of the printed circuit board designed for the microcontroller-driven UART is given in **Fig. 5**. There are very few components to fit, and construction should not present problems. Start by fitting the smaller parts: the resistors, the diode, the crystal (vertically mounted) and the capacitors. Next, mount an IC socket in position IC1, followed by the two connectors.

The UART is connected to the RS232 port on the PC via a 9-way cable. One end of this cable should have a 9-way sub-D plug, the other, a 9-way sub-D socket. The cable should be a 'straight through' type, i.e., no crossed wires for the TxD and RxD pins. If you want to go round making your own cable, go out and buy a so-called Hercules monitor extension cable. These are often cheaper than two 9-way sub-D connectors! ■





1	10kΩ	R1
1	1kΩ	R2

Capacitors:

1	4μF7/16V	C1
1	15pF	C2,C3

Semiconductors:

1	zener 4V7/500mW	D1
1	ST62T10 (order code 7151; see page 110)	IC1

Miscellanaeous:

1	4MHz quartz crystal	X1
1	PCB mount 9-way sub-D	

FIGURING IT OUT

PART 11 – QUADRIPOLES

By Owen Bishop

This series is intended to help you with the quantitative aspects of electronic design: predicting currents, voltage, waveforms, and other aspects of the behaviour of circuits. Our aim is to provide more than just a collection of rule-of-thumb formulas. We will explain the underlying electronic theory and, whenever appropriate, render some insights into the mathematics involved.

Quadripoles, otherwise known as 4-terminal networks, or 2-port networks, are the final excursion into network analysis in the present series. The essential features of a quadripole are illustrated in **Fig. 90**. The network is linear, its output being directly proportional to its input and varying continuously with it. Current I_1 enters Port 1 by one terminal and leaves by the other. Current I_2 enters and leaves Port 2. The behaviour of the network at any given frequency, and as seen from the outside, may be completely specified by reference to four impedances, known as the **open-circuit** impedance parameters, or **z-parameters**. Current I_1 produces a pd across Port 1 as the result of its flowing through z_{11}. It also produces a pd across Port 2, for which the relevant impedance is z_{21}. Similarly, I_2 produces pds across Ports 1 and 2, as the result of flowing through z_{12} and z_{22} respectively. Summing these pds at each port:

$$U_1 = z_{11}I_1 + z_{12}I_2 \quad \text{[Eq. 69]}$$
$$U_2 = z_{21}I_1 + z_{22}I_2 \quad \text{[Eq. 70]}$$

These two equations define the z-parameters. With Port 2 open-circuited, so that $I_2 = 0$, we find:

From Eq. 69: $z_{11} = U_1/I_1$ [Eq. 71]

From Eq. 70: $z_{21} = U_2/I_1$ [Eq. 72]

With Port 1 open-circuited, so that $I_1 = 0$, we find:

From Eq. 69: $z_{12} = U_1/I_2$ [Eq. 73]

From Eq. 70: $z_{22} = U_2/I_2$ [Eq. 74]

As an illustration, consider the T-section resistance network of

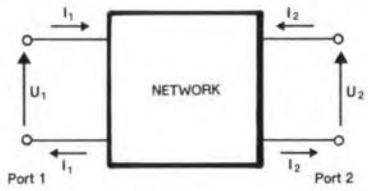


Figure 90

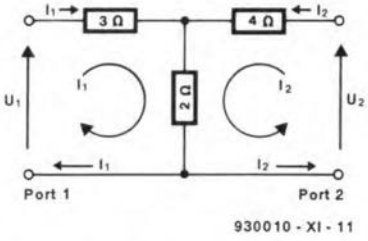


Figure 91

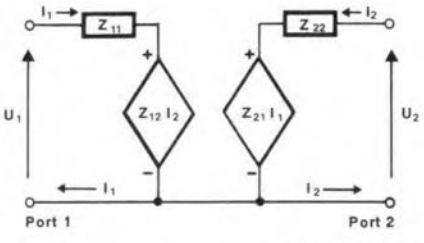


Figure 92

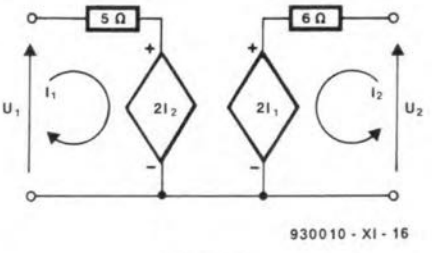


Figure 93

Fig. 91. Mesh current analysis (Part 4) provides equations from which the z-parameters may be calculated:

Mesh 1: $U_1 = (3+2)I_1 + 2I_2$;
Mesh 2: $U_2 = 2I_1 + 6I_2$.

Note that, instead of defining all currents as clockwise, as we usually do, I_1 is clockwise and I_2 is anticlockwise. This eliminates negatives from the equations. Comparing the coefficients in the mesh equations with those in Eq. 69 and 70, we see that:

$z_{11} = 5\ \Omega$;
$z_{12} = z_{21} = 2\ \Omega$;
$z_{22} = 6\ \Omega$.

All z-parameters are expressed in ohms.

z-parameter model

Based on the z-parameters, a quadripole may be represented by the model of **Fig. 92**. z_{11} and z_{22} are represented as impedances in series with the ports. U_1, the pd produced at Port 1 as a result of I_2, is represented by a **controlled voltage source**, $z_{12}I_2$, accounting for the last term of Eq. 69. Similarly, the last term of Eq. 70 is represented by the controlled voltage source $z_{21}I_1$. **Figure 93** shows the T-network of **Fig. 91** as a z-parameter model. This model can be used to predict the behaviour of the network when connected to external circuits. If we know the voltages at the ports, we use Eq. 69 and 70 to calculate the currents. Conversely, given the currents, we can calculate the voltages.

Example. In the network of **Fig. 91**, $I_1 = 2$ A, $I_2 = 3$ A. Calculate U_1 and U_2.

From Eq. 69:

$U_1 = 5 \times 2 + 2 \times 3 = 16$ V.

From Eq. 70:

$U_2 = 2 \times 2 + 6 \times 3 = 22$ V.

Determining parameters

If the circuit of the quadripole is known, z-parameters may be calculated by the usual network

techniques, as we did for **Fig. 91**. These are open-circuit parameters, which means that the ports can be considered in turn as open circuits to simplify the calculations. As an example, take the π-network of **Fig. 94**. With Port 2 open-circuited, I_2 flows through R_1 in parallel with R_3 and R_2. Their combined resistance is 4.167 Ω. From Eq. 71:

$$z_{11} = U_1/I_1 = 4.167\ \Omega.$$

The current flowing through R_2 is:

$$I_R = I_1 \times R_1/(R_1 + R_2 + R_3)$$

$$= 5I_1 / 30 = I_1 / 6.$$

This generates a pd across R_2:

$$U_2 = 15I_1 / 6 = 2.5I_1.$$

Now we can calculate z_{21}, using Eq. 72:

$$z_{21} = U_2 / I_1 = 2.5\ \Omega.$$

With Port 1 open-circuited, similar calculations show that:

$$z_{12} = 2.5\ \Omega;$$
$$z_{22} = 7.5\ \Omega.$$

Now suppose that R_3 is replaced by a 10 μF capacitor (**Fig. 96a**). If ω = 10^4, then $X_C = -1 / \mathbf{j}\omega C = -\mathbf{j}10\ \Omega$. We can use this in place of the resistance of R_3 in the calculations above. The combined impedance of R_2 and X_C is $(15 - \mathbf{j}10)\ \Omega$. In parallel with 5 Ω, the total resistance is

$$5\,(15 - \mathbf{j}10) / (5 + 15 - \mathbf{j}10)$$
$$= (15 - \mathbf{j}10) / (4 - \mathbf{j}2)$$
$$= 18.03\,\angle{-33.69°} / 4.47\,\angle{-26.57°}$$
$$= 4.03\,\angle{-7.12°}.$$
$$z_{11} = 4.03\,\angle{-7.12°}\ \Omega.$$

Techniques for handling complex numbers are described in Part 8.

Current flowing through R_2 is:

$$I_R = I_1 \times 5 / (20 - \mathbf{j}10).$$

The pd across R_2 is:

$$U_2 = I_R R_2 = 75I_1 / (20 - \mathbf{j}10)$$
$$= I_1 \times 75 / 22.36\,\angle{-26.57°}$$

$$\therefore\ z_{21} = U_2 / I_1$$
$$= 75\,/22.36\,\angle{-26.57°}$$
$$= 3.35\,\angle{26.57°}\ \Omega.$$

From these two parameters we can calculate the gain of this network, assming that it is lightly loaded. With a high-impedance load, $I_2 \approx 0$.

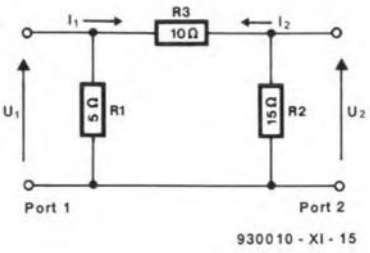


Figure 94

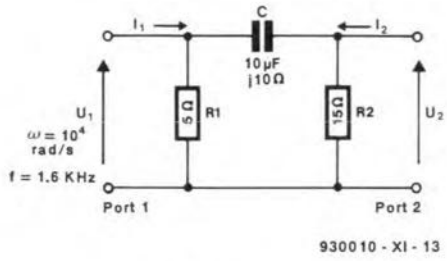


Figure 95 a

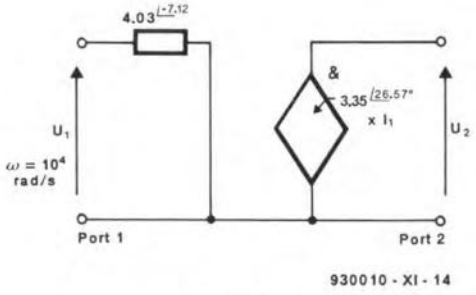


Figure 95 b

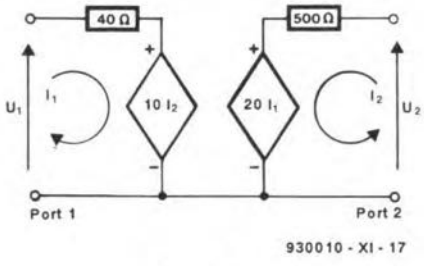


Figure 96

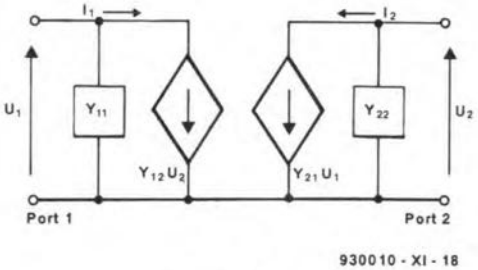


Figure 97

The Port 1 voltage source, $z_{12}I_2$, and z_{22} may be omitted from the model (**Fig. 95b**). Then, from Eq. 69 and 70:

$$\text{gain} = U_2 / U_1 = z_{21} / z_{11}$$
$$= 3.35\,\angle{26.57°} / 4.03\,\angle{-7.12°}$$
$$= 0.83\,\angle{33.69°}.$$

The output pd is 0.83 times the input pd and there is a phase lead of 33.69°.

Repeating this calculation with ω = 2 × 10^4 gives a gain of $0.95\,\angle{18.43°}$. Gain is increased and phase lead is reduced, as might be expected with a high-pass filter network.

Practical technique

The *z*-parameters of a complicated network may be measured indirectly. By leaving the appropriate port open-circuit, we can make either I_1 or I_2 equal to zero. Then, measurements of the other current and the voltage are substituted in Eq. 71–74. Once these values are obtained, we use them to predict the behaviour of the quadripole under other input and output conditions.

Example. At a given frequency, and with Port 2 open-circuited (so that $I_2 = 0$) and 10 V applied to Port 1, measurements made on an unknown network are:

$U_1 = 10$ V;
$U_2 = 5$ V;
$I_1 = 0.25$ A.

With Port 1 open-circuited (so that $I_1 = 0$) and 10 V applied to Port 2, measurements made are:

$U_1 = 0.2$ V;
$U_2 = 10$ V;
$I_2 = 0.02$ A.

With Port 2 open-circuited, substituting in Eq. 69 and solving for z_{11}:

$$z_{11} = 10 / 0.25 = 40\ \Omega.$$

Substituting in Eq. 70 and solving for z_{21}:

$$z_{21} = 5.0 / 25 = 20\ \Omega.$$

Similarly, with Port 1 open-circuited:

$$z_{12} = 0.2 / 0.02 = 10\ \Omega;$$
$$z_{22} = 10 / 0.02 = 500\ \Omega.$$

Figure 96 shows these results incorporated in the *z*-parameter model. The parameters may now be used to predict network behaviour with other values of pd or current at the same frequency.

Other parameters

The *z*-parameters show how the voltages are determined by the currents and impedances as defined in Eq. 69 and 70. We can write a corresponding pair of equations showing how the currents are determined by the voltages and another set of parameters, the *y*-parameters. This is another instance of duals (see Part 5), so it should come as no surprise to find that the *y*-parameter model of a quadripole has an **admittance** in **parallel** with each port, and a pair of controlled **current**

sources (**Fig. 97**). As might be expected from the duality, *y*-parameters are calculated or measured by **short-circuiting** one or the other of the ports. The equations for *y*-parameters are:

$$I_1 = y_{11}U_1 + y_{12}U_2;$$
$$I_2 = y_{21}U_1 + y_{22}U_2.$$

The *y*-parameters are admittances, so their unit is the siemens (S). They are used in calculations similar to those above, if working with admittances is more convenient.

A third set of parameters consists of the *h*-parameters. The *h* stands for 'hybrid', because these parameters are based on a mix of U_1 and I_2, the **pd** across Port 1 and the **current** through Port 2:

$$U_1 = h_{11}I_1 + h_{12}U_2 \quad [\text{Eq. 75}]$$
$$I_2 = h_{21}I_1 + h_{22}U_2 \quad [\text{Eq. 76}]$$

We will find the *h*-parameters for the circuit of **Fig. 91**. With Port 2 short-circuited, as in **Fig. 98a**, (so that $U_2 = 0$), from Eq. 75:

$$h_{11} = U_1 / I_1.$$

But U_1 / I_1 equals the resistance of the network when Port 2 is short-circuited: this is 3 Ω in series with 2 Ω and 4 Ω in parallel. This gives a total resistance of 4.33 Ω. Thus, h_{11} = 4.33 Ω. The unit of h_{11} is ohms.

From Eq. 76, we have:

$$h_{21} = I_2 / I_1.$$

Figure 98b shows the shorted network redrawn to make flow of current easier to visualise. The pd across *AB* is:

$$U = 2(I_1 + I_2) = -4I_2;$$
$$\therefore\ I_1 = -3I_2.$$

Substituting in the equation for h_{21}:

$$h_{21} = -1 / 3.$$

h_{21} is a ratio between two currents: it is a pure number without units.

With Port 1 **open-circuited**, as in **Fig. 91**, so that $I_1 = 0$, we have from Eq. 75:

$$h_{12} = U_1 / U_2 = 2 / 6 = 1 / 3.$$

Here, the 4-ohm and 2-ohm resistors act as a potential divider, and U_2 is divided by 3 to provide U_1. Again, this is a ratio with no units.

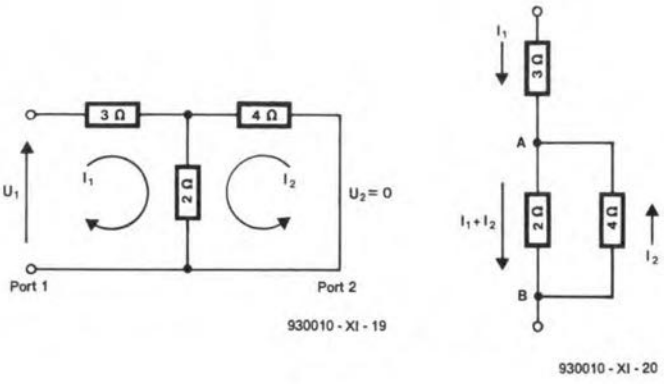


Figure 98

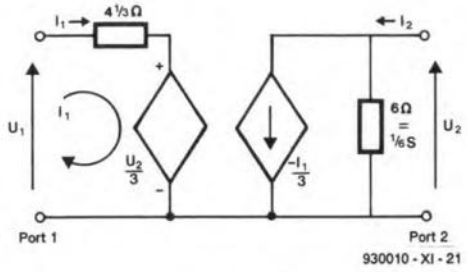


Figure 99

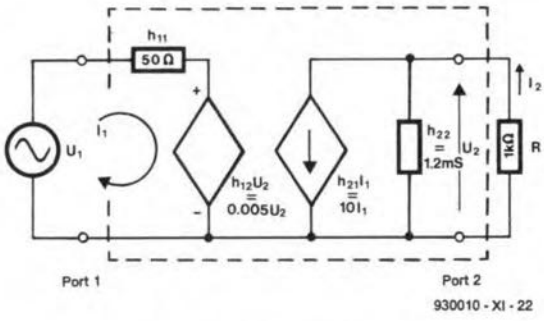


Figure 100

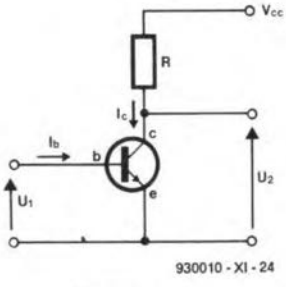


Figure 101a

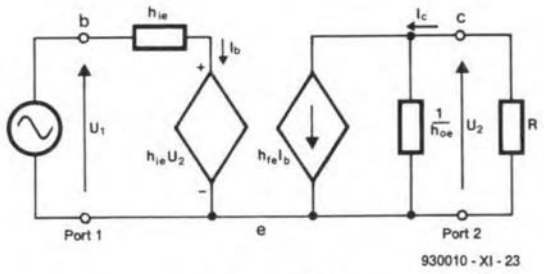


Figure 101b

From Eq. 76:

$$h_{22} = I_2 / U_2 = 1 / 6 \text{ S}.$$

This is the admittance of the 4-ohm and 2-ohm resistors in series; its unit is the siemens.

We now have all the parameters and can set up the model (**Fig. 99**). Use this to make predictions. For example, evaluate the currents if U_1 = 10 V and U_2 = 5 V. On the Port 1 side, the current through the resistor is the result of the pd across it, which is:

$$10 - h_{12}U_2 = 10 - U_2 / 3$$
$$= 10 - 5 / 3 = 8.333$$

$$\therefore\ I_1 = 8.333 / 4.333 = 1.923 \text{ A}.$$

On the Port 2 side, the current through the 6-ohm resistor (equivalent to 1/6 S admittance) is 5/6 A. The current from the controlled source is $-I_1 / 3 = -1.923 / 3 = -0.641$ A. I_2 equals the current through the 6-ohm resistor **plus** the current produced by the source, which, being negative, flows in the opposite direction to the arrow:

$$I_2 = 5 / 6 - 0.641 = 0.1923 \text{ A}.$$

The current gain of this network is $I_2 / I_1 = 0.1$.

This simple example has the merit that its results can be checked easily by mesh analysis of **Fig. 91**, with applied voltages of 10 V and 5 V. The reader may care to work this as an exercise, and confirm that the *h*-parameter technique gives the correct results.

Extending *h*-parameters

Consider the model of **Fig. 100**, the circuit details of which are not relevant for the moment. It receives input U_1 from a variable pd source and its output U_2 is fed to load resistor *R*. The *h*-parameters are marked on the figure. By Ohm's law:

$$I_2 = -U_2 / R = -U_2 / 1000 \quad [\text{Eq. 77}]$$

Also, from Eq. 76:

$$I_2 = h_{21}I_1 + h_{22}U_2$$
$$= 10I_2 + 0.0012U_2.$$

Substituting the value of I_2 from Eq. 77:

$$-U_2 / 1000 = 10I_2 + 0.0012U_2$$

$$\therefore\ I_1 = -(0.0012U_2 + U_2/1000)/10$$
$$= -U_2\,(0.0012 + 0.001) / 10$$
$$= -U_2\,(0.0022) / 10$$
$$= -0.00022U_2.$$

Substituting this value and the values of the *h*-parameters in Eq. 75:

$U_1 = -0.00022U_2h_{11} + h_{12}U_2$
$= -0.00022U_2 \times 50 + 0.005U_2.$
$\therefore\ U_1 / U_2 = -0.011 + 0.005$
$= -0.006.$

The pd gain of the network is the reciprocal of this:

$$U_2 / U_1 = -1 / 0.006 = -167.$$

That is, **the pd gain is –167**. The network is an inverting voltage amplifier. It has the features of a common-emitter amplifier based on an n-p-n bipolar junction transistor (**Fig. 101a**). In the figure we show a pd source U, but omit biasing resistors, which can be considered to be part of the pd source. Comparing the two parts of this figure, we see that I_1 is the base current I_b, while I_2 is the collector current, I_c. The h-parameters are given special subscripts to relate them to the operation of the transistor:

- h_{11} becomes h_{ie}, the input resistance;
- h_{21} becomes h_{fe}, the forward current ratio, or gain;
- h_{12} becomes h_{re}, the reverse feedback voltage ratio;
- h_{22} becomes h_{oe}, the output admittance.

The 'e' in each subscript refers to the fact that the transistor is in the common-emitter configuration. Each of these parameters is measurable for a given transistor, or can be obtained from a data sheet. h_{ie} and h_{fe} are measured with the transistor output short-circuited; h_{re} and h_{oe} are measured with an open-circuit input. Given these parameters, the behaviour of the amplifier can be predicted, provided that it is operating in the linear part of its range, and with small signals.

The values of h_{re} and h_{oe} for most transistors allow some simplification of the model. **Figure 102** shows a common-emitter amplifier with typical values for the h-parameters. We have omitted the controlled voltage source, because h_{re} is typically only 0.0001, with the result that the voltage source can usually be ignored. R is the load resistor in the collector circuit. In the model, we are specifying that the controlled current source is drawing the collector current through that resistor, ultimately from the negaive rail through the low impedance of the power supply. We can say this because

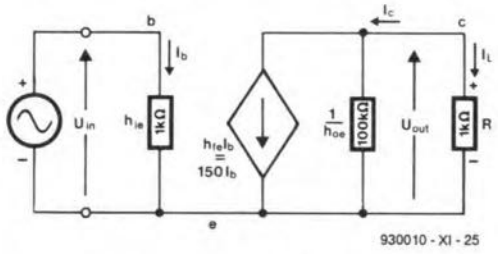


Figure 102

the collector current is virtually independent of supply voltage. The current is split between h_{oe} and R, which are in parallel. By the rules of current division:

$$I_L = -h_{fe}I_b \times \frac{1/h_{oe}}{1/h_{oe} + R}$$

$$= -h_{fe}I_b / (1 + h_{oe}R).$$

Current gain is

$$I_L / I_B = -h_{fe} / (1 + h_{oe}R_L)) \qquad \text{[Eq. 78]}$$

Given the values of **Fig. 102** ($h_{oe} = 10^{-5}$), the current gain is

$$-150 / (1 + 10^{-5} \times 10^3)$$
$$= -150 / 1.01 = -148.5.$$

This is a large current gain, as is typical of a common-emitter amplifier. The negative sign indicates that it is 180° out of phase with the input signal.

In practice, it is reasonable to simplify the model further without undue loss of precision. The output admittance is small (only a few microsiemens), so h_{oe} can usually be omitted, too. Given that h_{oe} is very small, the term $h_{oe}R$ can be omitted from Eq. 78, so that

$$\text{current gain} \approx -h_{fe} = -150.$$

Other characteristics of the amplifier are calculated in a similar way by making suitable assumptions and analysing the network with the use of techniques described in previous parts. Equations may become involved, but the mathematics is simple. For example, to calculate voltage gain, we first consider the left-hand mesh of **Fig. 102**:

$$U_{in} = h_{ie}I_b.$$

In the right-hand mesh, ignoring h_{oe}:

$$U_{out} = -h_{fe}I_b R.$$

Voltage gain $= U_{out} / U_{in}$
$= -h_{fe}I_b R / h_{ie}I_b$
$= -h_{fe}R / h_{ie}.$

In **Fig. 102**, the voltage gain is

$$(-150 \times 10^3) / 10^3 = -150.$$

The output signal is 180° out of phase with the input signal.

Other amplifiers

The models for common-base and common-collector amplifiers have the same layout as that of the common-emitter amplifier. The subscripts on the parameters end in 'b' or 'c', but otherwise the diagrams are the same. The typical values of the parameters are not necessarily the same as in the common-emitter model. For example, the absolute value of h_{fb} is a little less than unity, typically –0.99. Together with the fact that h_{ob} is exceedingly low (a few hundred nanosiemens, equivalent to over 1 MΩ), this means that current gain is very slightly less than 1 in any practical common-base amplifier. Also, since h_{fb} is negative, the output signal is in phase with the input signal. Typically, h_{ib} is small, around 20–30 Ω.

In the common-collector (emitter-follower) model, h_{ic} is large (1 kΩ or more), and h_{fc} is typically –100, giving large current gain with no phase shift (one of the main purposes of using a c-c amplifier). h_{rc} is 1, giving unity voltage gain, as required in an emitter follower, while h_{oc} has a moderate value.

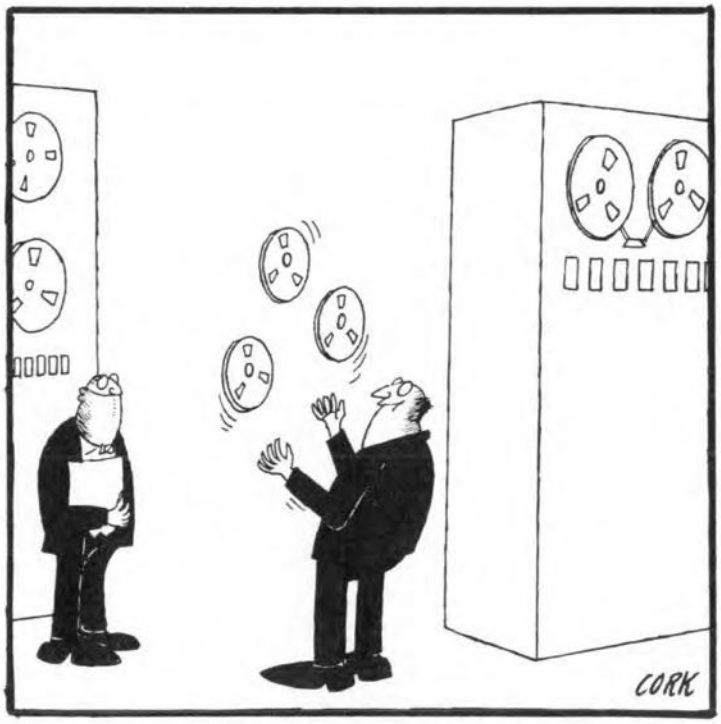
TO BE CONTINUED

Test yourself

1. Calculate the z-parameters for **Fig. 91**, given $R_1 = 10\ \Omega$, $R_2 = 14\ \Omega$ and $R_3 = 6\ \Omega$.
2. Calculate z_{11} and z_{21} for **Fig. 95a**, given that $R_1 = 10\ \Omega$, $R_2 = 12\ \Omega$, $C = 1\ \mu F$ and $\omega = 10^4$ rad/s. What is the voltage gain of this network?
3. In an unknown quadripole circuit, $U_1 = 1$ V, $U_2 = 3$ V, $I_1 = 20\ \mu A$ and $I_2 = 2.5$ mA. Calculate the h-parameters.

Answers to Test yourself (Part 10)

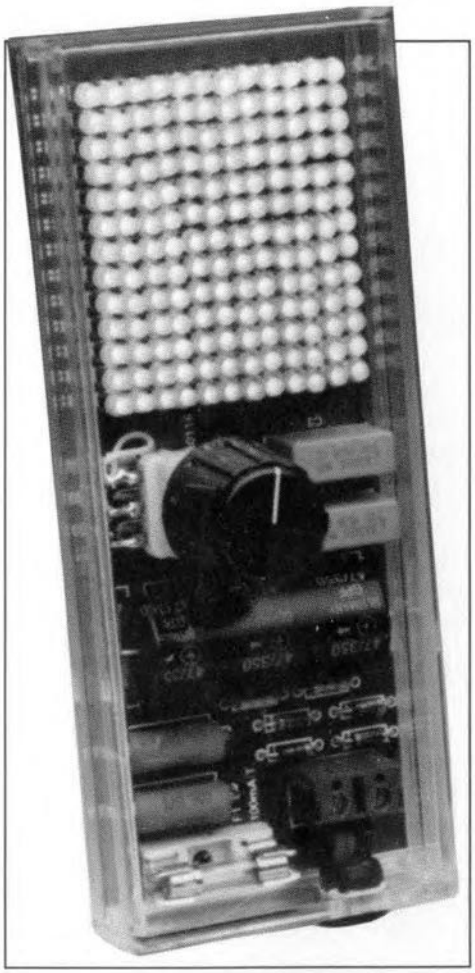
1. $I_1 = 0.56$ A; $I_2 = 0.04$ A; $I_3 = 0.32$ A. In 3 Ω: 0.9408 W; in 2 Ω: 0.0032 W; in 4 Ω: 1.0816 W; in 1 Ω: 0.0576 W; in 7 Ω: 0.7168 W. 4 V source: 2.24 W; 2 V source: 0.56 W. Total for resistors = total for sources = 2.8 W.
2. 40 W.
3. (a) 0.547 W; (b) 0 W.
4. 1.627 mW.
5. 12 mW.
6. $X_L = \mathbf{j}6$; $X_C = -\mathbf{j}6$. Power factor = 0.944.



PHOTOGRAPHIC WORKSHOP LIGHT

This article describes a low-cost alternative to the normally pretty expensive lamp used to light the photographic darkroom. It consists of an array of yellow LEDs (light-emitting diodes), which emit a wavelength to which (colour) photographic paper is highly insensitive.

Design by F. Stolpe



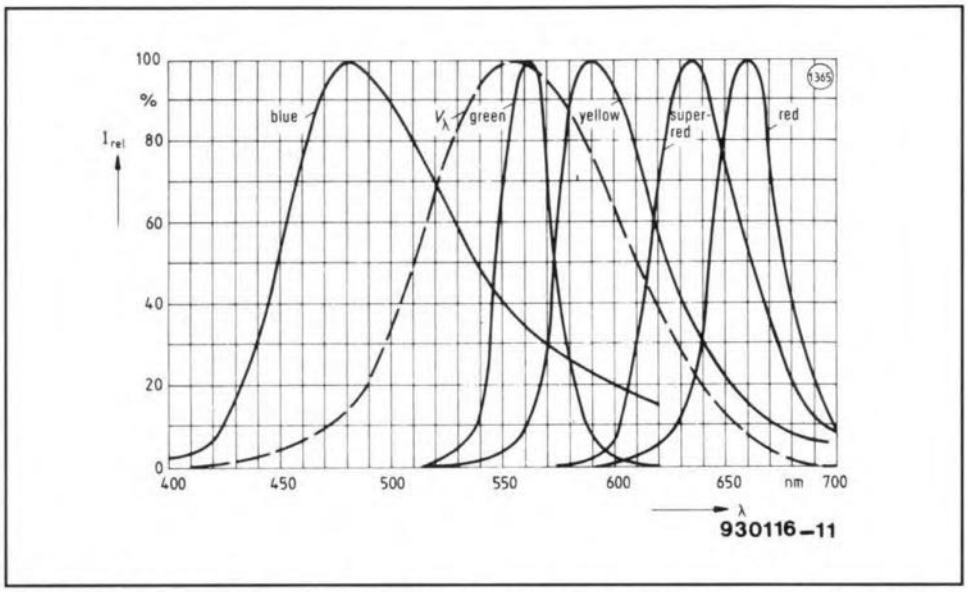


Fig. 1. Light spectrum as emitted by different colour LEDs (source: *Siemens Optoelectronics Databook 1990*).

AS far back as the days of black-and-white photography, photographic paper was already made insensitive to light of a certain colour. This was done to enable the photographer to see what he was doing in the darkroom while taking the photographic prints through the developing process. The colour red was chosen, and a normal bulb was painted red because the exact colour was not so important. With the introduction of colour photography things became a little more difficult, because the photographic paper has to be sensitive to all colours in the visible spectrum. None the less, this type of paper has been made insensitive to one specific colour, of which the wavelength is fairly accurately defined between 580 nm and 600 nm (nm = nanometres; 10^{-9} metres). This wavelength was chosen because a special type of sodium lamp has two spectral lines in this range, one at 588.99 nm, and one at 589.59 nm. The disadvantage of this lamp is its rather high price. Less expensive alternatives to the sodium lamp are normal bulbs with a narrow-band filter. Unfortunately, these lamps still cost well over £20.

The wavelength of light emitted by yellow LEDs is typically around 590 nm (see **Fig. 1**). The spectrum of the LED lamp is not as narrow as that of a sodium lamp, but that is of little consequence since this disadvantage also applies to the filter lamp. The width of the spectrum emitted by a yellow LED depends on the type and manufacturer. That is why you have to do an exposure test using the LED lamp and a sample strip of photographic paper to make sure that the lamp has no effect on the paper (see further on in this article).

Another problem is the low light intensity produced by an LED (10 to 20 milli-candela for normal LEDs, and about 100 milli-candela for high-efficiency LEDs). Fortunately, this problem is simple to solve by using a large number of LEDs.

The LED lamp

Obviously, to keep the cost of the LED lamp below that of a ready-made lamp, the number of components used (apart from the LEDs) must be kept as small as possible. Also, the design should be based on commonly available, inexpensive parts. With this in mind, it will not come as a surprise that a mains transformer has been omitted from the design. As shown by the circuit diagram in **Fig. 2**, it is possible to use the rectified mains voltage if a maximum of 156 LEDs are connected in series. The number of LEDs to be connected in series is determined by their colour and maximum forward voltage drop (see **Table 1**). Here, the darkroom demands yellow LEDs; the other colours given in the table are for different applications, of which more further on.

As already mentioned, the LEDs are supplied directly from the mains voltage, which means that you have to pay special attention to insulation and safety. The mains voltage (live and neutral) is connected to PCB terminal block K1, and arrives at a bridge rectifier, D1-D4, via fuse F1. The circuit is connected to the mains via a PCB

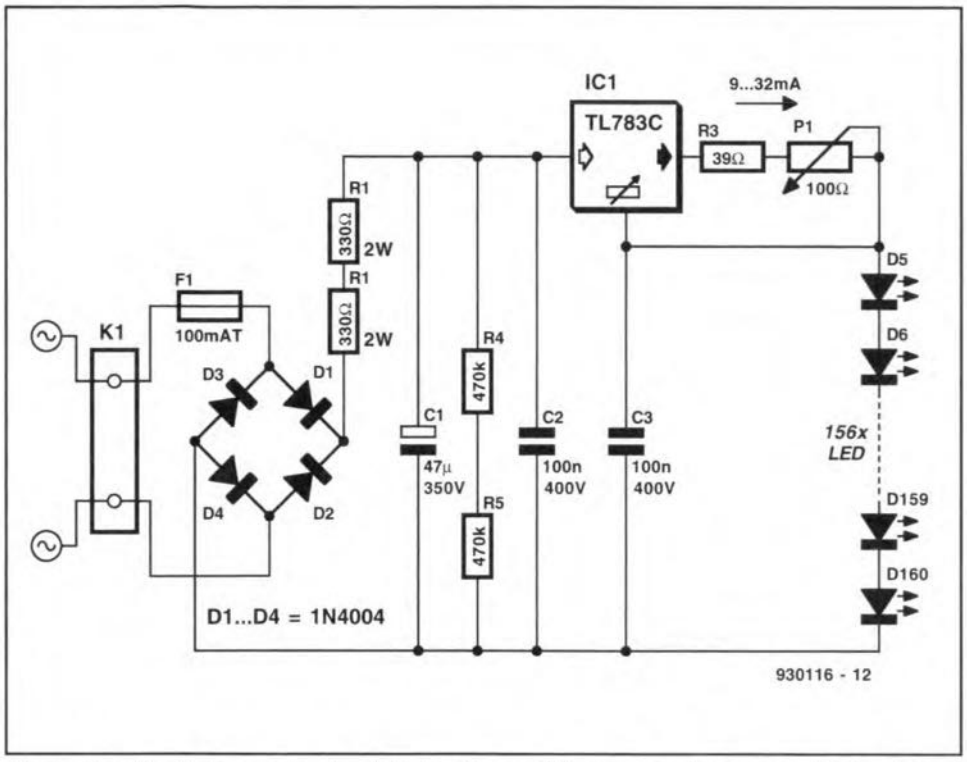


Fig. 2. The circuit diagram is simplicity itself: a rectifier, a current source and LEDs, lots of LEDs.

mount terminal block because that is the simplest way of connecting the mains cable in a safe manner. The fuse automatically removes the mains voltage from the circuit in the event of a fault, thus eliminating a fire risk. Resistors R1 and R2 limit the power-on surge current through C1 to about 0.5 A. This is done to prevent unnecessary burning out of the fuse. The voltage across C1 is about 335 V, which equals the peak value of the mains voltage (240 V_{rms} in the UK). The smoothing capacitor, C1, is shunted by resistors R4 and R5, which remove the capacitor's charge in a few seconds after the lamp is switched off. Of course, the LEDs also help to do this, but R4 and R5 ensure that no dangerous voltage remains across C1 when the circuit is switched off. R4 and R5 may **not** be replaced by a single 1-MΩ resistor. This is because most small resistors (0.25-W and 0.33-W types) are rated to only 200 V, which is too low for the 335 V which exists across C1. By connecting two identical resistors in series, the voltage across C1 is distributed equally, so that it is possible to use two ordinary low-power resistors.

Voltage regulator IC1 is connected as a current source. This is based on the tendency of the device to maintain a voltage difference of 1.25-V between its control input and output. Consequently, the voltage across R3 and P1 is always 1.25 V. The indicated values of R3 and P1 allow the current drawn by the LEDs to be set to a value between 9 mA and 32 mA with the aid of P1.

Since IC1 keeps the current through the LEDs constant, variations of the mains voltage and/or the forward voltage of the LEDs have no effect on the light intensity produced by the lamp. It does, however, affect the voltage across IC1. In particular, the voltage drop across the LEDs is a considerable factor, which is not surprising in view of the number of LEDs used. A deviation of 0.1 V per LED, for instance, gives a total error of more than 10 V. Such deviations are quite common, see the data in **Table 1**. Moreover, the voltage across IC1 varies appreciably as a function of the lamp intensity setting (with P1). To prevent this from causing an overload condition in the regulator, a TL783C is used instead of the perhaps more familiar LM317. The TL783C is capable of withstanding a voltage difference of 125 V between its input and output. By comparison, the 35 V specification of the LM317 is on the low side for this application.

Colour	Forward drop typ.	max.	Max. number
yellow	2.2	2.6	130
green	2.2	2.6	130
red	1.6	2	156
blue	4	8	65
IR	1.5	2	156

Table 1. Forward voltage of different types of LED, and the maximum number that may be accommodated on the printed circuit board.

Construction

The artwork designed for the printed circuit board used to build the LED lamp is shown in **Fig. 3**. To be able to fit the board into the transparent plastic enclosure stated in the parts list, notches have to be cut in the edges, at about the height of C1. Also, a rectangular clearance has to be cut in which C1 is seated. This reduces the mounting height of C1, and enables the enclosure to be shut. The mains cable is fitted with a strain relief clamp at the inside of the enclosure.

The LEDs

Each number of LEDs given in **Table 1** is rounded off to a multiple of 13 so that only whole rows of LEDs are fitted on to the board. Non-used rows must be bridged start-to-end by a wire. If you want to fit as many LEDs as possible, make sure that the voltage drop across the LED array remains below 290 V.

If you mount fewer LEDs, the voltage across IC1 rises. To prevent the voltage drop exceeding 125 V, the voltage across the LEDs may not drop below 210 V. With some colours, the maximum number of LEDs that can be fitted on to the PCB (156) is given, instead of the number the circuit would be capable of driving. If you choose not to build the circuit on the indicated printed circuit board, the actual maximum number of LEDs that may be used is fairly simple to calculate.

The circuit is, in principle, designed for yellow LEDs. When another colour is used, the number of LEDs that can be fitted changes, as indicated in **Table 1**. Note, however, that the current supplied by IC1 is geared to 'normal' LEDs — by contrast, the maximum current that may be used for low-power or high-efficiency LEDs is much lower. In that case, R3 and P1 must be changed (I=1.25/(R3+P1)). The reverse applies to infra-red LEDs, which require a higher current (typically around 100 mA).

The above goes to show that the circuit is eminently suited to driving all kinds of LED. Before choosing a particular colour and type, however, it is wise to check its typical operating current, and the voltage drop at different currents.

Apart from a darkroom light, there are a number of other applications of the LED lamp. Many possibilities are created just by changing the shape of the LED array. Infra-red LEDs allow the lamp to be used as a spotlight for infra-red photography, or to assist a CCD (charge-coupled device) camera when making pictures or recordings in the dark, for instance, of animals which are active during the night only.

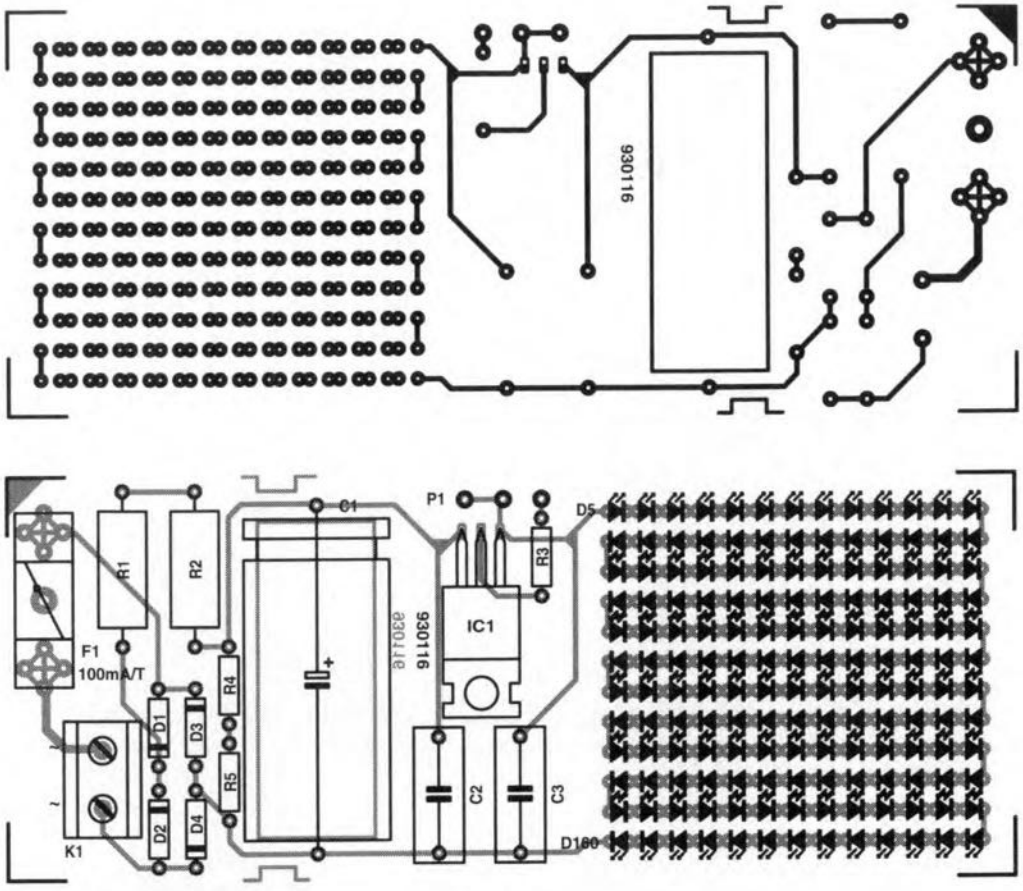


Fig. 3. The size of the PCB matches the inside dimensions of a transparent Type 'Profi' enclosure from Heddic.

COMPONENTS LIST

Resistors:

2	330Ω 2W	R1;R2
1	39Ω	R3
2	470kΩ	R4;R5
1	100Ω potentiometer w. plastic spindle	P1

Capacitors:

1	47µF 350V	C1
2	100nF 400V	C2;C3

Semiconductors:

4	1N4004	D1-D4
156	3mm LED (max. number, see Table 1)	D5-D160
1	TL783C	IC1

Miscellaneous:

1	2-way PCB terminal block, pitch 7.5mm	K1
1	PCB mount fuseholder w. 100mA slow fuse	F1
1	Enclosure, e.g., Heddic Profi	

Exposure test

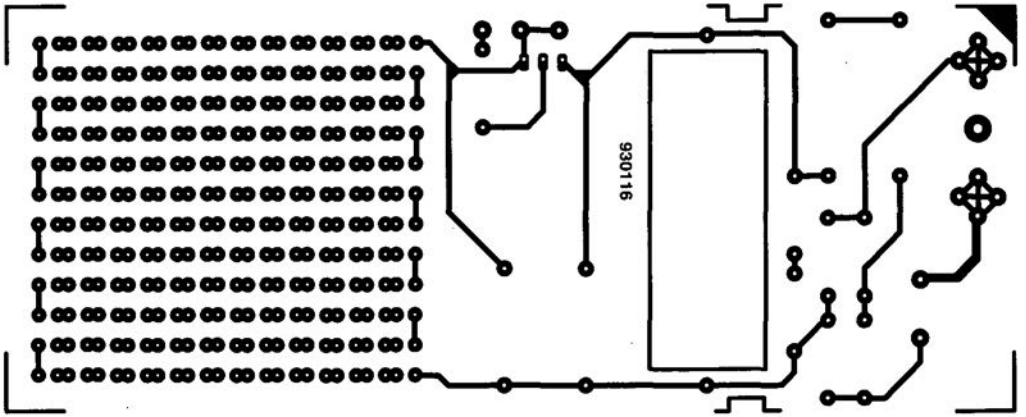
Before actually using the LED lamp as a darkroom light, it is necessary to make sure that it does not affect the photographic paper. Before the test, mount the lamp at the desired position in the darkroom. Next, put a piece of photographically sensitive paper where you would normally be working, and then closest to the lamp. A part of the paper is covered, and the other, 'exposed' for two minutes to the light emitted by the LED lamp. Next, the paper is developed in the usual way. If everything is in order no difference may be visible between the exposed and the unexposed part of the paper. If differences are noticed, the intensity of the lamp must be reduced with P1, or different types of yellow LED must be fitted. In both cases, the exposure test must be repeated.

A simpler alternative to the above test is to connect a few LEDs in series with a resistor, power them from a 9-V battery, and suspend them above the photographic paper. After developing the paper you have a clear indication of the LED type that has the smallest effect.

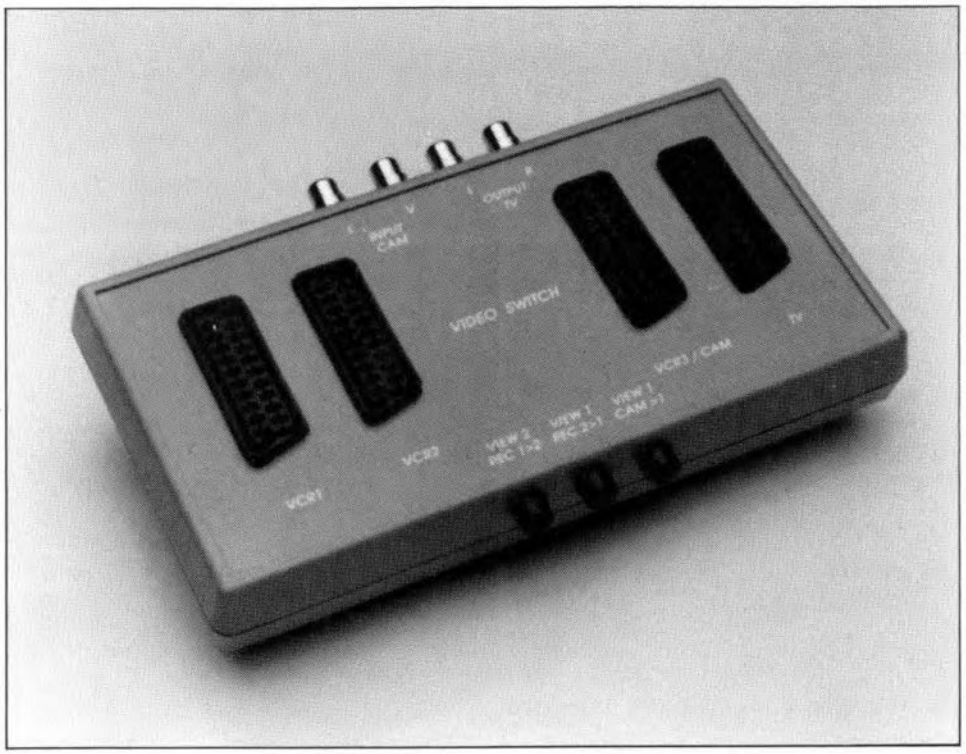
■

LIGHT-EMITTING DIODES (LEDs)

Like the normal diode, the light-emitting diode, or LED, consists of a piece of semiconductor material with an 'n' and a 'p' layer. If a forward current flows through the semiconductor material, the re-combination of electrons in the barrier junction between the 'n' and the 'p' layer gives rise to photon emission; in other words, light is emitted. This form of light emission is called p-n barrier luminescence. The same effect also occurs in normal germanium and silicon diodes. In these semiconductor materials, however, the p-n barrier luminescence efficiency is so small that it can not be put to practical use. The semiconductor material gallium-arsenide (GaAs), however, is far better suited to producing LEDs — a high intensity is achieved at fairly low currents already (a few mA).
LEDs emit virtually monochromatic light, which means that all light energy is contained in a narrow band of the spectrum. A GaAs LED produces light with a wavelength of 868 nm (red light). Similarly, other semiconductor materials are used to generate colours such as green, orange and even blue.


930116

SCART SWITCHING BOX



Now that the camcorder is here to stay as the mobile complement to the trusty video recorder, a problem has come about: selecting between different video signals that can be applied to the SCART input on the TV set. This article describes a simple three-input switching unit for video sources with mono sound. Provision has been made for copying between video recorders connected to the SCART switching box.

Design by L. Pijpers

SOME twenty to thirty years ago, the situation with audio equipment was, in a way, similar to that as it exists for video equipment today. In the old days, one had a radio with one input for a record player ('pickup'). Today's 'video' equivalent would be a TV set and one video recorder. In the course of time, the tape recorder appeared on the scene, and what was once known as a radio set gradually 'fell apart' into a tuner and an amplifier. This gave rise to a number of switching options required to connect the signal sources to the amplifier and/or the available recorders. Although a video installation with a switching layout similar to modern hi-fi sets will not be with us for a few years, it is not unusual for video and TV lovers to have one or two video recorders and a camcorder. Unfortunately, a TV set with two video inputs is not a complete solution, since it does not allow copying between the recorders. The SCART switching box described in this article enables you to enjoy all switching possibilities that you have come to appreciate from your audio equipment, for video!

Block diagram

The SCART selector could not be simpler: switches are used to establish and break connections — see the block diagram in **Fig. 1**. The switches used here are locking buttons which are coupled such that only one switch can be pushed in at a time. The advantage of the switch unit is that it allows you to determine the number of positions of the assembly (1 to 10), while the individual switches are available with 2, 4, 6, 8 and 10 change-over contacts. In this respect, the push-button assembly is much more flexible than the perhaps more usual rotary switch. Moreover, the switch assembly may be mounted directly on to the printed circuit board, which eliminates wire links between the switches and the PCB. On the down side, the push-button assembly is more difficult to fit into a front panel than a rotary switch, which requires only one hole to be drilled.

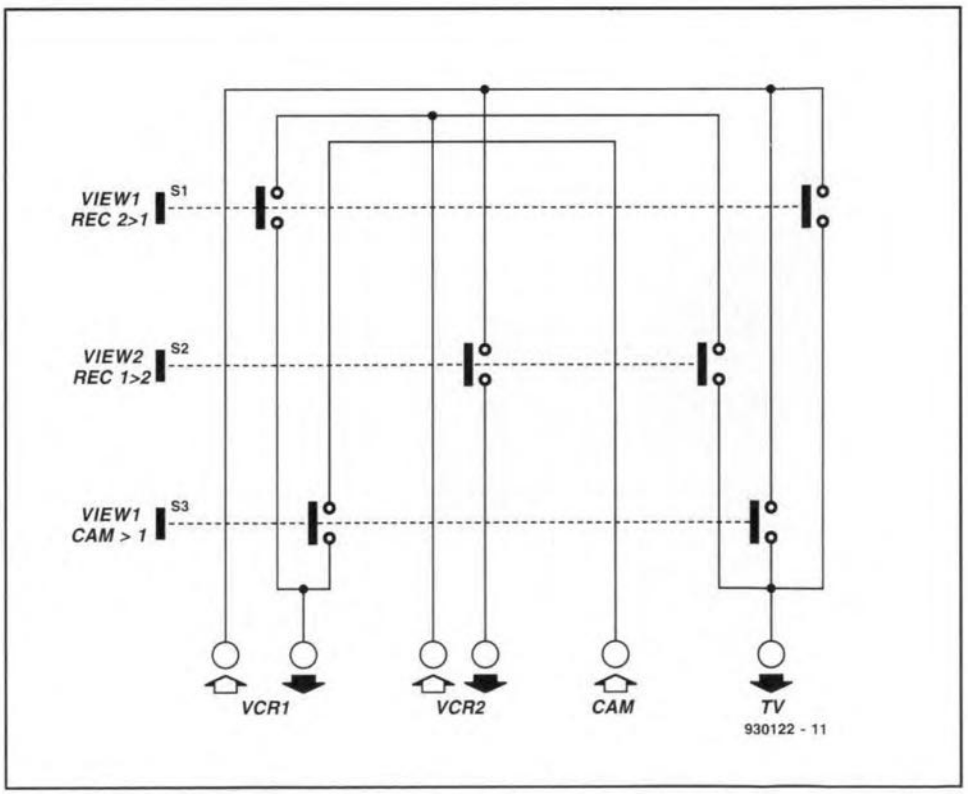


Fig. 1. Block diagram showing how the connections between the equipment are established and broken.

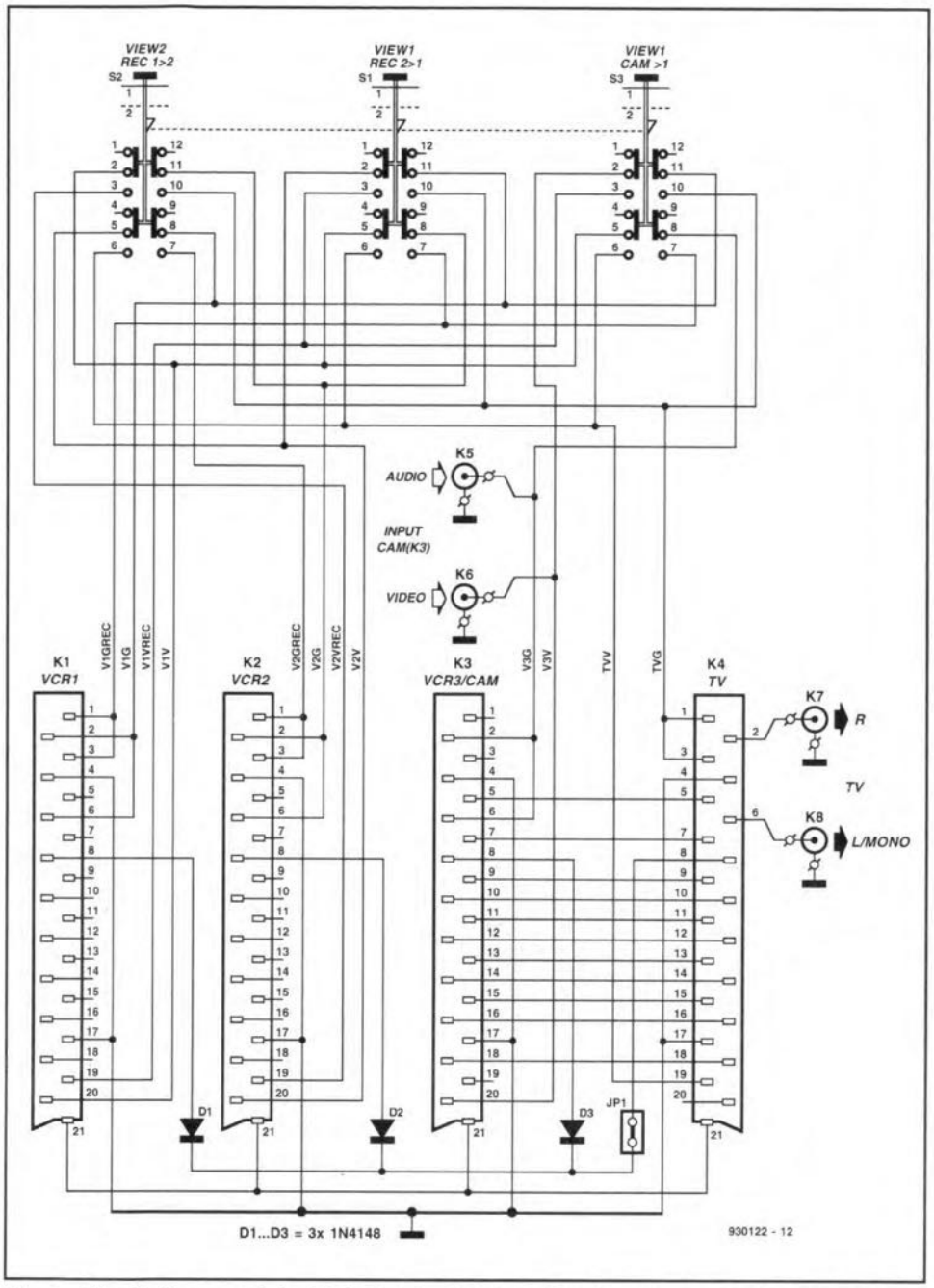
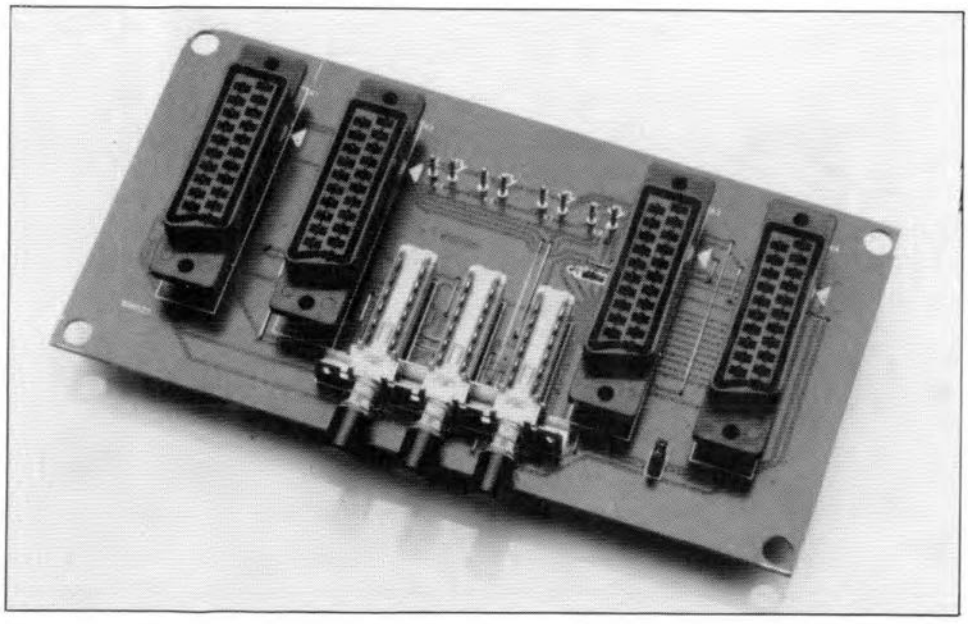


Fig. 2. Circuit diagram of the SCART switching box. The number of components has been kept as small as possible.



The circuit

The circuit diagram of the SCART switching box is shown in **Fig. 2**. To keep the circuit as simple as possible, it was decided not to wire the switching box for S-VHS or Hi8 and stereo sound. This limitation reduces the switching work to one video and one audio signal per connection. Actually, since the audio and video links run side by side, **Fig. 2** is just a double implementation of the block diagram in **Fig. 1**.

To increase the practical possibilities of the SCART switch, the camcorder connection (phono sockets K5 and K6) is connected in parallel to SCART socket K3, to which a third recorder may be linked. Note, however, that this third recorder can be used in 'play' mode only — K3 does not supply a signal that can be used for recording. This makes the K3 socket ideal for connecting a video player.

Most video recorders supply a switching signal which enables a TV or monitor to automatically change to the video signal supplied by the recorder. This switching signal is conveyed via the SCART link between the recorder and the TV. Diodes D1, D2 and D3 form an OR function for the three switching signals, and prevent the recorders from interfering with one another. Remove jumper JP1 if you prefer to switch your TV to 'audio/visual' (AV) manually.

As a finishing touch, the TV sound which arrives on K4 is connected to two phono sockets (since it was extremely simple to realize, this has been done in stereo). In this way, the TV sound is readily connected to the audio rack.

Construction

The layout of the printed circuit board designed for the SCART switching box is given in **Fig. 3**. Construction is simple since the circuit consists mainly of switches and SCART sockets. Start by fitting the wire links, the diodes, the jumper and the terminal pins to which the phono sockets are connected. Next, fit the SCART sockets on to the board. These sockets should be types with **straight** solder pins (angled pin types are more commonly found, but unfortunately can not be used here).

The push-button block has to be assembled before it can be mounted on to the board. Fortunately, assembling the unit is relatively straightforward and almost self-evident from the construction of the individual parts. For the sake of clarity, the assembly is shown in **Fig. 4**. The function of the drivebar spring (part FRV) may not be immediately evident. This tiny but es-

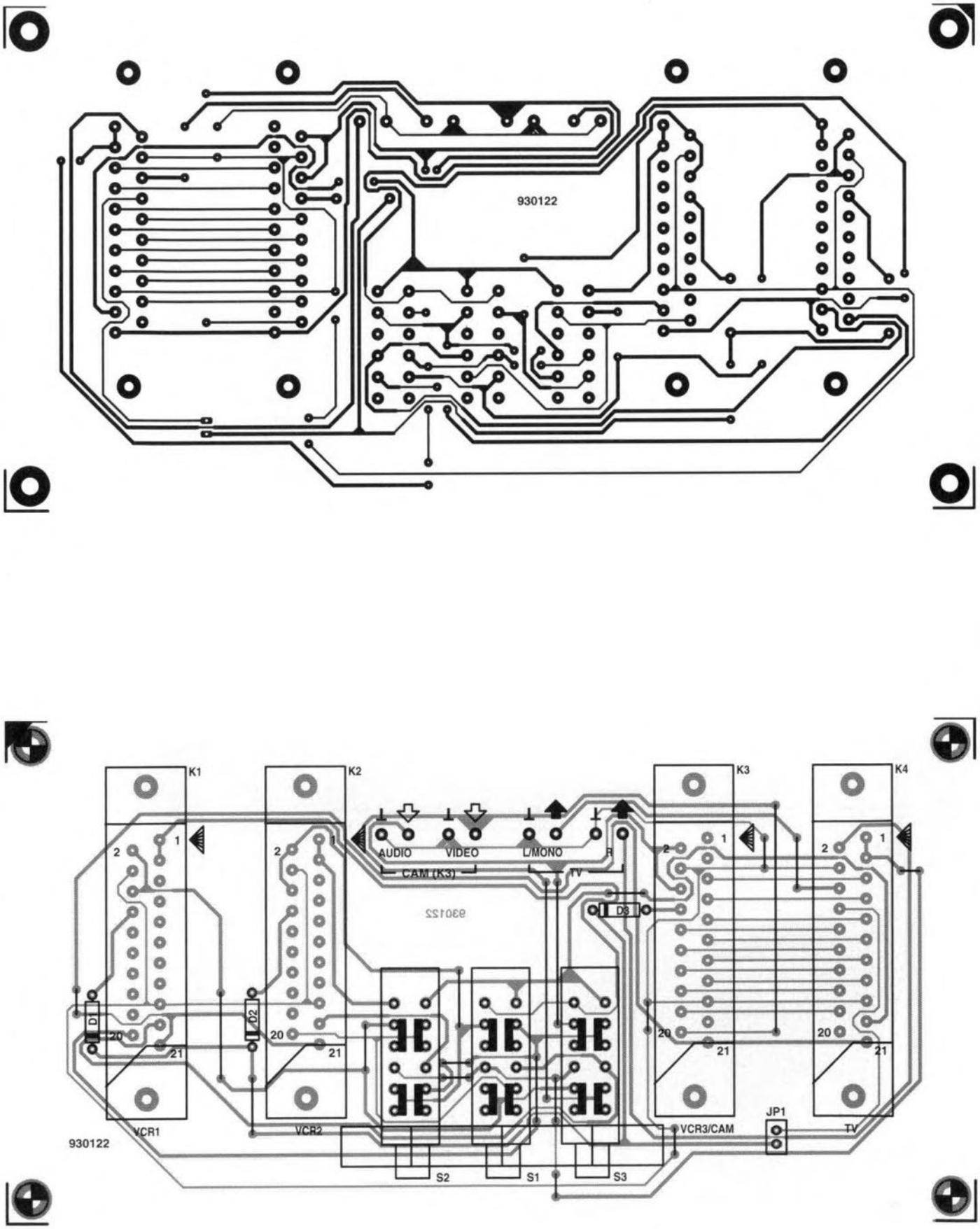


Fig. 3. Printed circuit board for the SCART switch (available ready-made through the Readers Services).

COMPONENTS LIST

Semiconductors:

3 1N4148 D1;D2;D3

Miscellaneous:

4 PCB mount SCART socket with straight solder pins K1-K4

4 Panel mount cinch socket K5-K8

3 Coupled switches
Components:
3 off 4-way switch F-4U/EE FS4
1 off front frame 3F17,5 FF37
1 off drive bar 3F17,5 FR37
1 off drive bar spring FRV
3 off button 8.8mm dia, black FG0
(ITT/Schadow switches [1])

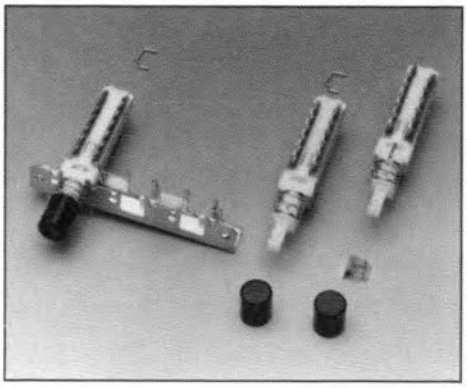
1 Jumper 0.1 in JP1

1 Enclosure o.d. 102×191×29mm, e.g. Pactec [2] type HPLkit.

1 Printed circuit board 930122 (see page 110).

[1] ITT MultiComponents (0753) 824131.
[2] OK Industries Ltd. (0703) 650055.

sential part serves to secure the drive-bar which locks and unlocks the switches. The spring is fitted on to the right-hand side (viewed from the front side) of one of the switches. As shown in the drawing, the T-shaped part of the spring is pushed into the slot in the corner between the top and the side of the switch. Next, secure the switch just like the other two by bending the protruding cams to the front and to the back. The switch assembly is then ready to be mounted on to the printed circuit board. The push-buttons may be fitted later when the completed PCB has been mounted into an enclosure. The centre-to-centre distance of the three holes that must be drilled for the push-buttons is 17.5 mm. ■



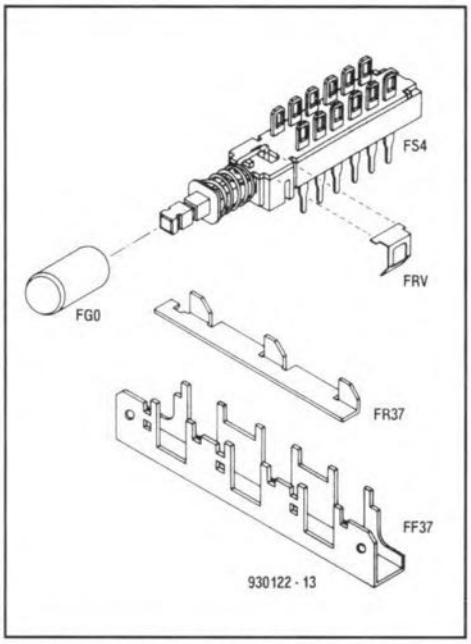


Fig. 4. Illustrating the assembly of switches S1, S2 and S3.

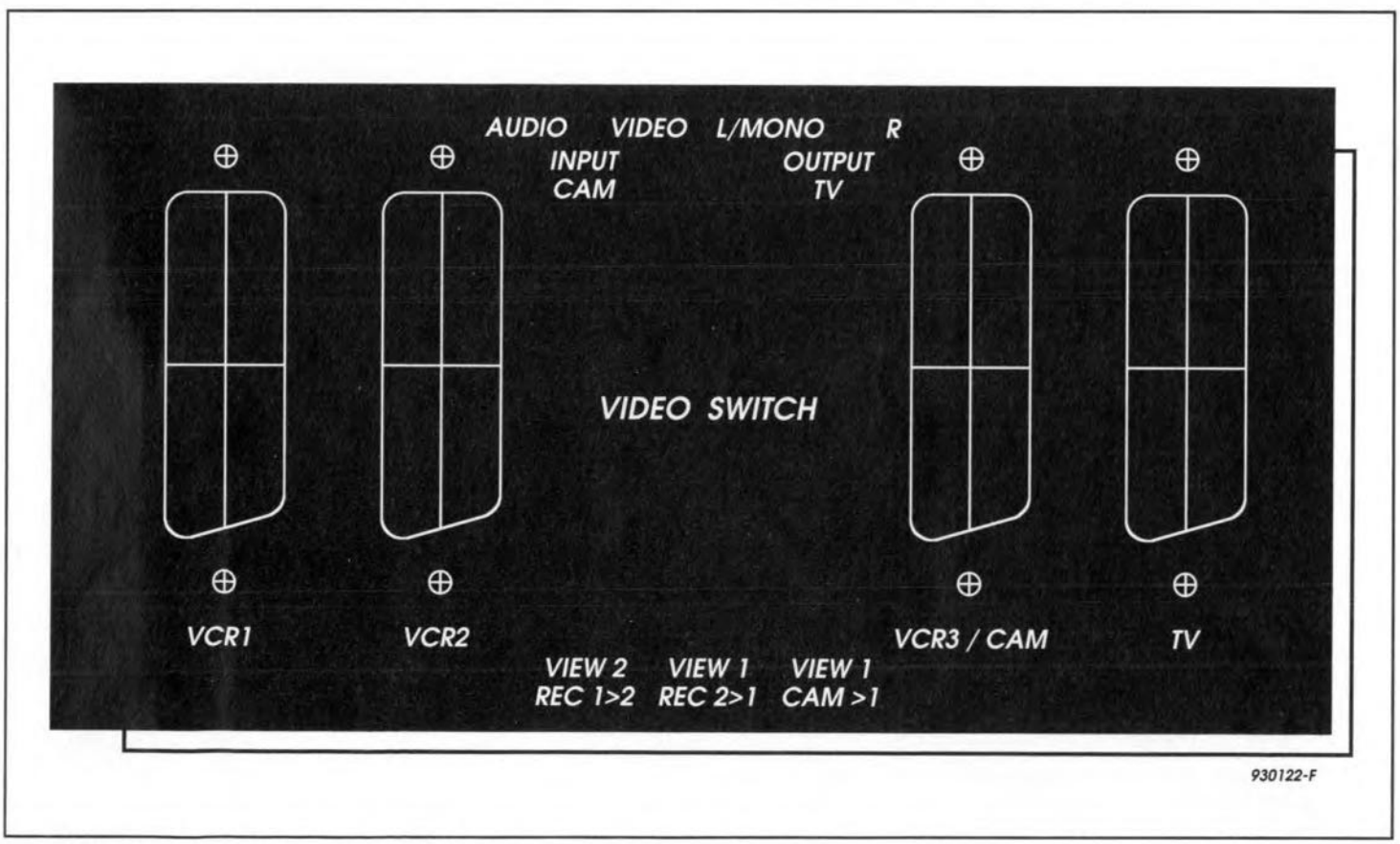
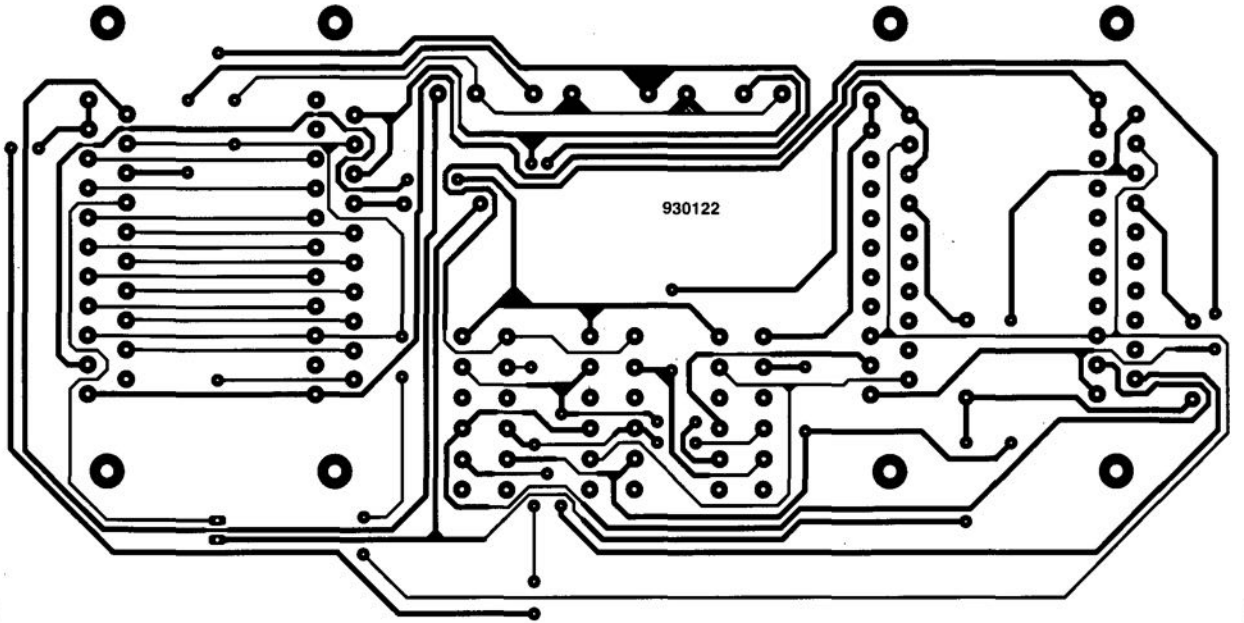


Fig. 5. Suggested front panel layout shown at true size (not available ready-made).


930122

amplifier?). The output pulse is picked up by a microphone and fed back into the IMP where it is digitized and then fed into an IBM (compatible) computer via the printer port. The IMP software then analyses the input via Fourier transforms and outputs the results on to the computer screen in graphical form in the shape of amplitude and phase response curves. Full control is via the PC. The amplifier output can be sampled via a probe to correct for errors in the pulse spectrum and amplifier response.

IM P allows the collection and analysis of 12-bit analogue data up to 4,095 samples in length and sample rates are selectable at either 61.441 kHz or 1.92 kHz which, along with the internal filtering, allows measurements from several hertz to 20 kHz.

Further information from Falcon Acoustics Ltd, Tabor House, Norwich Road, Mulbarton, Norfolk NR14 8JT, England. Telephone +44 (0)508 78272; fax +44 (0)508 70986.

CORRECTIONS

DIGITAL DIAL (January 1994)

An attentive reader has drawn our attention to the fact that the digital dial can not be used in conjunction with the receiver illustrated (a Yaesu Type FRG-7) since the IF of that receiver is much too high for the dial. Sorry for that oversight! [Editor]

VHF/UHF TUNER (Oct/Nov 1993)

The tuner module used in this design is no longer in production with Philips and its availability will thus become a problem. Fortunately, the Type UV916H is an excellent alternative. The snag is, however, that this unit is slightly smaller than the UV816, so that the antenna connector no longer protrudes from the enclosure. This can be overcome by terminating the antenna cable into a coaxial plug and making the entrance hole slightly larger. Moreover, one of the two earth tags of the UV916H must be connected at a different position.

LETTERS

SCART SWITCHING BOX
(December 1993)

I have a few problems with this project, which I believe have to do with the connections. Pin 1 of one connector is linked to pin 2 of the other. The same is true of pins 3 and 19, which are linked to pins 6 and 20 respectively. All other pins are interlinked as one would expect, i.e., pin 5 to pin 5, pin 10 to pin 10, and so on.
L. Bastiaenssen

In a SCART cable, the wires for the video and audio connections are always crossed. That is why the video output (pin 19) at one end of the cable is linked to the video input (pin 20) at the other end. This arrangement ensures that the input of one piece of equipment is always connected properly to the output of another. There is, therefore, nothing wrong with your cable.

*Note that two pieces of equipment must never be connected simultaneously to K_3 and K_5/K_6. Use SCART connector K_3 **or** the phono plugs K_5/K_6, but not both at the same time!* [Editor]

PRECISION CLOCK FOR PCs
(November 1993)

I have encountered a problem with the Precision clock for PCs. I have an IBM (compatible) PC486 and have, as stated in the article, complemented the CONFIG.SYS file with the following (last) line:
DEVICE C:\MSDOS\DCFCLOCK.SYS.

I should be pleased if you would tell me:
1. Whereto should the files of the software provided (DCFCLOCK.ASM, DCFCLOCK.DOC and DCFCLOCK.SYS be copied? To the root, the MSDOS or a separate directory?
2. Once the files have been loaded, how is the program called up to initialize the driver and to fill the options P, I, S, B and D?
(M. Meersschaut)

The file DCFCLOC.ASM is the assembler listing of the program, which you no longer need (it is of interest only to dyed-in-the-wool programmers). The file DCFCLOCK.DOC contains the instructions for the program, which you can read with a word processing program. It is not necessary to store this file on a hard diksk.

The only program that you need to copy to the hard disk is DCFCLOCK.SYS. Place this file in the directory containing the DOS commands (e.g., C:\DOS). Add a line that indicates where the computer can find that program to CONFIG.SYS (in C:\), e.g. DEVICE = C:\DOS\DCFCLOCK.SYS. Other suffixes may be added for changing certain settings (see DOC file), but even without these the system should work correctly.

Note, however, that the receiver circuit must be connected to the COM port 2 and that the computer must be restarted after the software has been installed. The program will then automatically set the correct time in the internal clock of the PC every minute.

[Editor]

CHOOSING COMPONENT VALUES FOR *L-C* RESONANT TANK CIRCUITS

Resonant 'tank' circuits consist of combinations of inductance (*L*) and capacitance (*C*) elements configured in such a manner that a single frequency — or more correctly a very narrow band of frequencies — is selected, while frequencies removed from the selected frequency are rejected.

By Joseph J. Carr

THE selection of a specific frequency occurs when the inductive reactance ($+X_L$) and capacitive reactance ($-X_C$) have equal magnitude, so therefore cancel each other. **Figure 1** shows two forms of *LC* resonant tank circuit, and a plot of impedance versus frequency. The parallel resonant form is shown in **Fig. 1a**, while the series resonant form is shown in **Fig. 1b**. The following rules apply to these forms (see **Fig. 1c**):

1. a parallel resonant circuit has a maximum impedance at its resonant frequency (F_0); and
2. a series resonant circuit has a minimum impedance at its resonant frequency (F_0).

In some cases, one of these types is clearly preferred over the other, but in other cases either could be used if it is used correctly. For example, in a wave trap — i.e., a circuit that prevents a particular frequency from passing — a **parallel resonant circuit in series with the signal line** will block its resonant frequency while passing all frequencies removed from resonance; a **series resonant circuit shunted across the signal path** will bypass its resonant frequency to common (or 'ground'), while allowing frequencies removed from resonance to pass.

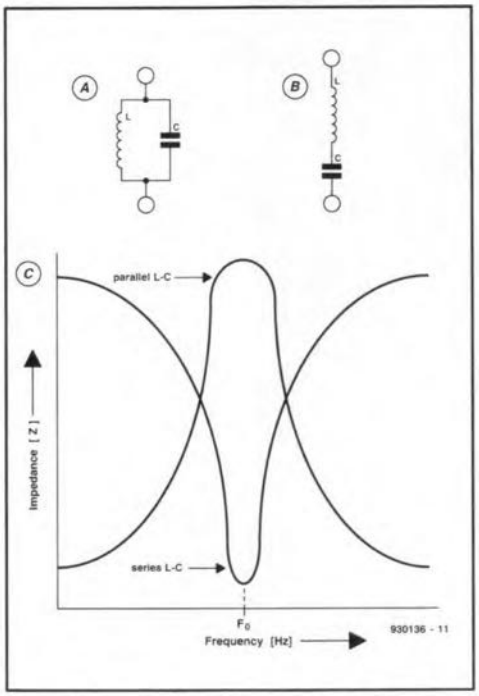


Fig. 1. a) Parallel resonant tank circuit; b) series resonant tank circuit; c) impedance-vs-frequency curves for series and parallel tank circuits.

LC resonant tank circuits are used to tune radio receivers; it is these circuits that select the station to be received, while rejecting others. A superheterodyne radio receiver (the most common type) is shown in simplified form in **Fig. 2**. According to the superhet principle, the radio frequency being received (F_{RF}) is converted to another frequency, called the **intermediate frequency** (F_{IF}), by being mixed with a **local oscillator** signal (F_{LO}) in a non-linear mixer stage. The output of the untamed mixer would be a collection of frequencies defined by:

$$F_{IF} = mF_{RF} \pm nF_{LO} \qquad (1)$$

Where m and n are either integers or zero. For the simplified case which is the subject of this article, only the first set of products (m=n=1) are considered, so the output spectrum will consist of F_{RF}, F_{LO}, $[F_{RF} - F_{LO}]$ (difference frequency), and $[F_{RF} + F_{LO}]$ (sum frequency). In older radios, for practical reasons the difference frequency was selected for F_{IF}; today, either sum or difference frequencies can be selected depending on the design of the radio.

There are several *LC* tank circuits present in this notional superhet radio. The antenna tank circuit (C1-L1) is found at the input of the RF amplifier stage, or if no RF amplifier is used it is at the input to the mixer stage. A second tank circuit (*L2-C2*), tuning the same range as *L1-C1* is found at the output of the RF amplifier, or the input of the mixer. Another *LC* tank circuit (*L3-C3*) is used to tune the local oscillator; it is this tank circuit that sets the frequency that the radio will receive.

Additional tank circuits (only two shown) may be found in the IF amplifier section of the radio. These tank circuits will be fixed tuned to the IF frequency, which in common AM broadcast band (BCB) radio receivers is typically

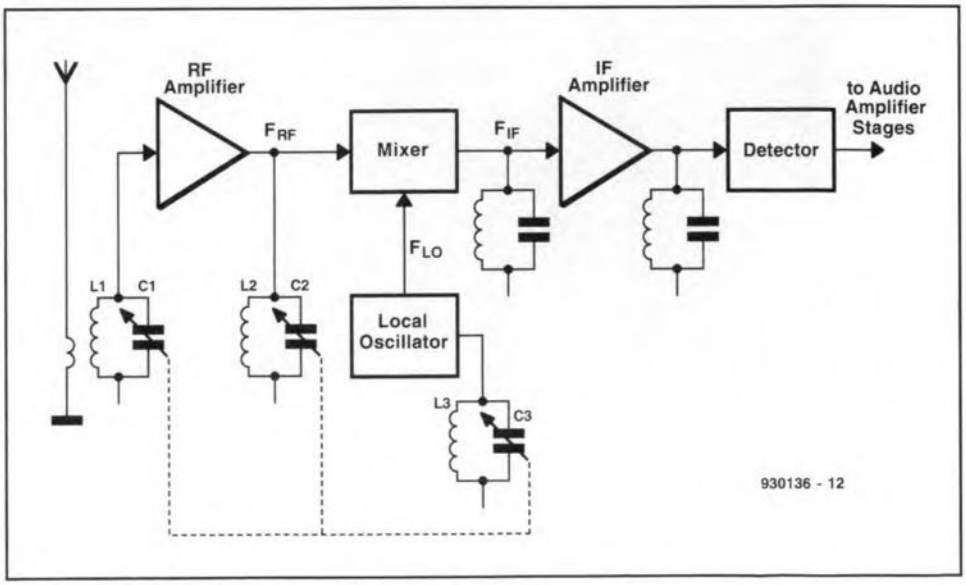


Fig. 2. *LC* tank circuits in a superheterodyne receiver.

450 kHz, 455 kHz, 460 kHz, or 470 kHz depending on the designer's choices (and sometimes country of origin). Other IF frequencies are also seen, but these are most common. FM broadcast receivers typically use a 10.7 MHz IF, while short-wave receivers might use a 1.65 MHz, 8.83 MHz, 9 MHz or an IF frequency above 30 MHz.

The tracking problem

On a radio that tunes the front-end with a single knob, which is almost all receivers today, the three capacitors ($C1$, $C2$ and $C3$ in **Fig. 2**) are typically **ganged**, i.e., mounted on a single rotor shaft. These three tank circuits must **track** each other; i.e., when the RF amplifier is tuned to a certain radio signal frequency, the LO must produce a signal that is different from the RF frequency by the amount of the IF frequency. Perfect tracking is probably impossible, but the fact that your single knob tuned radio works is testimony to the fact that the tracking isn't too terrible.

The issue of tracking LC tank circuits for the AM broadcast band (BCB) receiver has not been a major problem for many years: the band limits are fixed over most of the world, and component manufacturers offer standard adjustable inductors and variable capacitors to tune the RF and LO frequencies. Indeed, some even offer three sets of coils: antenna, mixer input/RF amp output and LO. The reason why the antenna and mixer/RF coils are not the same, despite tuning the same frequency range, is that these locations see different distributed or 'stray' capacitances. In the U.S.A., it is standard practice to use a 10 to 365 pF capacitor and a 220 µH inductor for the 540 to 1600 kHz AM BCB. In some other countries, slightly different combinations are sometimes used: 320 pF, 380 pF, 440 pF, 500 pF and others are seen in catalogues (see, for instance, the Maplin Electronics catalogue. Address: P.O. Box 3, Rayleigh, Essex SS6 2BR, England).

Recently, however, two events coincided that caused me to examine the method of selecting capacitance and inductance values. First, I embarked on a design project to produce an AM DXers receiver that had outstanding performance characteristics. Second, the AM broadcast band was recently extended so that the upper limit is now 1700 kHz, rather than 1600 kHz. The new 540 to 1700 kHz band is not accommodated by the now-obsolete 'standard' values of inductance and capacitance. So I calculated new candidate values.

The RF amplifier/antenna tuner problem

In a typical RF tank circuit, the inductance is kept fixed (except for a small adjustment range that is used for overcoming tolerance deviations) and the capacitance is varied across the range. **Figure 3** shows a typical tank circuit main tuning capacitor ($C1$), trimmer capacitor ($C2$) and a fixed capacitor ($C3$) that is not always needed. The stray capacitance (C_s) includes the interwiring capacitance, the wiring to chassis capacitance, and the amplifier or oscillator device input capacitance. The frequency changes as the square root of the capacitance change. If F_1 is the minimum frequency in the range, and F_2 is the maximum frequency, then the relationship is:

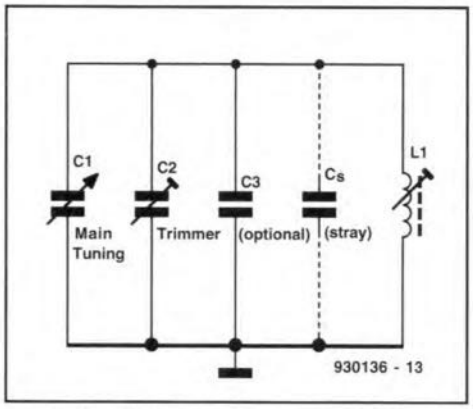


Fig. 3. Parallel resonant tuning circuit.

$$\frac{F_2}{F_1} = \sqrt{\frac{C_{max}}{C_{min}}} \qquad (2)$$

or, in a rearranged form that some find more congenial:

$$\left(\frac{F_2}{F_1}\right)^2 = \frac{C_{max}}{C_{min}} \qquad (3)$$

In the case of the new AM receiver, I wanted an overlap of about 15 kHz at the bottom end of the band, and 10 kHz at the upper end, so needed a resonant tank circuit that would tune from 525 kHz to 1710 kHz. In addition, because variable capacitors are widely available in certain values based on the old standards, I wanted to use a 'standard' AM BCB variable capacitor. A 10 to 380 pF unit from a vendor was selected.

The minimum required capacitance, C_{min}, can be calculated from:

$$\left(\frac{F_2}{F_1}\right)^2 C_{min} = C_{min} + \Delta C \qquad (4)$$

Where:

$F1$ is the minimum frequency tuned;
$F2$ is the maximum frequency tuned;
C_{min} is the minimum required capacitance at $F2$;
ΔC is the difference between C_{max} and C_{min}.

Example

Find the minimum capacitance needed to tune 1710 kHz when a 10 to 380 pF capacitor (ΔC= 380–10 pF = 370 pF) is used, and the minimum frequency is 525 kHz.

Solution:

$$\left(\frac{F_2}{F_1}\right)^2 C_{min} = C_{min} + \Delta C$$

$$\left(\frac{1710\,\text{kHz}}{525\,\text{kHz}}\right)^2 C_{min} = C_{min} + 370\,\text{pF}$$

$$10.609\,C_{min} = C_{min} + 370\,\text{pF}$$

$$C_{min} = 38.51\,\text{pF}$$

The maximum capacitance must be C_{min} + ΔC, or 38.51 + 370 pF = 408.51 pF. Because the tuning capacitor (C1 in **Fig. 3**) does not have exactly this range, external capacitors must be used, and because the required value is higher than the normal value additional capacitors are added to the circuit in parallel to $C1$. Indeed, because somewhat unpredictable 'stray' capacitances also exist in the circuit, the tuning capacitor values should be a little smaller than the required values in order to accommodate strays plus tolerances in the actual — versus published — values of the capacitors. In **Fig. 3**, the main tuning capacitor is $C1$ (10 to 380 pF), $C2$ is a small value trimmer capacitor used to compensate for discrepancies, $C3$ is an optional capacitor that may be needed to increase the total capacitance, and C_s is the stray capacitance in the circuit.

The value of the stray capacitance can be quite high, especially if there are other capacitors in the circuit that are not directly used to select the frequency (e.g., in Colpitts and Clapp oscillators the feedback capacitors affect the LC tank circuit). In the circuit that I was using, however, the LC tank circuit is not affected by other capacitors. Only the wiring strays and the input capacitance of the RF amplifier or mixer stage need be accounted. From experience I apportioned 7 pF to C_s as a **trial** value.

The minimum capacitance calculated above was 38.51, there is a nominal 7 pF of stray capacitance, and the minimum available capacitance from $C1$ is 10 pF. Therefore, the combined values of $C2$ and $C3$ must be (38.51–10–7 pF), or 21.5 pF. Because there is considerable reasonable doubt about the actual value of C_s, and because of tolerances in the manufacture of the main tuning variable capacitor ($C1$), a wide range of capacitance for $C2$+$C3$ is preferred. It is noted from several catalogues that 21.5 pF is near the centre of the range of 45 pF and 50 pF trimmer capacitors. For example, one model lists its range as 6.8 pF to 50 pF, its centre point is only slightly removed from the actual desired capacitance. Thus, a 6.8 to 50 pF trimmer was selected, and $C3$ is not used.

Selecting the inductance value for $L1$ (**Fig. 3**) is a matter of picking the frequency and associated required capaci-

```
100 'PROGRAM TO CALCULATE L-C TANK CIRCUIT VALUES
110 'A color monitor is needed for this program. If no color monitor is
120 'is used, then delete Line Nos. 140 and 150.
130  CLS:KEY OFF
140  SCREEN 9
150  GOSUB 1030:'Get graphic of circuit diagram
160 'Start of program
170    CLS:KEY OFF:SCREEN SCR:PI = 22/7
180 IF SCR > 0 THEN COLOR 1,7
190 LOCATE 6,15:PRINT "Calculate L-C tank circuit values from knowledge"
200 LOCATE  7,15:PRINT "of desired frequency range and variable capacitor"
210 LOCATE  8,15:PRINT "values (in picofards)."
220 LOCATE 10,15:PRINT "Enter MINIMUM frequency (F1)in kilohertz (KHz):";
230     INPUT F1$:' Obtain value of lowest frequency
240       F1 = VAL(F1$):' Test input of F1 to see if zero
250         IF F1 = 0 THEN BEEP
260         IF F1 = 0 THEN 220 ELSE 270
270 LOCATE 12,15:PRINT "Enter MAXIMUM frequency (F2) in kilohertz (KHz):";
280     INPUT F2$:' Obtain value of highest frequency
290       F2 = VAL(F2$):' Test input of F2 to see if zero
300         IF F2 = 0 THEN BEEP
310         IF F2 = 0 THEN 270
320           IF F2 = F1 THEN GOSUB 1440:'Test for incorrect freq. input
330           IF F1 > F2 THEN GOSUB 1440
340           IF F2 = F1 THEN 160 ELSE 350
350           IF F1 > F2 THEN 160 ELSE 360
360 LOCATE 14,15:PRINT "Select Capacitor Values..."
370 LOCATE 16,15:PRINT "Enter MINIMUM value of capacitor in picofarads (pF):";
380     INPUT CMIN$
390       CMIN = VAL(CMIN$)
400         IF CMIN = 0 THEN BEEP
410         IF CMIN = 0 THEN 360 ELSE 420
420 LOCATE 18,15:PRINT "Enter MAXIMUM value of capacitor in picofarads (pF):";
430     INPUT CMAX$
440       CMAX = VAL(CMAX$)
450         IF CMAX = 0 THEN BEEP
460         IF CMAX = 0 THEN 420 ELSE 470
470           IF CMIN = CMAX THEN GOSUB 1480:'Test for incorrect cap. input
480           IF CMIN > CMAX THEN GOSUB 1480:'and display error message
490           IF CMIN = CMAX THEN 360 ELSE 500
500           IF CMIN > CMAX THEN 360 ELSE 510
510 CLS:'Clear screen and print all entered values
520 LOCATE 6,15:PRINT "Minimum frequency (F1):";F1;" KHz"
530 LOCATE 7,15:PRINT "Maximum frequency (F2):";F2;" KHz"
540  LOCATE 9,15:PRINT "Minimum capacitance in C1: ";CMIN;" pF"
550  LOCATE 10,15:PRINT "Maximum capacitance in C1: ";CMAX;" pF"
560     FRATIO = F2/F1:'Calculate frequency ratio
570     CRATIO = FRATIO^2:'Calculate capacitance ratio
580     CDELTA = CMAX-CMIN
590  LOCATE 11,15:PRINT "Frequency ratio: ";
600    PRINT USING "##.###";FRATIO;:PRINT ":1"
610  LOCATE 12,15:PRINT "Required capacitance ratio: ";
620    PRINT USING "##.###";CRATIO;:PRINT ":1"
630  LOCATE 13,15:PRINT "Capacitance differential: ";
640    PRINT USING "####.##";CDELTA;:PRINT " pF"
650  XMIN = CDELTA/(CRATIO - 1):'Calculate min. total cap. needed
660  XMAX = CDELTA + XMIN:' Calculate max. total cap. needed
670  TRIMCAP = XMIN - CMIN
680    IF TRIMCAP < 0 THEN GOSUB 1580 ELSE 690
690    IF TRIMCAP < 0 THEN 160 ELSE 700
700  LOCATE 15,15:PRINT "Trimmer capacitance needed: ";
710  PRINT USING "####.##";TRIMCAP;:PRINT " pF"
720    LUH = 1/(4*PI^2*F1^2*XMAX*10^-12)
730  LOCATE 16,15:PRINT "Inductance needed: ";
740  PRINT USING "####.##";LUH;:PRINT " uH"
750  LOCATE 18,15:PRINT "Allocate a few pF for strays and then make up"
760  LOCATE 19,15:PRINT "remaining capacitance with either fixed or variable"
770  LOCATE 20,15:PRINT "trimmer capacitors."
780  LOCATE 22,15:GOSUB 1630:'Get press any key subroutine
790  CLS:'Clear screen for new message
800  LOCATE 10,15:PRINT "The trimmer capacitance will include all capacitances"
810  LOCATE 11,15:PRINT "seen by the inductor, and that could include a large"
820  LOCATE 12,15:PRINT "capacitance in other parts of the circuit. In certain"
830  LOCATE 13,15:PRINT "oscillator circuits, especially Colpitts and Clapp"
840  LOCATE 14,15:PRINT "oscillators, the other capacitances are large."
850  LOCATE 15,15:PRINT "Check a good oscillator design handbook for further"
860  LOCATE 16,15:PRINT "information."
870  LOCATE 18,15:GOSUB 1630
880  CLS:LOCATE 12,15:PRINT "(D)o Another Problem?"
890  LOCATE 13,15:PRINT "(E)nd Program?"
900  CHOICE$ = INPUT$(1)
910  IF CHOICE$ = "D" THEN CHOICE = 1
920  IF CHOICE$ = "d" THEN CHOICE = 1
930  IF CHOICE$ = "E" THEN CHOICE = 2
940  IF CHOICE$ = "e" THEN CHOICE = 2
950     IF CHOICE < 1 THEN 880 ELSE 960
960     IF CHOICE > 2 THEN 880 ELSE 970
970     IF INT(CHOICE) = CHOICE THEN 980 ELSE 880
980  ON CHOICE GOTO 160,990
990 CLS:LOCATE 12,20:PRINT "Program Ended...Goodbye"
1000  TIMELOOP=TIMER:WHILE TIMER < TIMELOOP + 2:WEND
1010 CLS
1020 END
1030 'Subroutine to draw circuit picture on screen
1040 CLS:LINE (450,100)-(100,100):'Draw connecting rails
1050 LINE (450,200)-(100,200)
1060 LINE (175,180)-(165,120),,B:'Draw inductor L1
1070 LINE (170,200)-(170,180)
1080 LINE (170,120)-(170,100)
1090 LINE (175,180-ZZ)-(165,180-ZZ)
1100 ZZ = ZZ + 5
1110 IF ZZ =  60 GOTO 1130
1120 GOTO 1090
1130 LINE (250,200)-(250,153):'Draw C1 (main tuning capacitor)
1140 LINE (250,147)-(250,100)
1150 LINE (265,153)-(235,153)
1160 LINE (265,147)-(235,147)
1170 LINE (265,165)-(235,135)
1180 LINE (350,200)-(350,153):'Draw C2 (trimmer capacitor)
1190 LINE (350,147)-(350,100)
1200 LINE (365,153)-(335,153)
1210 LINE (365,147)-(335,147)
1220 LINE (365,165)-(335,135)
1230 LINE (450,200)-(450,153):'Draw stray capacitances
1240 LINE (450,147)-(450,100)
1250 LINE (465,153)-(435,153)
1260 LINE (465,147)-(435,147)
1270 LINE (102,102)-(98,98),1,B
1280 LINE (102,202)-(98,198),1,B
1290 LINE (252,202)-(248,198),1,BF
1300 LINE (252,102)-(248,98),1,BF
1310 LINE (352,202)-(348,198),1,BF
1320 LINE (352,102)-(348,98),1,BF
1330 LINE (172,202)-(168,198),1,BF
1340 LINE (172,102)-(168,98),1,BF
1350 LOCATE 11,19:PRINT "L1":'Add alphabetic labels
1360 LOCATE 11,27:PRINT "C1"
1370 LOCATE 11,40:PRINT "C2"
1380 LOCATE 11,49:PRINT "Stray"
1390 LOCATE 16,15:PRINT "C1 is main tuning capacitor"
1400 LOCATE 17,15:PRINT "C2 is trimmer + fixed capacitors"
1410 LOCATE 18,15:PRINT "Stray is wiring capacitance plus other"
1420 LOCATE 19,15:PRINT "capacitors in the circuit."
1430 LOCATE 21,15:GOSUB 1630:CLS:RETURN:'End of Subroutine
1440 ' Error Message Subroutine (Incorrect Frequency Input)
1450   BEEP:LOCATE 17,15:PRINT "ERROR!  F2 must be greater than F1"
1460   LOCATE 19,15:GOSUB 1630:' Go get press any key subroutine
1470 RETURN:'End of Subroutine
1480 'Error Message Subroutine (Incorrect Capacitance Input)
1490  BEEP:LOCATE 20,15:PRINT "ERROR! Cmax must be greater than Cmin"
1500   LOCATE 22,15:GOSUB 1630:' Go get press any key subroutine
1510   GOSUB 1530:'Clear screen and reprint F1 and F2
1520  RETURN:' End of Subroutine
1530 ' Subroutine to clear screen and reprint values of F1 and F2
1540  CLS
1550  LOCATE 6,15:PRINT "Minimum frequency (F1):";F1;" KHz";
1560  LOCATE 7,15:PRINT "Maximum frequency (F2):";F2;" KHz"
1570 RETURN:'End of Subroutine
1580 'Subroutine for Too Small Trimmer Capacitance
1590  CLS
1600  LOCATE 12,15:PRINT "ERROR!!! Not a viable combination...try again"
1610  LOCATE 14,15:GOSUB 1630:'Go get press any key subroutine
1620  RETURN
1630 ' Press Any Key... Subroutine
1640 PRINT "Press Any Key To Continue..."
1650 A$ = INKEY$:IF A$ = "" THEN 1650 ELSE 1660
1660 RETURN:'End of Subroutine
```

930136-16

tance at one end of the range, and calculating from the standard resonance equation solved for L:

$$L = \frac{10^6}{4\pi^2 F^2_{\text{low}} C_{\text{max}}} \quad \mu\text{H} \qquad (5)$$

$$L = \frac{10^6}{4\pi^2 (525{,}000)^2 (4.085\times10^{-10})}$$

$$L = 224.97 = 225\ \mu\text{H}$$

The RF amplifier input LC tank circuit and the RF amplifier output LC tank circuit are slightly different cases because the stray capacitances are somewhat different. In the example, I am assuming a JFET transistor RF amplifier, and it has an input capacitance of only a few picofarads. The output capacitance is not a critical issue in this specific case because I intend to use a 1 mH RF choke in order to prevent JFET oscillation. In the final receiver, the RF amplifier may be deleted altogether, and the LC tank circuit described above will drive a mixer input through a link coupling circuit.

The local oscillator (LO) problem

The local oscillator circuit must track the RF amplifier, and must also tune a frequency range that is different from the RF range by the amount of the IF frequency (455 kHz). In keeping with common practice I selected to place the LO frequency 455 kHz **above** the RF frequency. Thus, the LO must tune the range 980 kHz to 2,165 kHz.

There are three methods for making the local oscillator track with the RF amplifier frequency when single shaft tuning is desired: the **trimmer capacitor** method, the **padder capacitor** method, and the **different-value cut-plate capacitor** method.

The trimmer capacitor method was shown in **Fig. 3**, and is the same as the RF LC tank circuit. Using exactly the same method as before, but with a frequency ratio of (2165/980) to yield a capacitance ratio of $(2165/980)^2 = 4.88{:}1$, solves this problem. The results were a minimum capacitance of 95.36 pF, and a maximum capacitance of 465.36 pF. An inductance of 56.7 µH is needed to resonate these capacitances to the LO range.

There is always a problem associated with using the same identical capacitor for both RF and LO. It seems that there is just enough difference that tracking between them is always a bit off. **Figure 6** shows the ideal LO frequency and the calculated LO frequency. The difference between these two curves is the degree of non-tracking. The curves

Fig. 4. BASIC program to calculate RF tank circuit component values.

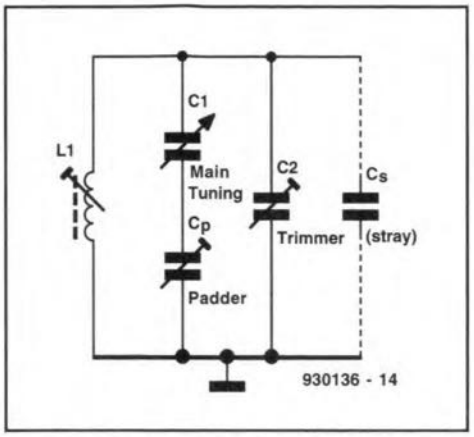


Fig. 5. Parallel resonant tank circuit using the padder capacitor method.

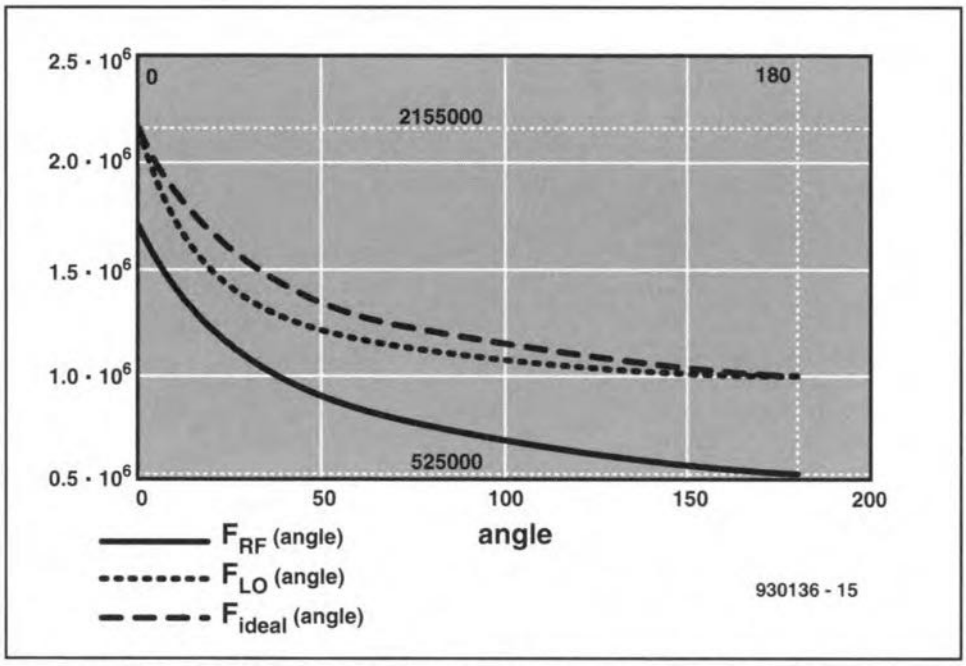


Fig. 6. MathCAD 3.1 plot of RF, LO (ideal) and LO (actual) tuning as a function of capacitor shaft angle.

overlap at the ends, but are awful in the middle. There are two cures for this problem. First, use a **padder capacitor** in series with the main tuning capacitor (**Fig. 5**). Second, use a **different-value cut-plate capacitor**.

Figure 5 shows the use of a padder capacitor (C_p) to change the range of the LO section of the variable capacitor. This method is used when both sections of the variable capacitor are identical. Once the reduced capacitance values of the $C1/C_p$ combination are determined the procedure is identical to above. But first, we have to calculate the value of the padder capacitor and the resultant range of the $C1/C_p$ combination. The padder value is found from:

$$\frac{C1_{max}\,C_p}{C1_{max}+C_p}=\left(\frac{F_2}{F_1}\right)^2\left(\frac{C1_{min}\,C_p}{C1_{min}+C_p}\right) \quad (6)$$

...and solving for C_p. For the values of the selected main tuning capacitor and LO:

$$\frac{(380\,pF)\,C_p}{(380+C_p)\,pF}=(4.88)\left(\frac{(10pF)\,C_p}{(10+C_p\,pF)}\right)$$

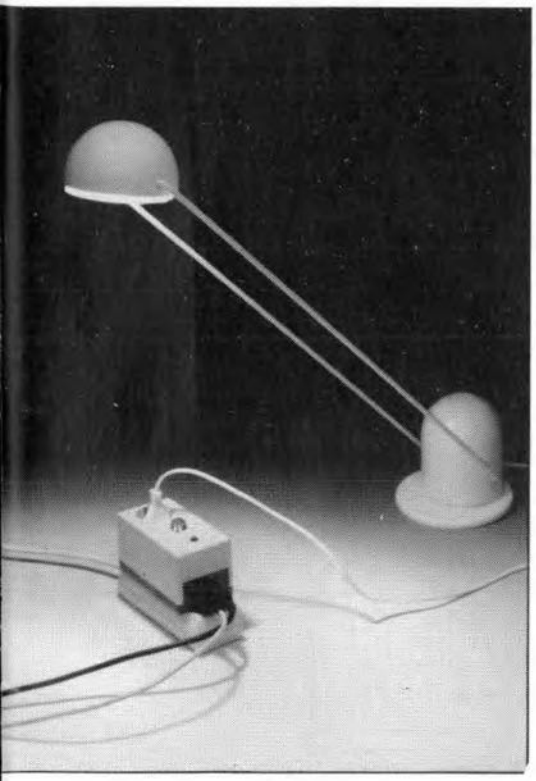
Solving for C_p by the least common denominator method (crude, but it works) yields a padder capacitance of 44.52 pF. The series combination of 44.52 pF and a 10 to 380 pF variable yields a range of 8.2 pF to 39.85 pF. An inductance of 661.85 µH is needed for this capacitance to resonate over 980 kHz to 2,165 kHz.

A practical solution to the tracking problem that comes close to the ideal is to use a **cut-plate** capacitor. These variable capacitors have at least two sections, one each for RF and LO tuning. The shape of the capacitor plates are especially cut to a shape that permits a constant change of **frequency** for every degree of shaft rotation. With these capacitors, when well done, it is possible to produce three-point tracking, or better.■

I²C POWER SWITCH

A module is described that enables a mains powered device of up to 275 VA to be controlled by a PC via the I²C bus. Since a direct connection to the mains voltage exists in the circuit, great attention has been given in the design to your electrical safety, as well as to protection of the expensive PC.

Design by K. Walraven



WHEREVER a PC is used to switch mains powered apparatus on and off, great care must be exercised with regard to safety, since even a small error can have disastrous consequences. And yet, being able to switch lamps and other (small) nonreactive devices powered from the mains appeals to many PC users. The power switch described in this article enables mains powered, nonreactive, devices of up to 275 VA to be controlled in a safe manner. Provided the user keeps to the construction notes, the electrical insulation provided by the circuit should afford the PC and its user adequate protection against dangerous voltage levels.

The electronics

The small circuit shown in **Fig. 1** is designed to minimize the risk of connecting a PC to devices which are powered from the mains. Safety is achieved essentially with the aid of a solid state relay (SSR) which contains an optoisolator. The heart of the circuit is an 8-bit quasi bidirectional I/O port Type PCF8574 from Philips Semiconductors. This IC is driven via the I²C bus (the associated PC interface card is described in Ref. 1). The PCF8574 comes in two versions: the 'plain' PCF8574 with base address 40H, and the PCF8574A with base address 70H. Since each IC can be located at eight different addresses with the aid of three jumpers (JP1, JP2 and JP3), up to 16 of these circuits can be connected simultaneously to a single I²C bus.

For the sake of safety, the module is fitted into a compact mains adaptor case with a moulded mains plug and socket. This is also the reason for having only one relay per module. The PC and the module communicate via a short length of 5-way cable. The two mini-DIN sockets on the module are typical of all I²C circuits published so far in this magazine (see the 'catch the I²C bus' inset), and allow modules to be 'chained'. The 5-way cable carries the two digital signals SDA and SCL as well as the supply voltage.

Only one of the eight digital I/O ports contained in the PCF8574 is used in every module. Here, output P0 is used to drive the LED in the solid-state relay, ISO1. After an automatic power-on reset, all I/O lines of the PCF8574 are logic high, which means that they function as inputs. Consequently, the power on/off LED and the LED in ISO1 are off after a reset. The triac contained in the electronic relay does not start to conduct until output P0 of IC1 is made logic low. LED D1 then also lights to indicate that the mains load is switched on. The triac in the SSR is shunted by a so-called snubber network. This con-

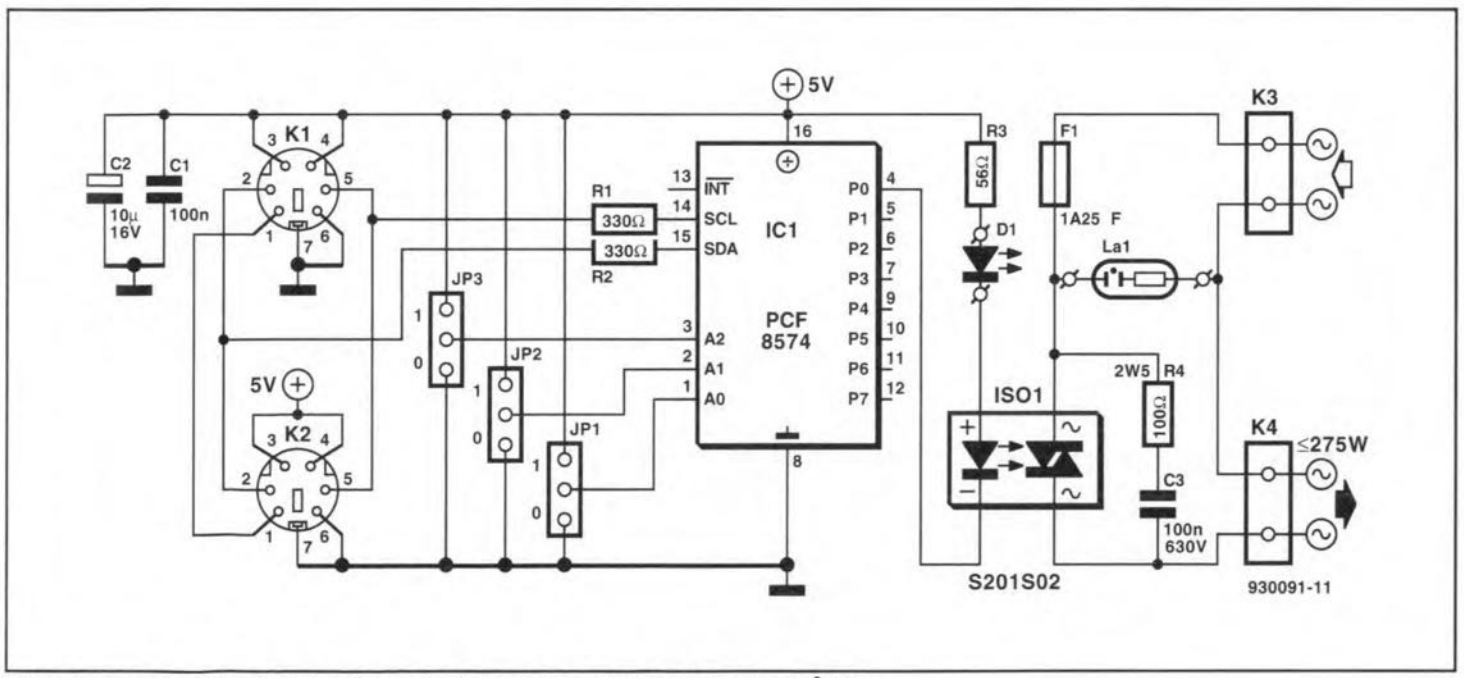


Fig. 1. Circuit diagram of the power switching module, which is driven via an I²C bus.

sists of R4 and C3, and serves to limit the voltage changes (d*U*/d*t*) across the triac. Without this network, there is a real chance of the triac starting to conduct spontaneously when fast voltage changes occur.

A neon lamp with built-in series resistor is connected across the *RC* network to indicate that the mains voltage is present in the module when it is plugged into a mains outlet. Fuse F1 is included to ensure that the current through the triac can not exceed 1.25 A. In this way, the triac is protected against overloading because the maximum continuous current through the solid-state relay is 1.5 A.

Al other components in the circuit are passive; two capacitors, C1 and C2, which decouple the supply voltage of IC1; resistors R1 and R2, which act as current limiters on the SDA and SDL lines; and three jumpers, JP1, JP2 and JP3, which are used to set the three least significant address bits.

From theory to practice

The copper track layout and the component positioning on the printed circuit board shown in **Fig. 2** afford a high degree of safety provided you work neatly and use the right components. Start the construction by cutting off the two corners and the notch in the PCB. Next, fit the four wire links on the board, and then the components. The neon lamp (LA1) is optional, and may be omitted. Set the jumpers to give the desired address. A '0' is selected when the jumper is at the side of the fuseholder, and a '1' when the jumper is at the side of the IC. To reduce the risk of touching the mains voltage while the circuit is not fitted into the enclosure, it is recommended to fit the plastic cap that comes with

COMPONENTS LIST

Resistors:

2	330Ω	R1;R2
1	56Ω	R3
1	100Ω 2W5	R4

Capacitors:

1	100nF	C1
1	10µF 16V	C2
1	100nF 630V	C3

Semiconductors:

1	green LED	D1
1	PCF8574(A)	IC1

Miscellaneous:

2	PCB-mount 6-way mini-DIN socket	K1;K2
2	2-way PCB terminal block, pitch 7.5mm	K3;K4
1	S201S02 (Sharp)	ISO1
1	1A25 fast fuse with PCB mount holder	F1
1	Neon lamp with internal resistor for mains voltage	La1
1	Enclosure with moulded mains plug and socket; size approx.120 × 65 × 50 mm, e.g. Bopla SE432 DE	
1	Printed circuit board 930091 (see page 110)	

CATCH THE I²C BUS

The Philips I²C bus offers an extremely simple way of interconnecting and controlling complex integrated circuits. A wide variety of I²C bus compatible ICs is available, while prices of these devices are relatively low because of mass production to cater for the need of consumer electronics. *Elektor Electronics* has published a number of articles that describe the operation and practical application of I²C compatible ICs, complete with suitable software for IBM PCs and compatibles. If you have not already done so, catch the I²C bus with the following articles in *Elektor Electronics*:

Inter-IC communications	September 1990
Video digitizer	July/August 1991
I²C interface for PCs	February 1992
I²C LED display	June 1992
Speech/sound memory	December 1992
I²C alphanumerical display	July/August 1993
I²C bus fuse	July/August 1993
I²C opto/relay card	February 1993

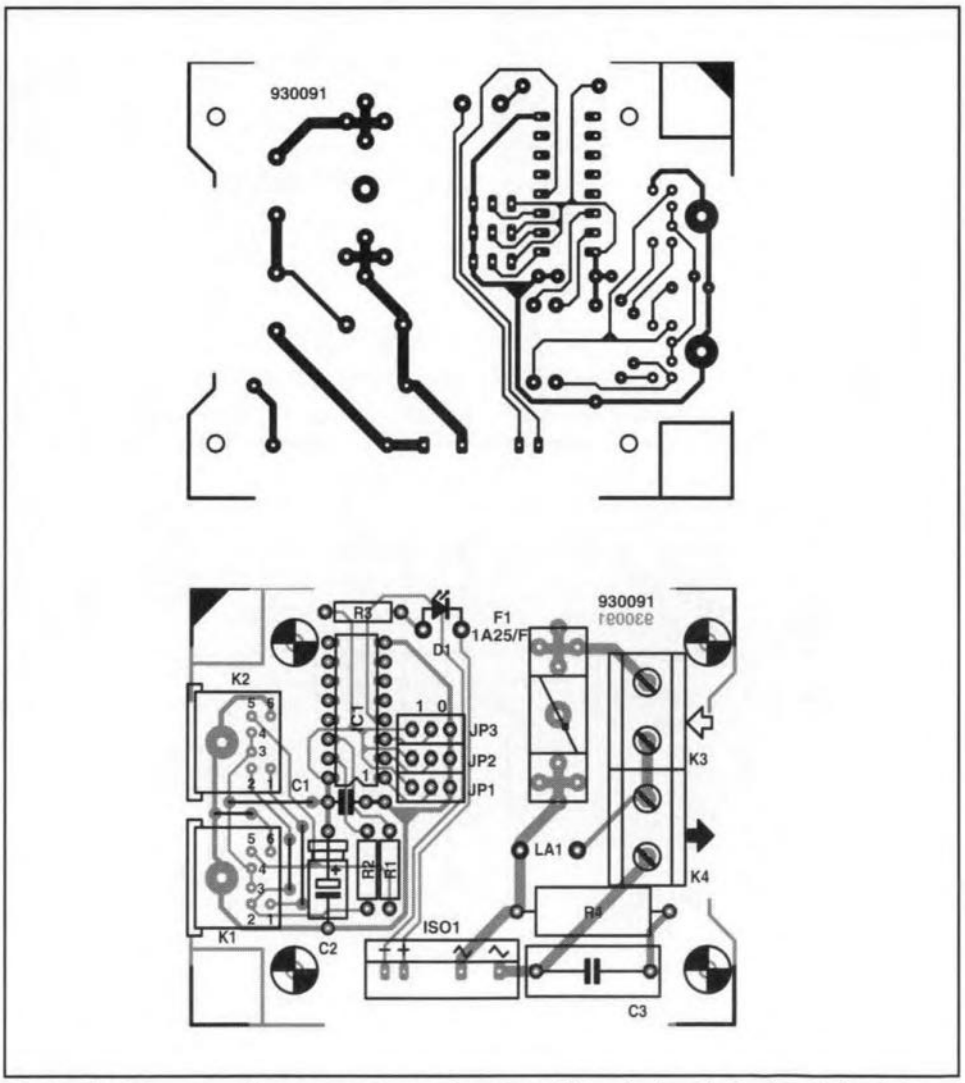


Fig. 2. Track layout and component mounting plan of the single-sided printed circuit board designed for the I²C power switch.

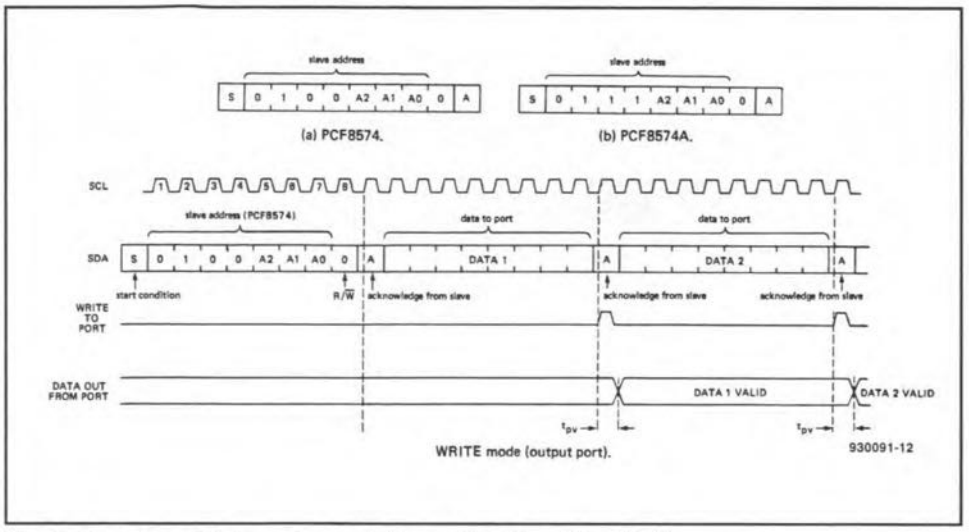


Fig. 3. Overview of data exchange between the PC and the I/O IC.

the PCB mount fuse holder.

Two holes are drilled in the mains adaptor enclosure to enable the DIN plugs to be inserted into the sockets on the board. Next, the PCB is secured into the enclosure with the aid of two screws. When the enclosure stated in the parts list is used, the two holes near the PCB terminal block may not be used for metal bolts. If you still want to fix the PCB at these locations, use nylon bolts instead.

Next, fit LED D1 into the cover of the case, and connect it to the PCB. Finally, connect the PCB to the integral plug pins and the socket terminals. Fit the cover onto the case, and secure the fixing screws. The circuit is then ready for testing.

One final remark on the electronic relay. The S210S02 contains a zero-crossing detector, and is only suitable for switching nonreactive loads. If you want to switch reactive loads also, use the S201S01, which switches randomly, and therefore does not cause problems with capacitive or inductive loads.

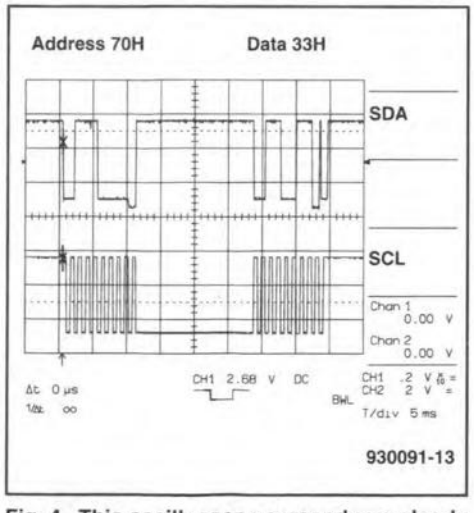


Fig. 4. This oscilloscope screendump clearly indicates the position of the acknowledge pulse. The signal level is not quite to specification because it is generated by the receiving IC.

Reading and writing

Once the hardware is finished, it is time to concentrate on the software. The base address of the PCF8574 is 40H, or 70H when the PCF8574A is used. The address set with the aid of the jumpers is added to this base address. Further, the LSB (least significant bit) determines the direction of the data: reading (1) or writing (0). Writing a logic 1 to an output bit causes the line to be switched to 'output'. If you wish to use a bit as an input, initialize it by writing a '1' to it. Once this is done, the relevant bit may be used as an input for the rest of the time.

Figure 3 shows the drive signals of the PCF8574 as reproduced from the Philips Semiconductors databook. The position of the jumpers is clearly seen in the address (JP1/JP2/JP3 = A2/A1/A0). A '0' for the eighth address bit indicates a write action to the IC, while a '1' indicates that data is read from the IC. The latter option is useful with regard to the I²C power switch because it allows the PC to interrogate the on/off status of the load. Writing 00H into the I/O port causes the load to be switched on, while writing 01H switches it off.

The digital oscilloscope screendump in **Fig. 4**, finally, shows a nice example of the signals present on the SDA and SCL lines during a write command to the IC. Since 330-Ω protection resistors were inserted in the lines during the measurement, the voltage level on the SDA line was strongly dependent on the transistor that happened to be switching at a particular instant. The advantage is that the acknowledge pulse is clearly discernible in the scope picture. The switching level is clearly different from that which arises when the computer is busy switching. This variation may come in handy during faultfinding: the closer you measure to the port that generates the acknowledge pulse, the closer the signal level is to the ground potential. ■

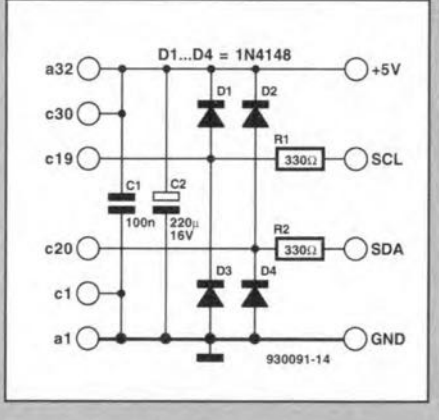
I²C ON THE ACORN PC

By virtue of the I²C interface on the podule bus, owners of an Acorn PC (also know as Acorn Archimedes) do not need a special insertion card to be able to use all the I²C application modules described in *Elektor Electronics*. What's more, all software needed to communicate with I²C devices is implemented in the Acorn operating system.

The circuit below shows how to connect the I²C modules to the Acorn PC. The SDA and SCL signals are on pins C20 and C19 respectively of the podule bus. The SWI called IIC_Control may be used to drive the hardware. Information on the use of this SWI in programs may be found on page 1-944 of the *RISC OS3 Programmer's Reference Manual*.

The resistors and diodes in the circuit protect the computer hardware against damage caused by errors during experimenting.

Users of the video digitizer (*Elektor Electronics* July/August 1991) may find the necessary signals directly on the podule, where the I²C bus is used to program I/O ports (PCF8574) and a DAC for picture intensity control (PCF8591). The fixing bracket of the podule will no doubt have some spare room to accommodate an extra mini-DIN socket. That is all there is to making an external I²C interface on the Archimedes.



Our thanks are due to Mr. J.P. Hendrix of Dongen, the Netherlands, for this useful tip.

Reference:

1. I²C interface for PCs, *Elektor Electronics* February 1992.

work neatly and use the right compo-

COMPONENTS LIST

Resistors:

2	330Ω	R1;R2
1	56Ω	R3
1	100Ω 2W5	R4

Capacitors:

1	100nF	C1
1	10µF 16V	C2
1	100nF 630V	C3

Semiconductors:

1	green LED	D1