# ELEKTOR ELECTRONICS

THE INTERNATIONAL ELECTRONICS MAGAZINE

November 1993

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Solution and winners of our September prize crossword

AUDIO & HI-FI • COMPUTERS & MICROPROCESSORS • DESIGN IDEAS • RADIO, TELEVISION & COMMUNICATIONS • SCIENCE & TECHNOLOGY • TEST & MEASUREMENT

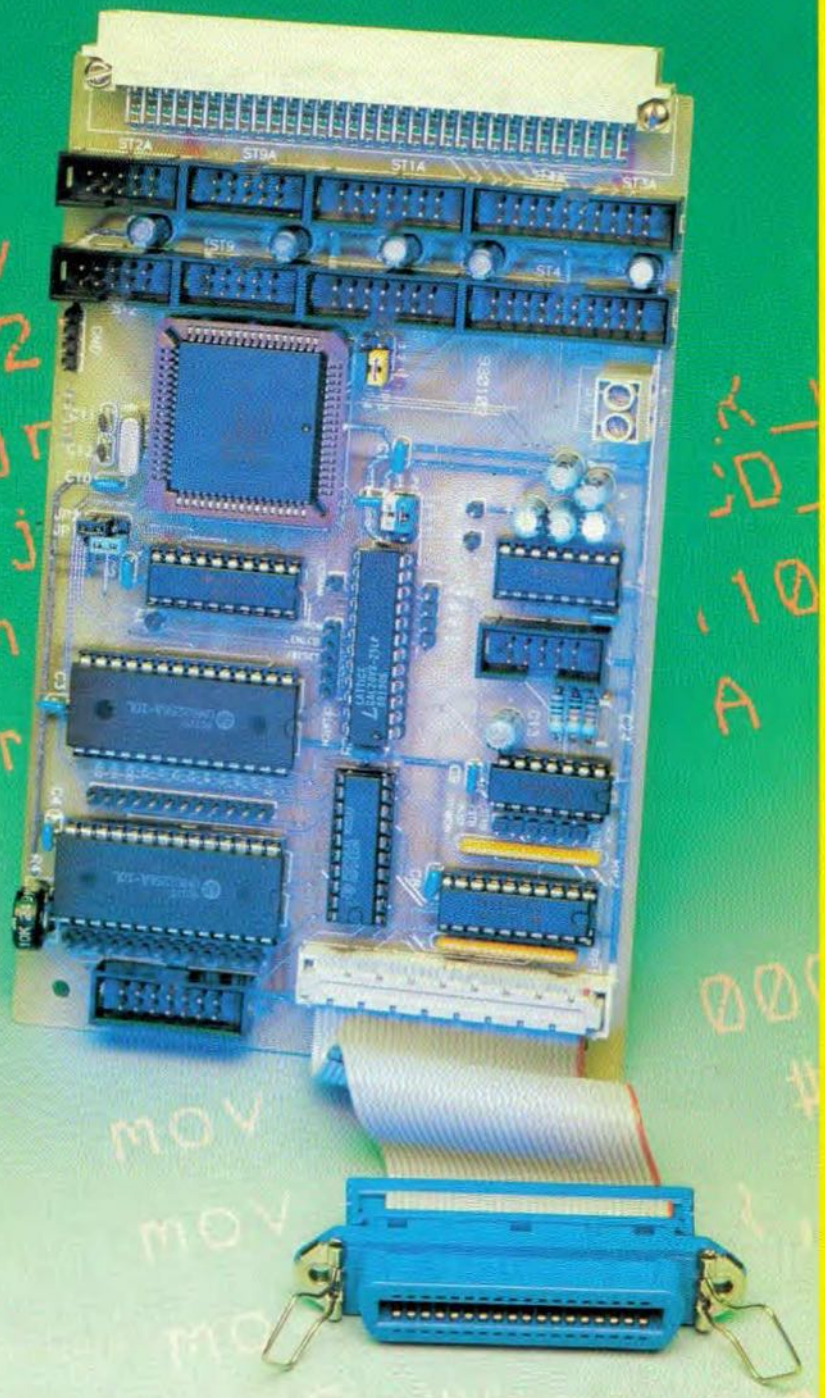
## 535 CARD WITH EPROM EMULATOR

## Precision clock for PCs

## Power MOSFET tester

## Digital hygrometer

## Electronic load for testing power supplies



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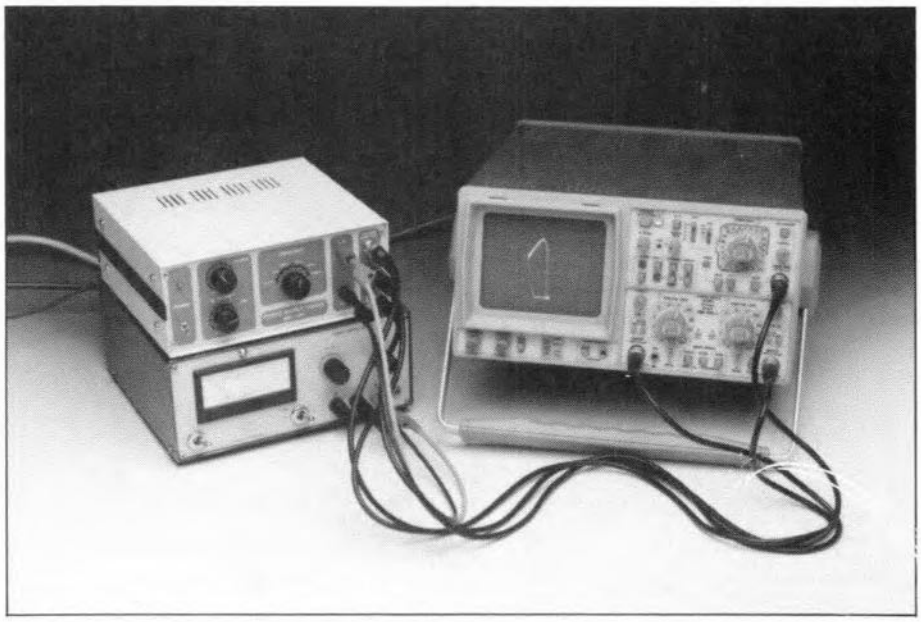
**Design by M. Marquart**

**For testing a power supply, a fairly large resistive load, preferably variable, is needed. Moreover, testing of the dynamic performance of the supply makes it essential that this load can be switched on and off rapidly. The load described in this article has been kept relatively simple, yet it can dissipate 130 W for brief periods and may be switched on and off at a repetition rate that can be set between 10 Hz and 100 kHz.**



# ELECTRONIC LOAD

## FOR TESTING POWER SUPPLIES

A load for testing a power supply must draw a steady current, that is, behave as a pure resistor, and enable the user to check the performance of the supply in rapidly changing circumstances. This last requirement means that a circuit is needed to switch the load on and off a number of times per second. How many times depends on the type of test: a few times per second shows the performance of the buffer capacitors, but it is also important to know how the supply behaves at an on-off rate of a few thousand times per second. An ideal power supply provides a constant voltage across any load (however variable), which shows up as a smooth trace on an oscilloscope. Since such units do not exist, the aim of the designer is to keep the output voltage as smooth as possible in widely varying circumstances. This means that the ripple on the output voltage of the power supply must be minimized. This may be tested by switching the load on and off rapidly.

### Circuit description

These requirements can be met by a power transistor or FET, which functions as a variable load, and a rectangular-wave generator, which switches the transistor on and off at a variable rate. In the present circuit (**Fig. 1**), a FET TYPE BUZ384 ($T_1$) and a Type 555 timer ($IC_1$) are used. The 12 V supply voltage is obtained from a mains adaptor. Diode $D_1$ is the 'supply on' indicator. The current through this LED is determined by $R_1$. Capacitor $C_1$ provides smoothing and buffering of the supply line.

Timer $IC_1$ functions as an astable multivibrator because of the feedback between its pins 2 and 6. Pin 7 is linked internally to the collector of a switching transistor. Pin 6 is connected internally to a comparator that reacts to voltages of $^1/_3$ and $^2/_3$ the level of the supply voltage, $U_{ss}$. One of capacitors $C_2$–$C_6$ (depending on the position of switch $S_2$) is charged via $R_3$ and $D_3$. When the potential on the capacitor has reached a value of $^2/_3 U_{ss}$, the comparator drives the switching transistor connected to pin 7 into conduction. This results in the discharging of the relevant capacitor via $R_2$ and $D_2$. When the voltage across the capacitor has dropped to $^1/_3 U_{ss}$, the comparator switches off the transtor linked to pin 7 and the capacitor is charged anew. Diodes $D_2$ and $D_3$

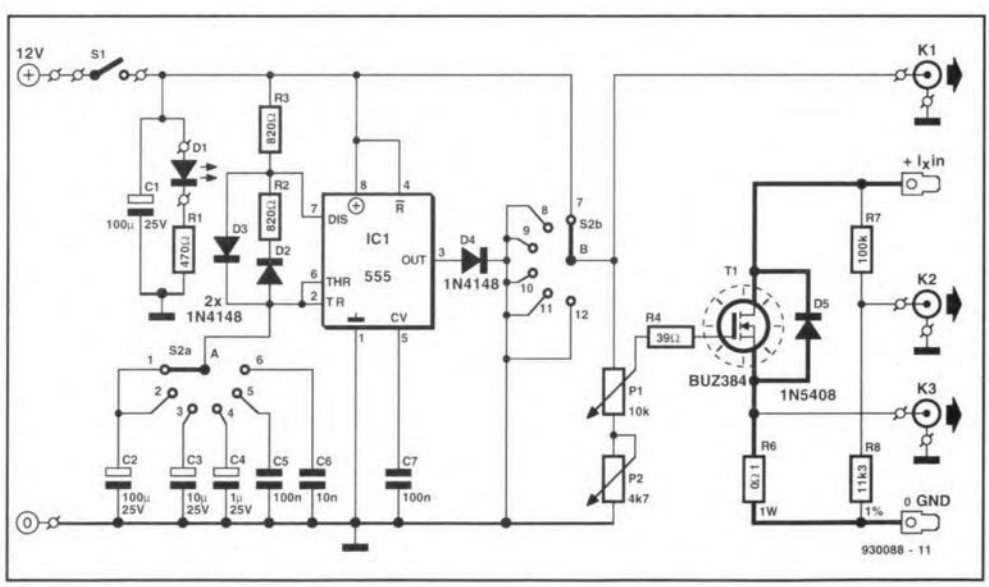



**Fig. 1. Circuit diagram of the electronic load.**

**PARTS LIST**

**Resistors**:
$R_1$ = 470 Ω
$R_2$, $R_3$ = 820 Ω
$R_4$ = 39 Ω
$R_5$ = 1 kΩ
$R_6$ = 0.1 Ω, 10 W
$R_7$ = 100 kΩ
$R_8$ = 11.3 kΩ, 1%
$P_1$ = 10 kΩ potentiometer, linear
$P_2$ = 4.7 kΩ potentiometer, linear

**Capacitors**:
$C_1$, $C_2$ = 100 µF, 25 V, radial
$C_3$ = 10 µF, 25 V, radial
$C_4$ = 1 µF, 25 V, radial
$C_5$, $C_7$ = 100 nF
$C_6$ = 10 nF

**Semiconductors**:
$D_1$ = LED, 3 mm
$D_2$–$D_4$ = 1N4148
$D_5$ = see text
$T_1$ = BUZ384

**Integrated circuits**:
$IC_1$ = 555

**Miscellaneous**:
$S_1$ = single-pole on-off switch
$S_2$ = 2-pole, 6-position rotary switch
$K_1$–$K_3$ = BNC socket for PCB mounting
2 off spade terminal (male and female) for PCB mounting
Heat sink for $T_1$ (SK85*, 75 mm high)
Enclosure 80×200×132 mm (H×W×D)

* Dau (UK) Ltd, 7075 Barnham Road, Barnham, West Sussex PO22 0ES
Telephone (0243) 553031

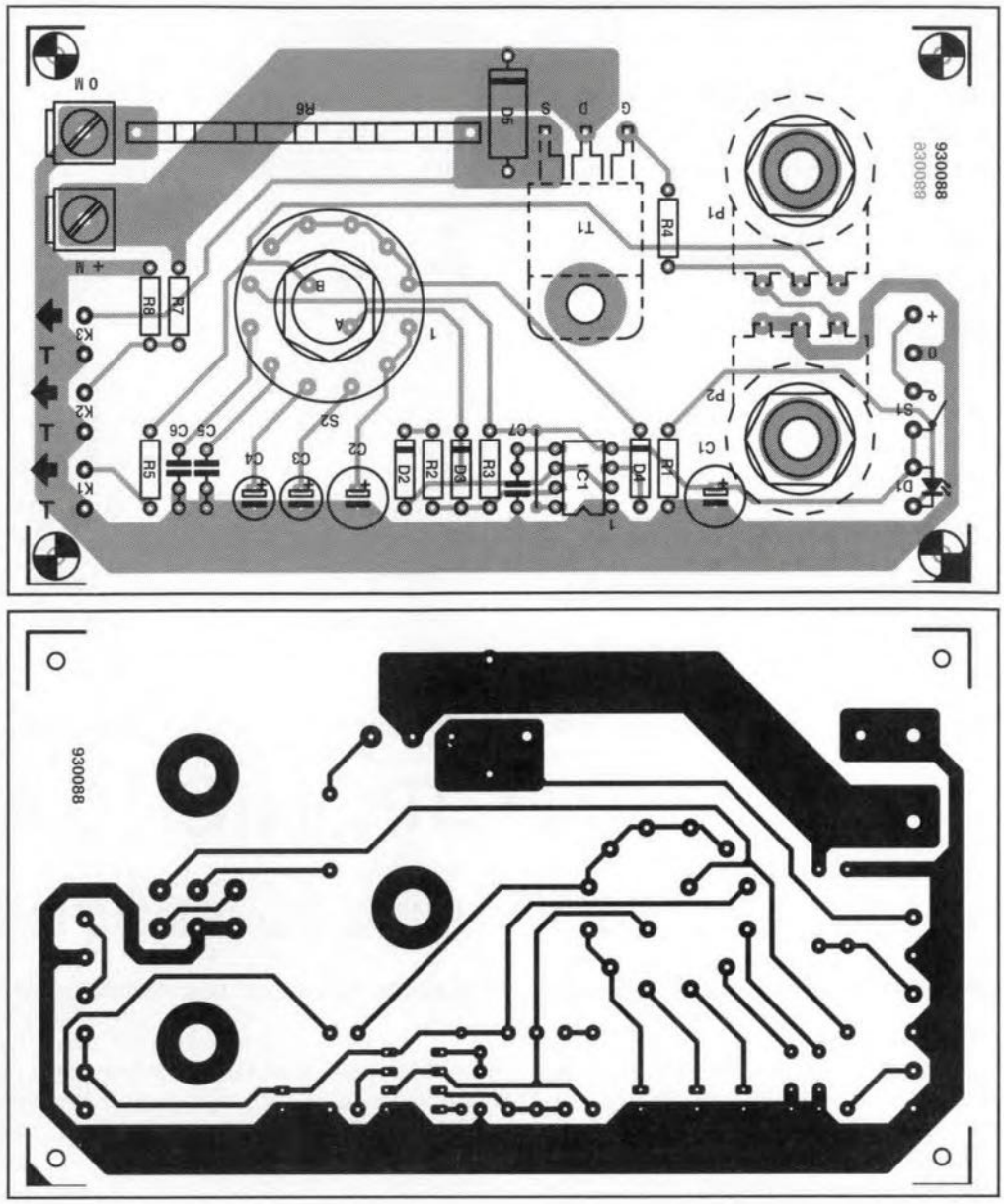



**Fig. 2. Printed-circuit board for the electronic load (not available ready made).**

ensure that the duty factor of the charging/discharging process is 1:1. Five different capacitors, and thus five different frequencies (10 Hz, 100 Hz, 1 kHz, 10 kHz, and 100 kHz), may be selected with $S_2$.

The square-wave output signal of $IC_1$, available at pin 3, is applied via $D_4$ and $S_{2b}$ to potentiometers $P_1$ and $P_2$, which set the gate voltage for $T_1$ (coarse and fine respectively). The magnitude of the gate voltage determines how hard the transistor conducts and thus the value of the resistive load that the FET presents to the power supply on test. The higher the drain voltage, the lower the drain-source transfer resistance of the FET and the harder the transistor conducts.

The drain and source of $T_1$ are connected to the power supply on test via spade terminals $I_x$in and GND.

The BUZ384 is a so-called FREDFET, which is typified by a very fast integrated inverse diode that prevents the device being damaged by negative voltages across the drain-source junction. It can handle currents of up to 10.5 A and has a minimum drain-source transfer resistance, $R_{DS(on)}$, of 0.6 Ω. Diode $D_5$ needs to be used only if a FET without an integrated protection diode is used.

The source of $T_1$ is linked to the GND terminal via a 0.1 Ω, 10 W resistor, $R_6$. The potential drop acros this resistor is a measure of the current through the FET (100 mV $A^{-1}$); it may be measured at $K_3$.

The output voltage of the power supply on test is measured with the aid of potential divider $R_7$-$R_8$ at $K_2$ (100 mV $V^{-1}$).

The pulses applied to the FET are also available at $K_1$ via $R_5$ and may be used to drive the trigger input of an oscilloscope.

Switch $S_2$ is shown in the calibration position in which $T_1$ is on continuously because $P_1$ is linked directly (via $S_{2b}$) to the positive supply line. In this position, the current the load draws from the power supply on test is measured at $K_3$ and set to the wanted value with $P_1$ and $P_2$. After this has been done,the dynamic performance of the supply on test may be checked by setting $S_2$ to the other positions.

## Construction

Although a ready-made PCB is not available, it is recommended to build the electronic load on a board made according to **Fig. 2**. The design of the board allows the potentiometers and the rotary switch to be mounted on it. It is best to start with fitting the smaller components, followed by the solder pins, the spade terminals, the potentiometers and the rotary switch.

Mount the FET on a heat sink, which must be fitted at the back of the board. The position must be such that the bent-forward terminals of the FET protrude through the relevant holes on the board.

Fit the PCB to the heat sink on short spacers that leave enough space between the board and the heat sink for access to the transistor terminals for soldering them to the board.

Fit the resulting assembly in an enclosure as specified in the parts list in such a way that the spindles of the potentiometers and the rotary switch protrude through the front panel far enough to enable knobs to be fitted to them. Note that the heat sink must be insulated from the enclosure since the drain of the FET

is connected internally to the housing.

Finally, wire up the controls and sockets: the supply on-off switch, the LED, two (car-type) spade terminals for connecting the power supply on test (use heavy-duty wire), and the three coaxial sockets for the measurement outputs ($K_1$–$K_3$). The coaxial sockets are best wired with screened cable since fairly high frequencies may occur.

Fit a suitable socket at the rear of the enclosure for the mains adaptor plug. The adaptor need not be able to provide high currents: 50 mA is sufficient. DO NOT TAKE THE SUPPLY VOLTAGE FROM THE POWER SUPPLY ON TEST!

## Using the electronic load

An oscilloscope is indispensable for viewing the waveforms. The simplest test is inspecting the waveform of the output voltage when the load is being switched on and off. To do this, connect the signal at $K_3$ to Channel 1 of the oscilloscope, so that the scope is triggered by the square-wave switching signal (it is also possible to trigger the scope by the signal at $K_1$). Connect Channel 2 to $K_2$ or to the outputs of the power supply on test. Connect a multimeter, set to 2 V d.c., to $K_3$. Set $P_1$ to zero before switching on the power supply on test. Then switch on the supply to the load and the power unit on test. Adjust the output of the power unit to, say, half the maximum permissible value, set the frequency switch on the load to the calibration position and adjust $P_1$ and $P_2$ so that a current flows which the unit on test can provide comfortably, say, 1 A or 5 A. Do not leave the load in the calibration position for too long to avoid the FET getting too hot. Then, switch to the various frequencies in turn and observe at each of them how the output voltage voltage and current behave. Depending on the output impedance of the power unit, the output voltage will drop slightly when the load is connected. If there are irregularities in the output voltage and current around the switching points, this points to the fact that the power unit is not able to cope satisfactorily with changes in the load. This may become particularly pronounced at high frequencies, because the control electronics then cannot follow the switching rate.

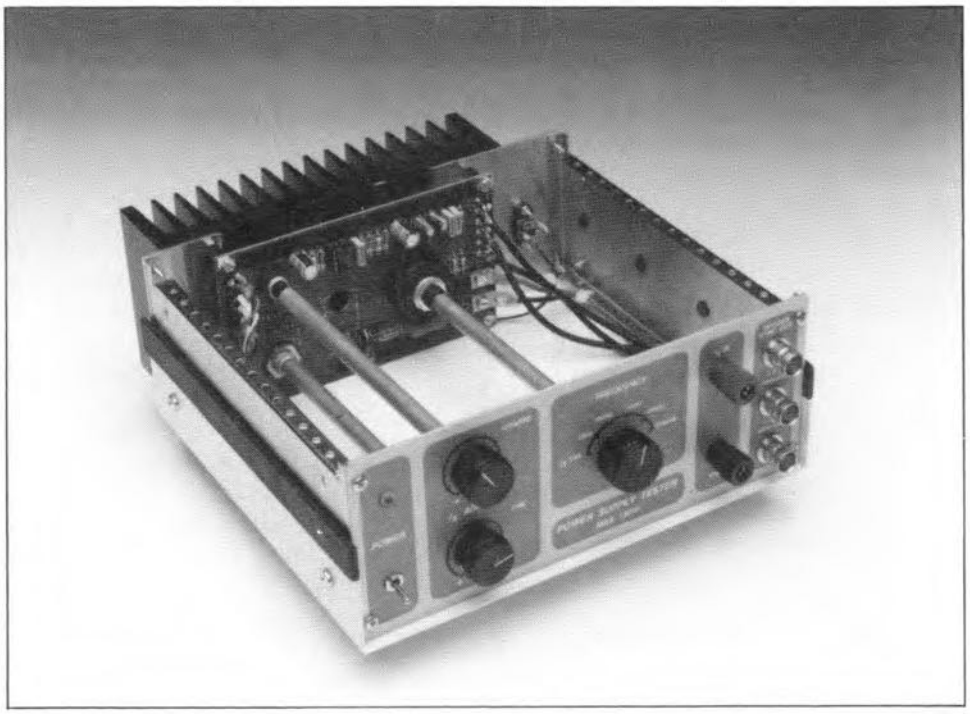


**Fig. 3. The prototype of the electronic load with the cover removed.**

It is also possibe to use the *x*-*y* setting of the oscilloscope ($K_2$ signal drives *y* and $K_3$ signal drives *x*). The oscilloscope trace will look like an hysteresis curve: the closer it is to a straight line (ideal case) the better the power unit is.

The maximum current that the FET can handle continuously is 10 A. Moreover, the rating of 130 W on the front panel applies to peak currents, not to average currents. This should be borne in mind especially during calibration.

**END**

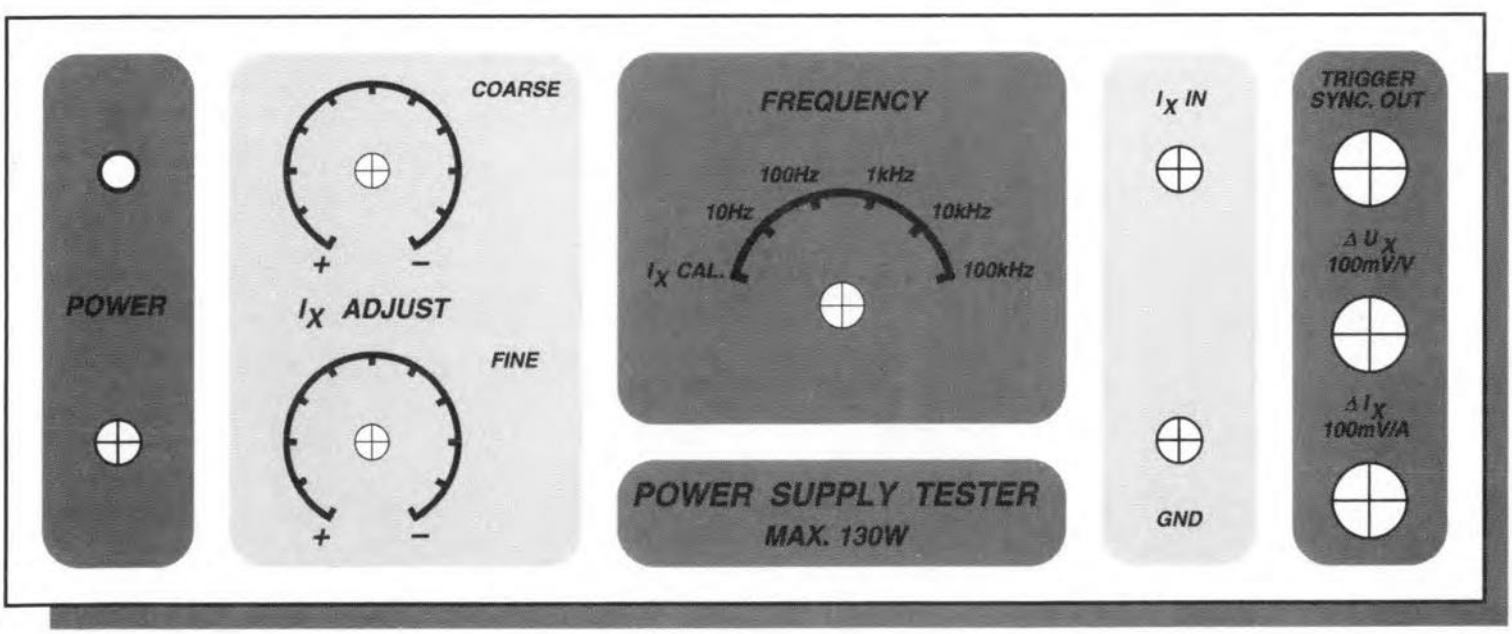



**Fig. 4. Suggested front panel for the electronic load (true scale).**

$D_1$ = LED, 3 mm
$D_2$–$D_4$ = 1N4148
$D_5$ = see text
$T_1$ = BUZ384

**Integrated circuits**:
$IC_1$ = 555

**Miscellaneous**:
$S_1$ = single-pole on-off switch
$S_2$ = 2-pole, 6-position rotary switch
$K_1$–$K_3$ = BNC socket for PCB mounting
2 off spade terminal (male and female) for PCB mounting
Heat sink for $T_1$ (SK85*, 75 mm high)
Enclosure 80×200×132 mm (H×W×D)

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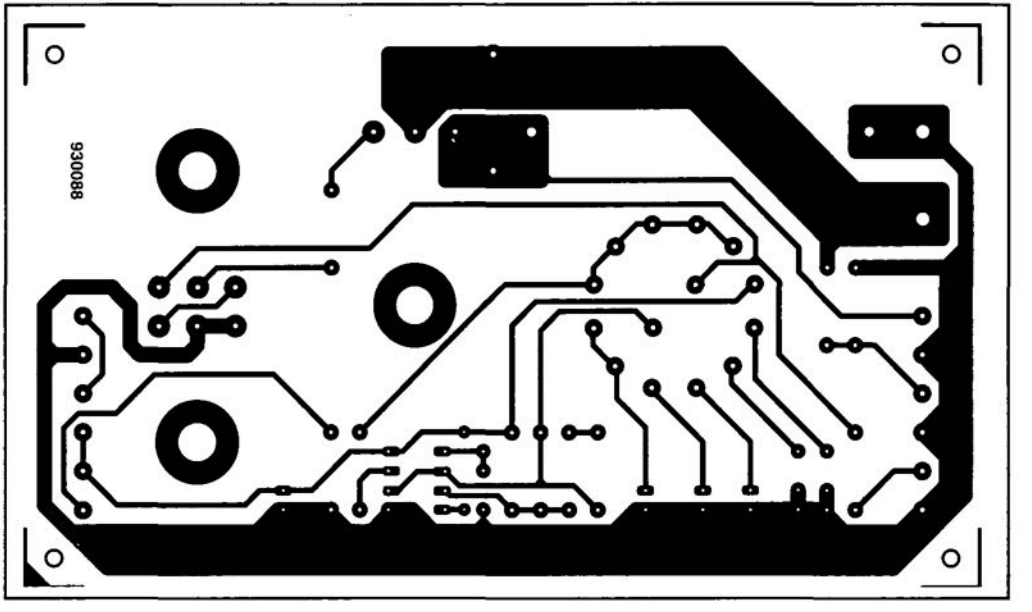


# VHF/UHF TELEVISION TUNER (PART 2 — FINAL)

**This second and final part of the article deals with the construction and mechanical finishing of the TV tuner. Also, we tell you how to operate and program the tuner via the built-in menu.**

**Design by W. Sevenheck**

The tuner is built on four printed circuit boards, which are supplied as two pairs. **Figure 7** shows the artwork of the single-sided processor board and the keyboard, while the artwork for the double-sided, through-plated main board and supply board is given in **Fig. 8**. Although populating these four printed circuit boards should not cause problems to the experienced constructor, there are a few simple rules to observe.

## Processor board

Start by separating the keyboard and the processor boards. This is easy thanks to the fraised seam between the two sections. There are no fewer than nine screw holes in the keyboard section. If you can make do with six, cut off the 'empty' part at the left-hand side of the small board. Next, mount the five press-keys and the two LEDs. The position of the LEDs is best determined by looking at the layout of the tuner's front panel. The last part fitted on to the keyboard PCB is the single-in-line 4-way PCB header.

On the processor board, it is recommended to fit a 40-pin IC socket for the 8751 microcontroller. The polarity of boxheaders K1, K2 and K3 is clearly marked on the component mounting plan. After fitting jumper JP1, the two resistor arrays may be soldered on to the board. Fitting the remainder of the parts is straightforward, and requires no further comment. The terminals of the LED on the processor board are bent such that the LED protrudes from the front panel. The function of this LED is to acknowledge reception of a valid (RC5) infra-red command signal.

The processor board and the keyboard are interconnected via seven wires. This connection is not made until all boards are installed in the 14-inch rack enclosure. The same goes for the LC display connection, which only requires a short length of flatcable.

## Main board

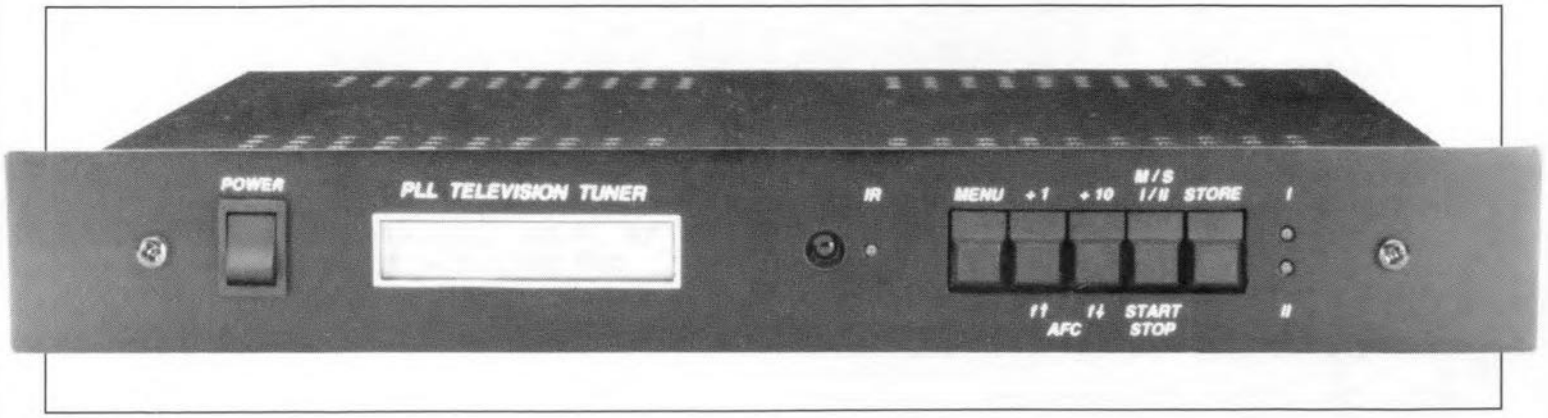
Separate the main board and the supply board along the fraised seam between them. Alternatively, if your enclosure has sufficient space, leave the board whole. Note, however, that a few wires are required to connect the main board to the supply board, irrespective of whether these are separated or not. Voltage regulators IC5 and IC6 are fitted with TO-220 style heat-sinks, which can be bolted on to the main board. To prevent strain on the solder joints caused by heating, align each regulator on to the heat-sink, and secure the two **before** soldering the terminals.

Pay attention to the polarity of the SAW filters, Fl1 and Fl2, before mounting these components. The polarity is indicated by a dot on the component overlay.

Having fitted all parts on to the boards, it is time to concentrate on the

## MAIN SPECIFICATIONS

| | |
|---|---|
| TV bands: | VHF-1, VHF-3 and UHF<br>47 MHz to 170 MHz<br>170 MHz to 450 MHz<br>450 MHz to 860 MHz |
| TV channels: | 2 through 120 (incl. Hyperband) |
| TV standards: | PAL, NTSC, SECAM |
| Presets: | 100 |
| Sound: | mono, analogue stereo, analogue two-language |
| Remote control: | RC5 compatible |
| Display: | 2-line alphanumerical LCD |
| Outputs: | CVBS, audio left and right (cinch sockets) |
| Input: | coax, 75Ω |
| Menu language: | English or German |



screening. Cut 1.5 to 2-cm high strips of tin-plate sheet or thin brass, and bend these as indicated by the dashed lines on the PCB overlay. The screening is essential, and helps to keep mutual interference between sub-circuits to a minimum. The SAW filters must be completely surrounded by screens, for which separate pieces of sheet metal must be bent.

To prevent interference in the audio demodulator section, the video output signal produced by the IF section is carried to cinch socket K2 via a length of screened cable. The cable ends are soldered to the points marked with an arrow (➡) and a ground symbol (near R28 and K2 respectively). In this way, the video signal can go safely across the analogue sound stage.

Check the type numbers of the ceramic filters and the Toko inductors to make sure that these parts go to the right PCB positions. An error is easily made at this stage because these parts look almost identical. The connecting pins of the Philips tuner module, X1, are soldered directly to the relevant solder spots. The two large metal tabs at the sides of the metal box are soldered to the ground plane at the component side of the board. For this operation you may need a high-power soldering iron. The rest of the parts on the main board should not cause problems. The polarity of the boxheader, K1, is indicated by the component overlay printed on the ready-made PCB.

The holes in positions D1 and D2 on the main board are used for wires that connect to LEDs D2 and D3 respectively on the keyboard via connector K4. This connection is best made by a length of 4-wire flatcable fitted with an IDC socket at the side of K4 on the keyboard PCB.

The parts list gives alternative types

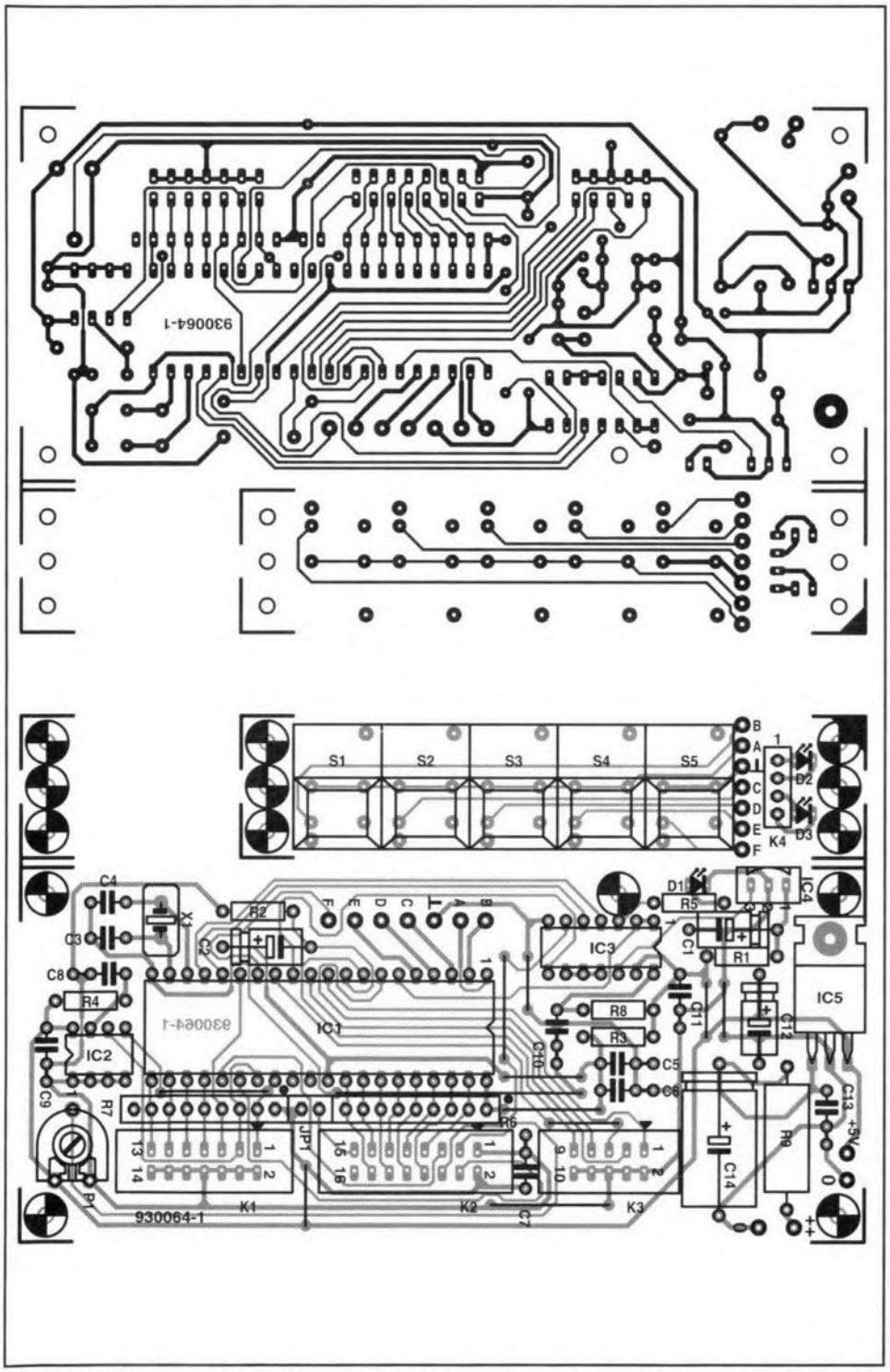



Fig. 7. The first PCB combination contains the processor board and the keyboard. These two boards are easily separated using the seam between them.

## COMPONENTS LIST

PROCESSOR BOARD

**Resistors:**

| | | |
|---|---|---|
| 1 | 150Ω | R1 |
| 1 | 8kΩ2 | R2 |
| 1 | 4Ω7 | R3 |
| 1 | 47kΩ | R4 |
| 1 | 390Ω | R5 |
| 1 | 10kΩ 8-way SIL array | R6 |
| 1 | 4kΩ7 8-way SIL array | R7 |
| 1 | 10Ω | R8 |
| 1 | 6Ω8 5W | R9 |
| 1 | 10kΩ preset H | P1 |

**Capacitors:**

| | | |
|---|---|---|
| 1 | 4µF7 63 V | C1 |
| 2 | 10µF 63 V | C2;C12 |
| 2 | 22pF | C3;C4 |
| 4 | 100nF ceramic | C5;C7;C10;C13 |
| 1 | 220nF | C6 |
| 1 | 3nF3 | C8 |
| 2 | 47nF ceramic | C9;C11 |
| 1 | 470µF 25 V | C14 |

**Semiconductors:**

| | | |
|---|---|---|
| 1 | LED, high efficiency 3mm | D1 |
| 2 | LED, high efficiency 3mm | D2;D3 |
| 1 | 87C51H (supplied ready-programmed, order code 7141, see page 70) | IC1 |
| 1 | PCF8582A (Philips Semiconductors)[1] | IC2 |
| 1 | 74HCT00 | IC3 |
| 1 | SFH505A (Siemens)[2] | IC4 |
| 1 | 7805 | IC5 |

**Miscellaneous:**

| | | |
|---|---|---|
| 1 | Jumper | JP1 |
| 1 | Boxheader 14-way | K1 |
| 1 | Boxheader 16-way | K2 |
| 1 | Boxheader 10-way | K3 |
| 1 | SIL-header 4-way | K4 |
| 5 | Digitast press-key (w=12mm) [1] | S1-S5 |
| 1 | Quartz crystal 10 MHz | X1 |
| 1 | LCD module with backlight, 2×16 characters, e.g., LM086ALN | |
| 1 | Printed circuit board 930064-1 (see page 70) | |

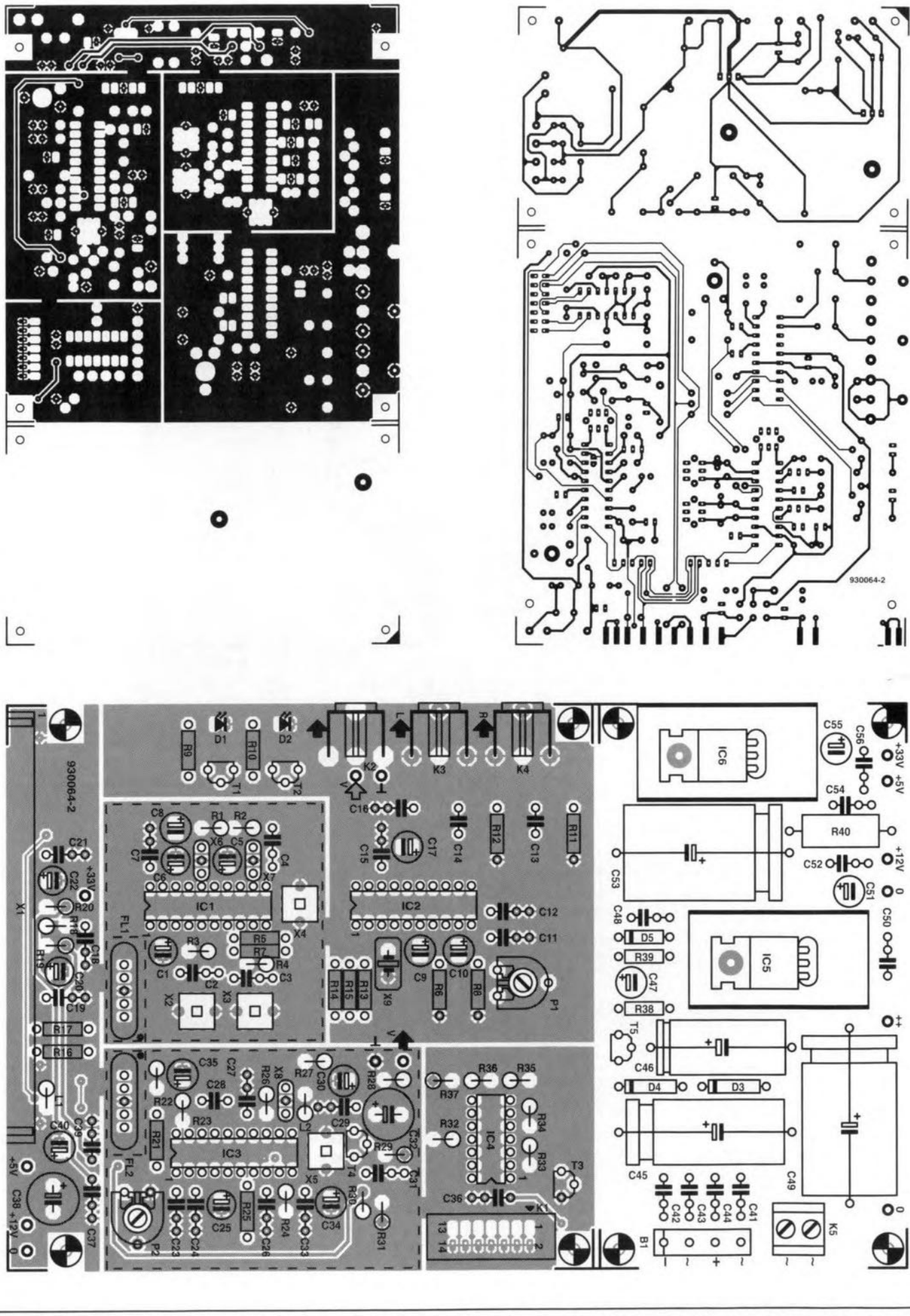



Fig. 8. Artwork of the double-sided and through-plated main board and supply board combination (track layouts shown at 70% of true size).

for inductors X2 through X5. The replacements for X4 and X5 are pin-compatible. Those for X2 and X3, however, have pins 4 and 6 soldered in the holes for pins 1 and 3.

If X8 can not be obtained, it may be replaced by a 270-Ω resistor connected between the input and the output.

Problems may occur regarding availability of the Siemens SAW filters. In the original design, the Types OFWG9250 and OFWG1963 are used. Unfortunately these devices are not Siemens 'preferred products', which means that series of these filters are only manufactured to customer orders, after which they are available for some time. Consequently, it may take a while before they are available again when they are out of stock at the time an order is placed. The upshot is that new batches of non-preferred products are not made until there is sufficient demand. Fortunately, both filters may be replaced by near equivalents that are better available: the OFWG9250 may be replaced by the OFWG9253, and the OFWG1963, by the OFWG1962. These near equivalents gave entirely satisfactory operation when compared with the types originally designed into the circuit. Equivalent types for the UK CCIR-I TV

## COMPONENTS LIST

RECEIVER BOARD

**Resistors:**

| | | |
|---|---|---|
| 2 | 560Ω | R1;R2 |
| 1 | 510Ω | R3 |
| 1 | 470Ω | R4 |
| 3 | 4kΩ7 | R5;R6;R8 |
| 1 | 2kΩ2 | R7 |
| 2 | 390Ω | R9;R10 |
| 2 | 1MΩ | R11;R12 |
| 1 | 5kΩ6 | R13 |
| 4 | 47Ω | R14-R17 |
| 2 | 22kΩ | R18;R22 |
| 2 | 2Ω2 | R19;R20 |
| 1 | 6kΩ8 | R21 |
| 1 | 1kΩ2 | R23 |
| 1 | 15kΩ | R24 |
| 3 | 1kΩ | R25;R33;R37 |
| 1 | 220Ω | R26 |
| 1 | 10Ω | R27 |
| 1 | 68Ω | R28 |
| 1 | 150Ω | R29 |
| 2 | 22kΩ1 1% | R30;R31 |
| 2 | 100Ω | R32;R39 |
| 1 | 120Ω | R38 |
| 1 | 5Ω6 5W | R40 |
| 2 | 820Ω | R34;R36 |
| 1 | 1kΩ5 | R35 |
| 1 | 5kΩ preset H | P1 |
| 1 | 25kΩ preset H | P2 |

**Capacitors:**

| | | |
|---|---|---|
| 3 | 4µF7 63V radial | C1;C20;C22 |
| 2 | 1nF | C2;C3 |
| 1 | 100nF | C4 |
| 3 | 2µF2 63V radial | C5;C6;C25 |
| 1 | 10nF ceramic | C7 |
| 2 | 22µF 25V radial | C8;C34 |
| 5 | 10µF 63V radial | C9;C10;C47; C51;C55 |
| 3 | 47nF | C11;C12;C26 |
| 2 | 2µF2 | C13;C14 |
| 3 | 220nF | C15;C18;C23 |
| 6 | 47nF ceramic | C16;C41-C44; C56 |
| 2 | 47µF 25V radial | C17;C35 |
| 10 | 100nF ceramic | C19;C21;C29; C31;C33;C36; C37;C39;C48; C54 |
| 2 | 330nF | C24;C52 |
| 1 | 10nF | C27 |
| 1 | 1µF | C28 |
| 2 | 100µF 10V radial | C30;C40 |
| 1 | 220µF 10V radial | C32 |
| 1 | 220µF 25V radial | C38 |
| 1 | 470µF 40V | C45 |
| 1 | 220µF 40V | C46 |
| 1 | 1000µF 35V | C49 |
| 1 | 470nF | C50 |
| 1 | 1000µF 16V | C53 |

**Inductors:**

| | | |
|---|---|---|
| 1 | 4µH7 | L1 |
| 1 | 15µH | L2 |
| 2 | 113CNS-K1272HM-81091 or 07202-342 [1] | X2;X3 |
| 2 | 199KCAS-A359HM-81088 or 199KCS-A877-2C [1] | X4;X5 |

**Semiconductors:**

| | | |
|---|---|---|
| 1 | B80C1500 | B1 |
| D1;D2 = D2;D3 on keyboard PCB | | |
| 2 | 1N4001 | D3;D4 |
| 1 | ZTK33 | D5 |
| 4 | BC547B | T1-T4 |
| 1 | BF256B | T5 |
| 1 | TDA3857 (Philips Semiconductors)[1] | IC1 |
| 1 | TDA8415 (Philips Semiconductors)[1] | IC2 |
| 1 | TDA3842 (Philips Semiconductors)[1] | IC3 |
| 1 | LM339 | IC4 |
| 1 | 7812 | IC5 |
| 1 | 7805 | IC6 |

**Miscellaneous:**

| | | |
|---|---|---|
| 1 | Boxheader 14-way | K1 |
| 3 | PCB-mount cinch socket | K2-K4 |
| 1 | 2-way PCB terminal block, pitch 7.5mm | K5 |
| 1 | TV tuner module UV816PLL (Philips Components)[1] | X1 |
| 1 | SFE5.74 (Stettner-Murata) | X6 |
| 1 | SFE5.5 (Stettner-Murata) | X7 |
| 1 | TPS5.5MB (Stettner-Murata) | X8 |
| 1 | Quartz crystal 10 MHz | X9 |
| 1 | OFWG9250 (Siemens) | FL1 |
| 1 | OFWG1963 (Siemens) | FL2 |
| 2 | Heatsink for IC5 and IC6. | |
| 1 | Mains transformer 15V/15VA (not on PCB) | |
| 1 | Mains socket with integral fuseholder | |
| 1 | Enclosure Type ET32/04 (21 cm deep) (ESM) | |
| 1 | Printed circuit board 930064-2 (see page 70) | |

Printed circuit boards 930064-1 and -2, and a programmed 87C51H are available as a package under order code: 930064 (see page 70). The programmed 87C51H is also available separately under order code 7141 (see page 70).

Component changes for PAL TV system I used in the UK (sound carrier at 6.0 MHz):
FL1: OFWG9253 (Siemens)
FL2: OFWJ1952 (Siemens)
X7: SFE6.0 (Stettner-Murata)
X8: TPS6.0MB (Stettner-Murata)

[1] C-I Electronics, P.O. Box 22089, 6360 AB Nuth, Holland. Fax: (+31) 45 241877.
[2] Electrovalue, see advert on page 53

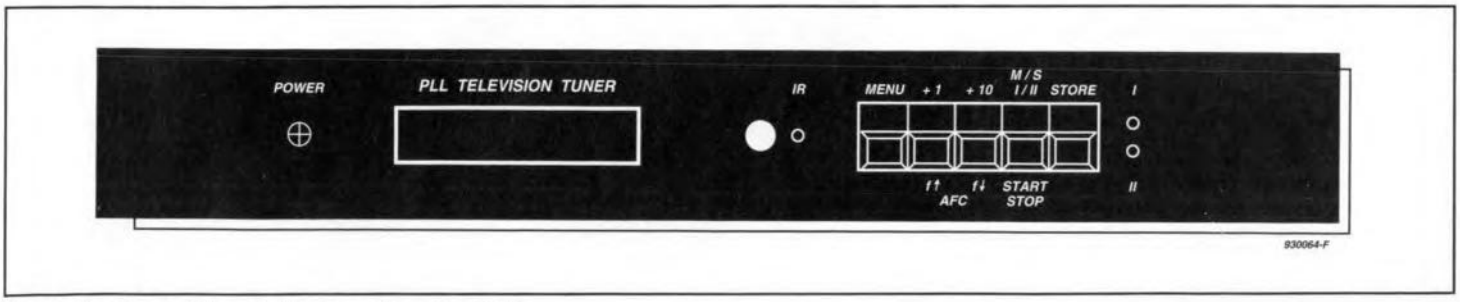



Fig. 9. Front panel layout (shown reduced to 50%).

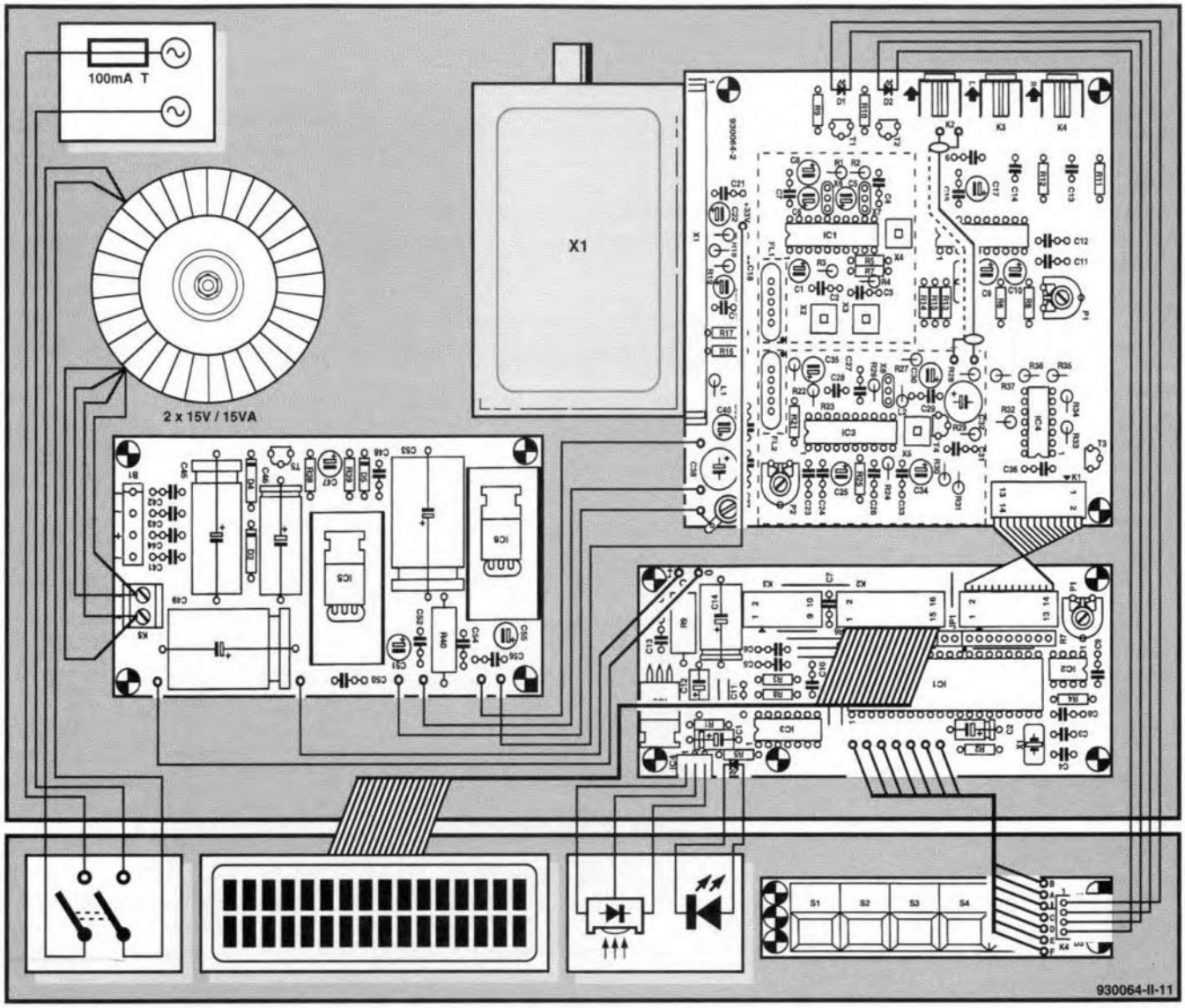



**Fig. 10. Wiring diagram of the TV tuner.**

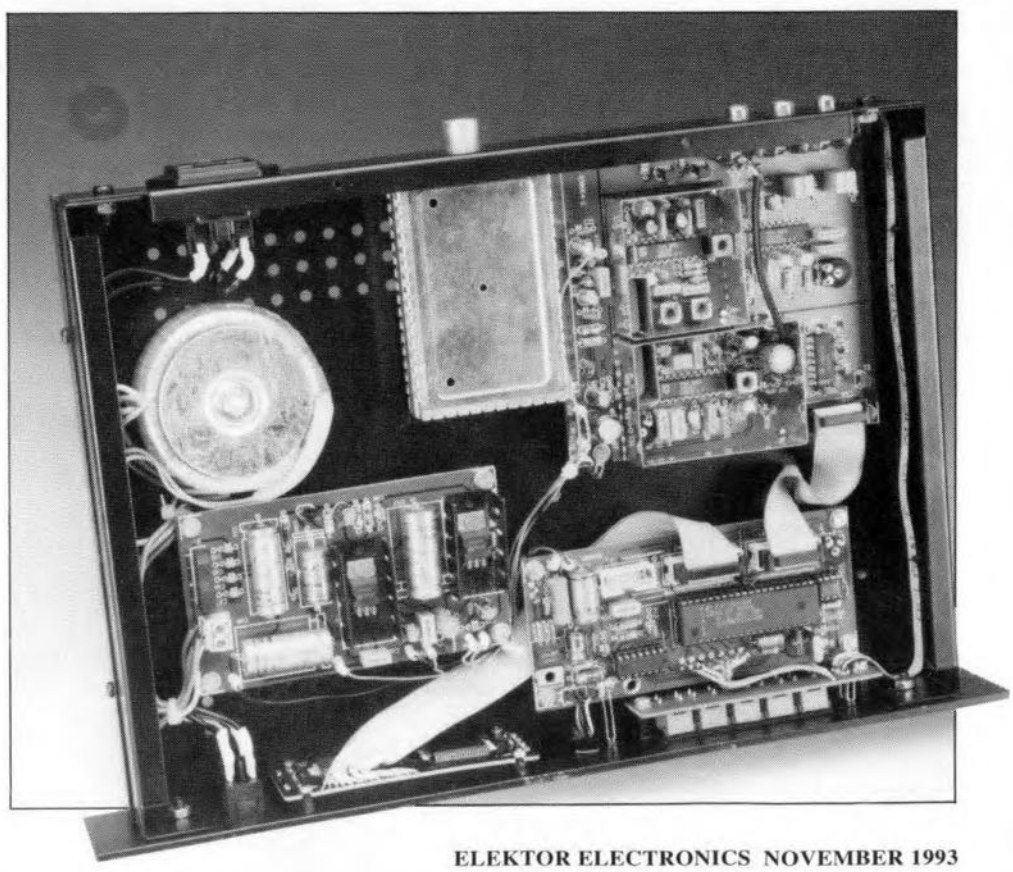
standard (vision-sound spacing 6.0 MHz) are also given in the parts list.

That completes the construction of the printed circuit boards, leaving you with mechanical work on the enclosure, mounting the boards into the case, and, of course, adjustment of the TV tuner.

## Mechanical work and wiring

The TV tuner is built into a matt black 13-inch rack type case from ESM France (type number ET32/04). A suggestion for the front panel layout and lettering is shown in **Fig. 9**. The arrangement of the four boards inside the case is evident from last month's front cover photograph.

Five holes have to be drilled in the rear panel: three for the audio and video outputs, one for the tuner's RF input (antenna socket), and a much larger one for the mains socket with integral fuseholder. The LCD and the five press-keys require two slots to be



cut in the front panel. Further, you need to drill three holes for the LED indicators, and one for the IR receiver, while a rectangular clearance is cut to accommodate the mains on/off switch.

Once all four boards, the mains transformer and the parts on the front and rear panels have been mounted, you are ready to start working on the wiring — see **Fig. 10**. All mains carrying wires and terminals should be properly insulated, and the case must be connected to the mains earth. Run a thorough check on the wiring before you apply power.

## Test and adjustment

Connect the coax input of the TV tuner to your antenna system. Apply power. If the LCD backlight does not work, actuate it by fitting jumper JP1. Start by turning the AGC preset (P2) to the centre of its travel. Next, connect a voltmeter between pin 8 of the TDA3842 (IC3) and ground. Turn off the AFC via the keyboard, and tune to a known TV station in the UHF band. Do not use the 'search' function to find a station. Instead, enter the channel number **directly**. Be sure to tune to a strong ('local') station which transmits on a standard channel number. This warning applies to those of you who connect the tuner to a cable network, where channel numbers such as 46+ and 66– are used to indicate positive or negative 1-MHz offsets from the CCIR standard frequencies. Do not select a station transmitting on a '+' or '–' channel. Next, connect a video monitor or TV set to the tuner's video output. Use a plastic trimming tool to adjust the core in the IF filter, X5, for a voltmeter reading between 2.4 V and 2.6 V, which indicates resonance at 38.9 MHz exactly. This is essential for the 'search' function and the AFC. If the picture on the monitor is noisy, the AGC adjustment must be corrected with the aid of preset P2. The operation of the AGC may be verified by tuning to another station, and checking if the received picture is all right again. If so, you may disconnect the voltmeter.

Next, adjust the sound receiver. Start with the IF section of the sound circuit. Be sure to tune to a stereo or two-language broadcast. Connect an oscilloscope to pin 15 of the TDA3857 (IC1). Adjust the 38.9-MHz filter until the 5.5-MHz and 5.74-MHz IF signals are in phase. If this is difficult to see on the scope screen, it is also possible to adjust the filter for the highest signal level measured at pins 13 and 17.

Next, adjust filters X2 and X3. Connect the scope to pin 5 of IC1, and adjust X2 for the highest possible signal level. Similarly, connect the scope to IC1 pin 9, and peak X3. At this point, the LEDs and the display should indicate reception of a stereo or two-language broadcast. Reception of a stereo broadcast is indicated by both LEDs lighting, while only one LED lights (depending on the selected channel) if the broadcast has two-language sound.

Finally, optimize the channel separation by adjusting P1 for best results. In practice, good results are obtained with this preset set to the centre of its travel.

## Operation

The use of a microcontroller allows all tuner functions to be selected and controlled with the aid of only five press keys on the front panel. The press keys have the following functions:

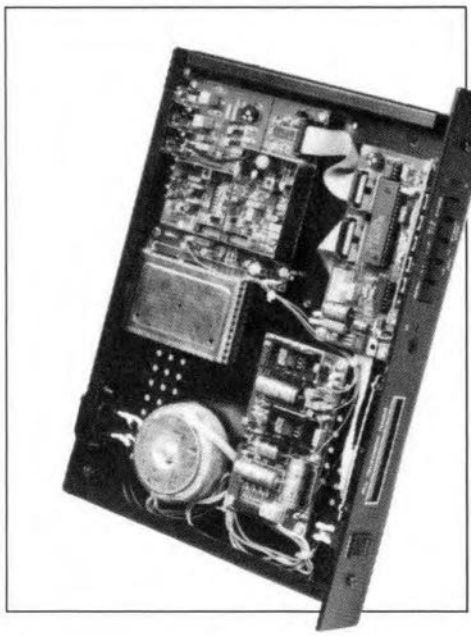
Key 1: menu selection
Key 2: menu-dependent
Key 3: menu-dependent
Key 4: menu-dependent
Key 5: store

**Main menu**
Key 1: menu selection
Key 2: programme number +1
Key 3: programme number +10
Key 4: mono/stereo or channel 1/2 switch
Key 5: no function
*Display shows:* program number; AFC and mono/stereo or two-language.

**Channel menu**
Key 1: menu selection
Key 2: channel number +1
Key 3: channel number +10
Key 4: no function
Key 5: store channel number with previously selected programme number
*Display shows:* channel and programme numbers; lower line: frequency.

**Search menu**
Key 1: menu selection
Key 2: frequency +62.5 KHz
Key 3: frequency –62.5 KHz
Key 4: search start/stop
Key 5: store channel number with any shift (62.5 kHz resolution)
*Display shows:* 'searching' flashes on start of search, programme and channel numbers; lower line: frequency.

**Language menu**
Key 1: menu selection
Key 2: switch on AFC
Key 3: switch off AFC
Key 4: select between English and German
Key 5: store setting
*Display shows:* language selection and AFC on/off.



## General user information

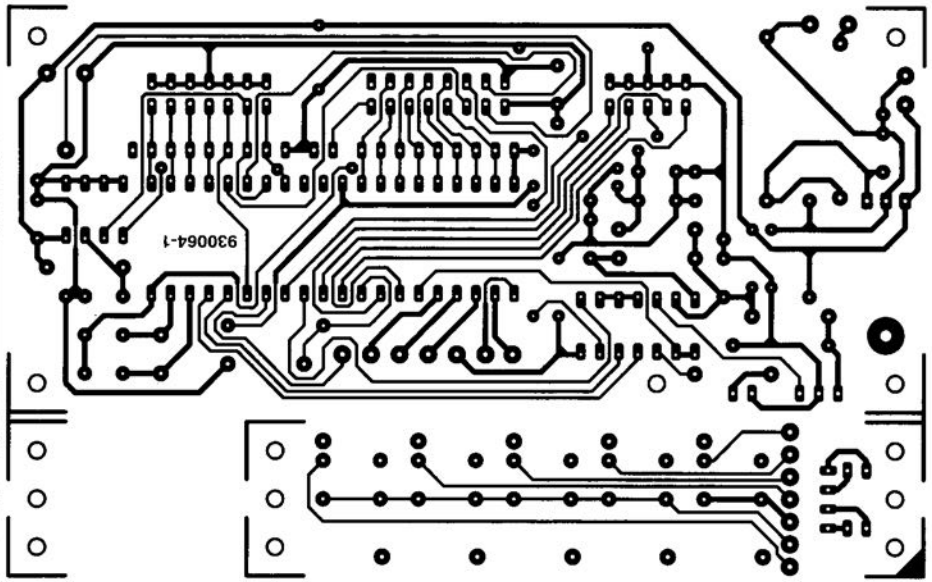
Pressing the 'store' key while in the search menu, channel menu or language menu automatically takes you back to the main menu. The audio output is muted during searching until a station is encountered. The search function has two speeds; it starts at high speed until a station is found, and then switches to low speed. If the received signal is too weak, or not from a TV station, the tuner switches to high speed searching again.

If you tune to a TV station from the main menu, the selection is automatically stored after 12 seconds. The station is immediately available the moment the TV tuner is switched on again.

The AFC is only active in the main menu, provided it has been enabled in the language menu. The frequency range of the AFC is ±375 kHz, and its tuning effect is visible on the LC display: a '>' indicates a tuning frequency above the standard frequency; a '<' a tuning frequency below the standard frequency. A '*' is shown if the tuned frequency is in accordance with the CCIR channel raster. The AFC action is delayed a few seconds after a programme number is selected.

One hundred presets (0-99) are available for television channels between CCIR E2 and 120, which includes the so-called S channels, S1-S20, and the channels in the hyperband, H1-H21.

Finally, the tuner responds to the following commands received via the RC5 infra-red receiver: programme number up/down, sound on/off, stereo/mono, channel 1 or 2, numbers 0 through 9, 1 or 2-digit input, and switching between the last two selected programmes. ■




PROCESSOR BOARD

**Resistors:**

| | | |
|---|---|---|
| 1 | 150Ω | R1 |
| 1 | 8kΩ2 | R2 |
| 1 | 4Ω7 | R3 |
| 1 | 47kΩ | R4 |
| 1 | 390Ω | R5 |
| 1 | 10kΩ 8-way SIL array | R6 |
| 1 | 4kΩ7 8-way SIL array | R7 |
| 1 | 10Ω | R8 |
| 1 | 6Ω8 5W | R9 |
| 1 | 10kΩ preset H | P1 |

**Capacitors:**

| | | |
|---|---|---|
| 1 | 4µF7 63 V | C1 |
| 2 | 10µF 63 V | C2;C12 |
| 2 | 22pF | C3;C4 |
| 4 | 100nF ceramic | C5;C7;C10;C13 |
| 1 | 220nF | C6 |
| 1 | 3nF3 | C8 |
| 2 | 47nF ceramic | C9;C11 |

930064-2

amplifier?). The output pulse is picked up by a microphone and fed back into the IMP where it is digitized and then fed into an IBM (compatible) computer via the printer port. The IMP software then analyses the input via Fourier transforms and outputs the results on to the computer screen in graphical form in the shape of amplitude and phase response curves. Full control is via the PC. The amplifier output can be sampled via a probe to correct for errors in the pulse spectrum and amplifier response.

IM P allows the collection and analysis of 12-bit analogue data up to 4,095 samples in length and sample rates are selectable at either 61.441 kHz or 1.92 kHz which, along with the internal filtering, allows measurements from several hertz to 20 kHz.

Further information from Falcon Acoustics Ltd, Tabor House, Norwich Road, Mulbarton, Norfolk NR14 8JT, England. Telephone +44 (0)508 78272; fax +44 (0)508 70986.

# CORRECTIONS

**DIGITAL DIAL** (January 1994)

An attentive reader has drawn our attention to the fact that the digital dial can not be used in conjunction with the receiver illustrated (a Yaesu Type FRG-7) since the IF of that receiver is much too high for the dial. Sorry for that oversight! [Editor]

**VHF/UHF TUNER** (Oct/Nov 1993)

The tuner module used in this design is no longer in production with Philips and its availability will thus become a problem. Fortunately, the Type UV916H is an excellent alternative. The snag is, however, that this unit is slightly smaller than the UV816, so that the antenna connector no longer protrudes from the enclosure. This can be overcome by terminating the antenna cable into a coaxial plug and making the entrance hole slightly larger. Moreover, one of the two earth tags of the UV916H must be connected at a different position.

# LETTERS

**SCART SWITCHING BOX**
(December 1993)

I have a few problems with this project, which I believe have to do with the connections. Pin 1 of one connector is linked to pin 2 of the other. The same is true of pins 3 and 19, which are linked to pins 6 and 20 respectively. All other pins are interlinked as one would expect, i.e., pin 5 to pin 5, pin 10 to pin 10, and so on.
L. Bastiaenssen

*In a SCART cable, the wires for the video and audio connections are always crossed. That is why the video output (pin 19) at one end of the cable is linked to the video input (pin 20) at the other end. This arrangement ensures that the input of one piece of equipment is always connected properly to the output of another. There is, therefore, nothing wrong with your cable.*

*Note that two pieces of equipment must never be connected simultaneously to $K_3$ and $K_5/K_6$. Use SCART connector $K_3$ **or** the phono plugs $K_5/K_6$, but not both at the same time!* [Editor]

**PRECISION CLOCK FOR PCs**
(November 1993)

I have encountered a problem with the Precision clock for PCs. I have an IBM (compatible) PC486 and have, as stated in the article, complemented the CONFIG.SYS file with the following (last) line:
DEVICE C:\MSDOS\DCFCLOCK.SYS.

I should be pleased if you would tell me:
1. Whereto should the files of the software provided (DCFCLOCK.ASM, DCFCLOCK.DOC and DCFCLOCK.SYS be copied? To the root, the MSDOS or a separate directory?
2. Once the files have been loaded, how is the program called up to initialize the driver and to fill the options P, I, S, B and D?
(M. Meersschaut)

*The file DCFCLOC.ASM is the assembler listing of the program, which you no longer need (it is of interest only to dyed-in-the-wool programmers). The file DCFCLOCK.DOC contains the instructions for the program, which you can read with a word processing program. It is not necessary to store this file on a hard diksk.*

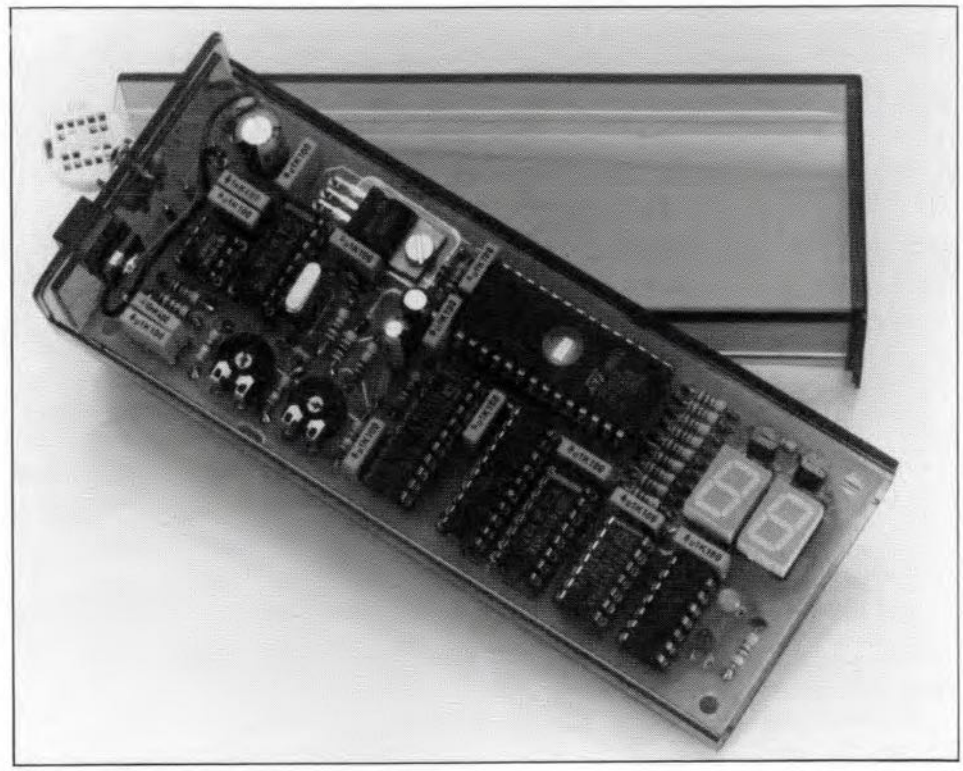
*The only program that you need to copy to the hard disk is DCFCLOCK.SYS. Place this file in the directory containing the DOS commands (e.g., C:\DOS). Add a line that indicates where the computer can find that program to CONFIG.SYS (in C:\), e.g. DEVICE = C:\DOS\DCFCLOCK.SYS. Other suffixes may be added for changing certain settings (see DOC file), but even without these the system should work correctly.*

*Note, however, that the receiver circuit must be connected to the COM port 2 and that the computer must be restarted after the software has been installed. The program will then automatically set the correct time in the internal clock of the PC every minute.*

[Editor]

# DIGITAL HYGROMETER

**Design by A. Rietjens**



The temperature of the human body is maintained at about 36.9 °C (98.4 °F), whatever the temperature of the surroundings and the nature of the thermal insulation with which it is clad. Heat is continually generated by the chemical actions which occur in the body, and this must be dissipated as fast as it is produced if the temperature is to remain steady. This dissipation is achieved largely by the evaporation from moist internal surfaces of water which is exhaled, and by evaporation of perspiration from the skin. If the evaporation is too rapid, as wehn one sits in a draught, a sense of chill and discomfort is felt. If the evaporation is not rapid enough, as in a small inadequately ventilated room, the even more acute discomfort of stuffiness is produced. This has little to do with the actual temperature or with the accumulation of carbon dioxide, for it is experienced in the open air at all temperatures in moist climates. It is because the air is so near saturation that the necessary evaporation from the body is reduced below the comfort level. The factor that determines personal comfort is not how much water vapour the air contains, but how much more there is room for at that temperature; in other words, how far the air is from being saturated with water vapour.

**Our personal comfort is determined not so much by the ambient temperature as by the relative humidity of the air surrounding us.**

The moisture content relative to that of saturated air, expressed as a percentage and called the **relative humidity** (r.h.), is thus the really important quantity that controls the evaporation of water from a surface. Relative humidity can be determined by an **hygrometer**. There are various types of this instrument, of which a modern one, based on digital electronics, is described in this article.

## Relative humidity sensor

The r.h. sensor used in the present design is an element whose capacitance changes with humidity. It consists of an air permeable housing that contains a non-conductive foil, which is sensitive to humidity, with a thin layer of gold at both sides. The gold layers form the electrodes and the foil the dielectric of a capacitor. The dielectric constant of the foil, and thus the capacitance, changes with varying relative humidity—see **Fig. 2**.

The capacitance is used to vary the frequency of an oscillator, here based on the HCT version of a Type 4060 IC.

There are two problems that need to be solved. The first is that the change in capacitance is not linearly proportional to the relative humidity. This is solved by the use of a linearization table contained in an EPROM. The second is the large production spread of the sensors, which is reflected in **Fig. 2** by the three curves. This is solved by the use of a capacitance factor instead of the absolute capacitance of the sensor. The calculations correlating the dielectric constant, relative hu-

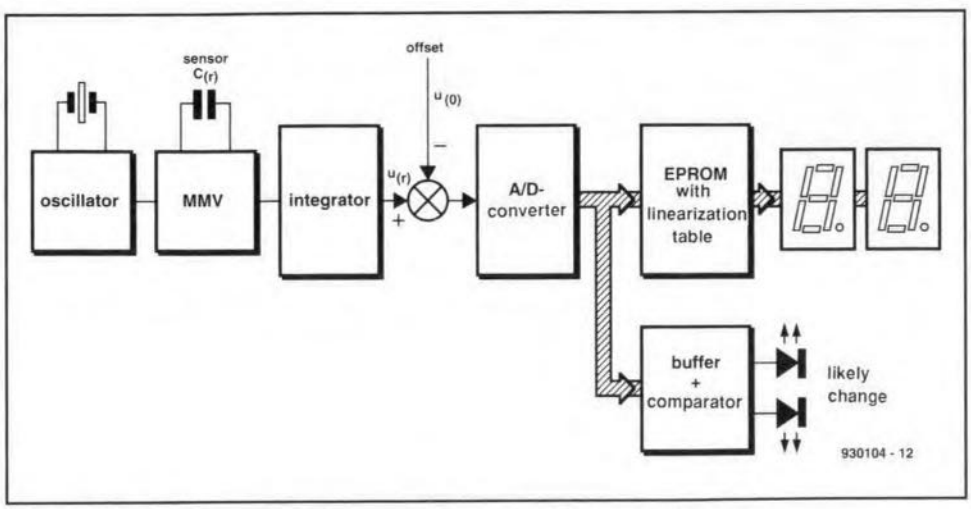



**Fig. 1. Block schematic diagram of the digital hygrometer.**

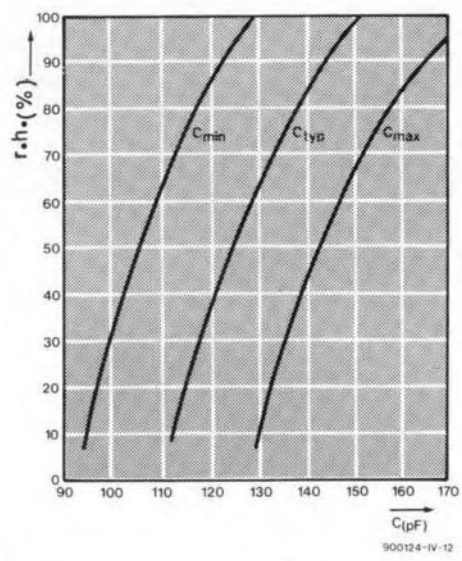



**Fig. 2. Capacitance of the sensor as a function of relative humidity.**

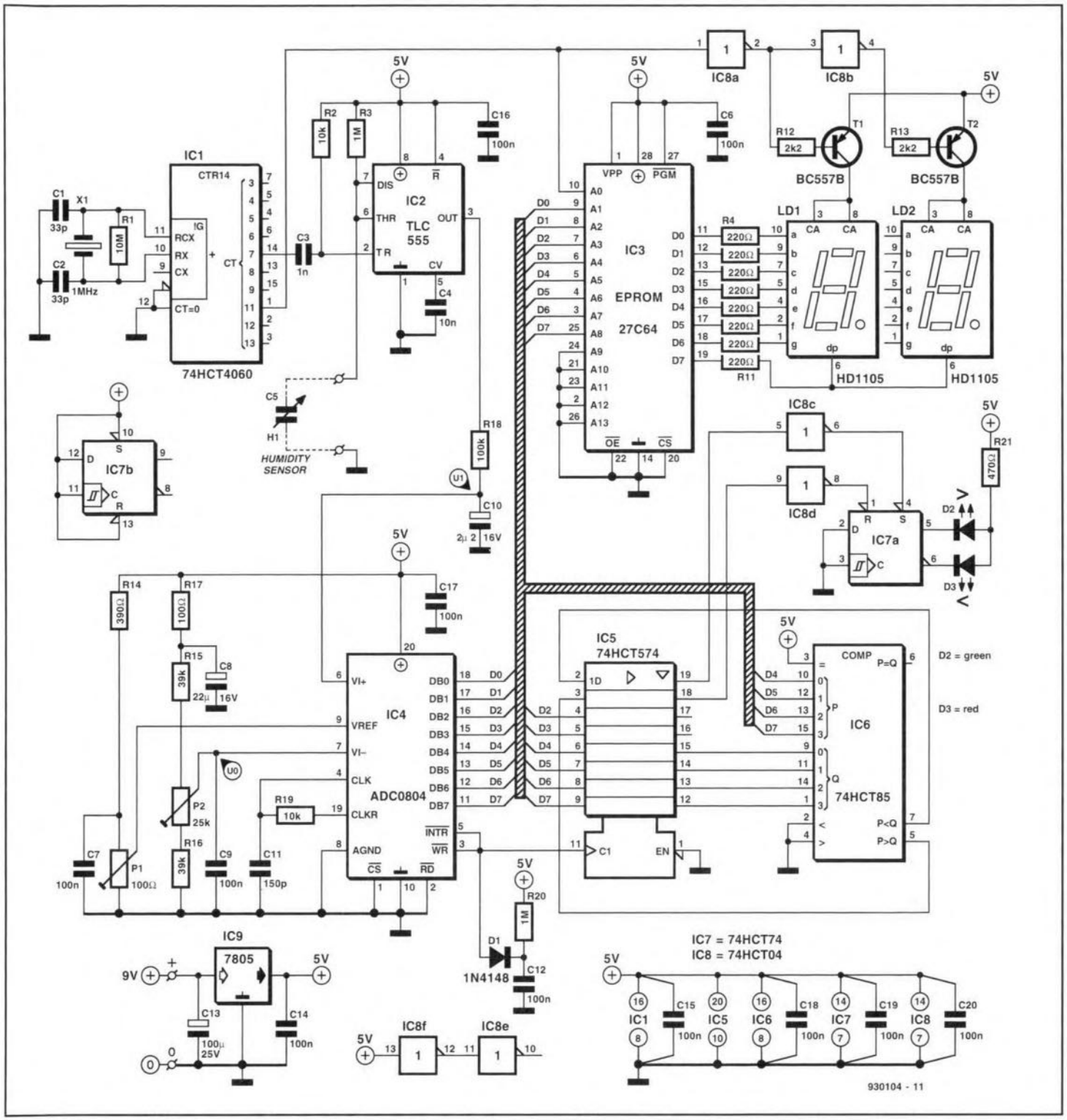



**Fig. 3. Circuit diagram of the digital hygrometer.**

## CALCULATION OF VARIOUS PARAMETERS

In these calculations:
ε is the dielectric constant of the sensor foil (F m$^{-1}$).
$A$ is the surface area of the electrodes (mm$^2$).
$C$ is the capacitance of the sensor (F).
$d$ is the thickness of the foil (mm).
$K$ is the capacitance factor (%).
$f$ is the oscillator frequency (Hz).
a, b are oscillator constants
r is relative humidity (%).
$U_{av(r)}$ is the average input voltage (offset deducted) into the A-D converter (V).

$C_r = \varepsilon_r A / d$ [Eq. 1]

$K_r = 100\,(C_r - C_0) / C_r$ [Eq. 2]

Substituting Eq. 1 into Eq. 2:

$K_r = 100\,(\varepsilon_r - \varepsilon_0) / \varepsilon_r$ [Eq. 3]

$f_r = a / bC_r$ [Eq. 4]

Substituting Eq. 1 into Eq. 4:

$\varepsilon_r = ad / Abf_r$ [Eq. 5]

Substituting Eq. 5 into Eq. 3:

$K_r = 100\,(1 - f_r / f_0)$ [Eq. 6]

from which:

$f_0 = f_r / (1 - K_r / 100)$ [Eq. 7]

$U_{av(r)} = [1 / (1 - K_r / 100)] - 1$ [Eq. 8]

midity, capacitance factor, and oscillator frequency are given on the preceding page.

## The design

The block schematic of the design is shown in **Fig. 1**. A crystal-controlled oscillator provides a stable frequency that is used to drive a monostable multivibrator (MMV). The length of the pulses produced by the multivibrator is determined by the capacitance of the r.h. sensor.

An integrator (a simple *RC* network) transforms these pulses into a direct voltage, the level of which is a measure of the humidity of the air. An offset is deducted to compensate for a relative humidity of 0%. The resulting direct voltage is thus an accurate measure of the relative humidity. This direct voltage is applied to an analogue-to-digital (A-D) converter.

The data produced by the converter are used to address an EPROM that contains a linearization table. The EPROM correlates the measured voltage with a particular relative humidity.

The EPROM drives two seven-segment displays, that is, the data stored in the memory determine which segments should light when a particular direct voltage is input.

The output of the A-D converter is also applied to a buffer and comparator which compare the previous data with the present ones to determine whether the relative humidity is rising or falling. This is

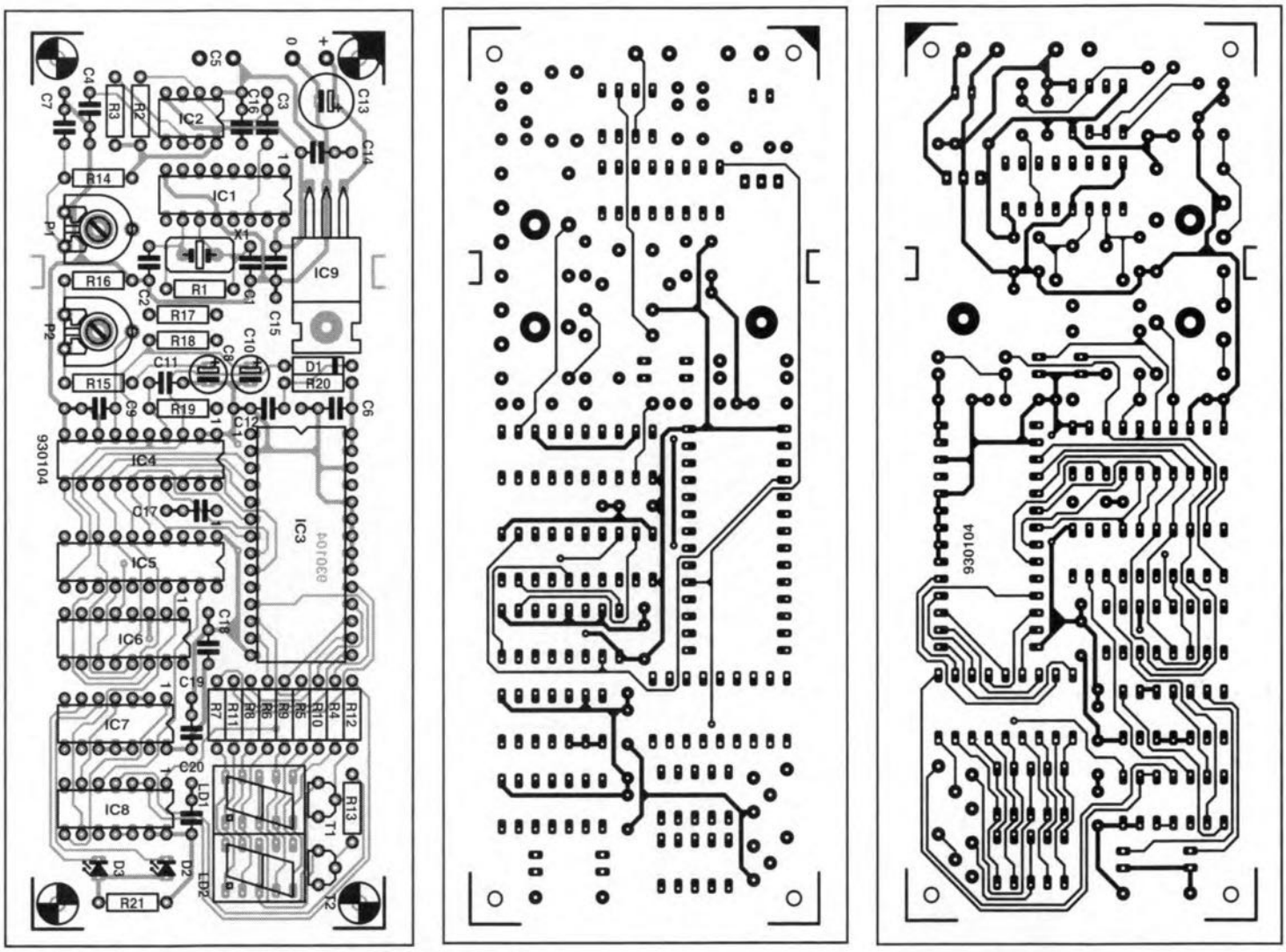



Fig. 4. Printed-circuit board for the digital hygrometer.

**PARTS LIST**

**Resistors:**
$R_1$ = 10 MΩ
$R_2$, $R_{19}$ = 10 kΩ
$R_3$, $R_{20}$ = 1 MΩ
$R_4$–$R_{11}$ = 220 Ω
$R_{12}$, $R_{13}$ = 2.2 kΩ
$R_{14}$ = 390 Ω
$R_{15}$, $R_{16}$ = 39 kΩ
$R_{17}$ = 100 Ω
$R_{18}$ = 100 kΩ
$R_{21}$ = 470 Ω
$P_1$ = 100 Ω preset
$P_2$ = 25 kΩ preset

**Capacitors:**
$C_1$, $C_2$ = 33 pF
$C_3$ = 1 nF
$C_4$ = 10 nF
$C_5$ = humidity sensor, Philips Type H1
$C_6$, $C_7$, $C_9$, $C_{12}$, $C_{14}$–$C_{20}$ = 100 nF
$C_8$ = 22 µF, 16 V, radial
$C_{10}$ = 2.2 µF, 16 V, radial
$C_{11}$ = 150 pF
$C_{13}$ = 100 µF, 25 V, radial

**Semiconductors:**
$D_1$ = 1N4148
$D_2$ = LED, green
$D_3$ = LED, red
$T_1$, $T_2$ = BC557B

**Integrated circuits:**
$IC_1$ = 74HCT4060
$IC_2$ = TLC555
$IC_3$ = programmed 27C64 (6301 – p. 70)
$IC_4$ = ADC0804
$IC_5$ = 74HCT574
$IC_6$ = 74HCT85
$IC_7$ = 74HCT74
$IC_8$ = 74HCT04
$IC_9$ = 7805

**Miscellaneous:**
$X_1$ = crystal, 1 MHz
$LD_1$, $LD_2$ = 7-segment LED display, common anode, Type HD1105 (0 = orange)
Enclosure
PCB with programmed EPROM, No. 930104

```
program test;

uses dos,crt;

var
 i:integer;
 j,l,k:integer;
 g: file of byte;
 result: real;

const
 display:array[0..9] of byte =($c0,$f9,$a4,$b0,$99,
                               $92,$82,$f8,$80,$90);
 vallist:array[0..16] of byte = (  0, 15, 31, 47, 63, 79, 95,111,127,
                                 143,159,175,191,207,223,239,255);
 humidity:array[0..16] of byte =(  0, 13, 23, 32, 40, 48, 55, 61, 67,
                                  73, 78, 82, 86, 90, 94, 97,100);

begin
  clrscr;
  assign (g,'humidity.dat');              (Open the desired filename)
  rewrite (g);
  for i:=0 to 15 do                                  (next curve part)
   begin
    for j:=0 to 15 do                              (linearise curve part)
     begin
      result:=j*(humidity[i+1]-humidity[i])/(vallist[i+1]-vallist[i]);
      result:=result+humidity[i];
      l:= (round (int (result/10)) ) mod 10;
      k:= round ((frac (result/10) *10) );
      if k=10 then
       begin
        k:=0;
        l:=l+1;
       end;
      if (l=10) and (k=0) then
       begin
        l:=9;
        k:=9;
       end;
      write (l);
      write (k,' ' );
      write (g,display[k]);
      write (g,display[l]);
     end;
    writeln;
   end;
  close(g);
end.                                                    930104-13
```

**Fig. 5. Pascal listing for computing the content of the EPROM.**

indicated by two LEDs.

## The circuit

The oscillator, $IC_1$, the HCT version of the 4060, generates a frequency of 1 MHz, which is divided by 256 and this signal, available at pin 14, is applied to the trigger input of monostable multivibrator $IC_2$, a CMOS version of the well-known 555. Differentiating network $R_2$-$C_3$ makes the trigger pulses short to ensure that the trigger level of a 555 is high again before the mono time has elapsed.

Humidity sensor $C_5$ determines the width of the output pulses from the MMV. The output of the MMV is integrated by $R_{18}$-$C_{10}$, whereupon the direct voltage across $C_{10}$ is converted into a digital value by eight-bit A-D converter $IC_4$. The reference voltage of the converter is set with $P_1$, while $P_2$ provides the offset voltage

Preset $P_2$ is part of potential divider $R_{15}$-$P_2$-$R_{16}$, which, via additional smoothing network $R_{17}$-$C_8$, is connected to the supply voltage.

Network $R_{19}$-$C_{11}$ is required by the internal clock used in the conversion.

Resistor $R_{20}$, capacitor $C_{12}$ and diode $D_1$ ensure that the converter starts promptly when the supply voltage is switched on.

When the supply is switched on, pin 3 is held low briefly to allow $C_{12}$ to be charged via $R_{20}$. Diode $D_1$ prevents $C_{12}$ short-circuiting the pulses at output pin 5, which are linked to pin 3, and which provide the clock for buffer $IC_5$. The link between pins 3 and 5 sets the converter in its free-running mode. As soon as a conversion has been completed, pin 5 signals to pin 3 that new data may be output.

The data provided by $IC_4$ are applied as addresses to EPROM $IC_3$ and to buffer $IC_5$. The data outputs of the EPROM drive LED displays $LD_1$ and $LD_2$.

The EPROM contains data that determine which segments must be powered to indicate the r.h. value associated with those data. The EPROM thus serves as a data-to-seven-segment converter and corrects the non-linearity of the sensor.

Since the content of the EPROM is only eight bits wide, which allows storage of the data for one display only, the displays are multiplexed by $IC_{8a}$, $IC_{8b}$, $T_1$ and $T_2$. The clock required for this is provided by $IC_1$ (pin 1). This clock is also applied to pin 10 of $IC_3$, so that when an interchange of displays takes place, there is also a change of address. Thus, for every number on the display, two addresses are required in $IC_3$. The EPROM is available ready programmed (see page 70), but may also be programmed with the aid of the Pascal program in **Fig. 4**.

Circuit $IC_5$ is supplied with a clock when new data appear at the output of the A-D converter. Immediately afterwards, these data are stored in $IC_5$. Comparator $IC_6$ checks whether the new data on the four highest lines are greater or smaller than the previous data. Its P inputs (pins 10 12, 13, and 15) are therefore linked to the four highest data lines of $IC_4$, while its Q outputs (pins 1, 9, 11 and 14) are coupled to latch $IC_5$. Pins 5 and 7 are connected to two inputs of $IC_5$, so that the status of these outputs is also stored in the latch.

At the instant new data appear at the outputs of the converter, they are applied immediately to the P inputs of $IC_6$. This circuit then compares the value with that of the previous data which at that moment are still stored in $IC_5$. Depending on the result, either pin 5 or pin 7 of $IC_6$ goes high and this level is applied to pin 2 or pin 3, as the case may be, of $IC_5$.

Pins 18 and 19 of $IC_5$ are linked to inverters $IC_{8d}$ and $IC_{8c}$ respectively. The inverters control the set and reset inputs of bistable $IC_{7a}$.

Since the signals from the comparator are applied via the buffer, they control the bistable synchronously with the new data. This ensures that the bistable does not give wrong readings owing to transit values on the D4–D7 lines.

The bistable controls a green and a red LED. These diodes indicate whether the relative humidity tends to rise (green) or to fall (red). It also ensures that when two successive data trains are identical, the LED that was lit at the previously detected change in r.h. remains on.

The power supply for the hygrometer is provided by a 9 V mains adaptor via a Type 7805 voltage regulator. The adaptor should be capable of providing a current of 300 mA.

## Construction

The hygrometer is most conveniently built on the printed-circuit board in **Fig. 4** (available ready made – see p. 70). Construction is straightforward by following the layout of the board. The ICs may be mounted in suitable sockets, as may the displays to elevate them slightly above the other components. The LEDs should be at the same height as the displays: this makes viewing them rather more convenient.

Regulator $IC_9$ does not need a heat sink and it may be screwed directly on to the board.

After everything has been soldered, the board can be mounted in a suitable enclosure. It is, of course, important to use

930127-II

**Solution to the Prize Electronic Crossword by Matrix (September 1993)**

**Across**
1 Bistables
6 Valve
9 Altitude
10 Elicit
12 Electromagnetic
14 Disarm
15 Deer
16 Pi
19 Ev
20 Isle
21 Allure
24 Radiotelescopes
25 Dreamy or dreams
26 Terrazzo
29 Satyr
30 Attenuate

**Down**
1 Biased
2 Sitter-in
3 Autotransformer
4 LED
5 SI
6 Valence-electron
7 Locate
8 Eutectic
11 NAND gate
13 Ohmmeter
17 Tetrodes
18 Trapezia
22 Advert
23 Ashore
27 ECT
28 mA

---

Winners of the construction kits, supplied by **Maplin Electronics** – see back cover – are:

1st prize: Stephen Lenham

2nd prize: Tony Pelham

3rd/4th/5th prizes:
Colin Izzard
John N. Taylor
Patrick Walker

Winners of the book prizes are
D.A. Ashton
Paul Barrett
M.J. Bastable
Gareth Blower
A. Burnley
M.I. Constantine
P. Cunane
L. Dyson
R.N. Golding
R. Hale
Christopher Hudson
Ken Jones
Tom Kelly
David Marston
K.C. Phillips
W.F. Ritchie
Stephen Scott
R.M. Smith
G.W. Spray
D. Westbury

All winners have been advised personally.


---

either a transparent case or one with an appropriate window through which the displays and LEDs can be viewed.

The sensor should be fitted on or near the enclosure and linked via two short lengths of flexible wire to the $C_5$ connections at the left-hand side of the PCB.

Finally, connect the output of the mains adaptor to the **+** and **0** terminals on the PCB, preferably via a plug and socket on the enclosure.

## Calibration

A calibrated hygrometer and multimeter are required for the calibration. Remove the lid of the enclosure and switch on the supply to the digital hygrometer. Wait a few minutes to give the unit time to adjust to the ambient humidity. Check the reading of the calibrated hygrometer. Find this value in Table 1 and note the associated rating of *K*. Enter this rating into the formula for calculating the offset voltage:

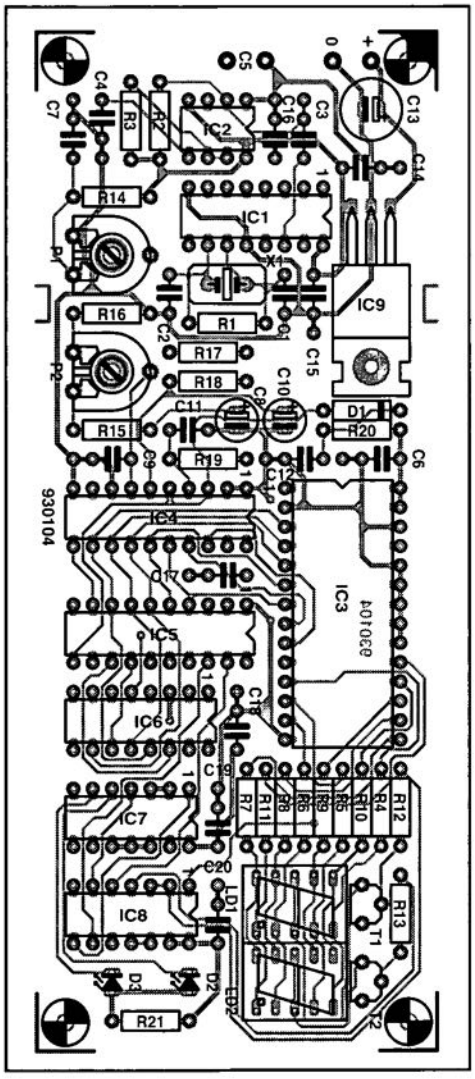
$$U_{offset} = (1 - K / 100)\, U_{rh},$$

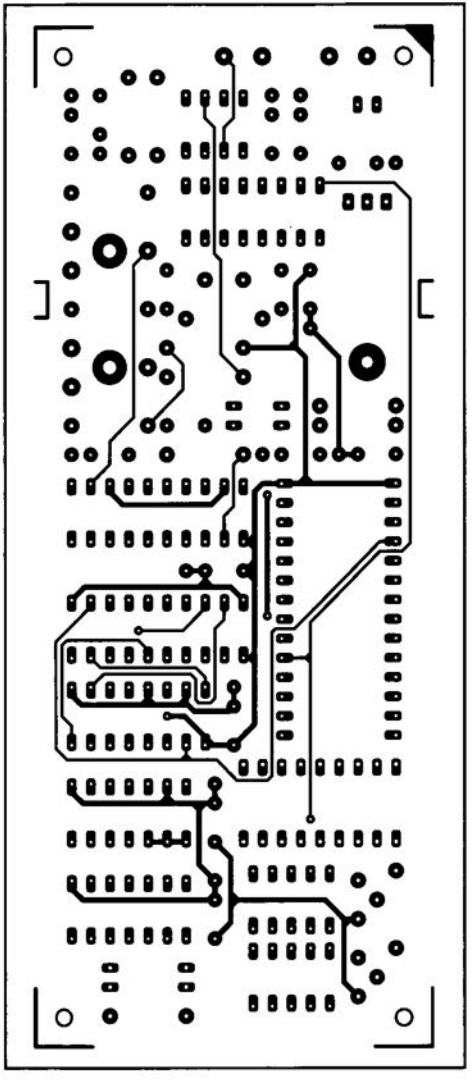
where $U_{rh}$ is the value of the direct voltage at pin 6 of $IC_4$. Connect the multimeter to pin 7 of $IC_4$ and adjust $P_2$ till the meter reads the calculated value of the offset voltage. Finally, adjust $P_1$ till the display reads the same value of relative humidity as the calibrated hygrometer.

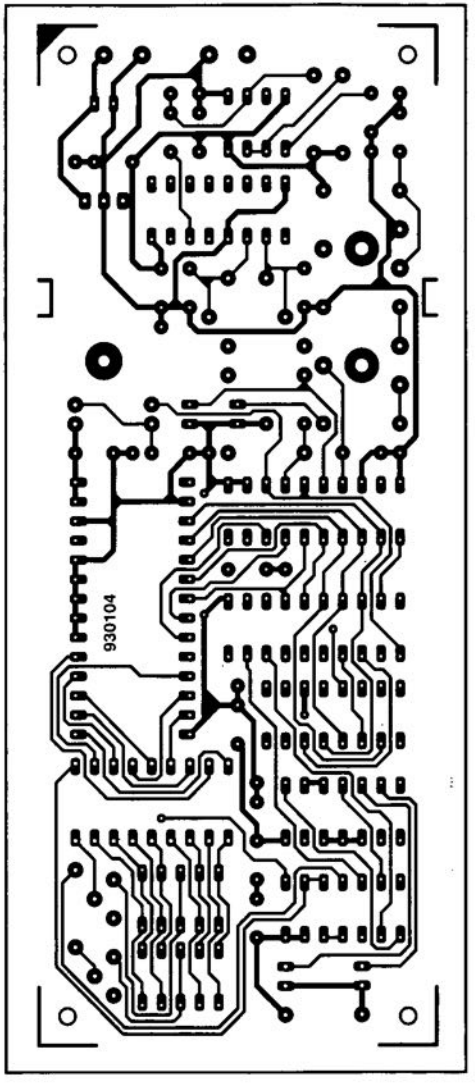
**END**

| R.H. (%) | *K* (%) | R.H. (%) | *K* (%) | R.H. (%) | *K* (%) | R.H. (%) | *K* (%) |
|---|---|---|---|---|---|---|---|
| 10 | 2.135 | 31 | 6.693 | 52 | 11.962 | 73 | 17.758 |
| 11 | 2.349 | 32 | 6.926 | 53 | 12.228 | 74 | 18.039 |
| 12 | 2.562 | 33 | 7.161 | 54 | 12.496 | 75 | 18.321 |
| 13 | 2.775 | 34 | 7.398 | 55 | 12.765 | 76 | 18.604 |
| 14 | 2.988 | 35 | 7.638 | 56 | 13.035 | 77 | 18.889 |
| 15 | 3.201 | 36 | 7.879 | 57 | 13.307 | 78 | 19.177 |
| 16 | 3.414 | 37 | 8.123 | 58 | 13.580 | 79 | 19.469 |
| 17 | 3.626 | 38 | 8.368 | 59 | 13.854 | 80 | 19.767 |
| 18 | 3.839 | 39 | 8.616 | 60 | 14.130 | 81 | 20.070 |
| 19 | 4.052 | 40 | 8.865 | 61 | 14.406 | 82 | 20.380 |
| 20 | 4.265 | 41 | 9.116 | 62 | 14.683 | 83 | 20.700 |
| 21 | 4.478 | 42 | 9.368 | 63 | 14.961 | 84 | 21.029 |
| 22 | 4.693 | 43 | 9.622 | 64 | 15.240 | 85 | 21.368 |
| 23 | 4.908 | 44 | 9.877 | 65 | 15.519 | 86 | 21.719 |
| 24 | 5.125 | 45 | 10.133 | 66 | 15.799 | 87 | 22.082 |
| 25 | 5.343 | 46 | 10.390 | 67 | 16.079 | 88 | 22.457 |
| 26 | 5.563 | 47 | 10.649 | 68 | 16.359 | 89 | 22.843 |
| 27 | 5.785 | 48 | 10.909 | 69 | 16.639 | 90 | 23.238 |
| 28 | 6.008 | 49 | 11.171 | 70 | 16.918 | 91 | 23.643 |
| 29 | 6.234 | 50 | 11.433 | 71 | 17.198 | 92 | 24.057 |
| 30 | 6.463 | 51 | 11.697 | 72 | 17.478 | 93 | 24.482 |

**Table 1. Correlation between relative humidity and capacitance factor *K*.**


930104
IC1
IC2
IC3
IC4
IC5
IC6
IC7
IC8
IC9
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18
R19
R20
R21
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13
C14
C15
C16
C17
C18
C19
C20
D1
D2
D3
LD1
LD2
T1
T2
X1
P1
P2
0
+

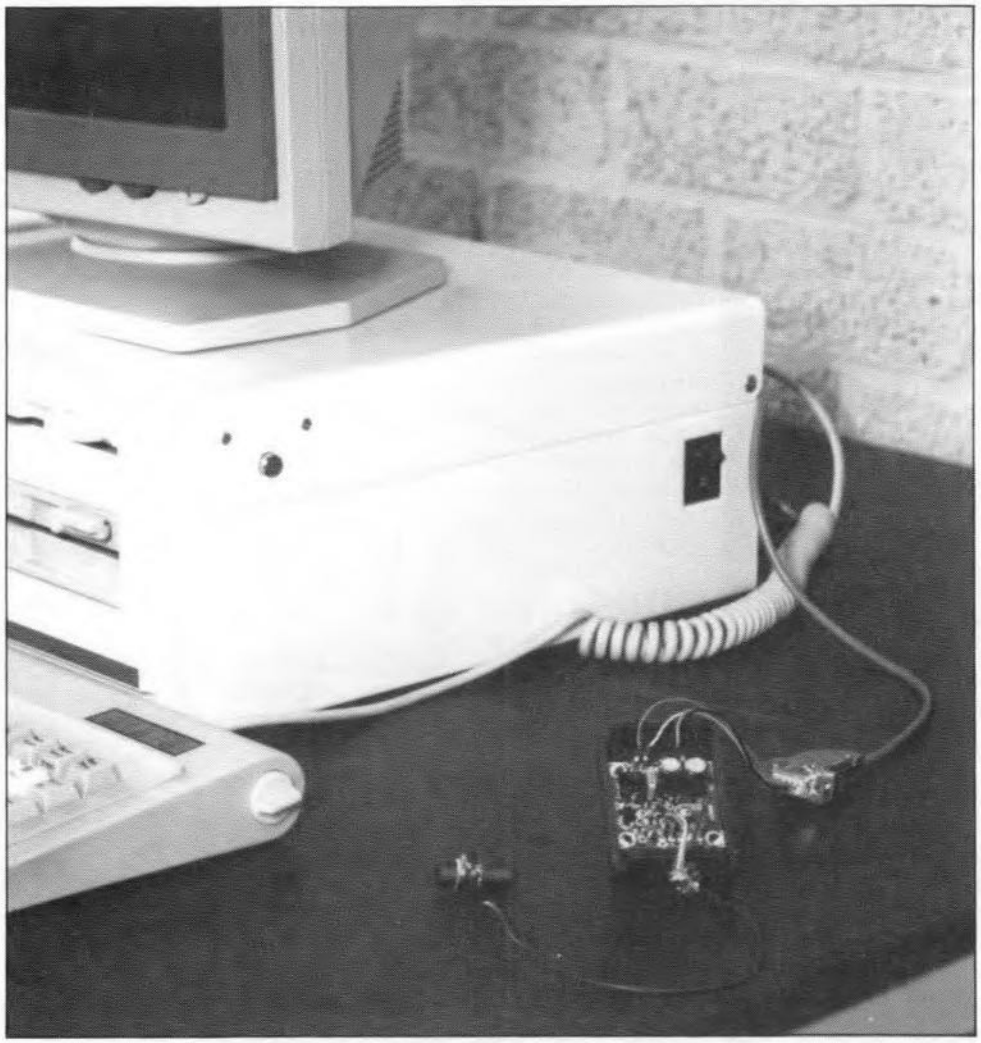



930104

93 0058

# PRECISION CLOCK FOR PCs

**Build this small add-on unit and put an end to the (often gross) inaccuracy of the real-time clock that ticks in your PC. Complete with a software driver, the precision clock synchronizes your PC to DCF77, a time standard transmitter operating in the long-wave band.**



**Design by B. Zschocke**

TO many PC owners, it is amazing and frustrating to note that even the cheapest quartz-controlled little alarm clock bought in a high-street shop has a far better accuracy than the real-time clock in, say, a state-of-the art 486-based PC. Although many PC users will notice the clock inaccuracy only twice a year (on changing from summer time to winter time and vice versa), there are also cases when large time errors on a PC have disastrous consequences. For instance, on a small network, where one program such as Turbo Pascal is shared, and the MAKE option is used from time to time to produce code (MAKE automatically compiles the latest version of the program). In this situation, it can happen that the latest version of the software is overwritten by an older version, because the associated time information is incorrect. It may also happen that a back-up program saves data which is outdated, while the latest version is 'forgotten' — all because of an inaccurate system clock.

The inaccuracy of a PC clock may have several causes: supply voltage dips and surges when the computer is switched on and off; large temperature variations in the case; or ageing effects of the quartz crystal. Furthermore, most PC clocks lack an adjustment point, so that one is totally dependent on the accuracy of a cheap crystal.

## Atoms for the right time

The radio-controlled clock described here enables a PC to always 'know' the right time. The time information received from the DCF77 transmitter in Mainflingen, Germany, is decoded and subsequently applied to the PC via the RS232 serial port. This is done to save space and energy required for an additional PC insertion card. Further, the current drain of the DCF77 receiver module and the associated interface is so small that an additional power supply is not needed. Before discussing the hardware, however, let us have a look at the source and structure of the time information picked up by the receiver.

DCF77 is a 50-kW transmitter operating at 77.5 kHz from Mainflingen, near Frankfurt in Germany. The station is operated by the Physikalisch-Technische Bundesanstalt, and has a range between 1,500 and 2,500 km. The time information transmitted by DCF77 is derived from a caesium atomic clock which is claimed to be among the most accurate in the world.

As with nearly every clock, an oscillatory movement is used as the reference. However, in contrast with, say, a pendulum clock where the length of the pendulum is a measure of 'time', or a quartz clock, in which the self-resonance of a crystal is used as the reference, an atomic clock is based on the fact that atomic energy levels are associated with certain frequencies. To understand this relation, a little knowledge of atomic physics is required.

Depending on their energy, atoms can take on different states. This phenomenon may be compared to a fuel gauge in a car: a high reading indicates a high energy, a low reading, a low energy. To change the meter reading from low to high, you have to fuel up, i.e., energy has to be added. Likewise, the state of atoms can be changed by adding energy. However, it is only possible to go from a low state to a high state by adding an exact amount of energy. Adding less or more energy than the critical amount will not change the atom's state from low to high. Because of this phenomenon, it is possible to generate an ultra-exact frequency by using radiation to add a defined amount of energy to the atom.

In the atomic clock, an amount of caesium is vaporized at a temperature of 100 °C. Caesium is a metal with a low melting temperature of 30 °C. In the first stage of the clock, atoms with

a 'low' and 'high' energy state are separated. The 'low' level atoms arrive in a resonator in which they are exposed to radiation from a signal source operating at a nominal frequency of 9.192631770 GHz. The radiation energy is transferred to the atoms, which change to the 'high' energy level. After being moved through the resonator, the atoms are collected and separated again.

The fewer 'low level' atoms remain in the resonator, the more accurate the resonator works. This enables a control system to adjust the resonator frequency for a minimum number of atoms that remain at the 'low' energy level. The resonator frequency so obtained forms the reference for the time information transmitted by DCF77. The estimated accuracy of the caesium reference is one second in 300,000 years.

## DCF77 time information

In order to transmit the complete time information, a protocol has been drawn up that enables the exact time and date to be contained in a periodic transmission which lasts 59 seconds. A complete time code is transmitted every minute, as illustrated in **Fig. 1**. The transmitter frequency is 77.5 kHz, which is derived from the caesium resonator. This has the advantage of allowing the transmitter frequency to be used as a reference, since its accuracy equals that of the timebase of the clock (phase errors may, of course, still occur in the path from the transmitter to the receiver). The transmit frequency used lies in the long-wave band, which means that only the ground wave is usable for transmission. Reflections of radio signals at this wavelength are insignificant, so propagation is by one 'path' only, the ground wave. Consequently, reception of long-wave signals is virtually constant around the clock. In practice, DCF77 reliably covers most of Continental Europe, the South of Scandinavia, and the larger part of the UK and Ireland.

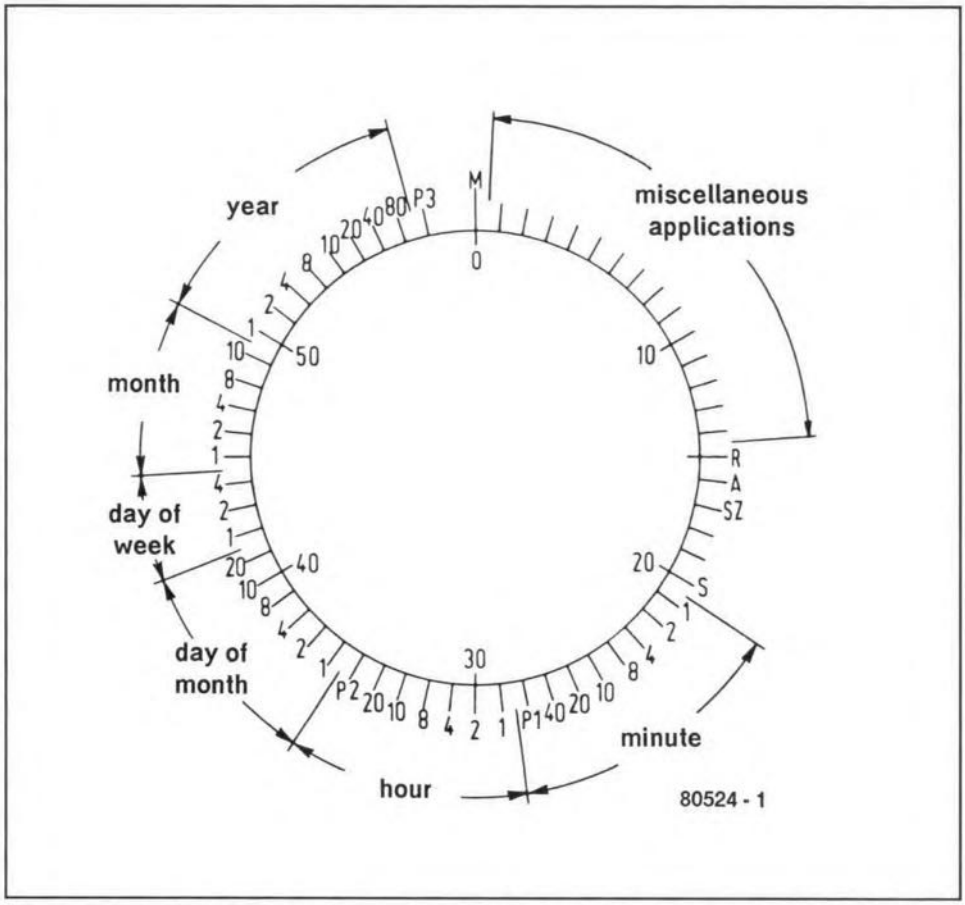



**Fig. 1. Schematic organization of the time/date information transmitted by the DCF77 time standard transmitter.**

## The coding system

The coding system used on DCF77 was developed at a time when microprocessors were virtually unknown. Hence, a simple coding system with BCD (binary coded decimal) was chosen, allowing 'ordinary' TTL components to be used for decoding the time information. Each code word consists of 59 bits (bit 0 through 58). One bit is transmitted every second. A logic one is transmitted as a pulse with a length of 200 ms, and a logic zero, as a pulse of 100 ms. During the pulse time, the transmitter carrier is reduced to 25% (amplitude modulation). The amplitude reduction takes place at the start of a second. Since there are 60 seconds to the minute, and only 59 bits are transmitted, the missing 60th bit is used to mark the start of the time code. The function of each of the 59 bits contained in the time code is given in **Table 1**.

Three times an hour, during the 19th, 39th and 59th minute, the station ident, DCF77, is transmitted in morse. Each letter or number is transmitted between two second signs by switching the transmitter modulation depth between 100% and 85% at a rate of 250 Hz. This identification is automatically transmitted without interrupting the time code.

## The idea

Today, a wide range of ready-made DCF77 receivers/clocks is available at reasonable prices. In most cases, such units are identified as 'radio-controlled' clocks. The receiver section in such a clock usually supplies the digital time code as 100-ms and 200-ms pulses. The best known receiver IC is the U2775B, developed by Telefunken AG for use in Junghans clocks. Apart from a ferrite rod antenna, this IC requires only a couple of external parts to make a sensitive and reliable DCF77 receiver. The U2775B is capable of operating at a low supply voltage of between 1.2 V and 3.4 V, and has a current drain of only 0.5 mA.

There are also ready-made receiver modules based on the U2775B. Unfortunately, these usually supply output pulses with a length of 160 ms and 60 ms because about 40 ms is required for reliable decoding of the time information.

The designer's aim was to find a simple way of using a DCF77 receiver module with 'shortened' output pulses to decode the time information with the aid of a PC. This has been achieved by turning the pulses into characters conveyed to the PC via a serial link operating at a low bit rate. In this system, the binary code 000011111 ($0F_H$) represents a 60-ms pulse, and 0000000001 ($00_H$), a 160-ms pulse. The leading 0 in the code is the start bit, and the trailing 1 is the stop bit. The advantage of this approach is that the software is relieved from pulse decoding, which is taken over by the serial interface. Furthermore, the interface ensures that an interrupt is generated only once a second. At such a slow interrupt rate, the PC is hardly slowed down. The functions that remain for the software are limited to finding the start of the time code, decoding the actual information, and conveying the decoded time to the op-

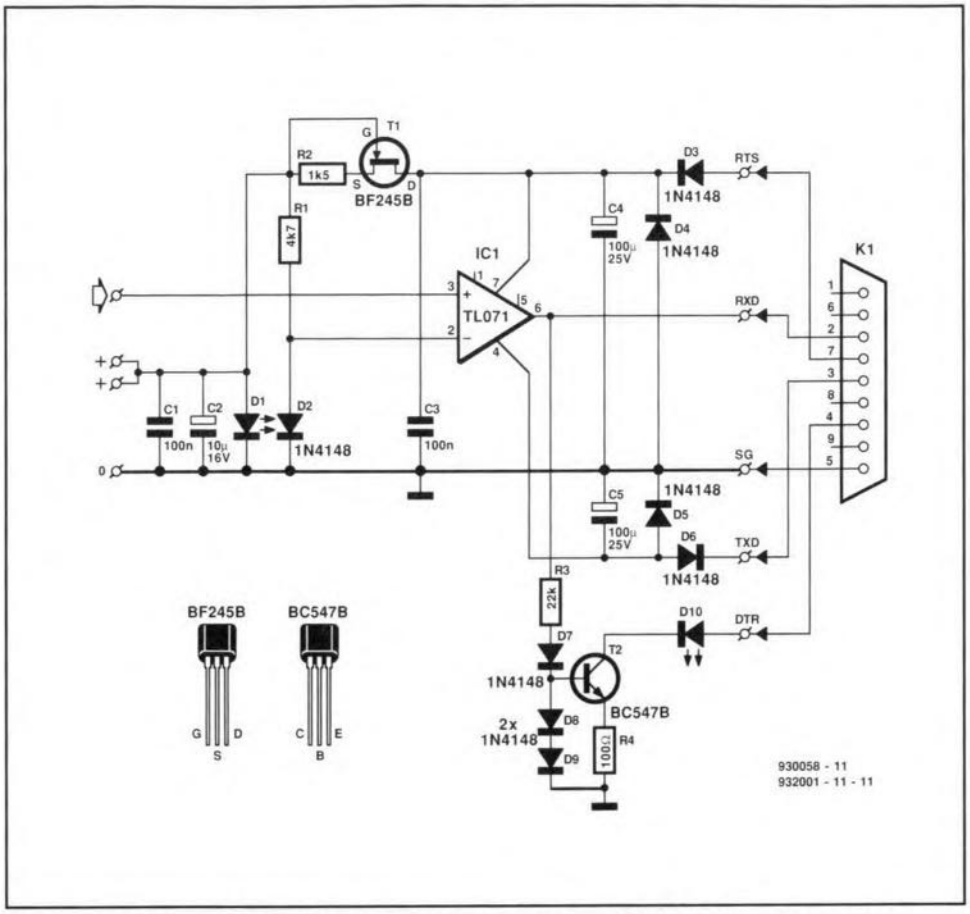



**Fig. 2. Circuit diagram of the interface between the PC and the DCF77 receiver module.**

erating system installed on the PC.

## The serial interface

The circuit diagram of the serial interface between the DCF77 receiver module and the PC's RS232 port is given in **Fig. 2**. The interface is powered via the RTS and TxD lines. Capacitor C4 is charged via diode D3 to the level of the RTS line, which is between +7 V and +12 V. At the same time, capacitor C5 is charged to the TxD line level, which is between –7 V and –12 V. Diodes D4 and D5 protect the circuit against damage caused by an incorrectly initialized RS232 port. The voltages built up across the capacitors form the symmetrical supply voltages for opamp IC1. The opamp gives the digital time code applied to its +input a level that enables it to be recognized as a serial signal by the PC's RS232 port.

Generating a suitable supply voltage for the DCF77 receiver module is a little more complex. Here, a **green** LED, D1, is used to stabilize the module's supply voltage. A stable voltage of about 1.8 V is obtained at a small current already.

Extensive decoupling is necessary in the interface, because cross-interference occurs easily between analogue and digital sub-circuits. In particular, every care has been taken to prevent the digital sections upsetting the operation of the sensitive analogue receiver. A very effective decoupling device is the high internal resistance formed by T1-R2, a current source inserted in the positive supply to the receiver module. Together with capacitors C1 and C2, this current source forms a filter that affords a very high degree of decoupling of the receiver's power supply lines. The combination D2-R1 is also connected to the module power supply, and provides a reference voltage of 0.6 V at the –input of the opamp. This is necessary to enable the opamp to recognize the high and low levels supplied by the receiver module.

The last part of the interface is the

## COMPONENTS LIST

**Resistors:**

| | | |
|---|---|---|
| 1 | 4kΩ7 | R1 |
| 1 | 1kΩ5 | R2 |
| 1 | 22kΩ | R3 |
| 1 | 100Ω | R4 |

**Capacitors:**

| | | |
|---|---|---|
| 2 | 100nF | C1,C3 |
| 1 | 10µF/16V radial | C2 |
| 2 | 100µF/25V radial | C4;C5 |

**Semiconductors:**

| | | |
|---|---|---|
| 1 | LED 3mm green | D1 |
| 8 | 1N4148 | D2-D9 |
| 1 | LED 3mm red | D10 |
| 1 | BF245B | T1 |
| 1 | BC547B | T2 |
| 1 | TL071 | IC1 |

**Miscellaneous:**

| | | |
|---|---|---|
| 1 | 9-way sub-D socket | K1 |
| 1 | DCF77 receiver module: Conrad[1,2] order code 190969-66. | |
| 1 | DCF77 ferrite antenna: Conrad[1,2] order code 535630-66. | |
| 1 | Plastic enclosure 60×50×30 mm; e.g., type E406 (Bopla)[2] | |
| 1 | Printed circuit board 930058 plus software 1871 (see page 70) | |

The control software for this project is also available separately: order code 1871 (see page 70).

[1] Conrad Electronic Nederland BV, P.O. Box 12, 7500 AA Enschede, Holland. Tel (+31) 53 282000. Fax: (+31) 53 283075.

[2] C-I Electronics, P.O. Box 22089, 6360 AB Nuth, Holland. Fax: (+31) 45 241877.

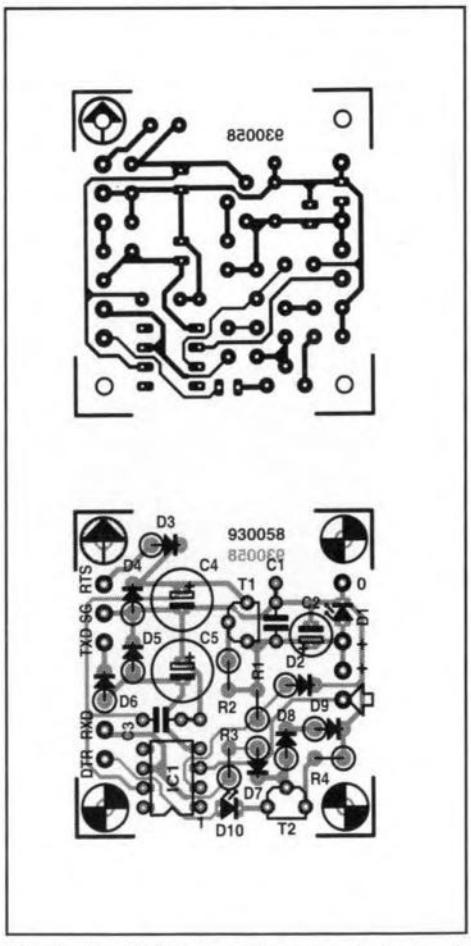



**Fig. 3. Track layout and component mounting plan of the printed circuit board designed for the receiver-to-PC interface.**

| Bit | Meaning | Function |
|---|---|---|
| 0-14 | | Miscellaneous applications / as required. |
| 15 | R | Antenna bit. 0 = normal antenna; 1 = spare antenna. |
| 16 | A1 | 1: change to summer or winter time in next hour. |
| 17 | Z1 | Time zone 1: 1 = summer time; 0 = winter time. |
| 18 | Z2 | Time zone 2. |
| 19 | A2 | 1: switching second follows. |
| 20 | S | Always 1; start marker for time/date transmission. |
| 21 | 1 | Minutes bit; value 1. |
| 22 | 2 | Minutes bit; value 2. |
| 23 | 4 | Minutes bit; value 4. |
| 24 | 8 | Minutes bit; value 8. |
| 25 | 10 | Minutes bit; value 10. |
| 26 | 20 | Minutes bit; value 20. |
| 27 | 40 | Minutes bit; value 40. |
| 28 | P1 | Parity bit for all bits transmitted so far (complement to give an even number). |
| 29 | 1 | Hours bit; value 1. |
| 30 | 2 | Hours bit; value 2. |
| 31 | 4 | Hours bit; value 4. |
| 32 | 8 | Hours bit; value 8. |
| 33 | 10 | Hours bit; value 10. |
| 34 | 20 | Hours bit; value 20. |
| 35 | P2 | Parity bit for all bits transmitted so far. |
| 36 | 1 | Day of month bit, value 1. |
| 37 | 2 | Day of month bit, value 2. |
| 38 | 4 | Day of month bit, value 4. |
| 39 | 8 | Day of month bit, value 8. |
| 40 | 10 | Day of month bit, value 10. |
| 41 | 20 | Day of month bit, value 20. |
| 42 | 1 | Day of week bit; value 1. |
| 43 | 2 | Day of week bit; value 2. |
| 44 | 4 | Day of week bit; value 4. |
| 45 | 1 | Month of year bit; value 1. |
| 46 | 2 | Month of year bit; value 2. |
| 47 | 4 | Month of year bit; value 4. |
| 48 | 8 | Month of year bit; value 8. |
| 49 | 10 | Month of year bit; value 10. |
| 50 | 1 | Year bit; value 1. |
| 51 | 2 | Year bit; value 2. |
| 52 | 4 | Year bit; value 4. |
| 53 | 8 | Year bit; value 8. |
| 54 | 10 | Year bit; value 10. |
| 55 | 20 | Year bit; value 20. |
| 56 | 40 | Year bit; value 40. |
| 57 | 80 | Year bit; value 80. |
| 58 | P3 | Parity bit for all bits transmitted so far. |

**Table 1. Meaning of all bits contained in the time information signal.**

circuit around transistor T2, which drives an LED, D10, to signal reception of time pulses received from DCF77. A 6-mA current source, T2-R4-D8-D9, is used to cope with the wide range of voltages that can occur on an RS-232 interface. In this way, the LED always lights at a constant intensity, while being supplied via the DTR line. Consequently, the opamp and receiver supplies are not loaded by the LED.

## Construction

The compact printed circuit board designed for the interface is shown in **Fig. 3**. Construction is simple. First fit the passive components, then the active components. You may want to fit capacitors C4 and C5 last because they are fairly tall, and complicate the fitting of the parts around them.

The DCF77 receiver module mentioned in the parts list is connected to the interface via four wires, for which solder pins are provided. The positive supply voltage is connected to the solder point marked '+' on the receiver module, while the ground wire goes to the point marked '–'. The module has two further connections. The point marked with an outgoing arrow is the signal output, which is connected to the signal input on the interface board. The last connection is marked with an 'input' arrow. This input is used to actuate the module, and must be connected to its positive supply. At the input side of the receiver module, connect the ready-made ferrite rod antenna to the indicated points on the printed circuit board. If the receiver module is fitted into an enclosure, two points should be observed. First, the enclosure may not be a metal type since that would make reception of the DCF77 signals on the ferrite rod antenna impossible. Second, to reduce interference to an absolute minimum, the receiver module must be fitted at a reasonable distance from the interface.

An alternative to the receiver module mentioned in the parts list is a ready-made DCF77 clock which contains an U2775B. If you happen to have such a clock, open it to see if it contains this IC. If so, proceed as follows: IC pin 14 is the signal output, pin 1 is ground. A power supply connection is not required, since the clock is usually battery-operated. Pin 13 must be connected permanently to the clock's supply voltage, and any other connection to it must be broken. Usually, the processor in the clock switches the receiver IC off after a certain period. This is done to save power. However, even if the U2775B is permanently on, the clock will run for more than a year on a fresh penlight battery. A suitable clock is, for instance, ELV's kit number 4434 (also available ready-made; order code 4435). For more information, contact ELV, Postfach 1000, D-2950 Leer, Germany. Telephone: (+49) 491 600888, Fax: (+49) 491 7016.

The connection between the interface board and the RS232 port on the PC is best made in 4-core screened cable. The screening of the cable is

used for the ground (SG) connection.

For best results it is recommended to install the receiver module or the clock at a distance of at least 4 m from the PC or the monitor. This helps to keep interference caused by stray radiation to a minimum. LED D10 is conveniently used to find a suitable location for the receiver module. Reception is all right when the LED flashes at a regular rate.

## Software

The control software for the precision clock is a so-called device driver, called DCFCLOCK.SYS, which is supplied on disk through our Readers Services (order code 1871). It must be installed **after** the mouse driver in the CONFIG.SYS file. Consequently, it is not allowed to call the mouse driver in the AUTOEXEC.BAT file. Any other order of initialization is only allowed if it is certain that the mouse driver, while looking for the mouse, does not affect the port to which the clock interface is connected. It should be noted that the software does **not** run on PC-XT computers.

The driver initialization command has the following options:

**P = n**
This sets the RS232 port the receiver is connected to. Valid numbers for n are 1 to 4; the default is 2. By default, the driver assumes the following interrupt lines for the ports:

COM1: IRQ4
COM2: IRQ3
COM3: IRQ5
COM4: IRQ7

**I = n**
This is used to change the interrupt line assignment from the default value. Valid numbers for n are 0 to 15. If you want to set the port **and** interrupt line, this parameter must be given **after P = n**. Owing to missing hardware, IRQ 8-15 could not be tested.

**S = n**
If n = 1, the driver will adjust the real-time clock in your PC-AT after every correctly received time information packet. Setting n to 0 will disable this function. The default is n = 1.

**B = n**
This sets the SIO's divisor rate and thus the baudrate. You only need this option if the pulse widths supplied by your receiver deviate considerably from the standard (60/160ms). The default is 2500, which equals 46 baud.

**D = n**
Generally, the driver checks whether another program or driver already uses the COM port in interrupt-driven mode. If so, an error report is produced. This test may be disabled by setting n to 1. The default is 0, i.e., run the test.

**W = n**
If n = 1, the driver will erase the COM port's I/O-address from the BIOS data segment. This is necessary if you are running MS-Windows, which resets all ports at startup and would otherwise turn the receiver's power off. Clearing the address makes the port invisible for Windows, and the clock continues to work. The default is n = 0.

**T = n**
This allows the driver to be used in a time zone different from that of the DCF77 transmitter, for instance, in the UK, where GMT = CET minus one hour during most of the year. Whenever a correct packet is received, this value will be added to, or subtracted from, the 'hours' information. Parameter n may be negative or positive.

## Practical use

Start your PC without the precision clock connected. Call up the time and date. If the clock is fast, you may have a small problem to fix — see below. Next, with the driver included in the CONFIG.SYS file, and the receiver module fitted in a suitable position, the PC may be started again. From then on, the clock in the PC ticks at atomic precision. Do take care, however, if the original PC clock used to be 'fast', i.e., running well ahead of the correct time. Once the precision clock has taken over from a 'fast' clock, new files suddenly have older date/time information than the original ones. It is, therefore, better to wait with saving new files until the precision clock has gained on the 'old' time. From then on, old and new files can not be swapped any more by accident. ■

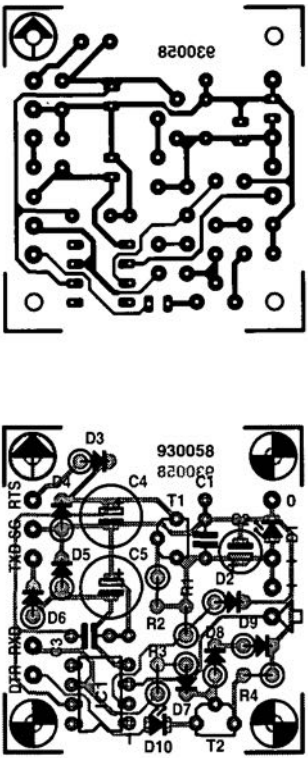



**Fig. 3. Track layout and component mounting plan of the printed circuit board designed for the receiver-to-PC interface.**

amplifier?). The output pulse is picked up by a microphone and fed back into the IMP where it is digitized and then fed into an IBM (compatible) computer via the printer port. The IMP software then analyses the input via Fourier transforms and outputs the results on to the computer screen in graphical form in the shape of amplitude and phase response curves. Full control is via the PC. The amplifier output can be sampled via a probe to correct for errors in the pulse spectrum and amplifier response.

IM P allows the collection and analysis of 12-bit analogue data up to 4,095 samples in length and sample rates are selectable at either 61.441 kHz or 1.92 kHz which, along with the internal filtering, allows measurements from several hertz to 20 kHz.

Further information from Falcon Acoustics Ltd, Tabor House, Norwich Road, Mulbarton, Norfolk NR14 8JT, England. Telephone +44 (0)508 78272; fax +44 (0)508 70986.

# CORRECTIONS

**DIGITAL DIAL** (January 1994)

An attentive reader has drawn our attention to the fact that the digital dial can not be used in conjunction with the receiver illustrated (a Yaesu Type FRG-7) since the IF of that receiver is much too high for the dial. Sorry for that oversight! [Editor]

**VHF/UHF TUNER** (Oct/Nov 1993)

The tuner module used in this design is no longer in production with Philips and its availability will thus become a problem. Fortunately, the Type UV916H is an excellent alternative. The snag is, however, that this unit is slightly smaller than the UV816, so that the antenna connector no longer protrudes from the enclosure. This can be overcome by terminating the antenna cable into a coaxial plug and making the entrance hole slightly larger. Moreover, one of the two earth tags of the UV916H must be connected at a different position.

# LETTERS

**SCART SWITCHING BOX**
(December 1993)

I have a few problems with this project, which I believe have to do with the connections. Pin 1 of one connector is linked to pin 2 of the other. The same is true of pins 3 and 19, which are linked to pins 6 and 20 respectively. All other pins are interlinked as one would expect, i.e., pin 5 to pin 5, pin 10 to pin 10, and so on.
L. Bastiaenssen

*In a SCART cable, the wires for the video and audio connections are always crossed. That is why the video output (pin 19) at one end of the cable is linked to the video input (pin 20) at the other end. This arrangement ensures that the input of one piece of equipment is always connected properly to the output of another. There is, therefore, nothing wrong with your cable.*

*Note that two pieces of equipment must never be connected simultaneously to $K_3$ and $K_5/K_6$. Use SCART connector $K_3$ **or** the phono plugs $K_5/K_6$, but not both at the same time!* [Editor]

**PRECISION CLOCK FOR PCs**
(November 1993)

I have encountered a problem with the Precision clock for PCs. I have an IBM (compatible) PC486 and have, as stated in the article, complemented the CONFIG.SYS file with the following (last) line:
DEVICE C:\MSDOS\DCFCLOCK.SYS.

I should be pleased if you would tell me:
1. Whereto should the files of the software provided (DCFCLOCK.ASM, DCFCLOCK.DOC and DCFCLOCK.SYS be copied? To the root, the MSDOS or a separate directory?
2. Once the files have been loaded, how is the program called up to initialize the driver and to fill the options P, I, S, B and D?
(M. Meersschaut)

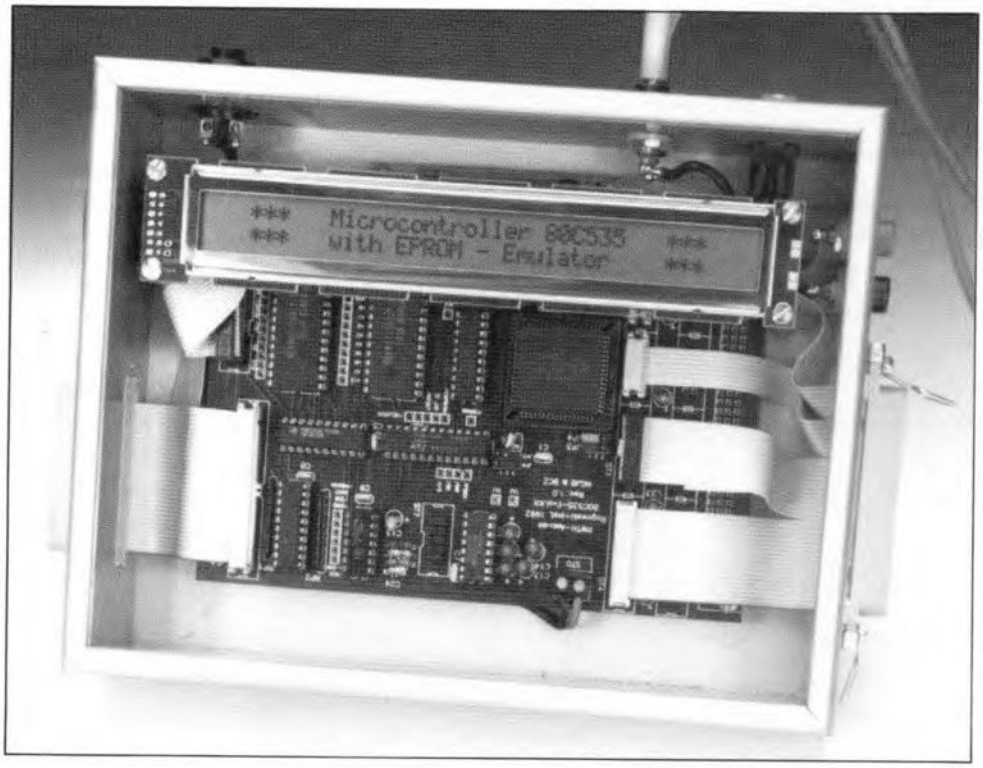
*The file DCFCLOC.ASM is the assembler listing of the program, which you no longer need (it is of interest only to dyed-in-the-wool programmers). The file DCFCLOCK.DOC contains the instructions for the program, which you can read with a word processing program. It is not necessary to store this file on a hard diksk.*

*The only program that you need to copy to the hard disk is DCFCLOCK.SYS. Place this file in the directory containing the DOS commands (e.g., C:\DOS). Add a line that indicates where the computer can find that program to CONFIG.SYS (in C:\), e.g. DEVICE = C:\DOS\DCFCLOCK.SYS. Other suffixes may be added for changing certain settings (see DOC file), but even without these the system should work correctly.*

*Note, however, that the receiver circuit must be connected to the COM port 2 and that the computer must be restarted after the software has been installed. The program will then automatically set the correct time in the internal clock of the PC every minute.*

[Editor]

# 535 CARD WITH EPROM EMULATOR (PART 1)




**Integrating an EPROM emulator into a microcontroller system gives flexibility while reducing cost. It also makes the 80C535 based processor board described here a splendid tool for application software developers.**

**Design by B. C. Zschocke**

ALTHOUGH microcontroller boards are generally inexpensive and easy to build, the cost of ancillary equipment to get a microcontroller to actually do something useful may well be on the high side for many enthusiasts. Assuming that you wish to develop your target program in a time-efficient way, i.e., forget about programming EPROMs bit-by-bit and byte-by-byte (which was nothing unusual about ten years ago), a minimal configuration consists of the following 'tools':

- a PC running an assembler capable of producing machine code for the relevant microcontroller;
- an emulator to enable target code to be tested in the controller system;
- an EPROM programmer to burn the final version of the program into EPROM.

The above equipment represents a considerable investment. Fortunately, it is possible to cut down on the bill. An EPROM programmer is not required if your activities are restricted to experiments only. Similarly, the emulator may be struck off the list if you have the time to burn a new EPROM after every modification made to the target program. However, developing software without these two tools is time consuming. After all, we do not tap our writings into clay tablets any more!

Considering that most computer hobbyists will have a PC, and that the main interest will be experimenting with a microcontroller, it is fair to say that the emulator is the most important tool. Ideally, an EPROM programmer is not called for until the code is debugged and ready to be installed permanently on a controller system (for example, a so-called turnkey system). The good news for all of you with tight budgets is that (1) the present 80C535 controller system has an on-board EPROM emulator, and (2) the system can be built without the EPROM emulator if you do not require this function.

## One controller, two functions

**Figure 1** shows a detailed block diagram of the system. In fact, the drawing is so detailed that it enables the operation of the entire system to be described in great detail. The block marked 'GAL' (generic array logic) has a crucial function because it contains the entire address decoding for the memory ICs, as well as the control logic that allows the system function to be switched from controller to emulator and vice versa. This means that the controller can execute instructions contained in the program memory or in the emulator memory. Actually, instructions in the emulator memory serve to copy a program downloaded from the PC into the program memory.

On close examination, the system drawn in **Fig. 1** looks very much like a standard configuration for controllers in the MCS51 family (of which the SAB80C535 is a member, although it is not manufactured by Intel). Such a standard configuration consists of the controller itself, an address latch, a data memory and a program memory. The program memory contains the code which is executed by the controller. The GAL allows a number of components to be 'moved around' in the system. If the GAL switches the controller to 'run' mode, the circuit works as a standard configuration described above, with the emulator memory and Centronics interface switched off. If the 'emulator' function is selected (again, via the GAL), the data memory is 'made invisible', and its function is assumed by the program memory, while the program memory is then formed by the emulator memory. This causes the microcontroller to run the program contained in the emulator memory. This program ensures that data (i.e., a target program) received via the Centronics interface is copied into the data memory (which is formed by the program memory).

It will be clear that the GAL has a key function in the circuit. Actually, the control of the GAL is based on a single signal: the strobe signal received via the Centronics interface. Before it arrives at the GAL, the strobe pulse is

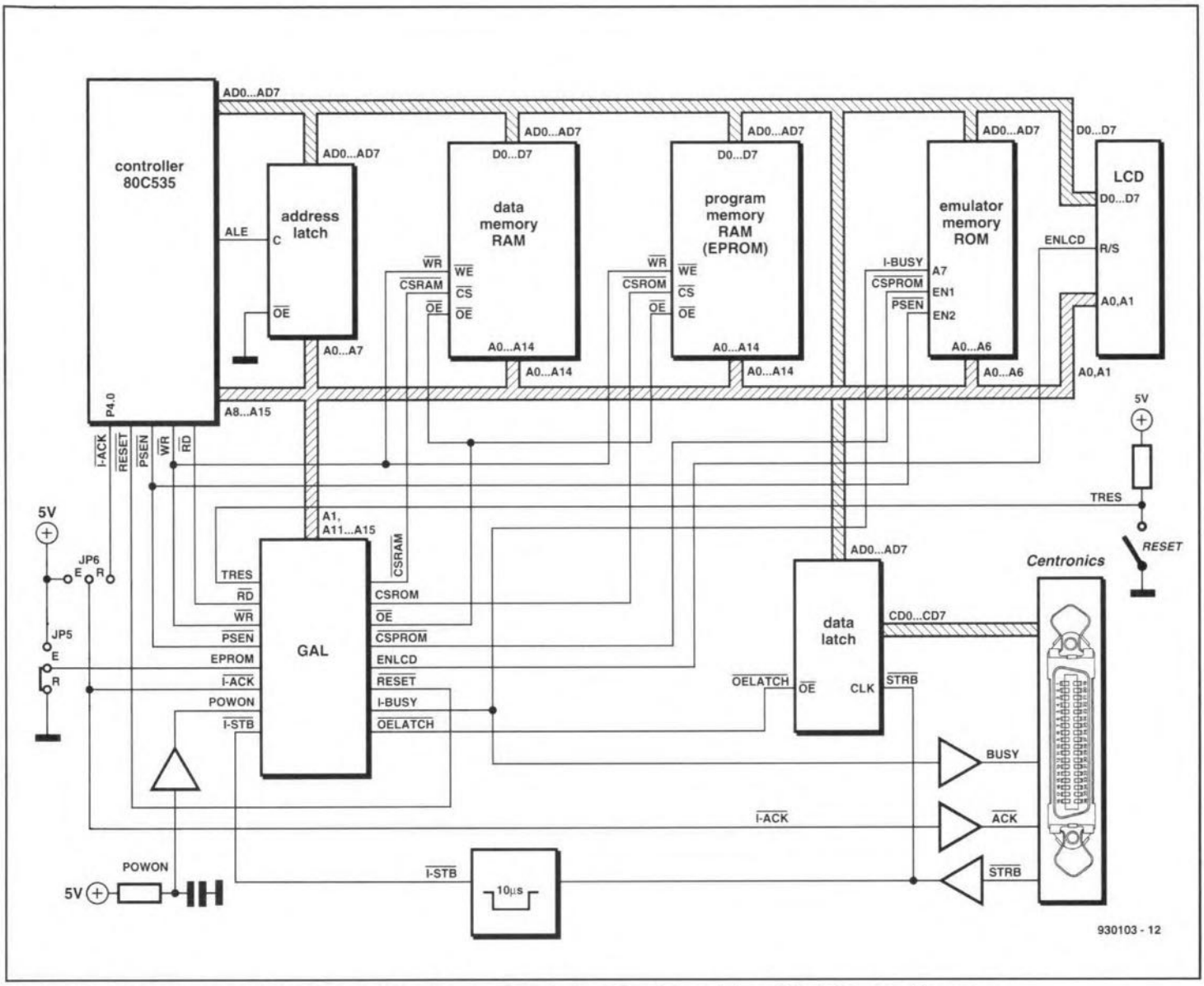



**Fig. 1. This block diagram is detailed enough for a comprehensive functional description of the 535 controller system.**

stretched to about 10 µs. This is done to make sure that it can be used also as a reset pulse for the GAL. Incidentally, the reset pulse is only supplied when the system is still in 'run' mode, and the strobe pulse indicates that the first byte of a new program has been sent. Next, the processor is supplied with a reset pulse, and the BUSY line is taken high. From then on, the GAL ensures that the controller uses the program memory as data memory, while allowing the controller to address the emulator program contained in the emulator memory. The reset causes the program to be run from address $0000_H$. The emulator program ensures that the received data is stored in the program memory. To enable the software to detect that data is held ready, the BUSY signal is tied to the most significant address bit of the emulator memory. In this way, the system is capable of switching between two program halves which are identical with the exception of one byte. Also, the

| address | data memory | program memory | address |
|---|---|---|---|
| 0000<br>7FFF | data memory (U3) address 0000 to 7FFF | program memory (U4) address 0000 to 7FFF | 0000<br>7FFF |
| 8000 | data latch (U8) read-only | program memory (U4) address 0000 to 7FFF | FFFF |
| 8001<br>87FF | data latch mirrors | | |
| 8800<br>8801<br>8802<br>8803 | LCD module instruction write<br>data write<br>instruction read<br>data read | | |
| 8804<br>8FFF | LCD module mirrors | | |
| 9000<br>BFFF | free for memory-mapped I/O | | |
| C000<br>FFFF | program memory (U4) address 4000 to 7FFF | | |

**Table 1. Memory map of the 535 board (all addresses in hexadecimal).**

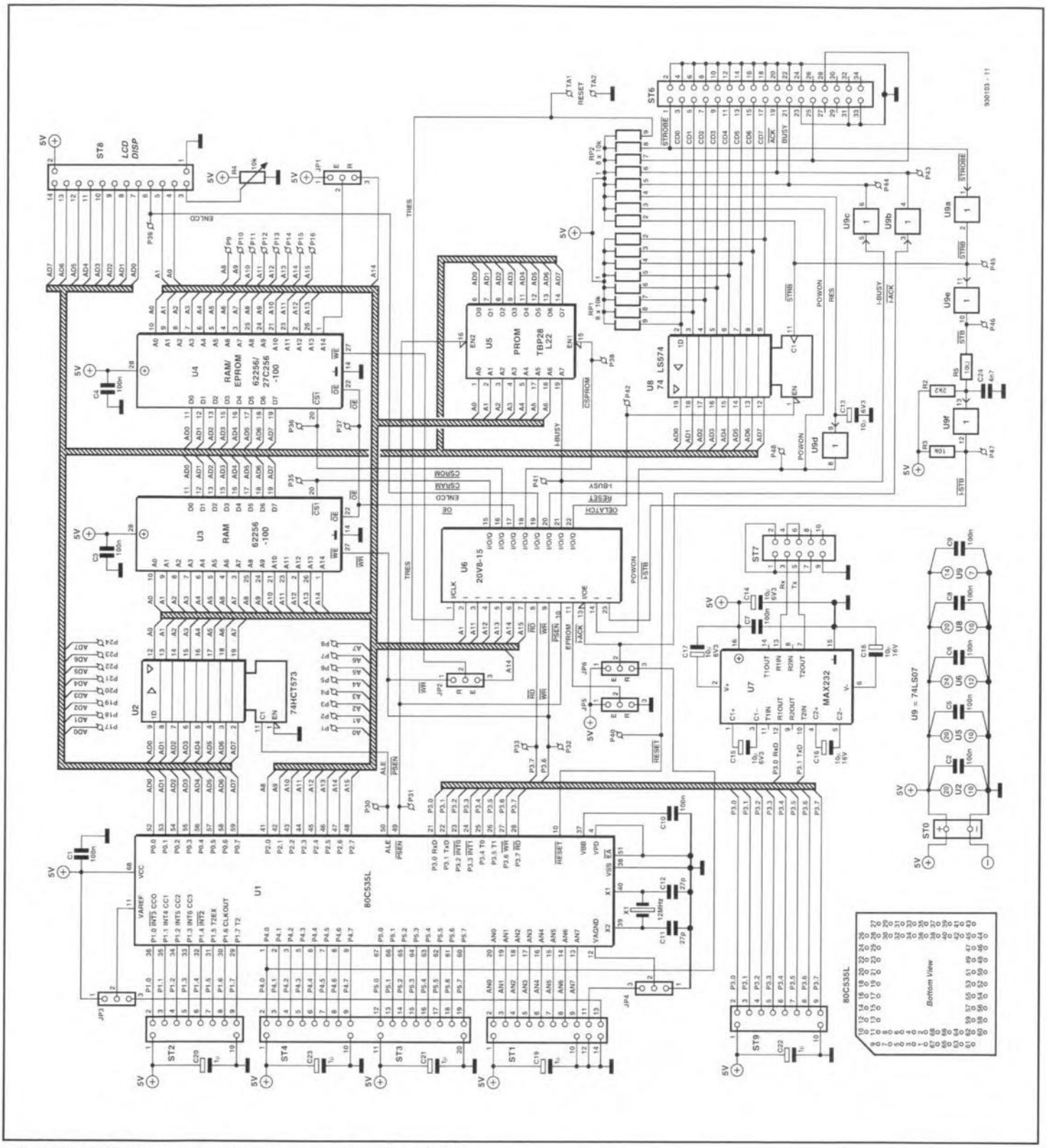



**Fig. 2. Circuit diagram of the 535 board with EPROM emulator.**

processor is not interrupted while executing a program, irrespective of the instant BUSY goes high. By the way, BUSY can only go high if the processor is not looking into the emulator memory. The only change is that the program uses the one byte to detect that a new byte is available in the data latch, and ready for storing away. On completing this action, the emulator program supplies an acknowledge pulse via output P4.0. This pulse causes the BUSY line to be taken low again, and the computer supplying the data to be flagged that the next byte may be sent.

Once the emulator program is running, the controller no longer needs to be reset on a strobe pulse. It is sufficient at this point for the GAL to respond by taking the BUSY line high. The program does the rest.

When all data has been received, the GAL has to ensure that the circuit is returned to 'run' mode. For this purpose, the program records how long is took since the last byte arrived. After one second, the program initializes the controller ('soft' reset), and jumps to $8000_H$ to signal the change to 'run' mode.

The jump to $8000_H$ is explained as follows. The program memory has a size of 32 kByte, and can be addressed with 15 of the 16 address bits. The 16th address bit, A15, is used in the circuit to select (address) the program, rather than for address decoding (which also goes for the GAL). Consequently, a jump to $8000_H$ is the

same as a jump to $0000_H$ (the address at which the controller starts after a reset). The only difference is that A15 goes logic high at address $8000_H$. This is detected by the GAL, which responds by switching the system to 'run' mode, when the data memory is enabled again, and the program memory serves to hold the program again. The upshot is that the controller starts executing the instruction at address $0000_H$ in the program memory, exactly one second after receipt of the last byte transmitted by the PC.

The memory map of the 535 board is determined by the structure of the address decoder contained in the GAL — see **Table 1**. In contrast with the program memory, the 16th address bit is decoded for the data memory. This prevents the 32-kByte large RAM from appearing two times in the memory map.

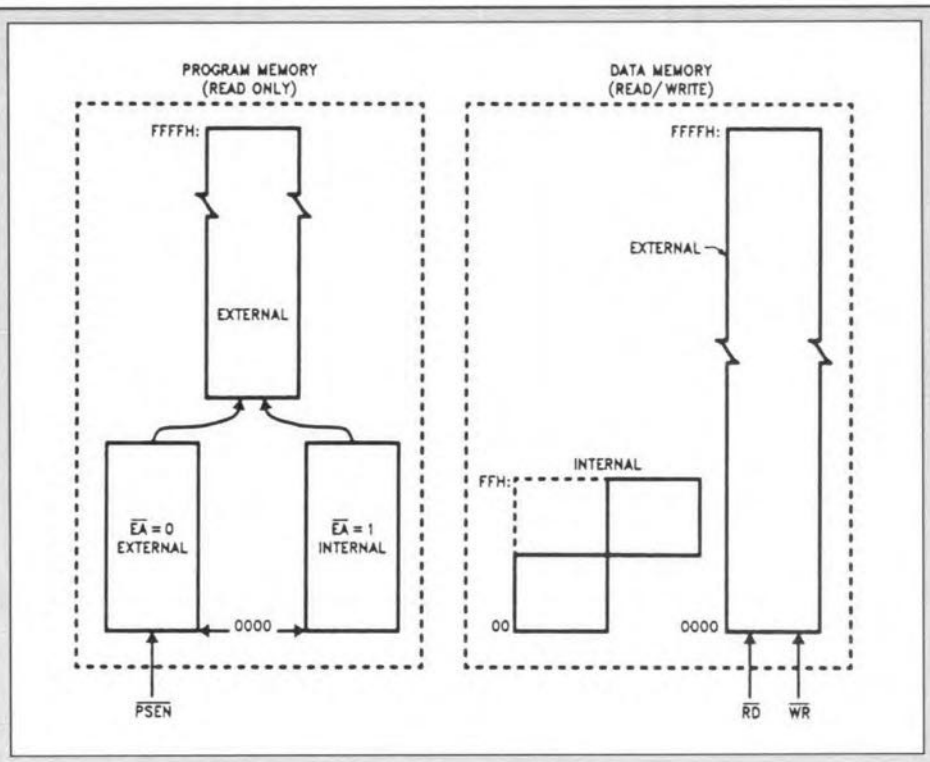
The second piece of data memory (also 32 kByte) contains a number of things. To begin with, there is the address of the data latch which serves to direct data into the system. Since its address decoding is limited to lines A14 and A15, the latch appears at a number of locations in the memory map. Next, memory space is reserved for an LC display, which is an optional extension of the 535 board. An example of an LCD that may be connected straight away is the Hitachi LM093LN, which was described in Ref. 1. The LCD also has a number of 'mirror' addresses in the memory. The next higher memory block has a size of 11 kByte, and may be used for extra I/O or RAM.

The highest part of the data memory has a size of 16 kByte, and offers a number of interesting applications. For instance, the upper half of the program memory ($4000_H$ to $7FFF_H$) may be used as data memory. In this way, it becomes possible to place data (default settings, look-up tables, etc.) into the program memory. This feature will be particularly valued in non-experimental systems, where such data is 'read-only' because it is contained in EPROM. It also allows a system without an external data memory to be set up, in which internal registers are used to store temporary data, while the fixed data are found in the program memory via addresses $C000_H$ to $FFFF_H$.

Since the resetting of the controller is also used to switch between 'run' and 'emulator' mode, it is not possible to connect the controller's reset input to a press-key. The same goes for the usual *RC* network to furnish a power-on reset pulse. To ensure proper timing and co-ordination, both reset signals are routed via the GAL. This ensures that the circuit is automatically switched to 'emulator' mode when the supply voltage is switched on. Pressing the reset key gives a totally different response from the GAL. The controller is also reset, but this time it starts executing the application program or the emulator program again.

Before turning to the circuit diagram, a word about using I/O bit P4.0 and the Centronics input in your own applications. Bit P4.0 consists of an open-drain output (with an internal pull-up resistor) which is connected in parallel with an input. This allows the bit to be used as an I/O port for your application, despite it being used as an output in 'emulator' mode. ❑

*Continued next month*




## MCS51 MEMORY STRUCTURE

The Siemens SAB80C535 is a member of the MCS51 family of microcontrollers. Originally designed by intel, the core and memory structure of all MCS51 family members is basically identical. The devices differ mainly in regard of the peripheral circuitry that has been added to the core.

An MCS51 controller has two types of memory: program memory and data memory. The controller can only read the program memory Is writing is not necessary because this area is usually ROM, PROM or EPROM. Some devices in the MCS51 family have an on-board mask-programmable ROM, or an EPROM. The presence of external memory is signalled with the aid of the $\overline{EA}$ (external access) pin, so that the controller 'knows' that the program memory is (partly) internal or (entirely) external.

The data memory always has an internal part, which also contains the so-called SFRs (special function registers). SFRs are addresses which are used to control the controller's peripheral circuits (I/O ports, timers, etc.). A part of this internal memory is 'hidden' behind a number of normally accessible addresses. The data contained in these indirect registers are accessible only by swapping them with data in directly accessible registers.

Independently of the internal data memory and the program memory, the controller is capable of addressing an extra amount of 64_kBytes of external data memory. This is achieved with the aid of separate instructions and address lines. This external data memory is usually RAM.

If the controller is not equipped with external memory, it is possible to use the data and address pins normally used for this purpose as an I/O port.

Since the controller can only read data from the data memory, it is often required to use a special initialization routine to put data in the data memory. This 'quirk' of the MCS51 processor is particularly annoying if fixed data is involved. A solution often adopted to solve this problem is to make a piece of the program memory visible as data memory to the controller. This is also done on the 535 board described in this article.

# OUTPUT AMPLIFIER WITH A.F. BAND-PASS FILTER

**Design by T. Giesberts**

The circuit consists of three parts: a steep-skirted speech filter, an integrated amplifier, and a power supply. The amplifier can provide an output of up to 1.2 W and may thus be used as an audio stage in home-constructed receivers.

The diagram of the circuit is shown in **Fig. 1**. Its sensitivity can be adjusted with potentiometer $P_1$. This potentiometer makes it possible for large signals, such as those at a headphone output socket, or the socket for a second loudspeaker, to be used. This enables the circuit to be used with a receiver without having to modify this (convenient in case of a type-approved unit, which cannot be tampered with for legal reasons). The signal at the wiper of $P_1$ is applied to filter $IC_{1a}$-$IC_{1b}$ and to switch $S_1$.

Depending on the setting of $P_1$, the signal is passed filtered or unfiltered to volume control $P_2$ and the amplifier. The filter consists of a low-pass section, $IC_{1a}$, and a high-pass section, $IC_{1b}$. Together these form a third-order band-pass filter with cut-off points at 740 Hz and 2.1 kHz. This

**Amateur listeners and DX-ers often have to contend with strongly distorted speech signals. The intelligibility of such signals can be improved appreciably by the circuit presented in this article.**

means that the bandwidth of the filter is narrower than that of a telephone signal, so that much interference is suppressed. However, a small part of the speech signal is also suppressed, so that it may become difficult to recognize a familiar voice. The frequency characteristics of the circuit with the filter actuated and with it disabled are shown in **Fig. 3**.

The d.c. operating point of the two filter opamps is set by $R_4$ and $R_5$. The + input of $IC_{1b}$ is set to half the supply voltage. Since this opamp has unity amplification, the + input of $IC_{1a}$ is also at half the supply voltage. The two resistors are decoupled by $C_4$, so that filter elements $R_1$ and $R_3$ are connected to ground, as they should be.

The amplifier comprises a single IC ($IC_2$) that contains a bridge amplifier complete with several protection circuits and a debouncing circuit. Strictly speaking, it needs no external components, but in the present circuit some have been added. At the input, two anti-parallel connected diodes, $D_3$ and $D_4$, ensure that the input signal is limited. This is necessary, because the sensitivity of the amplifier, and thus of the filter which, as already stated, has unity gain, for full drive is 120–150 $mV_{pp}$.

At the output, which is normally connected directly to a loudspeaker, provision is made for a headphone. This is connected to only one of the output terminals. Since both terminals carry half the supply voltage, a coupling capacitor, $C_{12}$, becomes necessary (this is not needed with the loudspeaker which is connected to both terminals). $R_{11}$ ensures that $C_{12}$ is charged

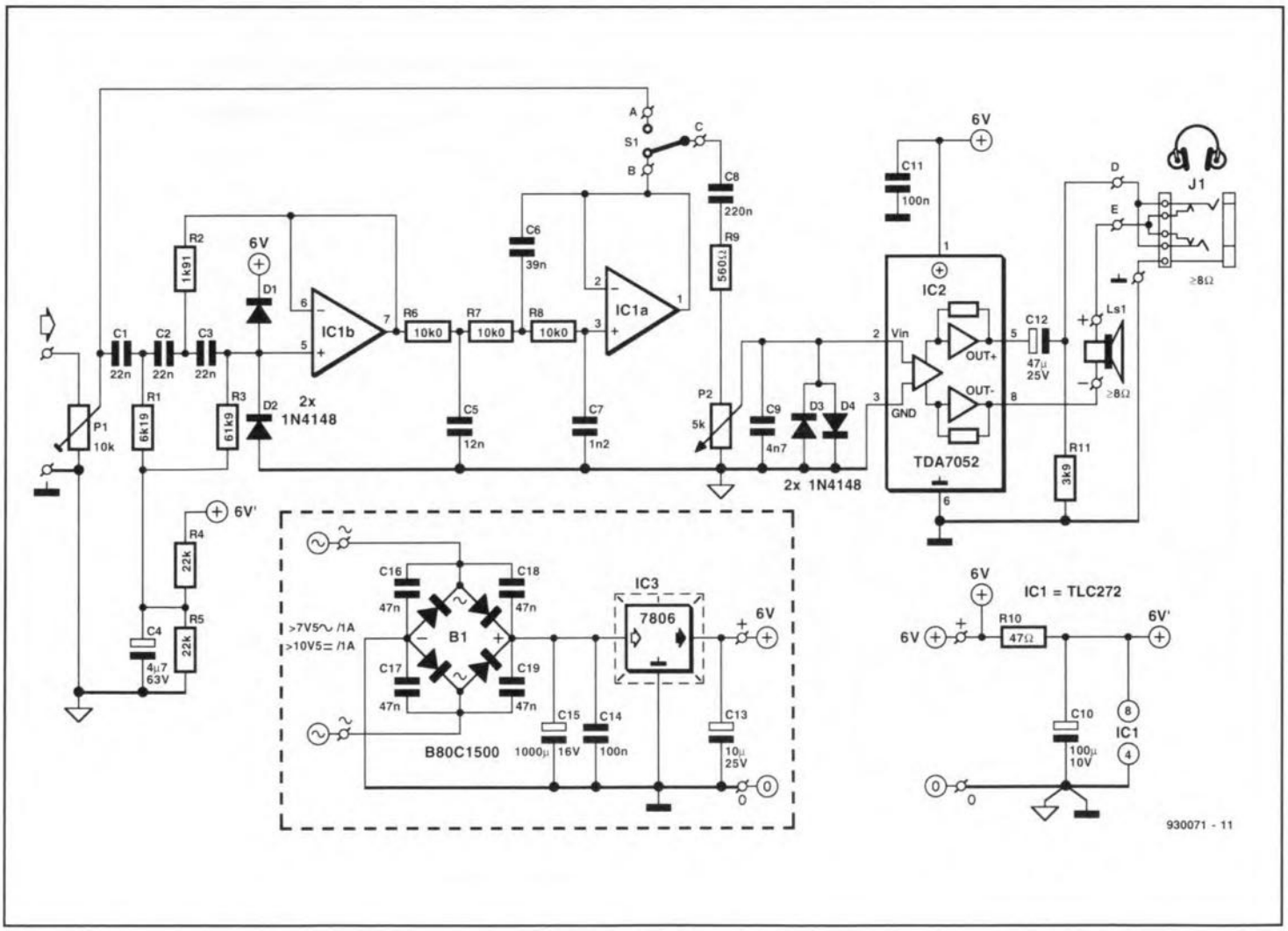



**Fig. 1. Circuit diagram of the amplifier and integral active band-pass filter.**

Fig. 2. General view of the completed printed-circuit board.

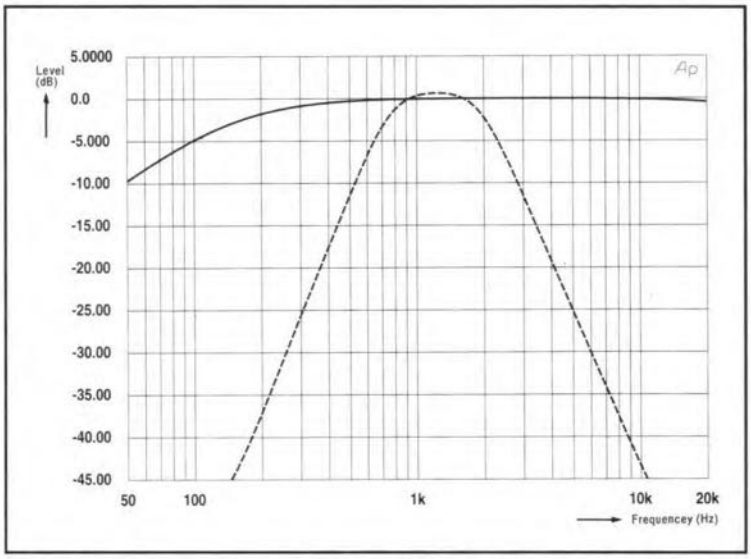



Fig. 3. Frequency characteristics of the amplifier withthe filter actuated and with the filter disabled.

and discharged, even when neither a loudspeaker nor headphones are connected. Although the headphone socket, $J_1$, is a stereo type, both earpieces carry the same signal.

It is possible to supply the unit from batteries, but these have a limited life, of course. If batteries are used, $IC_3$, $B_1$ and associated components may be omitted. It is, however, in many cases better to use a mains adaptor. This should be capable of providing 7.5 V a.c. or 10 V d.c. and a current of up to 1 A. Commercial adaptors normally have an output of 15 V and may be used with the filter and amplifier. The PCB (**Fig. 4**) has provision for a home-constructed mains adaptor; if batteries are used, this section of the board may be cut off.

Socket $J_1$, switch $S_1$ and potentiometer $P_2$ may be mounted on the board, but they may also be connected to the board via lengths of insulated circuit wire. **END**

**PARTS LIST**

**Resistors**:
$R_1$ = 6.19 kΩ, 1%
$R_2$ = 1.91 kΩ, 1%
$R_3$ = 61.9 kΩ, 1%
$R_4$, $R_5$ = 22 kΩ
$R_6$–$R_8$ = 10.0 kΩ, 1%
$R_9$ = 560 Ω
$R_{10}$ = 47 Ω
$R_{11}$ = 3.9 kΩ
$P_1$ = 10 kΩ preset potmeter
$P_2$ = 5 kΩ (4.7 kΩ) potmeter, log

**Capacitors**:
$C_1$–$C_3$ = 22 nF
$C_4$ = 4.7 µF, 63 V, radial
$C_5$ = 12 nF
$C_6$ = 39 nF
$C_7$ = 1.2 nF
$C_8$ = 220 nF
$C_9$ = 4.7 nF
$C_{10}$ = 100 µF, 10 V, radial
$C_{11}$, $C_{14}$ = 100 nF
$C_{12}$ = 47 µF, 25 V, radial
$C_{13}$ = 10 µF, 25 V, radial
$C_{15}$ = 1000 µF, 16 V, radial
$C_{16}$–$C_{19}$ = 47 nF, ceramic

**Semiconductors**:
$D_1$–$D_4$ = 1N4148
$B_1$ = B80C1500 bridge rectifier

**Integrated circuits**:
$IC_1$ = TLC272
$IC_2$ = TDA7052
$IC_3$ = 7806

**Miscellaneous**:
$S_1$ = change-over switch
$J_1$ = stereo audio socket, 6.3 mm, with integral switch
$LS_1$ = loudspeaker, 8 Ω, 1 W
Heat sink for $IC_3$ (about 17 K W$^{-1}$)
PCB No. 930071 (see page 70)

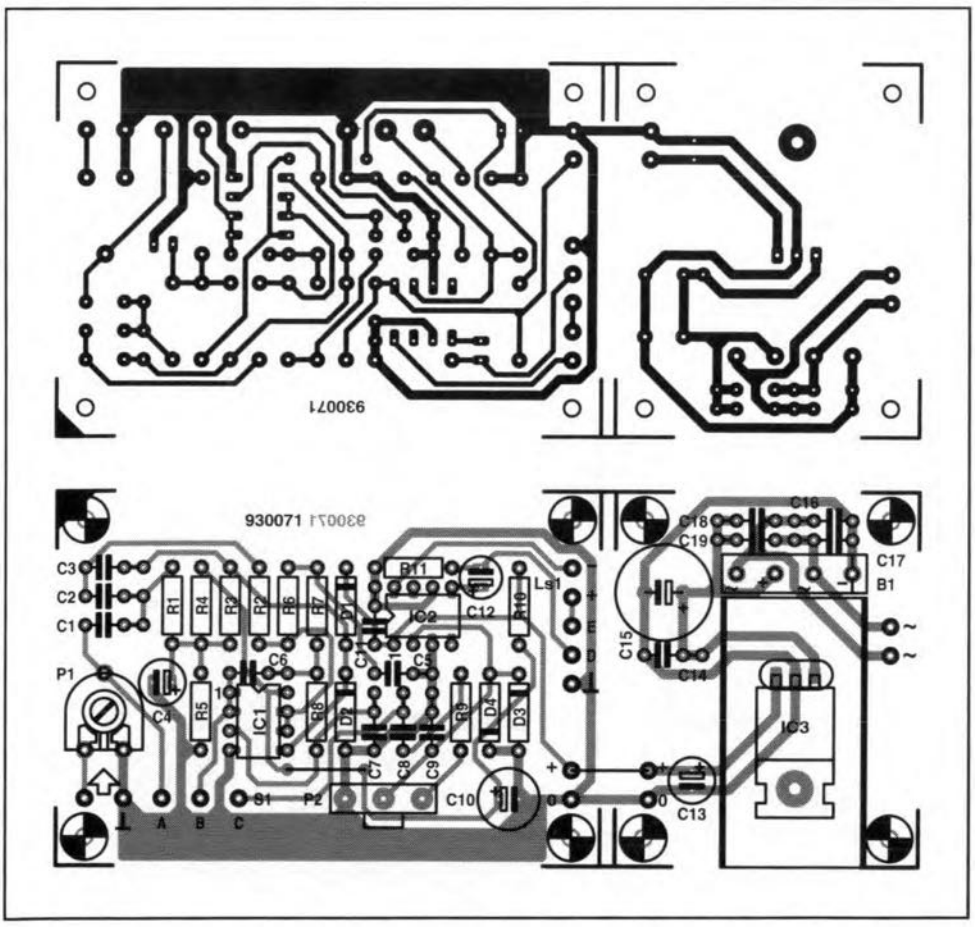
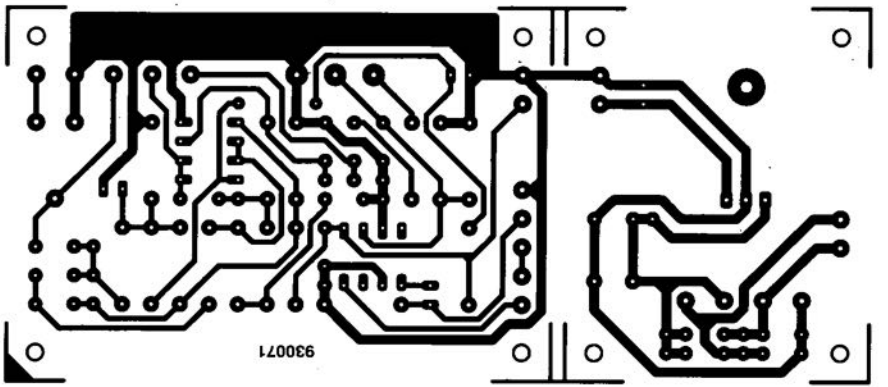



Fig. 4. Printed-circuit board for the amplifier and integral active a.f. band-pass filter.




$C_1$–$C_3$ = 22 nF
$C_4$ = 4.7 µF, 63 V, radial
$C_5$ = 12 nF
$C_6$ = 39 nF
$C_7$ = 1.2 nF
$C_8$ = 220 nF
$C_9$ = 4.7 nF
$C_{10}$ = 100 µF, 10 V, radial
$C_{11}$, $C_{14}$ = 100 nF
$C_{12}$ = 47 µF, 25 V, radial
$C_{13}$ = 10 µF, 25 V, radial
$C_{15}$ = 1000 µF, 16 V, radial
$C_{16}$–$C_{19}$ = 47 nF, ceramic

**Semiconductors:**
$D_1$–$D_4$ = 1N4148

# FIGURING IT OUT

## PART 10 – POWER

By Owen Bishop

**This series is intended to help you with the quantitative aspects of electronic design: predicting currents, voltage, waveforms, and other aspects of the behaviour of circuits. Our aim is to provide more than just a collection of rule-of-thumb formulas. We will explain the underlying electronic theory and, whenever appropriate, render some insights into the mathematics involved.**

In all our analyses of networks and circuits, we have been concerned with currents and potential differences, but have never considered their joint effect, **power**. Given a circuit element with a pd $U$ across it and a current $I$ flowing through it, the **instantaneous power**, $P_i$, is the product of $U$ and $I$:

$$P_i = UI. \qquad \text{[Eq. 64]}$$

Instantaneous power is measured in watts. It is the rate of conversion from one form to another at a given instant of time. In the case of resistance, electrical energy is being converted into heat energy. In a capacitor being charged, energy is being used to build up a charge on the plates against the opposition of the charge already existing there. In terms of energy, the watt (W) is equivalent to the expenditure of energy at the rate of 1 joule (J) per second:

$$1\ \text{W} = 1\ \text{J sec}^{-1}.$$

With a resistor or resistive element, we also have the relationships $U = IR$ and $I = U/R$. Substituting these in Eq. 64, we obtain two more equations for instantaneous power:

$$P_i = I^2R, \qquad \text{[Eq. 65]}$$

and

$$P_i = U^2/R. \qquad \text{[Eq. 66]}$$

As an example of the application of these equations, let us analyse a purely resistive network with a steady voltage applied to it. In such conditions, instantaneous power is constant. **Figure 84** is an example of a purely resistive network that may be analysed

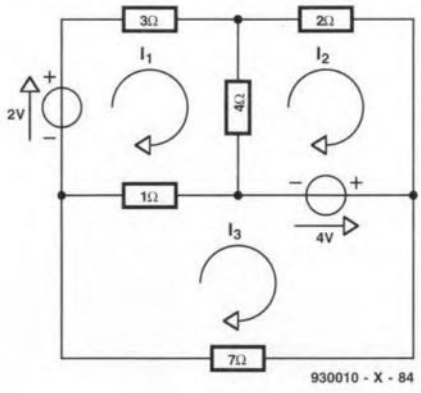



**Fig. 84.**

by the method of mesh analysis described in Part 3. First, we write out the equations for the three meshes:

$$\begin{aligned} 8I_1 - 4I_2 - I_3 &= 2; \\ -4I_1 + 6I_2 &= -4; \\ -I_1 + 8I_3 &= 4. \end{aligned}$$

These are solved as three simultaneous equations, aided if possible by a scientific calculator or the computer program for determinants (Part 4). The results are:

$I_1 = -0.032$ A;

$I_2 = -0.688$ A;

$I_3 = 0.496$ A.

**Figure 85** shows the currents in each branch of the network, combining the currents for two meshes where an element is part of two meshes. We use Eq. 65 to calculate the power being dissipated in each resistor:

3 Ω: $P = 0.032^2 \times 3 = 0.003$ W;
2 Ω: $P = 0.688^2 \times 2 = 0.947$ W;
4 Ω: $P = 0.656^2 \times 4 = 1.721$ W;
1 Ω: $P = 0.528^2 \times 1 = 0.279$ W;
7 Ω: $P = 0.496^2 \times 7 = 1.722$ W.

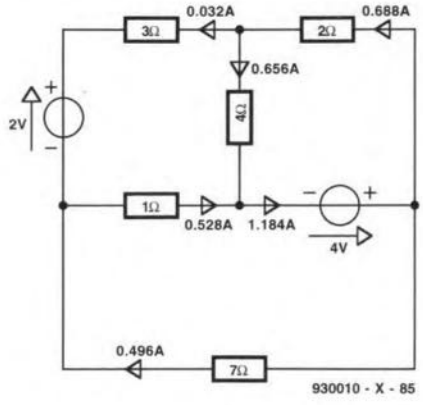



**Fig. 85.**

This adds up to a total resistor power of 4.672 W, that is, the resistors are converting electrical energy into thermal energy at the rate of 4.672 J $s^{-1}$. Note that the direction in which the current is flowing through the resistor makes no difference to the amount of energy being converted.

It follows from the Principle of Conservation of Energy that no energy is created or lost during this process. The energy is coming from the power sources supplying this network. The total energy supplied must equal the total energy converted to heat. This is a good check on the correctness of the current and power calculations. We calculate the energy being converted from chemical form (if it is a battery) or from mechanical form (if it is a generator) by the 4 V source. Use Eq. 64:

$$P_i = 4 \times 1.184 = 4.736\ \text{W}.$$

This is **more** than the energy being dissipated by the resistors! But let us look at the 2 V source. The energy being converted there is:

$$P_i = 2 \times -0.032 = -0.064\ \text{W}.$$

Here the direction of the current **does** matter. The calculations showed that that $I_1$ is negative, so that it flows anticlockwise around mesh 1 (**Fig. 84**), that is, **against** the polarity of the 2 V source. The current is supplying power to the source. If the source were a rechargeable cell, the current would be charging it. This fact makes the power equations balance correctly:

$P_{tot} = 4.672 + 0.064 = 4.736$ W
and
$P_{s4} = 4.736$ W,

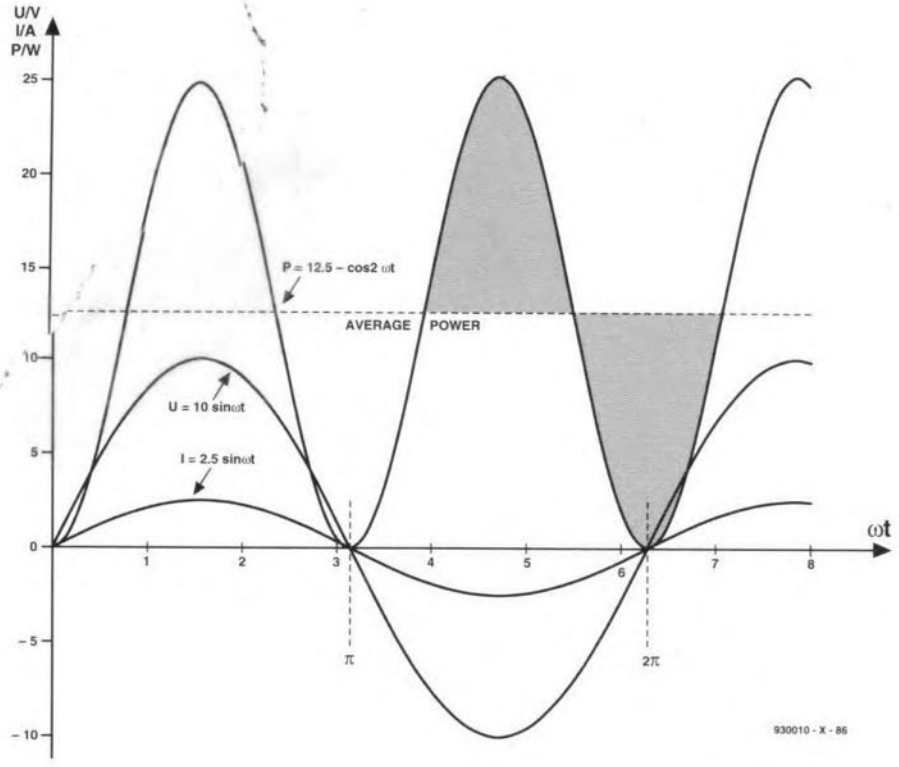



Fig. 86.

where $P_{tot}$ is the total power supplied **to** the resistors and the 2 V source, and $P_{s4}$ is the power supplied **by** the 4 V source.

In general, the total power supplied must equal the total power absorbed. From a practical point of view, it is interesting to note that the power dissipation varies widely between resistors. Calculations of this kind point to the components that need to be highly power rated.

## AC power

A sinusoidal voltage, $U = 10 \sin \omega t$, is applied across a 4 Ω resistor. The current through the resistor has the same frequency and is in phase with the voltage:

$$I = U/R = (10 \sin \omega t)/4 = 2.5 \sin \omega t.$$

The instantaneous power is, as before, the product of the pd and the current:

$$P_i = UI = 10 \sin \omega t \times 2.5 \sin \omega t = 25 \sin^2 \omega t. \quad [\text{Eq. } 67]$$

We make use of the trigonometric identity:

$$\cos 2\theta \equiv 1 - 2 \sin^2 \theta,$$

which gives:

$$\sin^2 \theta = (1 - \cos 2\theta)/2.$$

Substituting this in Eq. 67:

$$P_i = 25 \times (1 - \cos 2\omega t)/2 = 12.5 - 12.5 \cos 2\omega t. \quad [\text{Eq. } 68]$$

**Figure 86** shows the graphs for $U$, $I$ and $P_i$ plotted on the same scale; $U$ and $I$ are in phase, oscillating about zero. The graph for $P_i$ oscillates about 12.5 W. This level is the **average** or **apparent** power, $S$, since the curve is symmetrical about the line $P = 12.5$, as indicated by the shaded areas in **Fig. 86**. Note that the instantaneous power oscillates with a frequency which is twice that of $U$ and $I$. Current and voltage are both positive together from $\omega t = 0$ to $\pi$ and also from $\pi$ to $2\pi$. Thus, $S$ is always positive. This is another way of saying that the direction in which the current flows through the resistor makes no difference to the amount of power dissipated.

Another way of calculating average power is

$$S = U_{rms} \times I_{rms}.$$

In this example,

$U_{rms} = 10/\sqrt{2}$,
$I_{rms} = 2.5/\sqrt{2}$, and
$S = (10 \times 2.5)/(\sqrt{2} \times \sqrt{2}) = 25/2 = 12.5$.

This is the same result as obtained by the earlier calculation.

## Capacitive circuit

If the same sinusoidal voltage is applied across a capacitor, the current is also sinusoidal an d of the same frequency, but leads the voltage by 90° (see Parts 2 and 5). We say that $I = I_0 \sin(\omega t + 90°)$. Or we can consider the current curve is a cosine curve and that $I = I_0 \cos \omega t$, which is trigonometrically the same thing. The value $I_0$, that is, the amplitude of the current curve, is determined by the reactance of the capacitor:

$$I_0 = U_0/X_C = U_0 \omega C.$$

In this example, $U_0 = 10$ V, and let us assume that $C = 1000$ µF and $\omega = 400$. This makes $I_0 = 4$, and $I = 4 \cos \omega t$. The curves for $U$ and $I$ are plotted in **Fig. 87**.

The instantaneous power is, as before, the product of $U$ and $I$:

$$P_i = 10 \sin \omega t \times 4 \cos \omega t = 40 \sin \omega t \times \cos \omega t.$$

Once again, we make use of a trigonometrical identity:

$$\sin 2\theta = 2 \sin \theta \cos \theta.$$

The power equation then becomes

$$P_i = (40 \sin 2\omega t)/2 = 20 \sin 2\omega t.$$

This equation is also plotted in **Fig. 87**: the cxurve has amplitude 20 and frequency **twice** that of $U$ and $I$. In general, the amplitude may be calculated with

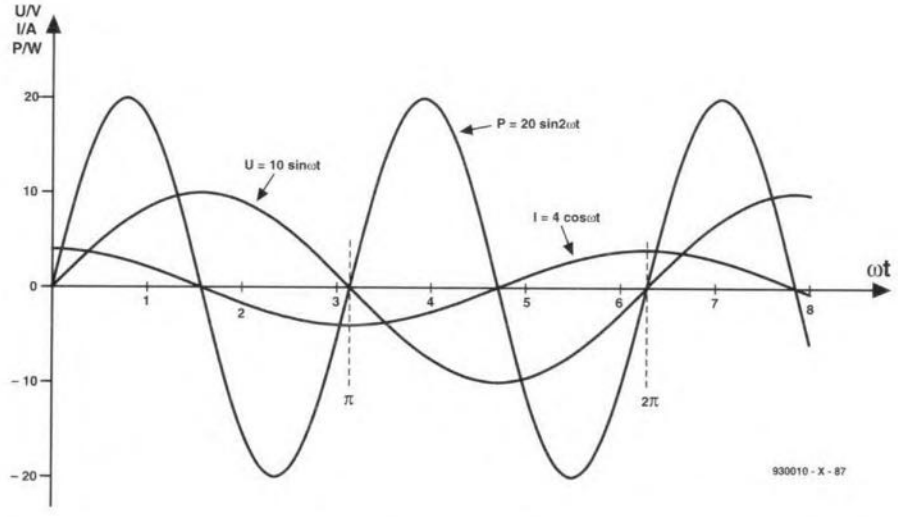



Fig. 87

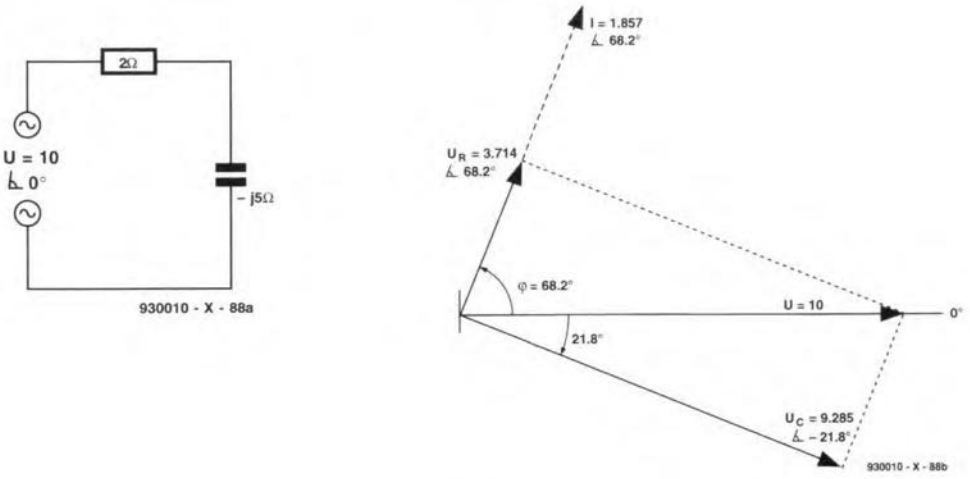



**Fig. 88.**

the equation:

$$P_i = U_{rms} \times I_{rms} \times \sin 2\omega t$$
$$= [(U_0 I)/(\sqrt{2} \times \sqrt{2})] \times \sin 2\omega t$$
$$= {}^1/_2 U_0 I_0 \sin 2\omega t.$$

One point to notice in **Fig. 87** is that the power curve is symmetrical about the $x$-axis. In other words, average power is zero. Instantaneous power is zero when either $U$ or $I$ is zero. Power is positive and energy is being transferred to the capacitor when both $U$ and $I$ are of the same sign. Work is being done against the repulsive force due to the charge already present: the charge on the capacitor is increasing. Power is negative and energy is being transferred from the capacitor to the circuit when $U$ and $I$ are of opposite sign. The charge of the capacitor is decreasing.

*Example.* A pd of $U = 3 \sin 4000t$ is applied across a 22 µF capacitor. What is the instantaneous power when $t = 1$ ms? From the equation, we identify the values of $U_0 = 3$ and $\omega = 4000$ (the frequency is 637 Hz). Calculate $I_0$:

$$I_0 = U_0 / X_C = U_0 / \omega C$$
$$= 3 / (4000 \times 22 \times 10^{-6})$$
$$= 34.09 \text{ A}.$$

Thus, the current equation is:

$$I = 34.09 \cos 4000t.$$

Instantaneous power is:

$$P_i = {}^1/_2 \times 3 \times 34.09 \times \sin(2 \times 4000t)$$
$$= 51.14 \sin 8000t.$$

When $t = 1$ ms,

$P_i = 51.14 \sin 8 = 50.6$ W.

## Inductive circuit

Similar behaviour is shown by an inductor, except that being the dual (Part 5) of a capacitor, some of the properties are inverted. Following the same lines of argument, if the applied pd is as before:

$$U = U_0 \sin \omega t.$$

Current lags the voltage:

$$I = -I_0 \cos \omega t.$$

Instantaneous power is:

$$P_i = -U_0 I_0 \sin 2\omega t$$
$$= -{}^1/_2 U_{rms} I_{rms} \sin \omega t.$$

The instantaneous power oscillates at twice the frequency, and average power is zero. Since the power curve is a negative sine curve, it is the inverse of the power curve of **Fig. 87**. Energy is being stored when $U$ and $I$ are of oppopsite sign (power positive) and is returned to the circuit when $U$ and $I$ are of the same sign (power negative).

*Example.* A pd $U = 4 \sin 5000t$ is applied across a 15 µH inductor. What is the instantaneous power when $t = 1$ ms? From the equation, we identify the values of $U_0 = 4$ and $\omega = 5000$. Calculate $I_0$:

$$I_0 = U_0 / X_L = U_0 / \omega L$$
$$= 4 / (5000 \times 15 \times 10^{-6})$$
$$= 53.33 \text{ A}.$$

Thus, the current equation is:

$$I = -53.33 \cos 5000t.$$

Instantaneous power is:

$$P_i = -{}^1/_2 \times 4 \times 53.33 \times \sin(2 \times 5000)t$$
$$= -106.7 \sin 10\,000t.$$

When $t = 1$ ms,

$P_i = -106.7 \sin 10 = 58.0$ W.

We have been preoccupied with sinusoidal signals, but voltage or current may vary in other ways. The voltage may be a ramp, for example, $U = 3t$. If such a voltage is applied to an inductor, the current may be calculated from Eq. 28 (Part 5).

Assuming there is no initial current:

$$I = {}^1/_L \int U \, dt = 3t^2 / 2L.$$

If $L$ has the value 0.5 H, then $I = 3t^2$. At any instant,

$$P_i = UI = 3t \times 3t^2 = 9t^3.$$

Conversely, we can calculate power when we are given the applied current. For instance, given that the current through a 0.1 H inductor is $I = 4e^{2t}$, we use Eq. 26 to calculate that

$$U = L dI/dt = 8Le^{2t} = 0.8e^{2t},$$

and

$$P = UI = 0.8e^{2t} \times 4e^{2t} = 3.2e^{4t}.$$

The power after 0.5 s is $3.2e^2 = 23.6$ W.

Calculations such as these assume that the network is in a steady state, by which we mean that the function for $U$ or $I$ is continuous, not piecewise. If there are abrupt changes in $U$ or $I$, a reactive impedance, as might be expected from its name, **reacts** to cushion or even to oppose the change. In passing from one steady state to another there is a **transient** period. The analysis of what happens in such brief periods is a fascinating one which we shall leave until a later issue.

## Mixed impedance

The examples above apply only to networks that are purely capacitive or purely inductive, so that the voltage and current are 90° out of phase. If the phase angle is other than this, a different situation arises. Consider the example of **Fig. 88**. The applied voltage and the impedance of the capacitor are expressed as complex numbers (see Parts 8 and 9). The total impedance,

$$Z = 2 - \mathbf{j}5 = 5.385 \angle -68.2° \ \Omega$$

in polar form. From this, we calculate $I$, which is the same for both components:

$$I = U / Z$$
$$= 10 \angle 0° / 5.385 \angle -68.2°$$
$$= 1.857 \angle 68.2° \text{ A}.$$

Now look at the power developed in the individual impedances. For this we need to know the pds across them:

$$U_R = RI = 2 \times 1.857 \angle 68.2°$$
$$= 3.714 \angle 68.2° \text{ V}.$$

$$U_C = X_C I = -\mathbf{j}5I$$
$$= 5 \angle -90° \times 1.857 \angle 68.2°$$
$$= 9.285 \angle -21.8° \text{ V}.$$

The phasor diagram in **Fig. 88** shows the relationship between these quantities. Current in the network is in phase with the pd across the resistor. It is 90° out of phase with the pd across the capacitor.

As far as the capacitor is concerned, the voltage-current relationship is the same as in **Fig. 87**, in which we saw that the average power is zero. During a whole number of cycles, the capacitor neither absorbs nor supplies energy.

For the resistor, the power may be calculated as in Eq. 64.

In a phasor diagram, all phasors must have the same angular frequency. Since power has double the angular frequency, we cannot show it in **Fig. 88,** neither can we calculate it by vector multiplication. However, since we are concerned with only two vectors, $I$ and $U_R$, which have the same direction, ordinary scalar multiplication is applicable. We do not use the moduli of the complex numbers directly, since these equal the **amplitudes** of the current and voltage. For a.c. power calculations, we need to use r.m.s. values as noted above:

$$U_{rms} = \text{mod } U_R / \sqrt{2}$$
$$= 3.714 / \sqrt{2} = 2.626 \text{ V}.$$

$$I_{rms} = \text{mod}\, I / \sqrt{2}$$
$$= 1.857 / \sqrt{2} = 1.313 \text{ A.}$$

From Eq. 64:

$$P = 2.626 \times 1.313 = 3.45 \text{ W.}$$

This is the **true** (or **active**) **power** dissipated in the network.

There is another way of looking at the power calculation. Knowing $U$, we can calculate $I$ and the phase angle $\varphi$. Then:

$$P = S \cos \varphi,$$

where $P$ is the active power, $S$ the apparent power ($U_{rms}I_{rms}$), and cos $\varphi$ the **power factor**. If $U$ and $I$ are in phase, as in a purely resistive network, $\varphi = 0°$ and cos $\varphi = 1$. The **whole of the apparent power**, $S$, is dissipated in the network. If $U$ and $I$ are 90° out of phase, as in purely capacitive or inductive circuits, $\varphi = 90°$ and cos $\varphi = 0$, and none of the power is dissipated in the network.

With mixed networks, when $U$ and $I$ are neither wholly in phase nor wholly out of phase, the power factor tells us what proportion of $S$ is being dissipated. We call the dissipated portion the **active** power, $P$, and the non-dissipated portion the **reactive power**, $Q$.

The apparent power is not expressed in watts, as there may be no or little actual conversion of energy, but in volt-amperes (VA). With reactive power, sometimes known as the **wattless component**, there is no conversion of energy; it is expressed in volt-ampere reactive (VAr).

## Power factor

We shall now see how to calculate the power factor of a circuit as in **Fig. 89**. If you have a circuit with impedances marked in ohms, henrys and farads, the first step is to calculate the complex impedances for the given frequency. These impedances have already been marked in the diagram. Next, we calculate the total impedance, $Z$, summing for the two branches and then using the standard formula for impedances in parallel.

$$Z = \frac{(10+\mathbf{j}3)(5-\mathbf{j}12)}{(10+\mathbf{j}3)+(5-\mathbf{j}12)}$$
$$= \frac{86-\mathbf{j}105}{15-\mathbf{j}9}$$
$$= \frac{135.7\angle -50.68°}{17.49\angle -30.964°}$$
$$= 7.758\angle -19.716° \quad [\Omega]$$

Now we calculate the current

$$I = U/Z$$
$$= 10\angle 0° / 7.758\angle -19.716°$$
$$= 1.289\angle -19.716° \quad [A]$$

The angle between the voltage phasor and the current phasor is 19.719°. The power factor, $pf$, is the cosine of the angle:

$$pf = \cos 19.716 = 0.941.$$

Another way of arriving at the same result is to proceed as follows. After calculating $Z$ as before, convert it to rectangular form:

$$Z = 7.758\angle -19.716°$$
$$= 7.303 - \mathbf{j}2.617. \quad [\Omega]$$

The real part of $Z$ is the resistive part of the total impedance:

$$R = 7.303\ \Omega.$$

Having found $I$ as above, we ignore the argument (the phase angle) and take only the modulus, since current and pd are in phase for resistive elements. Using this, we calculate the true power from Eq. 65:

$$P = I^2R = 1.289^2 \times 7.303$$
$$= 12.134 \text{ W.}$$

The ratio between the true power and the apparent power gives the power factor:

$$pf = P/S$$
$$= 12.134 / (10 \times 1.289)$$
$$= 0.941.$$

**TO BE CONTINUED**

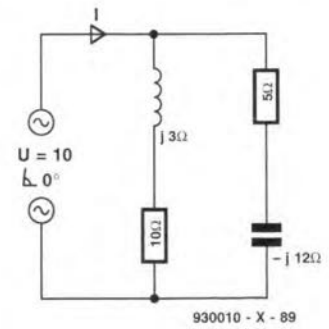



**Fig. 89.**

## Test yourself

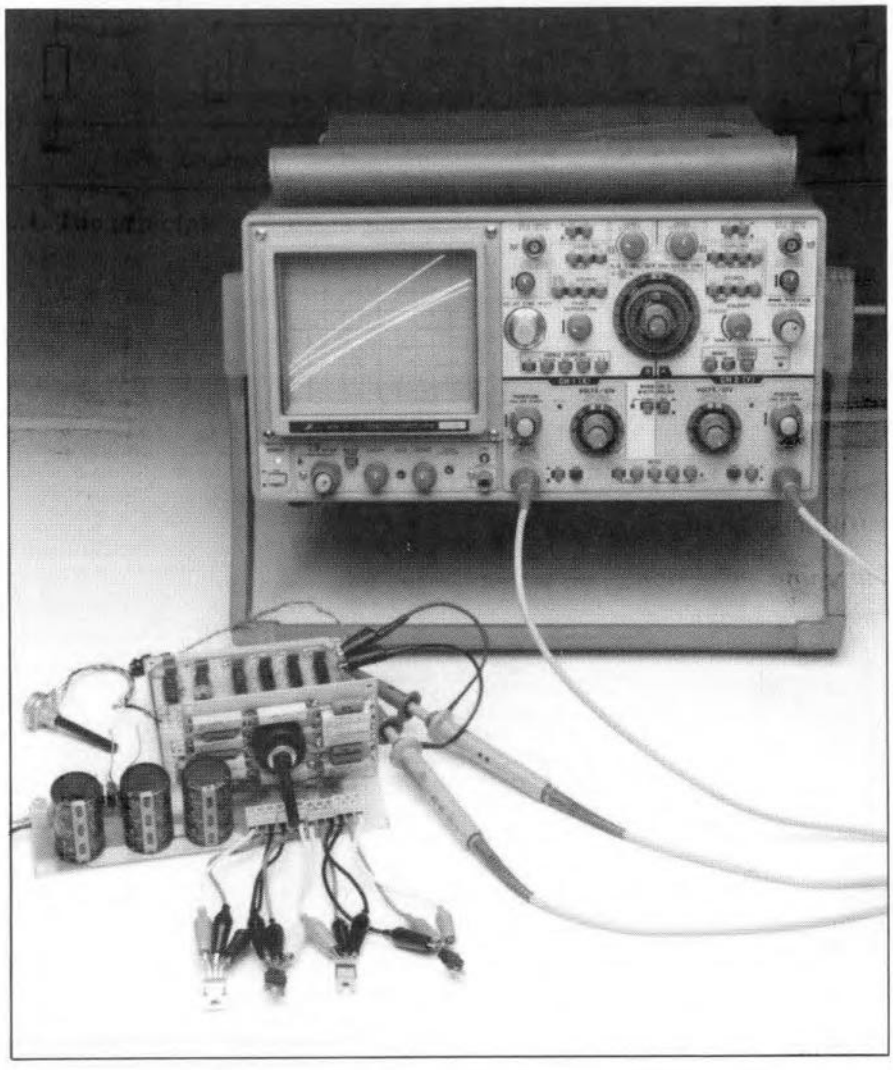
1. Calculate the power dissipated in each resistor of **Fig. 84** if the two voltage sources are interchanged. Confirm that the total power dissipated equals the total power supplied.
2. What is the average power dissipated by a 5 Ω resistor connected across a source $U = 20 \sin \omega t$?
3. A voltage $U = 4 \sin 2000t$ is applied across a 100 μF capacitor. What is (a) the instantaneous power when $t = 5$ ms, and (b) the average power?
4. A voltage $U = 2.5 \sin 3000t$ is applied across a 100 mH inductor. What is the instantaneous power when $t = 1.5$ ms?
5. A 40 Ω resistor and a 100 mH inductor are connected in series across a voltage source $U = 5 \sin 2000t$. Calculate the active power (i.e., that dissipated in the resistor).
6. Given the circuit of **Fig. 89**, calculate the power factor when the frequency is doubled.

## Answers to Test yourself (Part 9)

1. Product is (22+**j**7). Conversion gives: 3.606 ∠56.31° × 6.403 ∠–38.66° = 23.089 ∠17.65° = 22 + **j**7.
2. Quotient is (–1 + **j**2). Conversion gives: 8.062 ∠60.255° divided by 3.606 ∠–56.310° = 2.236 ∠116.565° = –1 + **j**2.
3. $I_1 = 3.444 - \mathbf{j}0.415$; $I_2 = 3.112 - \mathbf{j}0.830$; $I_3 = 0.332 + \mathbf{j}1.245$.
4. $I_2 = 18.570\angle 21.801°$. The current through the resistor is $I_1 - I_2$ clockwise. Its value is –3.448 + **j**8.6204 or 9.2845 ∠111.803°. The conversion at the last step may give the angle as –68.197°, but the negative sign of the real part of the rectangular form shows the resultant to be in the 2nd quadrant..
5. Without load: 0.37 ∠–68.3°. With load: 0.356 ∠–63.6°.

# POWER MOSFET TESTER

Design by T. Giesberts



The output signal of power amplifiers is usually provided by two transistors that each take care of one half of the signal. To ensure that these halves are processed in an identical manner – and that the d.c. operating point is stable – it is essential that the performance of the two devices is as near-identical as possible. This can be quite a problem, particularly in the case of a complementary output stage, because the designer needs to take into account not only the spread of the parameters, but also the differences ensuing from the dissimilar design and manufacture of n-p-n and p-n-p or n- and p-channel transistors.

**MOSFET output transistors should be as near-identical as possible, irrespective of whether they are complementary pairs or connected in parallel. The tester described here enables you to check that they are.**

An additional reason for matching MOSFET devices for use in power stages, is that in these amplifiers output transistors are often connected in parallel so that the amplifier can provide a higher current. If such transistors are very dissimilar, the current will be divided unequally between them. The transistor drawing the highest current will get hotter, which will accentuate the inequality, and the transistor will draw even more current. Soon it will be destroyed, so that the remaining transistors have to handle a higher current: this normally quickly leads to their destruction also.

The only way of minimizing the inequalities between two transistors is to find a matching pair from among many. This matching is best done in circumstances that are identical, or nearly so, to those in normal operation. Therefore, the present tester can provide drain currents of up to 13 A (peak).

## What needs to be tested?

The most important parameter that should be equal in two output transistors is the transfer function. In MOSFETs that is the relationship between the gate-source voltage, $U_{GS}$, and the drain current, $I_D$. To make that relation visible on an oscilloscope, a circuit is used in the tester whose principle is shown in **Fig. 1**. To enable n-channel as well as p-channel FETs to be tested, there are two complementary versions of the circuit. The circuit is driven by a direct voltage superimposed on a triangular voltage; it is designed to ensure that the current through the FET is directly proportional to this voltage. This task is carried out by the differential amplifier formed by the two transistors. Because of the feedback through the FET on test, the differential amplifier keeps the potential drop across $R_D$ equal to the drive voltage. Since only the FET can provide the current required to do so, it follows that $I_D$ is directly proportional to the drop across $R_D$ and thus to the drive voltage. To make the relationship between $I_D$ and $U_{GS}$ visible on an oscilloscope, use is made of the property that during the leading

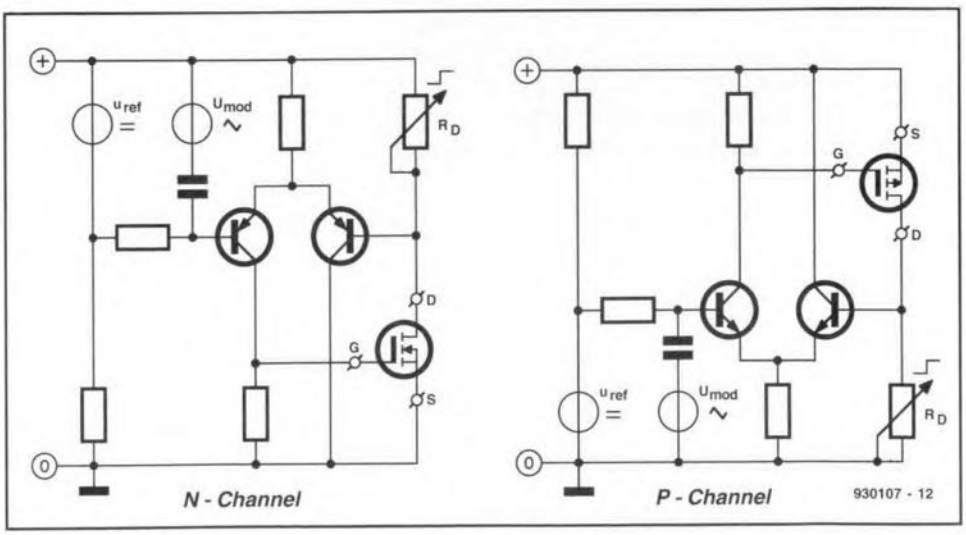



**Fig. 1. The principle of the power MOSFET tester.**

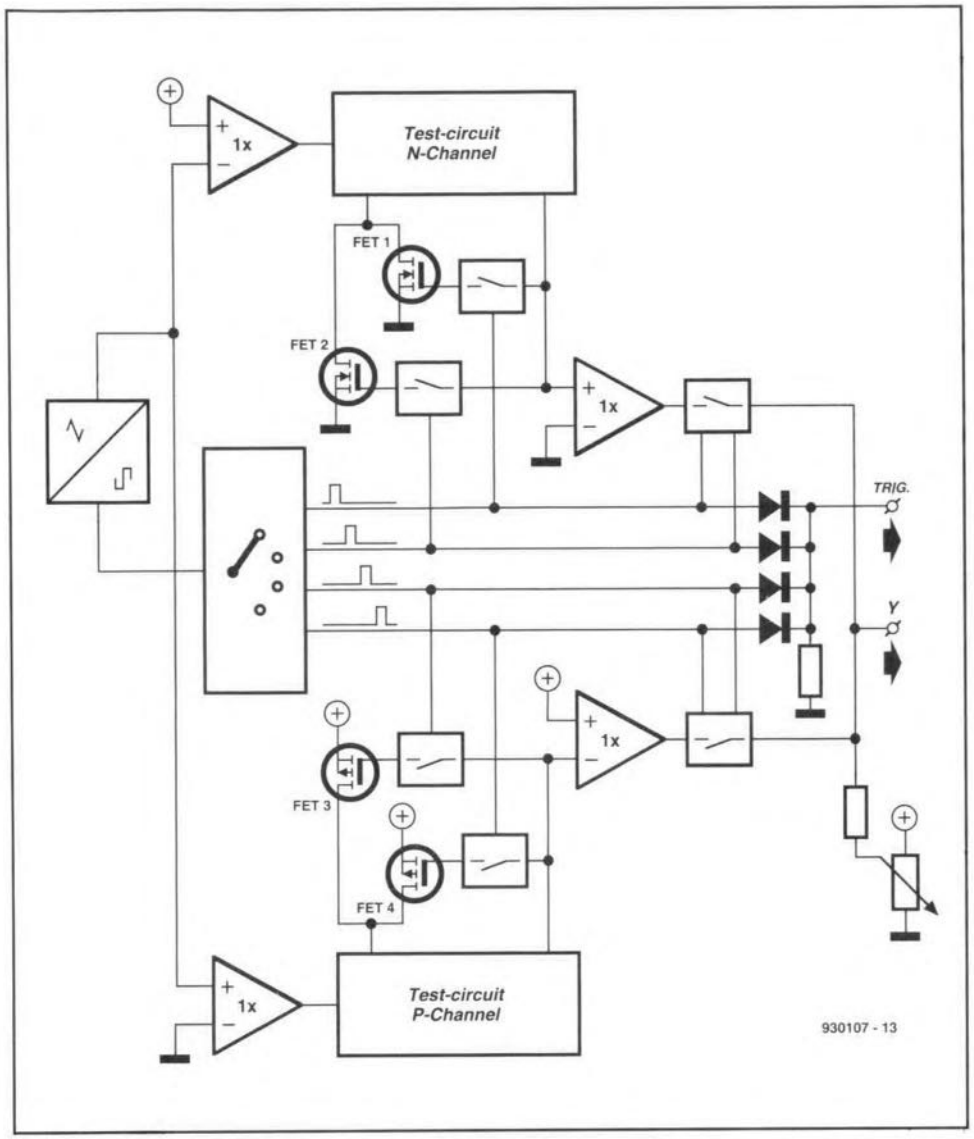



**Fig. 2. Block schematic diagram of the power MOSFET tester.**

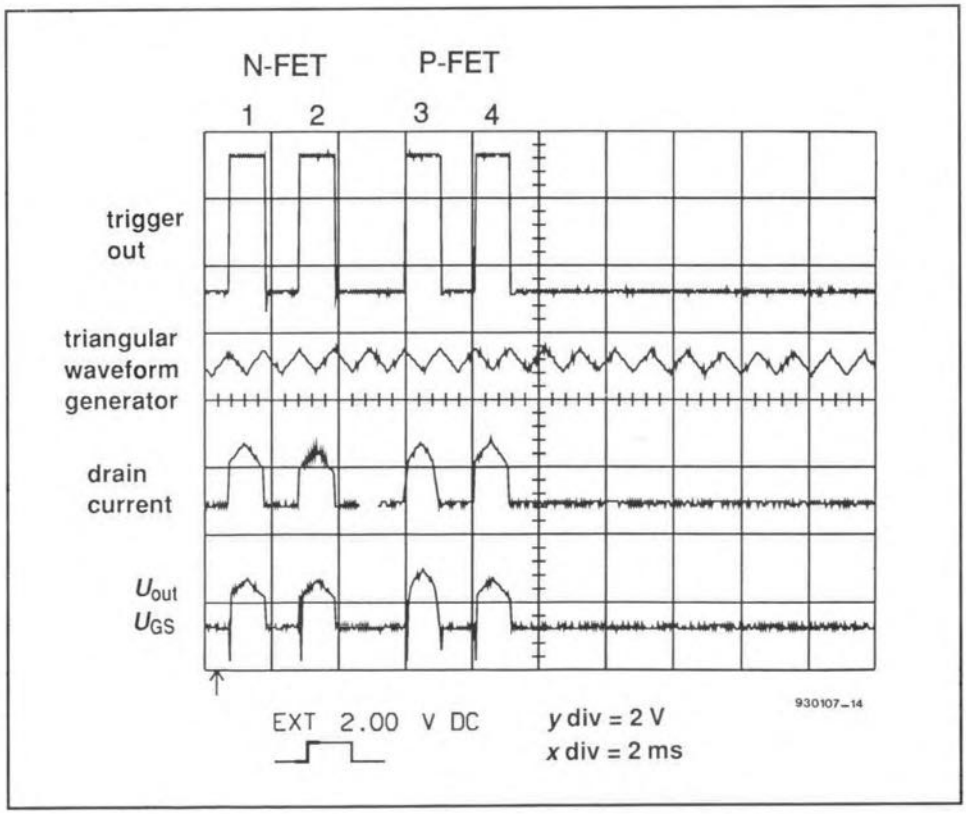



**Fig. 3. A number of important signals in the power MOSFET tester.**

edge of the triangular voltage, the drain current is directly proportional to the time. It suffices, therefore, to trigger the scope at the onset of the leading edge and to adjust the time base so that a sweep of the oscilloscope lasts exactly as long as the edge. This means that the drain current is portrayed on the $x$-axis of the oscilloscope. The gate-source voltage is depicted by connecting it to the $y$-axis. The oscilloscope then shows a clear $U_{GS} - I_D$ characteristic.

However, to make comparisons, the curves of at least two FETs must be displayed at the same time. The present design enables the simultaneous testing of two n-FETs; two p-FETs; an n-FET and a p-FET; or two n-FETs and two p-FETs. The latter possibility is particularly useful during the design of a complementary output stage with parallel connected output transistors. To display four curves, it is not enough to build four test circuits, because in one of them $U_{GS}$ must be measured with respect to ground and in another with respect to the positive supply rail. A similar problem occurs with the drive voltage of the test circuit.

**Figure 2** shows the basic design of the tester. The tester is driven by a generator that provides rectangular as well as triangular waveforms. The rectangular signal controls an electronic switch which switches the four FETs in turn ON for 1 ms and OFF for 99 ms. Since the devices are on for only $^1/_{100}$ of the time, they may be tested without a heat sink, even when they draw an average current of 10 A (13 A peak).

The operational amplifiers buffer the various signals and two of them perform the vital task of converting potentials that are referred to earth to voltages that are referred to the positive supply line and vice versa.

The electronic switches at the outputs arrange in the first instance that the output signals of two test circuits are applied to one oscilloscope input. In conjunction with a potentiometer, they also optimize the images of the curves: this is essential in view of the shape of these signals – see the bottom curve in **Fig. 3**. The shape of the pulses is the required $U_{GS} - I_D$ characteristic. Note the near-triangular apexes.

When the switches are closed, the operational amplifiers determine the output voltage (since they are ideal current sources). When they are open (i.e. none of the FETs is being measured), the potentiometer determines the output voltage. The potentiometer is used to shift the voltage level upwards during the measurements lulls until it is level with the apexes of $U_{GS}$. It is clear that in **Fig. 3** (bottom curve) the potentiometer had not been adjusted properly (yet). In this way, a steady voltage with a ripple superimposed on it is obtained. With the oscilloscope input set to AC, the ripple may be inspected in detail by increasing the sensitivity of the input amplifier.

This means that the time base of the oscilloscope must be set with some care. To display the four signals as in **Fig. 3**, it was set to 2 ms/div, which is a convenient setting for checking whether the FETs have been connected correctly and whether everything functions properly. However, for a detailed comparison of the FETs, the time base should be set (with the VAR control) to slightly more than 0.1 ms/div. If the oscilloscope is triggered by the TRIG output (set oscilloscope to normal trigger), it will display the four $U_{GS}$ - $I_D$ characteristics as shown on the introductory photograph. Any differences be-

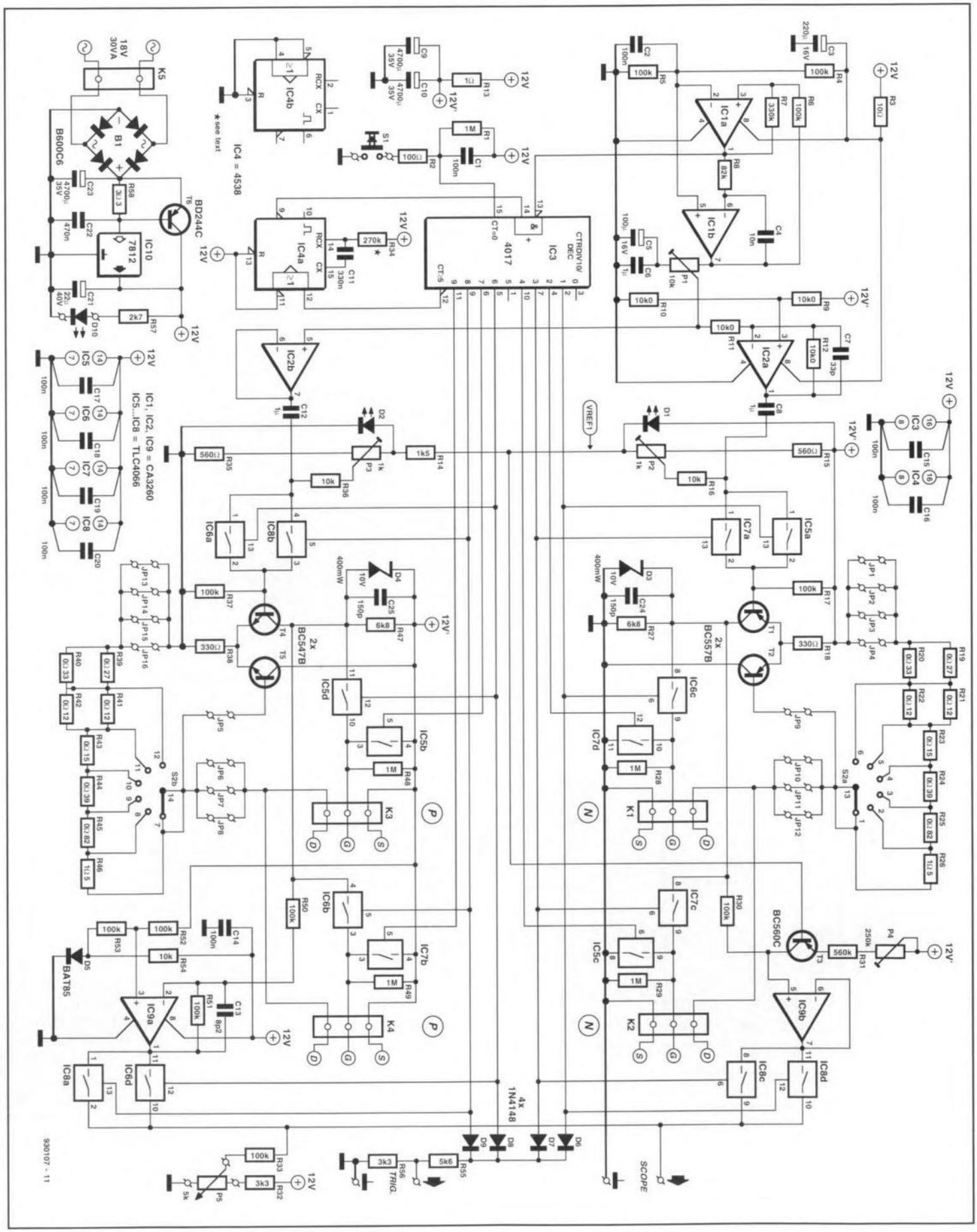



**Fig. 4. Circuit diagram of the power MOSFET tester.**

tween the FETs are then clearly visible.

## The circuit

The rectangular-triangular waveform generator is formed by Schmitt trigger $IC_{1a}$ and integrator $IC_{1b}$.

The rectangular signal clocks counter $IC_3$. This circuit serves as an electronic switch to switch the FETs on and off. After each FET has been switched, monostable multivibrator $IC_{4a}$ is triggered via pin 12 of the counter. The MMV then disables $IC_3$ for 90 ms, so that the FETs can cool off. To obviate unnecessary loading of the FETs, they are driven only when measurements are being carried out. This happens when $S_1$ is closed. When this switch is open, $IC_3$ is reset, so that there is no drive to the FETs. However, this does not mean that there is no voltage at their pins: a short-circuit between a drain and a source may still be disastrous.

Circuit $IC_3$ has more positions than the electronic switch in **Fig. 2**; there are also more of these switches. This is because, after testing, the gate of each FET must be linked briefly to the source to discharge the gate-source capacitance. This ensures that the FET switches off faster. During the ensuing pause, the oscilloscope gets ready for the next measurement. If the two switches at each gate are open, a 1 MΩ resistor connects the gate to the source, so that the FET is switched off.

The test circuits, $T_1$-$T_2$ and $T_4$-$T_5$, are powered by electrolytic capacitors $C_9$ and $C_{10}$. Since these capacitors are isolated from the regulated supply line by $R_{13}$, the test circuits can draw a current of up to 13 A from them, but the voltage regulator and transformer need not provide such a high current (the peak current through them is a few amperes). However, the average current is not more than 400 mA. Thus, the advantage of $R_{13}$ is that the power supply rating can be kept relatively low. A disadvantage is, however, that the supply voltage has quite a ripple. This is inconvenient, because in the case of n-channel FETs the drive voltage must be referred to the supply line, whereas in the case of p-channel FETs the gate voltage must be referred to ground. These slight problems are nullified by operational amplifiers.

The drive voltage for the n-channel test circuit is provided by $IC_{2a}$. It is unorthodox, but essential to keep the d.c. component on $C_8$ constant, to provide the inverted alternating output voltage with a different d.c. offset. Without this arrangement, the ripple on the voltage across $C_9$ and $C_{10}$ would cause the charging and discharge currents to distort the triangular drive voltage. This would lead to distorted characteristics on the oscilloscope.

In the p-channel test circuit, the gate voltage is converted from being referred to the supply line to being referred to ground. Here again, an operational amplifier, $IC_{9a}$, is used; this obtains its d.c. operating point from $C_9$ and $C_{10}$ via $R_{52}$ and $R_{53}$. Diode $D_5$ raises the operating point slightly to ensure that the amplifier works correctly in varying circumstances.

Several components, $T_3$, $R_{30}$, $R_{31}$ and $P_4$, have been added to the circuit around operational amplifier $IC_{9b}$ to provide the gate voltage of n-channel FETs with the same offset as that provided by $D_5$ in the

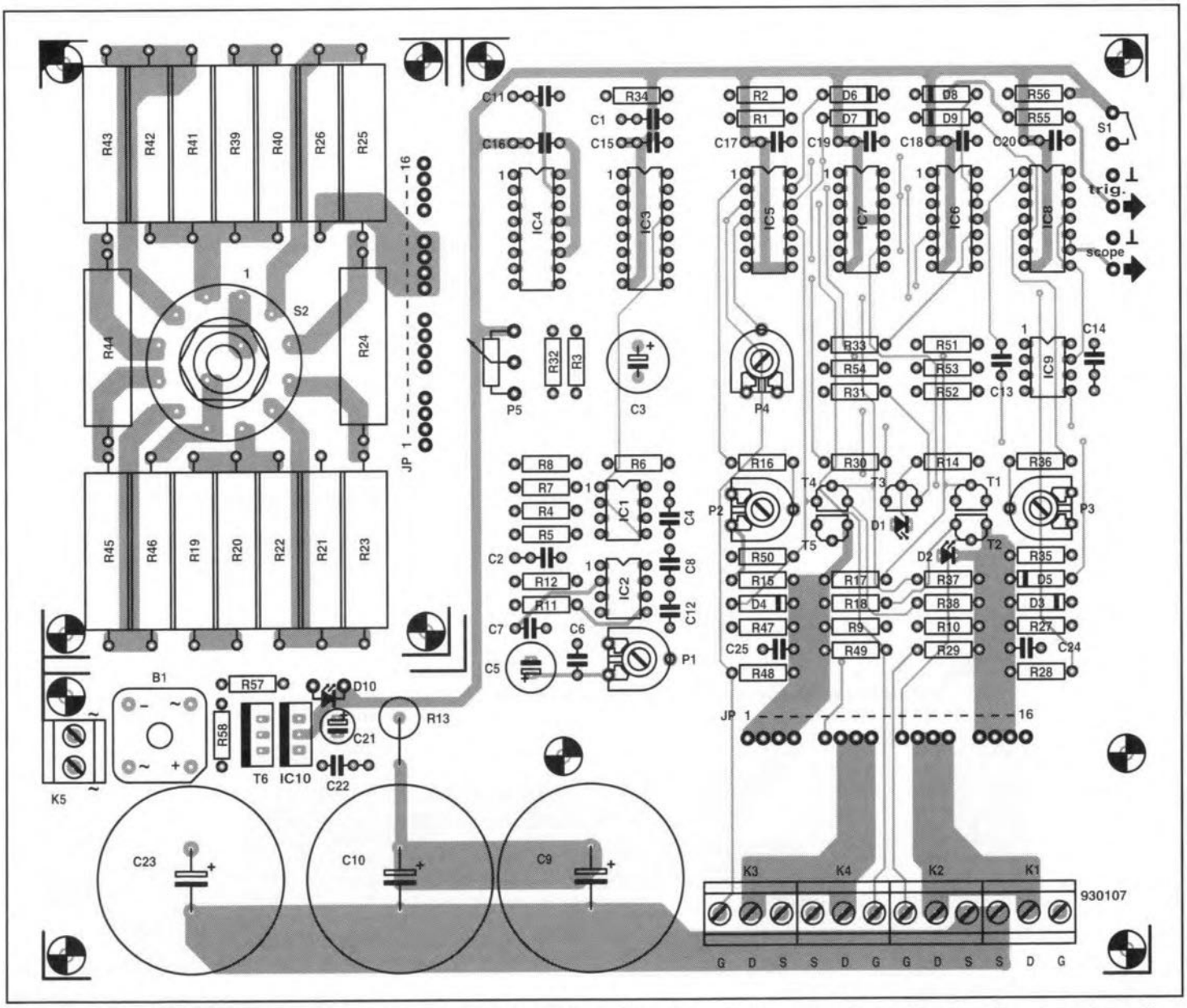



**Fig. 5. The double-sided, through-plated printed-circuit board for the power MOSFET tester (track side on next page).**

case of p-channel FETs. Preset $P_4$ is adjusted so that the outputs of $IC_{9a}$ and $IC_{9b}$ have identical offsets.

The drain current through the FETs is determined by the drain resistance and the drive voltage. The drain resistance is selected by switch $S_2$ from $R_{19}$–$R_{26}$ and $R_{39}$–$R_{46}$ as relevant.

The d.c. component of the drive voltage is derived from diodes $D_1$ and $D_2$.

The gate-source voltage is set to 1.5 V by $P_2$ and $P_3$, as the case may be.

Without the triangular voltage (that is, with the wiper of $P_1$ at the junction $C_5$-$C_6$), the following values of $I_D$ may be set with $S_2$: 10 A, 7 A, 4 A, 2 A, 1 A, and 500 mA. The position of S2 must not be altered while S1 is being pressed to avoid seriously reducing the life of that switch.

When the peak value of the triangular voltage is set to 0.5 V (with $P_1$), the drain current varies by ±33% with respect to the set operating point. It is possible to set $P_1$ to any value between 0 and that at which the circuit is saturated to make, respectively, only a small portion or a large part of the $U_{GS} - I_D$ characteristic visible on the oscilloscope.

The rating of the power supply is relatively low. Although the test circuits can draw a current of up to 13 A, the mains supply has ample time (90 ms or almost five mains periods) to recharge the capacitors from which that current is drawn. Nevertheless, the transformer can provide currents of up to 1.7 A, while the regulator has been enhanced by the addition of power transistor $T_6$.

Diode $D_{10}$ functions as on-off indicator.

Diodes $D_1$, $D_2$ and $D_{10}$ are low-current types. This is not essential in the case of $D_{10}$ but the other two must be, since they function as voltage references.

## Construction

The power MOSFET tester is intended to be built on the PCB illustrated in **Fig. 5**. The tracks of the test circuit that carry high currents are as short as possible and run, wherever feasible, on both sides of the board.

To keep the wiring of the drain resistors and $S_2$ short, these components are mounted on a small board which must be cut off the main board. This small board must be fitted at right angles to the main board just behind terminals $K_1$–$K_4$. The two boards are interconnected by a right-angle print header. The diameter of the header pins and the paralleling of several of these pins ensure that, even at currents of 13 A, the voltage drop across the connections is tiny. For mechanical robustness, the two boards should be fixed together with the aid of small angle pieces.

When the board is built into an enclosure, it is advisable to order the sequence of connecting the FETs. Owing to the short connections, connectors $K_1$–$K_4$ are not put in correct order on the board. This can be confusing when the oscilloscope is set to check whether a FET has been connected properly. On the oscilloscope, the curve at the extreme left is that of the signal at $K_1$; that at the extreme right results from the signal at $K_4$. Mistakes may be avoided by giving the connections on the enclosure the same position as the curves on the oscilloscope screen.

Short-circuits are avoided by the use

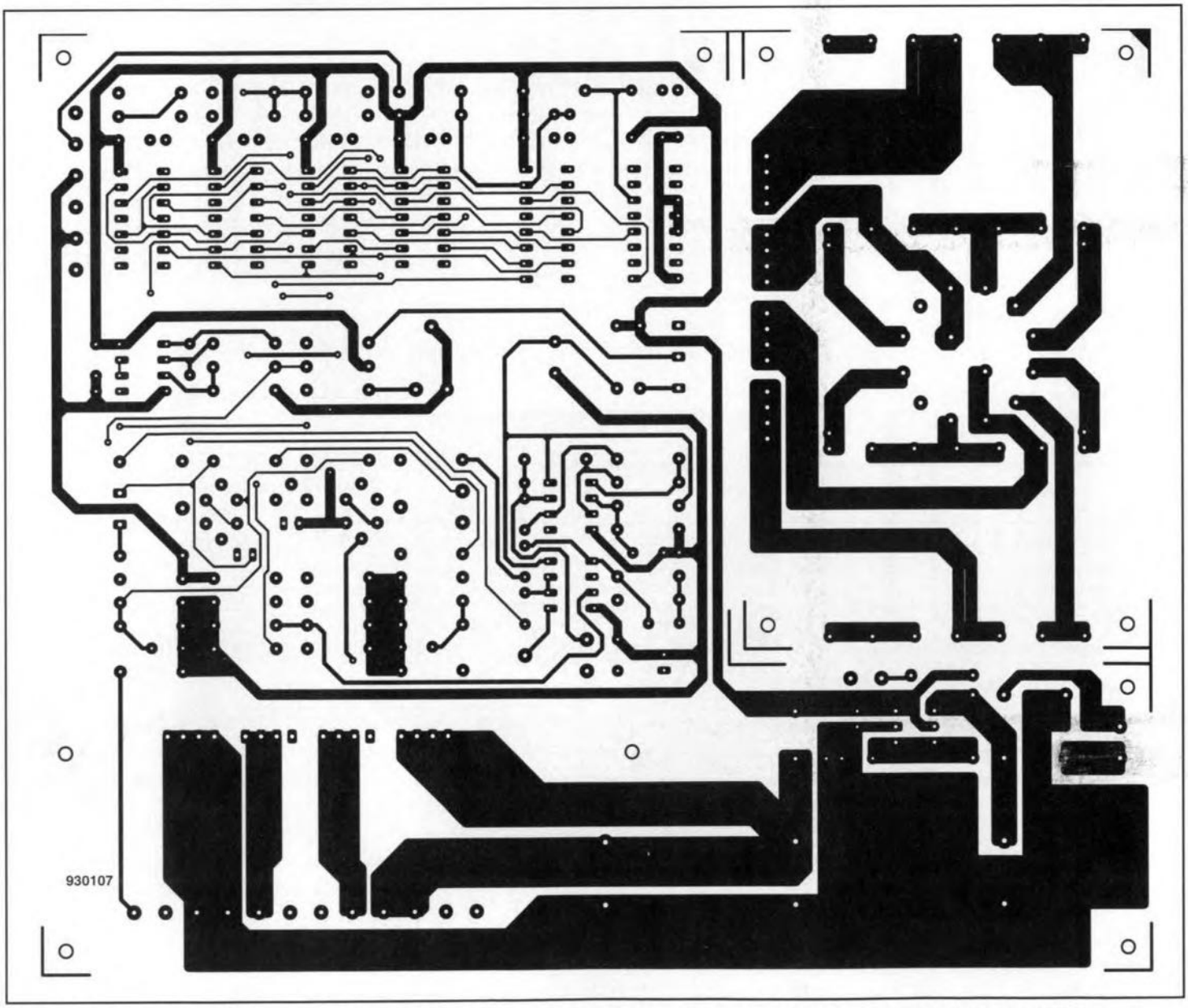



**Fig. 5b. Copper side of the printed-circuit board for the power MOSFET tester. Component layout on previous page.**

of well-insulated clips for attaching to the transistor pins. Further protection is obtained by inserting a fuse in each drain connection (fit the fuseholder on the front panel of the enclosure). Use a fast fuse rated at 0.5 A, although the current through the FETs may reach 13 A. That current flows for such a short time that even a fast fuse will not blow.

The electronics following the gate connection may be protected by inserting a 680 Ω resistor in the gate line.

Since, owing to the large currents, the circuit is sensitive to any voltage drop over the source line, it is advisable to run the connecting wires through the front panel of the enclosure and to connect them direct to to $K_1$–$K_4$. These wires should have a cross-sectional area of ≥2.5 mm².

## Calibration

Connect the wiper of $P_1$ to the junction $C_5$-$C_6$ and that of $P_5$ to ground. Close $S_1$, whereupon the signal at the TRIG output should look like that in **Fig. 3**. If the first pulse is shorter than the next, the period of the triangular-rectangular generator is not entirely in accord with the mono time of $IC_{4a}$. This results in an extra clock pulse in $IC_3$, which causes the first trigger pulse to be too short. In most cases this can be remedied by soldering a 1 MΩ resistor across $R_{34}$. If not, use 1 MΩ preset and turn this slightly past the position where the pulse has the correct width.

Connect the oscilloscope across $R_{17}$: DO NOT USE channel 2 or an external trigger input. Press $S_1$ and adjust $P_2$ until the peak value of the two pulses measured is 1.5 V.

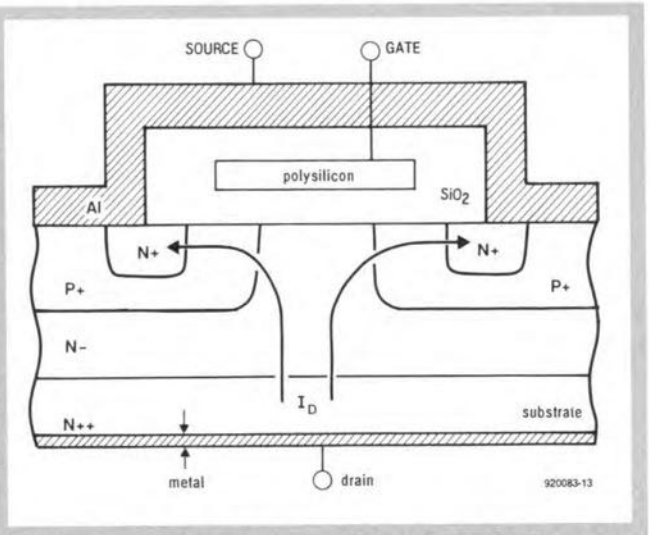
Connect the oscilloscope across $R_{37}$. Press $S_1$ and adjust $P_3$ until the peak value of the pulses measured is 1.5 V.

Connect the oscilloscope across the SCOPE output of the tester. Press $S_1$, whereupon four pulses are available (these look like the trigger signal). Adjust $P_4$ until the first two pulses are as high as the other two, or until the voltage across $R_{30}$ is equal to that across $D_5$.

Finally, adjust $P_1$ until the peak value of the triangular signal at its wiper is 1 $V_{pp}$.

### Power MOSFETs

It is typical of power MOSFETs that the drain current runs through the chip more or less vertically as shown in the diagram. In effect, this shows two paralleled FETs (a right-hand and a left-hand). For clarity's sake, only the area around the gat is shown, but the drawing should really be extended quite a bit to both sides. The drain and source terminals, situated in those imaginary extensions, are fairly stout so that the chip can draw fairly high currents.




If the chip consisted of perfectly doped silicon, the drain current, $I_D$, would split equally over the two FETs. But even with less perfect material, $I_D$ will divide fairly evenly. In the construction of power FETs, use is made of this property by paralleling not two, but hun dreds of small FETs. With the structure in the diagram, this is fairly simple: repeat the same structure and link it to the previous one, not only to the left and the right, but also in depth.

### PARTS LIST

**Resistors:**
$R_1$, $R_{28}$, $R_{29}$, $R_{48}$, $R_{49}$ = 1 MΩ
$R_2$ = 100 Ω
$R_3$ = 10 Ω
$R_4$–$R_6$, $R_{17}$, $R_{30}$, $R_{33}$, $R_{37}$ = 100 kΩ
$R_7$ = 330 kΩ
$R_8$ = 82 kΩ
$R_9$–$R_{12}$ = 10.0 kΩ, 1%
$R_{13}$ = 1 Ω, 5 W
$R_{14}$ = 1.5 kΩ
$R_{15}$, $R_{35}$ = 560 Ω
$R_{16}$, $R_{36}$, $R_{54}$ = 10 kΩ
$R_{18}$, $R_{38}$ = 330 Ω
$R_{19}$, $R_{39}$ = 0.27 Ω, 5 W
$R_{20}$, $R_{40}$ = 0.33 Ω, 5 W
$R_{21}$, $R_{22}$, $R_{41}$, $R_{42}$ = 0.12 Ω, 5 W
$R_{23}$, $R_{43}$ =0.15 Ω, 5 W
$R_{24}$, $R_{44}$ =0.39 Ω, 5 W
$R_{25}$, $R_{45}$ = 0.82 Ω, 5 W
$R_{26}$, $R_{46}$ = 1.5 Ω, 5 W
$R_{27}$, $R_{47}$ = 6.8 kΩ
$R_{31}$ = 560 kΩ
$R_{32}$, $R_{56}$ = 3.3 kΩ
$R_{34}$ = 270 kΩ
$R_{50}$–$R_{53}$ = 100 kΩ, 1%
$R_{55}$ = 5.6 kΩ
$R_{57}$ = 2.7 kΩ
$R_{58}$ = 3.3 Ω
$P_1$ = 10 kΩ preset potentiometer
$P_2$, $P_3$ = 1 kΩ preset potentiometer
$P_4$ = 250 kΩ preset potentiometer
$P_5$ = linear 5 kΩ potentiometer

**Capacitors:**
$C_1$, $C_2$, $C_{14}$–$C_{20}$ = 100 nF
$C_3$ = 220 µF, 16 V, radial
$C_4$ = 10 nF
$C_5$ = 100 µF, 16 V, radial
$C_6$, $C_8$, $C_{12}$ = 1 µF
$C_7$ = 33 pF
$C_9$, $C_{10}$, $C_{23}$ =4700 µF, 35 V, radial
$C_{11}$ = 330 nF
$C_{13}$ = 8.2 pF
$C_{21}$ = 22 µF, 40 V, radial
$C_{22}$ = 470 nF
$C_{24}$, $C_{25}$ = 150 pF

**Semiconductors:**
$D_1$, $D_2$, $D_{10}$ = 3 mm LED, red, low I
$D_3$, $D_4$ = zener diode 10 V, 400 mW
$D_5$ = BAT85
$D_6$–$D_9$ = 1N4148
$B_1$ = SB605 (600 V; 6 A)
$T_1$, $T_2$ = BC557B (pair)
$T_3$ = BC560C
$T_4$, $T_5$ = BC547B (pair)
$T_6$ = BD244C

**Integrated circuits:**
$IC_1$, $IC_2$, $IC_9$ = CA3260
$IC_3$ = 4017
$IC_4$ = 4538
$IC_5$–$IC_8$ = TLC4066
$IC_{10}$ = 7812

**Miscellaneous:**
$JP_1$–$JP_{16}$ = 4-way right-angle header
$K_1$–$K_4$ = 3-way terminal block 5 mm pitch
$K_5$ = 2-way terminal block, 5 mm pitch
$S_1$ = press-to-make push button switch
$S_2$ = 2-pole, 6-position, rotary switch for PCB mounting
PCB No. 930107 (see p. 70)

### Oscilloscope settings

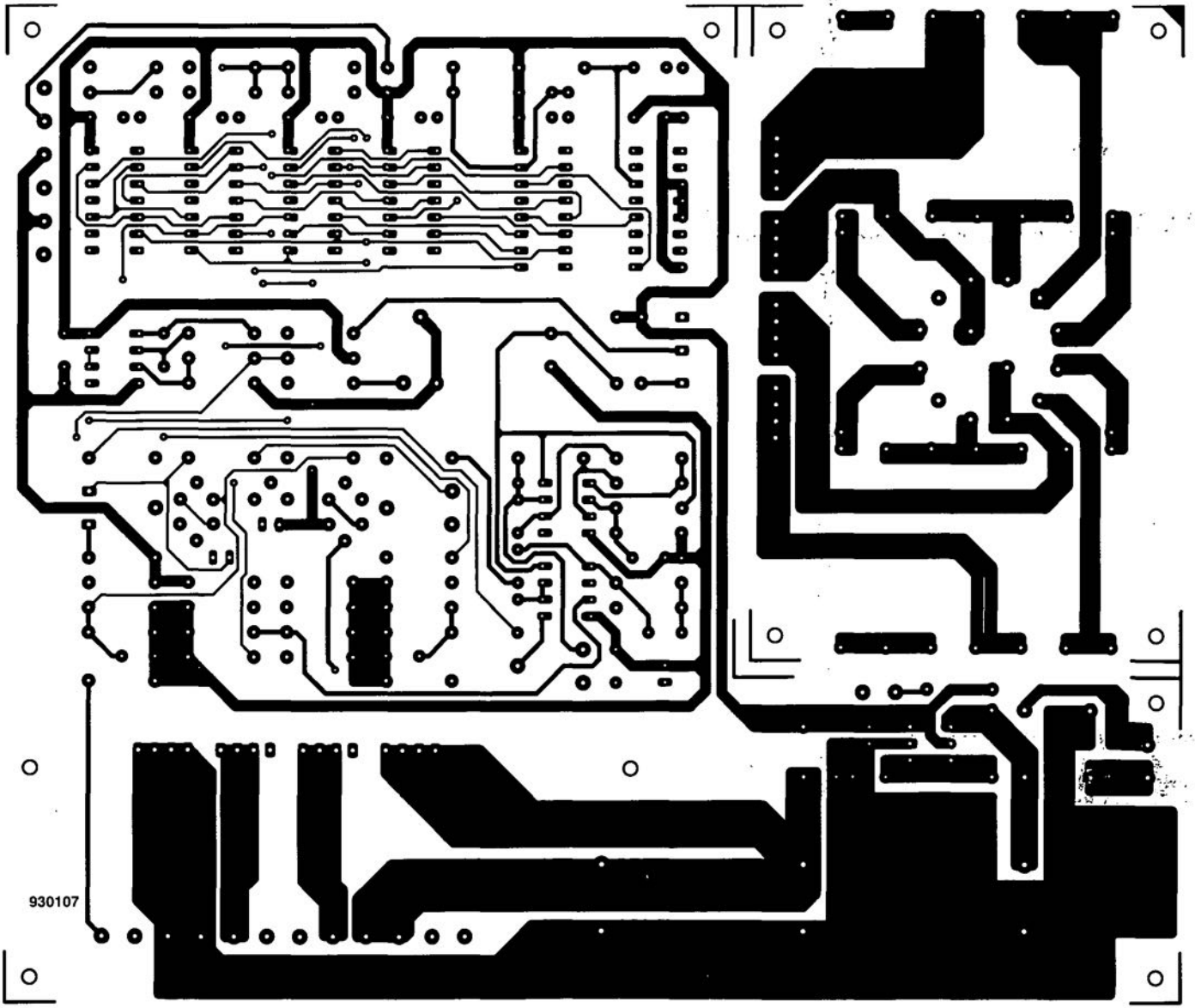
**Trigger:**
Extern
D.C.
Leading edge
Normal (NO auto trigger)

**Time base:**
Four consecutive measurements: 1 ms/div
Four simultaneous measurements: slightly more than 0.1 ms/div

***y*-channel:**
A.C.
No offset
Sensitivity as high as possible (depending on FET and chosen drain current).

**Power MOSFET tester:**
$S_1$: start measurement
$S_2$: $I_D$ 0–0.5–1–2–4–7–10 A
$P_5$: vertical position of characteristics on screen of oscilloscope (replaces offset setting of oscilloscope)

**END**


930107

# THE ANALOGUE SUBSYSTEM PART 3 (FINAL)

## BUILD A UNIVERSAL MULTI-GAIN ANALOGUE AMPLIFIER

**Amplifiers are used to boost weak electrical signals to higher levels. For example, a voltage amplifier will boost a weak voltage signal to a higher voltage level so that it can be displayed on a meter, viewed on a cathode ray oscilloscope (CRO), written on a paper chart recorder, or processed by an analogue-to-digital converter for input to a computer.**

**By Joseph J. Carr**

Although many experimenters will use their computers for data collection today, it is nonetheless true that it is still an 'analogue' world. Thus, one will still find a large number of applications for an analogue voltage amplifier. In this article you will find described a design idea for such an amplifier. This **universal multi-gain laboratory amplifier** (UMGLA) can be used for boosting the output signals from assorted sensors, biological signals, and a host of other signals found in scientific and electronic instrumentation.

But first, before looking at the amplifier, let us review some basic amplifier terminology so that everyone is on a level playing field. If you already know quite a bit about electronics, this material will be somewhat simplified. It will, however, serve as a good review, so you are invited to either read through it or skip ahead as you please.

Figure 20 shows the symbol for a basic amplifier. The symbol most commonly used is a triangle on its side. The input connections are along the vertical line on the left side, while the output connection is always at the opposite apex. Sometimes there are several inputs, but more of that shortly. Because both input signal voltage ($U_{in}$) and output signal voltage ($U_o$) are referred to the same common (sometimes called **ground** even when not connected to actual earth) connection, this type of amplifier is said to be **single-ended**; i.e., both input and output connections are single terminals. Another name for this particular amplifier configuration is **unbalanced**.

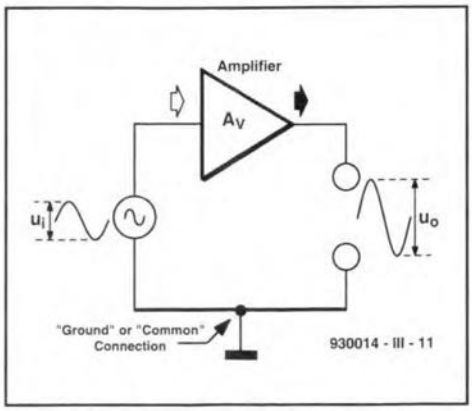



**Fig. 20. Basic amplifier symbol and connections.**

The **amplification** of an amplifier is a measure of how much it will boost the input signal. The symbol $A$ is usually used to represent amplification. Because the amplifier project in this article, and indeed the most commonly used type, is a **voltage amplifier**, the symbol is modified with a subscript v to denote voltage amplification: $A_v$. A current amplifier may have its amplification symbolized by $A_i$. There are other forms of amplification, but they are beyond the scope of this article. In all forms of amplifier, indeed in all forms of electronic circuit where there are inputs and outputs, the amplification is defined as the ratio of output to input. In the context of the voltage amplifier, therefore, the amplification is the ratio of the output voltage ($U_o$) and the input voltage ($U_{in}$) that produced it:

$$A_v = U_0 / U_{in} \qquad (1)$$

Consider a quick example. If a voltage amplifier produces a 1-volt output signal when a 2-millivolt (0.002 volt) input signal is impressed, the amplification is

$$(1\ V) / (0.002\ V) = 500.$$

The amplification term is dimensionless, and merely refers to the scaler by which the input signal is increased at the output.

The relationship between input voltage, output voltage and amplification is found from:

$$U_o = U_{in} A_v$$

Typical amplifications for amplifiers used in the laboratory are:

| CLASSIFICATION | VOLTAGE AMPLIFICATION |
|---|---|
| Low amplification | 10 to 50 |
| Medium amplification | 50 to 500 |
| High amplification | >500 |

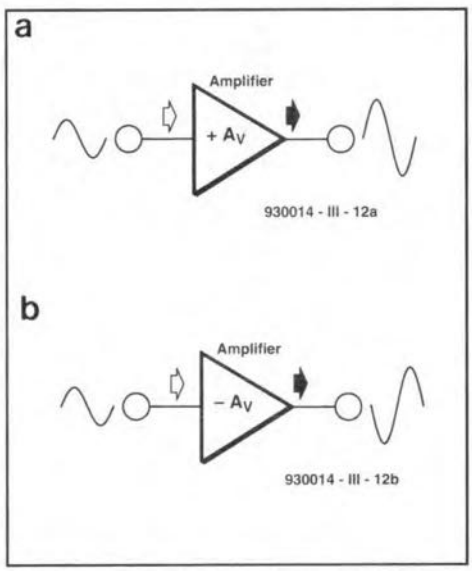



**Fig. 21. a) Non-inverting amplifier, b) inverting amplifier.**

Amplification can have either of two **polarities** (Fig. 21), which is seen by comparing the input and output signals. If a positive going input signal produces a positive going output signal (Fig. 21a), and vice versa, then the amplification is positive ($+A_v$). As you can see from the waveforms in Fig. 21a, the output signal is not inverted with respect to the input signal. Such an output signal is said to be **in phase** with the input signal, and the amplifier is said to be **non-inverting**. If the output signal is inverted with respect to the input signal (Fig. 21b), i.e., a positive going input signal produces a negative going output signal, the amplification is negative ($-A_v$) and the amplifier

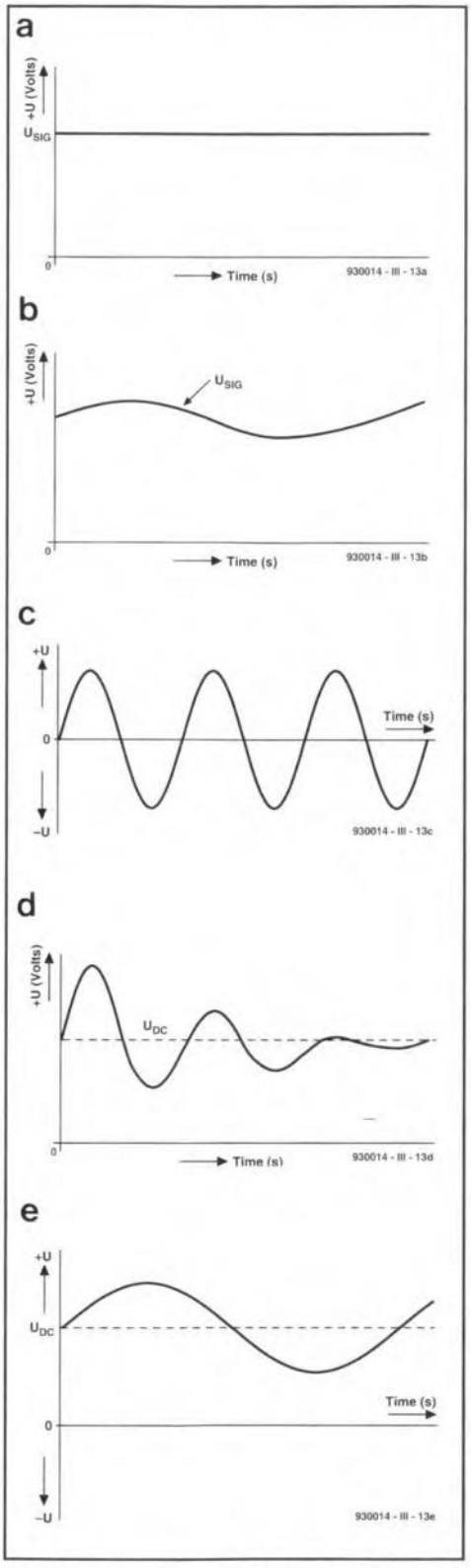



**Fig. 22. a) d.c. signal, b) quasi-static signal, c) periodic sine wave signal, d) varying d.c. signal, e) a.c. signal with d.c. component.**

is said to be **inverting**. The negative sign is used in math calculations of amplifiers, and indicates the phase reversal of the output with respect to the input signals.

The nature of the input signal is sometimes important to the design of the amplifier used to process it. For example, some signals are unchanging direct current voltages (Fig.22a), or very slowly varying voltages (Fig. 22b) that change only a small amount over a very long time. In other cases, the signal might be a **periodic** voltage such as a sine wave (Fig. 22c), square wave, triangle wave, sawtooth wave, pulse wave or other wave shape. Note in Fig. 22c that the signal is symmetrical around zero volts. One half of this bipolar signal is represented by positive voltage, while the other half of the signal is represented by negative voltage. One complete **cycle** consists of a single positive and single negative excursion, with an average value (taken together) of zero. An implication of this type of signal is that the amplifier that services it must be capable of operating over both negative and positive voltages, both at the input and at the output. Still other signals might be exponentially decaying peaks (Fig. 22d), either symmetrical about zero or all of one polarity (as shown).

Figures 22d and 22e illustrate one of the little problems found on real signals. Note that these signals are symmetrical around some line other than zero. If this line, representing a voltage, were depressed to zero, the sine wave signal of Fig. 22e would resemble Fig. 22c. This offset form of signal is said to have a **direct current** (d.c.) component. In other words, it can be thought of as a time-varying waveform (Fig. 22d) or periodic waveform (Fig. 22e) riding on a d.c. component, $U_{dc}$ .

In some cases, the d.c. component is a desired part of the overall signal, and therefore must be accommodated in any amplifier handling the signal. In other cases, the d.c. component is merely an offset on the desired signal, and should be suppressed. In some cases, the d.c. component is so severe that it is many times higher than the variations representing the desired signal. A good example is the **electrocardiograph** (ECG) signal. The ECG is a low value bipolar signal with a peak of about one millivolt (0.001 volt). When metallic electrodes (e.g. silver-silver chloride, Ag-AgCl) are attached to skin, which is electrolytic in nature, a tiny natural 'battery' is formed between the skin and electrode. This so-called **half-cell potential** can be as high as 2.5 V, although around 1 V is typical for the types of electrode normally used in ECG recording. In this, the desired 0.001-V ECG waveform is riding on top of a 1-V d.c. half-cell potential, so would be completely obscured.

The amplifier input circuit is sometimes modified in order to deal with various input signals. An amplifier input that is unmodified, that is, will recognize all components of the input signal including the d.c. offset component, is said to be **direct coupled** (d.c.). If an amplifier input circuit is modified to block the d.c. component and only passes the alternating current portion, it is said to be **a.c. coupled**. The a.c. coupled amplifier would pass the sine wave in Fig. 22e, but not the d.c. offset $U_{dc}$. The most usual

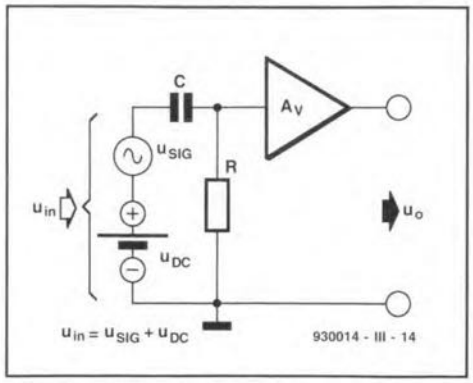



**Fig. 23. A.c.-coupling strips off the d.c. component.**

form of circuit for suppressing unwanted d.c. components is the **capacitor input** shown in Fig. 23. The signal voltage, $U_{in}$, is the algebraic sum of the actual signal ($U_{sig}$) and the d.c. offset ($U_{dc}$). In this type of circuit, the capacitor ($C$) is connected in series with the signal source voltages and the amplifier input terminal. In some amplifiers, there is also a resistor ($R$) connected between the amplifier input and ground. This resistor is used to prevent the capacitor from being erroneously charged by the d.c. offset voltage and spurious currents from the amplifier input (a fact of life in real amplifiers, unfortunately).

The type of amplifier in Fig. 20 is said to be single-ended because only one connection is made to the amplifier input and output sides; such amplifiers are unbalanced with respect to ground. In scientific and electronic instrumentation the single-ended amplifier may be either inappropriate (perhaps because the signals are not single-ended), or inadvisable (e.g., because of certain interferences). In such cases, a **balanced input** amplifier is needed. Such amplifiers are called **differential amplifiers** because they produce an output signal that is the product of the amplifier amplification and the **difference** between two input signals.

Figure 24 shows a typical differential amplifier. It has two inputs, labelled (–) and (+). The negative input is an inverting input (–IN), while the positive input is a non-inverting input (+IN). Both inputs provide the same amount of voltage

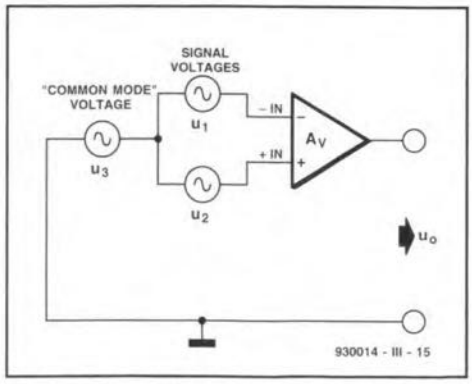



**Fig. 24. D.c. differential amplifier with input signals.**

amplification, but of opposite polarity. Thus, if the exact same voltage, with exact same polarity, is applied to both –IN and +IN, then the resultant output is zero. In the circuit shown in Fig. 24, the output voltage is the difference between the two input voltages, $U_1$ and $U_2$:

$$U_0 = U_d(U_2 - U_1)$$

Where $U_d$ is the **differential voltage amplification**, and $U_1$ and $U_2$ are single-ended input voltages.

If a voltage signal is applied equally to both inputs ($U_3$ in Fig. 24), it is called a **common mode voltage**. This voltage tends to be suppressed because of the reciprocal action of the two inputs. The suppression is not complete, but is very good (100,000:1 and 1,000,000:1 are common). The ratio of the differential amplification to the common mode amplification is a measure of this suppression, and is called the **common mode rejection ratio** (CMRR).

Real amplifiers are not ideal, although with modern integrated circuit amplifiers the departures from 'idealness' are very small. Although a complete discussion of practical amplifiers is beyond the scope of this article, there are at least two aspects that must be considered: **output resistance** ($R_o$) and **input resistance** ($R_{in}$) — these are sometimes called 'impedances' rather than resistances, so read **output impedance** ($Z_o$) and **input impedance** ($Z_{in}$). Figure 25

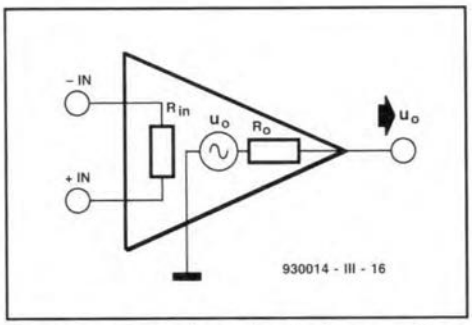



**Fig. 25. Equivalent circuit for a voltage amplifier.**

shows these resistances modelled as discrete resistors in the output and input circuits. In order to faithfully reproduce signals, the amplifier needs to be designed to maximize input resistance, and minimize output resistance. Ideally, $R_{in} \rightarrow \infty$ and $R_o \rightarrow 0$. In real amplifiers, the input resistance will be $10^6$ Ω up to $10^{12}$ Ω depending on design and quality, and output resistance will be 1 to 100 Ω, with 25 Ω being quite common.

## What kind of amplifier for the laboratory?

The amplifier for the laboratory needs to have certain characteristics. Although a discussion of 'why?' for some of the selected parameters can be a bit involved, there are some guidelines. For example, for maximum diversity, a lab amplifier should be a differential input type. In cases where single ended amplifiers are needed, it is only necessary to ground the unwanted input. For example, to make an inverting single-ended amplifier, simply ground the non-inverting input and use the inverting input. Similarly, to make a non-inverting amplifier all you need to do is ground the inverting input. Thus, the differential amplifier will serve as a differential amplifier, an inverting amplifier and a non-inverting amplifier. The laboratory amplifier should also have a single-ended output so that it is compatible with the usual types of display and recording devices (meters, oscilloscopes, paper recorders, A-D converters, etc), in order to process a wide variety of signals, but a.c. coupled and d.c. coupled inputs should be available.

## A laboratory amplifier design

The circuit for the UMGLA is shown in Fig. 26. The heart of this circuit is the Burr-Brown INA-110 integrated circuit instrumentation amplifier (IC1). This device is designed for a wide variety of instrumentation applications, of which the laboratory amplifier is a good representative example. It has a very high impedance, differential input stage, and a single-ended output. It uses a minimum of components, and the amplification is programmable. The INA-110 comes in a 16-pin integrated circuit dual in line package (DIP).

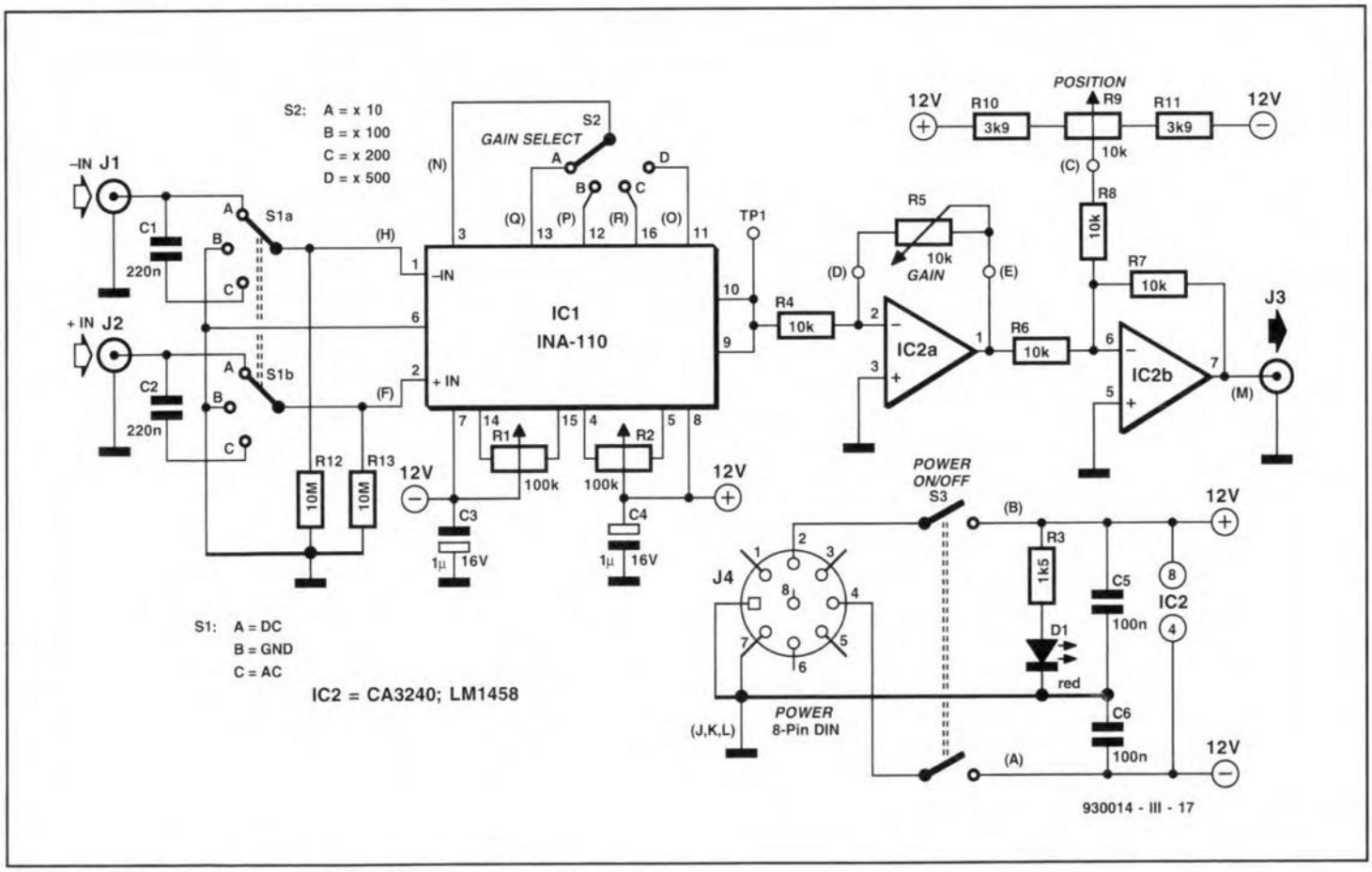



**Fig. 26. Circuit diagram of the lab amplifier.**

**Table 1**

| Voltage gain $A_v$ | connect together pins |
|---|---|
| ×10 | 3, 13 |
| ×100 | 3, 12 |
| ×200 | 3, 16 |
| ×500 | 3, 11 |

The INA-110 provides an amplification of ×10, ×100, ×200 or ×500, depending on the programming performed on pins 3, 11, 12, 13, and 16, according to the scheme in Table 1. To obtain any of the four specified voltage gains you only need to short together pin 3 and the indicated pin that corresponds to the desired gain. In Fig. 26, the gain is selected by a single-pole, four-position (SP4P) switch. The pole of the switch is connected to pin 3 of the INA-110, while the programming pins are connected to the four selectable positions (labelled A, B, C and D in Fig. 26).

The input pins of the INA-110 are pin 1 (–IN) and pin 2 (+IN). A two-pole, three-position (2P3P) input switch is used to either ground these inputs, connect them directly to the input connectors (J1/J2), or provide a.c. coupling by passing the signal through a pair of 0.22-µF capacitors ($C_1$ and $C_2$). A pair of matched 10-MΩ resistors ($R_{12}$ and $R_{13}$) are connected between the inputs of the INA-110 and ground. These resistors should be matched to exhibit the same resistance from a collection of 10 MΩ, 5% tolerance ¼ watt, metal film resistors. Alternatively, if you have them available, use a pair of 1% (or better) precision resistors and skip the matching task.

The second stage in the circuit of Fig. 26 is a post amplifier made with a dual operational amplifier (IC2). These devices contain two operational amplifiers (IC2A and IC2B) inside a single 8-pin DIP package. Use either the low-cost LM1458 device, or the somewhat pricier (but still reasonable), CA3240.

The first stage of the post amplifier, IC2A, is connected as an inverting amplifier with a gain that is adjustable from zero to one. The gain in these circuits is the ratio of the feedback resistor to the input resistor, or in the case of IC2A the ratio $R_5/R_4$. Resistor $R_4$ is a 10-kΩ fixed resistor, while $R_5$ is a 10-kΩ potentiometer. Thus, the voltage gain of IC2A is zero when $R_5$ is set to minimum (zero ohms), and the gain is one when R5 is set to maximum (10 kΩ).

The second stage serves to provide a **position** control ($R_9$), as well as serving as an output 'buffer' to isolate the amplifier from the outside world. The gain of IC2B is one ($R_7/R_6$), and is fixed. The output of IC2B is routed to the output connector, J3.

The position control ($R_9$) is connected as a d.c. offset control to IC2B. It provides a voltage that is seen at the output as a d.c. offset to the output baseline. When the voltage at the wiper of $R_9$ (point 'C') is zero, the output offset voltage of the amplifier is zero. When the signal is viewed on an oscilloscope or paper chart recorder, the effect of $R_9$ is to set the position of the 'zero' baseline of the combined signal + offset. Potentiometers $R_4$ and $R_5$ are mounted on the front panel of the amplifier so that they can be adjusted by the user.

The power supply for this amplifier is derived from outside of the circuit. A power connector (J4), which in this case is an 8-pin DIN audio-style connector, is provided. The required voltages are ±12 V. These voltages can be supplied either from an a.c. powered electronic power supply, or from a set of batteries.

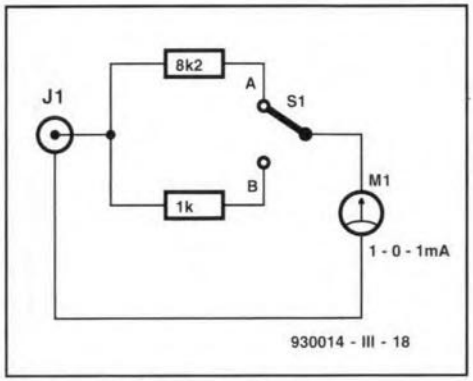



**Fig. 27. Output display circuit.**

A power switch (S3 in Fig. 26) turns the amplifier on and off. The switch can be any single pole-single throw (SPST), panel mounted, toggle switch, but it is more likely that you will, like I did, find it easier to obtain a double pole-double throw (DPDT) switch. Either can be used (ignore the extra connections on the DPDT version).

The output of the laboratory amplifier can be monitored on an oscilloscope, strip-chart paper recorder, analogue-to-digital converter (for input to a computer), or an analogue meter. If you prefer, a digital multimeter can be used to indicate output voltage values in static cases (e.g. the output of some sensors). Alternatively, use an analogue meter (Fig. 27). A single pole double throw (SPDT) switch is connected to a 1-0-1 milliampère, zero-centre, analogue meter. The other terminals of the switch are connected to a pair of resistors that determine the sensitivity, making this a two-range instrument. Analogue meters, incidentally, are best for nulling type measurements, as in when a Wheatstone bridge is used to measure certain scientific parameters. ■

# DX TELEVISION

930135

**A two-monthly column by Keith Hamer and Garry Smith**

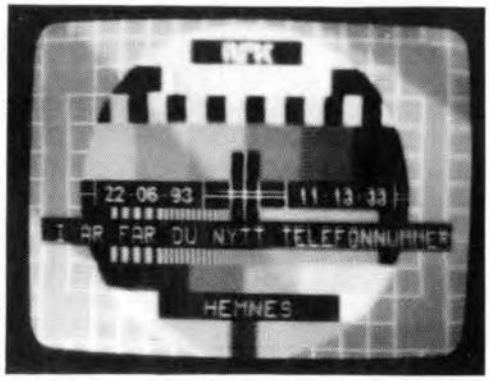



**Fig. 1. The new Norwegian test pattern with date and stylized 'NRK' at the top. The test pattern was received by Bob Brooks (South Wirral) on channel E3 from the Hemnes transmitter.**

JUNE and July 1993 proved to be an action-packed period for sporadic-E reception between 48 and 70 MHz. There were many days of intense all-day activity, with countries in the South and South-East of Europe received virtually daily in some parts of the UK. Many of the openings were already in progress before 0600 UTC, and with many countries screening a breakfast TV programme, very early monitoring was essential if you wanted to see test cards. Compared with previous seasons, 'exotics' were less evident. Nevertheless, there were reports of transatlantic DX on channel E2, and the Middle East (Jordan) on June 9th.

## Test card changes

**Norway:** Stephen Michie (Bristol) advises that the Norwegian PM5534 test card (with the date, time, transmitter identification and PTT message) is shown only before 1015 UTC. Just before this time, the transmitter name disappears, and the PM5534 switches to text pages with programme schedules. The schedules are also shown after closedown.

**Austria:** Stephen Michie has also commented that ORF-1 shows text pages before the station opens at 0700 UTC. There has been no sign of the PM5544 test card so far this season.

**Slovenia:** TV Slovenia shows mainly text pages during the day. The PM5544 test card is very rarely shown after 0600 UTC.

**Spain:** Tony Mancini (Belper) has identified TVE-1 Spain relaying 'Euro TV' news. The 'Euro TV' logo is shown in the corner of the screen, which is causing confusion among some DX-ers.

## Mystery signals

Readers have written in with several 'mystery' signals which they would like identifying. If you can help, please write to the address given at the end of this article.

1. Adverts introduced by the letters 'EPP' have been seen on channel E3. This abbreviation has been used to introduce advertisements for many years in former Yugoslavia.
2. The identification PTC-G1 (or PTC-61) appears to come from TVB-1 (Beograd). 'PTC' is the abbreviation for 'Radio Television Serbia' in Cyrillic.
3. Several sightings of a '2' corner logo on channel E3.
4. Various colour bars, line sawtooth and chessboard test patterns have been seen on channel R2.
5. 'NTA' corner logo on channel E3.
6. There is a mystery surrounding the possibility of a second Portuguese station operating on channel E2 when a second station was received in Europe early in the season. The only one known to be currently operating is Muro with an ERP of 40 kW.

Recently the RTP FuBK test pattern was noted in Derby, around mid-morning, superimposed in the background of a strong Spanish TVE-1 transmission. Although difficult to read, there seemed to be a '2' after the 'LISB' part of the identification. Since then, Chris Howles (Erdington) has returned from the Algarve in Portugal, and confirms that the RTP-2 FuBK is shown during the morning, while the 1st Network is on programmes. The local RTP-2 transmissions in the Algarve were on channel E5. Normally, the second network is confined to UHF. On June 8th, a transmitter announcement caption was shown by RTP at 1830 UTC with mention of various channels, but unfortunately it seemed insignificant at the time.

## Reception reports

Ian Johnson (Bromsgrove) reports an 'exciting' sporadic-E season for TV and 6-metre reception. The highlights include a 6-metre transatlantic opening to Virginia, North America, at 1827 UTC on June 11th, when he contacted station W4DR using 35 W (100 W ERP) into FM17. K1TO1 and WA1OUB were also heard. The 6-metre band also opened up to Maine, North America, very briefly at 1920 UTC on June 25th.

David Glenday (Arbroath) recalls 11 days of tropospheric reception during the first half of June. Conditions subsequently remained flat until the 28th. A 'first' was NRK TV2 on channel E37 with the 'TV Norge' PM5534 test card seen around 0000 UTC on the 29th/30th June. The signal is thought to have originated from a 1-kW outlet in Stavanger on the west coast of Norway.

Sporadic-E reception during the period brought in lots of Spanish stations. On June 21st, strong signals from Russia were received in colour. The signals were clean enough to decode Teletext; the Russian 1st programme has a page header called 'TELEINF'. David feels that the Moscow services have become too commercialized. There is an endless stream of adverts for Schweppes, Twix, various brands of shampoo, Kodak film, Sony electronic goods, Hewlett-Packard computers and even Cadbury's Fruit 'n' Nut chocolate!

Peter Chalkley (Luton) received Albania for the first time from the 100-kW Tirana transmitter on channel IC at 82.25 MHz. This reception confirms that the transmitter is still operating on this channel even though it is no longer listed in the *EBU Station Listings*. The 1993 edition lists many Band-I relays which have recently been commissioned, but unfortunately these are only low-power, so only time will tell whether these can be received in the UK. The Tirana transmitter has 'officially' moved to UHF.

Peter has also monitored the FM radio band during intense openings. He has noted several Spanish and Portuguese stations.

Barry Bowman (Manchester) has also taken advantage of the high m.u.f's, and DX-ed at FM. Catches on July 28th included Spain (Cadena FM) at 88.15 MHz, the Canary Islands (Onda Zero Musica) at 87.70 MHz, Portugal (various stations from 106.00 to 106.90 MHz) and Morocco at 87.55 MHz. Other openings produced Italian and Croatian FM stations.

Chris Howles (Erdington) has commented that RTE-1 signals from Eire on channel B (Gort) were in evidence several times during his recent two-weeks' holiday in Portugal. Other sporadic-E signals included Spain, Belgium, the Netherlands, Germany, Tunisia and Morocco. The latter signal originated from the Layounne transmitter (channel E4), which is located almost opposite the Canary Islands. TVE-1 trans-

missions on channel E3 were present at the time, possibly from the Izaña transmitter on Tenerife. Various Moroccan Band-III stations were present all the time in the Algarve, despite the distance of more than 200 km. Chris has commented that the Moroccan second network at UHF is encrypted.

## Log for June

Sporadic-E activity was evident every day except June 2nd and 6th. The most intense and prolonged openings are detailed below.

**09.06.93:** Finland on channel E4; Portugal E2 and E3, Spain E2, E3 and E4; Hungary R1; Unidentified signals from the CIS on R1, R2, R3 and R4; Italy IA and IB; Serbia E3; Croatia E4; Iceland E3 and E4; unidentified transatlantic signal on A2; Jordan E3; Germany E3; Albania IC; Corsica L2.

**10.06.93:** Czech Republic on R1; Italy IA and IB; Norway E2 and E3; Sweden E2, E3 and E4 (test card and programmes); Portugal E3; Spain E2, E3 and E4; Denmark E3; Albania IC; Switzerland E2 and E3; Austria E2a; Croatia E4; Hungary R1 and R4.

**11.06.93:** Unidentified transmissions from the CIS on R2; Germany E2; Italy IA, IB and IC; Moldova R2 and R3; Rumania R2 and R3; Estonia R2; Denmark E3; Croatia E4; Slovakia R2; Czech Republic R1; Sweden E2; E3 and E4; Austria E2a; Spain E2; Slovenia E3.

**12.06.93** Czech Republic on R1 and R2; Slovenia E3; Hungary R1 and R2; Rumania E3; Austria E4; Germany E2, E3 and E4; Switzerland E2 and E3; Italy IA and IB; unidentified CIS on R1 and R2; Spain E2, E3 and E4; Norway E2, E3 and E4; Poland R2; Ukraine R1.

## Log for July

Long-distance reception occurred daily except for July 3rd and 4th. The highlights were as follows:

**08.07.93:** Slovenia E3; Serbia E3; Croatia E4; Denmark E3 and E4; Sweden E2, E3 and E4; Finland E3 and E4; Norway E2, E3 (Hemnes) and E4 (Kongsberg); Italy IA and IB; Corsica L2 and L3; Czech Republic R2; Rumania R3; Albania IC; Iceland E4; Germany E2, E3 and E4; Switzerland E2; Hungary R2; Poland R2 and R3; Estonia R2; Austria E2a and E4; Spain E2 and E3; unidentified CIS R1; R2, R3 and R4.

**16.07.93:** Spain E2, E3 and E4; Italy IA and IB; Corsica L2; Czech Republic R1; Germany E2; Hungary R1, R2 and R4; Rumania R3; Austria E2a and E4; Slovenia E3; Serbia E3; Croatia E4; Denmark E3 and E4; Poland R3; Estonia R4; Moldova R1 and R3; Albania IC.

**Fig. 2. Rumanian 1st network logo received on channel R2 by Bob Brooks.**

Reception reports and logs kindly supplied by Barry Bowman, Simon Hamer, Peter Chalkley, Bob Brooks, Stephen Michie, Ian Johnson and David Glenday.

## Service information

**Germany:** The FuBK currently used by the ARD now carries the identification 'ARD1 - FFTM' with a digital clock in the lower part of the test pattern. A continuous announcement advises the viewer of which network they are watching. Regional variations (for example NDR-1) now appear only infrequently. MDR-3 have virtually abandoned the FuBK, which has been replaced by a full-screen caption advertising the *MDR Sputnik* radio channel.

Before the start of the breakfast magazine programme, ARD and ZDF show a 'live' picture of either Cologne (ARD) or Berlin (ZDF) with the latest news headlines running across the bottom of the screen. The main part of the screen usually features a 'Guten Morgen aus Köln' or 'Guten Morgen aus Berlin' message.

Bayern-3 are filling spare time before their programmes start by screening 'weather panoramas', i.e., pictures from various locations in Bavaria, giving detailed local weather information.

SFB in Berlin is filling the spare time between closedown and the start of programmes by giving viewers an unedited train driver's view of some of Berlin's urban railway routes. Up to 20% of viewers remain tuned in to the railway show!

West-3 is now on Astra 1C via transponder 39. BRF-3 (Bavaria) is on transponder 45. Since August 27th, MDR-3, SWF-3 and ZDF have been broadcasting via Astra; ARD-1 will eventually replace Eins Plus on transponder 19. S-3 in Baden-Württemberg is also considering such a move.

**Moldova:** The new channel R3 transmitter located at Straseni is 50 kW TRP providing an ERP of 800 kW!

**Netherlands:** Various channels have been assigned for regional public broadcasting with ERPs ranging from 1 kW to 1,000 kW.

**Russia:** The Finnish television company Oy Mainostelevisio Ab (MTV) has bought a minority share of the commercially-owned TV company called Regional Television (RTV), which is operating in St. Petersburg. RTV started transmissions in the St. Petersburg area in June, and broadcasts Monday to Friday from 1800-2300 local time.

Moscow on channel R3 has its own local Teletext service called 'MOSTEXT'. TELEINF via the OK-1 network has extended its pages, but still does not show the correct date — only a flashing day in Italian!

**Lithuania:** The low-power channel R11 transmitter in Vilnius is back on the air, relaying the German SAT-1 channel. TV26 (on channel R26 in Vilnius) is no longer operational.

Rytu R28 (Lietuvos TV, which was originally a state-owned enterprise) has been re-opened by the private TV company Baltijos Televizija. Their own programmes are screened several times per week, but at other times the transmitter relays TP-1 programmes from Poland as before.

The former CT-1 network has resumed a full-time relay of OK-1 from Moscow. The LTV-2 programmes from Kaunas, which used to share this channel, have ceased.

The former CT-2 network now carries a selection of satellite material from various sources, including Super Channel, Discovery and Pro-7, plus selected relays of Russian TV (TKR) such as the Vesti news and programmes of the new private TV company TELE-3. The government is opposed to the new private company and wants to close it down.

**Australia:** Channels in the upper part of Band III are to be moved up by 1 MHz to bring them in line with CCIR 'E' frequencies, as used in Europe. This will also allow the introduction of two new Australian allocations — channels 9a and 12 at 203.25 MHz and 224.25 MHz respectively.

This month's Service Information was kindly supplied by Gösta van der Linden and the BDXC, Netherlands; Reflexion Club, Germany; Pertti Salonen, Finland; Roger Bunney, UK; Thomas Pahlke, Germany; Bernd Trutenau, Lithuania, Lt. Col. Rana Roy, India.

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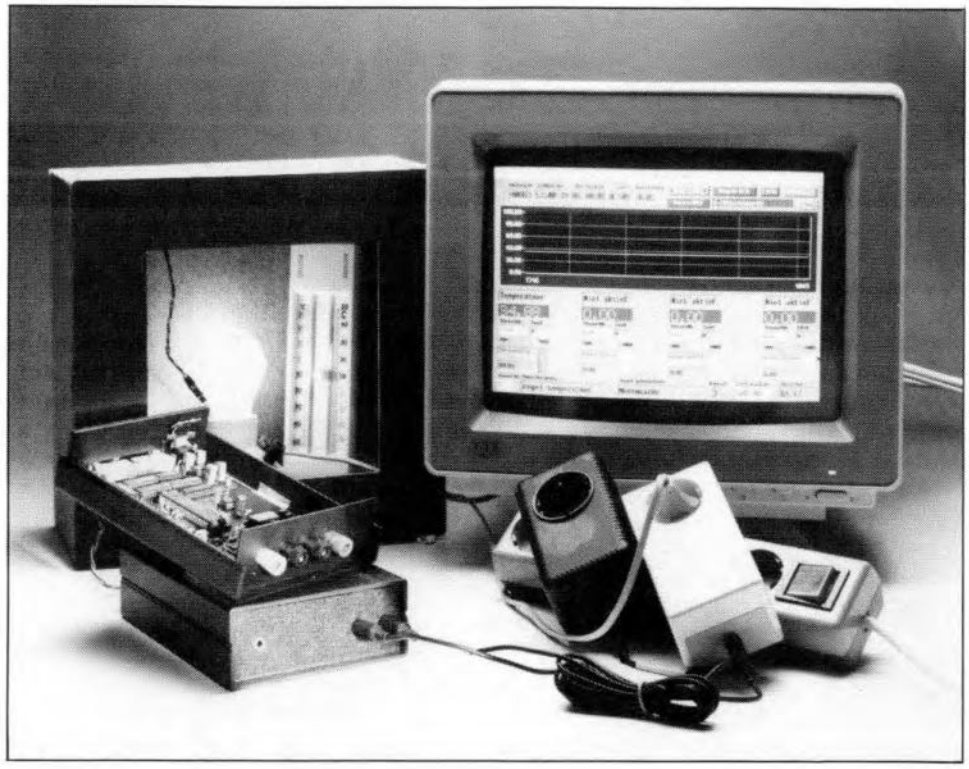
Please send any news about DX-TV in your part of the world to: Keith Hamer, 7 Epping Close, Derby DE3 4HR, England.

# FUZZY LOGIC MULTIMETER (PART 3 — FINAL)

**Fuzzy logic is not fuzzy at all, but a scientifically based way of getting electrical equipment to adapt to us, humans, instead of the other way around. This article introduces the Fuzzy Control One software package for PCs and compatibles, and in addition gives you hands-on experience in using this software by describing an intelligent heating system based on the PC DMM card discussed in the previous two instalments.**



**Design by H. Scholten**

The core of the hardware required for the experimental fuzzy logic control system described here is the 'Fuzzy logic DMM' described in the previous two instalments of this article. To be able to control a mains-operated load, the DMM needs to be complemented with a proportional phase angle control circuit, which is described here. You also need the Fuzzy Control One software, in particular, the digital multimeter software, which already contains a number of control routines specially written for the present example. Strictly speaking, the DMM hardware and the associated software are sufficient to set up an elementary control system. This is because the software contains a driver that makes use of the digital outputs on the multimeter board.

We decided to offer you something a little more elaborate than a control system based on a simple 8-bit parallel output. The fuzzy logic application example described here comprises phase angle control of the mains voltage, i.e., a regulation system that enables the power fed to mains-operated loads such as motors, heating elements and lamps, to be accurately adjusted. Just for the purpose of demonstration, a control system is made that keeps the temperature in a cardboard box constant at a certain value. An ordinary 75-watt bulb is used as the heating element. Admittedly, such a temperature control can be built with much simpler means, but the lamp in the box is just as good an example as the more esoteric (and often spectacular) applications conceived to demonstrate the power of fuzzy logic. A fuzzy logic 'starter' can not be simple enough, and should concentrate on setting up a limited, yet intelligent, control system. Once the basics of fuzzy logic have been mastered, you are, of course, free to make your own applications as complex as you desire. How? By writing your own system control specifications!

## Computer-driven phase angle control

Proportional phase angle control is the most commonly used method of controlling the amount of power fed to a mains-operated device. The best known application of phase angle control is probably the ubiquitous dimmer.

The block diagram of the computer-controlled 'dimmer' is given in **Fig. 9**. The heart of the circuit is a Type 8253 programmable interval timer (PIT). Apart from a computer interface, this IC from Intel contains three counters, which are programmed to function as monostable multivibrators (MMVs) in the present application. The length (duration) of the pulses supplied by the MMVs is determined by the computer. These pulses are synchronized to the mains frequency with the aid of a zero crossing detector.

Apart from the computer, a clock generator also determines the length of the counter output pulses. The clock frequency is 102,400 Hz, which means that there are 1,024 clock pulses to cover each half period of the mains voltage (assuming a mains frequency of 50 Hz). Essentially, the task of the computer is limited to telling the counters the length of the output pulses expressed in clock pulses. In other words, each half cycle of the mains can be divided into 1,024 phases, giving a resolution of $180°/1{,}024=0.176°$.

Before looking at the timing diagram to discover how the various signals are combined in the first two AND

gates, we first discuss the function of the three counters in the PIT. Counter 1 and counter 2 determine the phase angle at which the triac switches on the mains voltage for output 1 and output 2, respectively. Counter 0 serves to determine the phase angle after which the triac is no longer supplied with firing pulses. This is particularly useful when controlling inductive loads, since it prevents the triac being triggered again after the zero crossing of the current (when the triac is switched off).

The timing diagram inset in **Fig. 9** illustrates the operation of the PIT counters involved in the control of output 1 (counter 0 and counter 1). The counters are triggered on the zero crossing of the mains voltage, when their outputs go low. Since the output of counter 0 is inverted before it arrives at the AND gate, it enables the gate, and so indicates that the time available for triggering the triac is not over yet. However, counter 1 does not enable the AND gate yet, since the instant at which the triac is to be fired, is not reached yet. As soon as the output of counter 1 goes high, the AND gate is enabled, and clock pulses are allowed to reach the triac. The use of a pulse train to fire the triac has two advantages. First, it ensures reliable triggering (should the first pulse fail to fire the triac, there is always a second, a third, etc.); and, second, the gate is not constantly driven, which reduces the amount of power it has to dissipate.

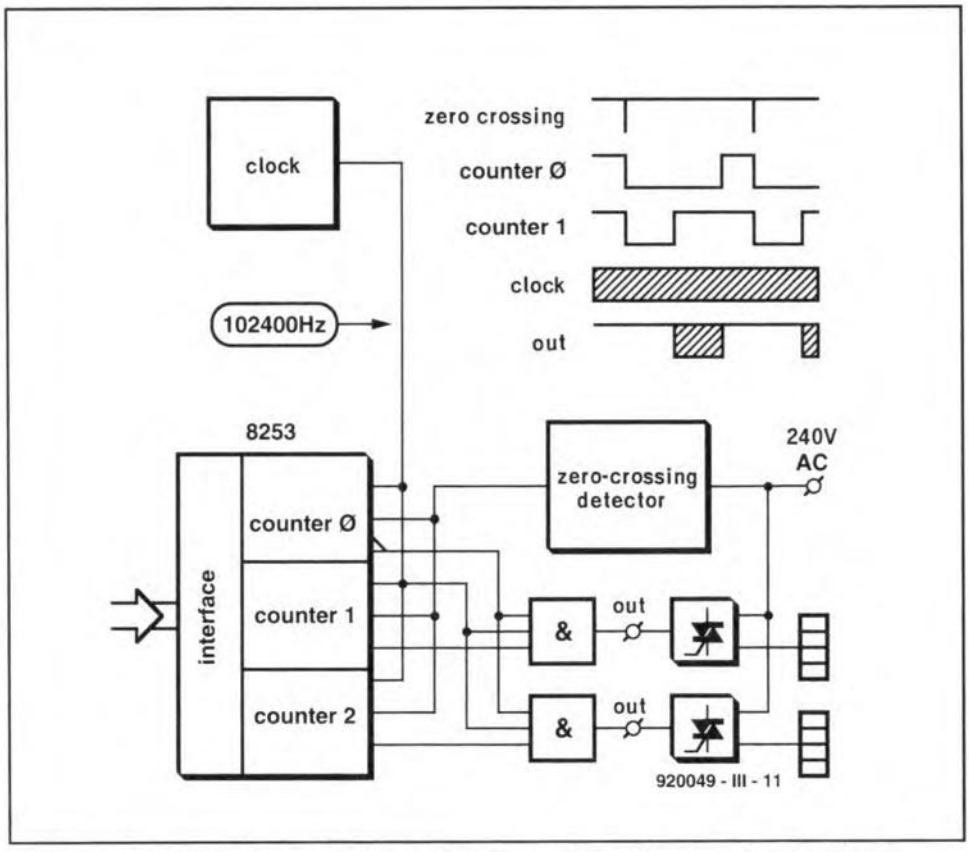



Fig. 9. Block diagram of the experimental heating control system based on fuzzy logic.

## Four pieces

The circuit diagram, **Fig. 10**, is subdivided into four sections, which correspond to the four printed circuit boards that make up the complete control system. Considering the total number of components, some of you may find the use of four boards extravagant. Note, however, that the (sub) circuits form part of the 'MicroSystem' developed by the author (see Part 2), and have to be relocatable because of the system's modular structure.

The **PIT board** contains relatively few components. The main circuit, IC1, contains the interface and the counters shown in the block diagram in **Fig. 9**. Circuits IC2 and IC3 are not shown in the block diagram, and form an extension of the interface between IC1 and the MicroSystem bus. Address decoder IC3 and register address lines R2, R3 and R4 enable up to eight PIT boards to be located at a single card address. In this system, jumper JP1 allows you to define the register address of the card. If the jumper is mounted in position 'K' (default), IC3 is disabled, and the PIT card is addressed with the aid of the card selection signal only. The PIT card also contains its own power supply, and that for the proportional phase angle control board. The 12-V supply voltage on the MicroSystem bus is reduced to 5 V by regulator IC4.

The **phase angle control** is accommodated on a separate board, on which the PIT counter and clock generator signals are combined to produce the firing pulses for the triac in the mains switching circuit. This board contains rather more electronics than suggested by the block diagram. One of the 'extras' is bistable IC3a, which provides the power-on reset. The bistable is reset when the supply voltage is switched on (or when the two contacts of terminal block KS1 are interconnected). Gates IC1c, IC1a and IC1b are then disabled, so that the mains switching circuit receives no drive signal. Setting the bistable enables the gates. This happens automatically as soon as the phase angle control is taken into use.

Another extra sub-circuit is a shift register based on IC2a and I2b. This serves to delay the PIT counter 0 output signal by two clock periods (20 µs). The delay prevents glitches which could cause early triggering of the triac.

The clock signal on the board is supplied by a clock generator, IC5. The two AND gates shown in the block diagram correspond roughly to IC1a and IC2a, although actually IC1d belongs to this function also. The gates combine the inverted counter-0 output signal with the clock signal. Next, the combined signal is applied to IC1a and IC1b (via IC1c) where it is combined again with the output signal of counter 1 and counter 2 respectively. The output signal produced by the AND gates is subsequently sent to a darlington transistor which serves as a driver stage.

The sub-circuit marked **mains switch** is controlled by the output signal supplied by the phase angle control. Ready-made electronic relays are, unfortunately, not suitable here, because they usually switch on the zero crossing, and not at the phase angle (instant) determined by the phase angle control. The mains switch drawn in the circuit diagram is nothing special: an optocoupler drives a triac which switches the load. Further, the switch is surrounded by the usual decoupling and noise-suppressing components.

The **zero-crossing** detector is also a conventional circuit, and for the most part contained in IC1. Resistor R1 and capacitor C1 provide the series reactance ahead of the supply circuit contained in IC1, while C2 is the buffer capacitor associated with that supply. The mains voltage is applied to the detector input via resistor R2. The detector output is connected to an optocoupler via R3. The optocoupler ensures that the signal is passed to the phase control in a safe manner.

## Four boards

As already mentioned, the complete control consists of four boards (apart from the DMM board). The artwork of the boards is given in **Figs. 11, 12, 13 and 15**. Construction is entirely straightforward with the exception of a small modification on the PIT board. In the original design, IC4 was a 78L05, which, unfortunately, proved unable to source enough current, and had to be replaced by a 7805. To enable the 7805 to be fitted on to the board, its central pin has to be bent backwards a little. Mount the 7805 such that its metal tab is at the side of the board edge.

The triac can make do without a heat-sink if the load current remains below 1 A or so. If higher load currents are expected (up to 4 A), the device is best fitted with a small heat-sink (thermal resistance approx. 17 K $W^{-1}$). If necessary, the voltage regulators may also be fitted with such heat-sinks.

Interwiring the boards is not a problem because the connections are clearly indicated in the circuit diagram.

The enclosure of the PIT board has sufficient space to accommodate the phase angle control also. The DMM board (discussed in the previous two instalments) is fitted into a similar enclosure. The mains switching board and the zero-crossing detector are fitted into a mains plug-in case with a moulded mains plug (see Fig. 17 and introductory photograph).

## Let's get fuzzy

The introductory photograph with this instalment shows the example application of the Fuzzy Control One software, developed to get you started. The example is a temperature control. Not a novel application, this, but it has, in principle, everything associated with a 'real' process control.

In addition to the hardware described here, you need the 'fuzzy logic DMM' board, a 75-watt bulb with a socket, a thermometer and an LM35 temperature sensor. The size of the cardboard box used for the prototype control was 30×30×10 cm. A perspex window is made in the box to allow the lamp intensity and the temperature to be viewed from the outside. Using the fuzzy logic control, the 75-watt bulb was capable of heating this little 'oven' to over 50 °C.

Connecting the LM35 is simple. The

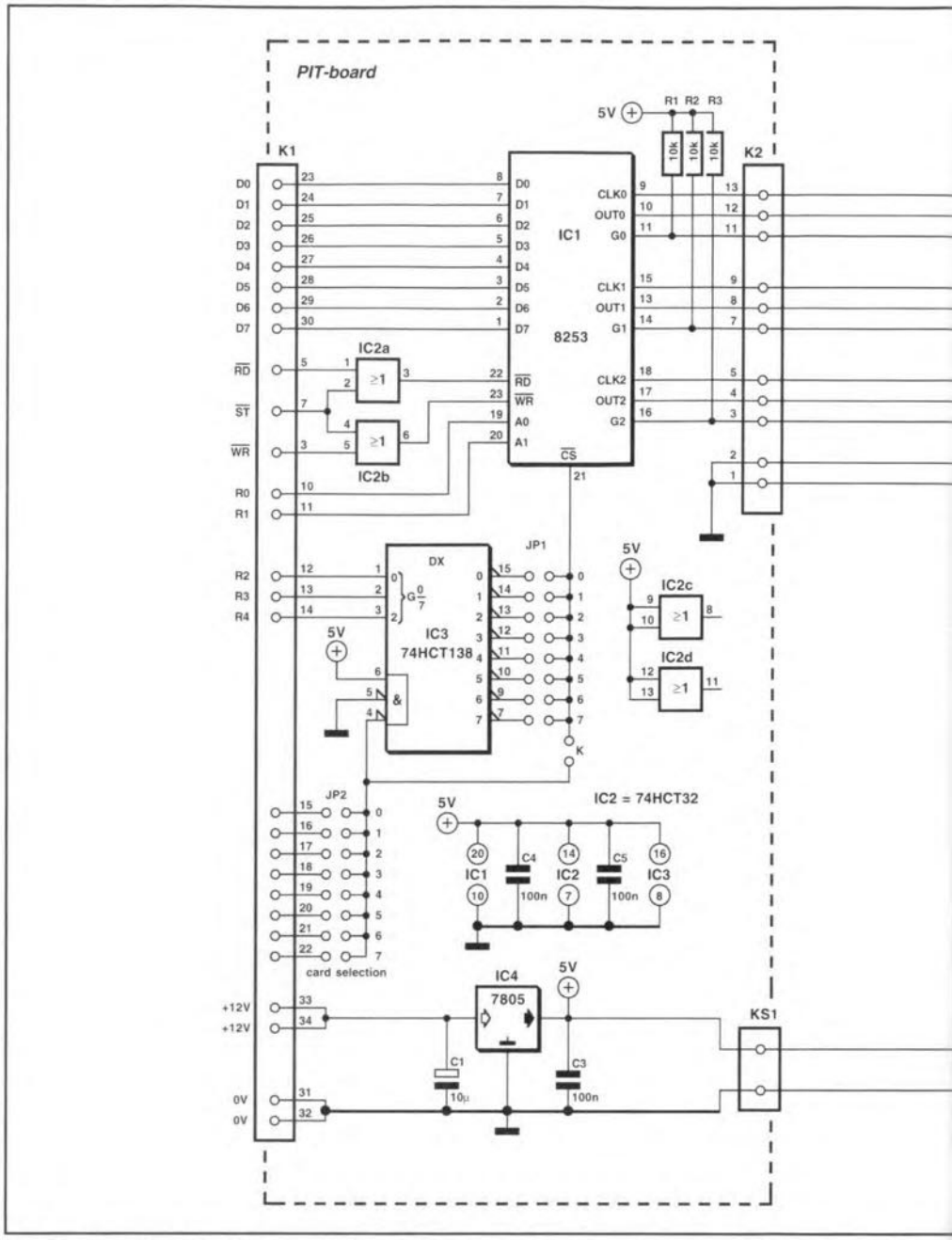



**Fig. 10. Combined circuit diagram of the PIT board, the phase angle control, the mains switch and**

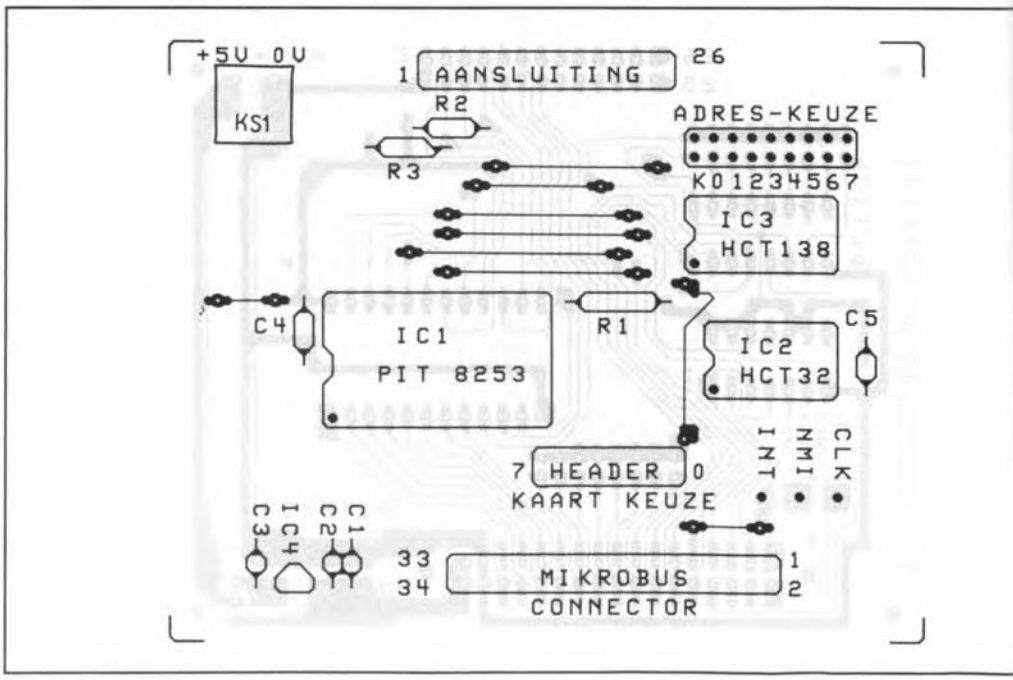
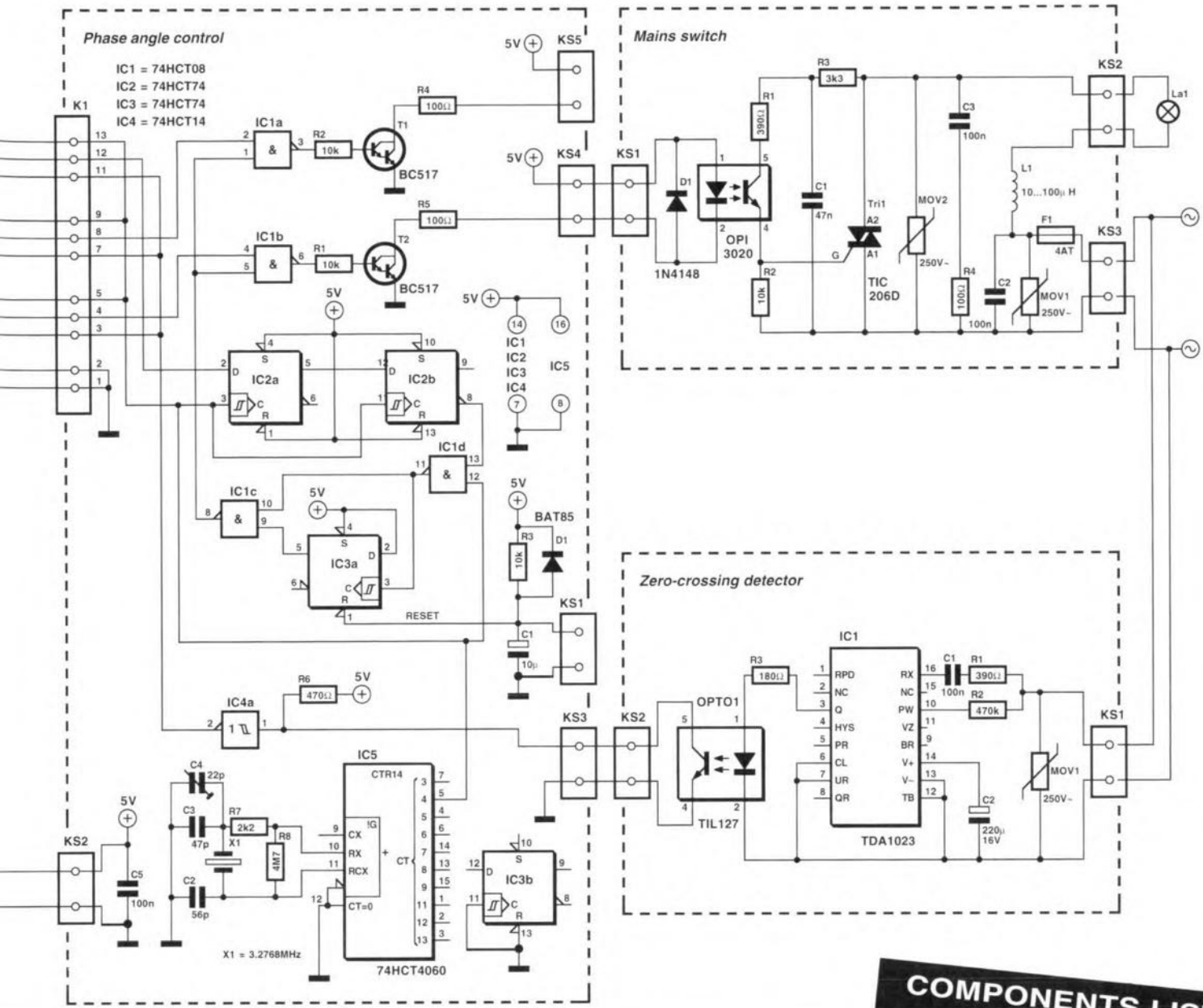
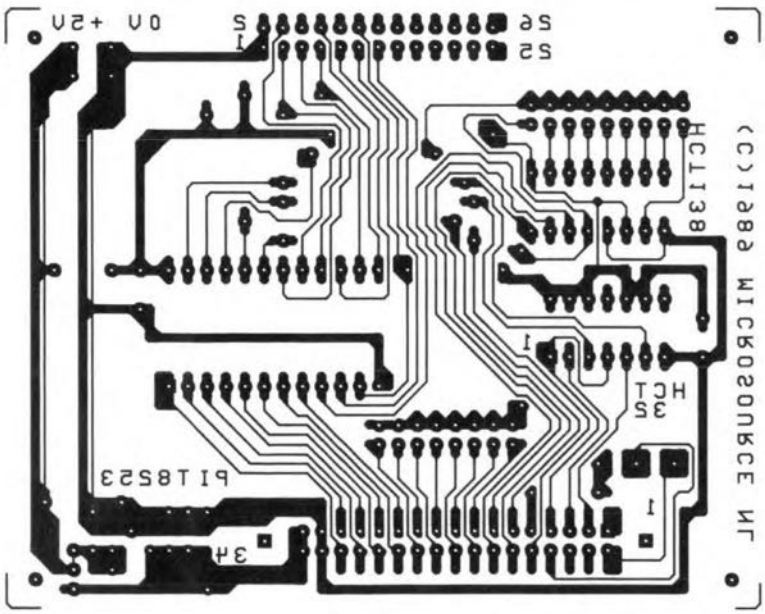



**Fig. 11. Artwork for the single-sided PIT board. 'Aansluiting' = connection; 'adres-keuze' = address setting; 'kaart keuze' = card selection.**




the zero-crossing detector.



## COMPONENTS LIST

PIT BOARD

**Resistors:**

| | | |
|---|---|---|
| 3 | 10KΩ | R1;R2;R3 |

**Capacitors:**

| | | |
|---|---|---|
| 1 | 10µF 16V radial | C1 |
| 3 | 100nF | C3;C4;C5 |
| C2: not fitted | | |

**Semiconductors:**

| | | |
|---|---|---|
| 1 | 8253 | |
| 1 | 74HCT32 | IC1 |
| 1 | 74HCT138 | IC2 |
| 1 | 7805 | IC3 |
| | | IC4 |

**Miscellaneous:**

| | | |
|---|---|---|
| 1 | 34-way header, angled pins, with side latches | K1 |
| 1 | 26-way boxheader | K2 |
| 1 | 2-way PCB terminal block, pitch 5mm | KS1 |
| 1 | 18-way 2-row pin header | |
| 1 | 16-way 2-row pin header | |
| 2 | jumper | |

## COMPONENTS LIST

ZERO CROSSING DETECTOR BOARD

**Resistors:**

| | | |
|---|---|---|
| 1 | 390Ω | R1 |
| 1 | 470Ω | R2 |
| 1 | 180Ω | R3 |
| 1 | SIOV S10K250 | MOV1 |

**Capacitors:**

| | | |
|---|---|---|
| 1 | 10onF 630VDC | C1 |
| 1 | 220µF 16V | C2 |

**Semiconductors:**

| | | |
|---|---|---|
| 1 | TDA1023 | IC1 |
| 1 | TIL127 | OPTO1 |

**Miscellaneous:**

| | | |
|---|---|---|
| 2 | 2-way PCB terminal block, pitch 5mm | KS1;KS2 |

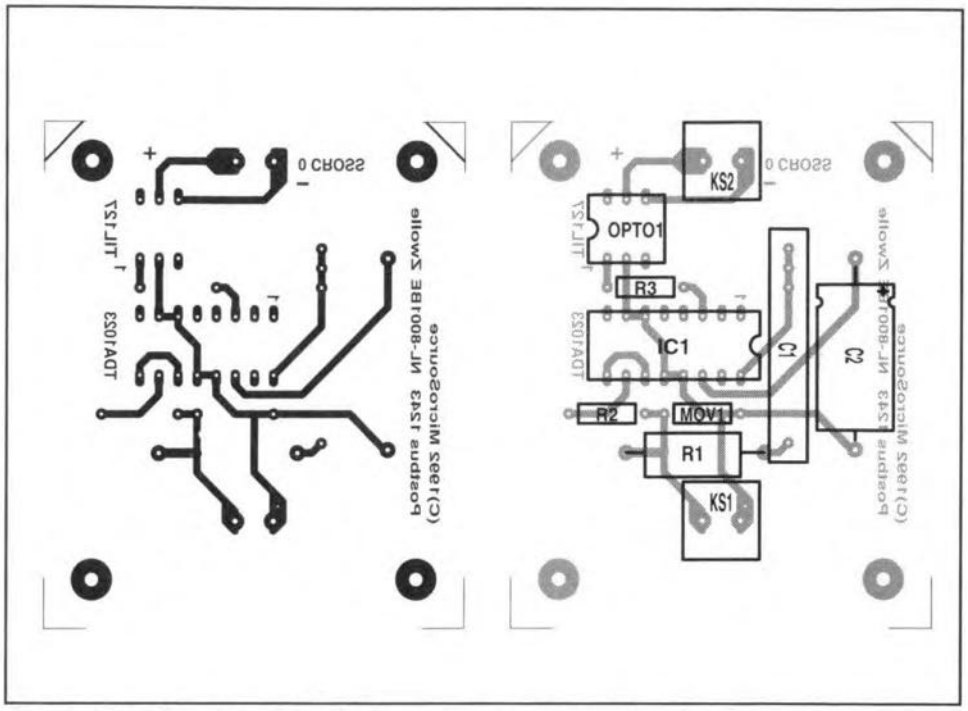



Fig. 12. Artwork for the single-sided zero-crossing detector board.

## COMPONENTS LIST

MAINS SWITCHING BOARD

**Resistors:**

| | | |
|---|---|---|
| 1 | 390Ω | R1 |
| 1 | 10kΩ | R2 |
| 1 | 3kΩ3 | R3 |
| 1 | 100Ω 1W | R4 |
| 2 | SIOV S10K250 | MOV1;MOV2 |

**Capacitors:**

| | | |
|---|---|---|
| 1 | 47nF | C1 |
| 2 | 100nF | C2;C3 |

**Semiconductors:**

| | | |
|---|---|---|
| 1 | 1N4148 | D1;D2 |
| 1 | TIC206D | TR1 |
| 1 | OPI3020 or MOC3020 | OPTO1 |

**Miscellaneous:**

| | | |
|---|---|---|
| 1 | 10-100µH 4A toroid choke | L1 |
| 1 | Fuse 4A slow plus PCB mount holder | F1 |
| 3 | 2-way PCB terminal block, pitch 5mm | KS1;KS2;KS3 |

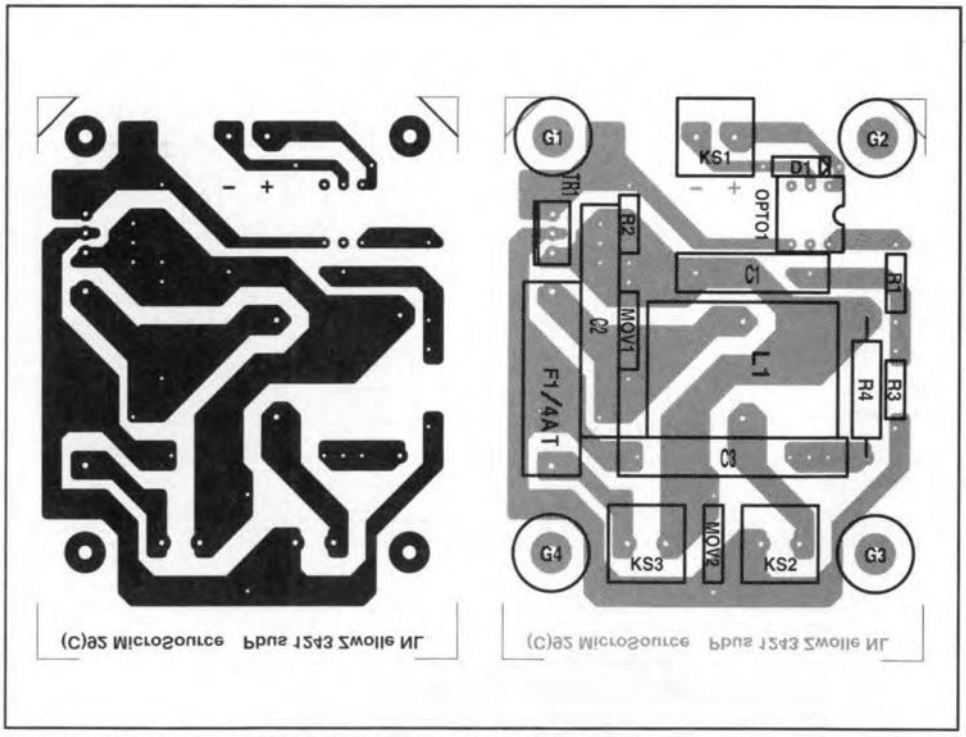



Fig. 13. Artwork for the single-sided mains switching board.

supply voltage is taken from connector K1 on the DMM board. Pin 1 has +5 V, and pin 2, ground. A third wire connects the temperature output signal supplied by the LM35 to the $U_i$ input on the DMM board. For your reference, **Fig. 16** shows the pin connections of the LM35.

Setting up the program is illustrated (and summarized at the same time) in the series of photographs in **Fig. 14**. Following the instructions in the captions with the screen photographs should produce a working control system. This control is based on the knowledge rules and the fuzzy set definitions provided by the demo batch on the Fuzzy Control One disk (order code 1721; see page 70). A discussion of these parameters is unfortunately beyond the scope of this article, since it would take up too many pages of this magazine. This is where the 40-odd pages of help texts supplied with the program come in (these pages can be printed to produce a kind of manual). Once you have the temperature control up and running, you have a solid basis for further experiments. A couple of tips are in order, though.

**Tip 1.** The file containing the fuzzy data does not define legible (i.e., meaningful) names for the various input and output groups ('fuzzy sets'). The group names are simply 1 through 7. Once the temperature control works, assigning legible names to the groups is easy using the 'input division' and 'output division' windows. This makes studying the knowledge rules much easier.

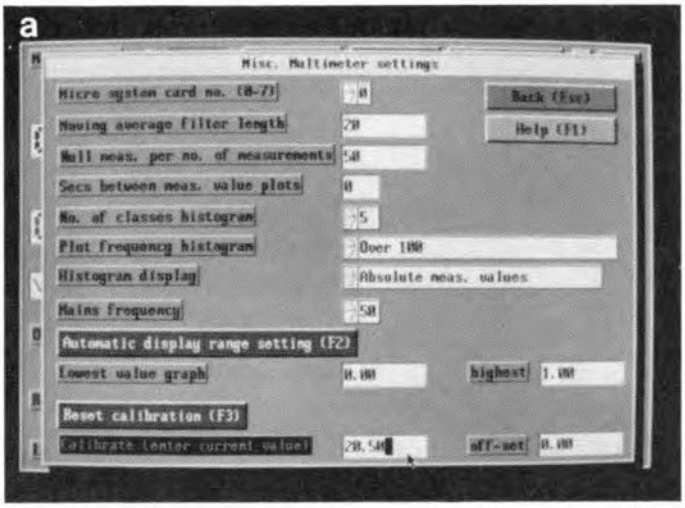



Fig. 14a. Start the program with DVM.BAT. Set the meter to the 4-V range. Leave it on for a couple of minutes while keeping the LM35 at a constant temperature. Go to the Multimeter Settings menu. Enter the temperature (in degrees celsius) in the 'calibrate' window. return to the multimeter screen, and leave the multimeter. This takes you back to the program's main menu.

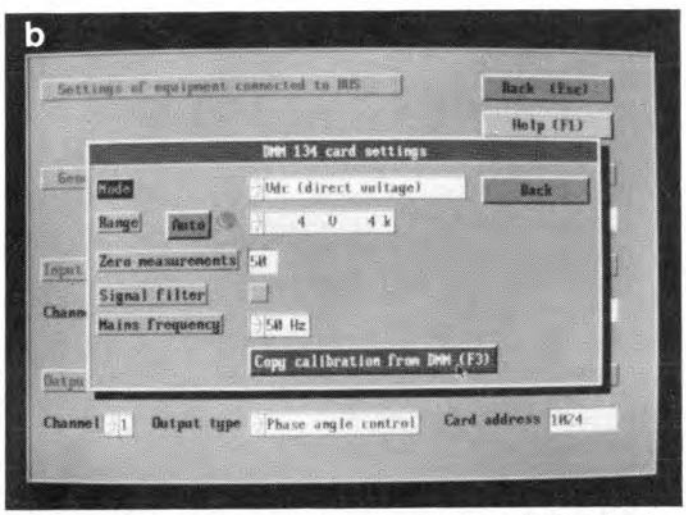



Fig. 14b. Click on the menu option 'hardware', and select 'set hardware'. Select channel 1 as the input channel, and define the multimeter card address (default: 0). Click in the white area behind 'input type', and select the DMM card as the input device. The associated window then appears. Turn off auto-ranging, and select the 4-V range. If necessary, correct the other entries in the windows. Copy the DMM calibration to the control settings. Return to the previous menu.

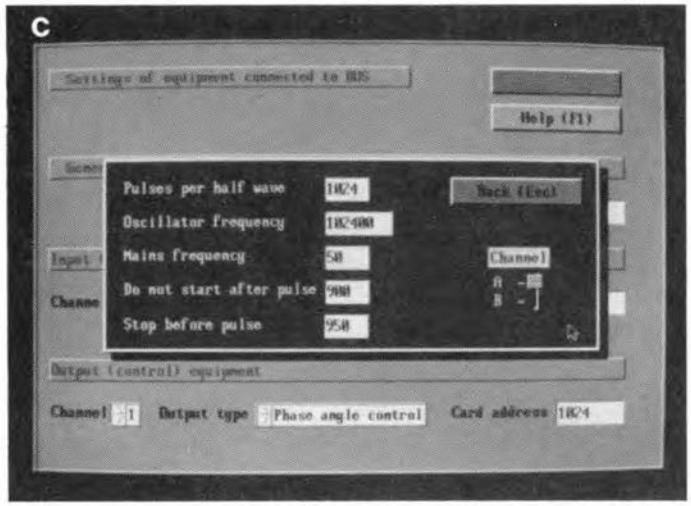



Fig. 14c. If necessary, set the output channel to 1. Set the card address to 1024 (assuming that the PIT card has the default setting). It is possible to enter the card number (1) or the real address relative to the base address (standard: 1024). Select 'phase control' from the options under 'output type' and, if necessary, enter the values shown in the above window. Return to the main menu, and save the file containing the hardware settings. save this file under the name CONTROL.FZH.

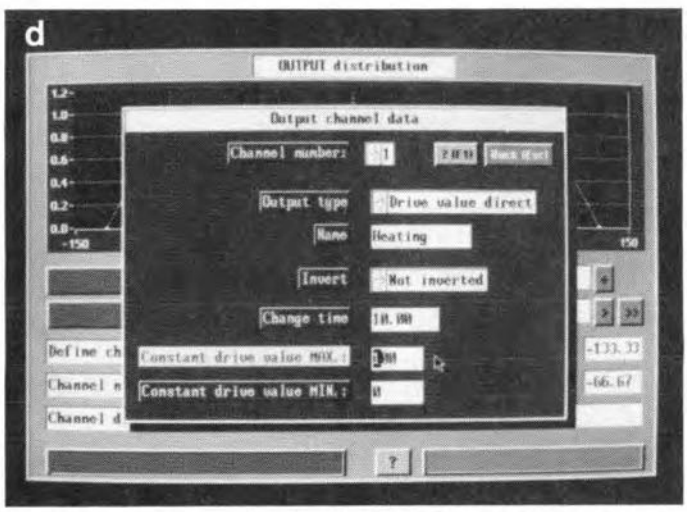



Fig. 14d. Load the control file DEMO1.FZK via the Files option in the main menu. DEMO1.FZK contains the fuzzy data on the control system. These data require only minor changes in the input and output descriptions. Via the main menu, you enter the above menu after passing through 'knowledge', 'input division' and 'channel data'. Enter the data shown above.

**Tip 2.** Looking at the output division, you will notice that the direct output value of the heating is spread over an interval ranging from –100 to 100. This may strike you as unusual, if not odd, for a phase angle control which is capable of regulating from 0 to maximum only. The interval limits can be explained as follows: we are looking at the output of a proportional control, of which the output signal equals the product: (*error* × *amplification*). Since the error can be positive or negative, and the amplification is a constant, the output signal of the proportional control may be positive or negative also. In the case of our example, this means that the interval –100 to 100 corresponds to 'reduce lamp intensity as far as possible' (maximum lamp intensity reduction), or 'increase lamp intensity as far as possible' (maximum lamp intensity increase). Note, however, that this does not imply that the hardware has to process negative drive values. This is because of the knowledge rules, which have an effect similar to that of integrating and differentiating regulators, ensuring a sum value with a range between 0 and maximum under normal circumstances. Although the sum may be negative or greater than the maximum in the rare case of extreme circumstances arising, the effective result is 'clipped' to nought or maximum.

There is one situation in which it is not advisable to program the direct output value division around zero: when you wish to create a proportional control based on knowledge rules of the type 'IF error THEN output' only.

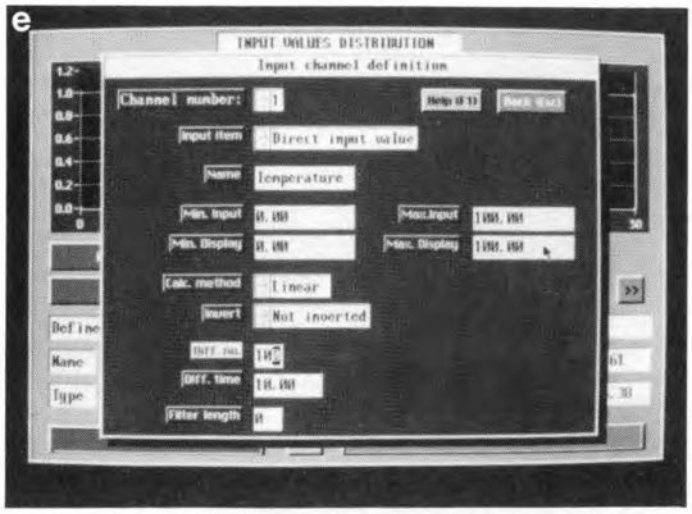



Fig. 14e. Back again in the main menu, you arrive in the above window via the selections 'control', 'output division' and 'channel data'. Copy the data shown above. Return to the main menu, and save the settings as CONTROL.FZK.

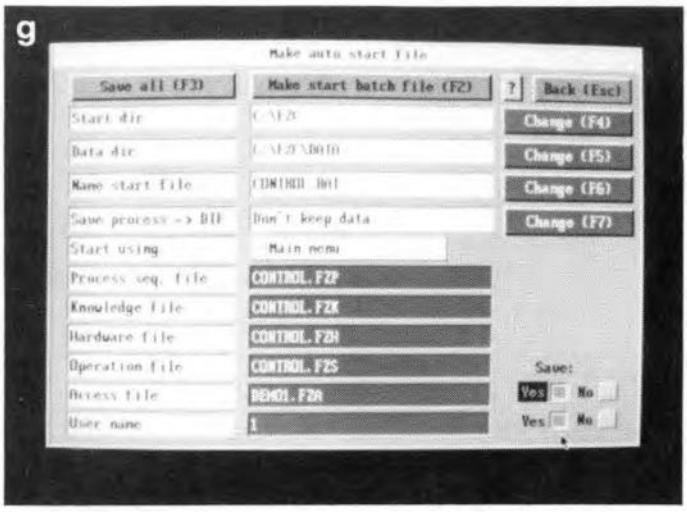



Fig. 14g. Before arriving in the above window, also save the 'operation' file as CONTROL.FZS for the sake of completeness. Next, to arrive in the above window, select (from the main menu) 'files' and 'make start batch'. if a file is missing from the list, or has a different name, you have forgotten to save it under the name 'CONTROL'. If necessary, correct this before proceeding. Click on the YES button, and select the desired 'start with' option. Click on the 'change (F6)' button, and enter the name of the start batch (for example, CONTROL.BAT). Finally, click on the button 'save all'.

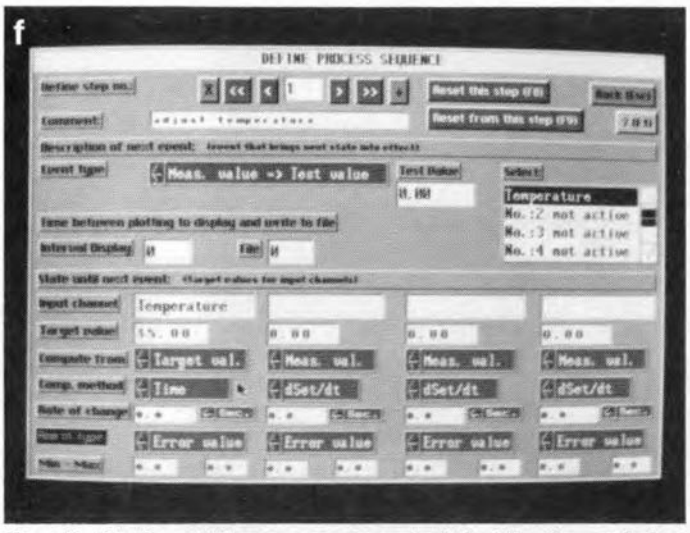



Fig. 14f. Finally, set the process characteristic. The above window is reached from the main menu by selecting 'process' and then 'define process characteristic'. The window is quite crowded, however, only the data in the upper section, and the ones in the first column, matter. The temperature you wish to set in the box is entered as the target value (see mouse arrow). Back in the main menu, save the process file under the name CONTROL.FZP.

In this case, set up a direct output values distribution with a range of zero to maximum.

**Tip 3.** If you create a fuzzy division on an input and an output channel, you can not locate the start of one group at the same value as the end of the next lower group. The software refuses to accept this division because it is an overlap of more than two groups. The problem may be solved by assigning a group start value that is just higher than the end value of the previous group.

**Tip 4.** Doubts can be raised about calling the proposed temperature control 'intelligent', because it strives to keep the temperature in the box constant. Many processes require a much more dynamic behaviour. Fortunately, that is not a problem because the program allows you to define increasing and decreasing target values using the windows available for the process definition. Alternatively, the process may be subdivided into different steps (up to three), for instance; first increase temperature, then keep it constant for 10 minutes after desired temperature is reached, then lower temperature in a controlled manner.

**Tip 5.** Try your hand at making a dimmer. If you succeed in achieving this (it should not be too difficult), and you have fine-tuned the results, it is fair to claim that you have a reasonable 'command' of the program as well as of fuzzy logic in general. A potentiometer of, say, 1 kΩ may act as an input control. The input is divided into two groups, 'resistance at minimum' and 'resistance at maximum'. The output is divided into 'lamp on' and 'lamp off'. Next, you need the following two knowledge rules:

IF resistance minimum THEN lamp off;
IF resistance maximum THEN lamp on.

The 'dead zone' of the control pot in the low-resistance part of its span may

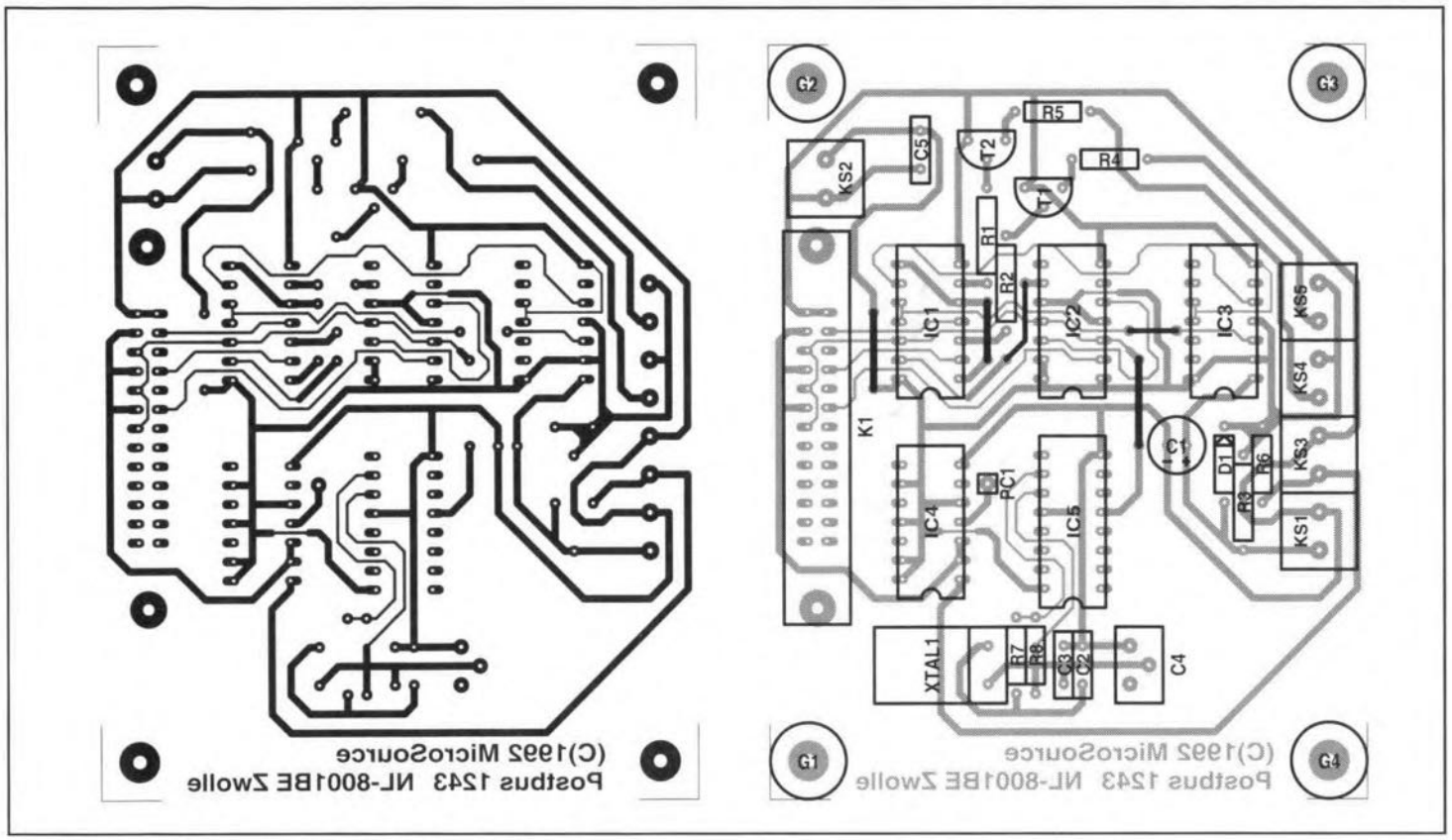



Fig. 15. Artwork for the single-sided phase control board.

## COMPONENTS LIST

PROP. PHASE CONTROL BOARD

**Resistors:**

| | | |
|---|---|---|
| 3 | 10kΩ | R1;R2;R3 |
| 2 | 100Ω | R4;R5 |
| 1 | 470Ω | R6 |
| 1 | 2kΩ2 | R7 |
| 1 | 4MΩ7 | R8 |

**Capacitors:**

| | | |
|---|---|---|
| 1 | 10µF 10V radial | C1 |
| 1 | 56pF | C2 |
| 1 | 47pF | C3 |
| 1 | 22pF trimmer | C4 |
| 1 | 100nF | C5 |

**Semiconductors:**

| | | |
|---|---|---|
| 1 | BAT85 | D1 |
| 2 | BC517 | T1;T2 |
| 1 | 74HCT08 | IC1 |
| 2 | 74HCT74 | IC2;IC3 |
| 1 | 74HCT14 | IC4 |
| 1 | 74HCT4060 | IC5 |

**Miscellaneous:**

| | | |
|---|---|---|
| 1 | 3.2768MHz crystal | XTAL1 |
| 1 | 26-way boxheader | K1 |
| 5 | 2-way PCB terminal block, pitch 5mm | KS1-KS5 |

be eliminated by moving the two output groups upwards.

**Tip 6.** The bulb appears to light unsteadily; it even appears to flash from time to time. This is normal, however, and no cause for alarm. To make the control as reliable as possible, the PIT is initialized over and over again. This, in turn, may cause the triac to be triggered too early by a glitch, or too late. Although this imperfection is visible when using a bulb, it has no effect on the control proper. ■

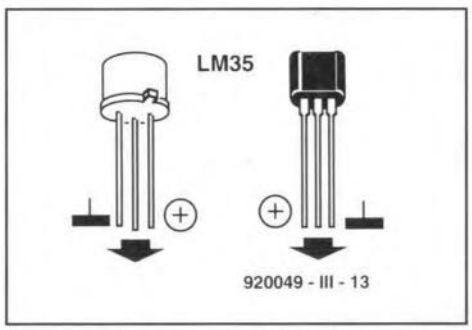
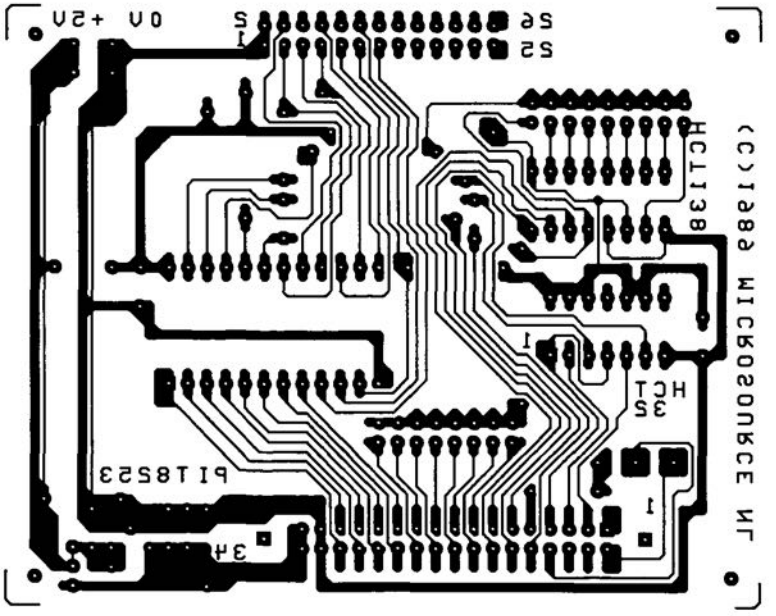



Fig. 16. LM35 temperature sensor connections.

Fig. 17. The PIT board and the phase control board fit in an Eurocard size plastic enclosure. The mains switching board and the zero-crossing board may be mounted into mains adaptor cases with a moulded mains plug/socket.




**Resistors:**

| | | |
|---|---|---|
| 3 | 10KΩ | R1;R2;R3 |

**Capacitors:**

| | | |
|---|---|---|
| 1 | 10µF 16V radial | C1 |
| 3 | 100nF | C3;C4;C5 |
| C2: not fitted | | |

**Semiconductors:**

| | | |
|---|---|---|
| 1 | 8253 | IC1 |
| 1 | 74HCT32 | IC2 |
| 1 | 74HCT138 | IC3 |
| 1 | 7805 | IC4 |

**Miscellaneous:**

| | | |
|---|---|---|
| 1 | 34-way header, angled pins, with side latches | K1 |
| 1 | 26-way boxheader | K2 |
| 1 | 2-way PCB terminal block, pitch 5mm | KS1 |
| 1 | 18-way 2-row pin header | |
| 1 | 16-way 2-row pin header | |
| 2 | jumper | |

ZERO CROSSING DETECTOR BOARD

**Resistors:**

| | | |
|---|---|---|
| 1 | 390Ω | R1 |
| 1 | 470Ω | R2 |
| 1 | 180Ω | R3 |
| 1 | SIOV S10K250 | MOV1 |

**Capacitors:**

| | | |
|---|---|---|
| 1 | 10onF 630VDC | C1 |
| 1 | 220µF 16V | C2 |

**Semiconductors:**

| | | |
|---|---|---|
| 1 | TDA1023 | IC1 |
| 1 | TIL127 | OPTO1 |

**Miscellaneous:**

| | | |
|---|---|---|
| 2 | 2-way PCB terminal block, pitch 5mm | KS1;KS2 |

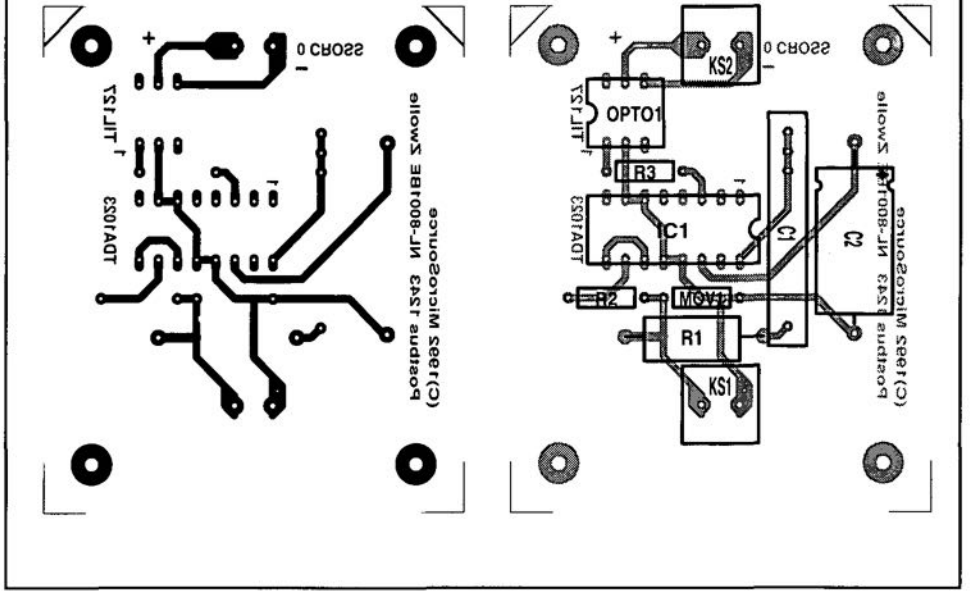



Fig. 12. Artwork for the single-sided zero-crossing detector board.

## COMPONENTS LIST

MAINS SWITCHING BOARD

**Resistors:**

| | | |
|---|---|---|
| 1 | 390Ω | R1 |
| 1 | 10kΩ | R2 |
| 1 | 3kΩ3 | R3 |
| 1 | 100Ω 1W | R4 |
| 2 | SIOV S10K250 | MOV1;MOV2 |

**Capacitors:**

| | | |
|---|---|---|
| 1 | 47nF | C1 |
| 2 | 100nF | C2;C3 |

**Semiconductors:**

| | | |
|---|---|---|
| 1 | 1N4148 | D1;D2 |
| 1 | TIC206D | TR1 |
| 1 | OPI3020 or MOC3020 | OPTO1 |

**Miscellaneous:**

| | | |
|---|---|---|
| 1 | 10-100µH 4A toroid choke | L1 |
| 1 | Fuse 4A slow plus PCB mount holder | F1 |
| 3 | 2-way PCB terminal block, | |

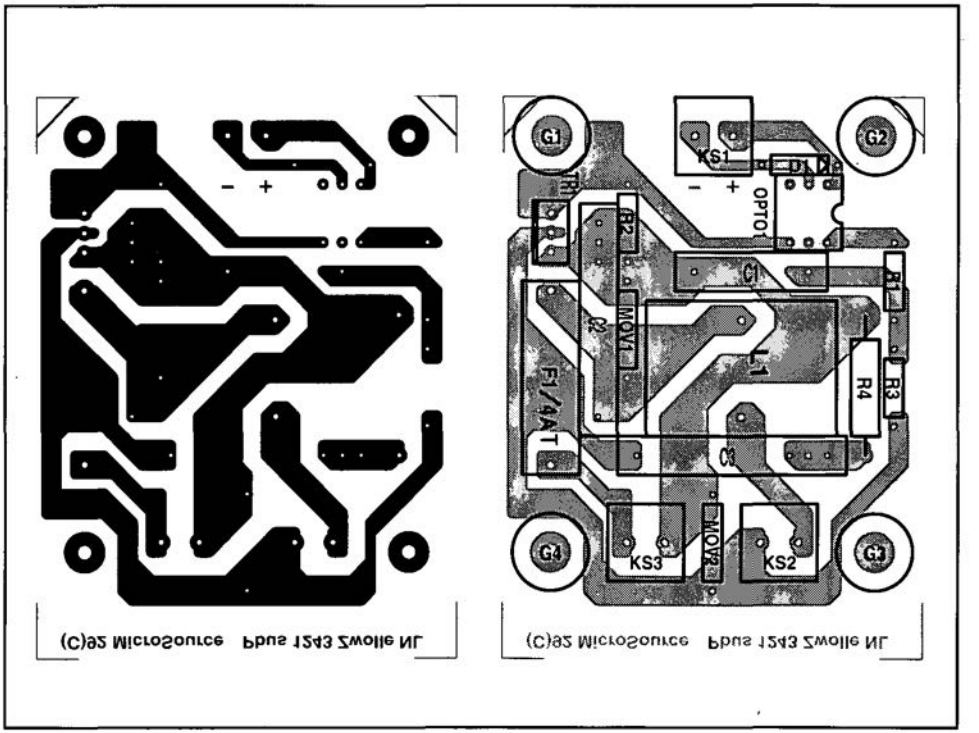



Fig. 13. Artwork for the single-sided mains switching board.