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FUZZY LOGIC MULTIMETER

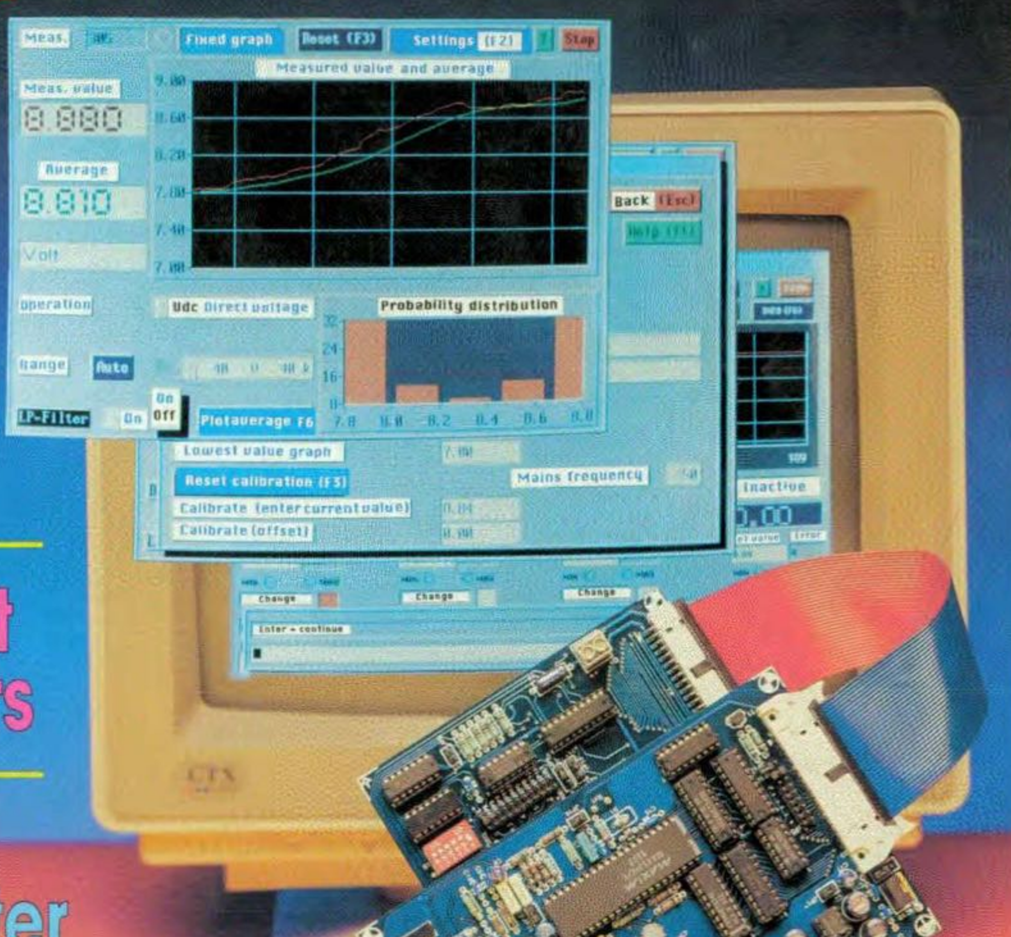
950–1750 MHz converter

Harmonics enhancer

Mini micro clock

Digital output for CD players

PC-aided transistor tester



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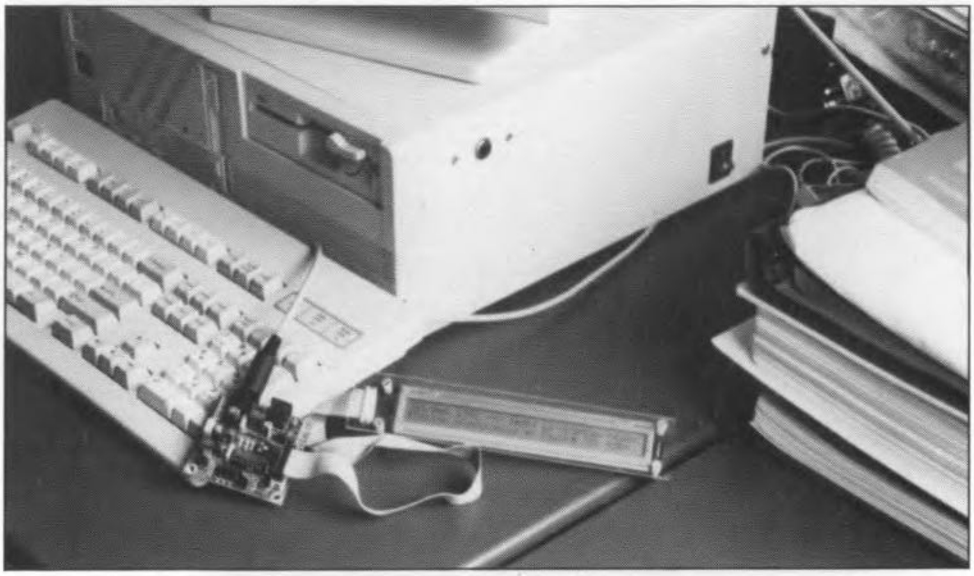
I²C ALPHANUMERICAL DISPLAY



Most alphanumerical LC display units lack an integrated PC interface. Fortunately, this problem is readily solved with the aid of an I²C-compatible interface described here. In addition to describing this clever bit of hardware, we take the opportunity to present an extension to the existing I²C software (in Turbo Pascal), that makes putting text on to an LCD just as easy as writing to PC files, or to the screen.

Design by J. Ruiters

THE text display capabilities of the I²C 7-segment LED unit described earlier (Ref. 1) are at best limited. Considering that the I²C bus is geared mainly to stand-alone microprocessor-controlled equipment, it seems logical to look at ways to have a PC process information other than numbers only via the I²C bus. Implementing text output on a stand-alone microprocessor (or microcontroller) application, such as a video recorder, almost invariably calls for a liquid crystal display (LCD). Unfortunately, while LCDs come in wide variety of sizes, types with an on-board I²C interface are, sadly, not found commercially, whence the present article.

The display

As shown in Fig. 1, what we call an 'LCD' actually consists of an LCD proper and an associated controller circuit. It is, therefore, better to speak of an LCD unit, or LCD module. The module used here is a two-line, 40-character, type from Hitachi. The matrix available for forming a character consists of 5×8 dots. The majority of characters stored in the character ROM, however, consist of 5×7 dots, since the lower dot row is reserved for the cursor. None the less, the lower dot row is used for a couple of special characters only, and, if so programmed, by user-defined characters.

The LCD module has an on-board LCD controller, which has two functions: (1) arrange the position and selection of characters on the LCD, and (2) arrange the communication with the computer. In the present case, this communication is via the I²C interface to be described. Note that only four bits, DB4-DB7, are used for the data exchange between the LCD controller and the I²C interface. Although the controller is perfectly capable of handling eight bits at a time, this would make the I²C interface more complex than necessary. Apart from the four data bits, there are four control lines. The functions of the R/$\overline{W}$ and the enable signal are self-evident. The level of the D/$\overline{I}$ (data/instruction) signal indicates whether the bits on the datalines are an instruction for the LCD controller, or data (i.e., a character) to be shown by the display. The fourth control line, V_{LED}, allows you to switch the LCD's backlight on and off. This backlight is formed by a number of LEDs fitted behind the display. The maximum current consumption of these LEDs is quite high, and causes the maximum current consumption of the module to rise to 250 mA (170 mA typ.) from a 5-V supply. By comparison, the backlight current of 1 to 3 mA as required by other LCDs is quite low.

How the LCD controller handles data and instructions is discussed further on in the section about the software that has been developed for this project. First, however, we tackle the description of the 'other' bit of hardware, the I²C interface.

I²C interface

The circuit diagram of the I²C interface for the 2×40 character LCD module is given in Fig. 2. Those of you who have

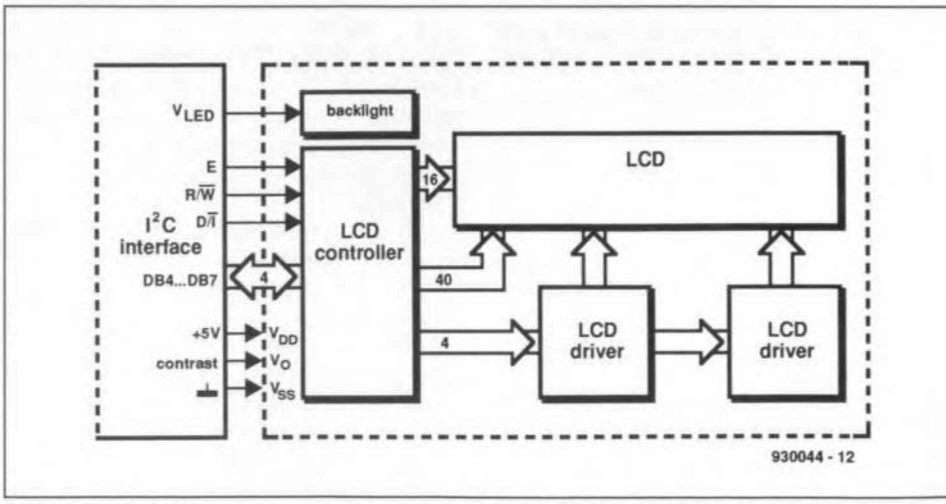


Fig. 1. Block schematic showing the structure of the I²C interface and the LCD module.

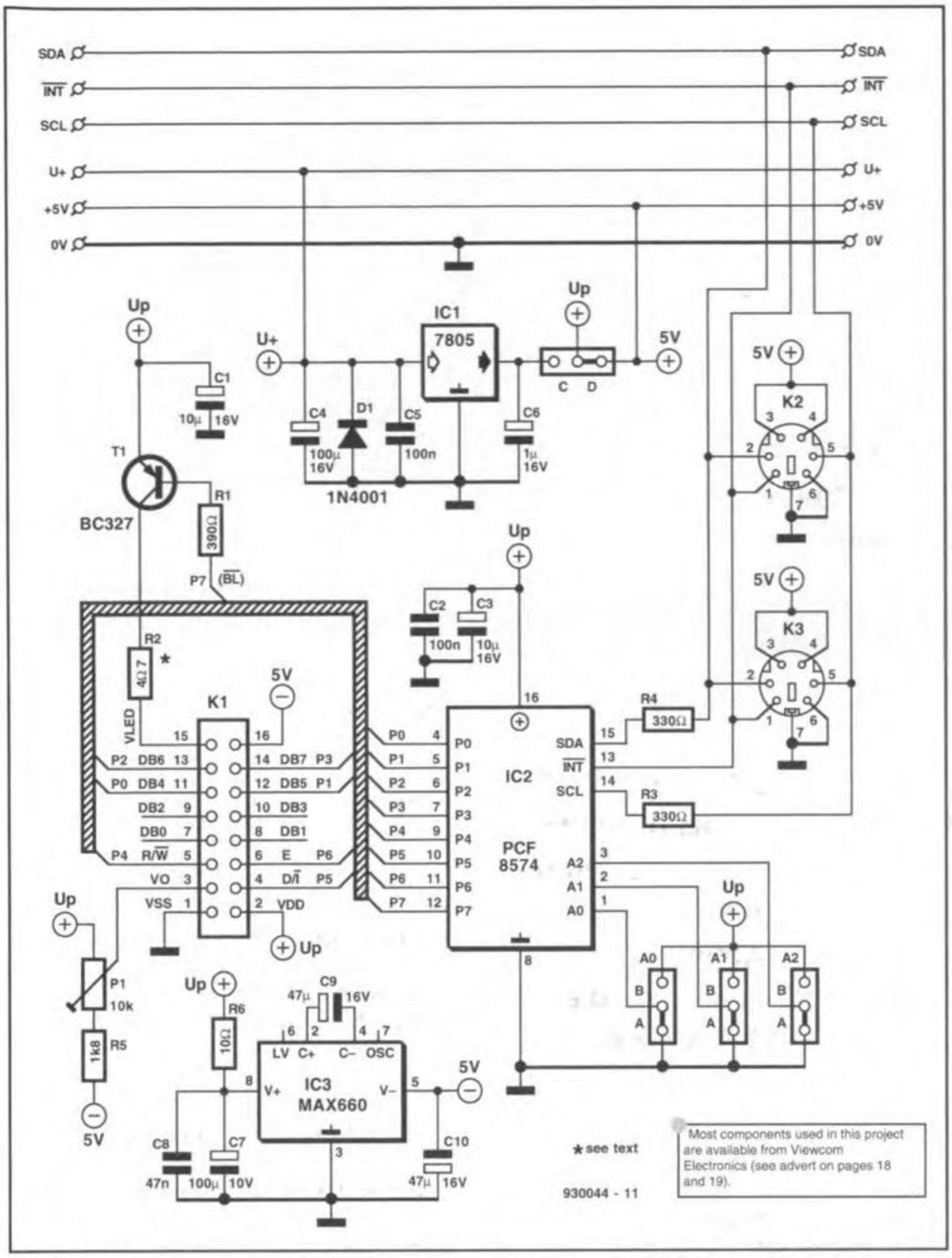


Fig. 2. The interface electronics. IC2 forms a buffer between the I²C bus and the display module input. Data is processed in 'chunks' of four bits.

read our earlier articles on I²C bus devices will recognize the standard bus connections and the 8-bit I/O module Type PCF8574. Actually, this IC forms the complete interface between the I²C bus and the display controller. However, since the PCF8574 has a 'width' of only eight bits, it is not possible to drive the display via eight databits and four control lines. A solution to this problem would be to use two PCF8574s, but that, unfortunately, reduces the total number of these devices that can be connected to the bus. Hence, only one I/O IC is used, and this is supplied with data via four bits only (DB4-DB7). The address assigned to IC2 on the I²C bus is set with the aid of jumpers A0, A1 and A2. The address has the following structure:

0 1 0 0 A2 A1 A0 R/$\overline{\text{W}}$

Transistor T1 also forms part of the interface between the LCD and the I²C bus. The function of T1 is to allow the LCD back light to be switched on and off under software control. The backlight LED current may be limited by R2, unless current limiting is already implemented on the LCD module, as, for instance, on the LM092LN used to develop this project. In case LED current limiting is implemented on the LCD module, R2 is replaced by a wire link. With displays that do require a current limiting resistor, the value of R2 is type dependent.

Circuits IC1 and IC3 are not, strictly speaking, part of the interface circuit, but form the 'finishing touch'. IC1 and jumper C/D enable the I²C interface and the LCD module to be powered from the +5-V line or the U+ line. This allows you to select the power supply most suitable to the application (remember, the LCD module can draw up to 250 mA with the backlight on).

The negative supply voltage for the contrast control is supplied by IC3. The negative voltage is, in principle, not required, since the contrast control can also work with a positive voltage only at the control input. In practice, however, a viewing angle of 90° requires a contrast that can only be achieved by making the control voltage a little negative. The voltage at the V_0 terminal may not drop below 6.5 V under the supply voltage, which equals –1.5 V with respect to ground. This maximum negative value is ensured by R5, which is inserted between the contrast control, P1, and the –5-V output of IC3. Although the –5-V supply is only used for the contrast adjustment, it is also connected to a free pin on connector K1. This is done to allow you to connect opamp circuits (e.g., comparators) to K1. Evidently, the use of the present interface is not limited to LCD control only.

Printed circuit board

Figure 3 shows the track layout and the component mounting plan of the single-sided printed circuit board designed for the I²C LCD interface. Start the construction by fitting the 12 wire links. A 13th wire is required in position R2 if you use the LM092LN display. The remainder of the construction is straightforward, and simply follows the parts list and the component mounting plan.

The interface is connected to the LCD module via a length of flatcable. At the display side, the cable is fitted with a plug-type IDC (press-on) connector, of which the pins are soldered directly to the display board (Fig. 6). This side of the cable is, therefore, not detachable. The plug-type IDC connector has a much lower overall height than a combination of a boxheader on the display board and an IDC socket on the cable. The low-profile connection will be particularly valued where space is tight, for instance, if the display is fitted behind a front panel. The other side of the cable is terminated with an IDC socket, which connects to the box header on the I²C interface board. The IDC socket is fitted such that pin 1 connects to pin 1 of the display board.

Software

The control software for the I²C LCD interface is available ready-programmed, and comes on a 5.25-inch MS-DOS formatted floppy disk for IBM PCs and compatibles. If you have Turbo Pascal on your PC, you may compile the unit 'LCD' contained on

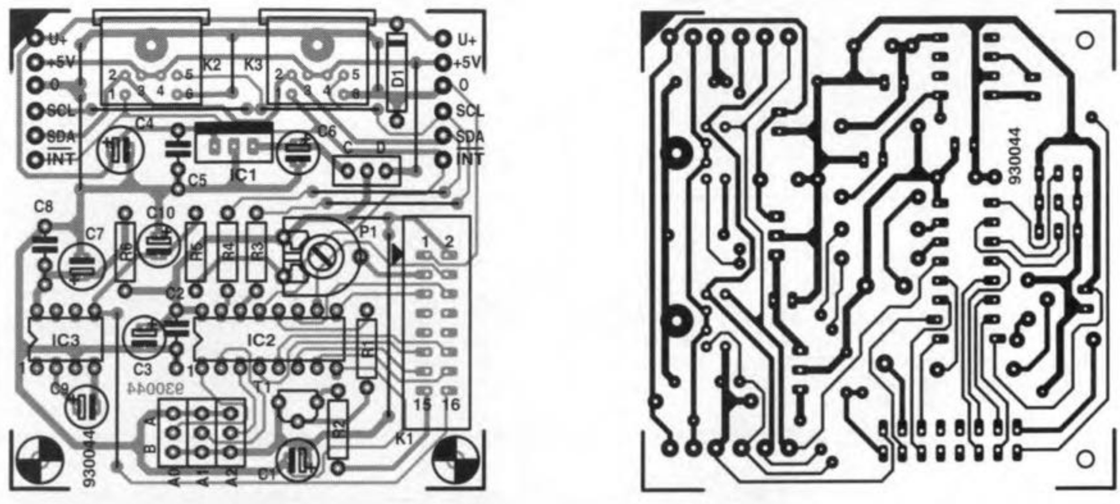


Fig. 3. Printed circuit board design for the I²C-compatible interface for alphanumerical LCDs.

COMPONENTS LIST

Resistors:

1	390Ω	R1
1	4Ω7 (see text)	R2
2	330Ω	R3;R4
1	1kΩ8	R5
1	10Ω	R6
1	10kΩ preset H	P1

Capacitors:

2	10µF 16V radial	C1;C3
2	100nF	C2;C5
1	100µF 16V radial	C4
1	1µF 16V radial	C6
1	100µF 10V radial	C7
1	47nF	C8
2	47µF 16V radial	C9;C10

Semiconductors:

1	1N4001	D1
1	BC327	T1
1	7805	IC1
1	PCF8574	IC2
1	MAX660	IC3

Miscellaneous:

1	16-way box header	K1
2	6-way mini-DIN socket	K2;K3
1	LM092LN LCD (Hitachi)	
1	16-way PCB mount IDC socket	
1	16-way IDC socket	

Approx. 30 cm 16-way flatcable

1 Printed circuit board plus software on disk; set order code 930044 (see page 78)

The control software is also available separately; order code 1851 (see page 78).

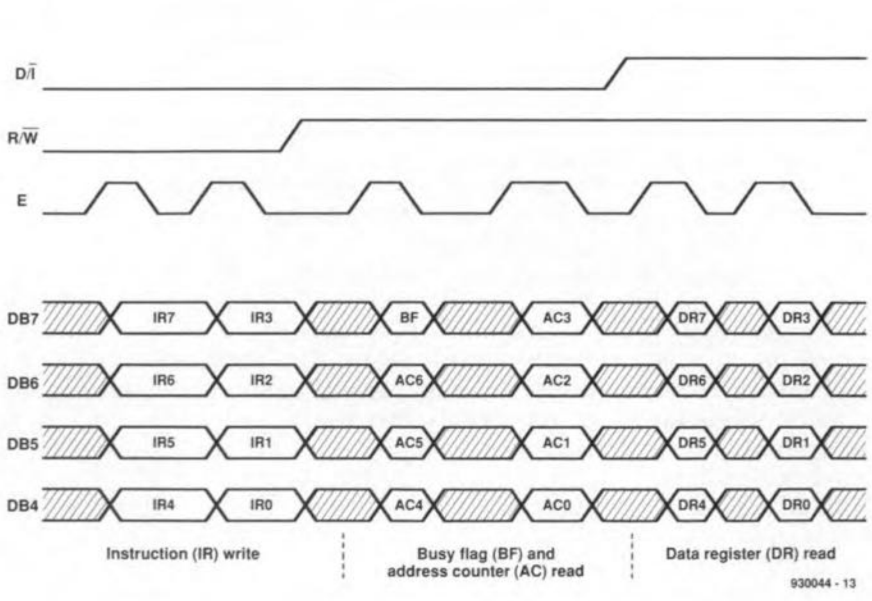


Fig. 4. Timing of data read and write operations.

the disk without worrying about its exact operation. Those of you who can not, for whatever reason, make direct use of the unit, will need to modify it, which obviously calls for a short description. First, however, we deal with the control of the display module. By the way, the source listing of the control software (LCD.PAS) is a great source of information if you want to write your own control software, even if you use a programming language other than Pascal.

The main function of the software is providing the display's data and control lines with the correct information. Remember, the function of the I²C interface is limited to converting the serial data on the I²C bus into parallel data which is fed to the LCD. The software arranges the timing of the data, and the order in which it is presented to the LCD module. Figure 4 shows a timing diagram that illustrates the data read and write operations. Instructions and data are always conveyed to the display in groups of four bits (nibbles). The most significant nibble of a byte is transmitted first.

In the timing diagram, an instruction is placed into the LCD the moment the enable line (E) goes low. The centre part of the timing diagram shows how the software can read the busy flag (BF). At the same time, the contents of the address counter contained in the LCD controller are conveyed. Since the LCD controller is temporarily 'stone deaf' after data is received (40 µs to 1.6 ms, depending on what the data does), the software **must** check the busy flag before doing any read or write operation. The only thing that can be read at all times is the byte containing the busy flag.

The third part of the timing diagram shows the data read operation. Data

```
program HelloLCD;
(****************)

{ Compiler directives.}  {$R-,S-,I-,F-,O-,A-,V+,B-,N-,E+,D-,L-}

{-----------------                     }uses
{ Used units.                          }  crt,LCD,I2C2;
{-----------------                     }const
{ Address of PCF8574 I/O-port.         }  IOAddr=$40;
{-----------------                     }

{-----------------                     }begin (* HelloLCD *)
{ Start I²C-communication.             }  if Start(Bus)<>0 then halt;
{ Address I/O-chip.                    }  if Address(IOAddr)<>0 then halt;
{ Put LCD into 4-bit mode.             }  InitLCD;
{ Turn backlight on.                   }  BackLight:=true;
{ Write to LCD "H"                     }  WriteCharLCD($48);
{ Write to LCD "e"                     }  WriteCharLCD($65);
{ Write to LCD "l"                     }  WriteCharLCD($6C);
{ Write to LCD "l"                     }  WriteCharLCD($6C);
{ Write to LCD "o"                     }  WriteCharLCD($6F);
{ Stop I²C-communication.              }  close(Bus);
{-----------------                     }end.  (* HelloLCD *)
```

must be read when E is logic high.

As already mentioned, those of you who use the Pascal unit 'LCD' need not bother about the above timing conditions, since they are all satisfied by four procedures and one function. With the exception of the procedure 'InitLCD' (the name speaks for itself), the procedures and the function ('GetAddrCntLCD') are found in Table 1, together with the different functions of the LCD controller, which can be actuated in this way. You need not bother about the busy flag, since all procedures run a subroutine to monitor the logic state of BF. All proce-

Fig. 5. Example of a Pascal program that writes 'Hello' on the display.

function			1st 4-bit cycle				2nd 4-bit cycle				Description	LCD.PAS procedure/ function
	D/I	R/W	DB7	DB6	DB5	DB4	DB7	DB6	DB5	DB4		
1: Clear display	0	0	0	0	0	0	0	0	0	1	Clears all display and returns the cursor to the home position (Address 0)	Write Instr LCD
2: return home	0	0	0	0	0	0	0	0	1	*	Returns the cursor to the home position (Address 0). Also returns the display being shifted to the original position. DD RAM contents remain unchanged.	Write Instr LCD
3: Entry mode set	0	0	0	0	0	0	0	1	I/D	S	Sets the cursor move direction and specifies or not to shift the display. These operations are performed during data write and read.	Write Instr LCD
4: Display ON/OFF control	0	0	0	0	0	0	1	D	C	B	Sets ON/OFF of all display (D), cursor ON/OFF (C), and blink of cursor position character (B).	Write Instr LCD
5: Cursor and display shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves the cursor and shifts the display without changing DD RAM contents	Write Instr LCD
6: Function set	0	0	0	0	1	DL	N	F	*	*	Sets interface data length (DL) number of display lindes (L) and character font (F).	Write Instr LCD
7: Set CG RAM address.	0	0	0	1	A_{CG}						Sets the CG RAM address. DD RAM data is sent and received after this setting.	Write Instr LCD
8: Set DD RAM address	0	0	1	A_{DD}							Sets DD RAM address. DD RAM data is sent and received after this setting.	Write Instr LCD
9: Read busy flag&address	0	1	BF	AC							Reads Busy flag (BF) indicating internal operation is being performed and reads address counter contents.	Get Addr (nt LCD)
10: Write data to CG or DD RAM	1	1	Write Data								Writes data into DD RAM or CG RAM.	Write Char LCD
11: Read data from CG or DD RAM	1	1	Read data								Reads data from DD RAM or CG RAM.	Read Char LCD

I/D = 1: Increment (+1) I/D = 0: Decrement (−1)
S = 1: Accompanies display shift.
S/C = 1: Display shift S/C = 0: Cursor move
R/L = 1: Shift to the right.
R/L = 0: Shift to the left.
DL = 1: 8 bits DL = 0: 4 bits
N = 1: 2 lines N = 0: 1 line
F = 1: 5810 dots F = 0: 587 dots
BF = 1: Internally operating
BF = 0: Can accept instruction

DD RAM: Display data RAM
CG RAM: Character generator RAM
A_{CG} : CG RAM address
A_{DD} : DD RAM address
Corresponds to cursor address.
AC : Address counter used for both of DD and CG RAM address

Table 1. LM092LN LCD display functions.

Higher 4bit / Lower 4bit	0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)		0	@	P	`	p		ー	タ	ミ	α	p
xxxx0001	(2)	!	1	A	Q	a	q	。	ア	チ	ム	ä	q
xxxx0010	(3)	"	2	B	R	b	r	「	イ	ツ	メ	β	θ
xxxx0011	(4)	#	3	C	S	c	s	」	ウ	テ	モ	ε	∞
xxxx0100	(5)	$	4	D	T	d	t	、	エ	ト	ヤ	μ	Ω
xxxx0101	(6)	%	5	E	U	e	u	・	オ	ナ	ユ	σ	ü
xxxx0110	(7)	&	6	F	V	f	v	ヲ	カ	ニ	ヨ	ρ	Σ
xxxx0111	(8)	'	7	G	W	g	w	ァ	キ	ヌ	ラ	g	π
xxxx1000	(1)	(	8	H	X	h	x	ィ	ク	ネ	リ	√	x̄
xxxx1001	(2)	)	9	I	Y	i	y	ゥ	ケ	ノ	ル	⁻¹	y
xxxx1010	(3)	*	:	J	Z	j	z	ェ	コ	ハ	レ	j	千
xxxx1011	(4)	+	;	K	[	k	{	ォ	サ	ヒ	ロ	ˣ	万
xxxx1100	(5)	,	<	L	¥	l	|	ャ	シ	フ	ワ	¢	円
xxxx1101	(6)	-	=	M	]	m	}	ュ	ス	ヘ	ン	£	÷
xxxx1110	(7)	.	>	N	^	n	→	ョ	セ	ホ	゛	ñ	
xxxx1111	(8)	/	?	O	_	o	←	ッ	ソ	マ	゜	ö	█

Note: CG ROM is a character generator RAM having a storage function of character pattern which enable to change freely by user's program.

Table 2. LM092LN character set.

1st line	00	01	02	03	04	...	26	27_{HEX}	DD-RAM address
2nd line	40	41	42	43	44	...	66	67_{HEX}	address counter
	1	2	3	4	5	...	39	40_{DEC}	display position

Table 3. Data memory organization of two-line display (N=1).

dures also check the variable 'Backlight'. If it is 'true', the display backlight is switched on. This means that making this variable 'true' is only effective when data is being exchanged with the display.

To give you an impression of the way in which the LCD procedures may be used in a program, Fig. 5 shows an example of a program that writes 'Hello' on the LCD. The floppy disk (order code 1851, supplied with the PCB, but also available separately) contains more examples, including a routine to write a string of characters to the display.

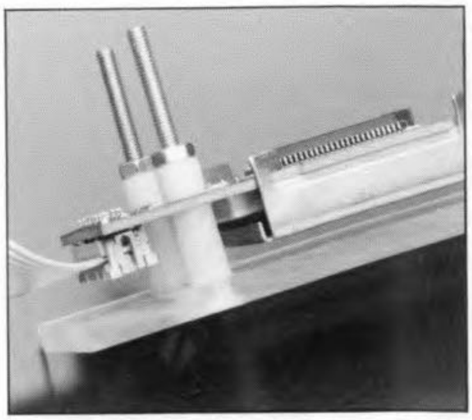


Fig. 6. Suggested flatcable connection on the LCD board.

The letters, numbers and (Japanese) characters that can be displayed, and the associated binary codes, are listed in Table 2. Fortunately, the letters and numbers, and some of the 'specials', have codes that correspond to those in the ASCII set. Obviously, this helps to keep text programming straightforward. The first column of the table (highest four bits 0000) shows eight numbers in brackets. These are the characters you can define yourself. For this purpose, the LCD controller has a small on-chip RAM area called 'CG RAM' (for character generator RAM). Alternatively, this RAM may be used to store data instead of characters.

Finally, you need to know which memory location in the display data RAM (DD RAM; this is the text memory) corresponds to a certain character position on the display. This information is provided by Table 3.

The floppy disk supplied for this project also contains the program 'LCDTEST', which uses all possibilities of the display. Apart from being an excellent hardware test, 'LCDTEST' also provides a lot of background information on the operation of the LCD module and the I^2C interface. One function of the LCD is, however, not covered by 'LCDTEST', and may be the first you wish to tackle on your own: the LCD controller is capable of putting 5×10 matrix characters on one line. However, with the LCD module used here, this makes sense for user-defined characters only, since the screen is divided into two lines with a height of 8 dots and separated by an empty space. This possibility, like many others offered by the combination of the I^2C interface and the LCD module, is open to experimentation. ■

Reference:

1. I^2C LED display. *Elektor Electronics* June 1992.

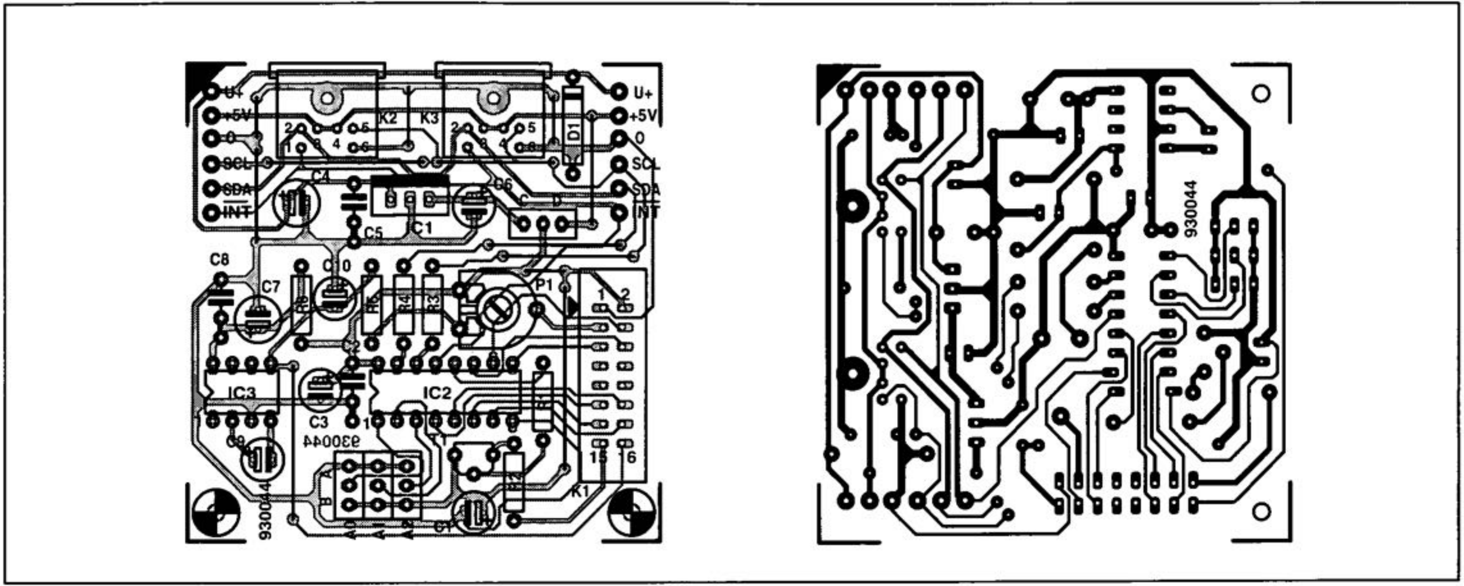
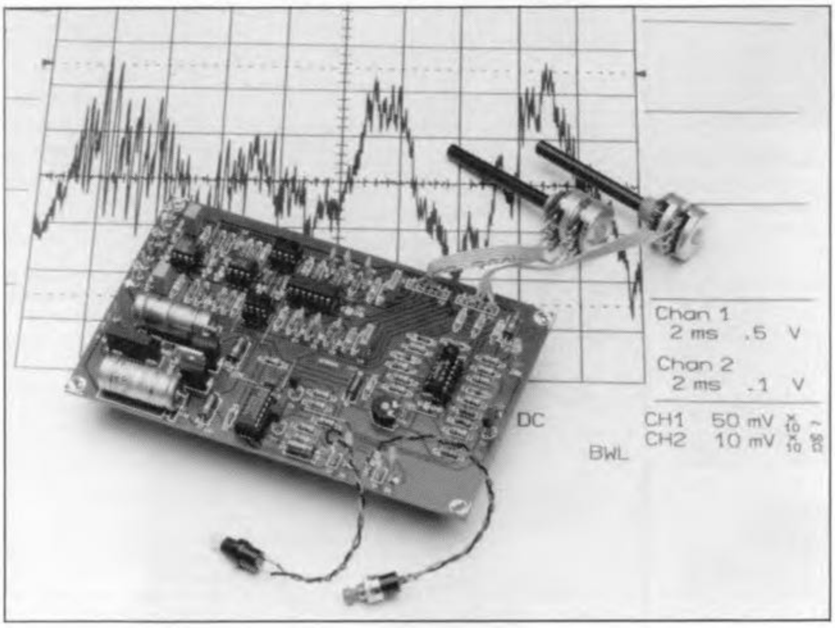


Fig. 2. Printed-circuit board design for the

HARMONICS ENHANCER

Based on a design by M. Eller



The effect of the enhancer is based on the addition of high harmonics to the music signal. This increases the proportion of high harmonics in the overall sound spectrum which makes the sound richer and clearer.

Some harmonics enhancers are capable of processing the signal of only one instrument. They are normally monophonic. Such units can, however, be finely matched to the one instrument.

It is often required, however, for the combined signal from several instruments to be enhanced. Then, a stereo unit as described here is needed.

Principle of operation

The block diagram of the harmonics enhancer—see Fig. 1—shows that the input signal is taken to the output by two paths: directly and via a third-order high-pass filter and a clipping network. The cut-off frequency of the filter is 3.2 kHz, which in most cases is high enough to prevent the fundamental frequencies of the instruments to be affected. Moreover, it is the upper limit of the part of the audio spectrum in which the human ear is most sensitive to changes in the sound.

Although the harmonics enhancer does not give such a dramatic effect as, say, a fuzz box (in fact, its operation is fairly subtle), the filtered high harmonics are distorted drastically by the clipping network: the larger portion of the positive half periods is chopped off. The degree of distortion is influenced by varying the signal level. Because of the distortion, a whole range of new harmonics is generated in addition to the original ones. All these harmonics, new and old, are added to the original signal via a potentiometer to make the final sound richer and clearer.

A gate circuit switches the effect on or off. It also ensures that during intervals there is minimum noise at the output. To that end, the signal to the filter is branched off to a rectifier and buffer capacitor. This arrangement prevents the on/off switching following each and every variation in the input signal. It takes some time, therefore, before the effect is switched off when the signal level is low, or is switched on when the signal level is high enough.

Circuit description

The enhancer is an assembly of small basic circuits based on opamps as shown in Fig. 2. There are buffers ($IC_{1a,\,1b}$, $IC_{3a,\,3d}$); summing amplifiers ($IC_{2a,\,2b}$); filters ($IC_{3b,\,3c}$); a rectifier (IC_{4a}), comparators ($IC_{4b,\,4c,\,4d}$); an AND gate ($IC_{7a,\,7b}$); a bistable ($IC_{7c,\,7d}$), and a power supply.

The gate circuit, based on bistable $IC_{7a,\,7b}$, serves to switch the effect on and off; the state of the circuit is indicated by LEDs D_8 and D_9. It would, of course, have been possible to use a manually operated switch, but the bistable has the advantage of aranging for the effect to be switched off automatically when the supply is switched on. This prevents the accidental use of the effect should the switch be left 'on'. Capacitor C_{15} arranges for the bistable to remain disabled slightly longer than the 'on' input when the supply is switched on. The bistable controls the two LEDs via T_1 and T_2. The actual enabling of the effect is arranged by gates IC_{7a} and IC_{7b}, and analogue switches IC_5 and IC_6.

The level indicator shows the (relative) magnitude of the signal applied to the filter, not that of the input signal. The signal for the indicator is taken from the same rectifier that is used in the noise limiting gate. The indicator shows three levels: too low (both LEDs out); correct (D_{11} lights); too high (D_{10} lights). The low level is detected by IC_{4d} and in-

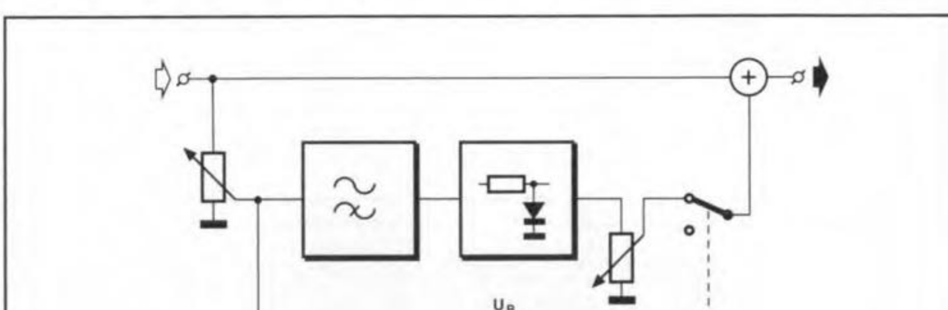


Fig. 1. Block diagram of the harmonics enhancer.

dicated by D_{11}. When this LED is on, the input level set with $P_{1a, 1b}$ is high enough for proper operation of the enhancer. If the level is set too high, the output of comparator IC_{4c} changes state, which causes D_{10} to light. At the same time, the change-over level of IC_{4d} is raised sufficiently via D_7 and R_{42} to cause the quenching of D_{11}. The two LEDs are powered in tandem with the enhancer via T_3.

In the left-hand channel (the right-hand channel operates identically, of course), IC_{1b} buffers the input signal, which is then applied directly to potentiometer P_{1a} and to summing amplifier IC_{2b} via R_3.

The signal at the wiper of P_{1a} is fed to

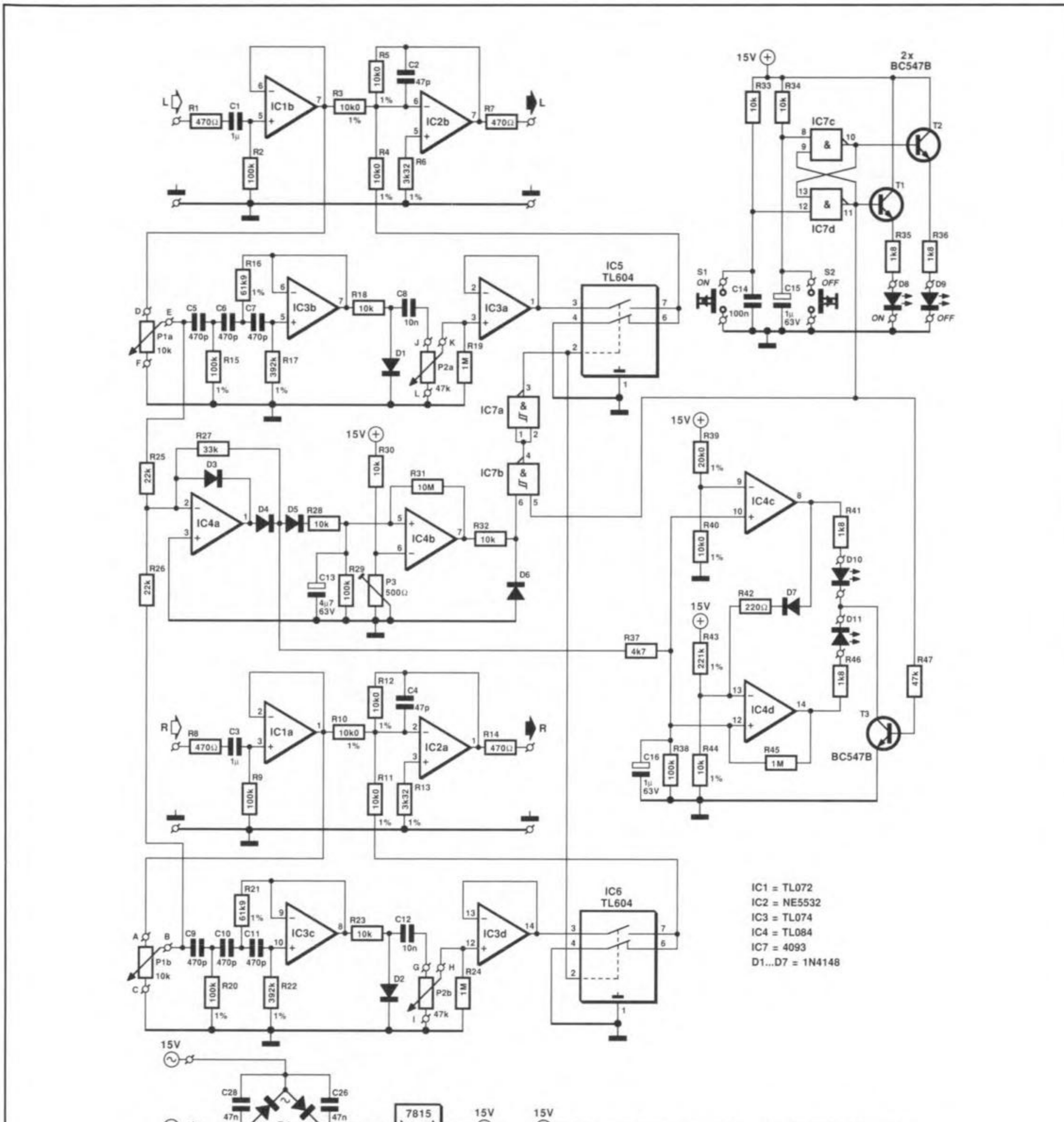


Fig. 2. Circuit diagram of the harmonics enhancer.

the filter based on IC_{3b} and to the rectifier for the gate circuit and level indicator (IC_{4a}).

The filter is a third-order type with Bessel characteristic. Its output is applied to clipping network D_1-R_8, from where it is passed to potentiometer P_{2a}, which sets the level of the distorted signal.

The distorted signal is applied via buffer IC_{3a} to electronic switch IC_5, with which the effect may be switched on or off. The type of switch used can handle the supply voltage (which a CMOS switch can not). From the switch, the distorted signal is applied to IC_{2b}, where it is added to the original signal.

The gate circuit, based on IC_{4b}, is, like rectifier IC_{4a}, common to both stereo channels. It compares the potential across C_{13} with the level set with P_3. Since C_{13} is charged faster than it can discharge, the circuit reacts quickly when the signal level rises above the switching threshold and rather more slowly when the signal level drops. This obviates the continual switching of the circuit.

The power supply is conventional: the symmetrical 15 V power lines are provided by two 3-pin voltage regulators. These are themselves fed by a symmetrical 15 V alternating voltage after this has been rectified by bridge B_1.

Construction

The enhancer is best built on the printed-

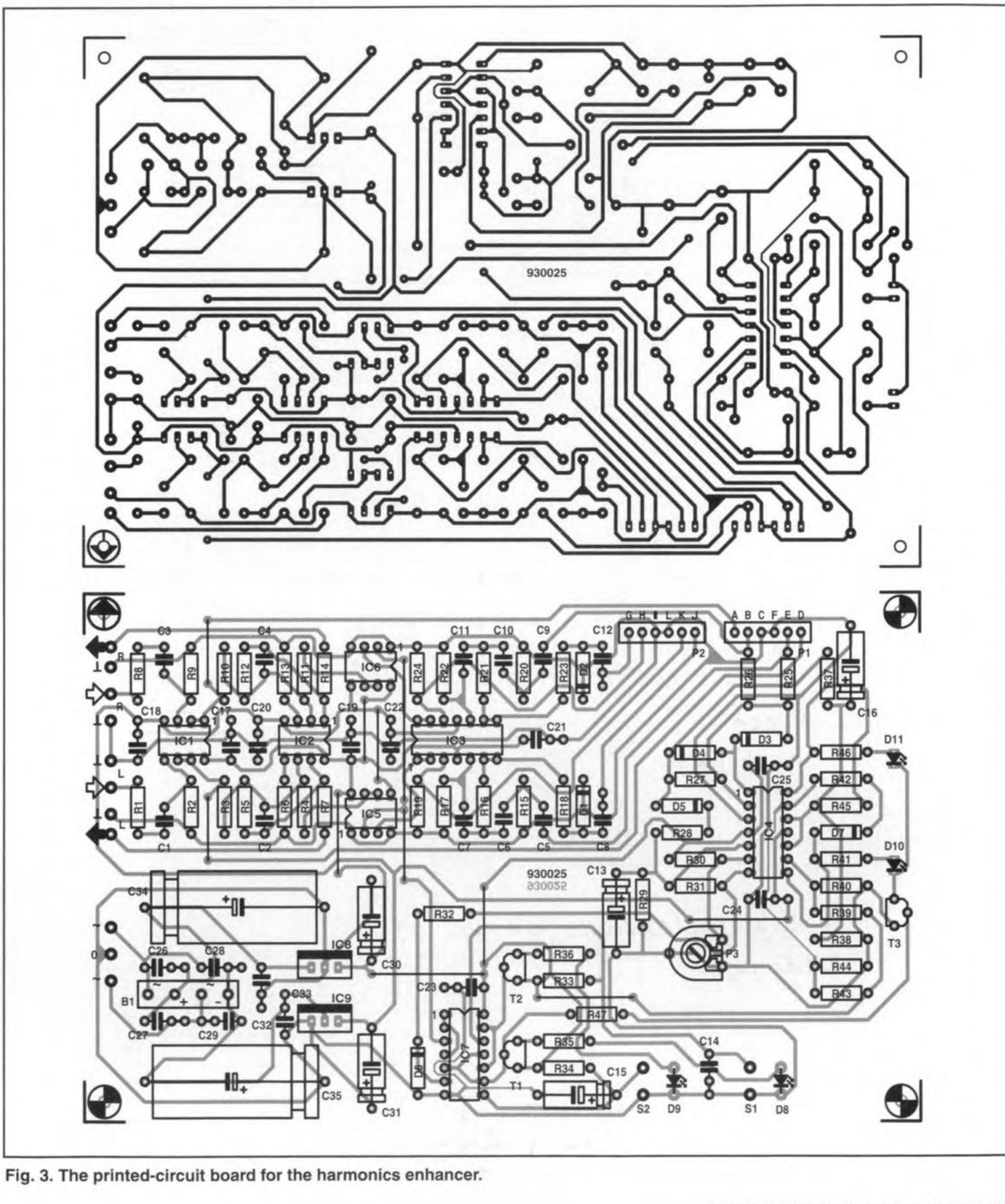


Fig. 3. The printed-circuit board for the harmonics enhancer.

PARTS LIST

Resistors:
R1, R7, R8, R14 = 470 Ω
R2, R9, R29, R38 = 100 kΩ
R3–R5, R10–R12, R40, R44 = 10.0 kΩ*
R6, R13 = 3.32 kΩ*
R15, R20 = 100 kΩ*
R16, R21 = 61.9 kΩ*
R17, R22 = 392 kΩ*
R18, R23, R28, R30, R32–R34 = 10 kΩ
R19, R24, R45 = 1 MΩ
R25, R26 = 22 kΩ
R27 = 33 kΩ
R31 = 10 MΩ
R35, R36, R41, R46 = 1.8 kΩ
R37 = 4.7 kΩ
R39 = 20.0 kΩ*
R42 = 220 Ω
R43 = 221 kΩ
R47 = 47 kΩ
P1 = linear stereo potmeter 10 kΩ
P2 = linear stereo potmeter 47 kΩ
P3 = preset 500 Ω

* 1% type

Capacitors:
C1, C3 = 1 μF
C2, C4 = 47 pF
C5–C7, C9–C11 = 470 pF
C8, C12 = 10 nF
C13 = 4.7 μF, 63 V
C14, C17–C25 = 100 nF
C15, C16 = 1 μF, 63 V
C26–C29, C32, C33 = 47 nF, ceramic
C30, C31 = 10 μF, 25 V
C34, C35 = 470 μF, 40 V

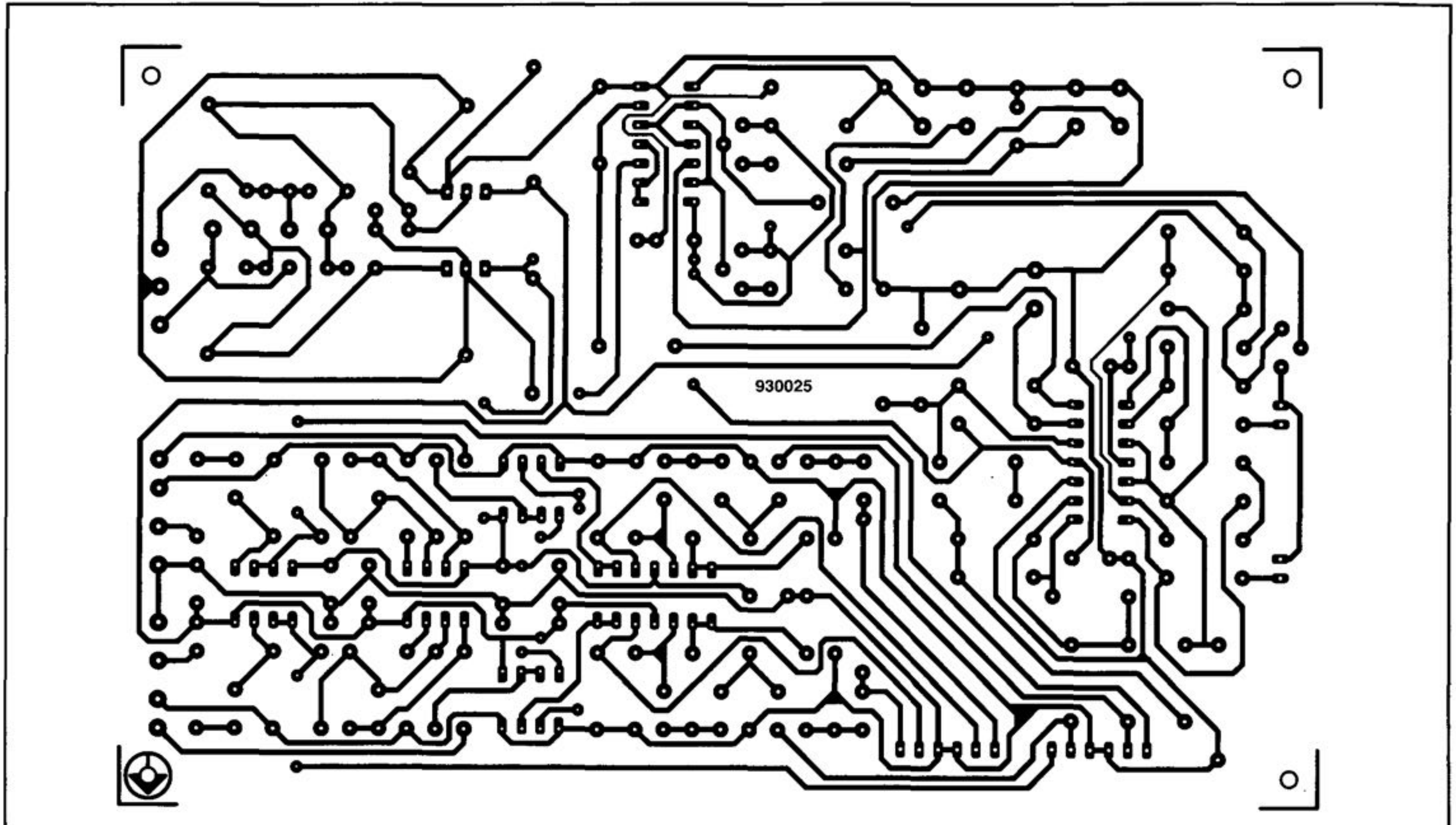
Semiconductors:
D1–D7 = 1N4148
D8, D9 = LED, yellow
D10 = LED, red
D11 = LED, green
B1 = B80C1500 rectifier bridge
T1–T3 = BC547B
IC1 = TL072
IC2 = NE5532
IC3 = TL074
IC4 = TL084
IC5, IC6 = TL604
IC7 = 4093
IC8 = 7815
IC9 = 7915

Miscellaneous:
S1, S2 = spring-loaded press-to-make switch
PCB No. 930025 (see p. 78)

circuit board shown in Fig. 3, which is available ready made. It is Eurocard size (100×160 mm — $4\times6^3/_8$ in). Little needs to be said about the population of the board, which is straightforward.

Generally, setting P$_3$ to the centre of its travel will give correct operation. When D$_{11}$ lights, the level is sufficiently high for a proper effect. Make sure, however, that the set resistance of the potentiometer does not exceed 400 Ω, because then the switching level is greater than the level at which D$_{11}$ lights.

When the enhancer is fitted between an input and output of a mixer panel, R$_3$ and R$_{10}$ may be omitted. The additional harmonics are then added to the original signal in the panel, not in the enhancer. **END**


930025

950-1750 MHz CONVERTER

An inexpensive tuner module obtained in the electronics surplus trade allows anyone who has successfully built the VHF/UHF receiver (described a few months ago) to listen to signals in the ether above 900 MHz. This brings you, among others, the complete 23-cm amateur radio band, the future 900-MHz CB band, car telephone repeaters and short-range cordless telephones. A mini-discone antenna with a built-in wideband preamplifier designed for the SHF band is also described.

Design by B. Romijn

At the heart of the present converter is a tuner module salvaged from a Ferguson SRB-1 ex-BSB (British Satellite Broadcasting) satellite TV receiver. The tuner used is designated 'AS SAT 5601', and is also available as a single part from electronics surplus outlets. With some dexterity, and provided connection details are to hand, other, similar, tuners may also be used. Satellite TV tuner modules come in an immense variety of makes with only marginally different specifications, and can often be picked up at bargain prices at radio amateur jumble sales, car booth sales, and rallies.

The input frequency of the AS SAT 5601 tuner is 950-1750 MHz. The internal local oscillator is varicap-tuned and covers a frequency range of 1430-2230 MHz. The IF (intermediate frequency) is 480 MHz, and may be 'tapped' from a clearly marked point in the tuner. This signal may be fed to the antenna input of the VHF/UHF receiver (Ref. 1), or that of a scanner. By tuning the receiver (or scanner) a little higher or lower, it is possible to go over 1750 MHz, or lower than 950 MHz. If the VHF/UHF receiver is used, this enables virtually continuous frequency coverage from 86 MHz to 1800 MHz to be achieved.

About the tuner

The photographs in Figs. 1 and 2 show the tuner module with the cover plates removed. It is very well possible that your tuner does not even have solder on its pins, simply because it is brand new.

Not all of the ten connecting pins are used for the present application — see the circuit diagram in Fig. 5. Also, the 480 MHz IF output signal is taken from point 'BP03' inside the tuner module via a 2.2-pF coupling capacitor. A printed circuit board is not used to fit the tuner module — all components mentioned below are soldered directly to the relevant pins and/or the tuner module enclosure. Where wires are used, these should be kept as short as possible.

Pins 2 and 5 are grounded, i.e., connected to the tuner enclosure via the shortest possible wires. The supply voltage pins, 3 and 7, are interconnected, and fitted with 150-pF decoupling capacitors direct at the pins. The same goes for the tuning voltage pins, 4 and 8. The 'regular' tuner supply and the tuning voltage supply are discussed further on. Three pins of the tuner are not used: pin 6, which supplies the baseband signal (FM demodulator output); pin 10, the +5-V supply connection for the internal prescaler (÷2); and pin 9, the prescaler output.

Amplification

The antenna signal is fed to the tuner input, pin 1, via a 2.2-pF coupling capacitor. Since the tuner itself is not sensitive enough for direct connection to an antenna, it is driven by a two-stage wideband preamplifier based on MAR6 integrated amplifiers (Fig. 4). One stage of the preamplifier is fitted on to the tuner module (Fig. 5), while the other MAR6 (the input stage proper) is part of the roof-mounted active mini discone antenna.

The construction of the MAR6 RF amplifier on the tuner is illustrated by the photograph in Fig. 6. The input pin of the MAR6 is marked by a white dot as well as a tapered end. The output/supply pin is directly across the device. The other two pins are the ground connections. They are bent down and then sideways, so that the MAR6 body is a little above the module. The 2.2-pF output coupling capacitor, C_3, and the power supply resistor, R_2, are soldered to the MAR6 output pin as shown in the photograph. The terminals of R_2 are turned into chokes L_{2a} and L_{2b} by winding them three times around a 1-mm precision screwdriver bit or similar. Stretch the turns as shown.

Although the input coupling capacitor, C_2, may be fitted directly between the core of the coax cable and the input pin of the MAR6, some of you may prefer to make this junction on a solder spot. This may be achieved by glueing a small piece of veroboard (or similar) on to the tuner module, and using a single copper spot to join the MAR6 input pin to C_2. A second copper

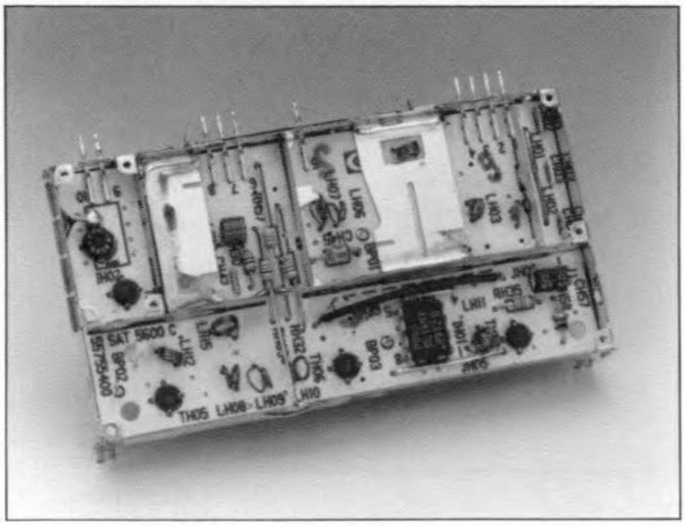


Fig. 1. One side of the AS SAT 5601 tuner has no cover. The IF output signal is 'tapped' from a terminal marked BP03 near the SL1451 demodulator IC.

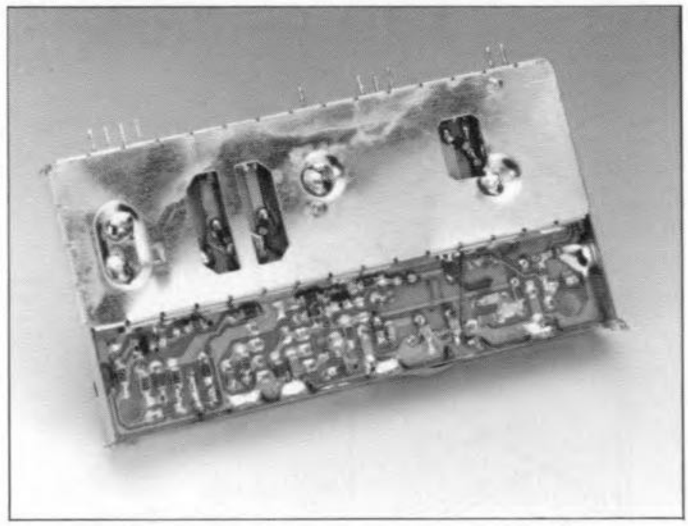
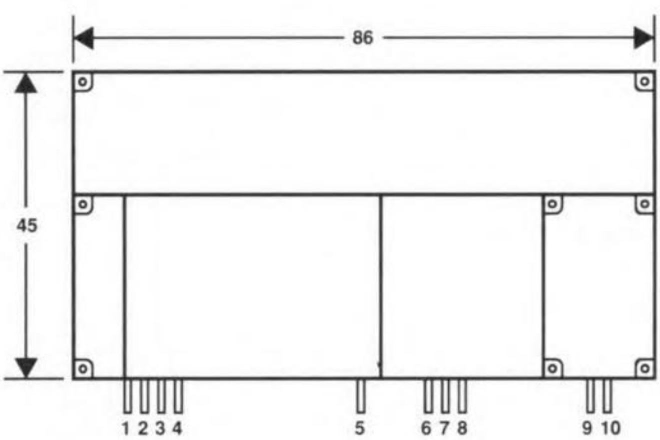


Fig. 2. The other side of the tuner is partly screened by a tin plate cover. Note that most of the components used are SMT (surface mount technology) types.



1	INPUT	6	Output Compose VIDEO
2	GROUND	7	+ 15V
3	+ 15V	8	Tuning Voltage
4	Tuning Voltage	9	Output Frequency Divider
5	GROUND	10	+ 5V

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Fig. 3. Enclosure dimensions and pinout of the AS SAT 5601 tuner module. Not all pins are used in the present application.

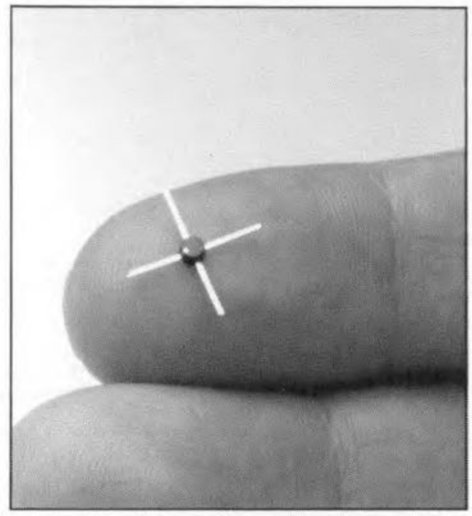


Fig. 4. Tiny but effective: the MAR6 integrated wideband monolithic amplifier from MiniCircuits Laboratories. The white dot indicates the supply/output terminal.

spot may then be used to make the junction between the other terminal of C2 and the core of the coax cable. The braid of the input coax cable is soldered securely to the tuner module over a length of 1-2 cm. The other end of the coax cable is connected to an N-type or BNC-type RF input socket fitted on the rear panel of the converter enclosure. Ordinary 75-Ω TV coax is fine for this application. The resistor/choke combination R1/L1 (Fig. 5), via which the mini discone antenna is powered, is soldered directly to the centre pin of the RF input socket. Inductors L1a and L1b are made in the same way as L2a and L2b (see above). Decoupling capacitors C5 and C11 are fitted as close as possible to the supply side of L1a.

The IF output signal is taken from terminal 'BP03' inside the tuner, via a 2.2-pF coupling capacitor. The braid of the output coax cable is again soldered directly to the tuner module to provide strain relief for the brittle capacitor. The other end of this coax cable is connected to an RF output socket (BNC or similar) fitted on the rear panel of the converter enclosure. The braid is also connected to the socket ground terminal. Again, TV coax can be used without problems since only short pieces are involved.

Power supply

The power supply for the converter is conventional, and consists of two parts; the 'regular' 12-V power supply, and the tuning voltage (0-30 V) supply. The unregulated voltage on C1 (approx. 35 V) is stepped down to 30 V by regulator IC1. This stabilized voltage is fed to the 100-kΩ multiturn tuning potentiometer (P1 in Fig. 5) via a 10-kΩ multiturn potentiometer (P2 in Fig. 5). The tuning voltage is taken from the wiper of P1. At a tuning voltage of 0 V (wiper turned to ground), the capacitance of the varicaps in the tuner module is maximum, and the tuner is tuned to 950 MHz (roughly). With the wiper

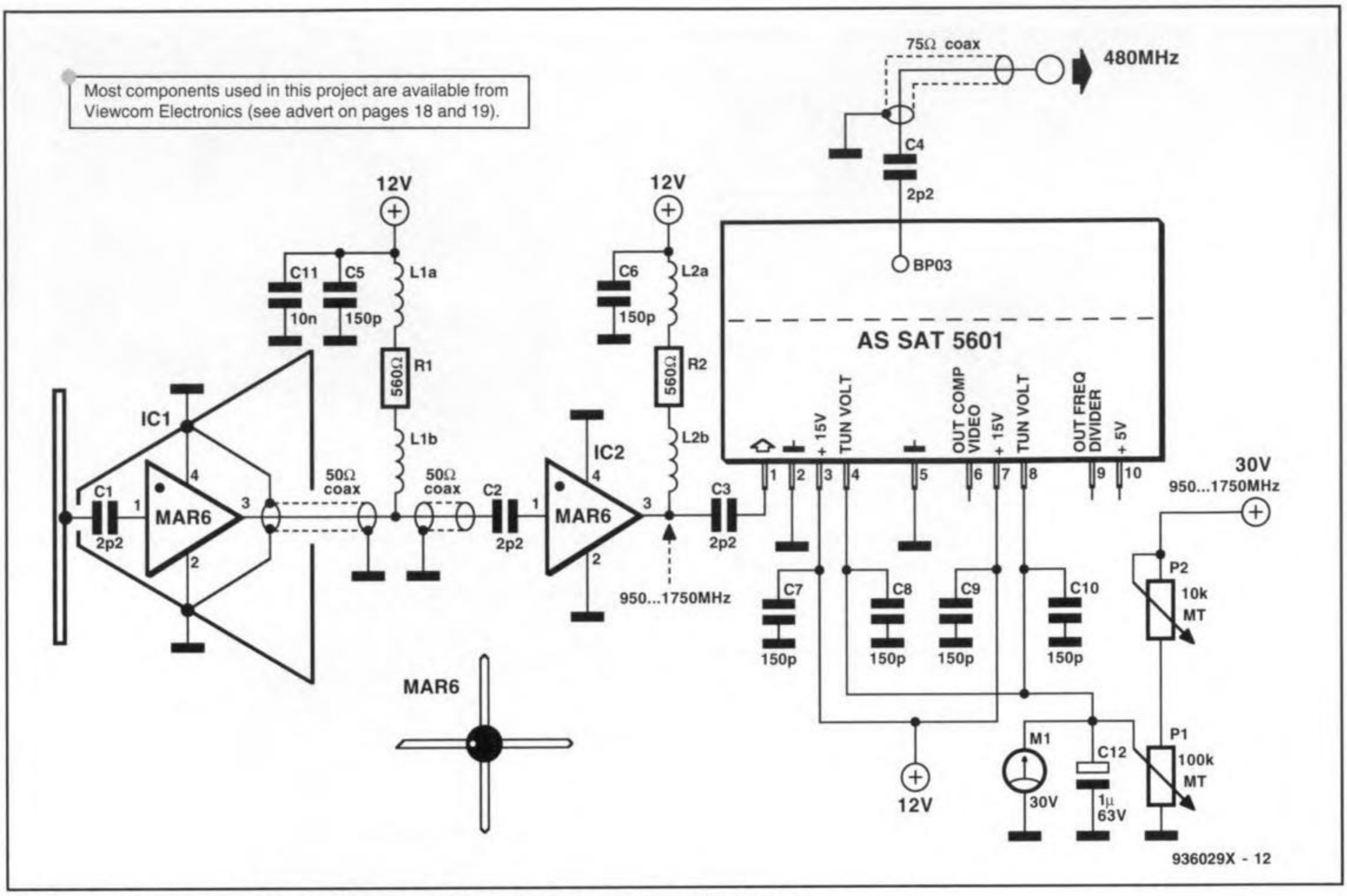


Fig. 5. Complete circuit diagram of the converter and the associated active antenna.

turned to the other extreme position, the capacitance of the varicaps is minimum, and the tuner is tuned to 1750 MHz. A voltage span of 30 V, therefore, covers a frequency range of about 800 MHz. The resulting tuning rate is quite large at 27 MHz per volt, and calls for a fine tuning even if a multiturn tuning potentiometer is used. That is the purpose of P1, which acts as a fine tuning control.

Alternatively, the frequency range of 950-1750 MHz may be divided into, say, ten small bands of about 80 MHz each. This is achieved by inserting a voltage divider with 2×10 taps between IC1 and the 100-kΩ potentiometer. This enables the fixed terminals of the tuning potentiometer to be taken to a pair of successive taps on the voltage dividers.

To suppress switching noises and 50-Hz hum, the tuning voltage is decoupled by a 1-µF electrolytic capacitor, C12, which is soldered between pin 8 of the tuner (+ side) and the tuner enclosure (ground). The wire that carries the tuning voltage from the wiper of P1 to tuner pin 8 should be kept well removed from the mains transformer. In case hum persists, try using screened wire.

The 12-V supply voltage for the tuner is obtained from a 7812 regulator (IC2) whose input voltage is stepped down by a zener diode, D1, to reduce the regulator dissipation. The current drawn from both supplies is relatively low (approx. 100 mA), so that heatsinks on IC1 and IC2 are not necessary. Finally, do not be surprised if you find that the zener diode drops about 0.6 V more than the specified 8.2 V — this is normal once this type of zener has reached its normal oper-

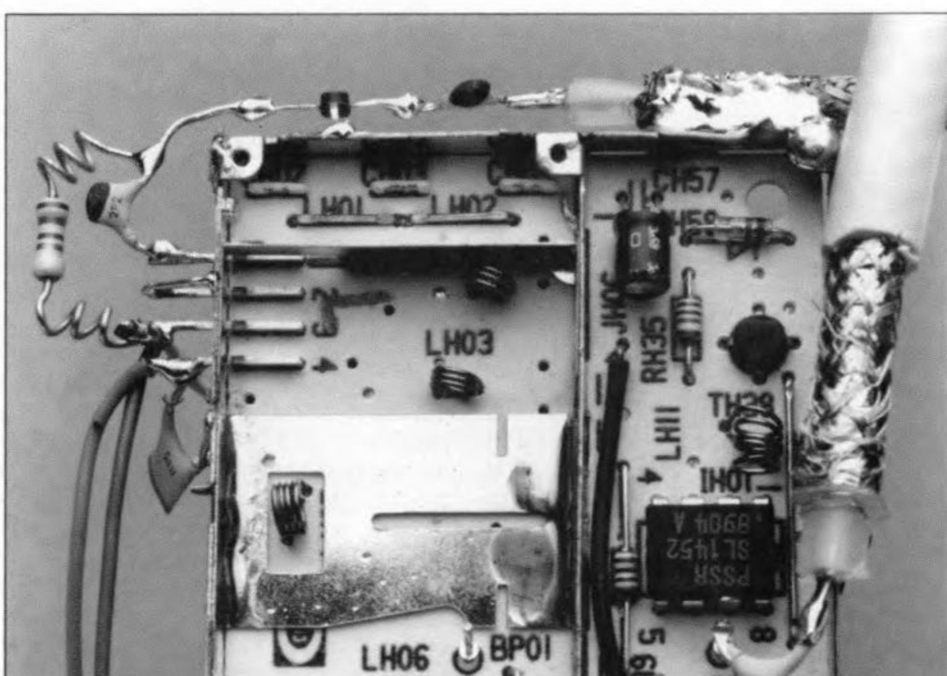


Fig. 6. Close up of the tuner module with the amplifier components fitted as external parts. Note that inductors L2a and L2b are made from the wires of resistor R2.

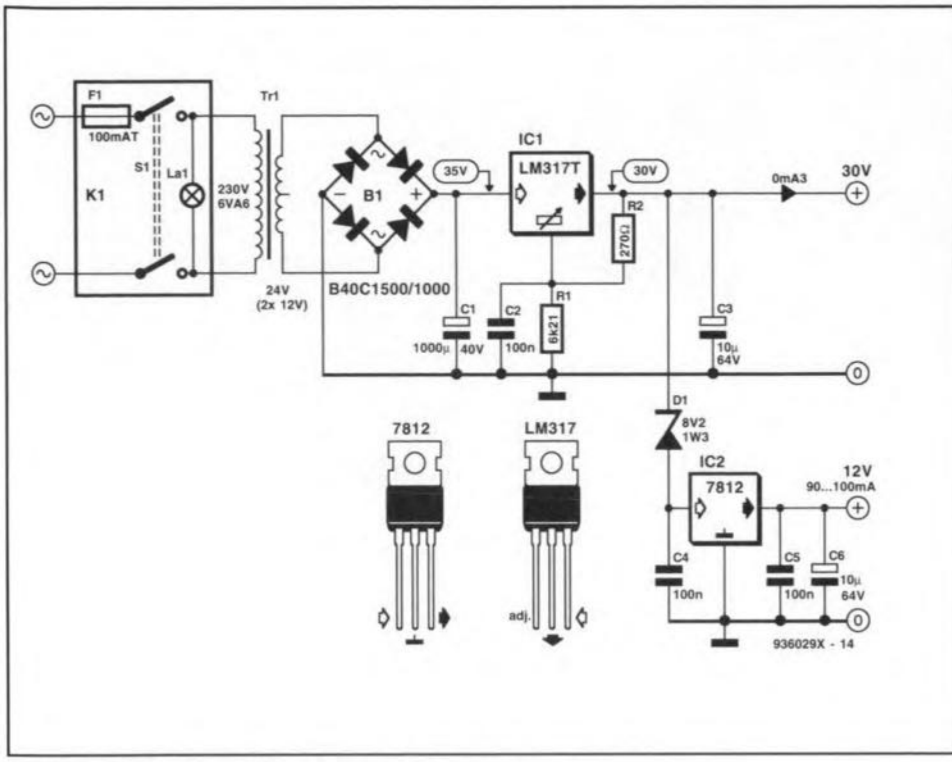


Fig. 7. Circuit diagram of the converter power supply.

ating temperature.

The power supply may be built on a UPBS-1 (universal prototyping board size-1) printed circuit board, which is available through our Readers Services. A suggested component arrangement on this board is shown in Fig. 8. For the sake of safety, the mains transformer is mounted on a separate piece of veroboard. The solder pins of the transformer and the two PCB terminal blocks (one for the mains side and one for the 24-V side) are inserted into the board, and soldered. Next, all copper within a distance of 1 cm of the pins is removed with a sharp knife. The mains pins of the transformer are connected to the terminal block pins using short pieces of sturdy, flexible, insulated wire. The same kind of wire is used for the connections between the terminal block, the mains switch and the mains appliance socket on the enclosure rear panel, as well as for the connection between the 24-V AC terminal block and the AC terminals of the bridge rectifier on the power supply board (Fig. 9). The transformer board is fitted on to the enclosure bottom panel with the aid of four 10-mm high plastic or nylon PCB pillars, and plastic or nylon screws and nuts. The wire connections on the mains switch and the mains appliance socket should be protected with small pieces of heat-shrink sleeving.

Converter assembly

Figure 10 shows the internal layout of our finished prototype. The enclosure used is quite large, offering plenty of space for extension circuits. Solder eyes are soldered to the four corners of the tuner modules. This allows the unit to be secured to the enclosure bottom plate using four sets of PCB pillars, screws and nuts. The ground connection between the tuner enclo-

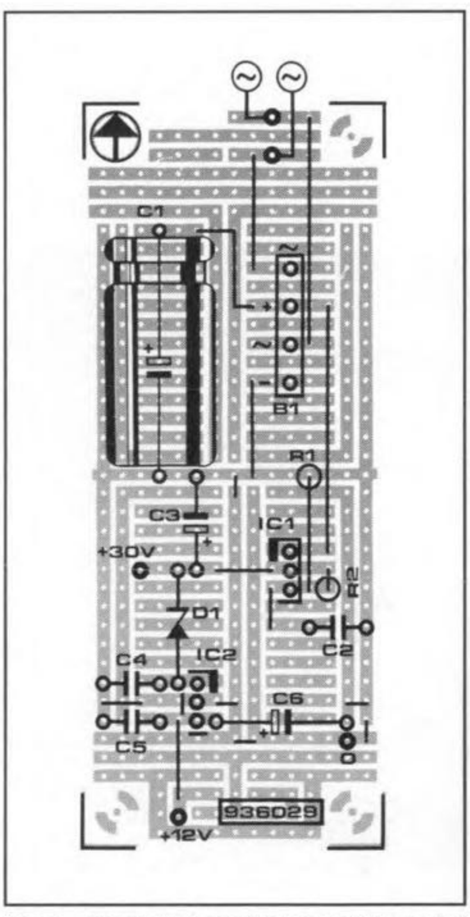


Fig. 8. Suggested component arrangement on the UPBS-1 board.

COMPONENTS LIST

CONVERTER PLUS ANTENNA

Resistors:

2	560Ω	R1;R2
1	10kΩ multiturn pot	P1
1	100kΩ multiturn pot	P2

Capacitors:

4	2pF2	C1-C4
6	100-150pF	C5-C10
1	10nF ceramic or MKT	C11
1	1µF 63V	C12

Inductors:

2	Choke; home-made, see text	L1;L2
2	MAR6*	IC1;IC2

Miscellaneous:

1 Satellite TV tuner module 950-1750MHz type AS SAT 5600 or AS SAT5601**

Length of 50Ω coax cable, or 75Ω TV coax

2 RF sockets and 2 plugs (see text)

CONVERTER POWER SUPPLY

Resistors:

1	6kΩ21 1%	R1
1	270Ω 1%	R2

Capacitors:

1	1000µF 40V	C1
3	100nF	C2;C4;C5
2	10µF 63V	C3;C6

Semiconductors:

1	B40C1500/1000	B1
1	8.2V 1.3W zener diode	D1
1	LM317T	IC1
1	7812	IC2

Miscellaneous:

1	Mains transformer 24V/350mA	Tr1
1	Mains switch with internal neon light	S1
1	Mains appliance socket with inegral fuseholder, plus 100mA(T) fuse	K1
1	30V moving-coil meter (see text)	M1
2	(optional) 2-way PCB terminal block 7.5m pitch	
1	(optional) board UPBS-1 (see page 78)	
1	Metal enclosure dim. approx. 80x250x180mm, e.g., Telet LC860**	

* MiniCircuit Labs USA. In the UK: Cirkit Distribution Ltd. (0992) 444111.

** C-I Electronics, P.O. Box 22089, 6360 AB Nuth, Holland. Fax: +31 45 241877.

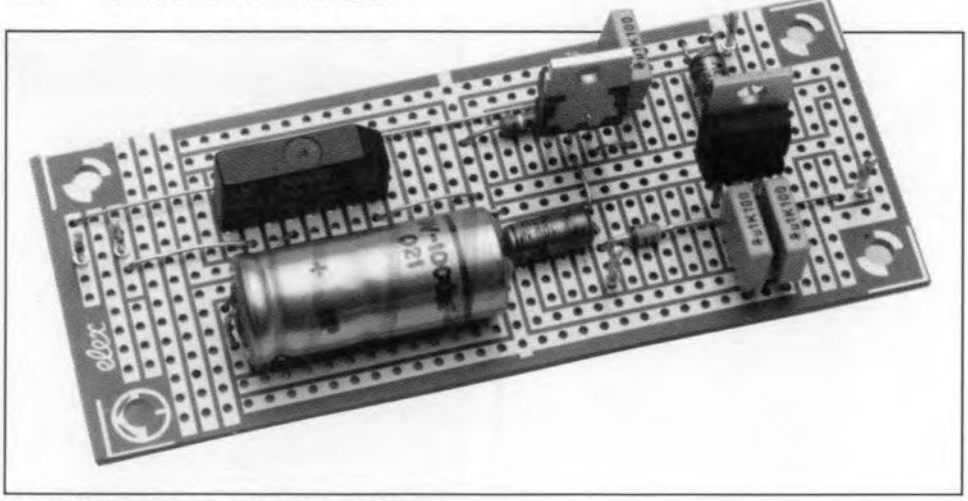


Fig. 9. Completed power supply board.

sure and the converter enclosure is established by the braids of the coax cables.

Suggested layouts for the front and rear panel are given in Fig. 11. The 30-V moving coil meter is provided with an appropriate tuning scale (Fig. 12) that gives a rough frequency indication. If a meter with a lower maximum voltage is used (e.g., 10 V), connect a 5 to 50 kΩ preset in series with the meter, and adjust it for full scale deflection at 30 V.

Wideband active SHF band antenna

Finding or designing a suitable antenna for the SHF converter is not easy because of two requirements: (1) a good wideband characteristic (800 MHz!), and (2) an omnidirectional reception pattern. This means that the loop yagi (familiar to radio amateurs active in the 23-cm band) is really out of the question. Unless, of course, the yagi is made for a specific frequency range, and is mounted on a rotor. The usable bandwidth of a home-made loop yagi is of the order of 50 MHz.

The antenna proposed here is a so-called discone type, which is a combination of a disc and a cone (Fig. 13). Just as with the more familiar dipole and ground plane antennas, the frequency range of the discone is determined by its size. Both the cone and the disc are cut from tin-plated sheet metal, or, for a more solid construction, from brass. The side of the cone has a length equal to ¼th the largest wavelength, while the diameter of the disc equals about ⅔rd the largest wavelength. The discone antenna is an unbalanced type, and has a feed impedance of 50-80 Ω. Assuming that the lowest frequency to be received is 1,000 MHz (1 GHz, wavelength 30 cm), the side of the cone is about 7.5 cm long (¼ × 30 cm), and the disc has a diameter of about 5 cm. Whereas these two dimensions determine to a large extent the lowest frequency at which he discone antenna can be used, they have a far smaller effect on the upper frequency limit. In fact, the theoretical highest/lowest frequency ratio of a discone antenna is 10:1. In practice, however, there will always be a few irregularities (dips) in the impedance characteristic over such a wide range. Also, the upper limit of 2 GHz assumed here is determined by the maximum input frequency of the antenna amplifier rather than the behaviour of the discone antenna.

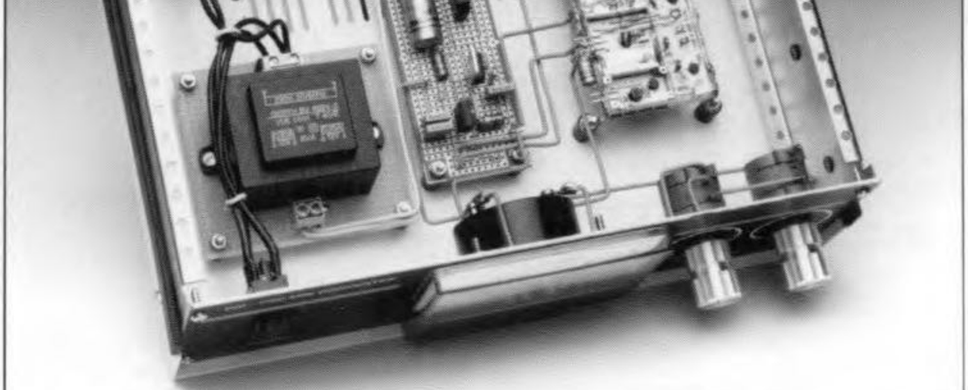


Fig. 10. A look into our completed prototype of the converter.

Active!

As already mentioned, the antenna for the 950-1750 MHz converter is 'active', i.e., it has an integral preamplifier. The preamplifier is a wideband type based on the MAR6 from MiniCircuits Laboratories. The prototype of the preamplifier is shown in Fig. 14. The MAR6 is fitted on a small piece of veroboard, which is (temporarily) secured inside the cone with the aid of ground wires. The input of the preamplifier is formed by the wire of the 2.2-pF capacitor. This wire is soldered to a short piece of thick copper wire which is inserted into the hole in the centre of the disc. In this way, the disc is held at a distance of 2 mm above the top of the cone. To enable the preamplifier board to be fitted as far up in the cone as possible, you may want to cut or file its top end into an angle of about 60°. The 2.2-pF capacitor serves to isolate the MAR6 input from ground. If you are able to give the disc solid isolation from the cone (for instance, by using a Teflon bush made to measure), the input capacitor may be omitted, and the disc connected to the MAR6 input by a short piece of thick copper wire.

The masthead preamplifier is powered via the downlead coax cable. The 12-V supply voltage is obtained from the converter.

Cutting and bending

Before tackling the construction of the discone antenna, you are well advised to practise on pieces of cardboard. Figure 15 shows the dimensions of the parts that make up the antenna: one tin-plate disc with a radius of 30 mm, and one half of a larger, 100-mm radius, disc. Use calipers to mark the two circles (30 mm and 100 mm radius) on the tin-plate (or brass) sheet. Next, the discs are cut out using plate shears. Drill a 2-mm hole in the centre of the small disc, and a 20-mm hole in the centre of the large disc. Next, cut the large disc into two (Fig. 15). One half is formed into a cone. This is done with the aid of a 10-mm dia. wooden stick clamped into a vise. Put the hole

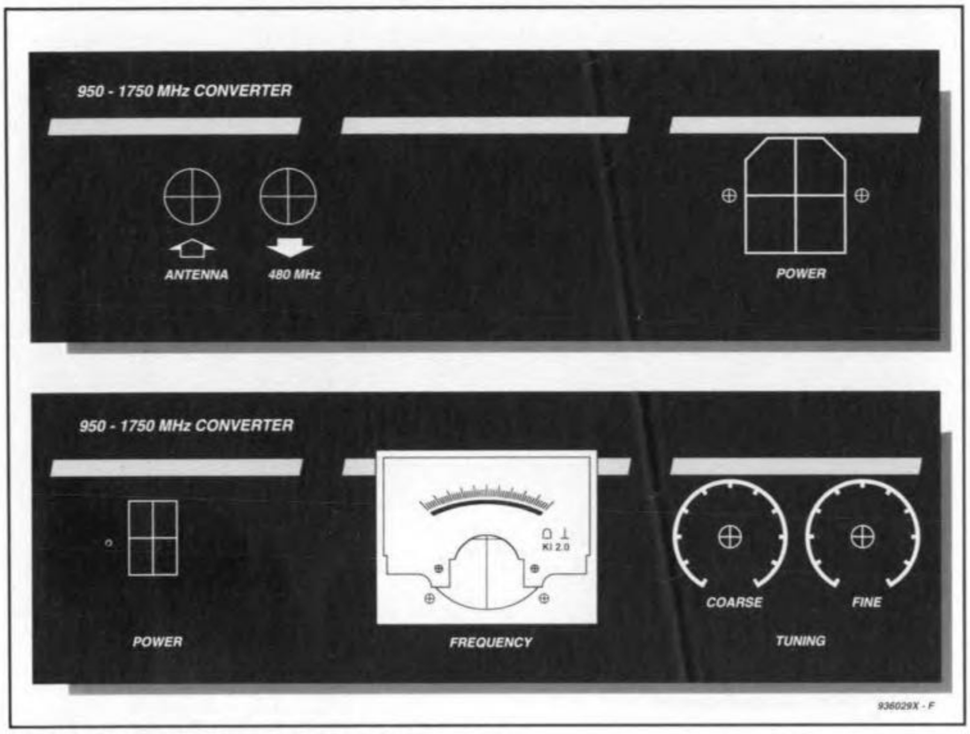


Fig. 11. Suggested front and rear panel layouts.

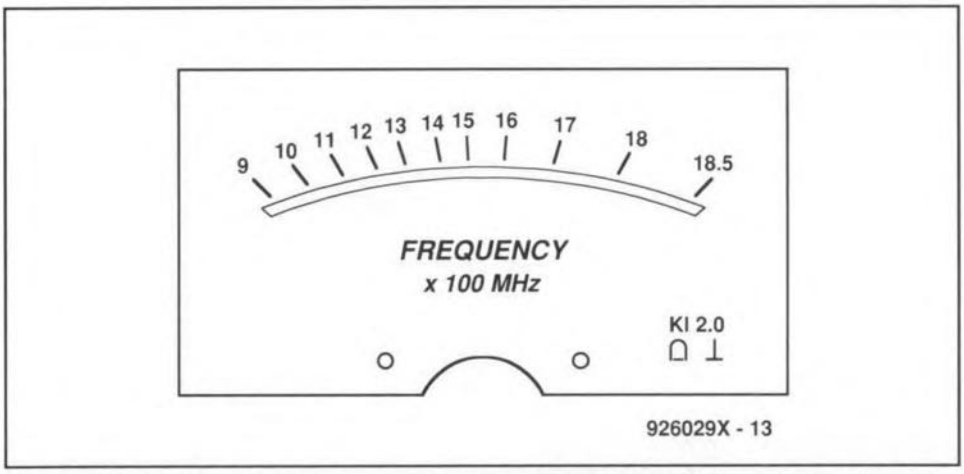
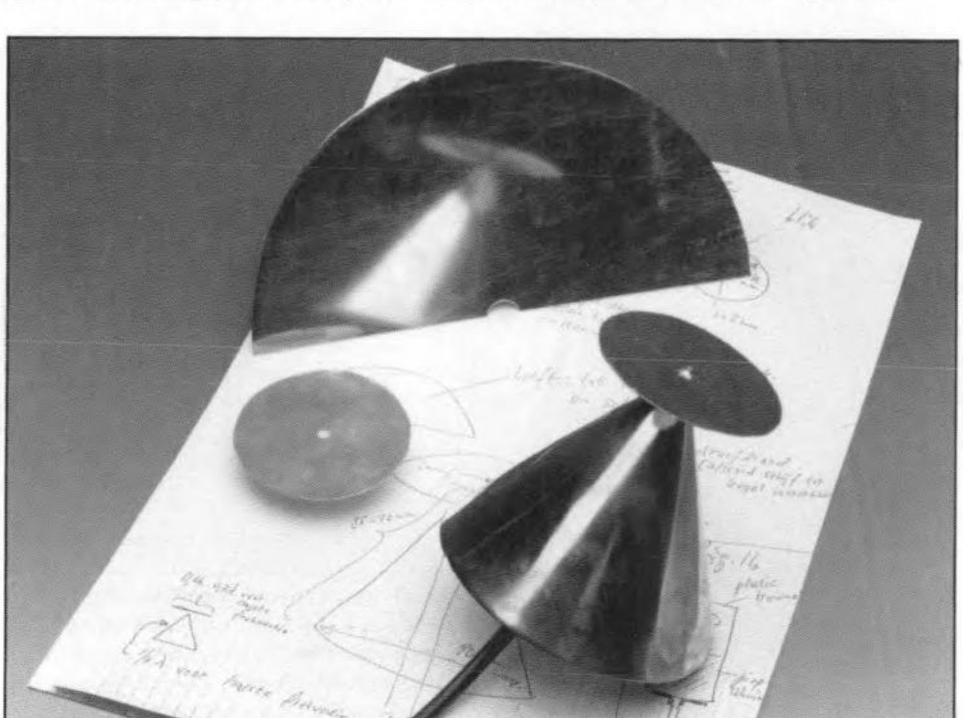


Fig. 12. This tuning scale is easily used to replace the scale card in the moving coil meter.



in the half disc over the stick. The cone shape is achieved by turning the plate material around the stick, and carefully bending the material until the ends meet. The lower rim of the cone is fairly easily shaped. To make sure that the top end is also round, the wooden stick has to be replaced, at a certain moment, by a thinner (metal) pin, for instance, a thick screwdriver bit. Since the tin plate at the top of the cone will become more difficult to bend into shape as the 'circle' starts to close, you will find it necessary at some time to apply a little more force using a plastic or rubber hammer.

Once the shape of the cone is satisfactory, the edges of the tin plate material are pressed together and joined by soldering over the full length of the seam. Next, the cone is finished by filing always burrs, and rounding the 10-mm hole at the top. The preamplifier board is carefully mounted inside the cone (Fig. 15), and the side wires (ground) are soldered to the tin plate. Insert the preamplifier input wire into the hole in the disc. Position the disc so that it is at a distance of about 2 mm above the cone, and solder the wire in the centre hole.

Once the preamplifier board and the disc are firmly in place, it is recommended to strengthen the ground connection at the top of the board by soldering it to the inside of the cone.

If you happen to live high up in a block of flats, the discone antenna requires no further finishing, and may be placed on a window sill. In all other cases, the unit must be fitted out of doors, and has to be protected against the weather. One way of doing this is to fit the antenna into a plastic box, for which a suggested construction is shown in Fig. 17. The underside of the box is secured to a metal pipe which allows the unit to be mounted to an antenna mast. The box is best sealed with acid-free silicone compound as used for aquariums. To avoid it being corroded by condensation, the antenna rests on a polystyrene block cut to fit in the box. Alternatively, glue a plastic rod inside the box. The rod is drilled to pass the downlead coax, and serves to support the mini discone antenna

Finally, if the downlead cable is relatively long, it is recommended to use a MAR8 instead of a MAR6 in the preamplifier to compensate the higher cable loss between the antenna and the converter. The MAR8, however, requires an input impedance of exactly

Fig. 13. A discone antenna consists of a disc and a cone. Here, the parts are shown before and after assembly.

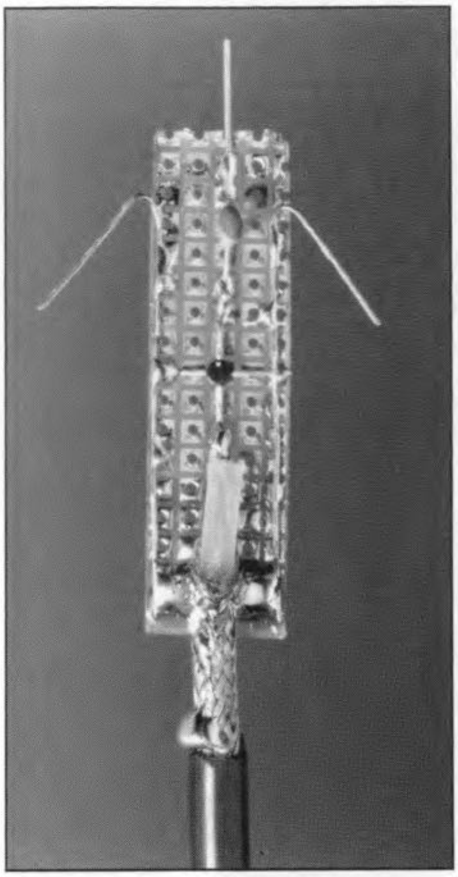


Fig. 14. Believe it or not, but the two components on the board form a wideband preamplifier for use with the discone antenna. The wires at the sides of the board serve to temporalily secure the unit inside the cone.

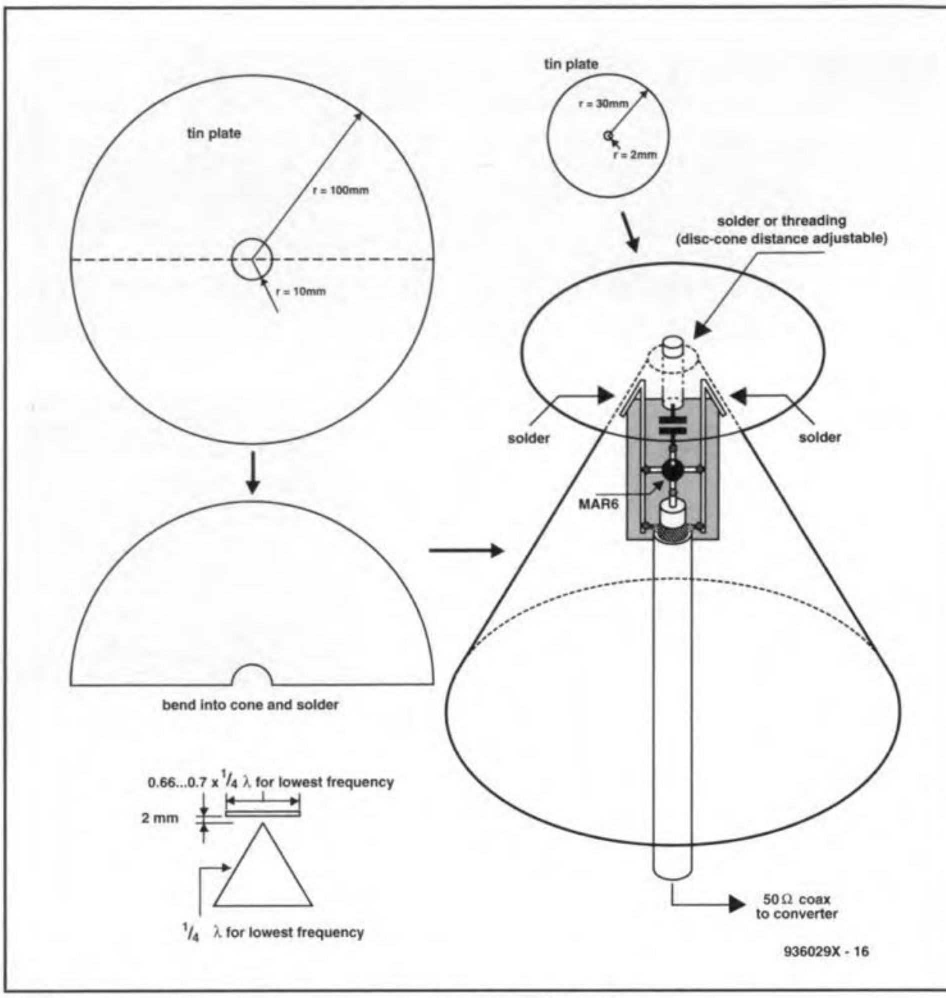


Fig. 15. Discone antenna dimensions and construction details.

50 Ω, which can only be achieved by making the distance between the disc and the top of the cone adjustable. Failing to adjust the input impedance to 50 Ω may cause the MAR8 preamplifier to start oscillating. ■

References:

1. VHF/UHF receiver. *Elektor Electronics* May 1993.

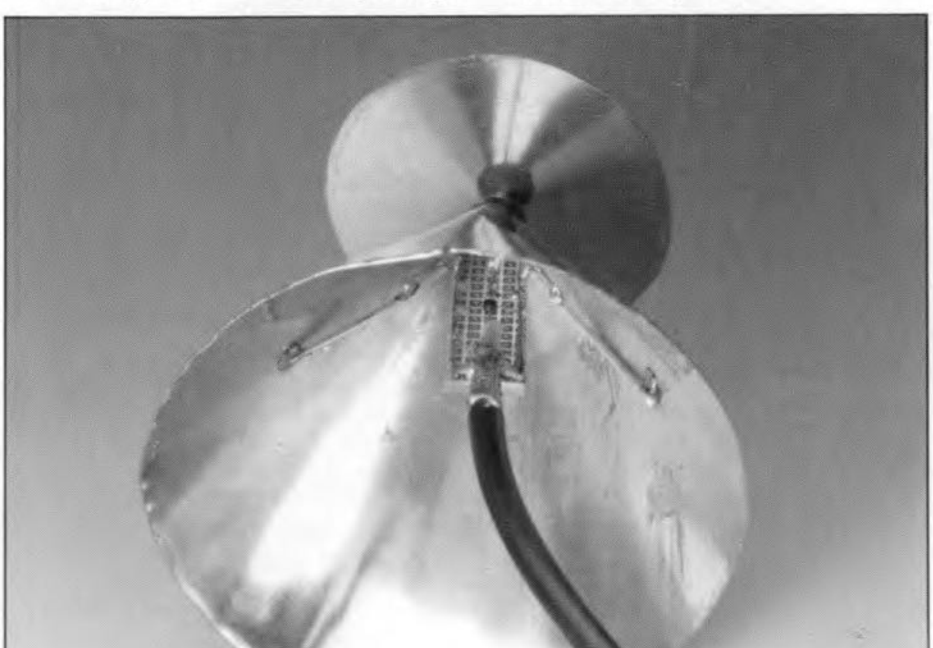


Fig. 16. The preamplifier board is temporarily secured in the top of the cone using two wires. Later, the top of the board is soldered flush to the cone, and the wires are removed.

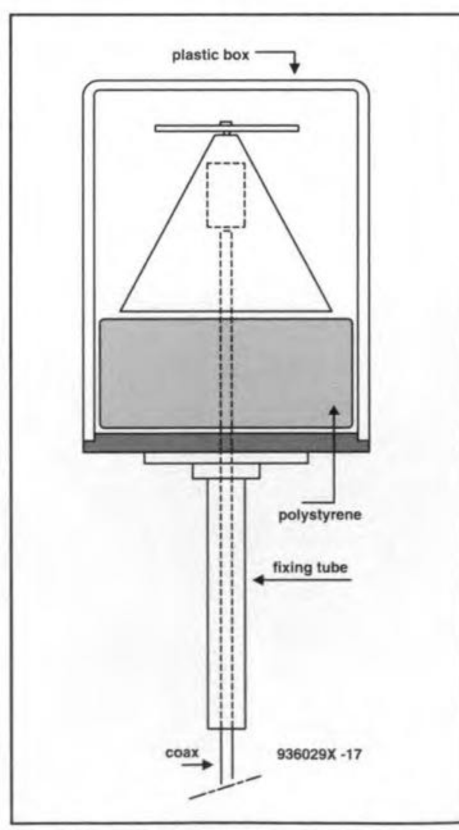
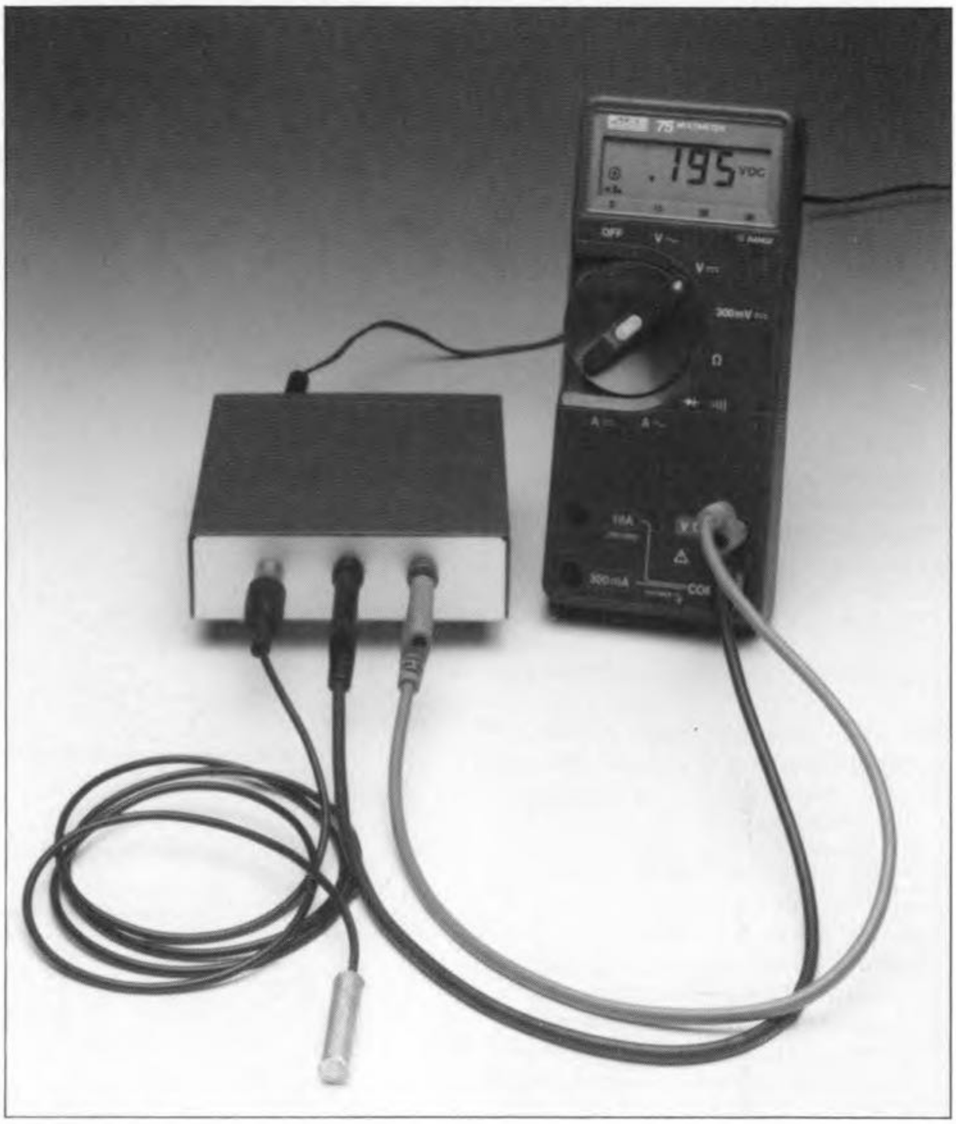


Fig. 17. In nearly all cases, the discone antenna has to be mounted out of doors to ensure good reception of SHF signals, which travel virtually by line of sight. Here, a suggested construction is shown to protect the unit from the weather.

LINEAR TEMPERATURE GAUGE

Design by H. Kühne



Temperature may be measured electronically with commercially available temperature-to-voltage converters. Since good-quality, calibrated ones are normally not cheap, the linear temperature gauge described uses an inexpensive silicon transistor as sensor.

Semiconductor silicon may be used as a temperature sensor to cover a range of roughly −50 °C to +150 °C. Indeed, apart from complete ICs that have been designed for measuring temperature, there are also special semiconductor temperature sensors on the market. They all make use of the temperature coefficient of n-doped silicon. The characteristic of sensors made from this material is more or less exponential and must, therefore, be made linear. Unfortunately, the linearity provided by a number of integrated sensors is not good enough for many applications. Problems may also arise when the operator wants to use a different sensor with the temperature gauge, because this is calibrated with its original sensor.

These drawbacks are overcome by a different approach as used in the present transducer. This uses a conventional silicon transistor as sensor. The transducer has good linearity and allows replacement of the sensor without the necessity of recalibration.

Theoretical considerations

The fact that the temperature of a silicon wafer affects the potential across the wafer is used in countless applications. It is, however, often overlooked that the relationship of −2 mV K^{-1} applies only over a limited temperature range and even then with a certain accuracy only. This becomes clear from the formula for the junction voltage:

$$U_d = E_g/Q - Tk/Q \log_e(AT^n/I_F), \qquad [V]$$

where U_d is the junction voltage; E_g is the energy gap, that is, the distance between the valence band and the conduction band of the semiconductor material; Q is the elementary charge of 1.602×10^{-19} C(oulomb); k is the Boltzmann constant (1.38×10^{-23} J K^{-1}); T is the temperature; A is a factor that depends on the geometry of the wafer; $n = 3$ in a p-n junction in silicon; and I_F is the forward current through the junction. For a junction in silicon, $E_g/Q \approx 1.1$ V.

It follows from this formula that there is a linear relationship between junction voltage and temperature only if the forward current also increases at a power n: the quotient T^n/I_F is then constant. When a constant current flows through a p-n junction, the drift dU_d/dT, that is, the drift of the temperature coefficient, is of the order of −450 ppm K^{-1}. The drift is given by:

$$d^2U_d/dT^2 = -k(n/TQ). \qquad [V\ K^{-2}]$$

Example: the absolute measurement error of a linear temperature gauge resulting from the instability of the temperature coefficient rises to over 0.5 °C when measurements are taken in the range −20 °C to +120 °C. This practical value applies when the display (or the transfer) of the measuring system is calibrated on the basis of the difference in forward voltage at 0 °C and +100 °C.

This shows that, in spite of the many claims to the contrary, an improvement in linearity cannot be achieved by a constant-current source. It is far better to

Brief parameters

Power supply	6–12 V (current drain at 9 V is 15 mA)
Measuring range	−20 °C to +120 °C
Sensitivity	10 mV °C^{-1}
Reaction time	<5 seconds
Sensor influence	<0.2 °C
Stability	±0.01 °C
Measurement error (full scale)	<0.2 °C
Sampling frequency	270 Hz
Power up delay	10 seconds

generate the current with an ideal voltage source and series resistor. As stated earlier, the threshold voltage at the p-n junction drops when the temperature changes. Because of this, the current through the junction rises, resulting in an improvement of the linearity. Assuming a resistance of 10 kΩ and a supply voltage of 10 V, the drift is about –400 ppm K^{-1}.

Constant A, which depends on the type as well as the model of semiconductor device, causes a certain spread of the voltage drop across the p-n junction and of the static temperature coefficient (dU_d/dT). This explains why after an exchange of sensor the gauge must be recalibrated. Thermometers that can operate with a number of sensors have a calibration point for each of them.

Much better results are obtained with the dynamic sensor concept. In this, use is made of the temperature dependence of the differential resistance r_d ($= dU_d/dI_F$) to determine the temperature of the p-n junction. From this and differentiation of the formula for U_d, it follows that:

$$r_d = kT/QI_F. \qquad [\Omega]$$

This equation throws up a number of interesting points. For instance, the differential resistance is directly proportional to the temperature of the p-n junction. Also, the slope of the characteristic is determined by constants k and Q, and the forward current through the junction. Moreover, E_g and A no longer play a role. It is clear that the differential resistance is in no way dependent on the geometry of the crystal, the production process and the material of the p-n junction. It should be borne in mind, however, that this is a theoretical approach: there are differences between theory and practice. One of these is caused by the self-resistance of the semiconductor material which so far has not been taken into account.

Experiments based on the theoretical considerations showed that a high-current-gain (β) RF transistor, used as a diode, would perform excellently. Note that the loss resistance, $R_{bb'}$, in this case is reduced by a factor β.

To ensure that the base resistance can really be ignored, it is vital that the bias current for the diode is small. Although a spread of $R_{bb'}$ has no influence on the temperature coefficient, it does affect the measured voltage across the diode. In other words, a spread in this resistance causes a static offset of the measured value indicated by the gauge.

To keep the hardware as simple as possible (which makes it easier to reproduce), the small-signal theory for semiconductors considered so far must be abandoned. It then becomes possible to derive the dynamic temperature coefficient from the general formula for the junction voltage:

$$U_d = E_g/Q - Tk/Q \times \log_e(AT^n/I_F). \qquad [V]$$

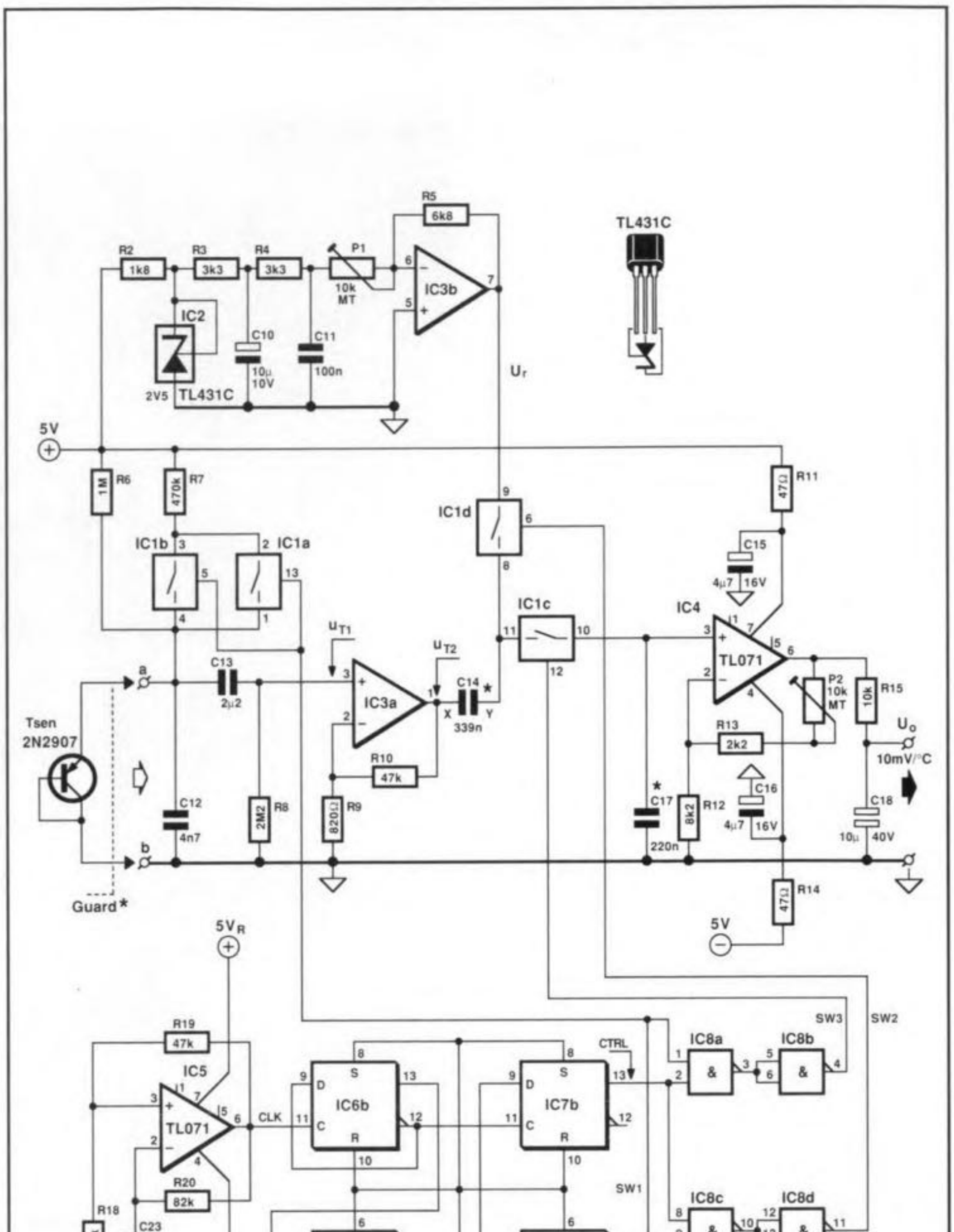


Fig. 1. Circuit diagram of the linear temperature gauge.

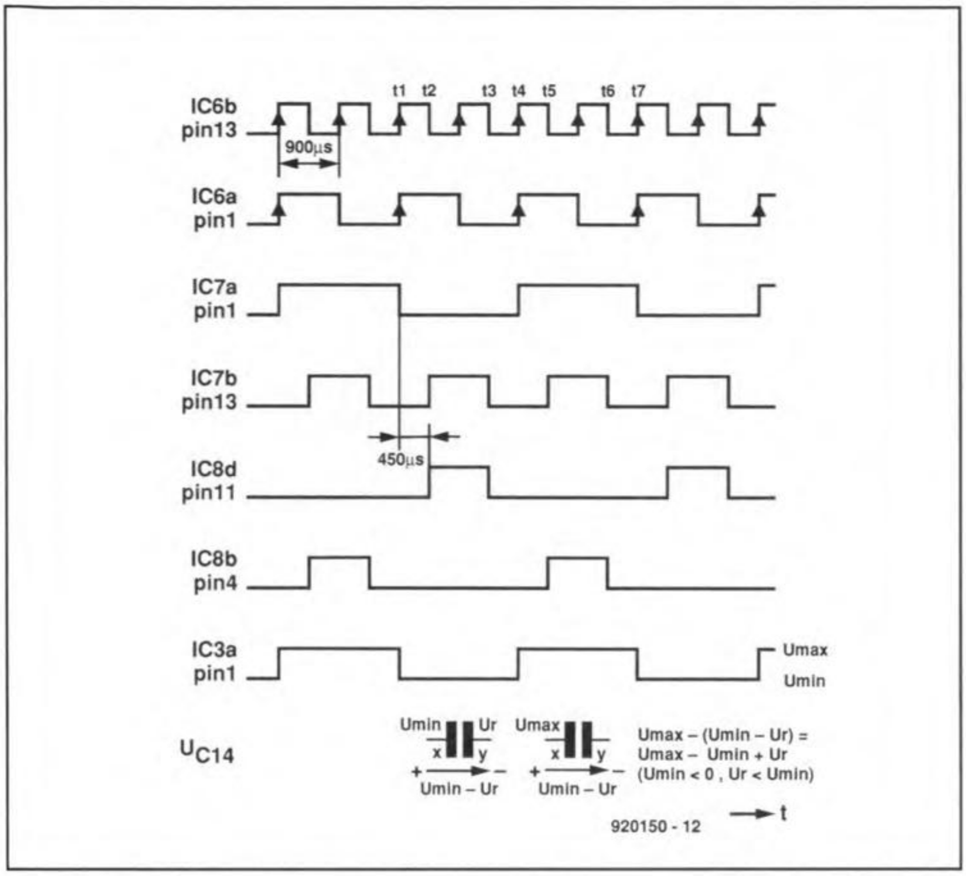


Fig. 2. Timing diagram of the linear temperature gauge.

$$\Delta U_d = Tk/Q \times \log_e(I_{F2}/I_{F1}). \qquad [V]$$

This defines the change in voltage across the p-n junction as a function of the change in current.

The dynamic temperature coefficient is given by:

$$d\Delta U_d/dT = k/Q \times \log_e(I_{F2}/I_{F1}). \qquad [V\,K^{-1}]$$

An important consequence of this equation is that all that is needed is a constant ratio of the two currents.This may be achieved without too much trouble.

The practical circuit

The circuit as shown in **Fig. 1** may be used to cover a temperature range of –20 °C to +120 °C. Its output is a direct voltage that changes linearly with temperature: the conversion factor is 10 mV °C^{-1}.

The sensor, T_{sen}, is a Type 2N2907 transistor, preferably in a metal case, because in this type the thermal contact between housing and p-n junction is appreciably better than in types housed in man-made fibre cases. This makes it possible for rapid temperature changes to be observed. The base and collector are interconnected close to the body of the device, which is then linked to the measuring unit with two-core screened cable. It is recommended to fit (with superglue or similar) the transistor in one of the ends of a short length of metal tube. Make sure with suitable sleeving that the terminals of the transistor are well insulated from each other.

The design of the measuring unit makes the temperature-to-voltage conversion insensitive to changes in temperature. Also, the design lends itself to use with long connections to the sensor: parasitic capacitances cannot cause measurement errors.

Operational amplifier IC_5 serves as the central clock. Its output is a rectangular signal whose exact frequency and shape do not affect the operation of the circuit. The frequency is set to 2.22 kHz by network R_{20}-C_{23}.

Bistables IC_6 and IC_7, and the NAND gates in IC_8, derive the necessary signals from the clock to switch the collector current of the sensor between two values.

The non-overlapping clock signals are also needed for the measurement amplifier based on IC_3 and IC_4.

The Q output of D-type bistable IC_{7a} controls parallel-connected electronic switches IC_{1a} and IC_{1b}. When these are both actuated, resistors R_6 and R_7 are in parallel. Collector current I_{F2} then flows through T_{sen}. When during the next half period the switches are open, the current through T_{sen} drops to I_{F1}. This current is determined solely by R_6, not by the combination of this resistor and R_7. With a supply of 5 V, the on-resistance of the parallel-connected switches is about 60 Ω. This is negligible compared with the value of R_7, which means that the ratio of the two currents is

$$I_{F2}/I_{F1} = R_6/(R_6 // R_7).$$

From this it may be computed that the sensitivity of the sensor is 98.2 µV K^{-1}.

Strictly speaking, currents I_{F2} and I_{F1} are also determined, to a very small degree, by the level of the forward voltage of T_{sen}. Since this voltage is a function of the forward current and the temperature, it is to be expected that a temperature-dependent drift of the ratio between the two currents occurs. The instability of the temperature coefficient, $d\Delta U_d/dT$, that arises in the forward direction has been computed with a simulation program (PSPICE*) and was found to be about –18 ppm K^{-1}. The measurement error caused by this over the range –20 °C to +120 °C does not exceed 0.1 °C. This is an acceptable error: the cost of an additional current source to (partly) eliminate it is out of all proportion with the possible improvement.

The rectangular signal, ΔU_d, across T_{sen}

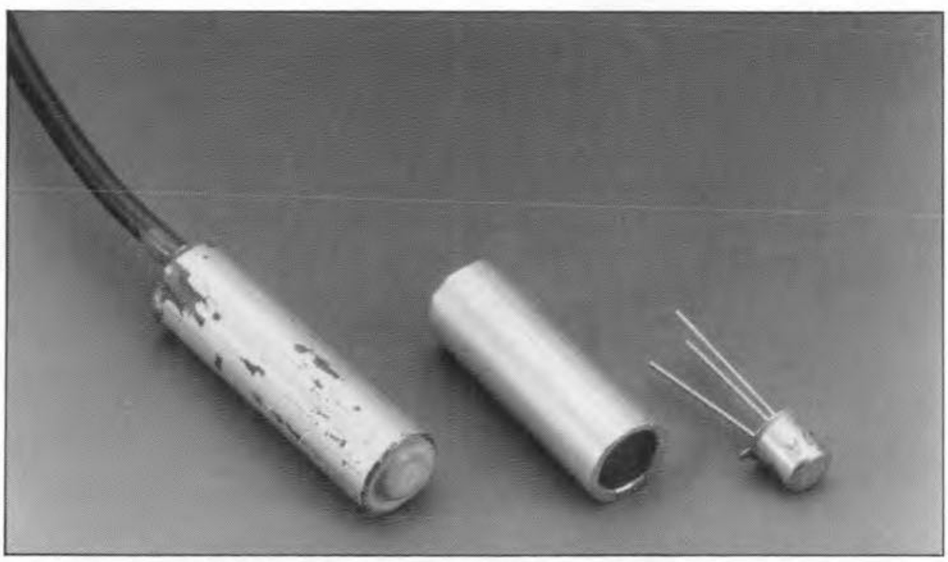


Fig. 3. Three stages in the construction of the sensor.

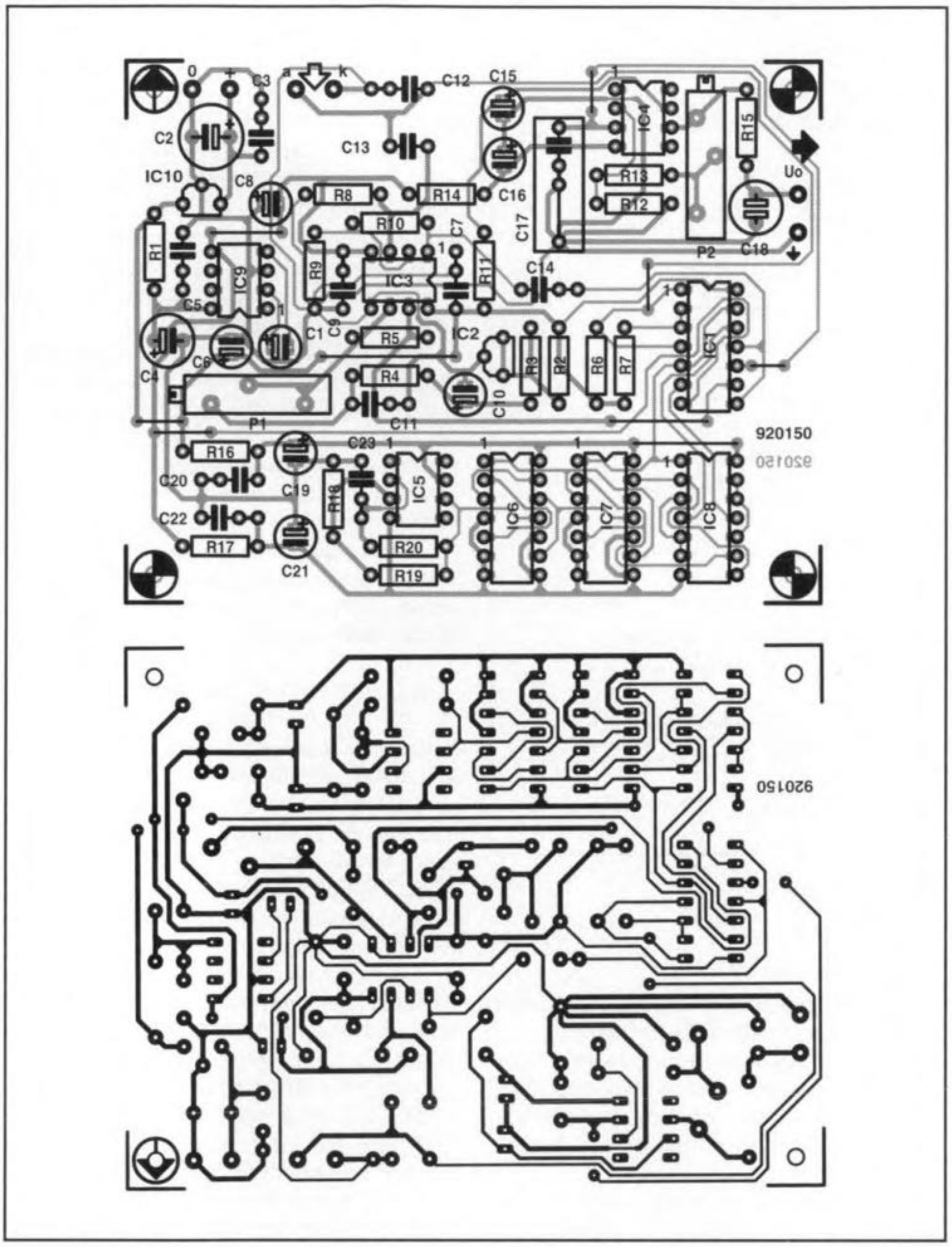


Fig. 4. The printed-circuit board for the linear temperature gauge.

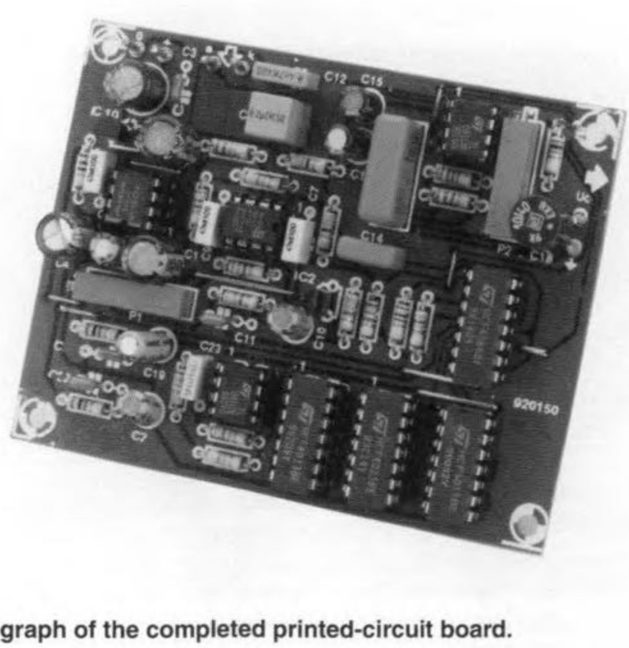


Fig. 5. Photograph of the completed printed-circuit board.

PARTS LIST

Resistors:
R1 = 10 Ω
R2 = 1.8 kΩ
R3, R4 = 3.3 kΩ
R5 = 6.8 kΩ
R6 = 1 MΩ
R7 = 470 kΩ
R8 = 2.2 MΩ
R9 = 820 Ω
R10, R19 = 47 kΩ
R11, R14 = 47 Ω
R12 = 8.2 kΩ
R13 = 2.2 kΩ
R15 = 10 kΩ
R16, R17 = 100 Ω
R18 = 18 kΩ
R20 = 82 kΩ
P1, P2 = 10 kΩ multiturn preset

Capacitors:0.5 pt
C1 = 47 µF, 16 V, radial
C2 = 100 µF, 16 V, radial
C3, C11, C20, C22 = 100 nF
C4 = 100 µF, 10 V, radial
C5, C7, C9 = 47 nF
C6, C19, C21 = 10 µF, 16 V, radial
C8 = 47 µF, 10 V, radial
C10 = 10 µF, 10 V, radial
C12 = 4.7 nF
C13 = 2.2 µF
C14 = 33 nF, polypropylene
C15, C16 = 4.7 µF, 16 V, radial
C17 = 220 nF, polypropylene
C18 = 10 µF, 40 V, bipolar, radial
C23 = 4.7 nF

Semiconductors:
IC1 = 4066
IC2 = TL431C
IC3 = TL072
IC4, IC5 = TL071
IC6, IC7 = 4013
IC8 = 4011
IC9 = ICL7660
IC10 = LP2950CZ-5.0
T_{sen} = 2N2907

Miscellaneous:
Enclosure 100×100×30 mm
(4×4×1$^{3}/_{16}$ in)
PCB No. 920150 (see p. 78)

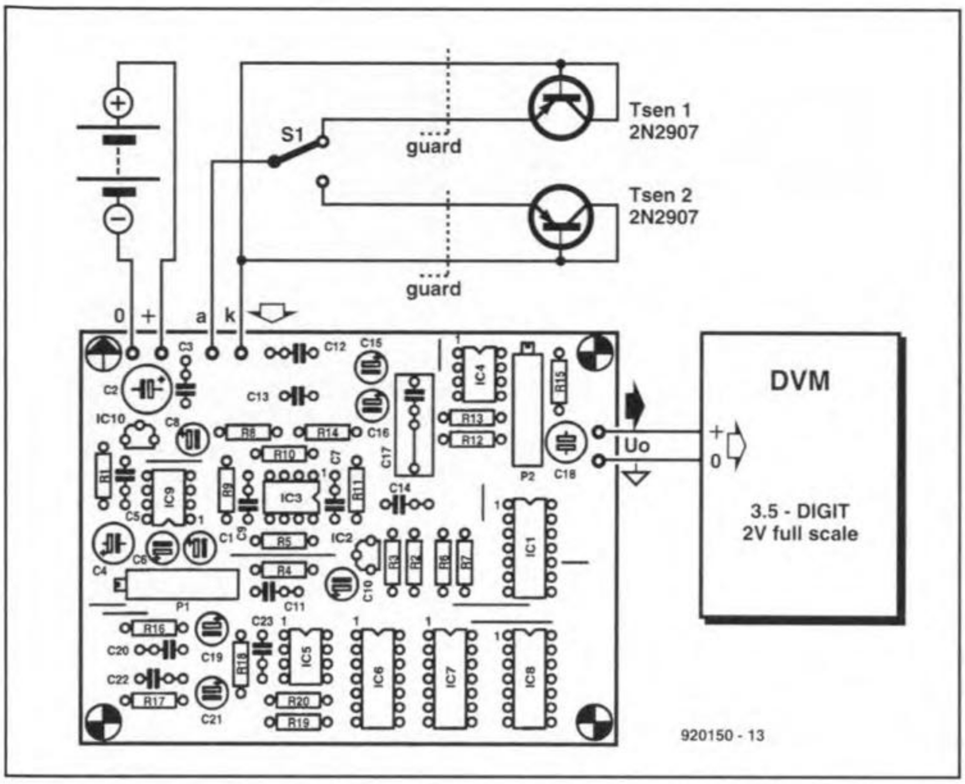


Fig. 6. The temperature gauge may be controlled by two switch-selected sensors.

is applied to IC_{3a} via C_{13}. The amplification of this opamp is determined by R_9 and R_{10}: with the values of these resistors shown it amounts to ×58.3. Correction of the offset voltage of the opamp is not needed, since the following components eliminate the ensuing error automatically. In other words, the amplification applies to alternating voltages only.

The remainder of the signal processing is carried out by IC_4 and analogue switches IC_{1c} and IC_{1d}. These switches function as a synchronous demodulator. This means that the measument amplifier functions as a differential amplifier, so that output voltage U_0 changes in direct proportion to the temperature, in °C, of the p-n junction.

The operation of the measurement amplifier, which does not experience drift, is explained best on the basis of the timing diagram in **Fig. 2**. At time t_1, the current drops from 14.1 µA (I_{F2}) to 4.5 µA (I_{F1}). As a consequence the potential across the sensor drops. This means that the output voltage of IC_{3a} (U_{t2}) drops to the lowest measuring level, U_{min}. This voltage becomes stable at time t_2, when the output of IC_{8b} closes analogue switch IC_{1d}. This action causes C_{14} to be connected to the negative reference voltage, U_r, at the output of IC_{3b}. During time interval t_2–t_3, this capacitor is charged to the potential difference between the outputs of IC_{3a} and IC_{3b}. At time t_3, switch IC_{1d} is opened again and the charge on C_{14} is retained.

At t_4, the current through the sensor is set to its maximum value. After a brief period, the output voltage of IC_{3a} then reaches its maximum value, U_{max}.

At t_5, the output voltage of IC_{8b} actuates analogue switch IC_{1c}. This results in C_{17} being charged to a direct voltage that, after a few cycles, is equal to the output voltage of IC_{3a} less absolute reference voltage U_{17} (= $U_{max}-U_{min} + U_r$). Put differently, the output voltage of IC_{3a} is equal to $A_1\Delta U_d$, where A_1 is the amplification of the opamp. This voltage is raised by one more amplifier stage, so that the final output voltage, $U_o = A_2(A_1\Delta U_d + U_r)$. Amplification factor A_2 may be set between 1.27 and 2.48 with P_2.

Negative reference voltage U_r is derived from IC_2 by IC_{3b}. At temperature T=273.15 K (0 °C), the reference zener diode must provide a voltage, U_r, of

$$U_r = -kT/Q \log_e(I_{F2}/I_{F1})A_1 = -1.57 \text{ V}.$$

Preset P_1 serves to set the zero of the t/U converter, and P_2 to calibrate the output voltage.

Atmospheric pressure (mbar)	Boiling point of water (°C)
910	97.0
920	97.3
930	97.6
940	97.9
950	98.2
960	98.5
970	98.8
980	99.1
990	99.4
1000	99.6
1010	99.9
1013.25	100.0
1020	100.2
1030	100.5
1040	100.7
1050	101.0
1060	101.3

Boiling point of water relative to atmospheric pressure.

Construction

The circuit is best constructed on the printed circuit board shown in **Fig. 4**. The completed prototype is illustrated in Fig. 5. The design of the board ensures that the influence of the digital part (IC_5–IC_8) on the analogue part (IC_1–IC_4) is minimized. The power lines are decoupled by low-pass filter R_{16}-R_{17}-$C_{19\text{-}22}$.

Since the control signals for the analogue section derive from the digital section, the relevant tracks are surrounded by reference tracks to minimize the influence of digital signals on capacitors C_{14} and C_{17} (which would degrade the accuracy of the measurement).

Start populating the board with the wire bridges, followed by the passive components, and finally the ICs.

Connect the sensor to the completed board with two-core microphone cable (100 pF m^{-1}). Screened cable is essential to effectively suppress the 50 Hz (mains) hum.

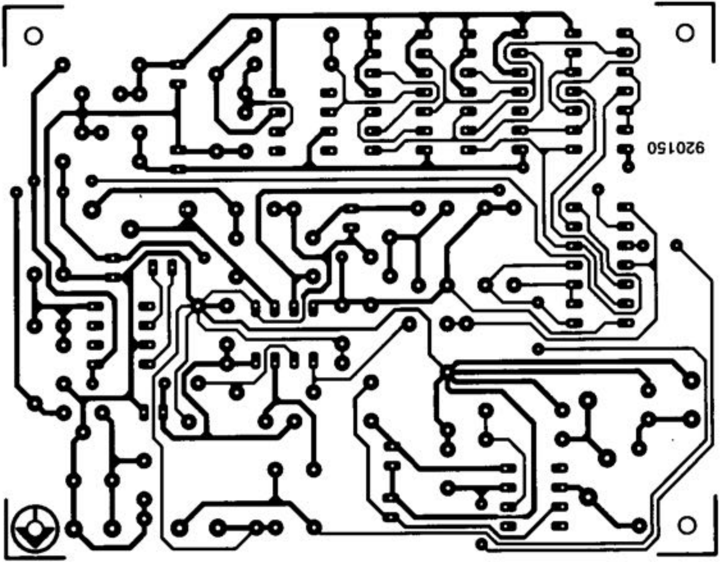
For calibrating the circuit, it is best to use a $3^1/_2$ digit multimeter with a full-scale deflection (f.s.d.) of 2 V.

The zero of the meter is set with the sensor immersed in a well-stirred mixture of water and crushed ice. The temperature of this mixture is 0 °C. Set P_1 to obtain a meter reading of exactly 0.00 V.

Next, immerse the sensor into boiling water (which has a temperature of 100 °C at the standard atmospheric pressure of 1013.25 mbar—see table). Adjust P_2 to obtain a meter reading of 1.00 V.

If the calibration is carried out accurately, the measurement error over the temperature range −10 °C to +120 °C does not exceed ±0.15 °C. The use of different types of transistor had no noticeable effect on the correct operation of the prototype. However, if transistors are used whose amplification factors fall into different groups (A, B or C), the relative measurement error may increase to ±0.2 °C. **END**

* PSPICE is a derivative of SPICE (Simulation Program with Integrated Circuit Emphasis) developed at Berkeley University, California. It is produced by MicroSim Corporation of California and is available from a number of computer software dealers.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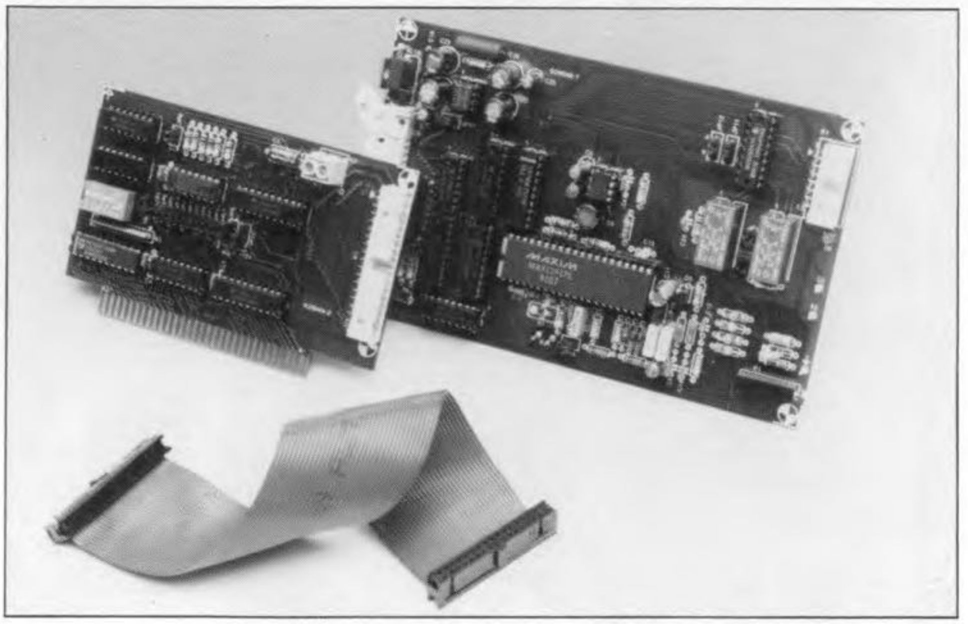
FUZZY LOGIC MULTIMETER (PART 1)



AUTORANGING, WITH SOFTWARE CONTROL FOR FUZZY LOGIC APPLICATIONS

Together with the associated software, this circuit is not only a 3¾-digit PC-controlled digital multimeter (DMM) with a plethora of bells and whistles, but also a very flexible measurement input for a control system based on fuzzy logic. Whether a sensor converts to current, voltage or resistance, the DMM can handle its output signal. Your sensor has a non-linear response? No problem for fuzzy logic. In the first two instalments we describe the PC-driven multimeter, while the last instalment will present a fuzzy logic control system that makes use of the present DMM.

MAIN FEATURES

Display:	3¾ digit
Ranges:	±400.0 mV - ±400 V (AC and DC)
	±400 mA (AC and DC)
	400.0 Ω - 40.00 MΩ
Accuracy after calibration	
- voltmeter:	better than ±(1% of measured value + 1 digit)
–1% bandwitdh	300 Hz
max. crest factor (U_p/U_{rms}):	5
- ohmmeter:	±(1% of measured value + 1 digit)
- ammeter:	±(1% of measured value + 1 digit)
Switching outputs:	
4 power outputs with flyback diode	50V/0.5A
6 HCT outputs	5V/35mA

System requirements:
IBM compatible PC-AT (286, 386 or 486) with 1MB EMS and hard disk (DMM software not suitable for PC-XT).
1.44-MB 3.5-inch floppy disk drive.
One free 8-bit slot.
Mouse and colour VGA monitor recommended.

Design by H. Scholten

YOU may wonder why we did not call the present circuit an A-D (analogue-to-digital) converter. After all, it converts the level of an analogue signal into a corresponding digital value. In general, an A-D converter is a circuit capable of fast conversion of a direct voltage into a digital value — 'fast' meaning within a few microseconds. Other physical quantities require additional (external) electronics circuitry.

Although a DMM (digital multimeter) also contains an A-D converter, this is not usually very fast. For example, in the case of the present DMM, the conversion time is 50 ms. Also, the DMM usually needs a few seconds before the measured value is correctly displayed following a large change in the input signal. This is called the settling time. Fortunately, in view of the application range of the DMM, 'slow' conversion is not really a problem. The above mentioned additional electronics required by an ADC to measure other quantities than direct voltages are already implemented in the instrument, whence the name *multi*meter. In the case of the present DMM, we are even more fortunate because a large part of this additional electronics is contained in a single integrated circuit.

Where a control system is involved, the choice between a DMM and an ADC depends on the nature of the signal to be measured. Dynamic signals require an A-D converter which is fast enough to follow all changes. Although an ADC may also be used when the input signal is (quasi-) static, a DMM has the advantage of easier sensor connection — all you need to do is set the right measurement range. As long as the sensor supplies a signal that falls within the range of the meter, you are relieved of separate adaptor circuits, and other problems that arise from driving a 'bare bones' A-D converter.

The PC interface

The multimeter consists of a PC insertion card and a DMM card proper. The circuit diagram of the first is shown in Fig. 1. The DMM card being a pretty sensitive unit, it is not fitted in the computer, but connected to the insertion card via a length of flatcable.

Although the PC interface is designed as an insertion card for 8-bit slots, it can not be used in a PC-XT. This is because the software has a graphics user interface (GUI), which calls for a PC-AT with a minimum of 1 MByte EMS.

The PC interface was not specifically designed for the DMM card. Its output connector, K1, supplies a number of signals intended for a bus system called MicroSystem, designed by the author for measurement and control systems. The bus allows several extensions, including DMM cards, to be connected, and consists of the following signals: eight data lines (D0-D7), eight card selection lines (K0-K7), five register address lines, read, write, strobe, reset, int, nmi, wait, clock, mc1, ground and the positive supply voltage.

Although the PC interface is relatively simple, a quick discussion of its operation may be useful for some readers. The address at which the card can be accessed by the PC is set with the aid of DIP switch block S1. Comparator IC3 compares the address on the switches with that on address lines A3-A9 (A9 has to be '1' in all cases). The addressing of the card complies with the 10-bit addressing system defined for I/O cards in PCs. None the less, the interface uses more address lines than the usual ten. However, the logic levels on these additional lines are only valid if the address decoder has detected that the interface is being addressed via the normal set of ten address lines. In other words, the 10-bit PC-I/O address is a 'key' that gives access to the addresses indicated by the

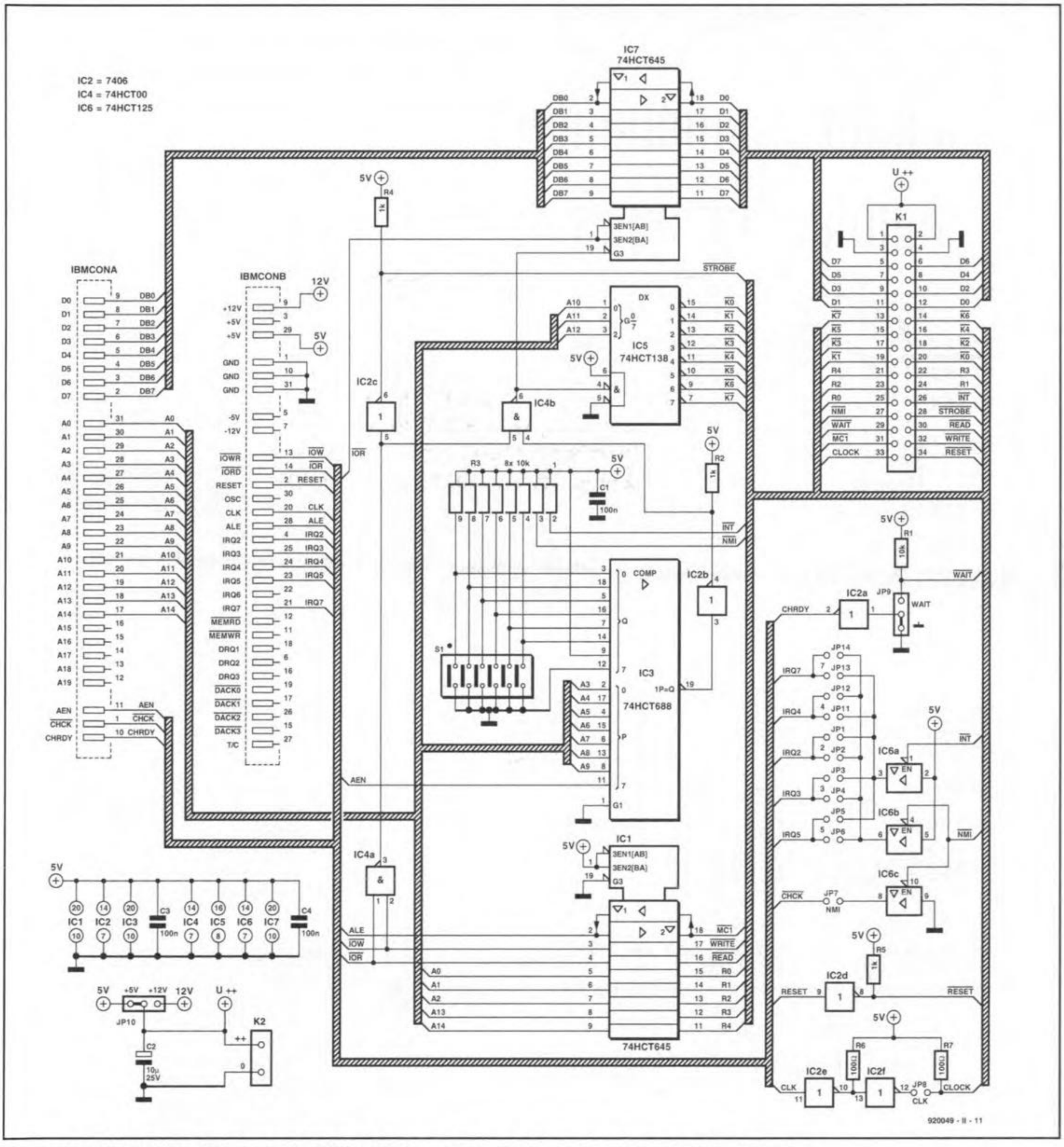


Fig. 1. This PC interface allows up to eight I/O cards to be controlled. One of these is the digital multimeter.

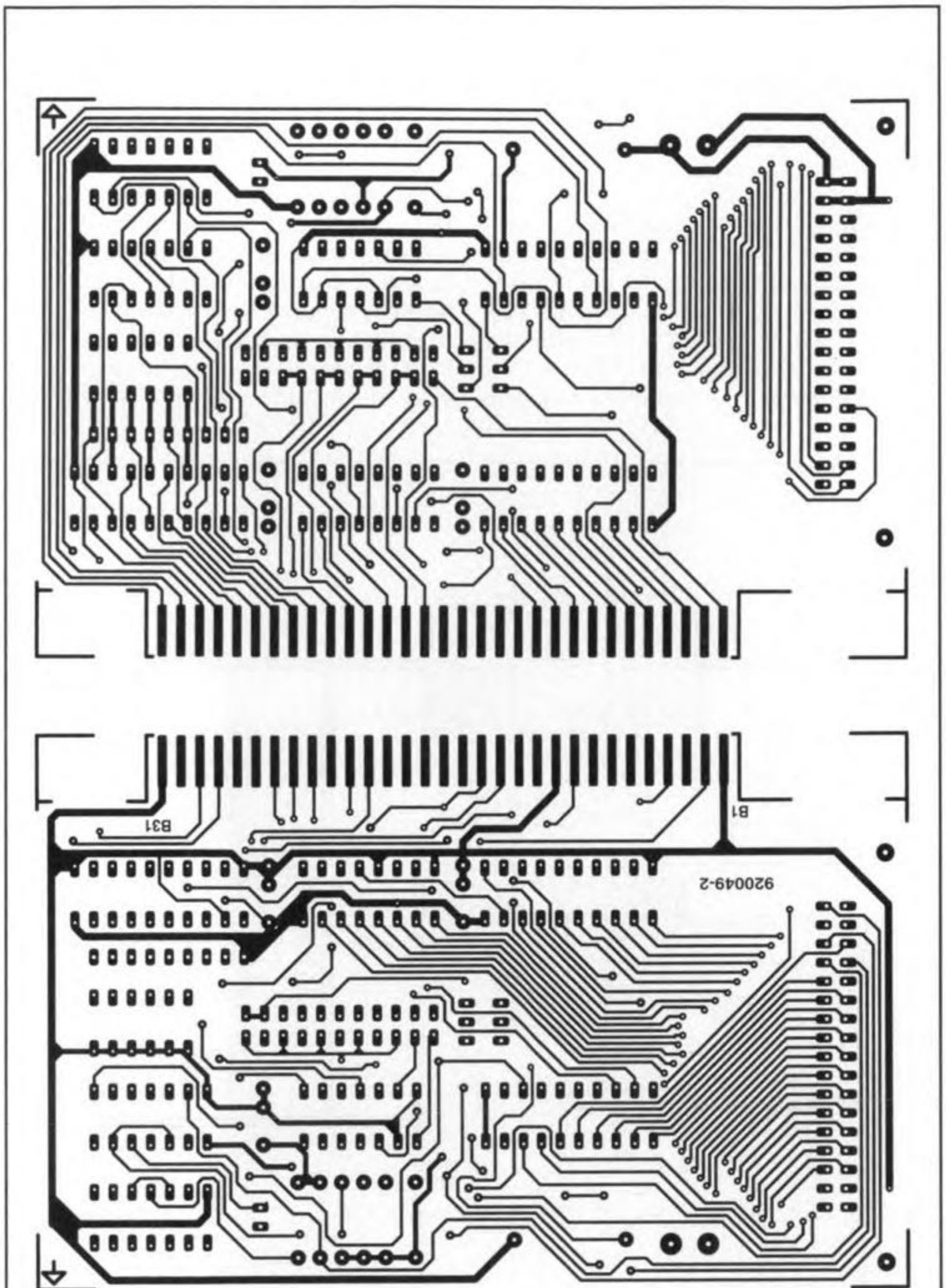


Fig. 2. PCB artwork for the PC insertion card (double-sided, through-plated).

higher address lines. No access without this key! The first three of the (rarely used) high address lines, A10, A11 and A12, are used by the interface to address one of the cards on the MicroSystem bus. This is achieved via IC5 which decodes A10, A11 and A12 into eight individual card selection lines (K0-K7), one of which can be active at a time. Further, address lines A13 and A14, together with A0, A1 and A2, are buffered by IC1, after which they are used as register address lines. In this way, up to 32 registers are created (if necessary) at every card address. Circuit IC1 buffers a couple of PC extension slot signals, and puts them on to the bus. IC7 does the same with the PC's databus signals.

Interrupt requests are conveyed to the PC via three-state buffers contained in IC6. If the MicroSystem bus does not supply interrupts (NMI or INT), the outputs of the buffers are switched to high impedance. In this condition, the PC's interrupt lines are 'free' for other interrupt sources. If the MicroSystem bus does generate an interrupt request, the output of the relevant buffer goes high, and causes an interrupt on the PC. Jumpers allow you to select the interrupt line used in the PC. The selection should be made carefully, since choosing a line that is already used by another extension card in the PC may upset the operation

COMPONENTS LIST

PC INTERFACE

Resistors:

1	10kΩ	R1
3	1kΩ	R2;R4;R5
1	8-way 10kΩ SIL	R3
2	100Ω	R6;R7

Capacitors:

3	100nF	C1;C3;C4
1	10µF 25V	C2

Semiconductors:

2	74HCT645	IC1;IC7
1	7406	IC2
1	74HCT688	IC3
1	74HCT00	IC4
1	74HCT138	IC5
1	74HCT125	IC6

Miscellaneous:

1	34-way box header, angled pins	K1
1	2-way PCB terminal block, 5mm pitch	K2
1	6-way DIP switch	S1
2	34-way IDC socket	
1	Printed circuit board 920049-2 (see page 78)	

of the entire system. Since the control of the DMM does not require interrupts, it is best to fit no jumpers at all if this extension is used on the MicroSystem. If you want to know which interrupt is still free in your system, use a PC diagnostic program such as MSD (MicroSoft Diagnostics 2.0), which is supplied with Windows 3.1 (but can be used without Windows, i.e. run from the DOS prompt).

The supply voltage selection on the bus is also made with the aid of a jumper. The options available are +5 V, +12 V or an external voltage connected to K2. The advantages of an external power supply over the one in the PC are mainly a cleaner output voltage and a higher maximum current.

The artwork of the printed circuit board designed for the PC interface is given in Fig. 2. Construction of this card is straightforward, and requires no further discussion. The printed circuit board is available ready-made through our Readers Services. The default jumper settings are as follows: JP3 fitted (no further interrupt jumpers fitted), JP8 fitted, JP9 to ground, JP10 to +12 V. The DIP switch block allows the base address of the interface to be set between 200H and 3F8H. This type of card is usually mapped in the range between 300H and 31FH. The default address assumed here is 300H, which is set up by sliding all switches in S1, except the one nearest to JP1, to the 'on' position.

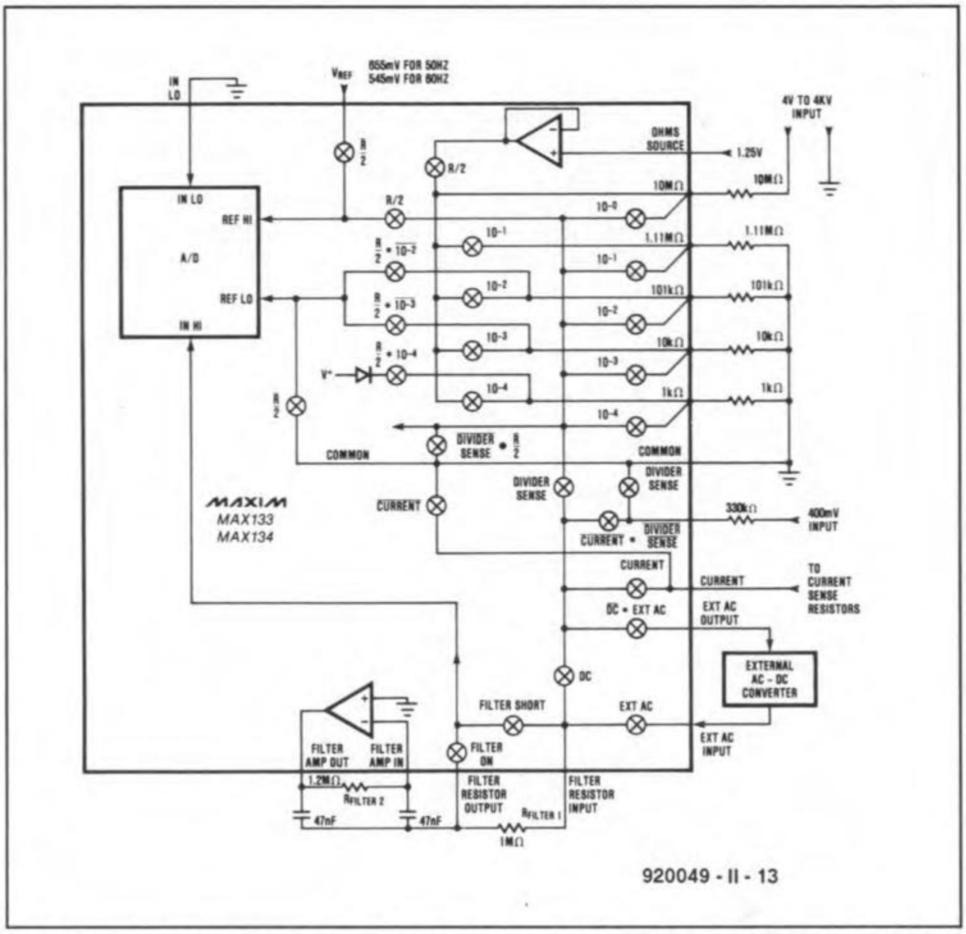


Fig. 3. Block diagram of the analogue part of the MAX134. The large number of switches contained in the IC enable the external component count to be reduced considerably.

MAX134: nearly everything...

The main IC in the multimeter circuit is the MAX134 from Maxim Inc. Apart from a 3¾-digit A-D converter, it also contains nearly all the switches required to build a complete DMM, and an associated computer interface. The integrated switches reduce the external component count considerably, and need to be complemented by only a few external contacts to create the DMM's resistance ranges. The block diagram of the analogue part of the MAX134 is shown in Fig. 3. The drawing also shows what is 'missing from the chip': resistors in the voltage divider that creates the measurement ranges, a true-rms converter, a voltage reference, and a couple of filter components.

The MAX134 is capable of exchanging data with a PC via an on-chip interface consisting of a four-bit bidirectional data bus (D0-D3), three address lines (A0, A1 and A2) and two control lines (read and write). Figure 4 shows the timing diagram pertaining to a read and a write operation on the interface. Remarkably, the address has to be stable for quite a while before the read or write pulse may be given. The relevant times are 3250 ns (t_{acc}) and 2500 ns (t_{as}), which are quite long for a PC. Further on, you will see that this has been taken into account in the design of the hardware and software. Table 1 indicates the type of data read from, or written to, the DMM addresses.

DMM card

The complete circuit diagram of the DMM card is shown in Fig. 5. Apart from the components already indicated in the block diagram of Fig. 3, the circuit diagram shows the interface to the MicroSystem bus (IC4; IC6-IC9), a couple of computer-controlled digital outputs (IC4, IC9 and IC11), a power supply based on a voltage regulator (IC10), a voltage inverter (IC3), a true-rms converter (IC2) and, finally, a reference voltage source. We will discuss these sub-circuits in reverse order.

The reference voltage source is headed by a filter, R21-C8-C9-C10, on the +5-V rail. Next, the voltage is reduced to 1.2 V by a high-precision bandgap reference diode, D5. The C-version of the ICL8069 used here has a temperature coefficient of only 50 ppm $°C^{-1}$ (0.005% $°C^{-1}$). The 1.2 V is used directly as a reference for the resistance measurements (via pin 32 of IC1), but it has to be halved to enable it to be used as a reference for the A-D converter. This is achieved with the aid of a voltage divider which consists of two precision resistors shunted by a

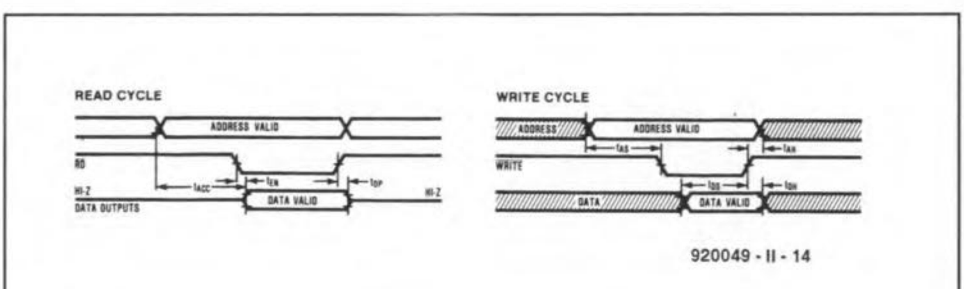


Fig. 4. The timing of the control signals for the MAX134 is quite slow, and requires a software/hardware trick to keep the (much faster) PC happy.

high-value multiturn preset (R23-R24-P1). This particular type of connection affords smooth adjustment while preserving the stability of the potential divider. The exact level of the reference voltage depends on the mains frequency to be suppressed. This will be either 50 Hz or 60 Hz (selected via the control software). The integration time of the converter ideally covers exactly one period of the mains voltage for optimum suppression of hum picked up by the sensor or the ADC itself. At 50 Hz, the period (integration time) lasts 655 ADC clock cycles, or 545 ADC clock cycles if the mains frequency is 60 Hz. Since the reference voltage is dependent on, among others, the number of clock cycles, it has to be adjusted to match the mains frequency. The exact reference levels are: 655 mV for 50 Hz, and 545 mV for 60 Hz.

Continued next month

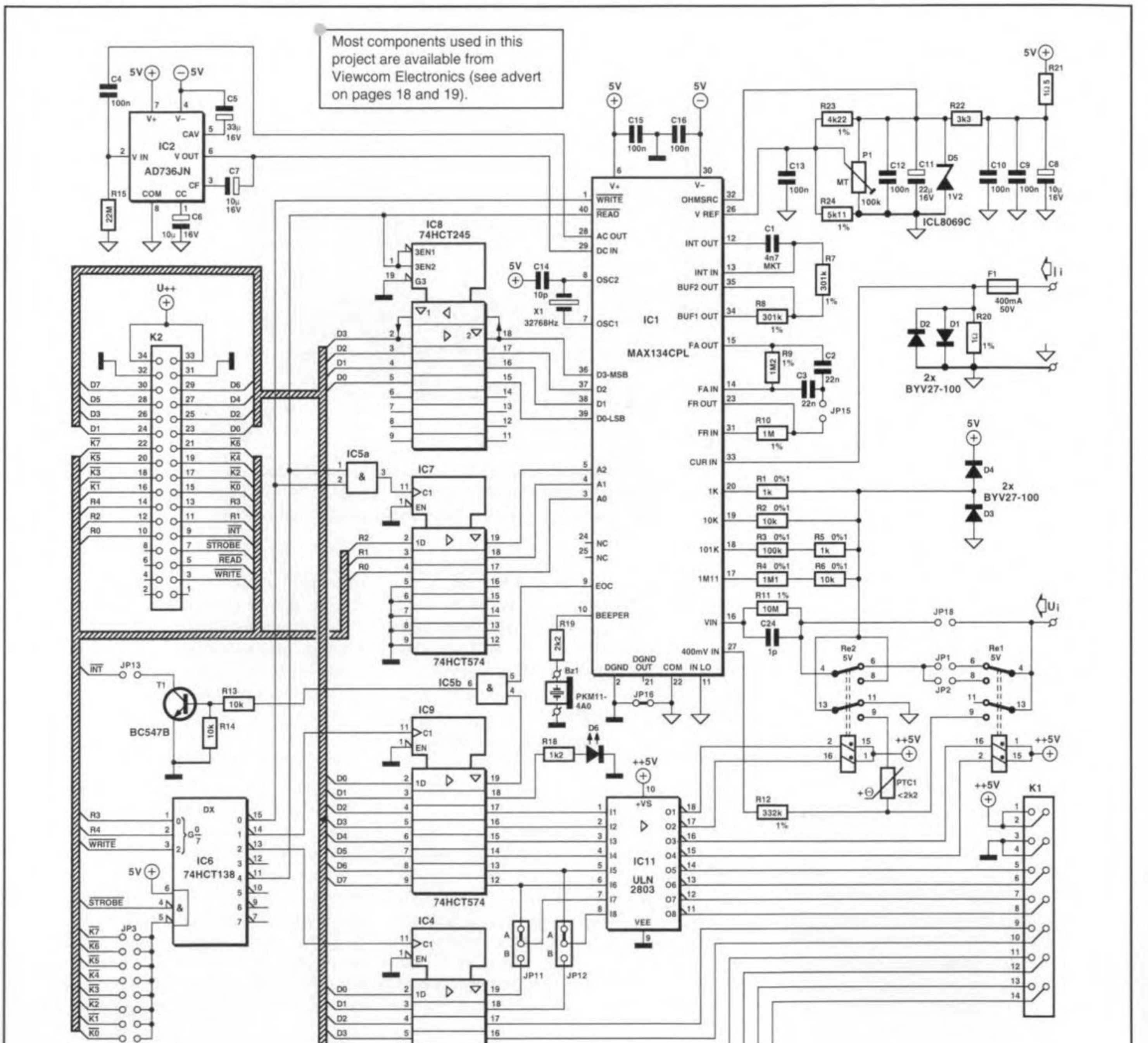
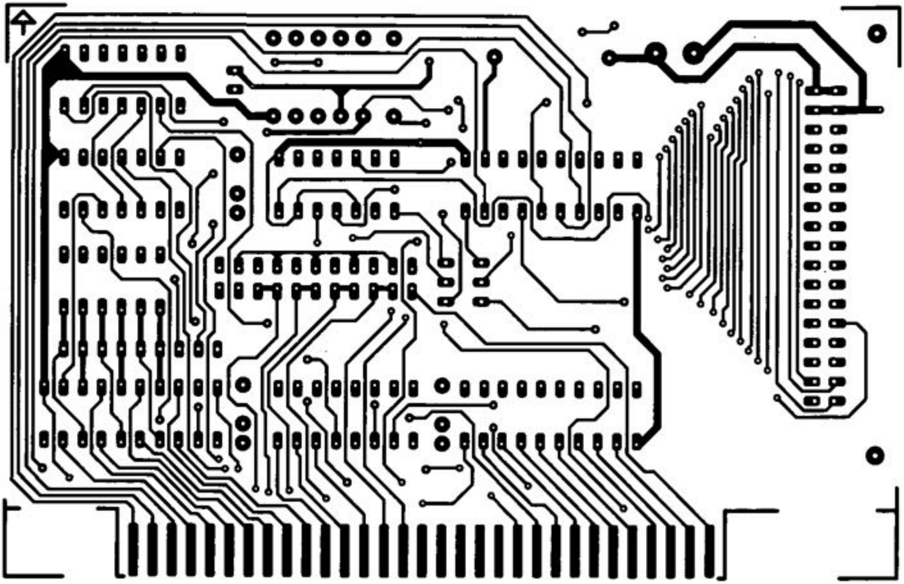
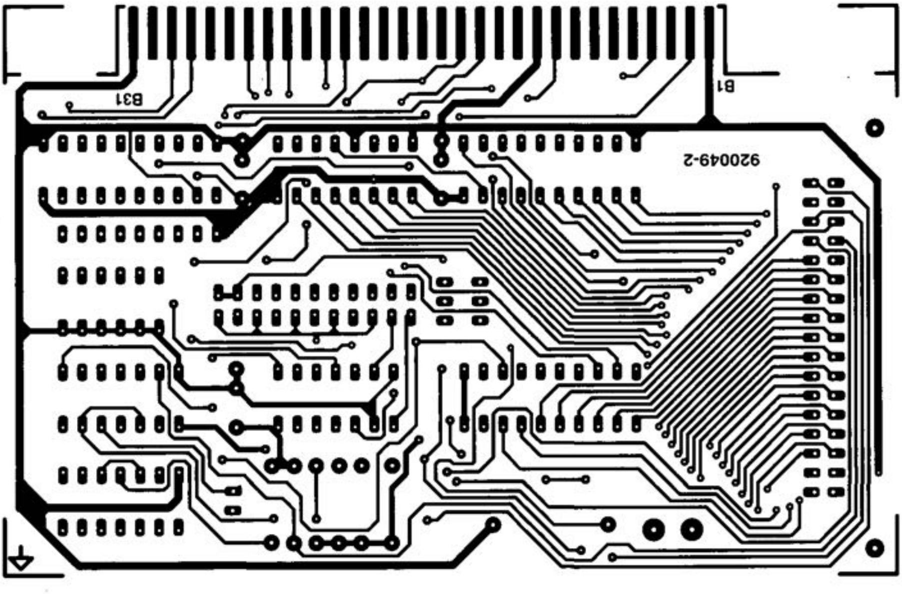


Fig. 5. Circuit diagram of the digital multimeter.

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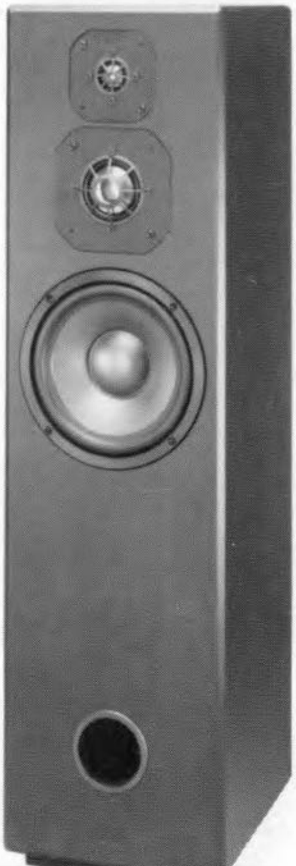
ACTIVE 3-WAY LOUDSPEAKER - PART 2

Design by T. Giesberts and H. Baggen

The prototype loudspeaker system is housed in a 90 cm (36 in) high enclosure, details of which are shown in Fig. 7. The drive units are a 200 mm (8 in) 4 Ω woofer, a 50 mm (2 in) 8 Ω mid-range unit, and a 25 mm (1 in) 8 Ω tweeter.

The frequency characteristics of the three cross-over networks are shown in Fig. 5. Note that a small error has crept into Part 1: it was stated that the mid-range section has cut-off frequencies of 500 Hz and 500 Hz; that should, of course, have read 500 Hz and 5000 Hz. It may be noted that the characteristics do not conform to a pure Bessel, Butterworth, or similar, design. This is because in practice cross-over filters must have a slightly non-standard characteristic, since the frequency response of the drive units and the summing behaviour around the cut-off frequencies must be taken into account. Simulation programs such as PSPICE or MicroCap are of great help in the design.

As already stated in Part 1, if a 4 Ω woofer is not available, an 8 Ω type may be used, but the supply voltage to the bass frequency output stage should then be increased to ±35 V. The output of this stage is then 70 W, but that of the other two output stages remains 30 W. This is a costly solution, because two separate power supplies are required. Note that ±35 V is the absolute maximum if the specified voltage regulators are used. It is possible to connect a resistor in series with IC_6 and IC_7 to lower the voltage slightly, but it is better to replace the regulators by 20 V types: 7820 and 7920 respectively, which can handle input voltages up to 40 V. In that case, C_{49} and C_{50} must be 50 V types and IC_1 must be replaced by a type that can handle higher voltages than the TL074: for example, TL34074(A); TLE2144; LF147;



LF444A (**not** LF444); MC34074; MC34084; OP11 (**not** OP11GR).

Construction

The PCB is populated in the usual manner: first the wire bridges, then the passive components, next the semiconductors (but see below for T_3–T_6 and IC_4 and IC_5), and finally the relay and electrolytic capacitors C_{49} and C_{50} (which must be mounted upright).

Drill and tap suitable screwholes in the heat sink for the power transistors and the modules. Fix the heat sink to a sheet of aluminium of about 230×260 mm ($9^1/_4$×$10^1/_2$ in) with the aid of right-angle brackets.

Next, fit the power transistors and modules to the heat sink with the aid of heat conducting paste and insulating washers (these should be ceramic for the transistors). Bend the terminals of these devices (and give them a kink as well to allow for tension during temperature changes) so that they fit properly into the relevant holes on the PCB and solder them in place.

Mount the mains switch, fuse holder(s), transformers, electrolytic capacitors, and the audio input socket on the aluminium sheet (see Fig. 2). Fit the bridge rectifiers on the free area of the heat sink. The audio input socket should be an insulated type, which enables the best earthing point to be established: the aluminium sheets is strapped either to the socket earth or to the central earth of the electrolytic capacitors: use the position that gives the least hum.

After all parts have been fitted securely to the aluminium sheet, wire up the assembly as shown in Fig. 6. This diagram shows the value of the four buffer capacitors for the bass amplifier as 10 000 μF; this is a minimum value: use 20 000 μF if possible. Fit the mains cable with a strain relief sleeve.

Next, the quiescent current for the bass amplifier must be set. Start by turning P_1 fully anticlockwise. Remove the –35 V connection from the board and insert a milliammeter in series with this supply line. Switch on the mains and turn P_1 till the meter reads 50 mA. Switch off the mains, remove the meter and reconnect the –35 V line to the board.

A few seconds after the mains has been switched on again, the relay should change over. If it does not, it is probable that T_8 does not provide enough current for the relay (remember, a cur-

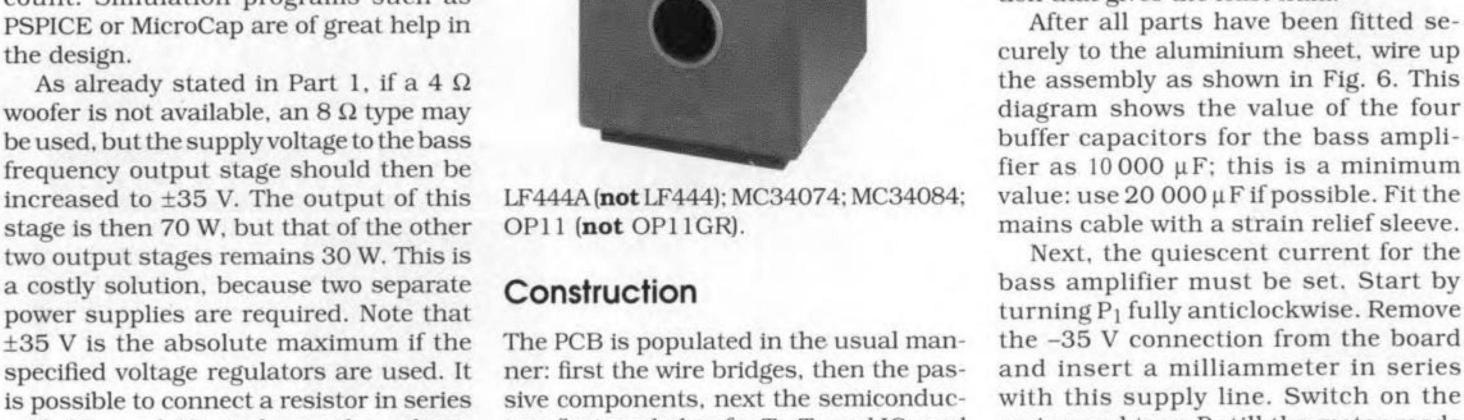


Fig. 5. Characteristic curves provided by the active filters.

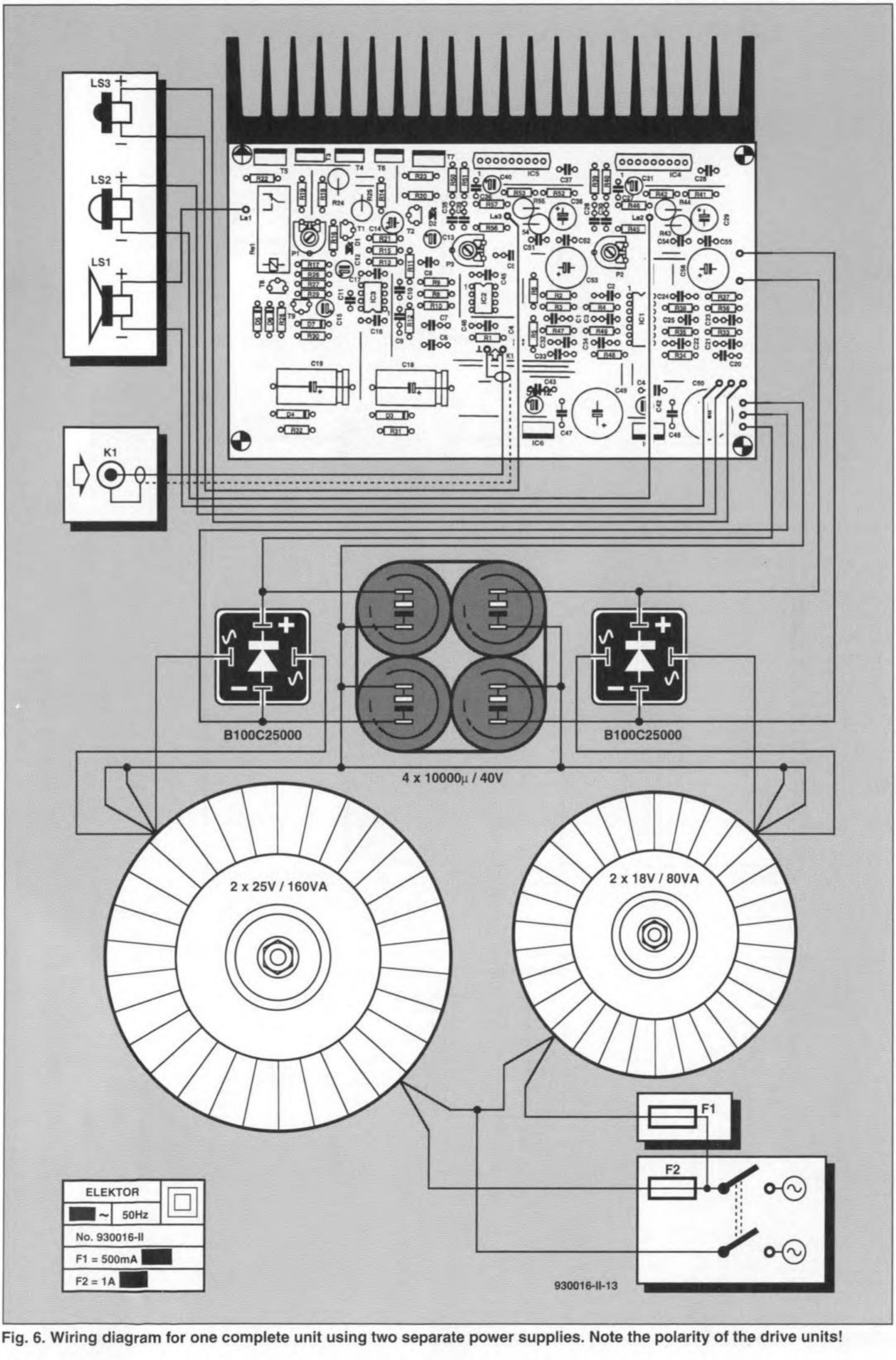


Fig. 6. Wiring diagram for one complete unit using two separate power supplies. Note the polarity of the drive units!

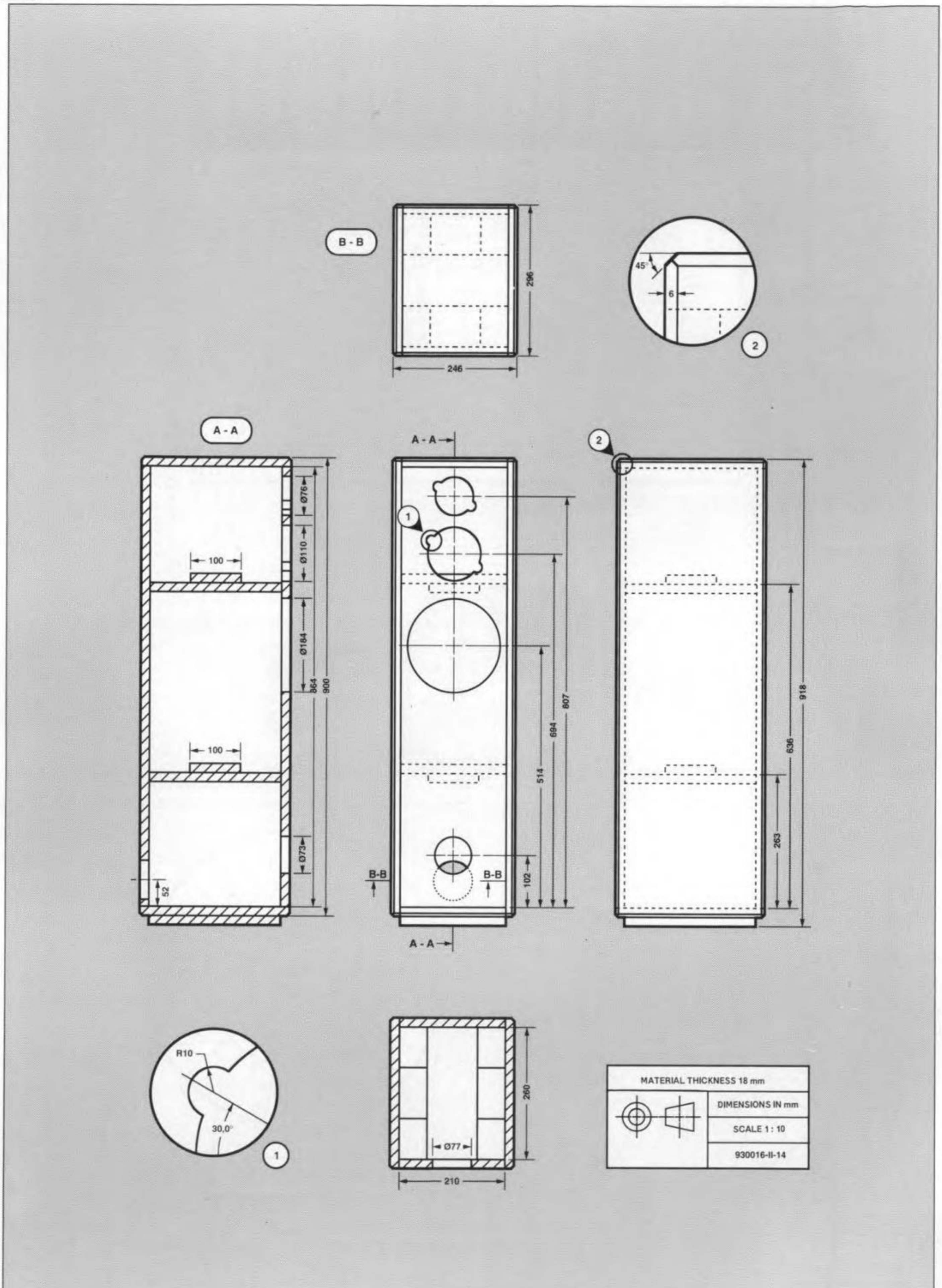


Fig. 7. Construction drawing of the enclosure. The hole for mounting the electronics assembly is not shown – see text.

PARTS LIST
(Additional to that in Part 1)

Mains transformer, 80 VA, secondary 2×18 V
Mains transformer, 160 VA, secondary 2×25 V
2 off bridge rectifier B100C25000
4 off capacitor ≥10,000 μF, 40 V
Mains entry with integral fuse holder and 1 A slow fuse, and on/off switch
Fuse holder with 500 mA slow fuse

ENCLOSURE

100 W, 200 mm (8 in), 4 Ω, woofer
50 W, 50 mm (2 in), 8 Ω, mid-range drive unit
30 W, 25 mm (1 in), 8 Ω, tweeter
18 mm thick medium density fibre board or high-density chip board:
2 off 864×210 mm
2 off 900×260 mm
2 off 210×296 mm
2 off 210×100 mm
2 off 260×100 mm
1 off 210×260 mm
Bass reflex duct, 145 mm ($5^{11}/_{16}$ in) long
3 metres mains cable
2 bags polyester wadding

rent source is used here). In that case, the value of R_{26} must be increased to the next or second higher E12 value. The value is correct when, a few seconds after the mains has been switched on, the potential across Re_1 is 24 V.

For safety's sake, measure all relevant supply voltages on the board and check that the direct voltage levels at the amplifier outputs are zero or very nearly so.

Finally, set P_2 and P_3 so that the resistance between wiper and ground is 55% of the total in the case of P_2 and 70% in the case of P_3.

The enclosure

The box is made from 18 mm thick medium density fibre board (MDF) or high-density chip board. The construction details are shown in Fig. 7. Basically, it is a rectangular box provided with two reinforcing cross members that prevent panel vibrations.

The one hole not shown in the drawing is that for the electronics assembly. It is best to fit this at the bottom of the enclosure, so that the board rests on spacers on the bottom panel. Saw a rectangular hole in the rear panel (see Fig. 2) whose width and height are 20 mm smaller than the aluminium sheet. On completion, the sheet is fixed across the hole with 10 or 12 suitable wood screws and sealed with draught-proofing tape.

Before that, however, fill the enclosure above the lower cross member evenly with the polyster wadding. The bottom third of the box, where the bass reflex duct and electronics assembly will be located, remains free of wadding.

Next, fit the drive units, provide them with cables and connect these to the board. Make sure that the polarity is as shown in Fig. 6.

Then, screw the electronics assembly across the rectangular hole at the rear as already discussed.

Next, push the bass reflex duct into the port on the front panel.

Finally, where deemed desirable, it is, of course, possible to use normal potentiometers for P_2 and P_3 and fit these to the aluminium sheet, so that they can be readjusted, when required, without the need of removing the entire assembly from the box. In that case, the connections between these controls and the board should be by screened audio cable. **END**

FIGURING IT OUT

PART 8 – COMPLEX NUMBERS

By Owen Bishop

This series is intended to help you with the quantitative aspects of electronic design: predicting currents, voltage, waveforms, and other aspects of the behaviour of circuits. Our aim is to provide more than just a collection of rule-of-thumb formulas. We will explain the underlying electronic theory and, whenever appropriate, render some insights into the mathematics involved.

We begin this month's discussion with a simple and apparently innocuous equation:

$$x^2 + 1 = 0 \qquad \text{[Eq. 47]}$$

The first stage of finding the value of x is easy:

$$x^2 = -1,$$

but now comes the ostensibly impossible part:

$$x = \sqrt{-1}.$$

It is a fact of elementary arithmetic that two positive numbers multiplied together give a positive product. Further, two negative numbers when multiplied together also yield a positive product. There is no way of multiplying two numbers with the same sign to obtain a negative product. Yet, here we are expected to multiply two identical numbers together and obtain −1. The way out of this impasse is to recognize that the value of x does not belong to the set of **real numbers**. It is an **imaginary number**. Mathematicians give it the symbol **i**, but, since this is likely to be confused with the symbol for electric current, electrical and electronics engineers use the symbol **j** instead. Thus, we define **j** by the equation:

$$\mathbf{j} = \sqrt{-1}. \qquad \text{[Eq. 48]}$$

Although **j** belongs to the realms of the imagination, it helps to understand it and to work with it if we represent it in diagrammatic form. All real numbers can be represented as points on a continuous line, the **number line** (see **Fig. 67**). We have marked the positions of the points that represent integers −5, −2, 0, 4, 7, ...; the points between these represent real numbers of various other kinds, including special numbers such as π. To represent imaginary numbers, we construct an **imaginary number line** which is perpendicular to the real number line (see **Fig. 68**). The points marked on this represent the integral multiples of **j**. For example, the point **j**3 is three times **j**:

$$\mathbf{j}3 = 3\times\sqrt{-1} = \sqrt{(9\times -1)} = \sqrt{-9}.$$

By convention, we write **j**3 in preference to 3**j** to make it clear that the term is imaginary.

Note that we can have negative imaginary numbers as well as positive ones. For example:

$$\mathbf{j} = -\sqrt{-25}.$$

The perpendicular lines of **Fig. 68** take us a stage further, since they can be taken to be the axes by which any point in the whole area of the figure can be defined. Points that are on the horizontal axis (known as the **real axis**) are real numbers. Points which are on the vertical axis (the **imaginary axis**) are imaginary numbers. Points within the four quadrants are defined by quoting their two coordinates, just as we would on an ordinary graph. Each point in the figure is defined by two numbers, one of which is real and the other of which is imaginary. A number so defined is known as a **complex number**. The area of the figure is the **complex number plane**. Sometimes it is referred to as the **Argand plane**, and the figure is known as an **Argand diagram**.

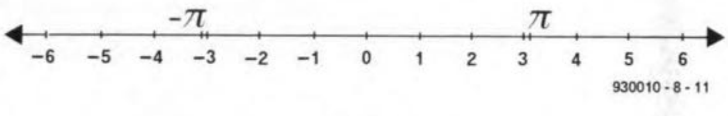


Fig. 67.

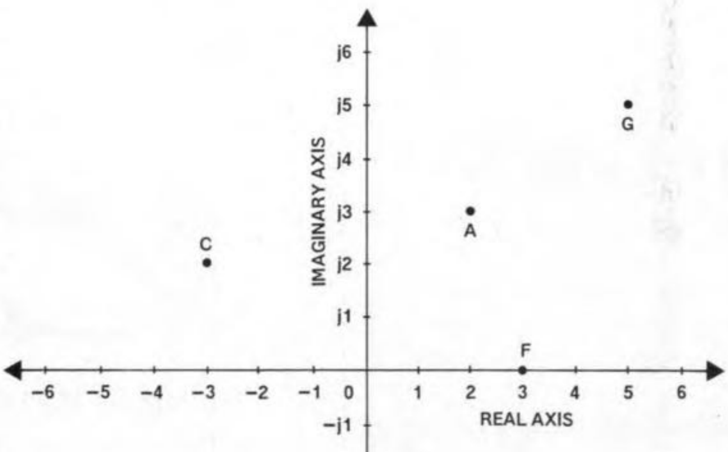


Fig. 68.

Working with complex numbers

Consider the point A in **Fig. 68**. If this were a point on a graph, we would say that its coordinates are (2, 3). Since this is an Argand diagram, we say that this point represents the complex number (2 + **j**3). We can never actually **add** 2 to **j**3, because these numbers represent distance in perpendicular directions. Because these distances are both positive, we know that the point is in the first quadrant. Values represented by other points in **Fig. 68** are:

$B = 2 - \mathbf{j}4 \quad E = 0 - \mathbf{j}2$
$C = -3 + \mathbf{j}2 \quad F = 3 + \mathbf{j}0$
$D = -4 - \mathbf{j}3 \quad G = 4.6 + \mathbf{j}5.2$

Each complex number has a real part and an imaginary part. Either part may sometimes be zero, in which event the number is represented by a point on one of the axes.

Addition of complex numbers follows the rules of algebra in that we are allowed to add a's to a's and b's to b's, but not a's to b's. With complex numbers, we may add the real parts and may add the imaginary parts, but the two parts must be kept separate. For example, add (4 + **j**6) and

(5 + **j**2):

$$\begin{array}{lr} & 4 + \mathbf{j}6 \\ & +\ 5 + \mathbf{j}2 \\ \hline \text{Answer} & 9 + \mathbf{j}8 \end{array}$$

Another example, add (3 + **j**2) and (2 − **j**4):

$$\begin{array}{lr} & 3 + \mathbf{j}2 \\ & +\ 2 - \mathbf{j}4 \\ \hline \text{Answer} & 5 - \mathbf{j}2 \end{array}$$

Subtraction is similar: for example, subtract (3 + **j**5) from (7 + **j**9):

$$\begin{array}{lr} & 7 + \mathbf{j}9 \\ & -\ 3 + \mathbf{j}5 \\ \hline \text{Answer} & 4 + \mathbf{j}4 \end{array}$$

Addition and subtraction of complex numbers presents no surprises and it might be wondered how these operations could be relevant to electronics. **Figure 69** helps to show the connection.

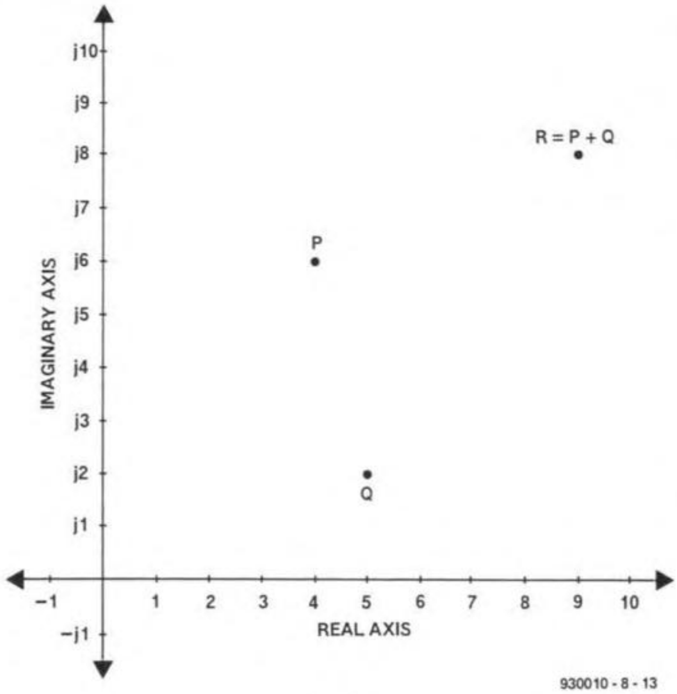


Fig. 69.

Vector addition

In **Fig. 69**, there are two points, *P* and *Q*, representing the two complex numbers added in the first of the three examples in the previous section. The sum of these two numbers is represented by point *R*. In **Fig. 70**, we have the same three points, but now these are seen to be the finishing points of three **vectors**, all of which begin at the origin. Not only can complex numbers be drawn as vectors, but it is clear that the vector ***R*** is the sum of the vectors ***P*** and ***Q***. Complex numbers are a way of representing vectors and adding complex numbers is a way of adding vectors. Now we are really connecting with electronics. In Parts 6 and 7 we used vectors (or **phasors**) to show the relationships between various currents, pds or impedances in circuits that have sinusoidal currents or pds applied to them. It was often necessary to sum two or more vectors. Application of Pythagoras' Theorem makes this relatively easy when the vectors are perpendicular. When they are not, the calculations may involve some elaborate trigonometry. To help us keep the trig under control, we make use of the conventions of imaginary numbers and the Argand diagram. Using imaginary numbers by no means implies that the currents, pds or impedances themselves are imaginary. It is just that the graphical representation of imaginary numbers is a useful tool for dealing with vector quantities such as current, voltage and impedance (and with other vector quantities besides).

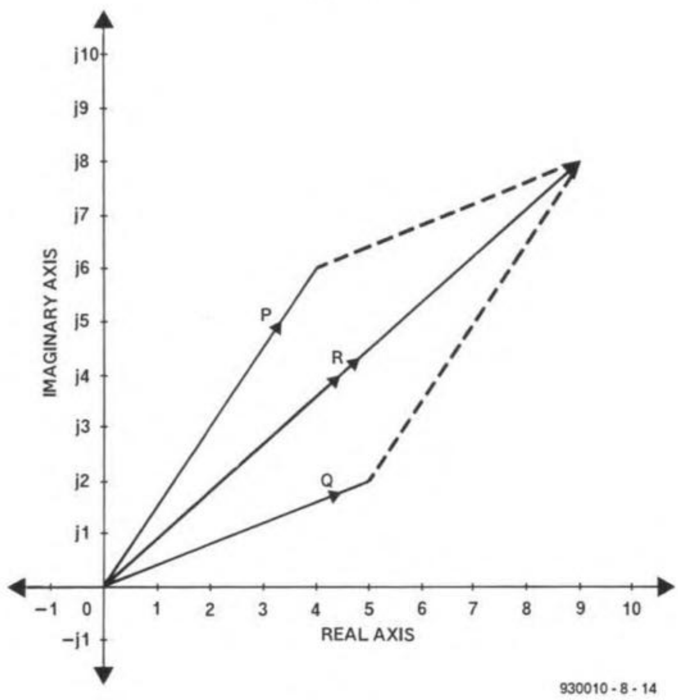


Fig. 70.

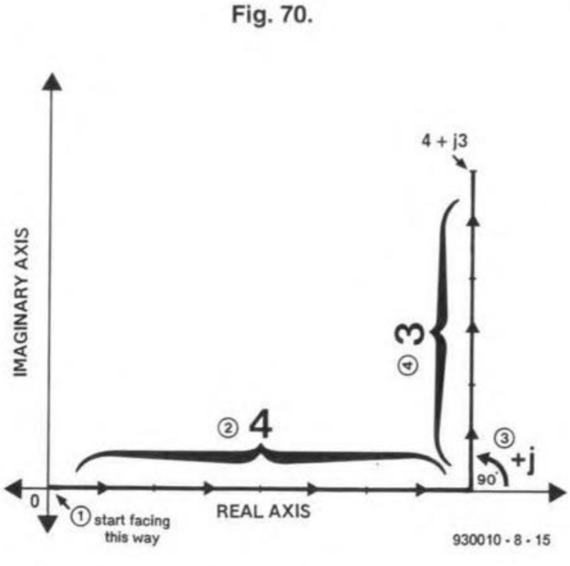


Fig. 71

The meaning of j

Before we go on to use complex numbers to analyse practical circuits, let us look again at that symbol **j**. We have given it a value (Eq. 48), though this is not a value like the value of a real n umber. There is another way of thinking of **j**, particularly in the context of the Argand diagram. We may think of **j** as the **imaginary operator**. An operator symbolizes an **operation**. For example, the symbol ∫ symbolizes the operation of integration. In logic and in digital electronics, the operator **+** symbolizes the OR operation. In the Argand diagram, **j** symbolizes the operation of a quarter turn (90°) in the anticlockwise direction. The convention of writing **j** first in an imaginary number reinforces the idea that it is an operator.

Given the complex number (4 + **j**3), for example, we interpret this as the following sequence of instructions, illustrated in **Fig. 71**:

1. Start at the origin facing along the real axis in the positive direction.
2. Move 4 units forward.
3. Turn 90° anticlockwise.
4. Move 3 units forward.

This take us to the point in the complex number plane which represents (4 + **j**3).

A negative value of **j** is interpreted as a 90° clockwise turn. For example, (5 − **j**2) means:

1. As above.
2. Move 5 units forward.
3. Turn 90° clockwise.
4. Move 2 units forward.

A 90° turn anticlockwise followed by another 90° turn anticlockwise equals a turn of 180°. We are facing in the opposite direction, along the real axis, but in the negative direction. This corresponds to the value of $\mathbf{j}^2$:

$$\mathbf{j}^2 = \mathbf{j} \times \mathbf{j} = \sqrt{-1} \times \sqrt{-1} = -1.$$

Similarly, $\mathbf{j}^3 = -\mathbf{j}$ (a three quarters turn) and $\mathbf{j}^4 = 1$ (a complete turn).

Using j

Figure 72 shows an *LCR* parallel circuit to which a sinusoidal voltage is applied. This figure is the same as **Fig. 60**, discussed in Part 7. At any instant, equal voltage is applied across each branch of the circuit. For each branch of the circuit, the current at any instant is calculated by dividing the voltage by the resistance or impedance of that branch. We consider each branch in turn.

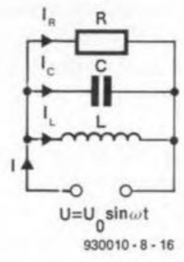


Fig. 72.

The current through the resistor is

$I_R = U/R.$

The current is in phase with the voltage, so we represent it in an Argand diagram by a vector lying along the real axis in the positive direction (**Fig. 73**).

The current through the capacitor is

$$I_C = U/X_C. \qquad \text{[Eq. 49]}$$

Owing to the properties of capacitors, this current leads the resistor current by 90°. There are two ways of taking this phase difference into account. One way is to state that fact, as we have just done, and then draw the vector in the appropriate direction as we did in **Fig. 61** of Part 7. The other way is to say that the reactance of a capacitor is

$$X_C = -\mathbf{j}/\omega C. \qquad \text{[Eq. 50]}$$

Eq. 50 is the same as Eq. 34 Part 6), except that we have incorporated the phase difference into it. Eq. 50 expresses X_C as an imaginary quantity, lagging 90° behind the applied voltage. This hypothetical quality of the impedance is related only to its representation in an Argand diagram. The current passing into or out of the capacitor continues to be subjected to a substantial opposition to its flow!

Similarly, Eq. 33 (Part 6) can now be modified to take phase into account:

$$X_L = \mathbf{j}\omega L. \qquad \text{[Eq. 51]}$$

Inductive impedance leads the applied voltage.

If we substitute the new expression for capacitive impedance (Eq. 50) into the equation for calculating current (Eq. 49), we are in the position of dividing a real number by an imaginary number:

$$I_C = U/X_C = U\omega C/-\mathbf{j}. \text{ [Eq. 52]}$$

As mentioned earlier, real numbers and imaginary numbers do not mix. If we are to solve Eq. 49, we must discuss how to perform multiplication and division with complex numbers.

Multiplication

Multiplication follows the usual routines of algebra. For example, multiply $(4 + \mathbf{j}3)$ by $(3 + \mathbf{j}2)$. Set this out in the usual format for multiplication:

$$\begin{array}{r} 4 + \mathbf{j}3 \\ \times\ \ 3 + \mathbf{j}2 \\ \hline 12 + \mathbf{j}9 \qquad \\ \mathbf{j}8 + \mathbf{j}^2 6 \\ \hline 12 + \mathbf{j}17 - 6. \end{array}$$

The third term has become real because of squaring **j**. Subtracting this, we obtain the answer: $(6+\mathbf{j}17)$.

Division

This is rather more difficult, but a simple trick helps. This subterfuge involves what is known as the **conjugate** complex number. In **Fig. 74**, there is a point A in the first quadrant. Its conjugate is A', in the fourth quadrant. It is clear that if, for example, A is $(4 + \mathbf{j}2)$, then A' is $(4 - \mathbf{j}2)$. The conjugate is formed by inverting the sign of the imaginary part.

Now consider the problem of dividing $(4 + \mathbf{j}5)$ by $(3 + \mathbf{j}2)$:

$$\frac{4 + \mathbf{j}5}{3 + \mathbf{j}2}$$

The trick is to multiply both numerator and denominator by the conjugate of the denominator. This does not affect the result of division, but gets rid of the imaginary component of the denominator:

$$\frac{(4 + \mathbf{j}5)(3 - \mathbf{j}2)}{(3 + \mathbf{j}2)(3 - \mathbf{j}2)}$$

$$= \frac{22 + \mathbf{j}7}{13}$$

$$= 1.69 + \mathbf{j}0.54.$$

Reciprocals

In circuit calculations, we often arrive at the expressions $1/\mathbf{j}$ and $1/-\mathbf{j}$. It is useful to know what to substitute for these. Following the rules of division give above, we first note that the **j** and **–j** are conjugates of each other, and so:

$$1/\mathbf{j} = (1\times-\mathbf{j})/(\mathbf{j}\times-\mathbf{j}) = -\mathbf{j}/1 = -\mathbf{j}. \qquad \text{[Eq. 53]}$$

Similarly,

$$1/-\mathbf{j} = (1\times\mathbf{j})/(-\mathbf{j}\times\mathbf{j}) = \mathbf{j}/1 = \mathbf{j}. \qquad \text{[Eq. 54]}$$

Continuing the analysis

Substituting the result of Eq. 53 into Eq. 52:

$$I_C = U\omega C/-\mathbf{j} = \mathbf{j}(U\omega C).$$

The result has no real part and its imaginary part is positive. The current vector of the capacitor lies along the imaginary axis and **leads** the applied voltage by 90°, as shown in **Fig. 73**. Drawing vector diagrams helps us to understand what is happening (it is usually worthwhile to draw a sketch at least), but the magnitude and direction of the current vector has been obtained solely by calculation using complex numbers.

Similarly, we calculate the current vector for I_L:

$$I_L = U/\mathbf{j}\omega L = -\mathbf{j}U/\omega L.$$

This calculation by-passes what happens to the factors ω and L in the denominator. The conjugate of $\mathbf{j}\omega L$ is $-\mathbf{j}\omega L$, so ω and L appear temporarily in the numerator and appear squared in the denominator; these cancel out to leave ω and L in the denominator, as at the beginning of the calculation. The overall effect is that **j** disappears from the denominator and **–j** appears in the numerator, as in Eq. 54.

The outcome of this calculation is that the current vector for the inductor lies along the

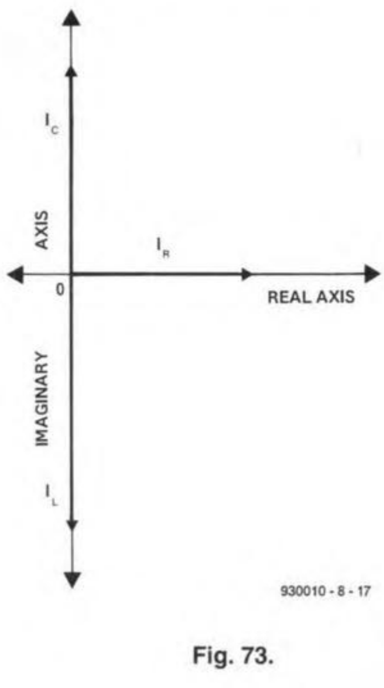


Fig. 73.

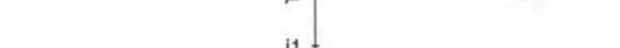


Fig. 74.

imaginary axis and **lags** the applied voltage by 90°, as shown in **Fig. 73**.

Resulting vectors

If we give some numeric values to L, C and R, and consider one particular frequency and a particular instant in time, the expressions become simpler. Suppose that $R = 250\ \Omega$, $C = 1.2\ \mu F$ and $L = 0.2$ H. Also suppose that $f = 500$ Hz, and that we evaluate the currents when $U = 2$ V.

The value of ω is

$\omega = 2\pi f = 3142 \text{ rad s}^{-1}$.

Now calculate the currents:

$I_R = 2/250 = 0.0080$ A;

$I_C = \mathbf{j}U\omega C = \mathbf{j}0.0075$ A;

$I_L = -\mathbf{j}U/\omega L = -\mathbf{j}2/628.4$

$= -\mathbf{j}0.0032$ A.

Express currents in milliamps for convenience: $I_R = 8.0$ mA; $I_C = \mathbf{j}7.5$ mA and $I_L = -\mathbf{j}3.2$ mA.

Finding the resultant of I_C and I_L is straightforward as they are both complex numbers with only imaginary parts:

$I_C + I_L = \mathbf{j}(7.5-3.2) = \mathbf{j}4.3$.

The resultant has magnitude 4.3 mA and leads I_R by 90°. Adding the resultant to I_R gives:

$I = 8.0+\mathbf{j}4.3$ [mA]

Figure 75 is an Argand diagram of these results. The magnitude of the total current I is obtained by Pythagoras' Theorem:

$I = \sqrt{(8.0^2+4.3^2)} = 9.1$ mA.

The phase angle is

$\varphi = \tan^{-1}(4.3/8.0) = 28.3°$.

Analysing LCR circuits

As a final example, we run through the analysis of a typical LCR circuit. **Figure 76** sets the problem, which is to calculate the magnitude and phase angle of the total current I when the frequency is 100 Hz at time $t = 0.001$ s. In **Fig. 76b**, the impedances are written in the form which incorporates the information about phase, that is to say, in the form of complex numbers. Given that $f = 100$ Hz, we calculate that:

$\omega = 2\pi f = 628 \text{ rad s}^{-1}$.

Using ω to evaluate the impedances at the given frequency, we arrive at **Fig. 76c**.

At time $t = 0.001$ s,

$U = 5\sin(628\times0.001) = 2.938$ V, remembering to work in radians.

$I_R = 2.938/200 = 14.7$ mA;

$I_C = 2.938/-\mathbf{j}72.4 = \mathbf{j}40.7$ mA;

$I_L = 2.938/\mathbf{j}157 = -\mathbf{j}18.7$ mA.

The resultant of I_C and I_L is $\mathbf{j}21.9$ mA. The resultant of this and I_R is $(14.7+\mathbf{j}21.9)$ mA. The magnitude of the resultant is $\sqrt{(14.7^2+21.9^2)} = 26.4$ mA. The phase angle is $\varphi = \tan^{-1}(21.9/14.7) = 56.1°$.

If we are not interested in calculating I_R, I_C and I_L individually, we can simply find the total impedance by applying the rules for impedances in parallel:

$1/X = 1/200+1/\mathbf{j}157+1/-\mathbf{j}72.4$

$= 0.005-\mathbf{j}0.00637+\mathbf{j}0.0381$

$= 0.005+\mathbf{j}0.00744$.

Then:

$I = U/X = 2.938/(0.005+\mathbf{j}0.00744)$

$= 0.0147+\mathbf{j}0.0219$.

In milliamps, $I = 14.7+\mathbf{j}21.9$, as above.

The complex impedances can be used in any of the network reduction techniques described in Parts 1, 3 and 4.

In the foregoing examples, the final stages rely on trigonometry. Next month we shall show how to calculate the magnitude and direction of the resultant directly from the complex numbers. **TO BE CONTINUED**

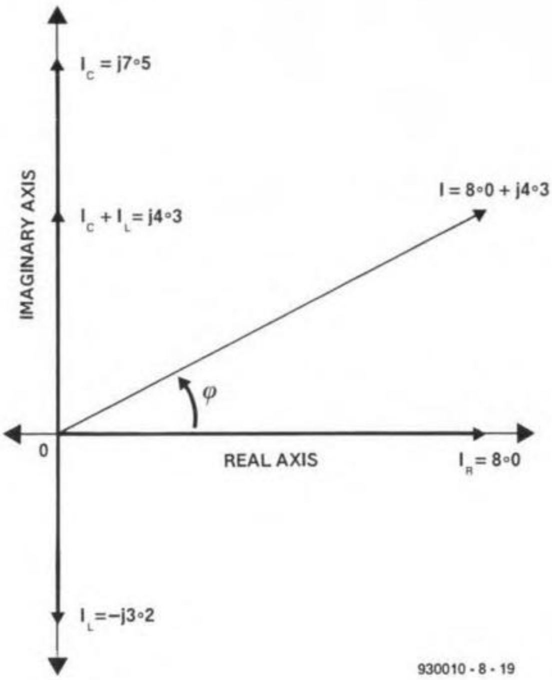


Fig. 75.

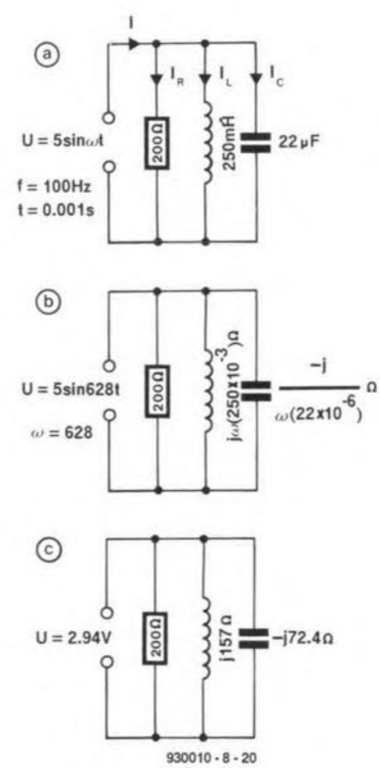


Fig. 76.

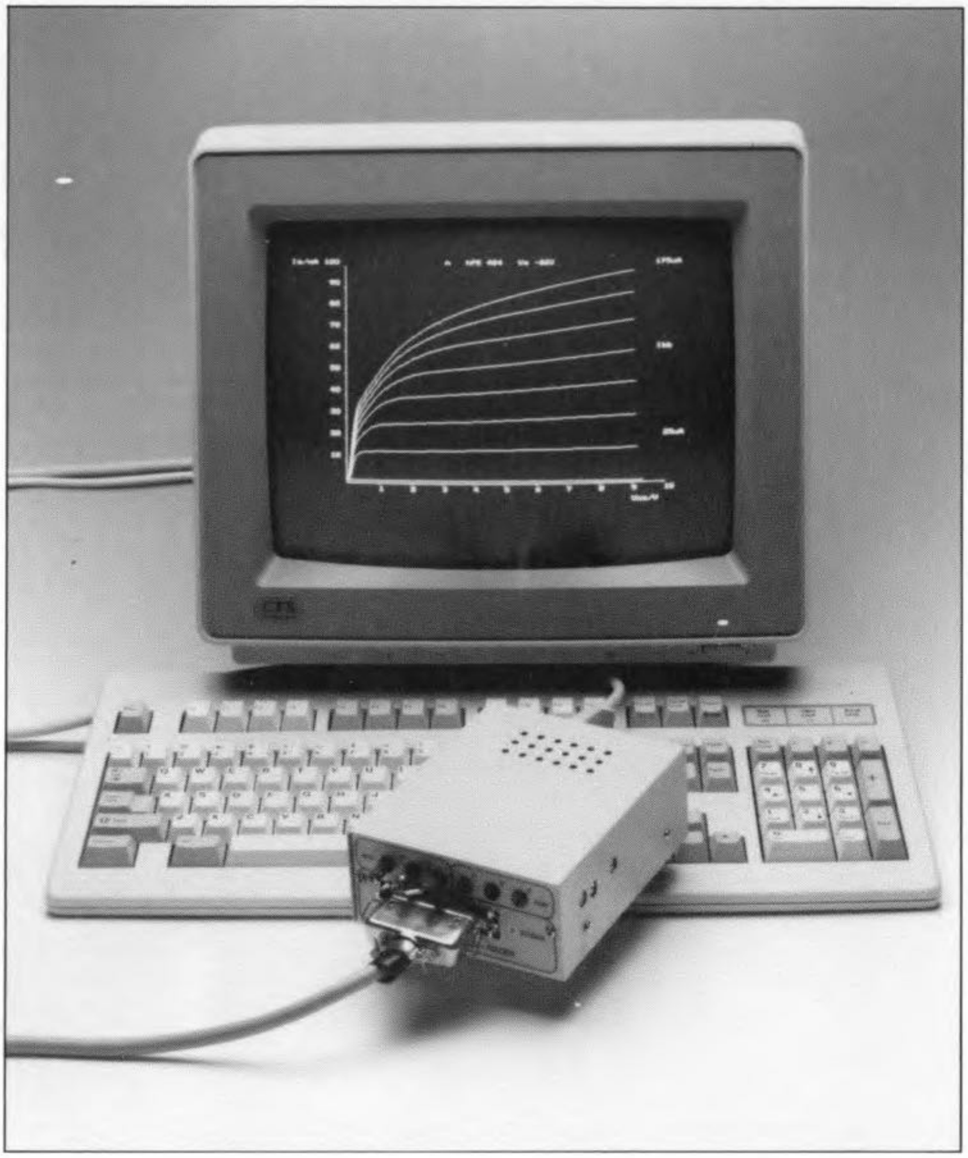
Test yourself

1. Add $(3+\mathbf{j}2)$ to $(6+\mathbf{j}3)$.
2. Add $(7+\mathbf{j})$ to $(3-\mathbf{j}4)$.
3. Add $(5.2-\mathbf{j}0.3)$ to $(-3.6-\mathbf{j}2.3)$.
4. Subtract $(4-\mathbf{j}2)$ from $(5+\mathbf{j}6)$.
5. Multiply $(3+\mathbf{j}4)$ by $(7+\mathbf{j}3)$.
6. Multiply $(5-\mathbf{j}3)$ by $(3+\mathbf{j})$.
7. What is the complex conjugate of $(4+\mathbf{j}5)$?
8. Divide $(3+\mathbf{j}2)$ by $(7+\mathbf{j}3)$.
9. In an LCR circuit (Fig. 74), $R=120\ \Omega$, $L=0.1$ H; $C=47\ \mu F$, $f=50$ Hz and $U=2\sin\omega t$. Calculate the current vectors and their resultants.
10. Recalculate the current vectors and resultants in the circuit of question 9 when the frequency is increased to 150 Hz. What are the magnitudes of U and I when $t=2$ s?

Answers to Test yourself (Part 7)

1. $U_A = 3.074$ V
   $U_B = -2.272$ V
   $U_D = 1.185$ V
   $I_{AC} = 0.741$ A
   $I_{AD} = 1.259$ A
   $I_{DC} = 0.395$ A
   $I_{DB} = 0.864$ A
   $I_{CB} = 1.136$ A
2. $I_N = -1.262$ A
   $G_N = 0.4309$ S
   $I = -0.463$ A
3. Perform nodal analysis at B and C; calculate U_B and U_C;
   $U_B = 232.1\times10^{-9}$ V
   $U_C = -0.172$ V
   voltage gain $= -0.172/0.01$
   $= 17.2$

PC-AIDED TRANSISTOR TESTER



The advantage of having a computer run gain tests on transistors is that you do not need an oscilloscope to view the characteristics. The circuit presented here is based on an earlier design, published about three years ago. This has been enhanced with a p-n-p test function, an on-board power supply, and a control program for IBM PCs and compatibles.

Design by S. Aaltonen

THE sheer simplicity of the n-p-n transistor tester described in Ref. 1 made it a wonderful little instrument. However, the circuit had two important disadvantages: firstly, it was unable to test p-n-p transistors, and, secondly, it could not be used on IBM PCs and compatibles for lack of appropriate software, which was only available for monochrome Atari ST computers. In retrospect, it was not so difficult to add the p-n-p test function. All that had to be added were three transistors, nine resistors and a small negative supply that provides the base current for the p-n-p transistor. These components may be found back in the block diagram (Fig. 1), where they form the DAC (digital-to-analogue converter) that supplies the base current to the p-n-p transistor. The remaining parts were already contained in the original design.

The curve tracer is controlled by the PC via the Centronics (printer) interface. Six data lines on the interface are used to control a counter and an A-D converter, while one of the handshake lines serves as an input via which the PC reads the ADC output data. In effect, the direction of the data on the Centronics interface is the same as that when a printer is connected.

The counter controls the measurement process. Eleven bits are under the control of two lines (clock and counter reset) on the Centronics interface. These 11 bits eventually control the measurement. During one complete measurement cycle, the counter is allowed to count from 0 to 4,095. The first eight bits control the DAC that supplies the collector-emitter voltage (U_{CE}) for the transistors under test. The remaining three (MS) bits determine the base current. During a measurement cycle, the base current is increased from 0 µA to 175 µA in steps of 25 µA. At each step of the base current, U_{CE} is increased from 0 V to 9 V in 256 steps.

As shown in the block diagram, the collector current, I_C, of the transistor under test causes a voltage drop across a series resistor. This voltage is first amplified and then applied to an A-D converter. Note, however, that the system actually measures the emitter current, I_E, when an n-p-n transistor is connected. Fortunately, that is not a problem because the computer is perfectly capable of calculating the collector current with the simple formula

$$I_C=I_E-I_B.$$

Circuit description

After the discussion of the block diagram, the circuit diagram (Fig. 2) has few surprises. In fact, we need only look at the operation of the DACs and the power supply, since not much else has changed with respect to the earlier design (Ref. 1).

The DAC that generates U_{CE} consists of an integrated 8-bit D-A converter (IC_2), an opamp-based amplifier (IC_{3a}) and a driver (T_1). The DACs that supply the base current are built from discrete components. The base current generator for n-p-n transistors is the simplest. Resistors R_8-R_{11} convert the voltage represented by three bits on counter IC_1 into a current. Diodes D_1, D_2 and D_3 ensure that this current can only flow via the base of the transistor under test, and not via an output bit that is at 0.

The base current (I_b) generator for p-n-p transistors is a little more complex. This is because the emitter voltage 'tracks' U_{CE}, and is not at (nearly) ground potential as with n-p-n transistors. To make sure that the transistor can be driven into conduction at a low U_{CE} value (the emitter is then virtually at ground potential), the base has to be made at least 0.6 V negative with respect to ground. This is achieved with the aid of a small auxiliary negative supply voltage, plus R12-R20, T2, T3 and T4. These components together form three small current sources that can be switched on and off by the three most significant bits of counter IC1. In this way, the base current for the p-n-p transistor is determined by the sum of the currents through the actuated current sources. The minimum level of the negative supply voltage is easily established from the base-emitter voltage of the p-n-p transistor (approx. 0.6 V), and the minimum voltage drop across the current sources (approx. 1 V). Thus, the minimum negative voltage required is −1.6 V, which leaves some headroom for the −1.8-V supply actually used.

Resistor R23 is the current sensing device. Since for reliable measurement results its value must remain comparatively low, it supplies a relatively small voltage. Whence the use of an amplifier, IC3b, which provides a gain of x48 before the signal reaches the A0 input of the A-D converter (IC4). The shape of this signal is shown in Fig. 3. In fact, you already see the seven successive lines of the characteristic (not including I_B=0). The peak value of this signal depends on the current gain of the transistor under test, and may not exceed 5 V (the supply voltage of IC4). Simple reverse calculation then tells us that the circuit can only handle transistors with a current gain smaller than 595, which corresponds to a maximum measurable I_C of 100 mA.

The collector voltage, U_{CE}, has to be reduced instead of amplified. This is done by R21 and R22, which halve the measured voltage to keep it within safe limits for the input of IC4.

The original design of the transistor curve tracer has two supply voltages: +5 V and +15 V. To these, one of −1.8 V is added for the present design. Also, the +15 V is increased to +16.3 V to obtain a slightly higher drive margin. These changes have led to a revised power supply section. The positive voltages are made in the conventional way: a mains transformer, a bridge rectifier, an adjustable voltage regulator for 16.3 V (IC5), and another voltage regulator that steps down the

MAIN SPECIFICATIONS

- Plots gain curves of n-p-n and p-n-p transistors
- Connects to Centronics port, using standard parallel printer cable
- Gain curves displayed on PC monitor
- On-board power supply
- Software for IBM PCs and Atari STs (monochrome)
- Collector-emitter voltage range: 0-9 V
- Max. collector current: 100 mA
- Collector current measured at 7 base currents between 0 and 175 μA
- Max. transistor gain: 595

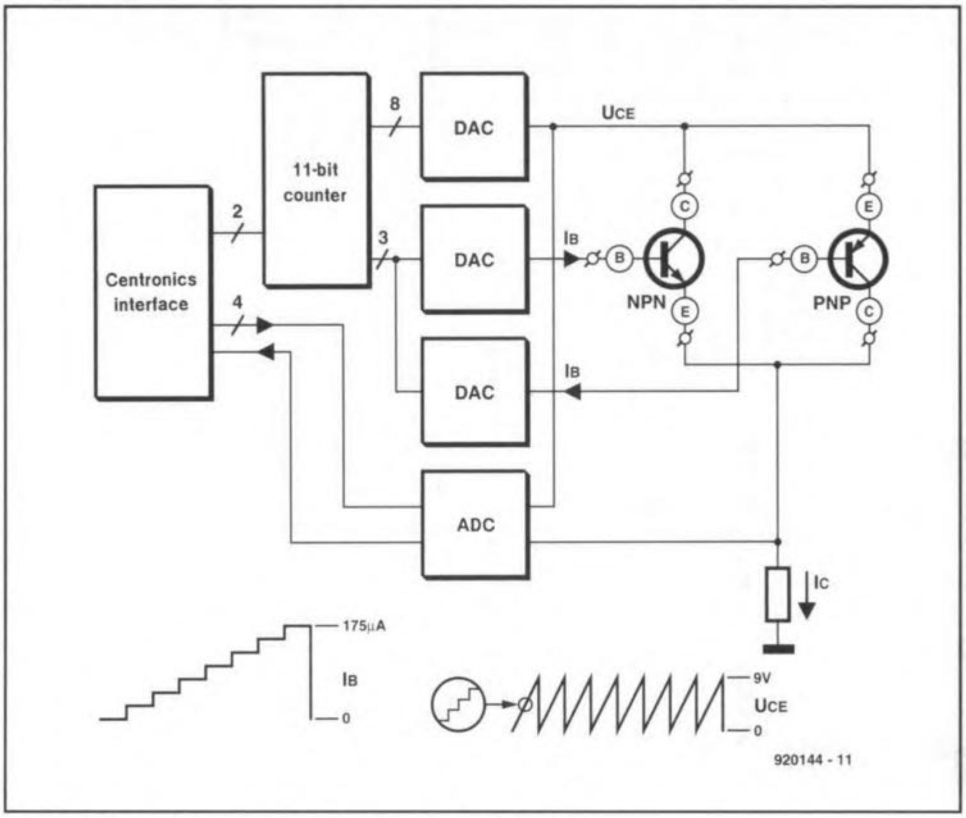
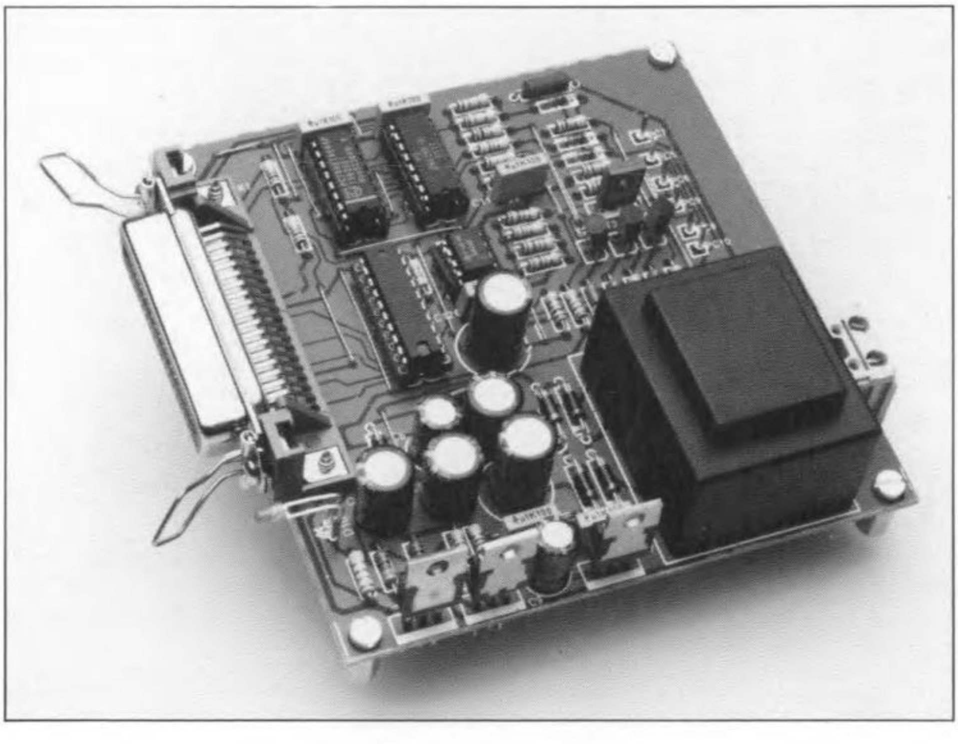


Fig. 1. Block diagram of the n-p-n/p-n-p transistor curve tracer.



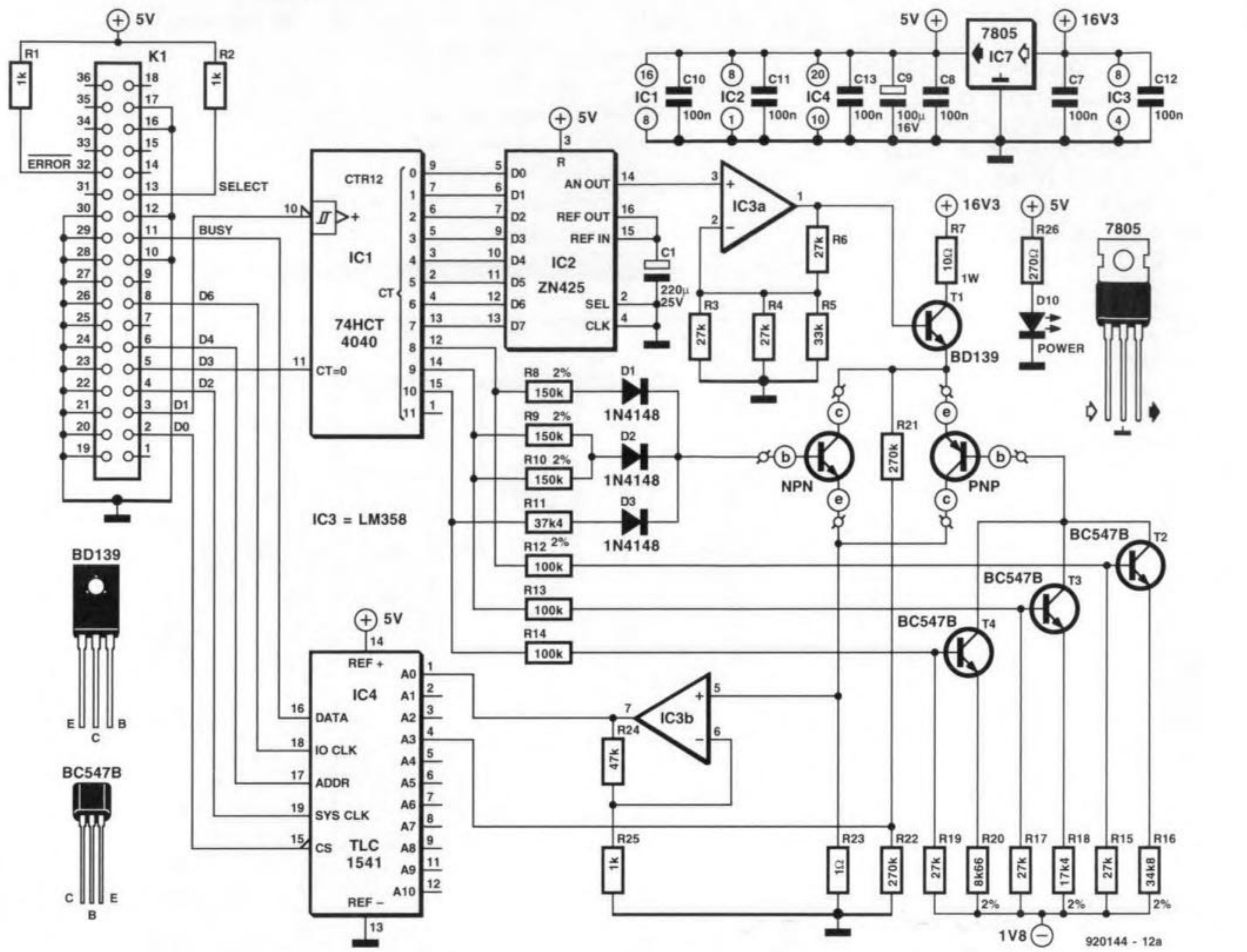


Fig. 2a. Circuit diagram of the computer-controlled transistor tester.

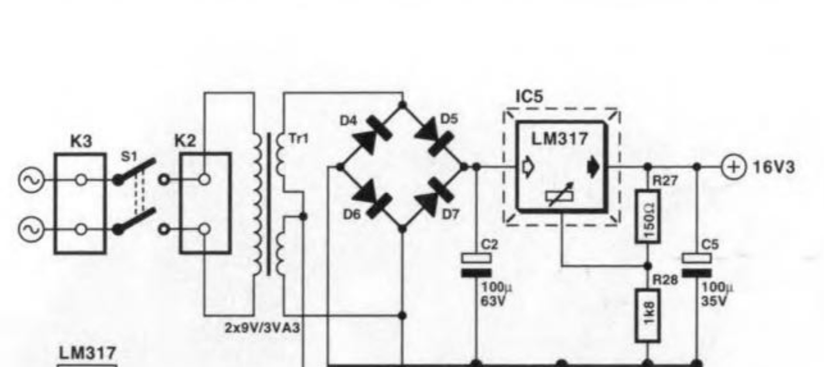


Fig. 2b. Three-voltage power supply for the transistor tester.

16.3 V to 5 V.

The negative voltage is supplied by C3, D8, D9 and IC6. Of the alternating current that flows through capacitor C3 (one half via D8, and the other, via D9), one half period is used to charge C4. C3 also ensures that no short-circuit is created for direct voltages. Next,

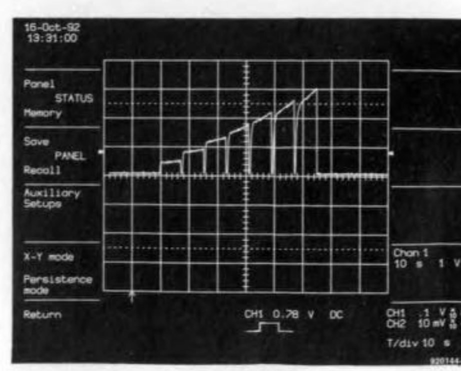


Fig. 3 The output signal of amplifier IC3b already describes the transistor gain characteristic, but the curves are arranged horizontally instead of vertically.

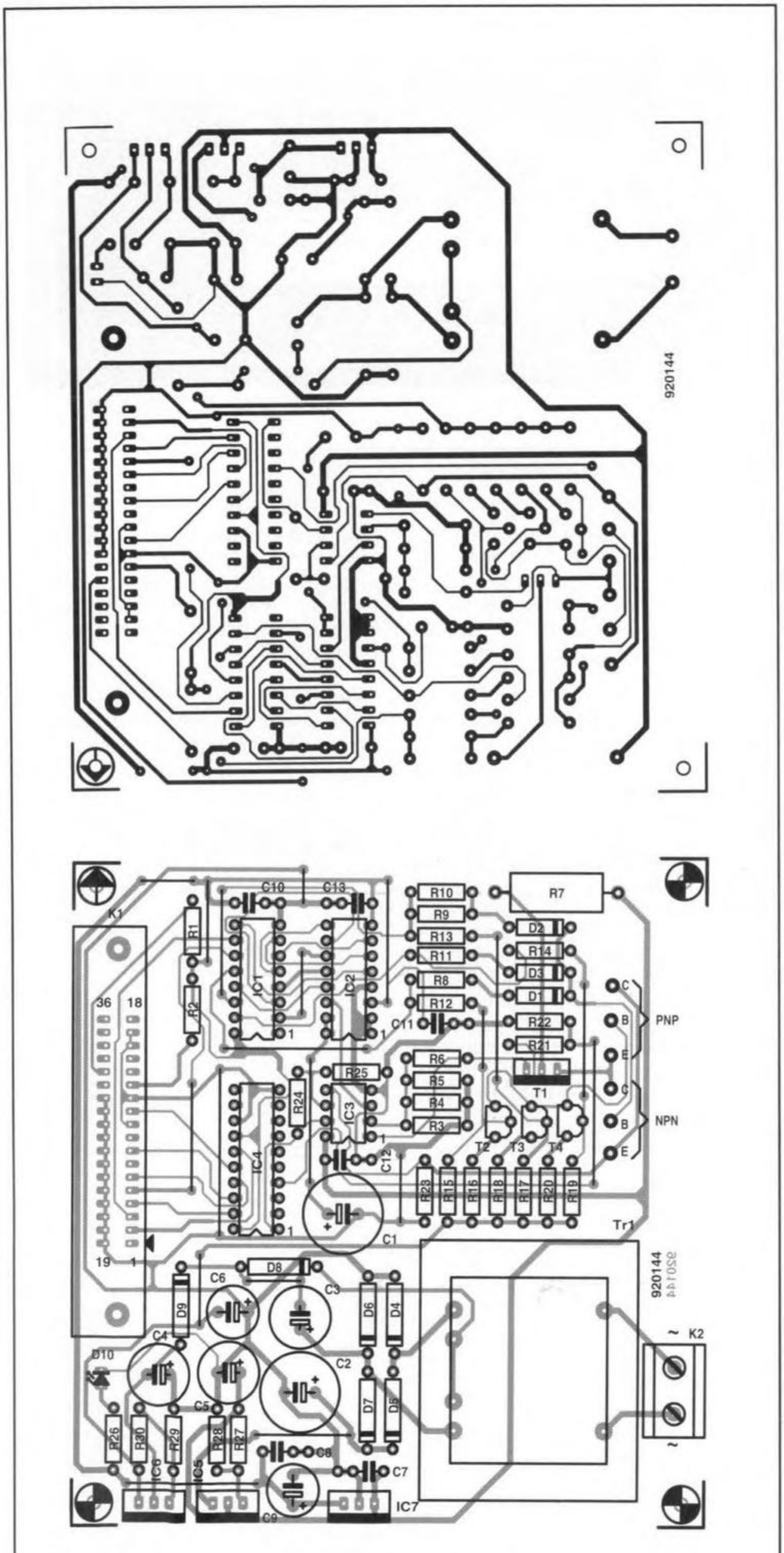


Fig. 4. Track layout and component mounting plan of the (single-sided) printed circuit board designed for the transistor tester.

COMPONENTS LIST

Resistors:

3	1kΩ	R1;R2;R25
6	27kΩ	R3;R4;R6;R15; R17;R19
1	33kΩ	R5
1	10Ω 1W	R7
3	150kΩ 2%	R8;R9;R10
1	37kΩ4 2%	R11
3	100kΩ	R12;R13;R14
1	34kΩ8 2%	R16
1	17kΩ4 2%	R18
1	8kΩ66 2%	R20
2	270kΩ	R21;R22
1	1Ω	R23
1	47kΩ	R24
1	270Ω	R26
1	150Ω	R27
1	1kΩ8	R28
1	150Ω 2%	R29
1	330Ω 2%	R30

Capacitors:

1	220μF 25V radial	C1
1	100μF 63V radial	C2
3	100μF 35V radial	C3;C4;C5
2	100μF 16V radial	C6;C9
6	100nF	C7;C8;C10-C13

Semiconductors:

3	1N4148	D1;D2;D3
6	1N4001	D4-D9
1	LED, red, 3mm	D10
1	BD139	T1
3	BC547B	T2;T3;T4
1	74HCT4040	IC1
1	ZN425	IC2
1	LM358	IC3
1	TLC1541	IC4
1	LM317	IC5
1	LM337	IC6
1	7805	IC7

Miscellaneous:

1	36-way PCB mount Centronics socket	K1
1	2-way PCB terminal block 7.5mm pitch	K2
1	Mains socket (optionally inclusive of S1)	K3
1	Mains-rated double-pole switch 2A	S1
1	Mains transformer 2x9V/3.3VA, e.g.. Monacor/Monarch VTR3209	TR1
1	Heat-sink for IC7, 6.5K/W, see text	
2	2-mm dia banana socket, blue (C)	
2	2-mm dia banana socket, black (B)	
2	2-mm dia banana sockets, red (E)	
1	Enclosure, dim. 115x50x135mm (e.g., ESM EB11/05)	
1	Control software on diskette (for Atari and MSDOS); order code 1781 (see page 78)	
1	Printed circuit board 920144 (see page 78)	

the voltage across C4 is stepped down to −1.8 V by an LM337 regulator, IC6. The regulator output voltage is determined by resistors R29 and R30.

Printed circuit board and software

All components, except the mains switch, the mains socket, the transistor test sockets and the on/off LED (D10) are accommodated on the printed circuit board (Fig. 4). Apart from the components, there are quite a few wire links to be fitted on to the board. The mains socket and mains switch have to be wired with due respect to electrical safety. The specified transformer is a short-circuit proof type, which obviates a fuse. A heat-sink is not required on IC7 if you use the metal enclosure mentioned in the parts list. All three regulators may be bolted on to the side panel with insulation sets (consisting of a mica washer, a plastic bush, a nut and a bolt). The bolts in these sets are best replaced by types with a countersunk head. This allows the case cover to be fitted without problems. If you use an enclosure without a metal side panel, a small heat-sink (approx. 6.5 K W^{-1} or better) is sufficient for IC7 to be kept reasonably cool. The two other regulators can make do without heatsinks.

If necessary, the operation of the circuit (and that of the DACs in particular) may be checked with the aid of an oscilloscope. Connect a square wave signal generator to the clock input of IC1, and hard-wire the reset input of this IC to ground. This causes the circuit to run the measurement cycle continuously, which makes testing, analysing and fault finding a lot easier. Be sure, however, to prevent the test transistor running too hot.

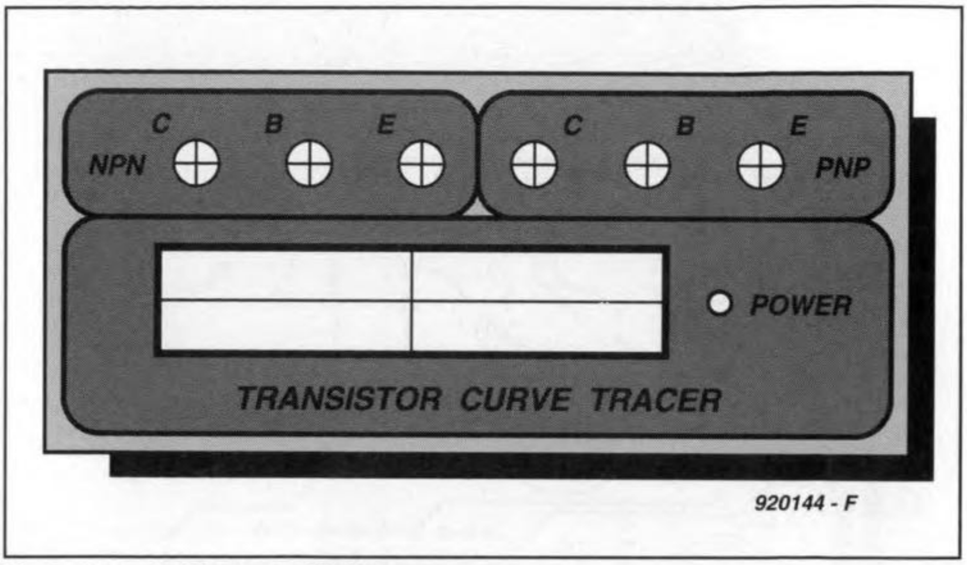


Fig. 6. Suggested front panel design.

Alternatively, write a program that generates a square wave on Centronics line D1, while keeping D3 low all the time. If you find that the Centronics lines fail to reach the proper '1' level, fit them with pull-up resistors (1-10 kΩ).

The floppy disk contains the files NP3ENG.TOS, NP3ENG.EXE and HERC.BGI. The TOS file is intended for Atari ST computers with a monochrome screen, while the EXE file is for IBM PCs and compatibles. Although it produces a black-and-white picture only, the program works with EGA and VGA display adaptors. Compatibility with a Hercules card is ensured by the HERC.BGI file.

The program gives reports to signal a number of fault conditions, including: curve tracer not connected; curve tracer switched off; and no transistor connected. For the rest, the operation of the program is self-evident, and requires no detailed descriptions. After writing the transistor curves on to the screen, the program halts until a key is pressed, and has to be started again for a new test to be run. This may be done automatically by an appropriate batch file. ■

Reference:

1. Transistor characteristic plotting. *Elektor Electronics* May 1990.

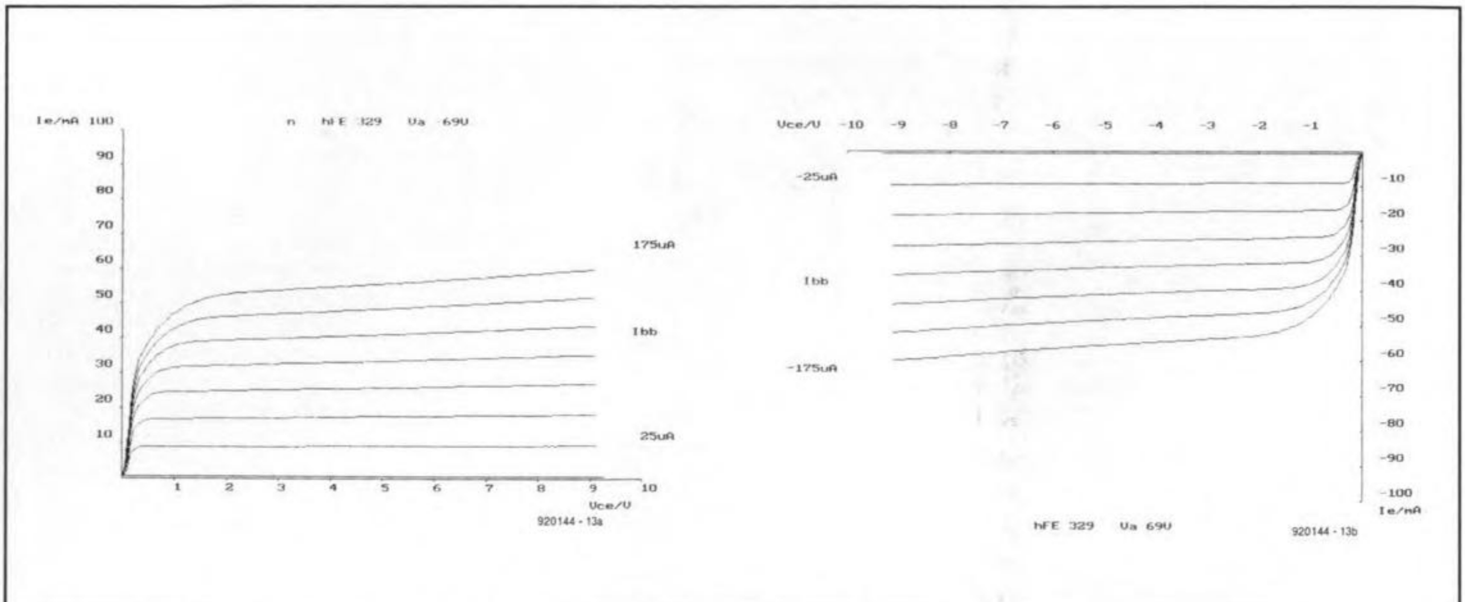
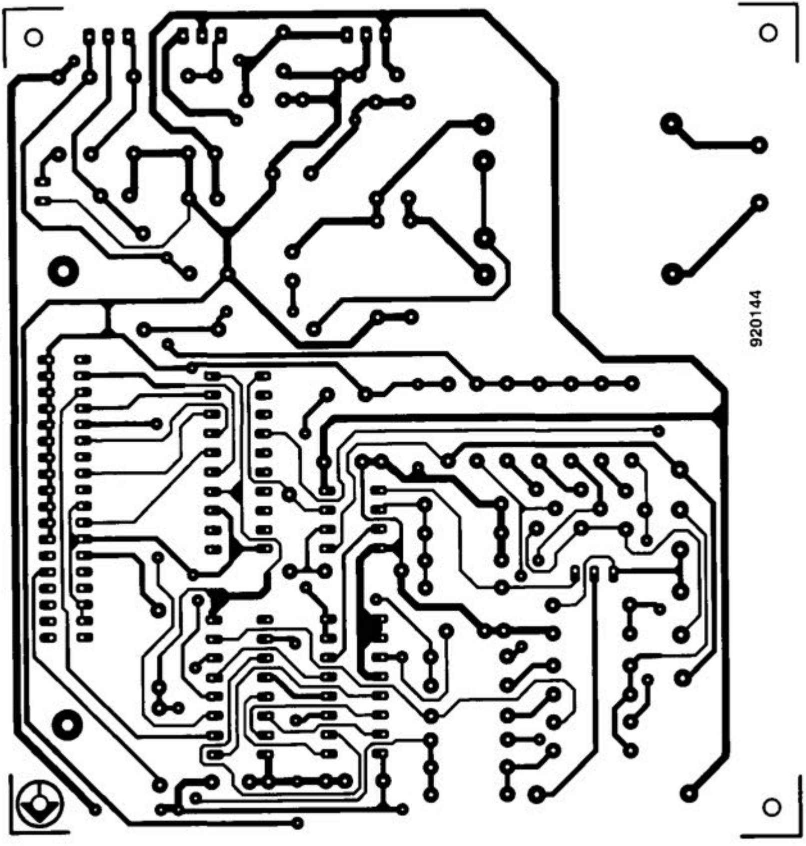
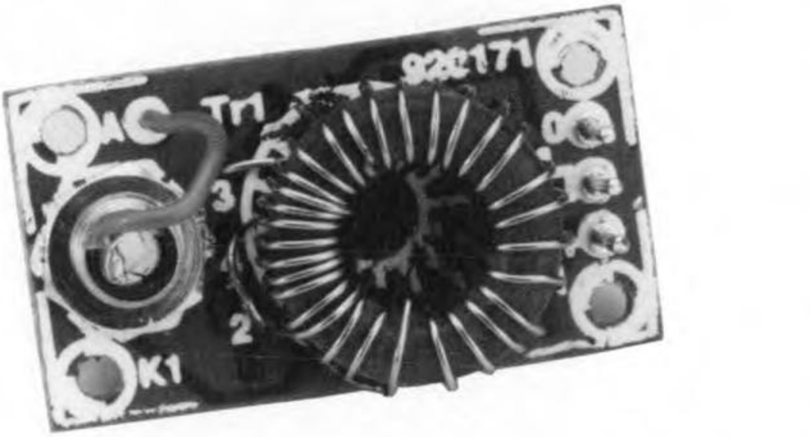


Fig. 4. Examples of gain curves plotted on the PC screen for an n-p-n (left) and a p-n-p (right) transistor.


920144

DIGITAL OUTPUT FOR CD PLAYERS

Design by T. Giesberts



Not all CD players have a digital output, which is a must if the player is to be connected to an external DAC or digital recorder. Since in many of them the digital signal is internally available, this article describes how a small circuit enables a digital coaxial output to be added in a simple manner.

Not only older, but also many modern (inexpensive), compact disc players have no digital output. Interestingly, some of the latter ones have an optical output, but as we have shown in an earlier issue[1], such outputs are not always ideal either: in fact, often a coaxial link is to be preferred. If your CD player has an optical output, the circuit described here will enable you to add a coaxial output in a straightforward manner. If not, it depends on the chip set used in the player whether a digital output can be added or not.

Biphase modulation

Since the early 1980s, standard data transmissions in consumer equipment make use of biphase modulation that renders the digital signals, which contain the bits to be transmitted, into S/PDIF (Sony/Philips DIgital Format). This format has become the basis of international standards IEAJ CP-340 and IEC 958 for all digital outputs, be they CD, DAT, DSR ore DCC.

The signals are modulated by a clock, which results in the biphase mark signal—see **Fig. 1.** In this signal, a logic 1 is represented by a high–low, or a low–high, transition halfway through the bit to be sent, and a logic 0 by the absence of such a transition. In this way, the 1s and 0s are represented not by levels but by the distances between individual transitions. The advantage of such a signal is that it contains not only the data, but also the clock rate at which the data are transmitted. Knowing this rate is essential for the processing of the data after reception.

The bandwidth of the signal ranges from 0.7 MHz to 3 MHz at data rates of 2048, 2822 and 3072 bits (clock frequency times 2 samples of every 32 bits in, respectively, CD, DSR and DAT signals).

The output level has been standardized at 0.5 V_{pp} (terminated output), and the input and output impedances at 75 Ω.

In an audio DAC (digital-to-analogue converter), the S/PDIF signal is converted back to the usual logic (1, 0) levels, which are then processed in a traditional manner. The reconversion is carried out by a special chip, called an ADIC (audio digital integrated circuit). Examples of this are Yamaha's YM3623B, the SAA7274 and TDA1315H from Philips, and Sony's CX23053

It depends on the ADIC used in a CD player whether a coaxial output can be added. Some of these ICs provide a standard output at which the S/PDIF signal is available. The addition of a buffer and an isolation transformer enables the signal to be output at the correct level and electrically isolated from the electronics in the CD player. A number of such ADICs are listed in **Table 1**.

Yamaha produces several types, most of which are based on their signal pro-

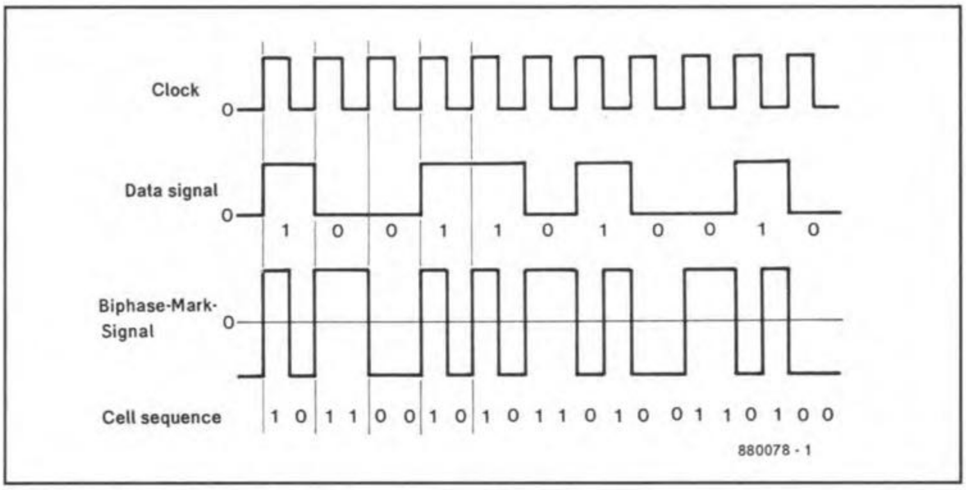


Fig. 1. In signals of the S/PDIF format, the data are biphase modulated.

Type	Manufacturer	Enclosure	DOBM/Ground
YDC101(B)	Yamaha	80-pin flatpack	pins 23, 29
YM347C	Yamaha	16-pin DIP	pins 16, 1
YM7121B	Yamaha	80-pin flatpack	pins 23, 29
SAA7220	Philips	24-pin DIP	pins 14, 12
SAA7340	Philips	80-pin flatpack	pins 32, 33
SAA7341	Philips	80-pin flatpack	pins 32, 33
SAA7345	Philips	44-pin flatpack	pins 2, 15
CXD1165Q	Sony	80-pin flatpack	pins 27, 12
CXD2500(A)Q	Sony	80-pin flatpack	pins 60, 52

Table 1. Pin numbers of the digital output of various ADICs.

cessor/controller/RAM ICs Type YDC101 and YM7121. Both these types have an output for a standard format digital audio signal. Audio processor YM7402, used in a number of multi-disc units, also has a digital output. The YM3437C is a converter IC for digital audio data: it can convert several formats into the standard format. The resulting signal is available at pin 16 of the chip.

Most Philips' ADICs, from the 2nd generation SAA7220 to the latest Type SAA7345, have a digital output biphase mark (DOBM) output. An exception is the SAA7310, to which an audio digital output circuit (ADOC), normally a Type PCF3523, must be added before a buffer and isolation transformer can be connected.

Sony's processor Type CXD1165Q, used in older equipment (providing a digital outlet), has a digital output. The output signal is synchronized via a bistable with a 4 MHz oscillator. In newer equipment, which uses processor Type CXD2500(A)Q, the output of the chip is taken to an output socket without this synchronization. In modern players, the processor arranges the muting of the audio signal, but in older equipment this is often done via an additional gate at the relevant output. In such equipment it may, therefore, be necessary to derive the muting from a source outside the processor.

Whatever type of CD player you have, a service manual is required to inspect the electronics meaningfully. The manual will tell you how the muting signal is generated. All we can tell you is that in players that use the Type CXD1124S filter the muting signal is available at pin 23 of this filter.

Output buffer

The digital output of an IC cannot be used without some precautions since, owing to the standard low impedance (75 Ω) of digital inputs and outputs, it is easily overloaded. Moreover, electrical isolation and a correct voltage level are needed. These requirements are met by the circuit in **Fig. 2**, which consists of a buffer stage followed by an isolating transformer. The circuit can be connected directly to the DOBM or DIF (digital interface format) output of any of the ICs mentioned.

Buffering is provided by six-fold inverter Type 74HC04. One gate inverts the signal, which is then used to drive the other five gates. These gates are connected in parallel and invert the signal anew. This arrangement makes it possible for an output current of up to 100 mA to be drawn.

Capacitor C_1 and the primary of transformer Tr_1 form a high-pass filter to prevent low-frequency constituents of the signal getting on to the digital link. The data signal (0.7–3.0 MHz), is thus free of low frequencies.

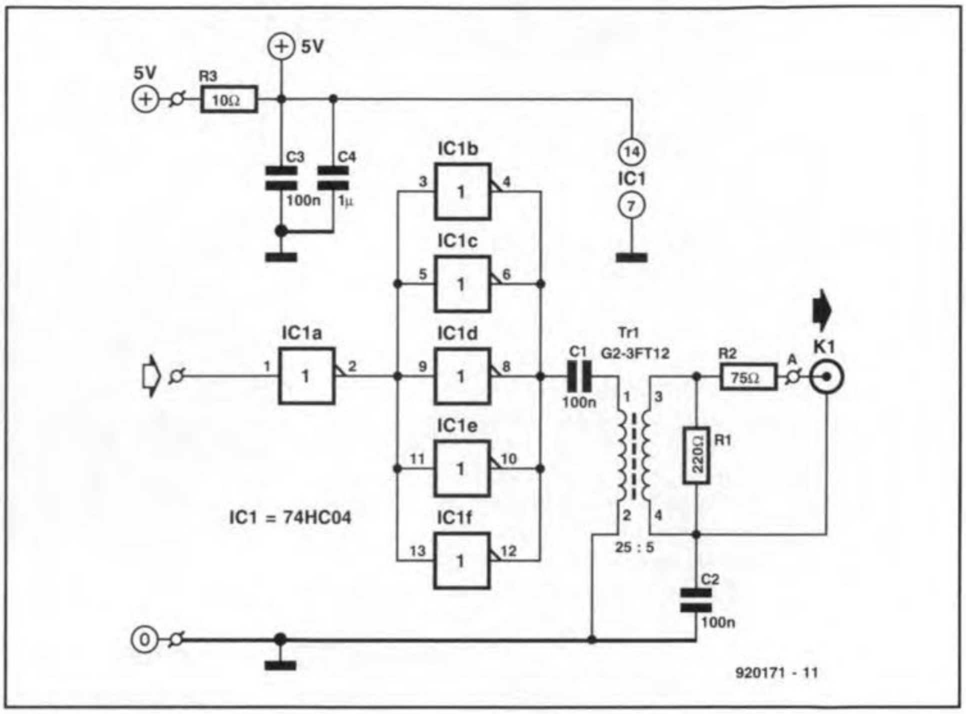


Fig. 2. Circuit diagram.

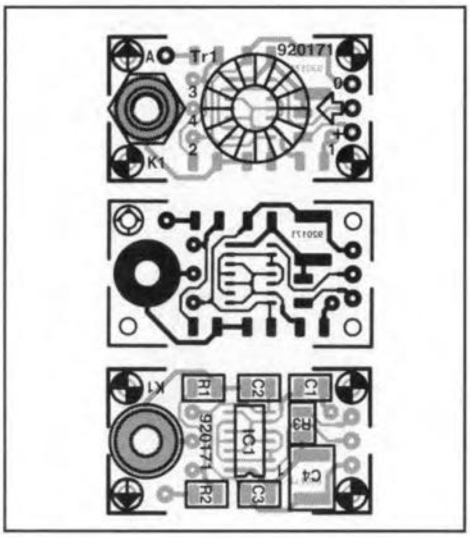


Fig. 3. Printed-circuit board.

PARTS LIST
(All SMD components, except Tr_1)

Resistors:
R_1 = 220 Ω
R_2 = 75 Ω
R_3 = 10 Ω

Capacitors:
C_1, C_2, C_3 = 100 nF, ceramic
C_4 = 1 µF

Semiconductors:
IC_1 = 74HC04

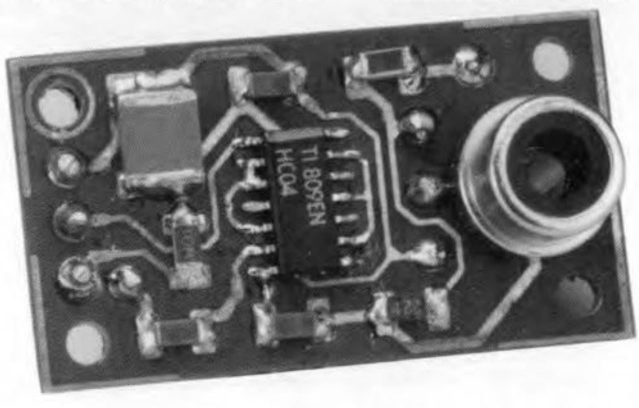
Miscellaneous:
K_1 = Coaxial socket for PCB mount
Tr_1 = 25 & 5 turns of 0.5 mm dia. enamelled copper wire on a G2-3FT12 core

The isolation transformer reduces the signal level from 5 V_{pp} at the primary to about 1 V across the secondary. Resistor R_2 ensures that the output impedance is 75 Ω. A 75-ohm output cable and R_2 form a 1:1 voltage divider so that the voltage across the load is 0.5 V_{pp}.

Resistor R_1 prevents any tendency to high-frequency oscillating when the output is not loaded.

Capacitor C_2 links the ground of the circuit to the screen of the output cable, so that, as far as a.c.is concerned, the cable does not float although there is proper electrical isolation.

Resistor R_3 and capacitors C_3 and C_4



decouple the supply line.

Construction and fitting

The circuit is best built on the PCB shown in **Fig. 3**. To keep it as small as possible, and thus ensure straightforward fitting into an existing apparatus, all components, except the transformer, are surface-mount devices (SMDs).

The transformer is made by close-winding 25 turns of 0.5 mm dia. enamelled copper wire on to the toroidal core (see **Fig. 4**). Then wind five turns of the same type of copper wire over a width of about 5 mm ($^3/_{16}$ in) over one end of the primary. The numbers at the terminals correspond with numbers on the PCB. It is essential that the specified core is used to ensure the transformer performs correctly.

Populating the board is best started with the coaxial socket, followed by the transformer. Do not use too much heat when soldering the nut of the socket to prevent melting of the insulation in the socket.

Solder the SMDs with a fine-tipped iron at a temperature not exceeding 275 °C. This work is not difficult, but requires precision and patience.

Where to fit the circuit in an existing equipment depends on the type of CD player. The best position is undoubtedly at the inside rear panel so that the coaxial socket can be made accessible through a hole in this panel.

The board must be linked to the digital output of the relevant IC (DOBM or DIF) by a short length of thin coaxial cable.

The supply for the circuit can normally be taken from the supply to the player electronics via two lengths of insulated circuit wire. **END**

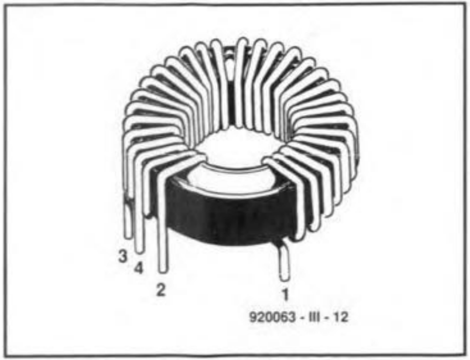
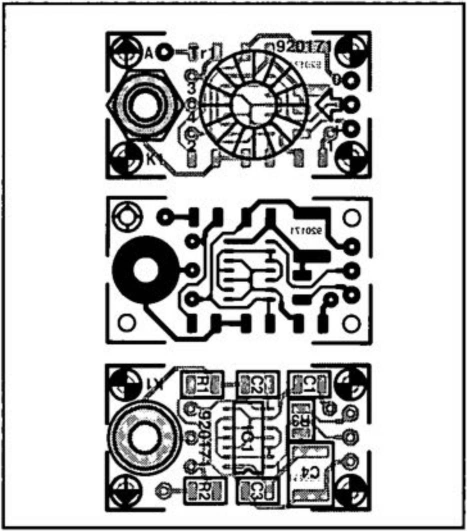


Fig. 4. Transformer on G2-3FT12 toroid.

[1] 'Digital-audio enhancer', *Elektor Electronics*, February 1993.



A
Tr1
920171
3
4
2
1
K1
R1
C2
C1
R3
IC1
C4
R2
C3

THE ANALOGUE SUBSYSTEM — PART 2

INTERFACING SENSORS AND OTHER SIGNAL SOURCES TO ELECTRONIC CIRCUITS

By Joseph J. Carr, M.Sc.

Sensors are used to measure physical parameters by producing an output current or voltage signal that represents that parameter. For example, a thermocouple produces a voltage that is proportional to the temperature at the junction of two dissimilar metals. Similarly, a piezo-resistive strain gauge produces an output voltage that is proportional to strain on a resistance element, which in turn is proportional to an applied displacement, force or pressure. While the number of different sensors is large and varied, there are only a few different forms of sensor output circuit configuration. These forms must be properly matched to the input of the circuit that follows the sensor, or trouble will result.

Sensor output circuit forms

Figure 8 shows an array of several different forms of sensor circuit. In each circuit, a current source, source resistance (R), and (in some) a voltage source are shown. Figure 8a shows the standard **single-ended grounded sensor**.[1] The term 'single-ended' means that one side of the sensor circuit is grounded. If neither side is grounded, then the sensor is said to be a **single-ended floating sensor** (Fig. 8b). In the single-ended sensor, the output signal is referenced either to ground or a single common, non-grounded, point. This form is sometimes subject to massive interference from external fields, especially in the presence of strong audio frequency (AF), radio frequency (RF) or 50 or 60-Hz power line fields. A variant of the single-ended floating sensor is the **single-ended floating driven off ground sensor** shown in Fig. 8c.

If a sensor drives the output through equal resistances, it is said to be **balanced**. Figure 8d shows an example of a **balanced grounded sensor**. In this form of output circuit, the sensor is referenced to ground through two equal resistances (both designated R). The version shown in Fig. 8e is an example of a **balanced floating sensor**. That is, the sensor is connected to a non-grounded common point ('A'), and outputs through two equal resistances (R). The important point in the balanced floating sensor is that it is both balanced **and** ungrounded. Finally, in Fig. 8f we see the **balanced driven off ground sensor**.

Amplifier input circuit types

The output circuit of the sensor is usually connected to a signal processing circuit, most frequently an amplifier of some sort (although certain other circuits are also used occasionally). Unfortunately, there are several types of amplifier input circuit, and not all sensors can be easily interfaced with all types of amplifier input circuit. Figure 9 shows four basic types of input circuit. Figure 9a shows the Type I circuit, i.e., one that is a **single-ended** input amplifier. The input circuit is modelled as a resistance to ground. Figure 9b shows the Type II circuit, which is modelled as a pair of **differential inputs** that each sees equal resistances to ground. In both cases, the output circuit is a voltage source in series with an output resistance. Figure 9c shows the Type III input circuit, which is **single-ended floating and shielded**. The input resembles the regular single-ended input (Fig. 9a), but the input is grounded and protected from interference by a shield. Finally, in Fig. 9d we see the Type IV input circuit. This circuit resembles the Type II, except that the input circuit is protected by a shield, is floating, and is **guarded** (of which, more later).

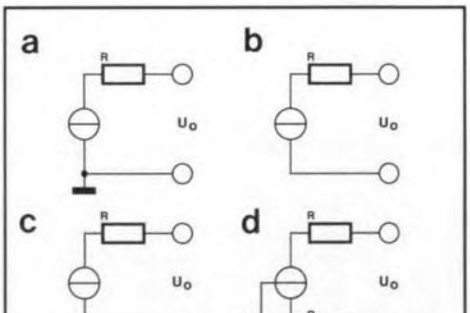


Fig. 8. Types of sensor circuit: a) single-ended grounded sensor; b) single-ended floating sensor; c) single-ended floating driven off-ground; d) balanced grounded sensor; e) balanced floating sensor; f) balanced driven off-ground.

Matching sensors and amplifiers

One cannot simply connect the various forms of sensor to the various types of amplifier input circuit willy-nilly without some thought about the matter. Figure 10 shows a general table relating the sensor and amplifier circuits. A 'yes' in a block means the combination (row vs. column) is recommended. A 'no' means that there are problems in that particular combination, so it is not recommended.

There are two combinations where it may or may not work, depending on the circumstances, so some degree of caution is required. For example, mixing a Type I input circuit with a Form A sensor output circuit requires consideration of signal levels. Do not use it when the output of the sensor is in the microvolt or millivolt range. Also, it is not a good idea to mix two grounds, i.e., one each on the amplifier and the sensor. Either eliminate one of the grounds, or join them together in a 'single point' (also called 'star') ground. A similar problem occurs when interfacing a Form A sensor and a Type II amplifier input. Some differential amplifiers can be converted into a single-ended amplifier, but one must be certain in each case.

Practical sensor amplifiers

Sensor amplifiers can easily be constructed from operational amplifier ICs, or certain other linear amplifier IC devices. There are three basic forms of amplifier that are useful for sensor interfacing: **single-ended** (Fig. 11), **differential** (Fig. 12), and **isolated** (Fig. 13).

Single-ended amplifiers

Figure 11 shows three variations on the single-ended amplifier. The circuit of Fig. 11a is an op-amp **inverting fol-**

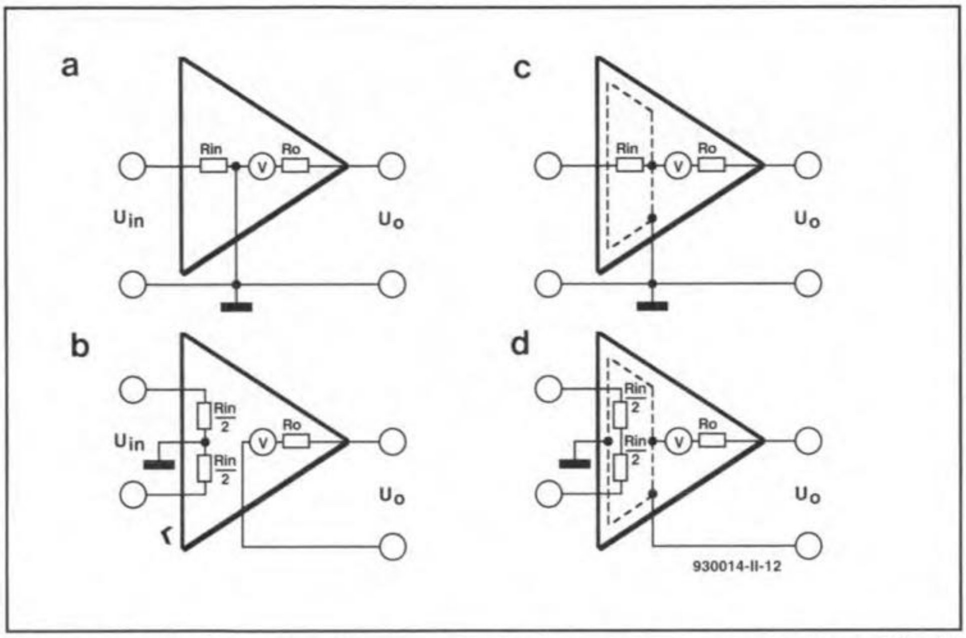


Fig. 9. Four basic types of amplifier input circuit: a) Type I (single-ended input amplifier; b) Type II (differential inputs); c) Type III (single-ended floating and shielded); d) Type IV (single-ended, floating, shielded and guarded).

lower. The voltage gain is $-R2/R1$, and the input impedance is basically the resistance of $R1$. As with all op-amp voltage amplifier circuits, the output impedance is low. A **non-inverting unity gain follower** is shown in Fig. 11b. This circuit has a very high input impedance, a low output impedance (which means that impedance transformation takes place between input and output), and a voltage gain of one. The power (P) gain, however, is larger than one because U_{in} and U_o are equal, yet $R_{in}>>R_o$ (note: $P=U^2/R$). Finally, is the **non-inverting follower with gain** circuit. This circuit has the same attributes as the unity gain non-inverting follower, except that the voltage gain is $(R2/R1)+1$.

Differential amplifiers

A differential amplifier is one that has balanced inputs such that one input is inverting (–) and the other input is non-inverting (+). The inverting input produces an output signal that is out of phase with the input signal. The non-inverting input produces an output signal that is in phase with the input signal.

The main reason to use a differential amplifier is for interference suppression. In many systems, the input leads pick up 50-Hz signals from the power line fields that permeate all electrified buildings. In single-ended amplifiers, the 50-Hz interfering signal is treated as a valid input signal, just like the desired sensor signal. But in differential amplifiers, the two leads are affected **equally** by the field, so present equal input signals to the (–) and (+) inputs. This type of signal is called a **common mode signal** because it affects both inputs equally. Because these inputs perform opposite each other, the net result is that the two output signal components due to the common mode signal, cancel each other. The degree to which common mode signals are suppressed by this mechanism in differential amplifiers is called the **common mode rejection ratio** (CMRR), which is usually expressed in decibels.

There are two basic configurations for differential amplifiers. The **dc differential amplifier** circuit, using one opamp device, is shown in Fig. 12a. The input resistors are balanced (R1=R2), as are the feedback resistors (R3=R4). The differential voltage gain of this circuit is R3/R1.

Input circuit type	Sensor signal form					
	A	B	C	D	E	F
I	see text	yes	no	no	yes	no
II	see text	yes	no	yes	yes	no
III	see text	yes	yes	no	yes	no
IV	see text	yes	yes	yes	yes	yes

Fig. 10. Table of compatibility between input and output types (see Figs. 8 and 9). A 'yes' denotes a recommended combination, a "no" denotes a combination that is not recommended.

If the resistors of the d.c. differential amplifier are perfectly matched, the CMRR will be very high — of the order of the inherent CMRR of the op-amp device itself (70 to 120 dB). But any mismatch, even when due to resistor tolerances, will upset the balance and force the CMRR lower. This problem can be overcome by replacing $R4$ in Fig. 12a with a series combination of a fixed resistor (R4A in the inset) and a potentiometer (P1) connected as a rheostat. This network is adjusted by shorting the two inputs together, applying a signal (1 V_{ac} is good in most cases), and adjusting P1 for minimum output signal.

Limitations of the d.c. differential amplifier of Fig. 12a include a relatively low maximum gain, and a low input impedance (set by $R1$ and $R2$). But these problems are overcome in an advanced form of differential amplifier called the **instrumentation amplifier** (Fig. 12b). Several semiconductor companies make integrated circuit versions of this circuit in which all three amplifiers are in one package (often called 'ICIAs' for **integrated circuit instrumentation amplifiers**).

The instrumentation amplifier circuit has a very high input impedance, especially when the input amplifiers (A1 and A2) are either BiMOS or BiFET types (which use field effect transistor input stages). The two input amplifiers should be identical types, or (preferably) two sections of a dual or triple op-amp device.

In this amplifier, the assumption is that $R2=R3$, $R4=R5$, and $R6=R7$. As in the case of the d.c. differential amplifier, CMRR adjustment can be provided by making $R7$ a series combination of a fixed resistor and a potentiometer. The gain of the circuit is:

$$A_v = \left(\frac{2R2}{R1}+1\right)\left(\frac{R6}{R4}\right) \qquad (1)$$

It is common to use R1 as a **gain control**, but it is important to not allow the value of $R1$ to get too low. When $R1=0$, the gain tries to go to infinity and the amplifier will saturate. The input signals U_1 and U_2 are referenced to ground, so the differential input signal $U_d=U_2-U_1$. The common mode signal (if any) is shown as U_{cm}.

Isolation amplifiers

The isolation amplifier is one in which the input circuits (section 'A' in Fig. 13) are isolated from the output circuits (Section 'B') by an extremely high impedance ($\geq 10^{12}$ ohms). These devices are usually variants of differential amplifiers, but their purpose is to isolate the sensor circuit from the following electronics.

One very common application is in medical electronics where patient safety requires such isolation.[2]

Guard shielding

One of the properties of the differential amplifier, including instrumentation amplifiers, is that its CMRR tends to suppress interfering signals from the environment. When an amplifier is used in a situation where it is connected to an external signal source through wires, those wires are subjected to strong local 50-Hz ac fields from nearby power line wiring. Fortunately, in the case of the differential amplifier, the field affects both lines equally, so the induced interfering signal is cancelled out by the common mode rejection property of the amplifier.

Unfortunately, the cancellation of interfering signals is not total. There may be, for example, imbalances in the circuit that tend to deteriorate the CMRR of the amplifier. These imbalances may be either internal or external to the amplifier circuit. Figure 14a shows a common interface scenario. In this figure we see the differential amplifier connected to shielded leads from the signal source, U_{in}. Shielded lead wires offer some protection from local fields, but there is a problem with the standard wisdom regarding shields: it is possible for shielded cables to manufacture a valid differential signal voltage from a common mode signal!

Figure 14b shows an equivalent circuit that demonstrates how a shielded cable pair can create a differential signal from a common mode signal. The cable has capacitance between the centre conductor and the shield conductor surrounding it. In addition, input connectors and the amplifier equipment internal wiring also exhibits capacitance. These capacitances are lumped together in the model of Fig. 14b as C_{S1} and C_{C2}. As long

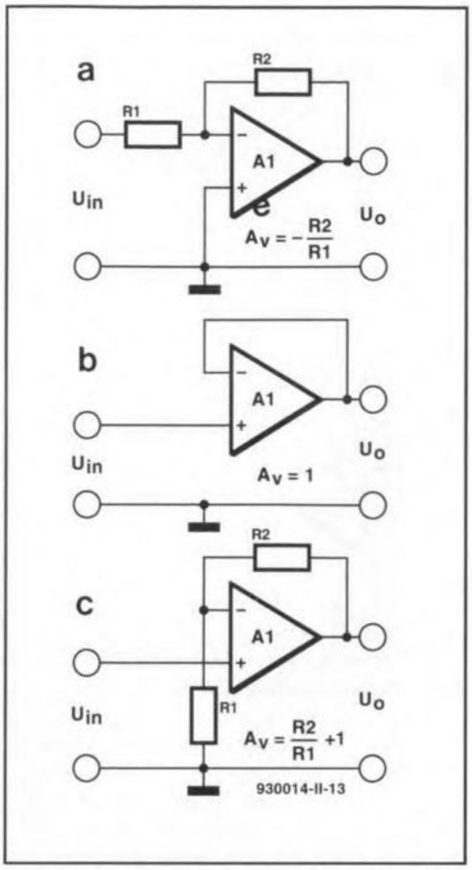


Fig. 11. Single-ended amplifiers: a) Inverting follower (op-amp); b) noninverting unity gain follower (op-amp).

as the source resistances and shunt resistances are equal, and the two capacitances are equal, there is no problem with circuit balance. But inequalities in any of these factors (which are commonplace) creates an unbalanced circuit in which common mode signal U_{cm} can charge one capacitance more than the other. As a result, the difference between the capacitance voltages, U_{CS1} and U_{CS2}, is seen as a valid differential signal.

A low-cost solution to the problem of shield-induced artifact signals is shown in Fig. 15a. In this circuit, a sample of the two input signals are fed back to the shield, which in this situation is not grounded. Alternatively, the amplifier output signal is used to drive the shield. This type of shield is called a **guard shield**. Either double shields (one on each input line) as shown, or a common shield for the two inputs, can be used.

An improved guard shield example for the instrumentation amplifier is shown in Fig. 15b. In this case a single shield covers both input lines, but it is possible to use separate shields. In this circuit a sample of the two input signals is taken from the junction of resistors R8 and R9, and fed to the input of a unity gain buffer/driver 'guard amplifier' (A4). The output of A4 is used to drive the guard shield.

Perhaps the most common approach to guard shielding is the arrangement shown in Fig. 15c. Here we see two shields used; the input cabling is double-shielded insulated wire. The guard amplifier drives the inner shield, which serves as the guard shield for the system. The outer shield is grounded at the input end in the normal manner, and serves as an electromagnetic interference suppression shield.

A related problem that is solved with guard shielding is seen in circuits were very high input impedance, very low bias current, amplifiers are used. Today it is possible to obtain operational amplifiers with 10^{12} ohms of input impedance, and input bias currents in the fractional picoampère region. In these amplifiers, the leakage currents normally found in any printed circuit material can actually exceed the leakage current of the amplifier. This situation becomes a problem in electrometer circuits, or any other place where an extremely high source impedance exists. Figure 16 shows how a guard ring on the printed circuit can be used to guard the inputs of the amplifier. The idea is to create a conductor ring around the input connections, and then connect

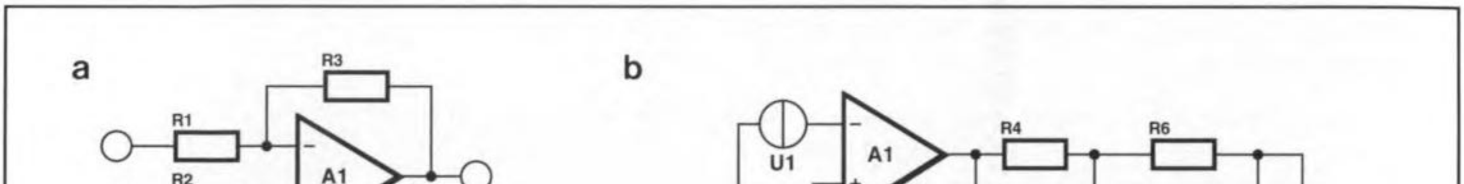


Fig. 12. Differential amplifiers: a) simple DC differential amplifier; b) instrumentation amplifier.

this guard ring to a low impedance point that is at signal potential levels. Figure 16a shows the connection of the guard ring to inverting amplifiers. The ring is connected to the grounded non-inverting input. Figures 16b and 16c show methods for use with non-inverting amplifiers. In both cases, the guard ring is connected to the inverting input of the op-amp.

AC-coupled differential amplifiers

There are some cases where instrumentation amplifiers need to be AC-coupled. Perhaps the most common problem is where a small amplitude AC signal is riding on a large DC component. An example is found in medical electronic devices such as the electrocardiograph (ECG). These instruments record the biopotentials waveforms generated by the heart activity. These signals tend to have peak amplitudes in the 1-mV region. But there is a real problem. The biopotentials are picked up with metal electrodes, usually made of silver-silver chloride (Ag-AgCl) material, that interface to electrolytic skin. In other words, the junction forms a battery. The half-cell potential of medical electrodes can be 500 to 1,000 mV, which is seen by the amplifier as a DC component creating an offset. Given that the weak signal needs to be amplified 1,000 times, the amplifier will quickly saturate when faced with the DC offset. Another example exists in optoelectronics. The usual situation for photodiodes and phototransistors is to have a weak light generated signal riding on a large static level.

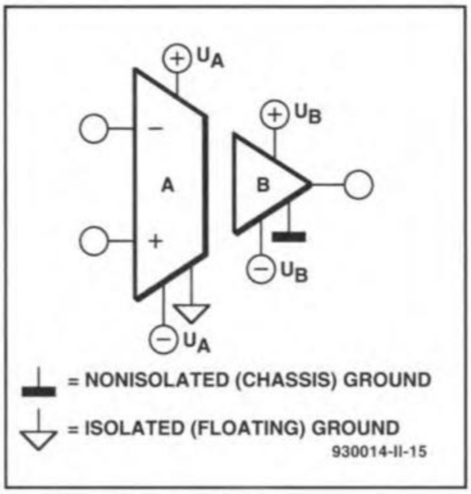


Fig. 13. Isolated amplifier.

There are a couple methods for stripping off the signal component, leaving behind the offset, so that it can be amplified and otherwise processed. Figure 17a shows an AC-coupled instrumentation amplifier, such as shown previously in Fig. 12b and 15b. Each non-inverting input (+IN) is coupled through a capacitor (C_a and C_b). If the amplifier is a very low bias current type, only the capacitors are needed. But most practical op-amps have an input bias current that cannot be ignored, and this current will charge the capacitors creating a second DC offset source. For most practical circuits, therefore, bleeder resistors (R_a and R_b) are needed. These resistors set the input impedance of the amplifier, so depending on the application should have values in the 100 kΩ to 10 MΩ region.

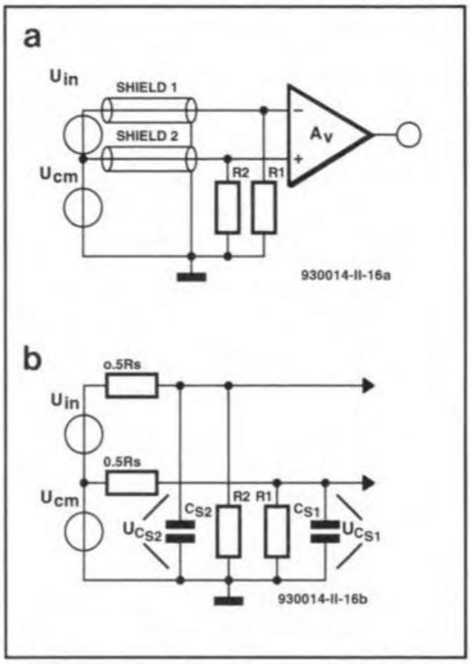


Fig. 14. a) Standard input configuration in which the differential amplifier inputs are connected to shielded leads from signal source; b) equivalent circuit showing distributed capacitances.

Maintaining the common mode rejection ratio (CMRR) of the differential in-

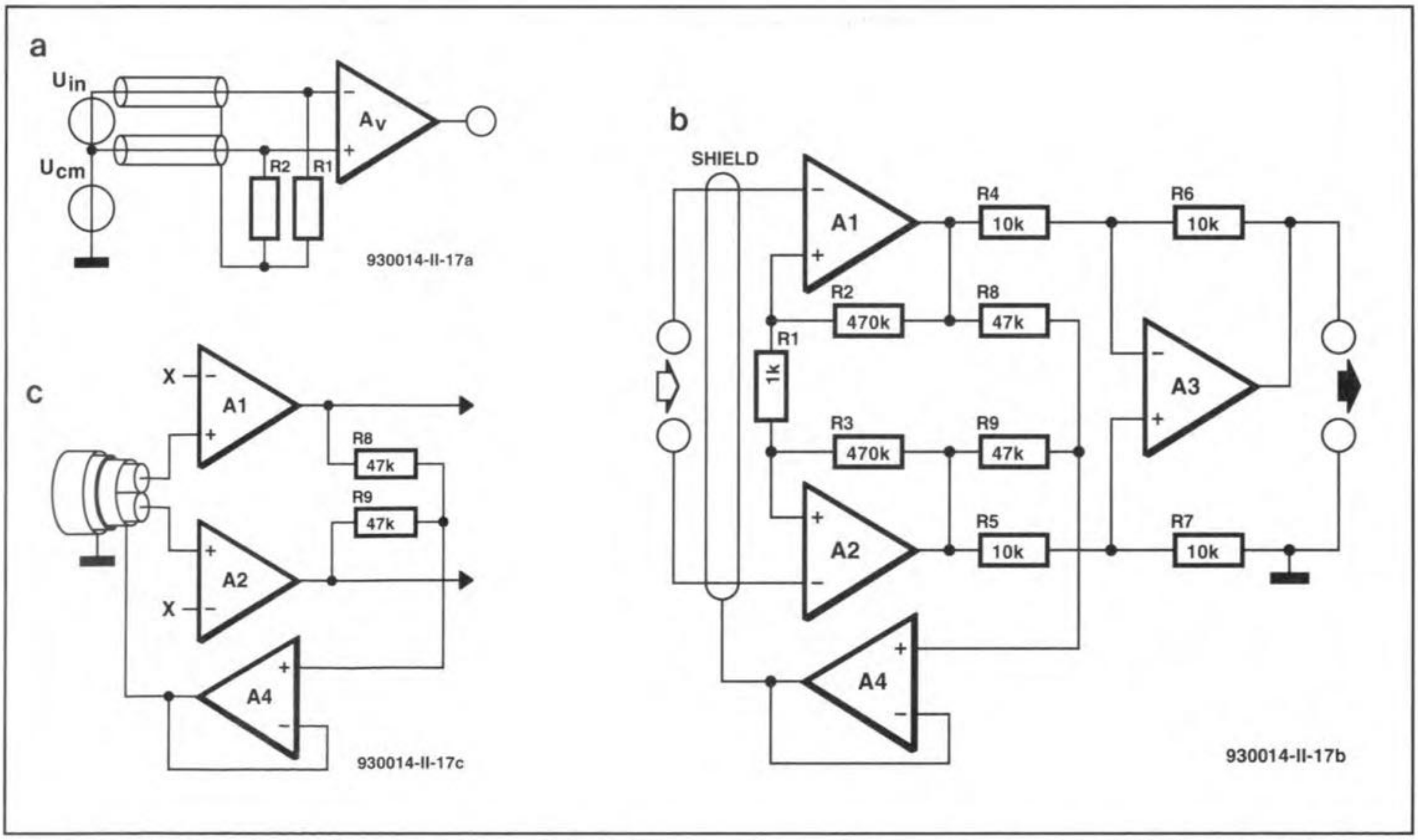


Fig.15. a) Simple guard shield solution to problem of Fig. 14a; b) improved version that uses a guard amplifier (A4); c) double shielded guard shield circuit.

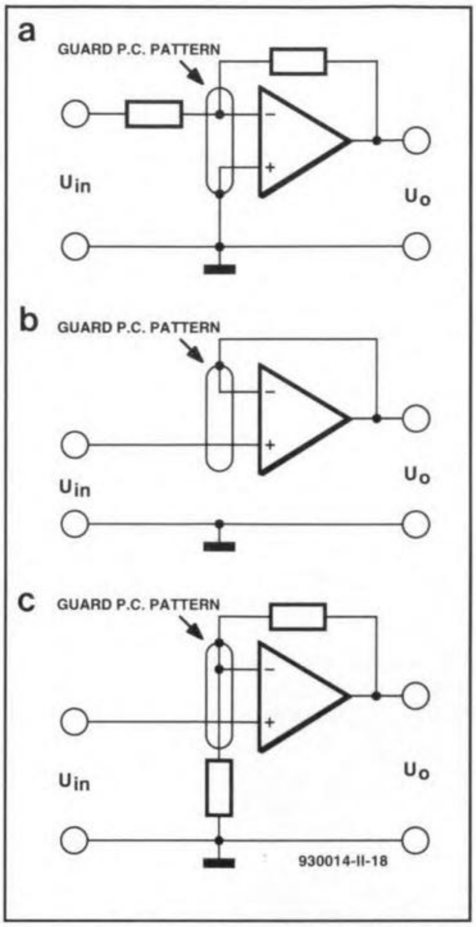


Fig. 16. Use of a printed circuit guard ring feature: a) inverting amplifier version; b) & c) noninverting amplifier versions.

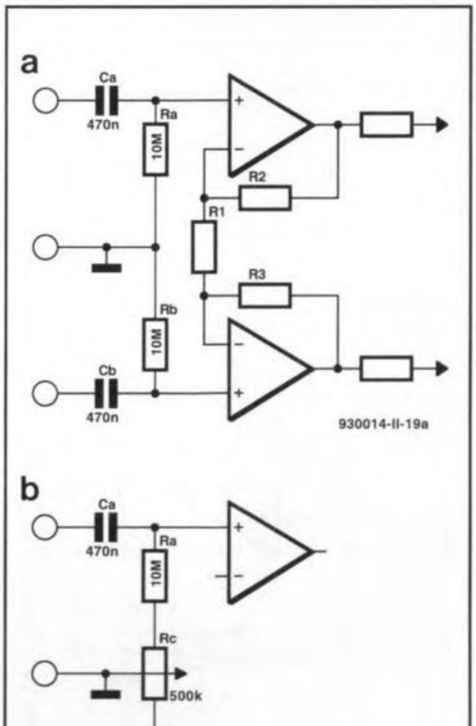


Fig. 17. a) AC coupled instrumentation amplifier input; b) use of a CMRR ADJUST control.

strumentation amplifier requires that R_a=R_b, but that requires high precision resistors. If ordinary five percent tolerance resistors are used, a CMRR adjust potentiometer (resistor R_c in Fig. 17b) may be needed.

Another way to handle the DC offset problem is to use a **d.c. restoration circuit**, such as Fig. 18.[4] This circuit uses a Burr-Brown INA-117 difference amplifier (A1). This device features unity gain, but has a very common mode input range (±200 V), with ±500-V input protection circuitry. A second amplifier (A2) is used to provide a low-pass filter response in the feedback loop, which translates to a high-pass response for the circuit overall. The –3-dB frequency response for this amplifier is given by:

$$F_{-3\mathrm{dB}} = \frac{A_{\mathrm{vref}}}{2\pi R1\,C1} \qquad (2)$$

where:
A_{vref} is the voltage gain seen from the reference pins on the amplifier;
$C1$ is the capacitance of $C1$ in farads;
$R1$ is the resistance of $R1$ in ohms.

For the component values of Fig. 18, the –3 dB frequency is of the order of 6.1 Hz, so only signals having a frequency well removed from d.c. will pass the circuit.

Auto-zero circuit

A very useful circuit for amplifiers that must maintain a very low internal drift is shown in Fig. 19. This circuit uses a method similar to the d.c. restoration method of Fig. 18. Amplifier A1A is the main amplifier, and it has a forward gain of $-R2/R1$, or about 100 for the component values shown. The d.c. restoration circuit (amplifier A1B) is used to bias the non-inverting input of A1A. Switch S1 is used to auto-zero the circuit. Switch S1 is shown in the **zero** position in Fig. 19. The signal input is grounded through S1A, setting the effective U_{in} to zero. At the same time, S1B connects the input of A1B to the output. When U_{in}=0, the output voltage U_o is due to the inherent offset of the amplifier circuit. This voltage is used to charge capacitor $C1$. When S1 is returned to the **operate** position, this voltage is used to counter itself through the non-inverting input. In order to prevent capacitor leakage from degrading the offset cancellation, $C1$ should be a polypropylene type.

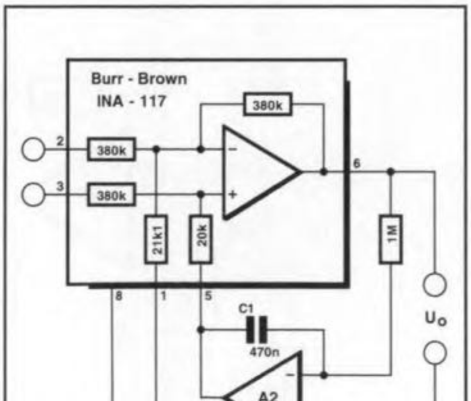


Fig. 18. DC restoration circuit.

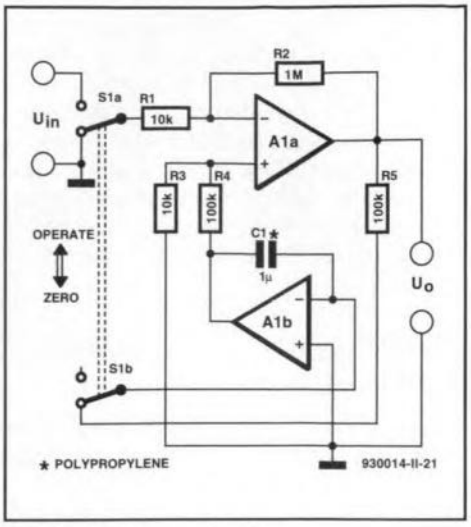


Fig. 19. Auto-zero circuit.

Conclusion

Sensor interfacing can be a dicey process because of these pitfalls on the pathway, but with due regard for signal source output circuit form, amplifier input type, and the other factors in the interfacer's basket of tricks, the job is a lot easier.

In next month's concluding instalment we will be looking at a universal multigain analogue amplifier.

Notes and recommended reading

1. Definitions derived in part from George Klier (Gould, Inc.), 'Signal Conditioners: A Brief Outline', *Sensors: The Journal of Machine Perception*, Jan. 1990, Vol.7, No.1, pp.44-48. Some of the definitions used in this article were originated in the Klier article cited above. For additional information see: Daniel H. Sheingold (ed.), *Transducer Interfacing Handbook*, Analog Devices, Inc., (Norwood, MA 1981).

2. John M. Brown and Joseph J. Carr, *Introduction to biomedical Equipment Technology*. Formerly published by John Wiley & Sons, Inc., but now with Prentice-Hall.

3. Joseph J. Carr, *Integrated Electronics*, Technology Publications — Division of Harcourt, Brace, Jovanovich (1990).

4. 'AC Coupling Instrumentation and Difference Amplifiers'. R. Mark Stitt, Burr-Brown Corporation Applications Bulletin No. 8 (Tucson, AZ, USA, 1990).

MINI MICRO CLOCK

This is the 'little brother' of the Maxi Micro Clock published in the previous issue of *Elektor Electronics*. A true miniature design, the Mini Micro Clock has nevertheless the same functions as the 'maxi' version. This makes it ideal for use in a larger unit, or on a car dashboard.

Design by A. Rietjens

THIS time the circuit is based on the ST6215 microcontroller from ST (SGS/Thomson). The ST6215 is supplied in a 28-pin plastic DIL enclosure, and has sufficient I/O lines to implement the clock function without a single additional logic IC. Despite the fact that the ST6215 is larger than the ST6210 used in the Maxi Micro Clock (Ref. 1), the Mini Micro Clock is a very compact unit, with four LED displays squeezed in between the microcontrollers's two rows of pins.

The circuit

Figure 1 shows the complete circuit diagram of the Mini Micro Clock. To the right you see the four displays, LD_1-LD_4, with their transistor drivers. The drivers are switched by the microcontroller via outputs Digit0-Digit3. A low level at one of these outputs actuates the associated transistor driver, which, in turn, causes the LED display to be supplied. The four digital outputs allow the displays to be multiplexed under software control. The selection of active (lit) segments in the displays is determined by the levels at outputs A-G, which are also found on the microcontroller. Like the display enable lines, the segment selection lines are 'active low'. The same goes for the decimal point, which is controlled by the level on output DP. A clear difference with the Maxi Micro Clock is that a BCD decoder and separate buffers with open-collector outputs are not required.

The ADJ (adjust) input of the processor is connected to a preset potentiometer, P_1, which serves to adjust the clock. Although the adjustment range of this preset is relatively small (approx. 60 s per week), it is, fortunately, ample to ensure good synchronization of the clock. An 8-MHz quartz crystal is used as a reference in the clock, and connected to the oscillator bonded out to pins 3 and 4 of the microcontroller. The two 22-pF capacitors ensure that the crystal resonates at the correct frequency. An additional trimmer is not required, since the clock is adjusted with the aid of P_1.

The three switches used to set and operate the clock are connected directly to I/O lines. Their functions are described further on.

The communication of the clock with the outside world is not limited to the four displays. If desired, a buzzer may be actuated via transistor T_6, or a relay energized via transistor T_5. If you object to the sound of the buzzer, silence it by removing jumper 'A'. Alternatively, replace the jumper by a miniature switch to make the buzzer on/off selection easier.

The last two components around the microcontroller that need to be discussed are resistor R_9 and capacitor C_1 — these parts serve to decouple the microcontroller's power supply.

The power supply, shown at the top of the circuit diagram, has an additional switching transistor that is actuated when the mains supply is switched off, or disappears otherwise. As long as the mains supply is present, diode D_7 is cut off, so that the battery connected to the terminals marked 'Bt1' is not loaded. Also, transistor T_7 is driven into conduction via resistor R_{14}, and the output voltage of IC_2 is connected to the circuit. In case the mains voltage disappears, diode D_6 is cut off, and D_7 conducts. Next, regulator IC_2 reduces the battery voltage to 5 V. Since D_6 is cut off, transistor T_7 does not receive base current, so that the displays remain off. The microcontroller, however, is still powered, and continues to operate in this condition. Switching off the displays causes the current consumption of the clock to drop from 100 mA to about 8 mA, allowing a 9-V battery to keep the clock ticking for several hours in the absence of mains power.

Although a 4.5-V battery would appear the first choice as a backup device, a 9-V (PP3) type is used because of its much smaller size. A 4.5-V battery is about two times as large as the entire clock, and is, therefore, not a good choice when compactness is a prime requirement.

If the clock is used in a car, the switched battery voltage is connected to diode D_6, and the unswitched battery voltage to diode D_7. With the ignition switched off, the clock continues to work with the displays switched off. The displays are switched on again when the car is started.

Construction

Having described the circuit diagram of the mini clock we now turn to the practical construction of the device. Figure 2 shows the compact, double-sided and through-plated, printed circuit board (PCB) designed for the Mini Micro Clock. The PCB and the 9-V battery are fitted into a compact ABS enclosure, which makes the clock smaller than a packet of cigarettes.

The cover of the enclosure is cut and drilled to make the necessary clearances for the LEDs, displays and press-keys. The Conrad enclosure mentioned in the parts list requires a small (35×5 mm) piece of the PCB to be cut out of the PCB, to allow for a moulded support. When the Diptal box is used, the PCB edges are cut off to the extra corner points printed on the overlay. Next, file the PCB until it can be clamped into the box. The connection to the mains supply may be made in one of the side panels.

After this preparatory work, you are ready to start soldering. As indicated by the photograph of the prototype, components are fitted at both sides of

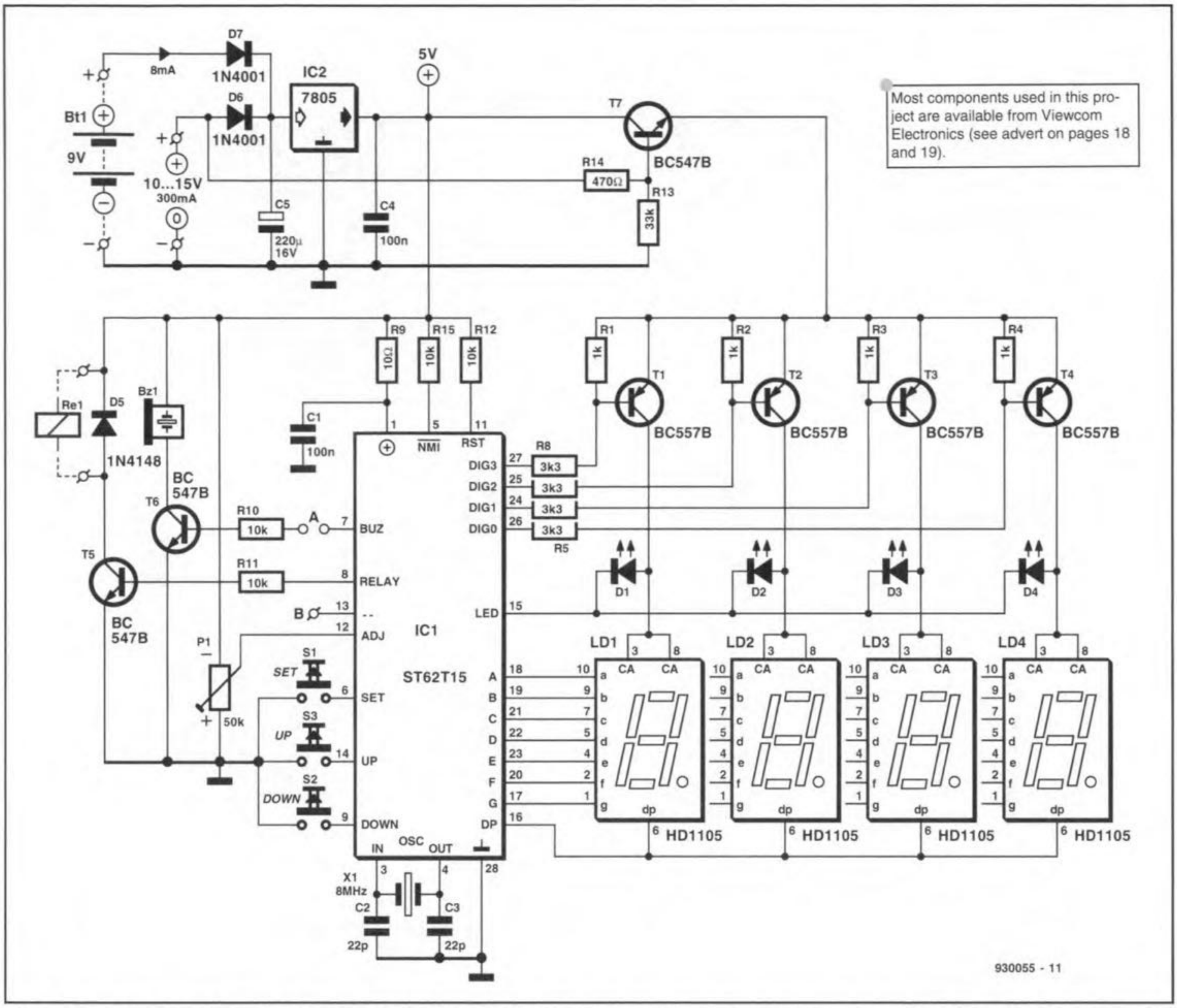


Fig. 1. Circuit diagram of the Mini Micro Clock. The heart of the circuit is formed by a microcontroller Type ST62T15 from SGS/Thomson. The controller is supplied ready-programmed, in three different versions, through our Readers Services.

the PCB. Apart from the microcontroller, all components are fitted directly on to the board. Start by fitting all passive parts. Initially, you may have problems getting the SMT parts fitted, but rest assured that with patience the technique will be mastered after a little while. Next, fit the displays, followed by the IC socket for the microcontroller. It is important to keep to this order because a number of display connections are difficult to reach once the IC socket is on the board. Mount two pins for jumper 'A', so that the jumper is readily fitted, or a miniature switch connected via short wires. Small pins may also be fitted to connect the relay and the supply voltage. Next, mount the diodes, LEDs and transistors (all upright). The length of the LED terminals depends on the arrangement of the other components at this side of the PCB. The top of each LED, the displays and the switches must all be at the same height, as well as level with the cover of the enclosure used. To assist in its cooling, voltage regulator IC2 is best fitted above the board surface using a 5-mm long PCB spacer. Finally, fit the crystal. The circuit is then ready for use.

Three versions

Just as with the Maxi Micro Clock, the Mini Micro Clock may be built for three different applications: clock; darkroom clock/long-period timer; or cooking timer. Each of these applications requires its own microcontroller, which is supplied ready-programmed through our Readers Services. As with the Maxi Micro Clock, the cooking timer requires only two of the four displays (LD1 and LD4 may be omitted). The operation of each of the three versions of the Mini Micro Clock is discussed below.

Clock

This function is realized by fitting a microcontroller with software order code 7111. The SET press-key selects between clock setting and alarm time setting. Depending on the selection, LED D1 or D2 lights. The desired time is set by pressing the UP and DOWN keys. If neither of the two functions is selected (both LEDs off) the UP and DOWN keys enable you to select between an 'hours:minutes' or a 'minutes:seconds' display, both with the alarm enabled or disabled.
One of these four options remains selected until the user selects another setting. Consequently, the clock will not automatically return to the preferred settings.
When the alarm is enabled (jumper 'A' fitted), and the time equals the alarm time, the buzzer will sound. The alarm may be turned off by pressing S1 or S2.

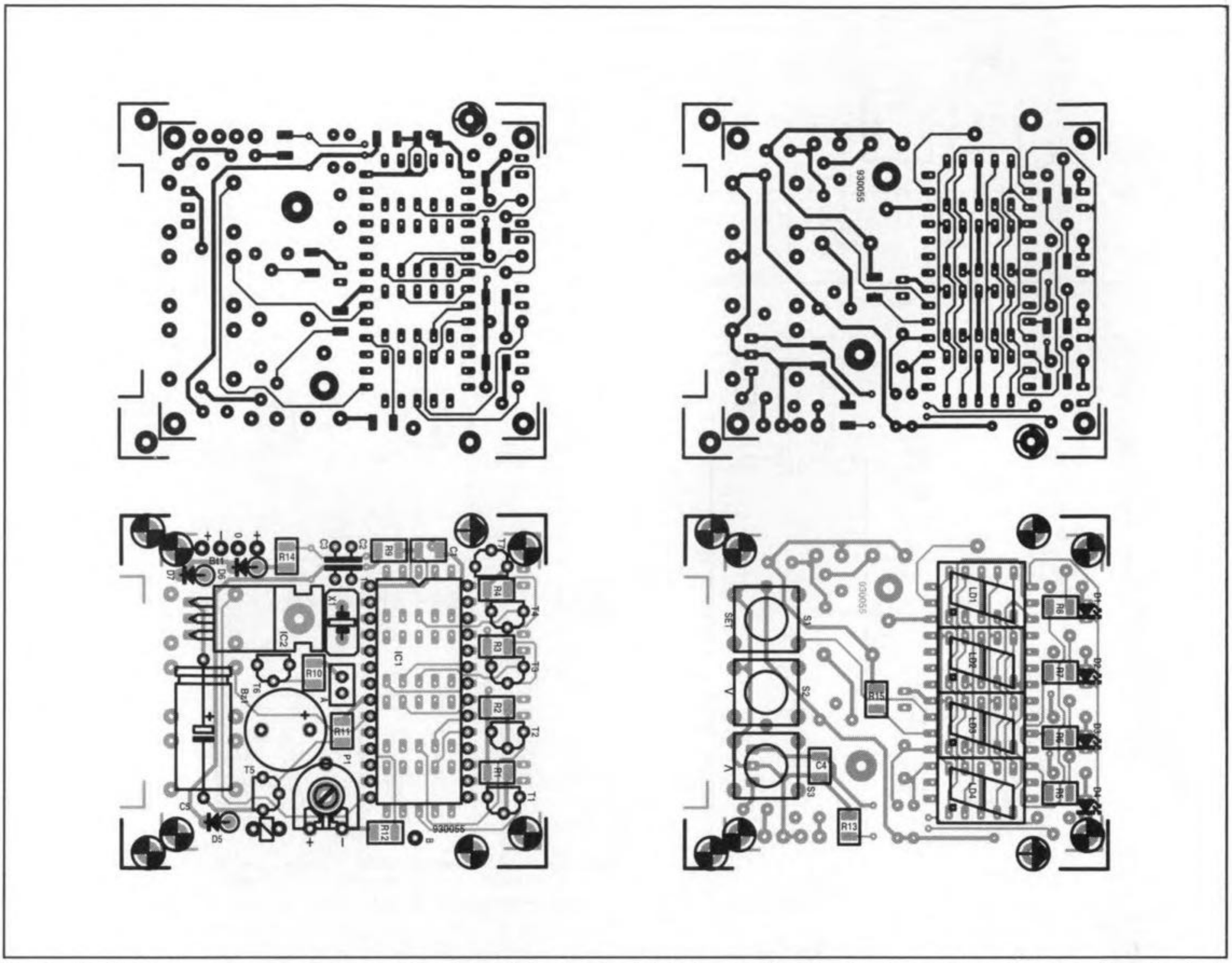


Fig. 2. Track layouts and component mounting plans of the double-sided, through-plated, printed circuit board designed for the clock. ATTENTION: pin 10 of the microcontroller (TEST) should be connected to ground via a short piece of wire.

COMPONENTS LIST

Resistors (all SMT):

4	1kΩ	R1-R4
4	3kΩ3	R5-R8
1	10Ω	R9
4	10kΩ	R10;R11;R12; R15
1	33kΩ	R13
1	470Ω	R14
1	50kΩ preset H	P1

Capacitors:

2	100nF SMT	C1;C4
2	22pF	C2;C3
1	220µF 16V	C5

Semiconductors:

2	LED, red, 3mm	D1;D2
2	LED, green, 3mm	D3;D4
1	1N4148	D5
2	1N4001	D6;D7
4	BC557B	T1-T4
3	BC547B	T5;T6;T7
1	ST62T15[1]	IC1
1	7805	IC2

Miscellaneous:

1	9-V PP3 battery	Bt1
1	5-V buzzer	Bz1
4	HD1105O (Siemens)[2]	LD1-LD4
3	3CTL3 press-key (MEC)[3]	S1-S3
1	8MHz quartz crystal	X1
1	Plastic enclosure dim. 61x22x80mm e.g. Conrad[4] 523950, or Diptal[5] 57x30x86mm	
1	Printed circuit board 930055 (see page 78)	

[1] supplied ready-programmed through the Readers Services (see page 78). Three different versions are available:

7111	mini clock
7121	mini darkroom clock
7131	mini cooking timer

[2] ElectroValue, Unit 3, Central Trading Estate, Staines, Middx TW18 4UX. Telephone: (0784) 442253. Fax: (0784) 460320.

[3] C-I Electronics, P.O. Box 22089, 6360 AB Nuth, Holland. Fax: (+31) 45 241877.

[4] Conrad Electronic Nederland BV, P.O. Box 12, 7500 AA Enschede, Holland. Tel (+31) 53 282000. Fax: (+31) 53 283075.

[5] Diptal, France. Tel. +33 50 569497, fax: +33 50 569517.

We are advised that nearly all components for this project are available from Viewcom Electronics. For address and telephone number, see advert on pages 18 and 19 in this issue.

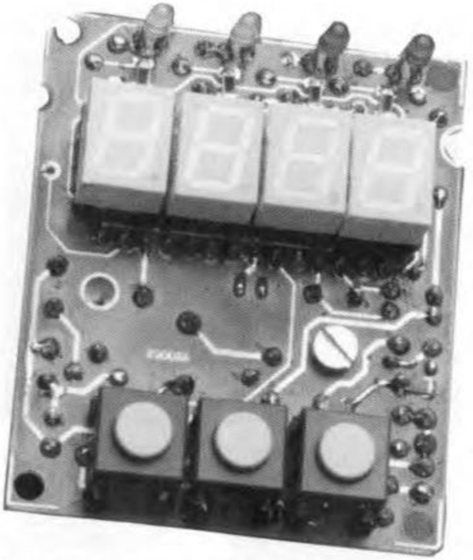


Fig. 3. Prototype, showing the displays, switches and LEDs fitted at the front side of the PCB.

Fig. 4. The rear side of the PCB holds the rest of the parts, which are densely packed.

Transistor T5 is controlled together with the buzzer, and actuates the (optional) 5-V relay.

Darkroom clock

The darkroom clock or long-period timer function (software order code 7121) allows a programmed timing interval to be signalled. Both repetitive and single signalling are possible. In darkroom clock mode, the 'min:sec' display function is not used, and replaced by a 'repetitive alarm' function. The maximum time between two short alarm signals is 99 minutes and 59 seconds (99:59). The darkroom clock function is selected with the DOWN key, which also serves to select between alarm (buzzer) on and off.

The SET key allows the alarm time only to be programmed — there is no point in setting the actual time. The counter is reset when the UP key is pressed after setting the desired alarm time. Depending on your selection, the buzzer will sound once, or repetitively, after a set period has elapsed. The latter function is particularly useful to time the film developer.

The optional relay is actuated via transistor T5 during the first period (after resetting). This allows an electrical apparatus, for instance, an enlarger, to be switched on for a maximum period of 99 minutes and 59 seconds.

Cooking timer

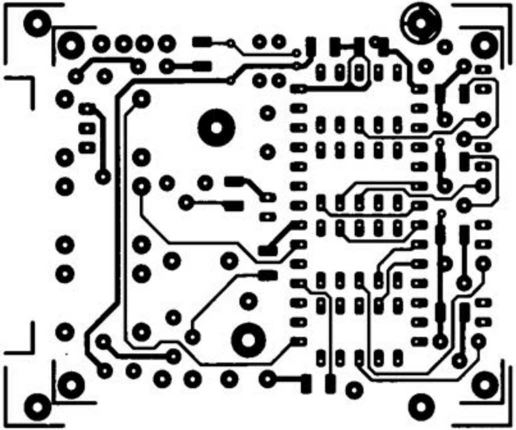
This function requires the microcontroller with order code 7131. The UP and DOWN keys are used to set the desired time, which is counted down to zero. A short beep is produced when the programmed time has elapsed.

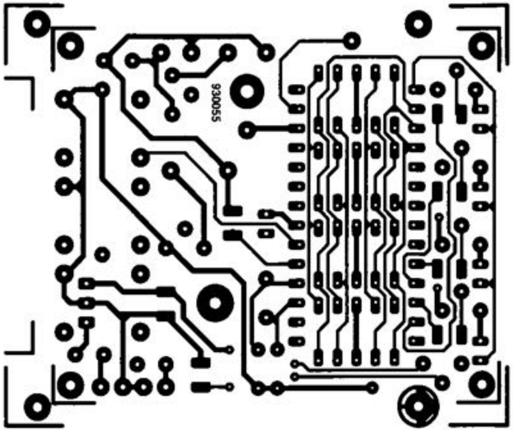
The cooking timer does not use displays LD1 and LD4, so that only the minutes and/or tens of seconds readouts are visible. Before programming the cooking time, the SET key must be used to select between cooking times longer or shorter than 10 minutes. Next, the desired time is set with the UP and DOWN keys. When the cooking time is shorter than 10 minutes, the first display shows the remaining minutes, and the second display the remaining tens of seconds. For instance, if the displays read '8.3', the remaining time is 8 minutes and 30 seconds. With cooking times longer than 10 minutes, the display shows the number of minutes only. The point between the two displays flashes at a rate of 1 Hz. ■

Fig. 6. Suggestion for a front panel layout.

Reference:

Maxi Micro Clock. *Elektor Electronics* July/August 1993.

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DX TELEVISION

A two-monthly column by Keith Hamer and Garry Smith

After a sluggish start, the long-awaited 1993 sporadic-E season finally established itself. The first signs of reception occurred on May 2nd with an opening already in progress at 0600h UTC. A strong and stable signal from the CIS 1st network was present on channel R2 and, at times, the SECAM colour locked.

The most intense and busiest opening occurred on May 12th with strong signals throughout the day from South, South-east and Central Europe. Among the countries identified were Spain, Portugal, Italy, Germany, Hungary, the Czech Republic, Switzerland, Poland, Slovenia, Serbia and Croatia. Three separate openings on the 15th brought in Central European stations, although the exact source of the transmissions could not be determined. A variety of test patterns were resolved by several enthusiasts on May 21st from Norway, Sweden and the CIS.

Tropospheric reception had its moments — in fact it has been prevalent this year. April 27th was extremely productive with various Benelux, Scandinavian and German catches, some of which fell into the 'exotic' category.

Reception reports

Peter Chalkley of Luton has notched up several countries already this season using a D-100 DX-TV converter fed into an elderly Philips TV-ette portable. During an opening to Scandinavia and the East on May 14th, Peter discovered 6-metre amateur radio activity from Estonia.

The same opening produced test cards from Norway, Sweden and Finland for Andrew Jackson at his QTH in Birkenhead. Of particular interest was a modified Norwegian PM5534 test card with the initials 'NRK' at the top with the date and time across the centre. There was no identification in the lower black rectangle.

Bob Brooks of South Wirral and Stephen Michie of Bristol have also noticed the modified NRK test pattern with the date display on two occasions, but in between these sightings the normal version with transmitter identification has been seen. Both Bob and Stephen were fortunate enough to identify Iceland on May 14th. The PM5544 test card carried the identification 'RUV' at the top, and 'ISLAND' in the lower black rectangle.

Neil Purling of Hull has noted a slow start to the sporadic-E season. Even so, he has successfully managed to identify Portuguese, Spanish and Italian signals in Band I.

Simon Hamer of New Radnor in Powys did well with tropospheric reception at the end of April when signals from the new Norwegian TV-2 network were discovered on channel E12. During the same opening programmes from the Swedish TV-4 service were seen.

Stephen Michie has reported strong colour reception from the Dutch Lopik transmitter using a wideband UHF grid indoors. A second (stacked) grid is being added to the system to reduce the capture angle in the hope of reducing problems from local UHF relays.

The sporadic-E season (November to March in the Southern hemisphere) produced some spectacular long-haul high MUF signals 'down-under' according to Anthony Mann of Perth in Western Australia. Double-skip FM reception from Victoria was identified on December 24th of last year, and again on January 24th. TV signals from the North on channels E2 and R1 were also noted. These were thought to have originated in Thailand and China, respectively.

The highlight of the Australian season was the reception of several channel A2 vision carriers from Hawaii and Mexico on January 16th from 0530-0600h UTC, possibly via a combination of F2-layer and sporadic-E propagation.

Meanwhile, Todd Emslie of Sydney is still trying to trace a mystery Pacific FM station on 93.25 MHz during an intense Sporadic-E opening to New Caledonia on February 6th. The early afternoon reception lasted for around 30 minutes during which the US Top 40 and adverts were heard but there were no clues as to their origin.

Log for April

13.04.93: Unidentified meteor-scatter 'pings' on channels E3 and R2 at 1315h UTC.

15.04.93: Tropospheric reception from Sweden and Denmark in Band III and at UHF.

27.04.93: Excellent tropospheric reception from France, Eire, Belgium, the Netherlands, Luxembourg, Norway, Sweden and Denmark. In addition, at least nine German services were identified on various Band III and UHF channels.

28.04.93: Similar reception to the 27th.

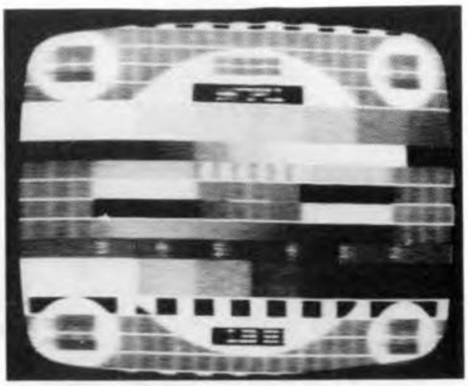

Fig. 1. A typical UEIT test card as used by most ex-USSR stations for all networks. There are many subtle identification variations, some with letters and others with numbers, thus making positive identification difficult.

Log for May

02.05.93: Sporadic-E signals from an unidentified CIS transmitter on channel R2 at 0600 UTC in SECAM colour.

05.05.93: A late afternoon sporadic-E opening with Italian signals on channels IA and IB.

12.05.93: Intense and active sporadic-E reception throughout the day from Southern and Central European on various Band I channels. At least eleven countries were identified.

13.05.93: Sporadic-E signals from Finland, Norway, Sweden, Iceland and Estonia.

15.05.93: Sporadic-E openings at early morning, midday and late afternoon with various unidentified signals from Eastern Europe on channels R1 and R2. At 1645h UTC, a clock two hours ahead of UTC was noted.

21.05.93: Sporadic-E signals between 1100h and 1300h UTC from Norway (Steigen on channel E2 and Hemnes E3), followed by signals from Sweden, including the PM5534 test card. At 1225h UTC a UEIT test pattern from an unidentified CIS transmitter appeared.

24.05.93: Sporadic-E reception from Scandinavia in Band I and good-quality tropospheric signals from the Netherlands at UHF.

25.05.93: Denmark (DR) on channel E7, and TV-2 on E27 from Abenraa with the PM5534 test card, tone and music at 0630h UTC. Towards midnight, several Benelux stations were noted, plus a German ZDF station on channel E24.

26.05.93: Strong tropospheric reception from the NED-3 Lopik outlet on channel E30.

27.05.93: Sporadic-E reception from Spain, Portugal, Hungary, Austria, Sweden, Denmark and the Czech Republic.

29.05.93: Early evening sporadic-E reception from Spain, Portugal and Corsica.

The DX-TV logs were kindly supplied by Andrew Jackson, Stephen Michie, Simon

Hamer, Garry Smith, Bob Brooks and Peter Chalkley.

DX-TV information

There have been several requests from *Elektor Electronics* readers for publications covering the DX-TV hobby. There are in fact various books available written by DX-TV enthusiasts. There is also a range of videos covering test cards, propagation, equipment, etc.

'DX-TV For Beginners' by Simon Hamer (£4.80, UK) covers the basics of TV DX-ing with practical ideas for getting into the hobby with the minimum outlay. 'A TV-DXers Handbook' by Roger Bunney (new edition to be published soon), covers the subject in greater technical depth, while 'Guide to DX-TV' (£4.80, UK) by Keith Hamer and Garry Smith provides ideas for improving an existing set, with the emphasis on choosing the correct type of aerial and pre-amplifier, and ways of preventing or curing common forms of interference. A free copy of the latest HS Publications catalogue covering DX-TV books, videos and equipment is available by sending a large stamped and addressed envelope (or two IRCs) to: HS Publications, 7 Epping Close, Derby DE3 4HR. (Telephone: 0332 381699).

Channel allocations

Some explanation may be necessary concerning the channel numbering system used by TV stations overseas. In general, countries in Western Europe use an 'E' prefix, while those in the East use an 'R' prefix, but the channels do not coincide. There are three 'E' channels allocated in Band I, and these are used by countries such as Norway and Spain. The channels are referred to as E2, E3 and E4. Channels E5 to E12 are located in Band III.

There are only two 'R' channels allocated to Band I: R1 and R2. Countries such as Poland or Hungary use 'R' channels. Channels R3, R4 and R5 are located within a special band (TV Band II) just below the FM radio band. Channels R6 to R12 are to be found in Band III.

There are exceptions. Italy uses letters instead of numbers to identify channels; also an 'I' prefix is used. These are IA and IB in Band I, IC just below the FM band, and ID to IH in Band III. France is another exception: an 'L' prefix is used. In Band I the channels are L2, L3 and L4, although the frequencies used do not coincide with those of other countries. In Band III, the French channels range from L5 to L10.

UHF allocations are little more civilized, and UK channel 30, for example, has the same vision frequency as E30 in Sweden, L30 in France or R30 in Poland.

Recognizing the various channel numbers and their relative positions on each band comes with experience, and often the reception can be identified by these factors. It is best to imagine a band as being a horizontal tuning scale on a radio. TV sets with VHF tuners fitted usually have a scale inscribed only with 'E' channels 2-4 in Band I, and 5-12 in Band III. Specialized converters such as the D-100 also have the Italian and 'R' channels marked around the Band I dial.

Band I channels, in ascending order, are: E2 (Western Europe), R1/E2a (Eastern Europe and Austria), IA (Italy), E3, L2 (France), R2, L3, E4/IB and L4.

European DAB plan

Further information has come to hand regarding the proposed Digital Audio Broadcasting plan for Europe. In Europe, the proposed allocations will mean the loss of Band III channel E12; existing transmissions will be move to UHF.

It seems likely that the United Kingdom will have approximately 12.5 MHz of spectrum centred around 230 MHz, producing seven blocks of 1.5 MHz bandwidth. Each block will support up to twelve national radio channels. One block will be reserved for the BBC with a second for independent radio. The remaining five blocks will be used for around the UK, and each area should have enough space for six local stations, with as many as twelve in large cities.

Service information

France: Experiments using the Ceefax teletext system are continuing, and the existing Antiope system will be phased out next year. Teletext subtitles on Ceefax page 888 are already available via the France-3 network. TF1, France-2 and France-3 are the only networks with a Teletext service.

Belgium: The French-speaking RTBF network has abandoned their own Teletext system, known as Percival, in favour of the Ceefax system. Other important changes to the network include the conversion of the existing service into French-based ones, such as Canal Plus and ARTE. The Tele21 service from Tornai (channel E63, 20 kW, vertical) and Wavre (channel 28, 500 kW) is now called 'Sport21', while the Anderluès transmitter on channel 61 (200 kW horizontal) broadcasts ARTE21, which is identical to ARTE in France. The ARTE21 transmissions have 'normal' sound, but the picture is encrypted.

The PM5544 test pattern for the Flemish-speaking network has changed its top identification from 'BRT' to 'BRTN'. The lower identification remains as before, namely TV1 or TV2.

Switzerland: A fourth network called 'S Plus' will be launched at the end of August. Competing with German stations such as RTL, SAT-1, PRO-7, etc.,

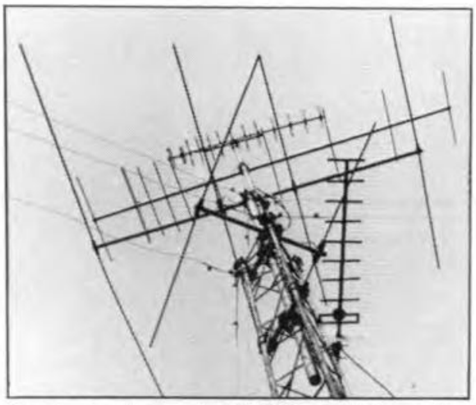

Fig. 2. An elaborate DX-TV installation using separate yagi arrays for each band. For sporadic-E reception, a simple loft-mounted dipole can be used if aerials cannot be fitted outdoors.

the network will broadcast initially throughout the North of Switzerland, covering 70% of the population via cable distribution and terrestrial transmitters operating around channel E36. RTL in the meantime have opened an office in Zürich in an attempt to attract local advertising. Special news and programme feeds for Switzerland have also been proposed.

Estonia: the first PAL transmitters are planned for 1994/1995.

Russia: At station opening, the RTV (Russian TV) network now identifies itself as 'Telekanal Rossija'. Most of the programmes aired via the TKR channel are produced by independent TV production companies, and the trend is for them to display their own identification in the corner of the picture during the programme. Thus, there are dozens of different logos to be seen via the TKR channel, so caution is needed when trying to identify this channel.

Germany: in the North of the country, regional magazine programmes shown between 1830-1900h UTC have been transferred from the ARD-1 service to the N3 network.

In the Berlin area, ORB-1 and SFB-1 have merged, producing a common programme on channel E7. This means that channel E5, which was used by SFB-1, is no longer in use. N-TV (the news channel) has been assigned channel E51 (5 kW ERP), while channel E44 has been allocated to VOX-TV.

Due to interference problems, the SSVC (British Forces) transmitter at Mülheim has moved from channel E41 to E54.

This month's service information was kindly supplied by Gösta van der Linden and the Benelux DX Club; Bernd Trutenau, Lithuania; Pertti Salonen, Finland; Reflexion Club, Germany; Roger Bunney, UK; Jürgen Klassen, Germany; Simon Hamer, UK; André Gille, France. Please send any news about DX-TV in your part of the world to: Keith Hamer, 7 Epping Close, Derby DE3 4HR, England.