ELEKTOR ELECTRONICS

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BUMPER CHRISTMAS ISSUE

With over 50 construction projects

1.2 GHz frequency meter

Solid-state transverter interface

A model analysis

Digital blackjack

NiCd charger

Seven-eleven

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ELEKTOR ELECTRONICS

December 1992
Volume 18
Number 206

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In next month's issue
(among others):

- We start a new series on understanding electronics: 'Figuring it out'
- PAL test signal generator
- Multi-core cable tester
- Dual video amplifier/ splitter
- Convolutional and block codes for multiple error detection
- Digital audio-visual system Part 3
- 1.2 GHz multifunction frequency meter – Part 2

Front cover

This month we start a three-part article on an advanced frequency meter/pulse generator. The instrument offers microprocessor control, pulse and period measurement, battery option, pulse generator, LCD read-out and menu-driven operation. The compact, portable instrument is a worthy successor to the very successful frequency meter we published in 1985, thousands of which are in use all over the world.

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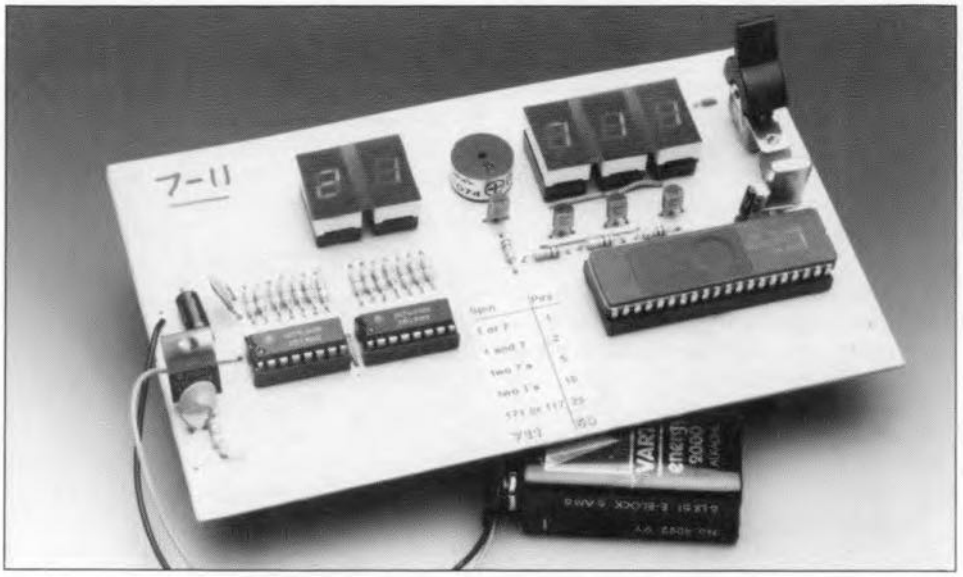
We thank all our readers wherever they are for their continued support and extend to all of you our best wishes for PEACE, HOPE, BROTHERHOOD, LOVE AND FAITH in the New Year

SEVEN-ELEVEN



Seven-Eleven is an electronic slot machine. The object of the game is to 'break the bank' by accumulating 99+ points. The player starts with 20 points and wins points based on the outcome of the spin of the 'wheel', attempting to spin 7's and 1's.

By Larry L. Cameron

SEVEN-ELEVEN is a simple electronic game project based on the 8748/8749 ('874x') series of microcontrollers manufactured by Intel. Features of the project include simple construction, entertaining play, and educational instruction for those interested in seeing the use of the 874x instruction set in an application. This article will detail theory of operation and use of the 7-11 'one-armed bandit'.

Returning to the actual game, each spin on the 7-11 machine costs 1 point and the player is subsequently awarded points based on the following table:

Spin	Payoff	Prob.	Note
single 1 or 7	1	37.3%	
7 and 1	2	3.9%	
two 7's	5	3.1%	(two 7's and one 1 = 5 pts)
two 1's	10	1.6%	
171 or 117	25	0.8%	
711 in order	50	0.4%	**jackpot!**

For example, a spin of 631 would pay off one point, and a spin of 113 would pay off 10 points. The 'probability' column indicates the percentage chance that a particular spin combination will be seen. The probability of getting any winning spin is 47.1%, so just as with a real slot machine the odds are against you! The game ends when your score is zero (after a spin without a pay off).

Theory of operation

The power of the microcontroller lies in its ability to easily coordinate hardware to software with a minimum of support components. In this project, an 8748 controls the operation of the entire game, such as debouncing the switch signal, keeping track of the player's score, and controlling the spinning wheel displays with a minimum of support circuitry. Two 74LS48's

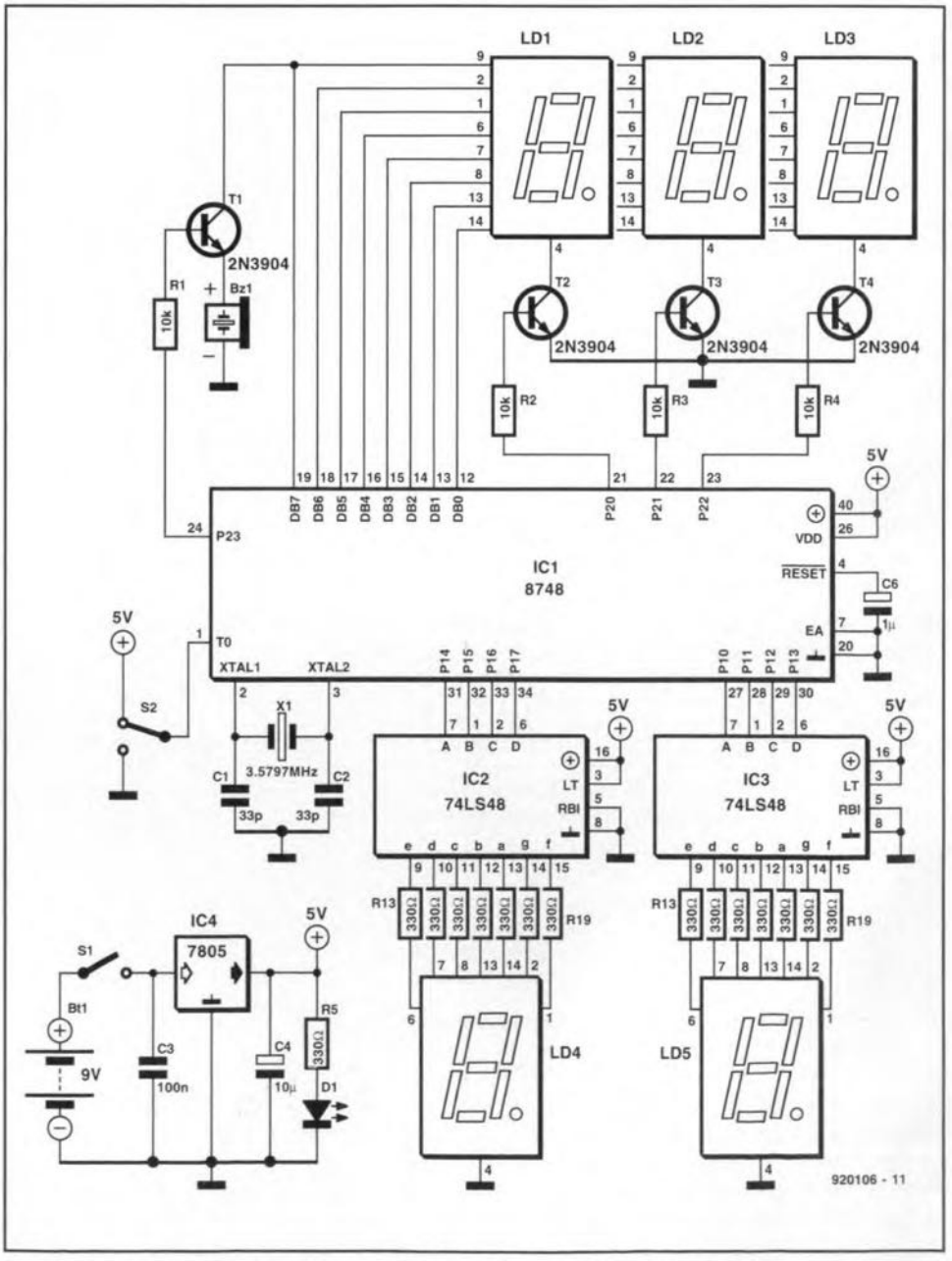


Fig. 1. Seven-eleven is an electronic game based on an 8748 microcontroller.

are required to display the score, but all other aspects of the game are controlled exclusively by the 8748. The following discussion assumes familiarity with the pinout and operation of the 874x microcontrollers; please consult an Intel databook for more information if you need to.

When power is first applied, the game scrolls the numbers '711' on to the wheel display, initialize variables, and then enters a waiting period, decreasing a register value and waiting for a high signal on processor line T0. The register is used to seed a random number. When a high is seen on T0 from the switch, S2, the software waits for a few milliseconds and then checks again to makes sure the signal is still high. This serves to debounce the high signal. If the signal is still high, the software decrements the player's score (two BCD numbers), and latches these numbers on its P1.0-P1.7 outputs which are decoded by the 74LS48's, and displayed. The number wheels are then set in motion until all displays have stopped spinning. Next, the software checks to see if the spin has a payoff, and if not enters the waiting period again to seed a new random number, and repeats the above.

If the player's score is zero, no more spins are possible, and the software goes into a continual loop, horizontally scrolling the numbers '711' on and off the wheel displays. The game is lost at this point. If the spin has a pay off, the winning digits blink three times, and the player's score is increased by the appropriate amount as per the pay off table.

If the player's score reaches over 99-points, the software also goes into a continual loop with the scrolling '711' display, and the game is won. If the score is not over 99, the software repeats the above by waiting for a random seed, etc.

The three wheel displays are multiplexed to the microcontroller. To minimize hardware, the controller's BUS latch outputs are used, along with the P2.0-P2.3 outputs to switch the appropriate display off and on via three n-p-n transistors operating in a saturated mode. For example, to display '711', the appropriate bus lines that correlate to lighting a 'seven' are driven high, P2.0 is driven high to forward bias the transistor, and the segments for the first wheel display are lit (the common cathode of the display is grounded). Line P2.0 goes low to turn off the transistor, and the display extinguishes. The bus lines change state to reflect the next number, 'one', and P2.1 goes high. The second display lights up to display 'one'. The transistor is turned off, and the same process repeats for the third displayed number. By repeating this process at a fast rate, the illusion of a constant ('static') display is achieved. Multiplexing the displays in this way also eliminates the need for any current limiting resistors. For sound, a buzzer is connected to the dot point display, and controlled via P2.3 and another transistor,

7-11 V1.1 HEX LISTING

ADDR	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
0000	15	54	50	14	C5	B8	26	23	00	A0	C8	A0	C8	A0	B8	33
0010	23	21	A0	39	B8	33	F0	96	25	BA	14	BB	FF	14	D1	EB
0020	1D	EA	1D	24	D0	14	D1	36	14	BB	7F	CB	14	D1	26	2B
0030	BD	10	14	7B	26	2B	23	00	3A	B8	33	F0	07	A0	53	0F
0040	37	03	0F	37	96	4C	F0	53	F0	43	09	A0	F0	39	CB	54
0050	95	34	00	BA	03	14	D1	EA	55	36	4E	BD	10	14	7B	36
0060	4E	14	82	54	95	34	00	BA	05	14	D1	EA	69	B8	26	BC
0070	03	F0	96	65	C8	EC	71	34	72	04	14	BE	FF	EE	7D	ED
0080	7B	83	FB	B8	20	A0	C6	BA	BC	03	F0	E7	E7	A0	53	1F
0090	AB	96	95	BB	01	BE	0B	BA	37	FA	E3	53	80	C6	A7	EE
00A0	A3	BE	0A	EB	A7	04	AB	EA	99	04	97	FC	03	20	A9	FE
00B0	A1	FC	03	26	A9	FA	A1	EC	8A	83	B8	23	23	03	A0	C8
00C0	23	09	A0	C8	A0	B8	29	23	10	A0	C8	23	30	A0	C8	A0
00D0	83	B8	29	B9	26	BC	03	BD	01	BF	FF	F1	96	E0	BF	7F
00E0	F0	E3	5F	02	FD	3A	8A	08	E7	AD	C8	C9	23	00	3A	EC
00F0	D9	83	00	00	00	00	00	00	00	00	00	00	00	00	00	00
0100	BC	03	FC	03	23	A8	F0	F2	0E	D2	4E	EC	02	83	FC	03
0110	2C	A8	F0	07	A0	C6	19	24	0B	FC	03	26	A8	F0	07	96
0120	23	23	37	A0	E3	53	80	C6	3F	FC	03	29	A8	F0	07	A0
0130	37	03	50	37	96	3F	FC	03	23	A8	23	00	A0	24	0B	FC
0140	03	29	A8	F0	E3	2F	FC	03	2C	A8	2F	A0	24	0B	FC	03
0150	26	A8	F0	07	96	58	23	37	A0	E3	53	80	C6	70	FC	03
0160	2F	A8	F0	07	96	6F	FC	03	23	A8	23	80	A0	24	70	A0
0170	24	0B	BA	FF	B9	23	BC	03	FA	E3	C6	83	2F	F1	37	6F
0180	37	96	89	C9	CA	EC	78	24	95	CA	EC	89	CA	FA	37	03
0190	AB	37	96	74	83	B8	35	23	05	A0	BE	FF	14	D1	EE	9C
01A0	B8	35	F0	07	A0	96	9C	54	BE	FA	E3	AC	03	96	37	AF
01B0	B8	33	23	80	02	F0	03	01	57	A0	C6	CE	39	23	08	3A
01C0	FF	AD	14	7B	23	00	3A	BE	7F	EE	C9	EC	B5	83	04	19
01D0	54	50	54	63	24	D0	BD	05	BE	FF	C5	14	D1	D5	EE	DA
01E0	ED	DA	83	00	00	00	00	00	00	00	00	00	00	00	00	00
01F0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
0200	00	06	06	07	02	06	07	00	06	07	10	02	07	04	02	07
0210	00	02	07	20	00	07	02	00	07	00	00	07	00	10	03	00
0220	04	03	10	00	03	04	00	03	00	00	03	00	20	01	00	02
0230	01	20	00	01	02	00	01	00	00	01	00	01	00	01	00	00
0240	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
0250	B8	42	B9	29	BC	03	F8	A3	A1	C8	C9	EC	56	54	7A	F8
0260	96	52	83	B8	01	B9	27	BC	03	F8	A3	A1	19	18	EC	69
0270	54	7A	F8	37	03	43	37	96	65	83	BD	03	BE	FF	BA	03
0280	B9	29	BF	01	23	00	02	FF	3A	E7	AF	F1	02	C9	EA	84
0290	EE	7E	ED	7C	83	B8	26	23	40	A0	C8	A0	C8	A0	B8	2C
02A0	23	8C	A0	C8	A0	C8	A0	B8	2F	23	01	A0	C8	A0	C8	A0
02B0	B8	32	23	0A	A0	C8	23	78	A0	C8	23	F0	A0	83	D5	BC
02C0	03	BB	03	B8	29	B9	37	F0	A1	37	03	10	37	C6	EE	F0
02D0	37	03	30	37	C6	EE	C8	C9	EB	C7	34	D6	BB	03	B8	29
02E0	B9	37	F1	A0	C8	C9	EB	E2	34	D6	EC	C1	C5	83	23	01
02F0	A0	44	D6	00	00	00	00	00	00	00	00	00	00	00	00	00
0300	00	00	08	5C	EF	43	01	00	08	5C	FF	63	01	00	08	44
0310	87	02	00	08	58	FD	63	01	00	08	58	ED	43	01	00	1C
0320	E6	03	00	08	4C	CF	43	01	00	08	4C	DB	61	01	00	04
0330	86	02	00	08	54	BF	62	01	00	00	00	00	00	00	00	00
0340	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
0350	00	FF	FF	80	40	40	40	20	20	20	20	10	10	10	10	10
0360	08	08	08	08	08	08	04	04	04	04	04	04	04	04	04	04
0370	02	02	02	02	02	02	02	02	02	02	02	01	01	01	01	01
0380	01	01	01	01	01	01	01	01	01	01	01	01	01	00	00	00
0390	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
03A0	00	00	00	00	00	00	00	00	00	00	00	00	01	03	00	00
03B0	01	00	03	00	01	00	00	03	01	09	00	00	01	00	09	00
03C0	01	00	00	09	02	09	03	00	02	03	09	00	02	03	00	09
03D0	02	00	03	09	02	09	00	03	02	00	09	03	05	03	00	03
03E0	05	03	03	00	05	00	03	03	0A	09	00	09	0A	09	09	00
03F0	0A	00	09	09	19	03	09	09	19	09	03	09	32	09	09	03

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Fig. 2. Microcontroller program in the form of a hexdump.

being continually forward biased while the wheel spins, and turned off for the rest of the game's functions.

Construction hints

The introductory photograph shows the author's prototype of the game. For those unwilling to program their own 8748 with the aid of the hexdump given in Fig. 2, the author can supply ready-programmed controllers at $12.00 each. Also available at $4.00 is a disk formatted in IBM 360 KByte format containing both a binary file and an Intel hex file of the object code, ready to be loaded into most IBM PC controlled programmers. If you would like to purchase any of these items from the author, please make your cheque payable to Larry Cameron, and mail to my address. Call (512)-467-7983 before 5 p.m. central standard time, for more information.

For a professional looking project, it is best to produce a printed circuit board, which you may want to design yourself. Advanced constructors may also consider building the project on veroboard or stripboard, as the component layout is not particularly critical. Alternatively, contact the author for a suggested PCB layout (not given here). Unfortunately I can not provide for sale a pre-etched, pre-drilled board, but a simple method I use frequently to make boards is the 'TEK-200' film method (also goes by other names), which involves photocopying the PCB layout to be etched on to a special sheet of mylar film, ironing the subsequent film on to a copper-clad board, and etching.

Most of the parts for 7-11 can be bought at Radio Shack (Tandy), or at any other well-stocked electronic parts store. If you can not find an SPDT momentary switch, you may substitute an SPDT toggle switch if necessary. You may have to hunt around for switches that fit in the PCB layout holes, or simply modify the board by drilling holes and adding jumpers to fit your switch.

I recommend the use of sockets for the ICs, and 7-segment displays. I used five Radio Shack 7-segment common cathode displays, but any other display could be substituted as long as it conforms to the same pinout as the Radio Shack ones (see circuit diagram). A piece of red cellophane taped over the displays provides for good contrast, and allows you to see the lit segments very well in daylight.

You may substitute 7448's or 74C48's, but I found the 74LS48's to be the cheapest variety. If constructing the project on to a printed circuit board produced from the author's layout, please note that the 74LS48's are oppositely aligned versus the controller, i.e., pin 1 of the 74LS48's is in the lower left corner of the socket, but pin 1 of the controller is on the upper right side. This was done to facilitate design of a single-sided PCB with a minimum number of jumpers on the component side. Be careful to correctly orient pin 1's, e-b-c transistor orientation, anodes, cathodes of polarized parts, etc., as you fit components.

The author's game is powered by a 9-V d.c. wall adaptor transformer, but it can be powered from a 9-V PP3 battery. The circuit draws rather a lot of current (approx. 130 mA), so for long periods of operation an adaptor is really the only option. ■

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COMPONENTS LIST

Resistors:
All resistors are ¼ watt, 5%

4	10kΩ	R1-R4
15	330Ω	R5-R19

Capacitors:

2	33pF ceramic	C1;C2
3	100nF ceramic disc	C3;C4;C5
1	1µF 16V electrolytic	C6
1	10µF 16V electrolytic	C7

Semiconductors:

1	8748H, preprogrammed (see text)	IC1
2	74LS48	IC2;IC3
1	7805	IC4
4	2N3904	T1-T4
1	LED	
5	0.3" 7-segment common cathode LED display, Radio Shack #276-075B	LD1-LD5

Miscellaneous:

1	SPDT switch, on-on	S1
1	SPDT switch, on-none-(on) momentary	S2
7	Wire link 22AWG	J1-J7
1	3.579MHz crystal	XTAL
1	5-V buzzer, Radio Shack #273-074	Bz
1	40-pin IC socket (optional)	
5	14-pin IC socket (optional)	
2	16-pin IC sockets (optional)	
1	9-V battery with clip (optional)	
1	9-VDC mains adaptor	
1	Printed circuit board (see text)	
1	Enclosure	

NEW PRODUCTS

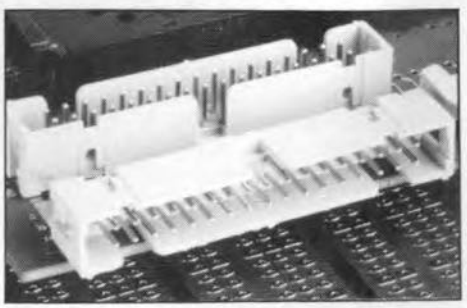
NEW RANGE OF PROGRAMMER/EMULATORS

Ice Technology have announced the launch of a new range of universal programmers with built-in emulation capabilities, offering superb capabilities for the design engineer at a very affordable price. While other programmer/emulators can only support EPROMs, the Speedmaster 1000E and Micromaster 1000E can program EEPROMs, serial EPROMs, NVRAMs, Flash, PALs, GALs, EPLDs, PEELs, Machs, MAPLs, etc., and can emulate ROM and RAM up to 128 kBytes (equivalent to 1 Meg EPROM). The programmers are housed in an attractively styled high-density polyurethane enclosure, and come complete with software, manual, printer port cable, power supply adaptor and emulator cable. The printer cable plugs straight into the standard parallel port of any IBM compatible PC without the need for any expansion card. More details can be obtained from

ICE Technology Ltd., Unit 4, Penistone Court, Station Buildings, Penistone, S. Yorkshire S30 6HG. Telephone (0226) 767404. Fax (0226) 370434.

SHORT HEADERS— HIGH PIN COUNT

New from 3M Electronic products is the 2500 series of shrouded, low-profile, box headers for board-to-board and wire-to-board applications. The 2500 series is available in 11 pin counts (10-60 ways), offering design engineers one of the widest choices of pin count options.The headers are based on a 0.1 in. × 0.1 in matrix.

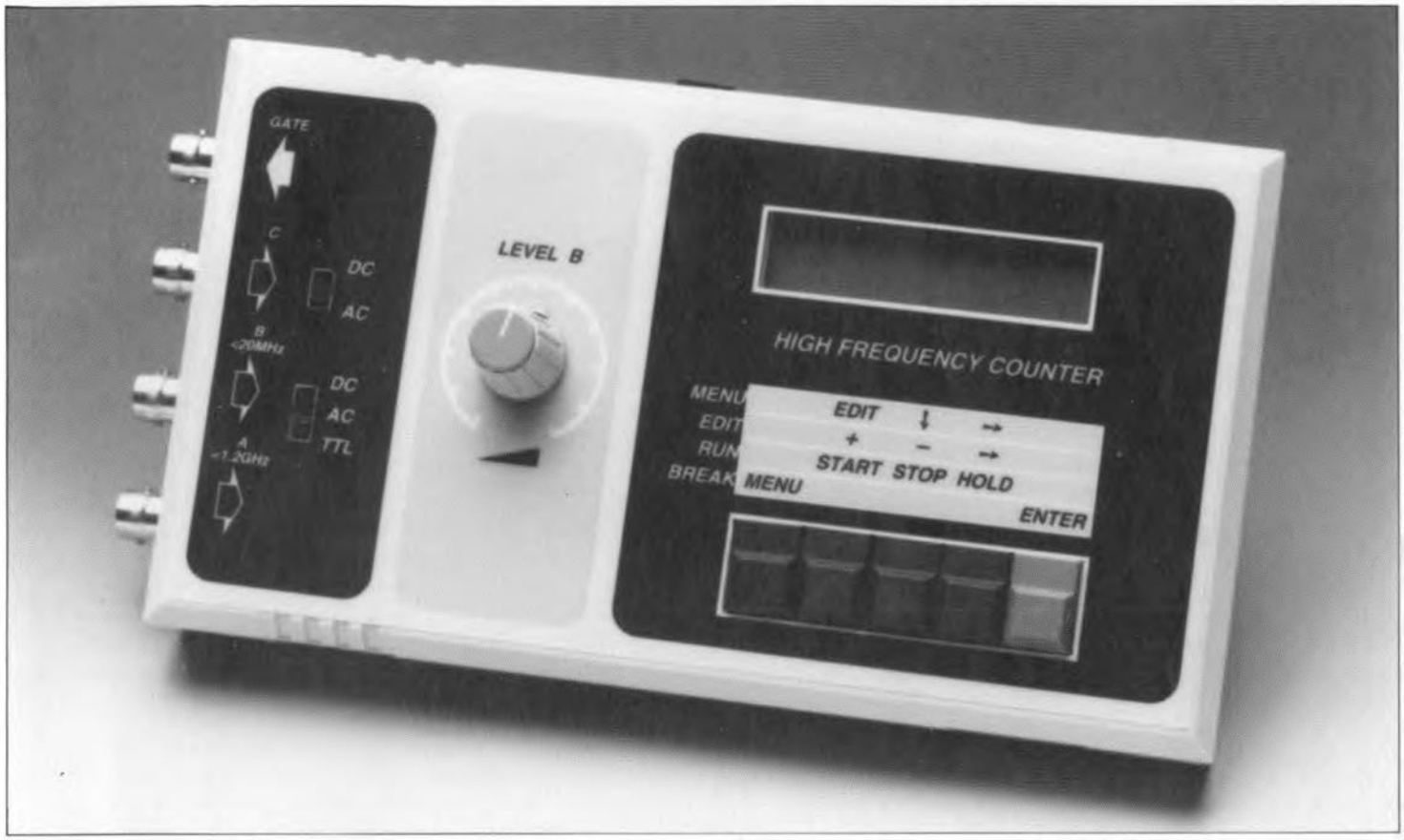


3M Electronic Products, 3M UK plc, Market place, Bracknell, Berks RG12 1JU. Telephone: (0344) 426726.

1.2 GHz MULTIFUNCTION FREQUENCY METER

g20095

PART 1: CIRCUIT DESCRIPTION



The instrument described in this three-part article is one you can not afford to give a miss since it is very likely the most advanced frequency meter/pulse generator you can build yourself. Sporting microprocessor control, pulse and period measurement, a battery power option, a built-in pulse generator, LCD readout and fully menu-driven operation, the instrument is compact and portable, and a worthy successor to our famous 1985 microprocessor controlled frequency meter, thousands of which are in use all over the world.

FRONT COVER PROJECT

Design by B. C. Zschocke

THE use of a powerful microprocessor gave an interesting turn to the development of the present instrument: what was but a simple frequency meter at one stage evolved into a multifunction test instrument that can be built at a fraction of the cost of a commercial equivalent. The basic thought was this: if the simple instrument is capable of measuring frequency and pulse duration, why not use the microcontroller's power to reverse these functions, and **output** programmable signals as well? After all, the design was already quartz-controlled, and the measuring algorithms available. Thus, by extending the control software, the original frequency meter was turned into the multifunction instrument described here. The final result is a versatile, accurate and extremely sophisticated piece of test equipment you would, of course, only expect to see described in *Elektor Electronics*.

A brief list of features would look something like this:

- Universal counter and signal generator;
- Powered by mains or by batteries;
- Compact and portable
- Alphanumerical two-line LCD readout;
- Menu-driven;
- Serial interface for connection to a PC;
- Low cost — no expensive components.

The choice of the microcontroller to use in the instrument was not a difficult one. Intel's 80C32 is a CMOS controller with very low power consumption, which allows the instrument to be battery powered. The 80C32 has the ports required to drive a two-line LC display, to interface to the measurement peripheral circuitry, and to convey data via a serial interface. The ports allow the additional hardware to be reduced to a couple of gates, an EPROM from which the control program is run, an analogue signal shaping section, and an LC display. The LCD is used to display data as well as the menu that assists the user in setting up the instrument parameters for a particular type of measurement or signal generator mode.

CONCISE SPECIFICATION

Features:
2 inputs with AC/DC selectable input
1 TTL input
GATE output (short-circuit proof)
RS232 serial interface for PC control
Extension port
Battery or mains powered
Two-line (2×16 character) alphanumerical LCD readout
Single or continuous measurement
Compact size (20×11×3.5 cm) and lightweight
Excellent price/performance ratio

Measurement modes:
Frequency meter: 1 mHz to 1.2 GHz
Period (1/frequency): 1 ps to 4,000 s
Revolution counter: 0.001 to 4×10^6 rev/min
Event (pulse) counter: 1 to approx. 4×10^9
Zero counter: 1 to 4×10^9

Generator modes:
Timer: 1 µs to 4,000 s
Pulse generator: 8,500 s (0.117 mHz) to 4 µs (250 kHz)
Duty factor: 1:1 to $1:4\times10^9$
Period number: 1 to 4×10^9

User-defined settings:
Single/continuous measurement
Floating gate time
Intermediate measurement result display
Period analysis (accurate measurement of low frequencies at short gate periods)
Quiescent level
Pulse polarity
Sounder on/off

Test routines:
LCD test
Main test
Serial I/O test

Note: mHz = millihertz (0.001 Hz); kHz = kilohertz (1,000 Hz); MHz = megahertz (10^6 Hz); GHz = gigahertz (10^{12} Hz); ps = picoseconds (10^{-12} s).

Provision has been made to test the instrument in steps. Test routines are implemented in the software to help those of you who get stuck with a certain fault during the construction, and do not know whether the cause is hardware or software (this is often a problem with microprocessor controlled equipment). The test routines should help you locate the error in a step-by-step manner, since they address sub-sections of the circuit in a rather clever way.

Block diagram

The 80C32 has three internal counters, which are used here to implement a frequency meter. One counter is used to provide the gate time, the second to count pulses. Unfortunately, there is a snag in this set-up: the highest frequency that can be measured is lower than 1/24 times the oscillator frequency. Obviously, this will not do for a GHz frequency meter, hence the use of a prescaler to overcome the problem. The prescaler is shown in the lower left-hand corner of the block diagram in Fig. 1. Two different input signal paths are possible: either via channel A and a GHz prescaler (IC10), or via channel B and a preamplifier, T1-T4-T5. A multiplexer selects one of the signals, and outputs it to a further prescaler, IC5. Actually, IC5 should be labelled 'pre-counter' rather than 'prescaler', but this may be less familiar. The carry output of IC5 ensures sufficiently long pulses at the microcontroller timer/counter inputs, T0 and T1. The operation of prescaler IC5 is controlled by the microprocessor via port line P1.7. The prescaler enable signal is also the counter gate signal, which is amplified by T7-T8 and output to the GATE output of the instrument. This output also supplies gate pulses when the instrument is used as a signal generator.

Channel C serves to set up different trigger conditions (positive or negative pulse edge), and is connected to the interrupt inputs of the microcontroller. This allows the selection between the trigger conditions (positive or negative signal edge) to be made in software.

The operation of the frequency meter is based on the reciprocal pulse count principle. A gate time is set up during which the input frequency and a reference frequency are measured. The reference frequency is supplied by the third counter contained in the 80C32. The input frequency is calculated by dividing the two counter states, and subsequent multiplication of the re-

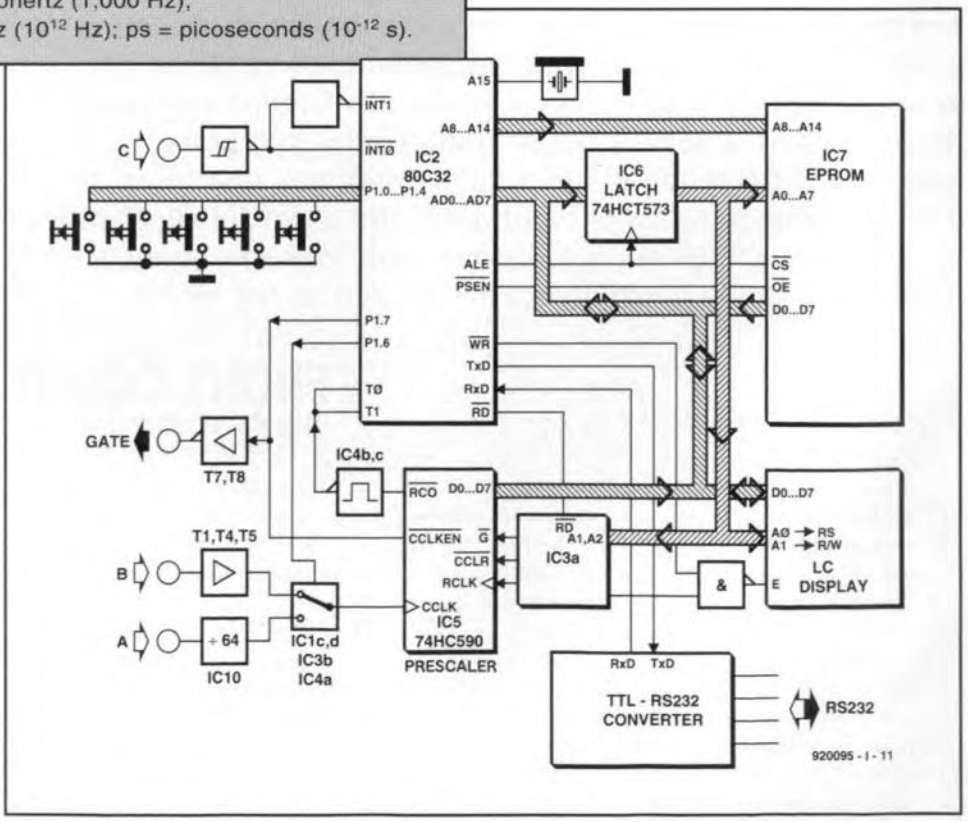


Fig. 1. Block diagram of the multifunction frequency meter.

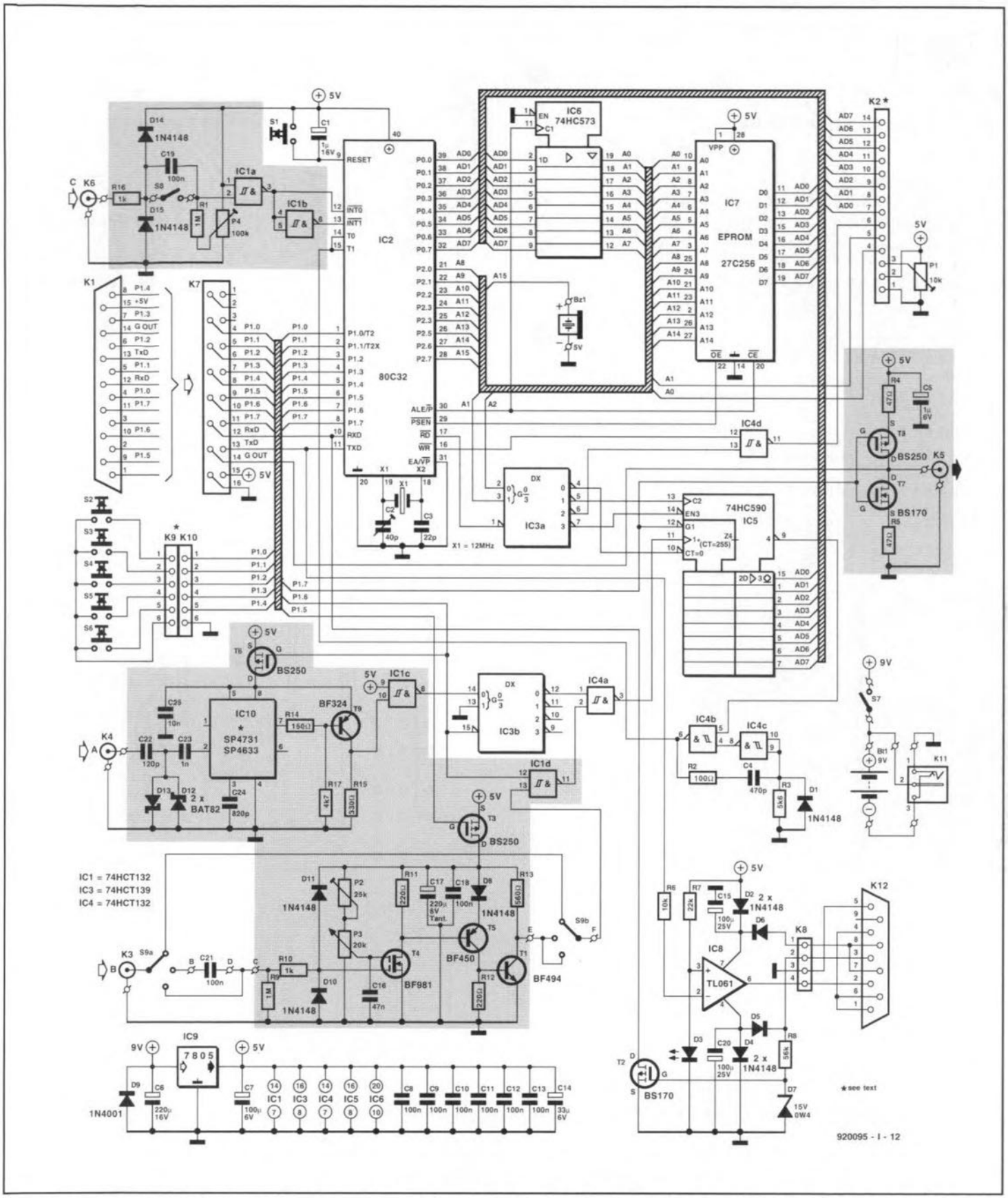


Fig. 2. The functional blocks shown in Fig. 1 are easily found back in the circuit diagram of the instrument. Note that the shaded sections are enclosed in a metal screening to prevent spurious radiation affecting the measurements.

sult with the reference frequency. Provided the gate time is properly synchronized to the input signal, this system allows very low frequencies to be measured with great accuracy. More about the frequency measurement principle in a separate article instalment!

The circuit in detail

Since the elements that make up the block diagram (Fig. 1) are fairly easily found back in the circuit diagram (Fig. 2), we can limit ourselves to noting the 'not so obvious' only.

Input A is provided for high frequencies (>20 MHz). The high frequency signal reaches the GHz prescaler via coupling capacitors C22-C23. Two Schottky diodes, D12 and D13, limit the input voltage swing to ±0.3 V maximum. It is important to note that a number of equivalent or near-equiv-

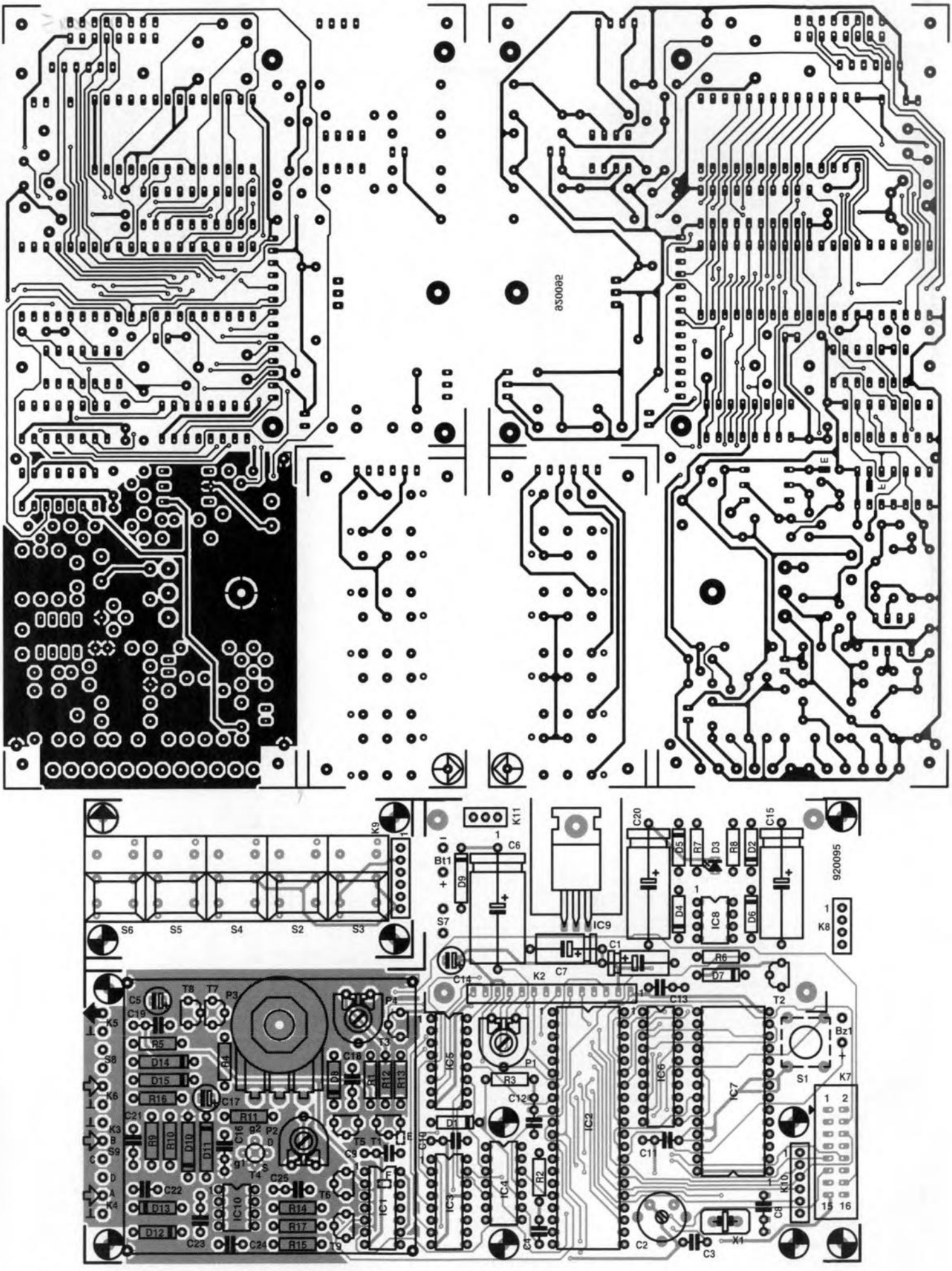


Fig. 3. Artwork for the double-sided through-plated printed circuit board.

COMPONENTS LIST

Resistors:

2	1MΩ	R1;R9
1	100Ω	R2
1	5kΩ6	R3
2	47Ω	R4;R5
1	10kΩ	R6
1	22kΩ	R7
1	56kΩ	R8
2	1kΩ	R10;R16
2	220Ω	R11;R12
1	560Ω	R13
1	150Ω	R14
1	330Ω	R15
1	4kΩ7	R17
1	10kΩ preset H	P1
1	25kΩ preset H	P2
1	20kΩ potentiometer linear, 6mm spindle dia.	P3
1	100kΩ preset H	P4

Capacitors:

1	1µF 16V	C1
1	40pF trimmer	C2
1	22pF	C3
1	470pF	C4
1	1µF 6V3 radial	C5
1	220µF 16V	C6
1	100µF 6V3	C7
10	100nF	C8-C13;C18; C19;C21
1	33µF 10V tantalum	C14
2	100µF 25V	C15;C20
1	47nF	C16
1	220µF 6V3 tantalum	C17
1	120pF	C22
1	1nF	C23
1	820pF	C24
1	10nF	C25

Semiconductors:

10	1N4148	D1;D2;D4;D5; D6;D8;D10; D11;D14;D15
1	LED, green, 3mm dia.	D3
1	15V 0.4W zener diode	D7
1	1N4001	D9
2	BAT82	D12;D13
1	BF494	T1
2	BS170	T2;T7
3	BS250	T3;T6;T8
1	BF981	T4
1	BF450	T5
1	BF324	T9
2	74HCT132	IC1;IC4
1	80C32	IC2
1	74HCT139	IC3
1	74HC590	IC5
1	74HCT573	IC6
1	27C256 EPROM (ESS 6141; see page 110)	IC7
1	TL061	IC8
1	SP4731 or SP4633 (Plessey). Alternatives: SDA4212 (Siemens); U664B (Telefunken); SAB6456 (Philips Semiconductors)	IC10
1	7805	IC9

Miscellaneous:

1	9-V PP3 battery	Bt1
1	passive 5V piezoceramic buzzer	Bz1
1	15-way sub-D socket	K1
1	combination of 14-way SIL header and socket	K2
4	BNC socket; single-hole mounting	K3-K6
1	16-way box header	K7
1	4-way SIL pin header	K8
1	6-way IC pin strip or SIL socket	K9
1	6-way IC pin strip or pin header	K10
1	mains adaptor socket	K11
1	9-way sub-D socket	K12
1	PCB mount press-key (Multimec 2CTL2)	S1
5	Press-key (Digitast)	S2-S6
4	Black keycap (w=12mm)	
1	Red keycap (w=12mm) (ENTER)	
2	SPST slide switch	S7;S8
1	3-position slide switch	S9
1	12MHz quartz crystal	X1
1	LCD module 2×16 characters; 1 row of 14 connections. Preferred type: LTN211F10 (Philips Components). Alternatives: LM016L (Hitachi); EA-D16025AR (Seiko-Epson).	
1	ABS enclosure; Bopla EG2030	
1	9-V battery holder; Bopla BE30	
1	9-V battery clip with wires	
4	M2.5×16mm or M2.5×20mm screw	
8	M2.5 nut	
4	M3×16mm or M3×20mm screw	
8	M3 nut	
8	Plastic PCB spacer, 10mm long	
IC sockets for IC1-IC8 and IC10		
30	Solder pins, 1mm dia.	
1	PCB plus software, order code 920095 (see page 110)	
1	Front panel foil 920095-F	

Suggested component suppliers for this project:
Cricklewood Electronics (081) 4520161 (passives and semiconductors); Electrovalue Limited (0784) 33603 (passives, semiconductors and Siemens parts); C-I Electronics (fax +31 45 241877) (passives, semiconductors; case; switches, LCD and kits).
These are not exclusive suppliers; others may also be able to help.

alent ICs may be used for the GHz prescaler. Unfortunately, some of these, including the SDA4212, U664B, SAB6465 and SP4731, have a tendency to oscillate when no input signal is applied. The instrument then indicates a random frequency. This effect is normal, however, and no cause for alarm. Other ICs, like the SP4633, are stable in the absence of an input signal, however offer insufficient amplification at signal frequencies below 50 MHz or so. An RF transistor, T9, converts the prescaler output into TTL level. Since the GHz prescaler IC has a typical current consumption of the order of 50 mA, provision has been made to switch it off when it is not used. This is achieved with the aid of FET T6, which is controlled by the microprocessor via port line P1.6. This means that the current reduction is achieved via the instrument's user menu.

Input B is intended for input signals with a frequency below about 20 MHz. Input selection switch S9 on channel B allows you to choose between (1) no preamplifier (TTL input); (2) a.c. coupled or (3) d.c. coupled. Depending on the switch setting, the channel B input signal arrives either at pin 13 of IC1d, or at gate 1 of DG-MOSFET T4 (via R10 and protection diodes D10-D11). Potentiometer P3 allows the operating point of the MOSFET amplifier to be adjusted depending on the required sensitivity. Transistors T4 and T1 give the amplified and rectangular-wave limited signal a TTL swing. The amplifier is quite sensitive to supply voltage fluctuations, whence the presence of decoupling capacitors C17 and C18. Like the GHz prescaler, the TTL level converter can be switched off to reduce current consumption. the switching transistor is again a FET, T3. Preset P2 serves to limit the span of the sensitivity potentiometer, P3.

Input C is not followed by a preamplifier. To still ensure the highest possible sensitivity, one input of Schmitt trigger gate IC1a is raised to a potential just between the higher and the lower switching threshold. This potential is adjusted with preset P4. Note, however, that this 'raised quiescent level' is only effective when S8 is set to a.c. coupled. Components R16 and D14-D15 protect the input.

The channel A and B input multiplexer is built with a part of demultiplexer IC3. The channel A input signal, shaped and inverted by IC1c, is switched through to one of the multiplexer outputs 0-3 under the control of the signal applied to the enable input (pin 15). The relevant output is selected by the logic level combination applied to the 0-1 inputs. Since the input signal is connected to the '0' input, the output toggles (pins 12/11). When the enable signal is low, output 0 supplies a copy of the input signal, and output 1 the inverted input signal. When the enable pin is pulled high, all demultiplexer outputs are high. At the same time, channel B is enabled via IC1d. The channel A and channel B signals are combined in IC4a.

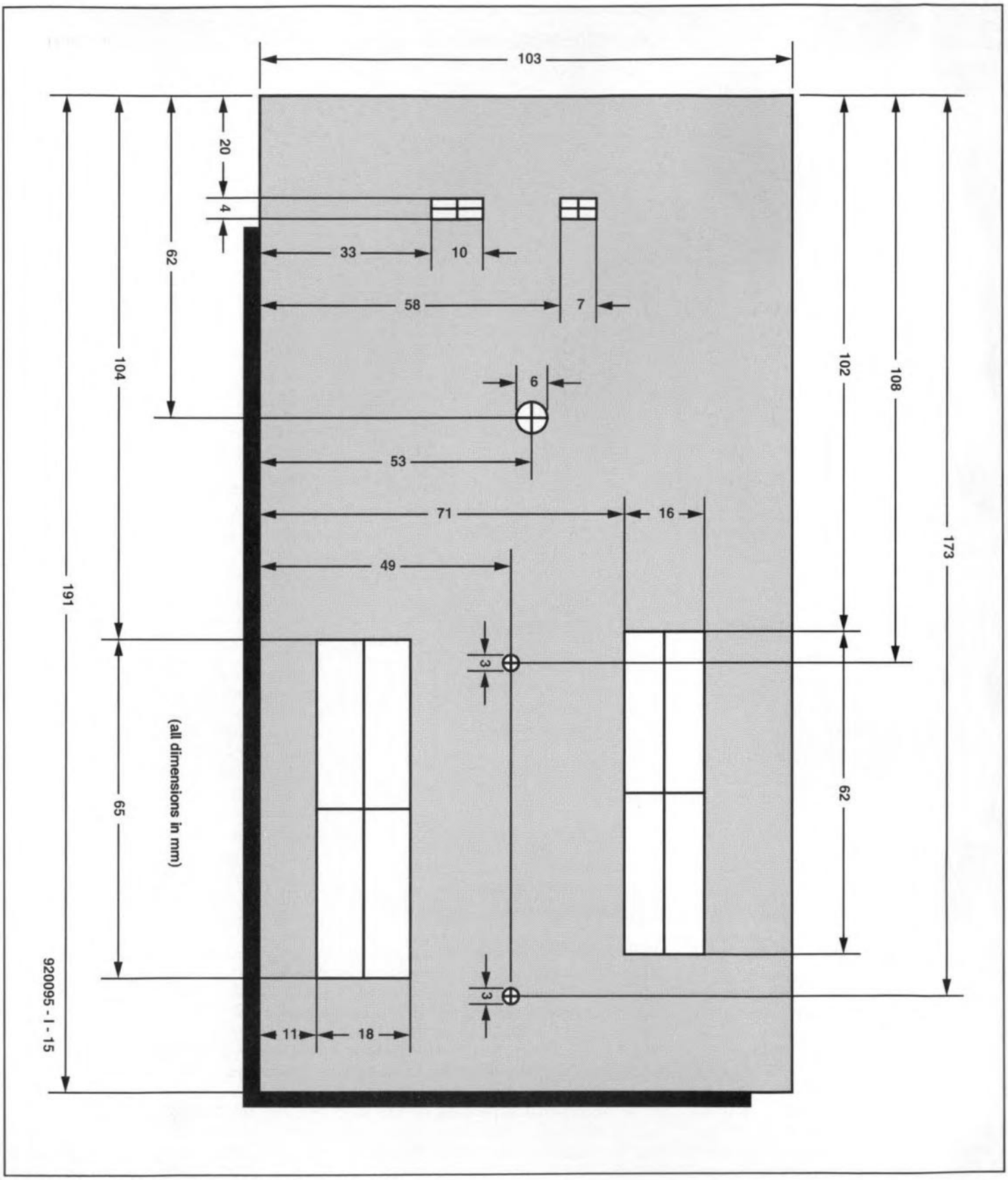


Fig. 4. Drilling template for the front panel of the instrument.

Schmitt-trigger gates IC4b and IC4c form a monostable that serves to lengthen the carry pulse supplied by external counter IC5. The pulse length is determined by C4 and R3. Diode D1 and resistor R2 protect the input and output of this circuit against the small peak at the end of the pulse. If the carry pulse is longer than the monostable time, the monostable effectively does nothing.

Transistors T7 and T8 provide the necessary drive at the GATE output of the instrument. Resistors R4 and R5 limit the drain-source currents of the FETs to the extent of making the output short-circuit resistant.

The TTL-to-RS232 converter is built around IC8 and T2. It does not require a separate ±12-V supply since it is powered by the PC's RS232 port. If this is initialized and not in use, the TxD (transmit data) line is at –12 V, and the RTS (request to send) line at +12 V. A supply voltage of –12 V is built up across capacitor C20 (via diode D5), and a supply voltage of +12 V across capacitor C15 (via diode D6). Diodes D2 and D4 protect the circuit when the RS232

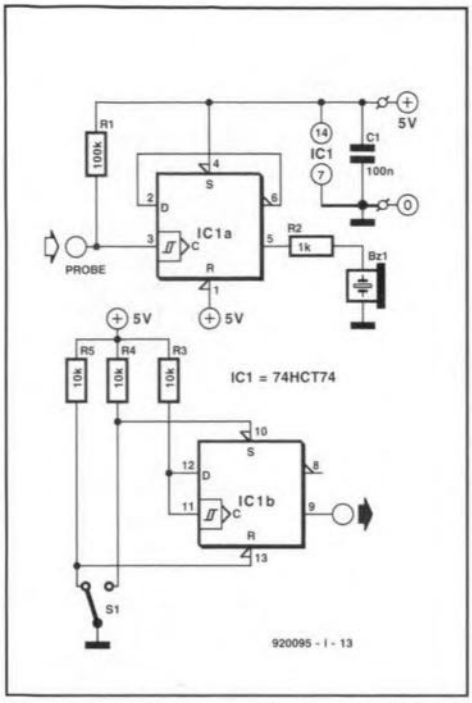


Fig. 5. Lacking an oscilloscope, build this simple adaptor circuit to test a number of sub-sections of the circuit.

interface is not connected, or when the port is incorrectly initialized on the PC. IC8 converts the microcontroller's serial output pulses into an RS232 compatible signal. The voltage drop across LED D3 is about 2 V, which serves as the reference voltage. The TxD signal from the PC is first limited to +15 V (max.) by resistor R8 and diode D7. Next, it is inverted by FET T2, and fed to the microcontroller's RXD input. An external pull-up resistor is not required since this is contained in the 80C32.

The instrument contains a piezoceramic buzzer, Bz1, of which the drive is slightly unconventional. The buzzer is a passive type connected to address line A15. This line is not decoded, which means that the content of the 32-kByte large EPROM is 'mirrored' in the upper half of the 64-kByte address space. This circumstance is exploited by to enable the microcontroller to drive the buzzer by toggling A15.

Construction

The instrument is built on a double-sided through-plated printed circuit board of which the artwork is shown in Fig. 3. This PCB is available ready-made, together with the control software in EPROM, through our Readers Services (see page 110). To prevent noise and spurious radiation from the digital section affecting the measurements, it is necessary to fit a metal screening around the channel B amplifier and the channel A prescaler. The relevant sections of the circuit are indicated by a background shade in the circuit diagram.

Returning to the PCB, start by breaking off the keyboard section. The space so created in the enclosure is used to fit the 9-V battery holder later. Check that this can be done using the unpopulated board, the case and the battery holder. The connecting wires of the switches must be cut off as far as possible because the keyboard PCB is fitted on top of the main PCB later.

Make sure that the clearances in the enclosure for the keyboard, the LCD and the slide switches, as well as the hole for the spindle of potentiometer P3 ('LEVEL B'), are cut and drilled before actually fitting and connecting these parts. The same goes for the small holes that give access to the LCD contrast preset, P1, and the reset switch, S1. If you can get hold of low-profile parts you may want to fit the preset and the switch at the track side of the board, and make holes in the bottom half of the enclosure.

The cutting and drilling details for the plastic case are given in Fig. 4. After finishing the mechanical work on the case, take the populated keyboard and the LCD module, and fit them provisionally on the main board using plastic PCB spacers. Adjust the length of the spacers until the LCD and the keyboard are at the desired height (try the 'fit' by mounting the top half of the enclosure a couple of times).

On the main board, fit all resistors, all diodes (except D3), and all transistors (except T4). Take care to avoid short-circuits with the screening around the prescaler and input preamplifier section. Next, concentrate on transistor T4, which must be fitted as close as possible to the PCB surface. Also note the orientation of this MOSFET: depending on the manufacturer of the device, the drain is usually the longest terminal of the four.

Proceed by fitting the IC sockets, followed by the remainder of the compo-

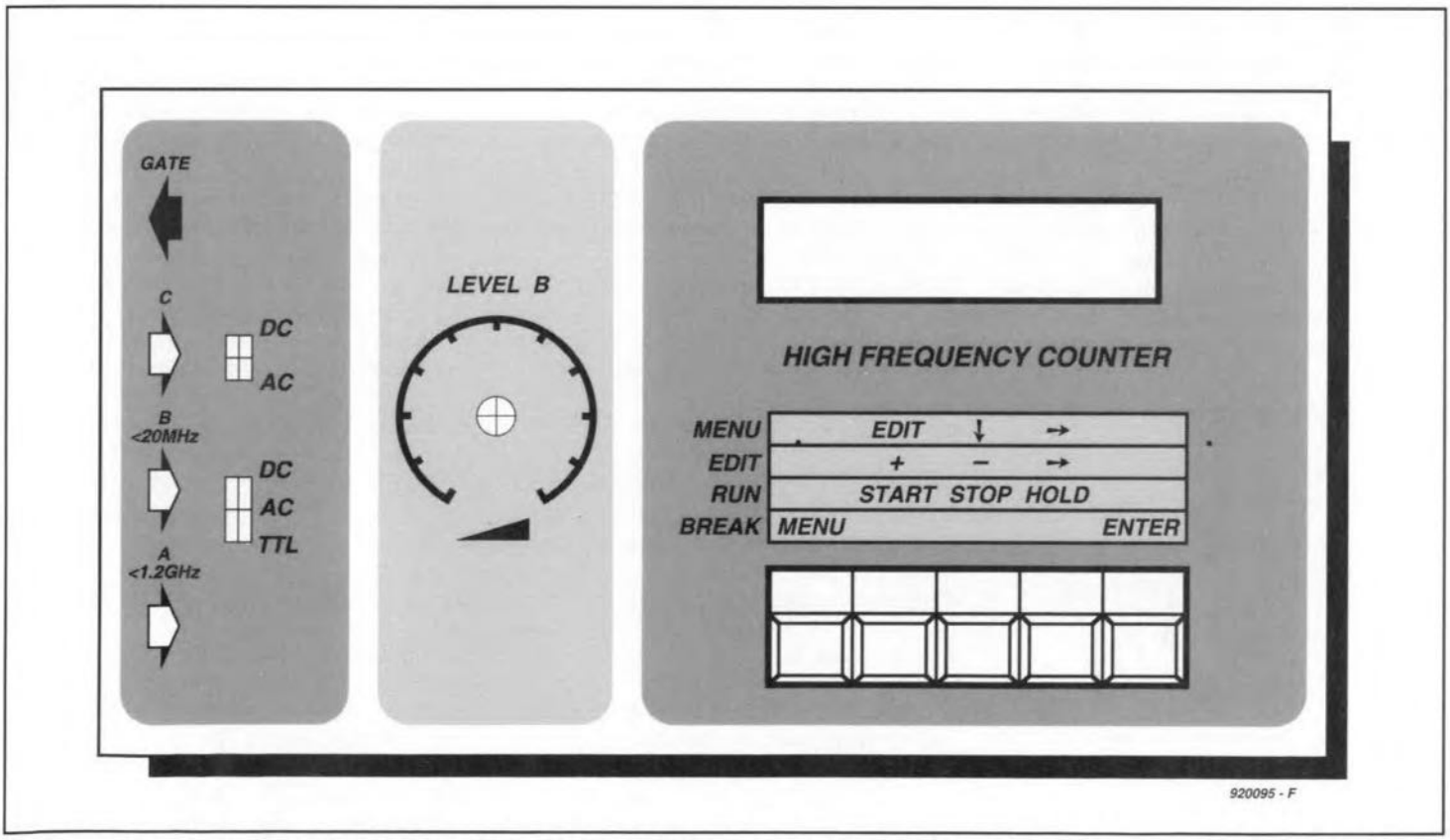
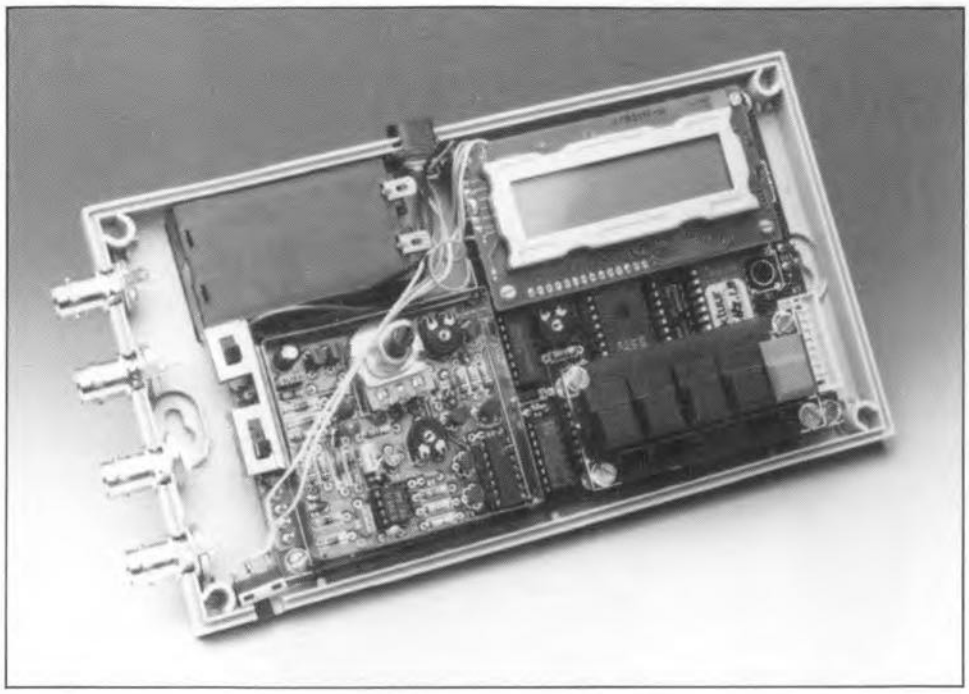


Fig. 6. Front panel foil design shown reduced to about 82% of true size. The ready-made three-colour self-adhesive foil is available through our Readers Services.



nents. To enable the LCD and the keyboard to be fitted properly, it may be necessary to cut off the small plastic studs at the underside of trimmer capacitor C2. LED D3 is mounted like a resistor, i.e., straight on to the PCB surface. It has no function as a visual indicator, and is obscured by the LCD module above it.

The keyboard does not need connecting wires. A length of wire wrap style IC pin strip may be used to make a 6-way pin header (K9) and a 6-way mating socket, K10. Note that the pins that form K9 must be mounted at the solder side of the keyboard PCB. The display connections are made in a similar way. The LTN211-F10 LCD module (from Philips Components) used in the prototype was fitted with a 14-way SIL socket, of which the connecting wires were left at a length of about 3 mm, so that the body of the connector is at about 5 mm of the underside of the LCD board. This socket mates with a 14-way pin header, K2, on the main board. Note that such a direct connection may not be possible with other LCD modules, in which case a bit of wiring may be necessary.

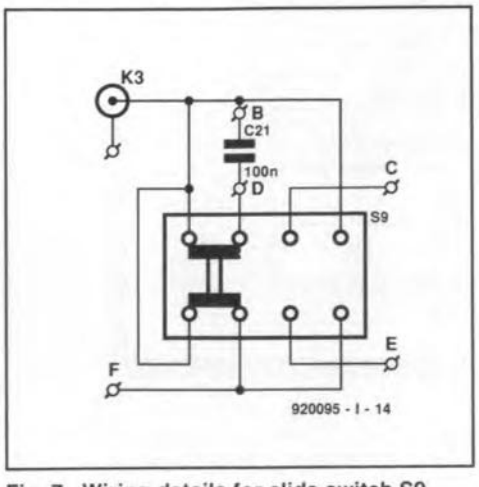


Fig. 7. Wiring details for slide switch S9.

With the exception of S7, S8 and S9, all switches are fitted direct on to the PCB. S9 is a two-pole three-position slide switch of which the wiring is given in Fig. 7. Points B, C and D are solder pins at the PCB edge. Point E is a solder pad at the PCB underside, next to transistor T1. The same goes for point F (solder pad underneath IC1). Be sure to use screened cable here.

At this stage, you are ready to fit the screening around the prescaler/preamplifier input. Bend an approximately 240-mm long, 13-mm high, piece of tin plate or brass around the solder pins in the four corners of the PCB section, as indicated by the component overlay. Solder the screening to the corner pins. Next, cut and bend a cover for the screening using the same plate material. Drill holes in the cover to enable the spindle of P3 to pass, and to give access to presets P2 and P4. Do not mount the cover on to the screening until the circuit has been adjusted and tested.

The two slide switches, S8 and S9, may be glued on to a small bracket which is soldered to the screening. Most of the above construction details are illustrated in the photograph of the opened prototype.

First test

Give your construction a thorough inspection before connecting the supply voltage. At the component side, look for incorrectly oriented polarized parts (diodes, electrolytic capacitors, transistors, ICs). At the solder side, look for dry joints, splashes and hair joints between solder spots.

Turn presets P1 and P4 fully clockwise, and P2 fully anti-clockwise. Turn the potentiometer, P3, fully clockwise.

Fit the keyboard PCB and the LCD module, connect the power supply (a mains adaptor), and switch the instrument on. Adjust the LCD contrast preset, P1, until the text

GHertz counter
START or MENU

can be read on the display. What to do if these two lines do not appear? Not to worry, the test routines built into the instrument will come to your aid. All you need in addition to the following text is a multimeter and an oscilloscope. If you do not have an oscilloscope, build the small test adaptor shown in Fig. 6. A PC is required to test the RS232 interface of the instrument.

Test routines

The frequency meter must be switched off immediately if the power-on message does not appear on the display. Disconnect the power supply and check its output voltage. If this is okay, connect it to the instrument again, switch on, and measure the current consumption. Any value greater than about 100 mA indicates a fault, the most likely of which is that the supply voltage is reversed (when D9 conducts). If this is not the case, the fault may be a short-circuited copper track, or a defective component.

For the following tests it is assumed that the CPU, the EPROM, the quartz crystal and the address latch function correctly. Display indications are printed *in italics*.

The test routines can be divided into three main groups: LCD test, main board test, and serial I/O test. The instrument is switched to the test mode by keeping the MENU or ENTER key pressed at power-on, whereupon you enter a wait routine (*End Test with >> BREAK <<*). From this wait loop, you can call up a group of test routines by pressing the appropriate key (see below). The wait loop is left when the ENTER and MENU keys are pressed simultaneously (BREAK), whereupon the instrument switches to its normal mode of operation. Within the groups, the individual tests are completed one after another. You can move through the tests by pressing the ENTER key. However, the *Key-test* can be left only by a BREAK, i.e., by pressing MENU and ENTER simultaneously.

LCD test (Group 1)

Pressing the START key takes you into the *LCD test*. Alternatively, you can enter this test directly by keeping the START key pressed at power-on. Provided the LCD works (adjust the contrast with P1!), the text *LCD-test: press ENTER to go on* appears. After pressing ENTER two times, the instrument enters the test for IC3a. This test causes outputs 0 and 1 of IC3a to produce tones that can be heard when the test adaptor is connected. These tones are visible on an oscilloscope as rectangular signals with near-TTL swing. The next test routine drives the inputs of IC4d alternately. The resulting tone at the output of the gate is two times as high as the input

tones. In this test mode, the LCD indicates an irregular pattern.

The last test in the LCD group feeds all characters contained in the character set to the display. The characters move from the end of the lower display line to the start of the top line. Since the user-defined characters in the set have not been set up at this stage, it is possible that random patterns appear between the standard ASCII character set and the Japanese character set. For the following tests, it is assumed that the display functions correctly.

Main board test (Group 2)

The *Main test* group is entered by pressing the STOP key. Alternatively, you can enter this test directly by keeping the STOP key pressed at power-on.

The first test, *Key-test*, serves to check the operation of the keyboard section. It prompts you to press a certain key, and indicates its function in the RUN mode. Do a BREAK to leave this test. The next test is the *Gate-Out test*, which should produce an audible signal on microcontroller port line P1.7. This signal can be traced right up to the GATE output with the aid of the test adaptor or the oscilloscope. If it arrives at the GATE output, the wiring of P1.7 and the transistor output driver are all right.

Next, the *Channel-A Test* switches on the GHz prescaler via T6 (+5 V at pin 8 of IC10, and at the emitter of T9). The channel switch is set to channel A. At the same time, a frequency of 971 Hz is generated at the GATE output. This signal may be used to test the channel selector and T9. This requires switching off the instrument, and removing the prescaler, IC10. Connect the GATE output to pin 7 of the empty IC socket via a 100-nF capacitor. Switch on, step through the test menu, and run the test. Check that an audible tone is present at the following points: pins 8 and 10 of IC1c, pins 12 and 14 of IC3b, and pins 1 and 3 of IC4a.

During the *Channel-B Test*, the channel selector is switched to channel B, and the associated preamplifier is switched on via T3 (+5 V on C17). The GATE output supplies a 971-Hz test signal, which may be connected directly to the channel B input. The test tone should be audible at transistors T1, T5 and T4, at pins 13 and 11 of IC1d, and at pins 2 and 3 of IC4a.

For the *Channel-C Test* it is necessary to connect the GATE output to the channel C input, with the input coupling set to DC. If the display shows *??* behind *IC1A* or *IC1B*, either the connection between channel C and the GATE output is at fault, or the relevant integrated circuit. When everything is in order, the display shows *OK*.

The *Pre-counter Test* serves to check the function of IC5, IC4b and IC4c. Since the GATE output is used to control the pre-counter, input B must be supplied with an external frequency. This may be the ALE signal (CPU pin 30, EPROM pin 20, or IC6 pin 11). The input frequency divided by 256 is then available at pin 9 of IC5, and at pins 4, 5, 6, 8, 9 and 10 of IC4.

The last test in this group is the *Buzzer test*, which should cause the buzzer to produce an audible tone when the HOLD key is pressed.

Serial I/O test (Group 3)

This group of test routines is entered by pressing the HOLD key, and serves to check the operation of the RS232 interface. Alternatively, you can enter this test directly by keeping the HOLD key pressed at power-on.

To be able to use the tests, connect the instrument to a PC on which a communication program is run. This program should initialize the RTS output. The PC and the counter should not have any other electrical connection than the RS232 link. In a follow-up publication we will describe an optocoupler circuit for insertion between the PC and the frequency meter. Such a circuit guarantees a potential-free coupling in all cases.

The data transfer rate is set to 2400 baud. After the PC has completed the initialization of the RS232 port, you should be able to measure a positive voltage across C15, and a negative voltage across C20. These voltages are measured with respect to ground, and must be considerably greater than 5 V. Pin 3 of IC8 should be at about 2 V with respect to ground.

During the *SIO Send Test*, the instrument sends a continuous string of *BCZ* characters to the PC. In case the characters are transmitted too fast, you can slow them down by pressing the HOLD key. The SIO Send routine checks the function of opamp IC8.

The *SIO Receive Test* is used to verify the operation of the RS232 receiver circuitry in the instrument, in particular, T2. Characters you type on the PC should be displayed on the LCD.

That concludes the descriptions of the test routines built into the frequency meter. The test mode may be left by doing a BREAK.

Alignment

The alignment of the frequency meter is very simple and should not present problems. First, set all presets, and the potentiometer, to the positions mentioned in the section 'First test'. Adjust P1 until the LCD contrast is optimum. Next, turn P3 fully clockwise (full amplification on channel B). Measure the collector voltage of T1, and adjust P2 for a reading of 2.5 V. Next, carefully turn P4 counter-clockwise until pin 3 of IC1a changes from high to low. Measure and record the voltage at the wiper of P4 with the aid of a high-impedance voltmeter. This is the high switching level of the Schmitt trigger gate. Carefully turn the wiper back again until the output reverts to logic high. This point corresponds to the low switching level of the Schmitt trigger gate. Measure the wiper voltage, add it to the high switching level, and divide the result by two. Adjust the preset to give this centre voltage. Alternatively, if you do not have a high-impedance voltmeter, find the switching levels, and set the wiper as accurately as possible in between the two corresponding wiper positions.

Next, the central oscillator is adjusted to 12 MHz exactly. This is best done by applying a known, high-precision test frequency to the meter, and adjusting trimmer capacitor C2 until this frequency is displayed. In case the span of C2 is too small, fit a small capacitor (20 pF) in parallel with the quartz crystal.

SYSTEM TESTS

Component	Test Group	Test
T1	Group 2	Channel B
T2	Group 3	SIO-Receive
T3,T4,T5	Group 2	Channel B
T6	Group 2	Channel A
T7,T8	Group 2	Gate-Out
T9	Group 2	Channel A
IC1a,b	Group 2	Channel C
IC1c	Group 2	Channel A
IC1d	Group 2	Channel B
IC2	test not possible	
IC3a	Group 1	IC3a
IC3b	Group 2	Channel A
IC4a	Group 2	Channel B
IC4b,c	Group 2	pre-counter
IC4d	Group 1	IC4d
IC5	Group 2	pre-counter
IC6,IC7	test not possible	
IC8	Group 3	SIO-Send
IC9	power supply	
IC10	test not possible	
S2 - S6	Group 2	keyboard
Bz1	Group 2	buzzer

Operation

Press the MENU key to enter the normal (measurement) mode of the instrument. Menu options are selected by pressing the 'down' key, and the selection is confirmed by pressing the ENTER key. The next menu then appears. The EDIT key allows user defined settings to be entered. The EDIT mode can be left by pressing the ENTER key. Pressing the MENU and ENTER keys simultaneously takes you out of the menu mode. The same key combination is used to end a measurement. A more extensive description of the various menu options will be given in a future instalment. ❑

Part 2 of this article will give detailed descriptions of all menu options and instrument settings.

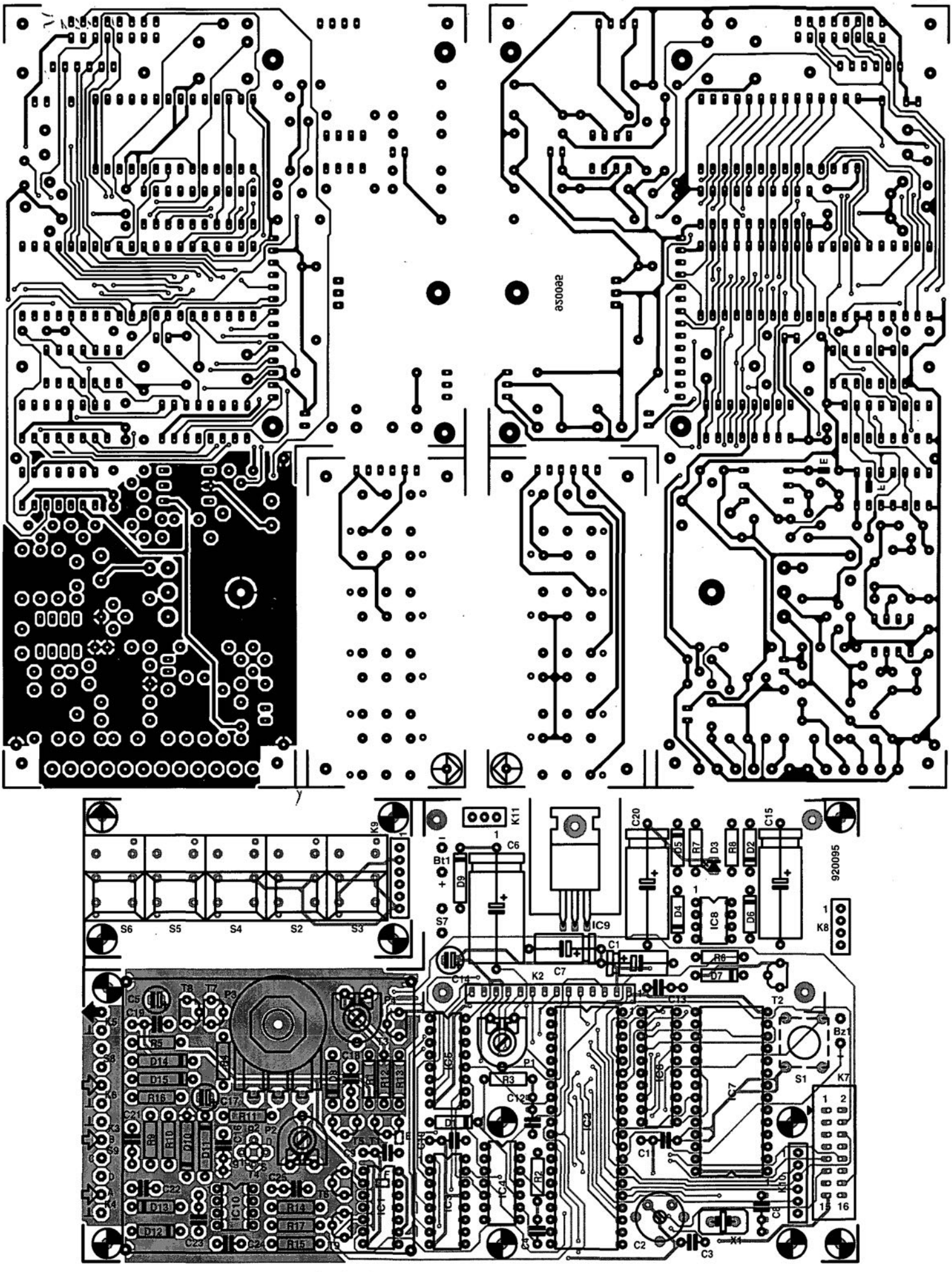


Fig. 3. Artwork for the double-sided through-plated printed circuit board.

CORRECTIONS AND UPDATES

I²C interface for PCs

February 1992

The PCD8584 iused in this project is no longer manufactured by Philips Semiconductors, and replaced by the PCF8584. This is a fully compatible IC and only improved as regards the 4-wire long-distance mode, which did not work correctly on the PCD8584.

Real-time clock for 80C32 computer

June 1993

Contrary to what is implied by the description of the parallel connection of the SmartWatch IC pins with the EPROM pins, pin 1 of the SmartWatch should be connected separately to +5V, for instance, to EPROM pin 28, via a short wire. This is necessary because pin 1 on the SmartWatch is 'reset', while on the EPROM it is address line A14, which may be made high by 'high' addressing or glitches, causing the clock to be reset.

VHF-low converter

June 1993

The parts list should be corrected to read:

1	2µH2	L3
1	0µH1	L5

The circuit diagram is correct.

The sub-1µH chokes used in this project are available from, among others, Cricklewood Electronics.

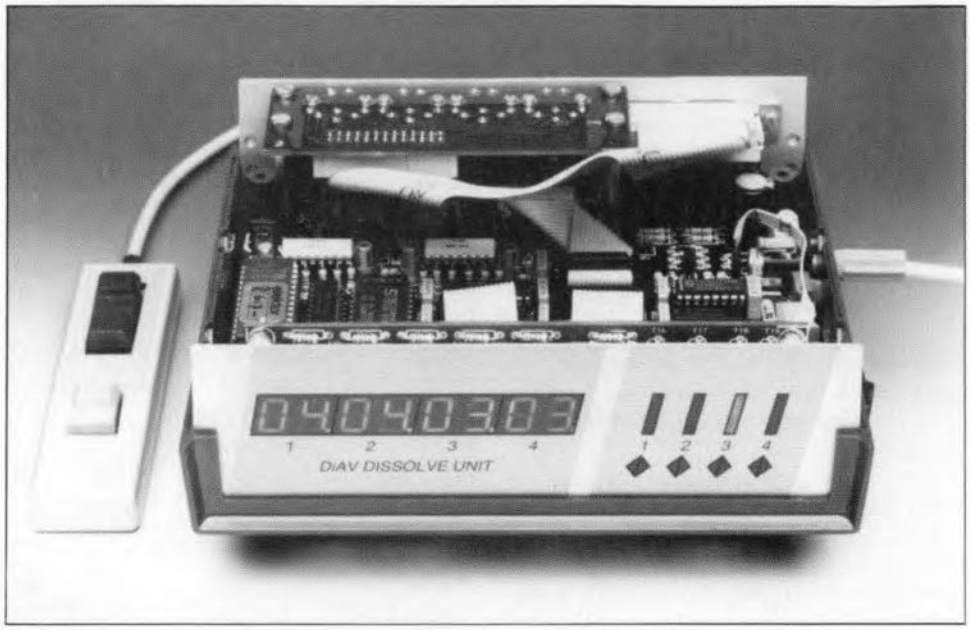
1.2 GHz multifunction frequency meter

December 1992

The recommended LCD module Type LTN211-F10 is no longer manufactured by Philips Components, and may be replaced by the compatible types LM016L from Hitachi, or the LM16A21 from Sharp.

DIGITAL AUDIO/VISUAL SYSTEM

PART 2: CONSTRUCTION



After last month's introduction and the description of the dissolve unit and the projector, we are now ready to tackle the construction of the various modules that make up the DiAV system. As you may recall, there are two construction options: all modules in one enclosure, or each module in its own enclosure. In this instalment, we deal with the latter option.

Design by A. Rietjens

Fitting all DiAV system modules in separate enclosures has the advantage of allowing full use to be made of all display functions. The other option, fitting the units into a single enclosure, also has an advantage: it results in a compact piece of equipment that is easy to carry around and connect. It is also the cheaper option, since a number of displays and enclosures may be omitted.

The choice between the above two options is entirely your own. Note, however, that each option is based on its own component set. This means that you first have to decide on an option, and only then start purchasing components. This will save you a lot of desoldering work later, in particular with the connectors.

This article instalment is the first of two that deals with the construction of the DiAV. As already mentioned, it will deal with the construction of the DiAV as separate modules. Part 3 of the article will tackle the construction as a single unit. Part 4 will concentrate mainly on the control software.

Dissolve unit construction

The dissolve unit described last month is built on a compact printed circuit board that allows the unit to be built into a relatively small case. The PCB is supplied inclusive of the system software (see page 110), and consists of six sub-PCBs, which have to be separated from one another before they are populated. The PCB artwork is shown in Figs. 15, 16 and 17. In view of the high track density and the high number of through contacts, it is not recommended to produce this PCB yourself. Hence, the component side and solder side track layouts are shown reduced to 50% in Figs. 16 and 17.

A breaking line is fraised between the three largest sub-PCBs. This line makes the sub-PCBs easier to separate. The three other boards with K14-K17, K20 and K21 on them are easily separated with a jig-saw. The small piece of PCB material left over after cutting the boards should not be thrown away as it has a function later.

The largest sub-PCB contains the control electronics, and may be assembled in the usual fashion by referring to the component overlay and the parts list. However, before you start soldering, you may have to cut off the PCB corners near T1 and IC16. This is only necessary if you use the enclosure mentioned in the parts list. To be able to run an initial check on the board, the ICs must not be fitted as yet. The same goes for connector K1. This has to do with the Centronics output, which requires the connections of K2 to be brought out via the small board that contains K20 and K21. At the side of K21, remove as much PCB material as possible to enable a flatcable connector for PCB mounting to be fitted (see Fig. 18). Next, fit K20 and K21 on this board (with a 10-cm long piece of flatcable). This construction is mounted on top of K1 as illustrated in Fig. 19. To be able to do this, however, first cut off a small piece of K1, as shown in Fig. 18. If this is not possible on your particular connector, the pins of K20 must be must be cut off flush with the PCB before soldering, so that nothing protrudes from the board underside after soldering. Alternatively, if you do not intend to use the ready-made front panels supplied through the Readers Services, the remaining piece of PCB material may be inserted between the stacked connectors. Note, however, that this neither allows the connector PCB to be fitted above the stacked connectors, nor in the case mentioned in the parts list. If you do not have sufficiently long M2.5 (2.5 mm dia.) bolts, drill out the mounting holes of the eject headers so that 3-mm bolts can be used instead.

The connector board that contains K9-K13 requires no further explanations. This board may be secured on to the main board with the aid of four 4-cm long PCB pillars (see introductory photograph and Fig. 26). To make sure that the enclosure can be closed with the top cover, the PCB pillars have to be reduced by about 2 mm. Also file a little material off connectors K11 and K12 to provide enough room for K1 and K20.

Mount all parts on the display board, except the LEDs. Note that the displays must be mounted on IC sockets. This is necessary to provide enough room for the LEDs behind the front panel. Before fitting the LEDs, drill and cut the front panel with the aid of the drilling template sup-

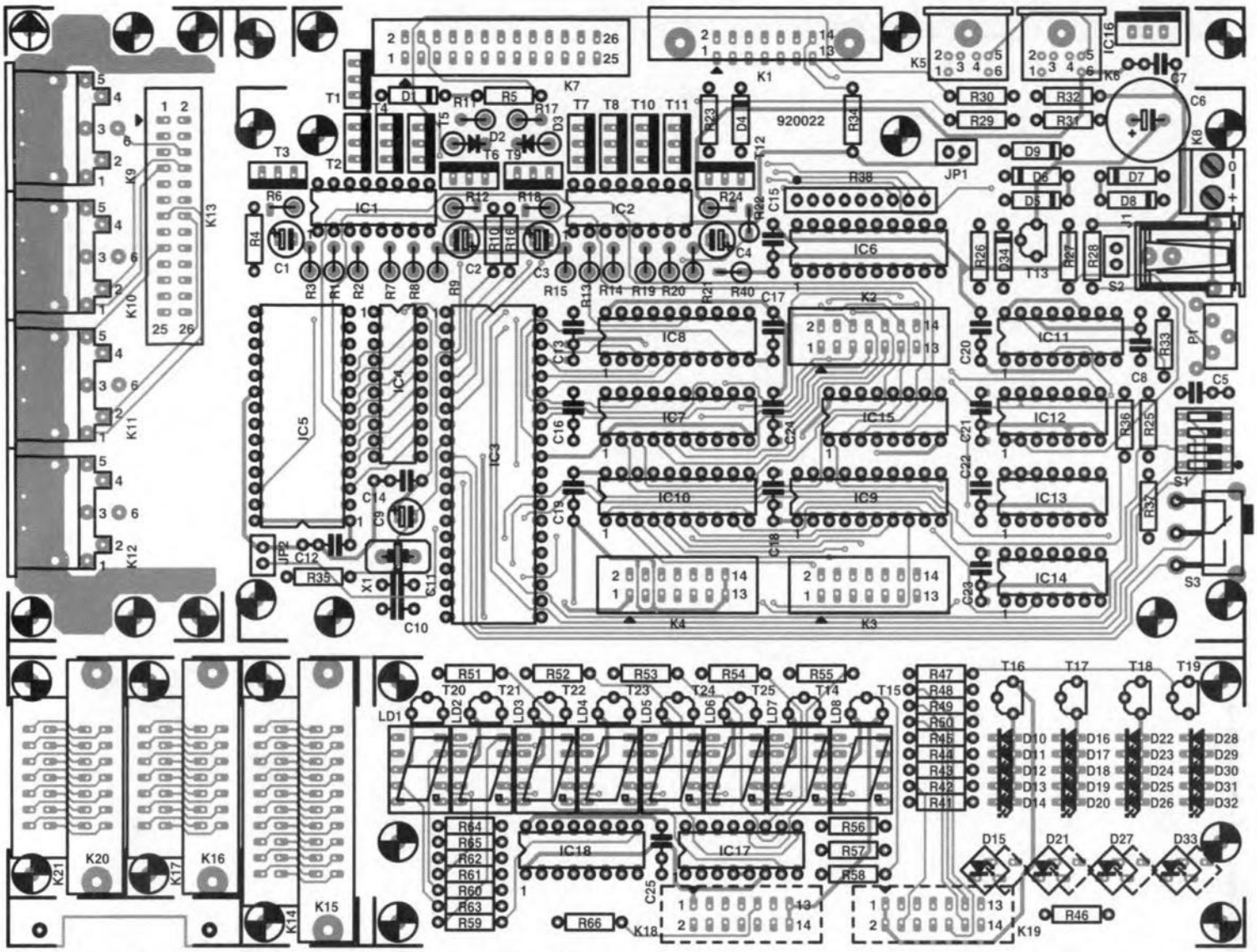


Fig. 15. Component overlay (size: 100%) of the dissolve unit PCB.

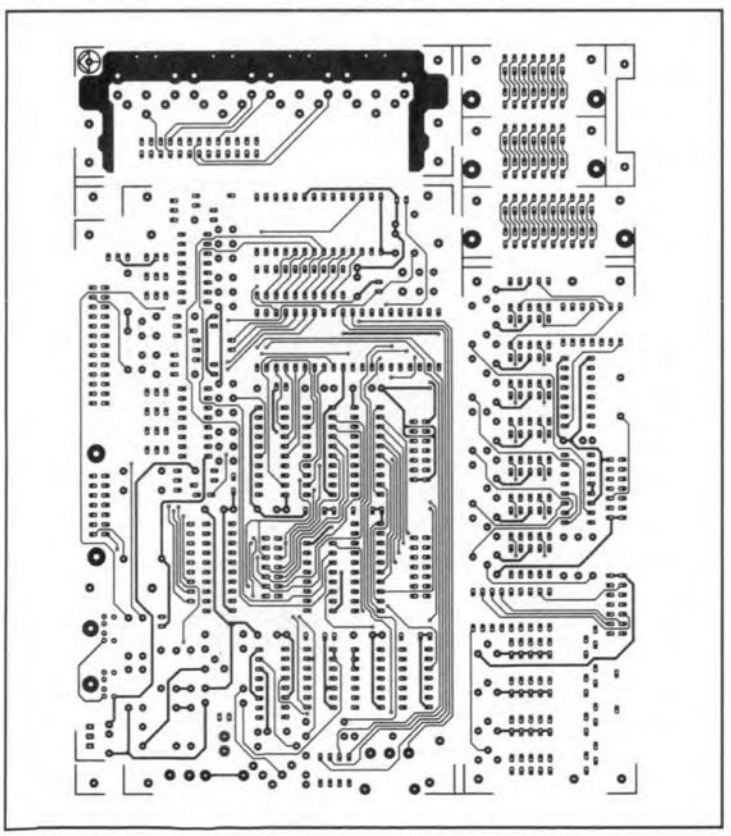


Fig. 16. Component side track layout (mirror image; reduced to 50%).

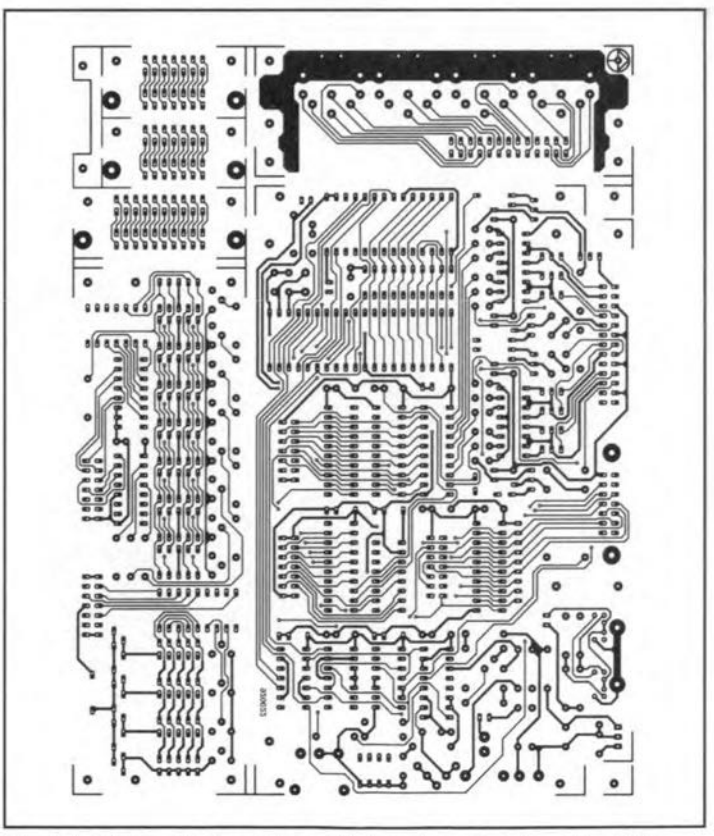


Fig. 17. Solder side track layout (mirror image; reduced to 50%).

COMPONENTS LIST

DISSOLVE UNIT MAIN BOARD

Resistors:

8	220Ω	R1;R2;R7;R8;R13;R14;R19;R20
8	47Ω	R3;R5;R9;R11;R15;R17;R21;R23
7	1kΩ	R4;R10;R16;R22;R33;R36;R37
6	10kΩ	R6;R12;R18;R24;R28;R34
2	2kΩ2	R25;R26
1	120kΩ	R27
2	330Ω	R29;R30
2	3kΩ3	R31;R32
1	47kΩ	R35
1	8-way 1kΩ SIL array	R38
1	100kΩ	R40
1	10kΩ SMA (for T13; see text)	
1	50kΩ preset H	P1

Capacitors:

4	10µF 16V radial	C1-C4
1	1nF	C5
1	1000µF 16V miniature radial	C6
14	100nF	C7;C12-C24
1	150nF	C8
1	4µF7 16V radial	C9
2	22pF	C10;C11

Semiconductors:

9	1N4001	D1-D9
1	1N4148	D34
8	BD679	T1;T2;T4;T5;T7;T8;T10;T11
4	BD140	T3;T6;T9;T12
1	BC547B	T13
2	CNY74-4	IC2;IC2
1	80C32-16	IC3
1	74HCT573	IC4
1	2764 EPROM (ESS6171; supplied with the PCB; see page 70)	IC5
4	74HCT574	IC6;IC8;IC9;IC10
1	74HCT541	IC7
1	74HCT123	IC11
1	74HCT32	IC12
1	74HCT74	IC13
1	74HCT00	IC14
1	74HCT139	IC15
1	7805	IC16

Miscellaneous:

2	14-way angled PCB header with eject latches	K1;K20
3	14-way box header	K2;K3;K4
2	6-way PCB mount mini-DIN socket	K5;K6
2	26-way box header	K7;K13
1	2-way 5-mm raster PCB terminal block	K8
4	6-way 240° PCB mount DIN socket	K9-K12
1	14-way IDC header for PCB mounting	K21
1	4-way angled DIP switch	S1
1	chassis mount SPST switch	S2
1	SPST PCB mount slide switch; angled pins	S3
1	16 MHz quartz crystal	X1
1	PCB mount mains adaptor socket (2.1 mm dia centre pin)	J1

10cm 14-way flatcable
30cm 26-way flatcable

1	14-way IDC socket	
2	26-way IDC socket	
1	25-way male IDC style sub-D connector	
1	12VAC @1A (min.) mains adaptor	
1	Elbox RE-2 enclosure (Retex)*	
4	PCB pillar; length 4cm	
1	Printed circuit board and software order code 920022 (see page 110)	
1	Front panel foil 920022-F1 (see page 110)	
1	Rear panel foil 920022-F2 (see page 110)	

REMOTE CONTROL

3	push-button with change-over contact	
1	6-way mini-DIN plug	

approx. 2m 3-wire cable

DISPLAY BOARD

Resistors:

14	220Ω	R41-R46;R59-R66
12	2kΩ2	R47-R58

Capacitors:

1	100nF	C25

Semiconductors:

20	LED; red; rectangular; face 5×2.5mm	D10-D14;D16-D20;D22-D26;D28-D32
4	LED; red; square; face 5×5mm	D15;D21;D27;D33
4	BC557B	T16-T19
7	BC547B	T14;T15;T20-T25
1	74HC4543	IC18
1	74HCT238	IC17
8	HD1107O (orange)	LD1-LD8

Miscellaneous:

2	14-way PCB mount IDC header	K18;K19
2	10-cm 14-way flatcable	
2	14-way IDC socket	

*Retex, Jerusalén 10, 08902 Hospitalet, Barcelona, Spain. Tel. +34 3 335 5562. Fax +34 3 335 7468.
Distributor: Boss Industrial Mouldings Ltd., James Carter Road, Mildenhall, Suffolk IP28 7BD. Tel. (0638) 716101.

plied as a 1:1 copy with the front panel foil. The drilling template is also shown (reduced) in Fig. 21. Stick the template on to the aluminium front panel, and mark all corner points with a centre punch. Next, mark out the clearances with the aid of a ruler and a scribe. The Retex case has a very 'soft' aluminium front panel, which is easy to cut and finish with a jig saw and a set of small files.

After making the holes, secure the display board to the front panel using PCB pillars and bolts with countersunk heads. The distance between the display board and the front panel should be tuned such that the display fronts are flush with the front panel. Next, insert the LEDs into the holes, adjust their positions, and solder. Fit two 10-cm long pieces of flatcable to K18 and K19. These cables are later connected to K4 and K3 respectively via appropriate connectors. Mind you: K18 and

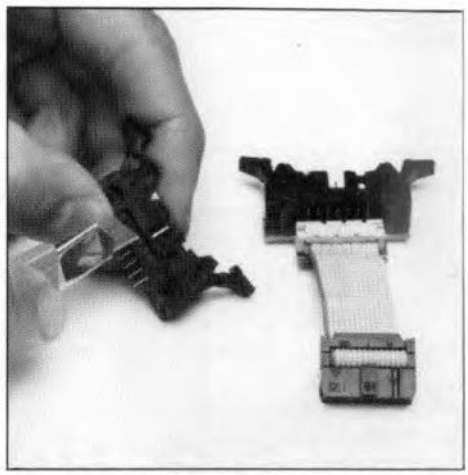


Fig. 18. Illustrating how K20 and K21 and the flatcable are combined on the small connector board. Before fitting this board and K1 on to the main board, a small part has to be cut off K1.

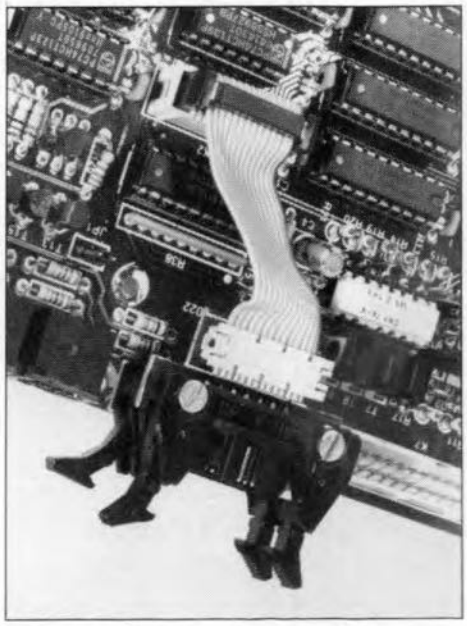


Fig. 19. Seen here are connectors K1 and K20 fitted neatly on to the main board.

K19 must be fitted at the solder side of the board, as indicated by the dashed outlines on the component overlay.

Before sticking the foil on to the front panel, darken the area around the LED holes (at the inside of the foil!) using a waterproof black marker pen. This is necessary because the front panel foil is a little too translucent, and its design is such that only sections of the LED faces are really visible at the outside. All clear? Then carefully stick on the front panel foil.

Connection and test

Before we can run our first test on the dissolve unit, it is necessary to make a small hardware modification. During the development of the system it appeared that some mains adaptors cause problems with the zero crossing detector. To be more precise: the mains zero crossing instants were not sufficiently accurately defined. This problem was traced down to a floating base of T13 during the zero crossing. The remedy is simple: fit a 10-kΩ resistor between the base and the emitter of T13 (an SMA resistor fits exactly between the base and emitter solder spots on the board).

To be able to hook up the connector board, fit two IDC (insulation displacement connector) sockets and one male sub-D25 connector on to a length of flatcable. The dimensions of this cable are shown below in Fig. 22, and the practical appearance to the right in Fig. 23. The cable at the left in Fig. 23 and the dimensions shown at the top in Fig. 22 are applicable if the DiAV system is fitted in a single enclosure (further details in Part 3). The D25 connector may be used where the projectors are not close to the dissolve unit. In that case, one cable is sufficient to hook up all four projectors. The connections made by this cable are shown in Fig. 24. One of the headers is connected to K7, the other to K13. Note: pin 1 goes to pin 1 (the headers and sockets are polarized, and have a 'pin 1' mark in the form of an arrow or a dot).

Next, it is time to fit the first three ICs on the main board: IC1, IC2 and IC16. Connect the mains adaptor to the circuit, and close switch S2. Check the presence of the supply voltage. If this is okay, switch off, open S2, and connect projector 1 to K9. Switch on again and check the supply voltage. If this is still okay, you are ready to test the projector connections. This is done by screwing a wire into K8, at the ground side. The other end of the wire is used as a probe to test the carrier control input of projector 1. Touch pin 18 or pin 19 of the IC socket in position IC8 with the wire end. The projector should respond by doing a slide change. Touch pin 3 of the IC socket in position IC3, whereupon the lamp should light.

If this works so far, the other projector connections may be tested by hooking them up to K10, K11 and K12, and connect-

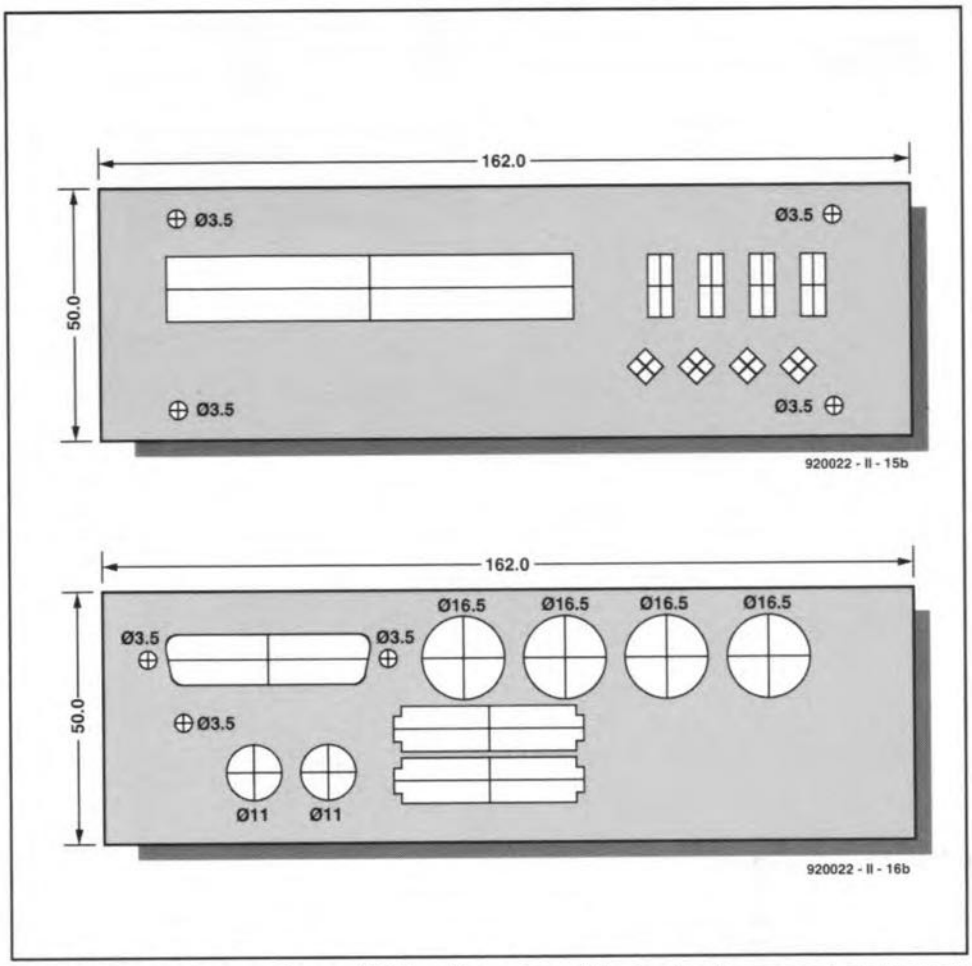


Fig. 20. Keep to these cutting and drilling dimensions of the front and rear panel, and you are able to use the ready-made self-adhesive front panel foils supplied through the Readers Services (see page 110).

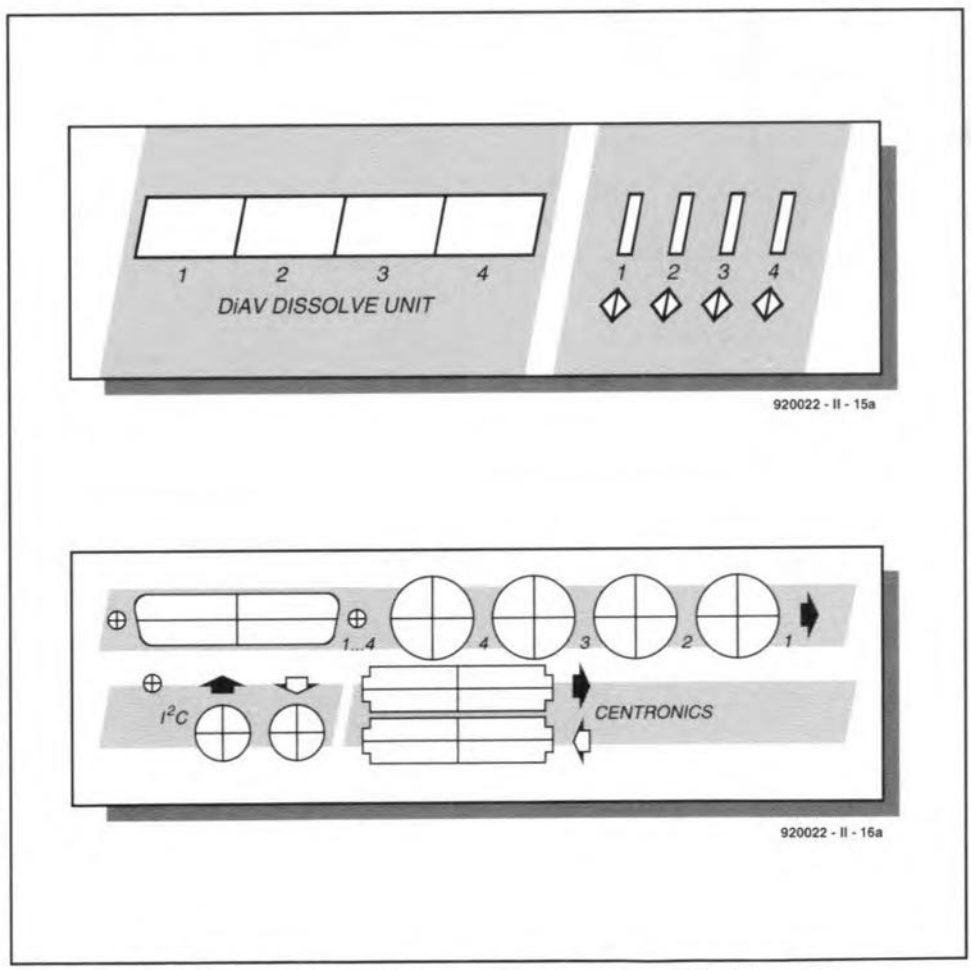


Fig. 21. Front panel and rear panel foil layouts (shown at about 60% of true size).

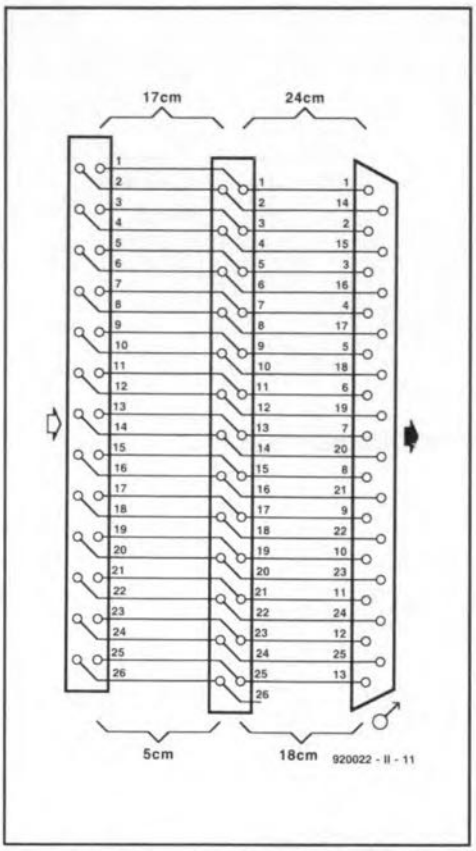


Fig. 22. Basic connections of the two IDC sockets and the D25 connector on the flatcable. The cable lengths given at the top and the bottom of the diagram apply to 'single enclosure' and 'individual enclosure' construction respectively.

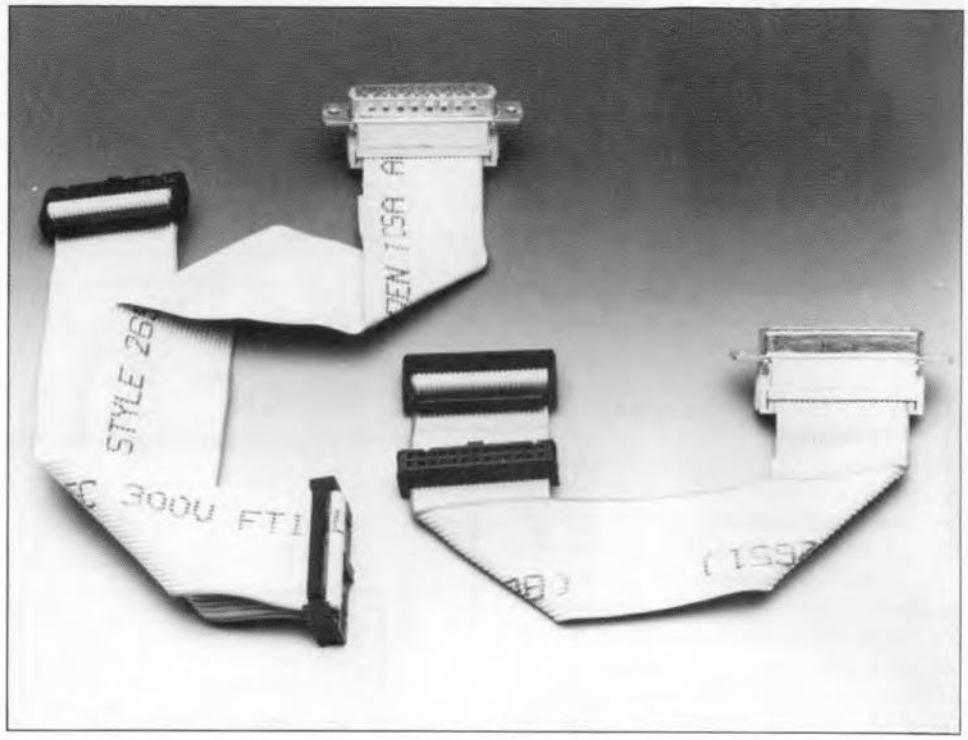


Fig. 23. Flatcables for the 'single enclosure' (left) and 'individual enclosures' (right) options of the DiAV system.

COMPONENTS LIST

TRIAC MODULE

1 TIC263 plus insulation material
1 12-way male RTG-22 plug
1 6-way 240° DIN socket
1 Heat-sink SK182/37.5SA
1 Diecast case 91×38×25mm; e.g. Hammond 1590A

6-TO-6-WAY CONNECTING CABLE

2 6-way 240° DIN plug
Approx. 75cm long piece of 6-way cable

6-TO-10-WAY CONNECTING CABLE

1 6-way 240° DIN plug
1 10-way DIN plug (e.g. Hirschmann Type MIS100, order code 931 876-117)
Approx. 75cm long piece of 6-way cable

ing the associated pins on IC socket IC8 (pins 12-17) and IC3 (pins 4, 5 and 6) to ground. If these tests check out, fit the remaining components on to the main board, and connect the display.

After switching on, each display pair should indicate '01'. This indicates a correct power-up, and that zero-crossings have been detected. If no alternating voltage is applied, the decimal points on the displays will flash to indicate the error condition. If this happens, check that you have connected an alternating voltage source. Remember, the lamp dimmer circuitry can not function without zero crossings, even though the lamp intensity display gives a normal indication. This condition may be simulated on a correctly functioning board by shorting out D9.

Switch S3 allows you to choose between two display intensity levels. The lower level ensures that the display is dimmed such that it is visible, but not obtrusive, in the dark.

Assuming that everything checks out so far, the minimum projector lamp intensity may be set by adjusting preset P1. The lamp filaments should just glow, without producing a visible image on the projector screen. If this can not be achieved, decrease the value of R27 to 68 kΩ. Do not forget to select between 'one-button' (JP1 closed) and 'two-button' (JP1 open) projector control.

Next, connect the remote control as shown in Fig. 25. The three switches are wired such that they keep the two microcontroller inputs 'low' when they are not pressed. This allows the system to detect whether the interface is controlled via the Centronics input or manually. In the latter case, the number of projectors selected equals that set on switch block S1 (switches S1-3 and S1-4). The lamp intensity displays of the non-used projectors are automatically switched off, which allows the number of used projectors to be seen at a glance.

When the 'forward' button (S4) is pressed, the first projector will be enabled. The next button action will result in a fade from projector 1 to projector 2. Next, projector 1 will do one forward change. In this way, all connected projectors may be controlled one after another.

On pressing the 'reverse' button, the previous projector will first do a reverse change (carrier one position backwards). Next, a fade is done to the previous projector. This simple sequential control allows the dissolve unit to be used on its own,

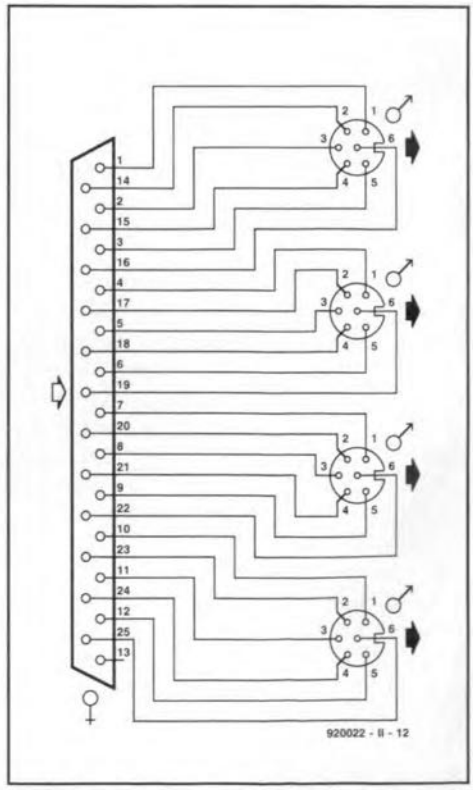


Fig. 24. The 25-way male sub-D connector allows all projector connections to be joined into one cable.

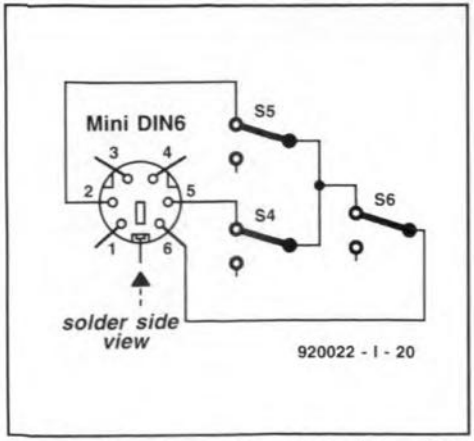


Fig. 25. Manual control: connections of the three switches to the mini-DIN plug inserted into the I2C control input.

with two to four projectors, where the slides are distributed over the projectors. Switch S6 serves to set the dissolve (fade out/fade in) time. Pressing it once causes a LED bar to appear on all four lamp indicators. The LED bar indication is proportional to the dissolve time. The 'forward' and 'reverse' button then serve to increase and decrease the dissolve time respectively, in steps of one second. The LED bar will change accordingly. Pressing S4 again takes you back to the projector control mode.

Provision has been made for the projector illumination areas (on the screen) to be matched. All four projectors light when the 'forward' or 'reverse' button is pressed when the unit is switched on. This allows you to position the projectors such that their light beams overlap exactly on the screen. This mode is left by pressing the 'forward' or 'reverse' button again, whereupon the system can be used as described above.

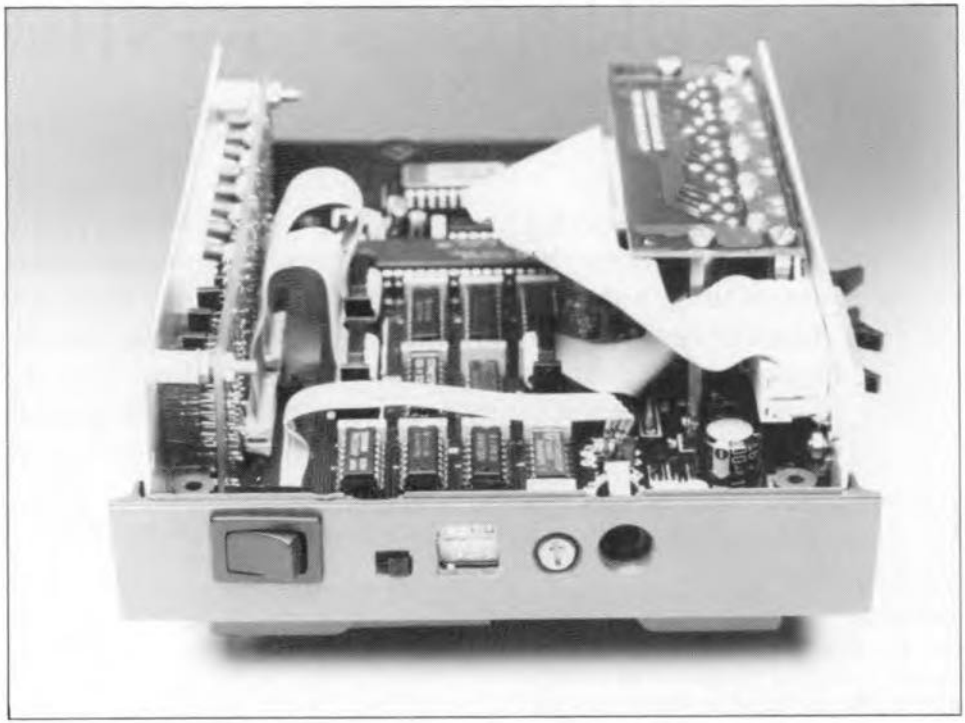


Fig. 26. The side panel of the Retex enclosure has holes for the mains adaptor plug, the switches and the potentiometer.

The case

If everything works to your satisfaction, the dissolve unit may be fitted into its enclosure. Self-adhesive foils are available for the front as well as the rear panel of the Retex enclosure. The rear panel layout is shown reduced in Fig. 21. These foils give the unit a professional and attractive finish. There is one point to note about the rear panel and the rear panel foil: in some cases, the hole for the mini-DIN plug may have to be made larger than indicated by the drilling template. This is necessary because the plug body has to touch the socket to make proper contact.

The right-hand side panel of the Retex case is drilled and filed to allow S1, S2, S3 and P1 to be operated. Also note the hole required to insert the mains adaptor plug (see Fig. 26). The voltage regulator is bolted on to the rear panel. If you use another enclosure than the one we recommend, remember that the metal part of IC16 and the sides of the I^2C plugs are connected to ground. To prevent a short circuit with the alternating voltage, the mains adaptor input socket must be an insulated type if it is fitted on the same panel as the regulator. ❑

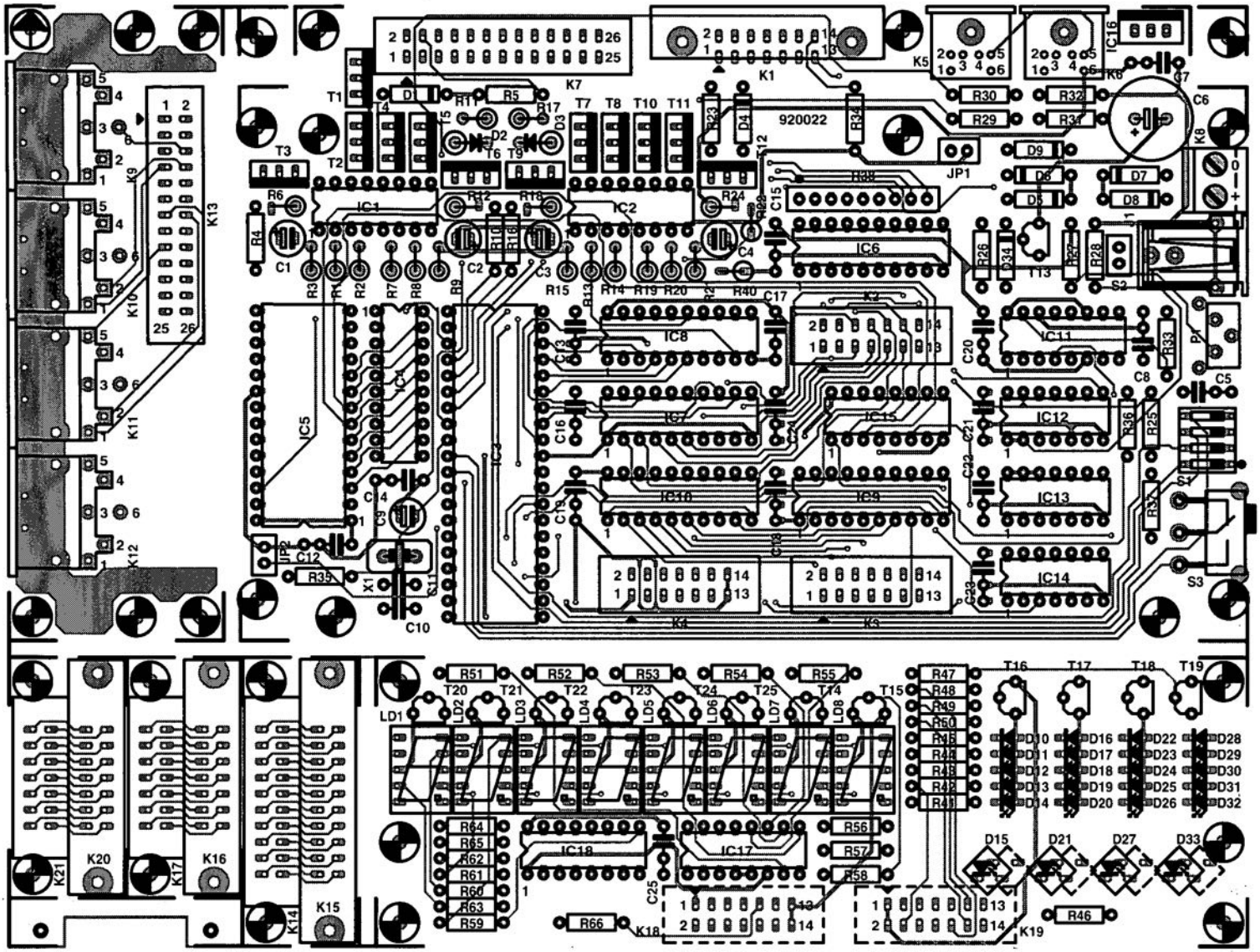


Fig. 15. Component overlay (size: 100%) of the dissolve unit PCB.

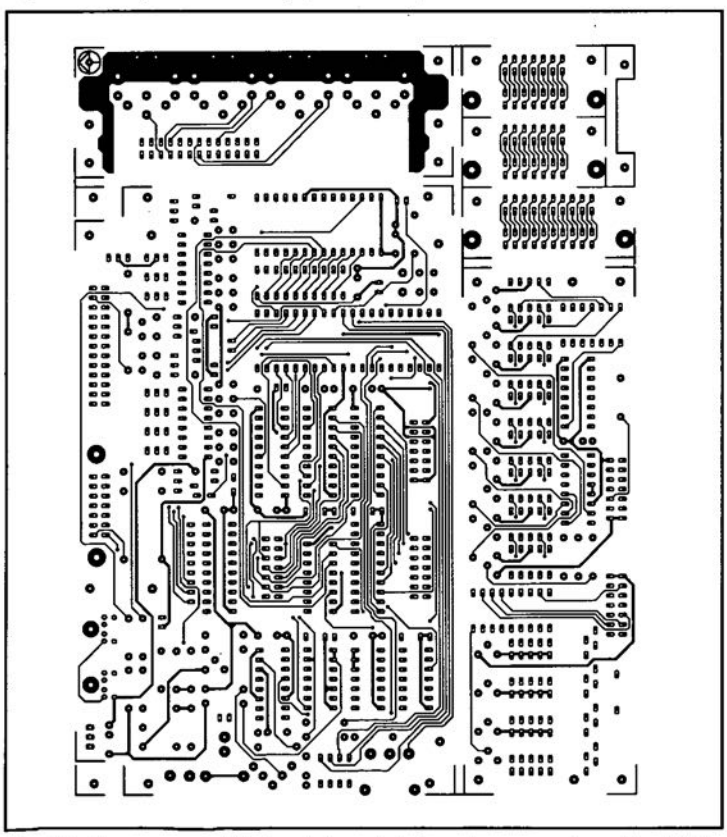


Fig. 16. Component side track layout (mirror image; reduced to 50%).

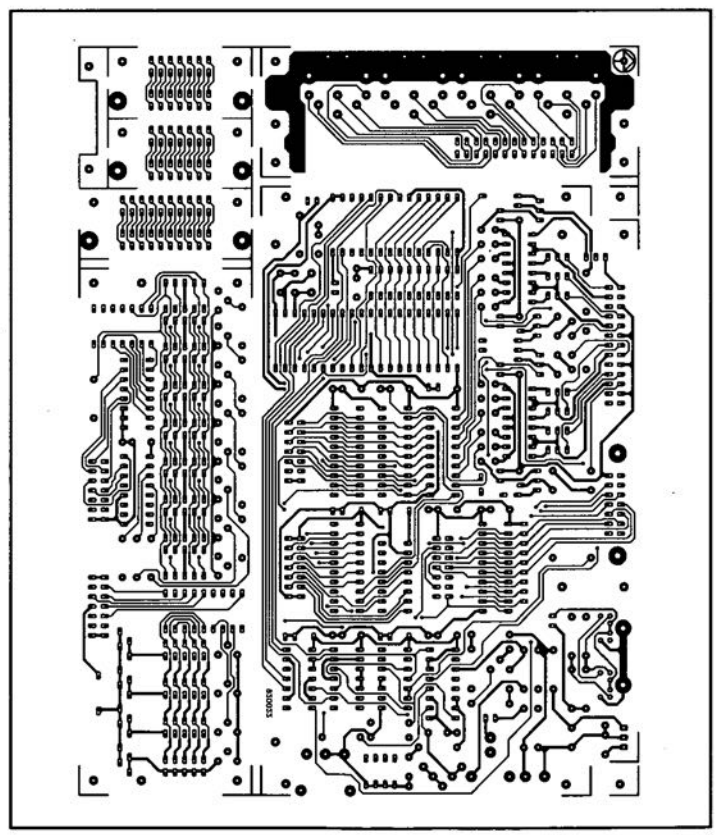


Fig. 17. Solder side track layout (mirror image; reduced to 50%).

UNBLOCKING THE PUMP

By Bryan Hart, BSc, C.Eng., MIEE

Although the pump circuit, in one or other of its many guises, has been used in electronics for some fifty years, textbook explanations of its operation tend to be either sketchy and qualitative or overly mathematical. This article aims to remove the confusion surrounding the circuit by concentrating on its physical operating mechanisms and to show that algebraic analysis can be replaced by a simple, but novel, graphical procedure.

In use in electronics for over fiffty years, the pump circuits has appeared in a wide variety of applications that include counting/frequency division; frequency-voltage conversion; frequency-sensitive switch design; demodulation; and staircase voltage generation for display systems. Unfortunately, textbook treatment of its operation tend to be either sketchy and qualitative or overly mathematical. Budding engineers studying the circuit for the first time might be forgiven the resulting mental blockage

The principal aims of this article are to remove that confusion by concentrating on physical operating mechanisms and to show that algebraic analysis can be replaced by a simple, but novel, graphical procedure. This is unusual in showing the output voltage as a function of a charge increment transferred during an input pulse. The result is an easily constructed '$U_o/\Delta Q$ lattice plot' from which the output waveform can be sketched by inspection.

Pump circuit modelling

A basic form of the pump circuit is shown in Fig. 1. For reasons that will become apparent later, it is sometimes more colourfully known as a 'cup-and-bucket' circuit.

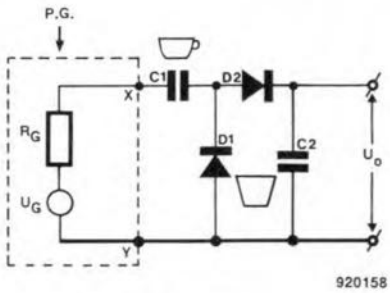


Fig. 1. Basic diode pump circuit.

In modelling the circuit, it is desirable first to idealize the properties of the components used. Then, when the general operating principles are understood, the consequences of using non-ideal components are more easily appreciated. Thus, C_1 and C_2 have no defects such as leakage resistance that require parasitic elements to model them.

The pulse generator, P.G., has a constant output resistance, R_G and produces an output waveform as shown in Fig. 2a that is a train of rectangular pulses, P_1, P_2, ...P_r, ...P_n, having zero transition times, pulse duration t_d, pulse recurrence time T, and open-circuit pulse amplitude E.

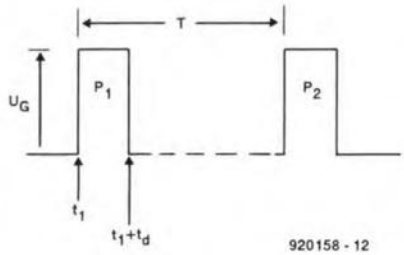


Fig. 2a. Assumed input waveform.

The P.G. is modelled in Fig. 2b by an ideal switch Sw_G and battery E. Initially, Sw_G is at position 'a' and between pulses, and at 'b' when the pulses are present. The time taken to switch from 'a' to 'b' and vice versa is taken as zero.

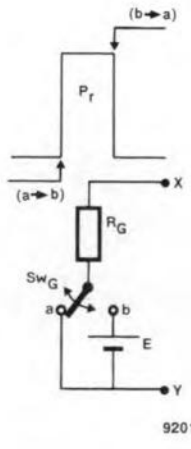


Fig. 2b. Equivalent representation by a mechanical switch.

Diodes D_1 and D_2 are also modelled by ideal switches as shown in Fig. 3. In the composite circuit model in Fig. 4, the switches Sw_G, Sw_1 and Sw_2 are all ganged together. The overall effect produced in the circuit by the repeated movement backward and forward of the moving parts of the switches is analogous to that produced in a hydraulic system by a mechanically operated piston pump displacing a quantity of fluid, so the adjective 'pump' used to describe the circuit is quite appropriate. In our case, of course, the 'fluid pumped' is electric charge.

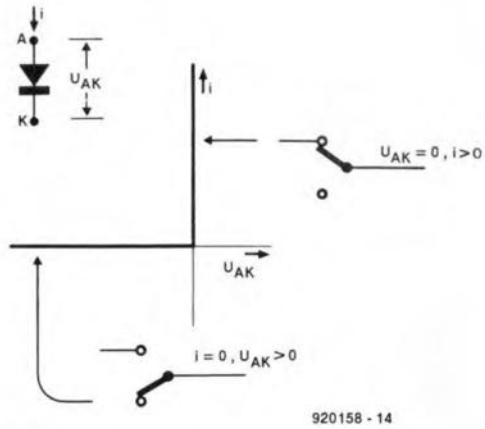


Fig. 3. Idealized electrical description of D_1 and D_2.

Circuit operation and graphical development

Prior to the arrival of the first pulse, P_1, capacitors C_1 and C_2 in Fig. 4 are both uncharged. This condition, while not obvious for C_2, is guaranteed by a voltage level sensing circuit connected across it. Since that piece of circuitry is not relevant at present, a brief discussion of it is left to the end of the article.

After the arrival of P_1 ('the first stroke of the pump'), D_1 cuts off, D_2 switches on and the reduced equivalent circuit is shown in Fig. 5a. This is a single time constant switch-

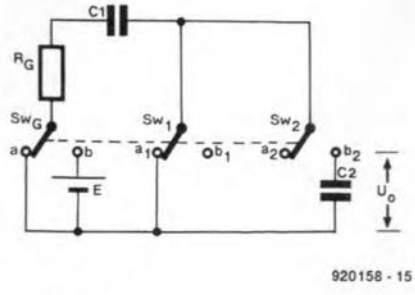


Fig. 4. Modelling the pump with switches.

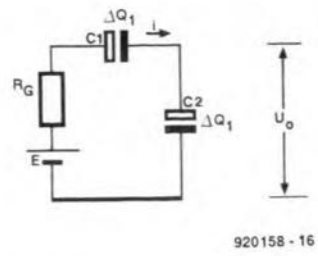


Fig. 5a. Equivalent circuit during P_1.

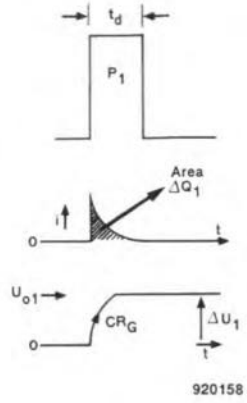


Fig. 5b. Circuit response to P_1 for $t_d>5CR_G$ ($C=C_1C_2/(C_1+C_2)$).

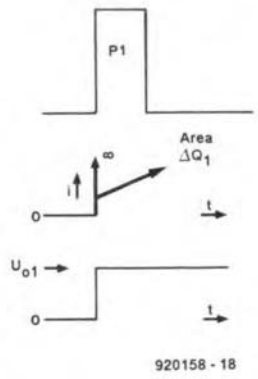


Fig. 5c. Theoretical response for $R_G=0$.

ing circuit, the time constant being the product CR_G. In this, $C=C_1C_2/(C_1+C_2)$ and is the effective capacitance of C_1 and C_2 in series.

On the leading edge of P_1, the whole of the input voltage, E, appears acorss R_G because C_1 and C_2 are initially uncharged and the potential differences across their plates cannot change instantaneously. The initial charging current is therefore E/R_G and it decays exponentially to zero as C_1 and C_2 are charged. The charging current causes an equal increment of charge to be deposited on the plates of both capacitors.

The time elapsing between the 10% and 90% output voltage levels is $2.2CR_G$ and, for all practical purposes, the charging process is taken as complete in a time interval $5CR_G$. Let ΔQ_1 be the charge increment transferred from E to C_1 and C_2 during pulse P_1. Provided $t_d>5CR_G$, the case shown in Fig. 5b, we can write

$$\Delta Q_1=CE. \qquad [1]$$

Note that the symbol Δ, rather than δ, is employed because the change is not necessarily small.

Equation [1] deserves a further brief discussion. Subject to the condition placed on CR_G, it means that ΔQ_1 is independent of R_G. The reason is that by the time the trailing edge of P_1 appears the potential difference across R_G is zero. Hence, the full applied e.m.f. E appears across the equivalent capacitor C.

The output voltage, U_{o1} when P_1 has passed, and the first output 'step' ΔU_1 are given by

$$U_{o1}=\Delta U_1=\Delta Q/C_2=C_1E/(C_1+C_2). \qquad [2]$$

The condition $t_d>5CR_G$, which we will assume to be valid from now on, is easily met in practice. Thus, if $R_G=50\Omega$ (a typical value) and $C=0.1\,\mu F$, the condition is $t_d>25\,\mu s$.

Figure 5c corresponds to the case $R_G=0$, which is implicit in some textbook discussions. However, it is purely an abstraction. It requires an understanding of the more difficult mathematical concept of a current impulse of infinite amplitude and zero duration, but nevertheless finite area. that dumps a charge ΔQ_1 on C_1 and C_2 in zero time. It is best to regard the situation shown in Fig. 5c as the theoretical limit case of what would happen in Fig. 5b if R_G were made progressively smaller.

A related method of finding step amplitude leads on to a graphical procedure that is best described below. The charge transferred from E to C_1 during P_1 is $\Delta Q_1=C_1(E-U_{o1})$; that transferred to C_2 is, of course, the same and is given by $\Delta Q_2=C_2\Delta U_{o1}$.

Equating these two expressions for ΔQ_1 again produces eq. [2].The same result is also obtained from a '$U_o/\Delta Q$ plot'. On this, lines are drawn as if C_1 were part of a voltage source with e.m.f. E, and C_2 were the load. To see how the plot arises, refer back to Fig. 5a.

Taking into account voltage drops at the end of P_1, the 'source characteristic for P_1', *s.c.*‹1› for short, of E and C_1 is

$$U_o=E-(\Delta Q/C_1). \qquad [3]$$

Similarly, the 'load characteristic' for P_1, *l.c.*‹1›, of C_2 is

$$U_o=(\Delta Q/C_2). \qquad [4]$$

In these two expressions, the number subscripts for U_o and ΔQ have been omitted because these quantities are now regarded as variables whose values are to be found.

Consider, now, the $U_o/\Delta Q$ plot of Fig. 6, where *s.c.*‹1› is a straight line with slope $-(1/C_1)$ that passes through the axes points $D_0(U_o=E)$ and $A_0(\Delta Q=C_1E)$; *l.c.*‹1› is a straight line with slope $+(1/C_2)$ that passes through the origin and which is most easily plotted by locating a convenient point on it other than the origin. For C_2 expressed in µF, a suitable point is $U_o=1$ V, $\Delta Q=(C_2\times1)\,\mu C$.

The intersection point, A_1, of *s.c.*‹1› and *l.c.*‹1› occurs where $\Delta Q(=\Delta Q_1)$ is the same charge increment transferred to both capacitors. $U_{o1}(=\Delta U_1)$ can be obtained by inspection.

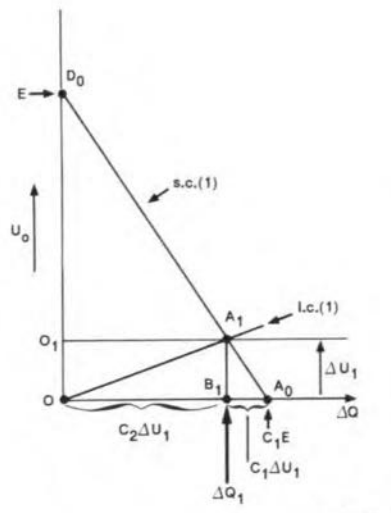


Fig. 6. A '$U_o/\Delta Q$ plot' for finding ΔQ_1 and ΔU_1 at the end of P_1 Bold lines show source and load characteristics.

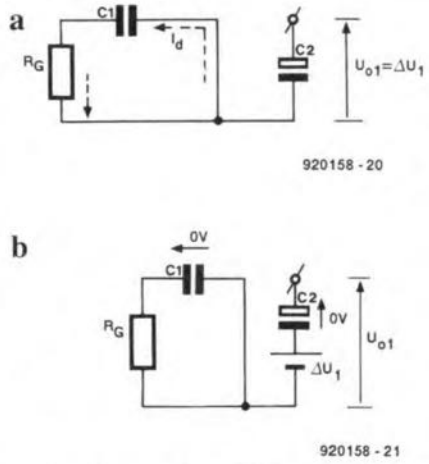


Fig. 7. Circuit conditions after P_1 and before P_2: (a) C_1 discharging – i_d=discharge current; (b) C discharged – $i_d=0$.

At the end of pulse P_1, D_2 cuts off and D_1 switches on. The charge on C_2 remains at ΔQ_1, but that on C_1 decays to zero with time constant C_1R_G—see Fig. 7a. Since this decay requires a time interval $5C_1R_G$ to complete, a second condition placed on t_d is $(t_d+5C_1R_G)<T$.

Figure 7b shows the condition when C_1 is fully discharged and before the arrival of P_2. The charged capacitor C_2 is now replaced by its equivalent, an uncharged capacitor in series with a battery of e.m.f. ΔU_1.

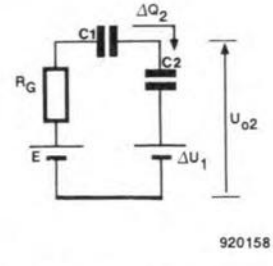


Fig. 8. Charge transfer during P_2. Compare with Fig. 5a.

From Fig. 8, which shows the circuit applicable for charge transfer during P_2:

$$U_0=E-(\Delta Q/C_1), \quad [5]$$

and

$$U_0=(\Delta Q/C_2)+\Delta U_1. \quad [6]$$

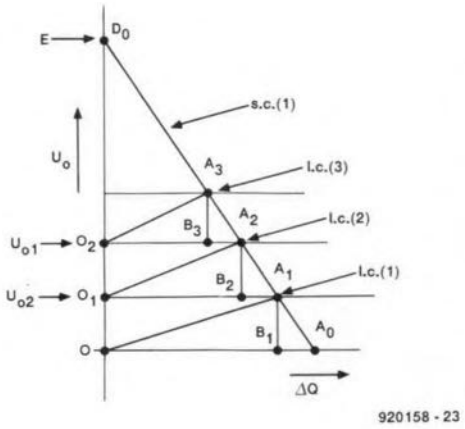


Fig. 9a. A $U_0/\Delta Q$ lattice plot for the first three pulses, P_1, P_2, P_3.

As with eq. [3] and [4], and for the same reason, the number subscripts have been omitted from the variables U_0 and ΔQ.

Equation [5] represents *s.c.*‹2›, the source characteristic for P_2. This is the same as *s.c.*‹1›, because C_1 is completely discharged between input pulses.

Equation [6] describes *l.c.*‹2›; this is parallel to *l.c.*‹1›, but has a U_0 axis intercept ΔU_1.

On the $U_0/\Delta Q$ plot of Fig. 9a, intersection point A_2 gives ΔQ_2, U_{02}, and hence ΔU_2.

The plotting procedure for further pulses, P_3 ... and so on, now becomes clear. The source characteristic remains fixed: it is *s.c.*‹1›. However, there is a new load characteristic for each successive pulse. This is parallel to that for the preceding pulse, but is shifted vertically up the U_0 axis by an amount equal to the previous step. The overall result is an easily constructed 'lattice diagram". From it, the output waveform can be readily obtained by cross-plotting as in Fig. 9b.

In Fig. 10, $O_{(r-1)}A_r$ and $O_rA_{(r-1)}$ are the load characteristics respectively for P_r and $P_{(r+1)}$.

From the geometry of the figure,

$$U_{(r+1)}/\Delta U_r=C_2/(C_1+C_2)=K \text{ (say)}. \quad [7]$$

Thus, the amplitudes of the output steps form a geometrical progression. By inspection of the plot, the maximum value of U_0 is E, which is reached after an infinite number of input pulses.

We can look on C_1 as a cup, C_2 as a cylindrical bucket and E as a tank of water. Then, as far as the output is concerned, the operation of the diode pump is analogous to that of using the cup to scoop up water from the tank and dump it into the bucket. In the first scoop, the cup is full, but the next time round it is only a fraction K full; the third time, it is a fraction K^2 full, and so on. As a result, the water level rises up the inside of the bucket by decreasing amounts after each dumping.

Step equalization

In an instrumentation application, such as the display of the terminal characteristics of a semiconductor device on a 'Curve tracer', we normally require the output voltage steps in Fig. 9b to be equal. Using our water analogy, the 'cup' must be full for each dumping.

The graphical method described provides

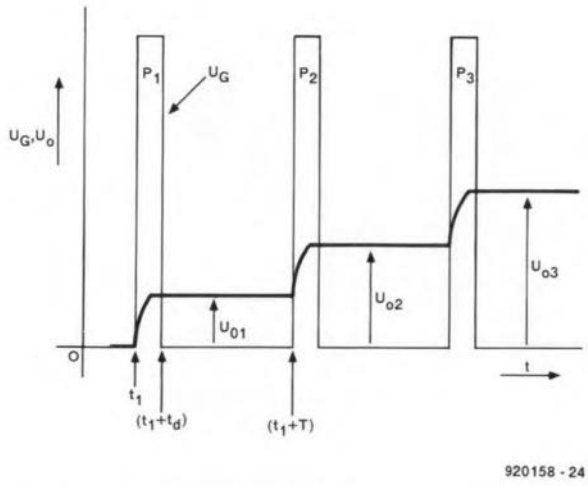


Fig. 9b. Cross-plot to show output waveform (bold line) and input waveform (faint line).

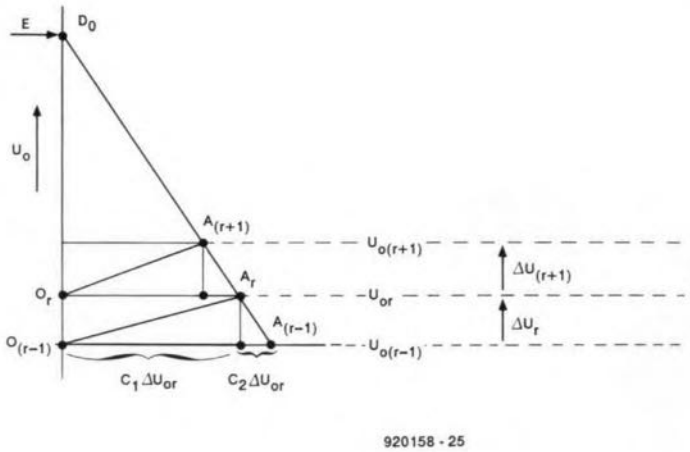


Fig. 10. Construction for finding the ratio of magnitudes of successive steps.

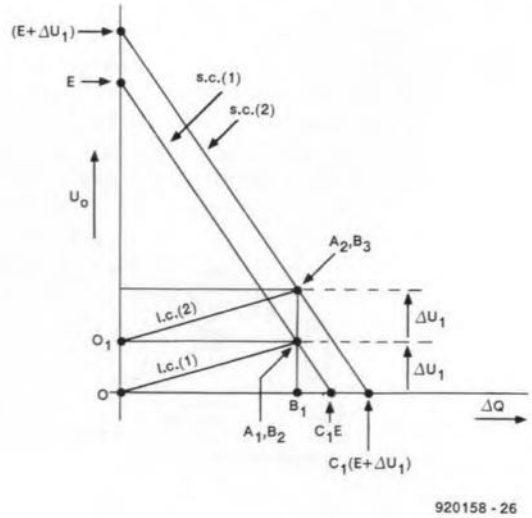


Fig. 11. Modification of the source characteristic for equal steps.

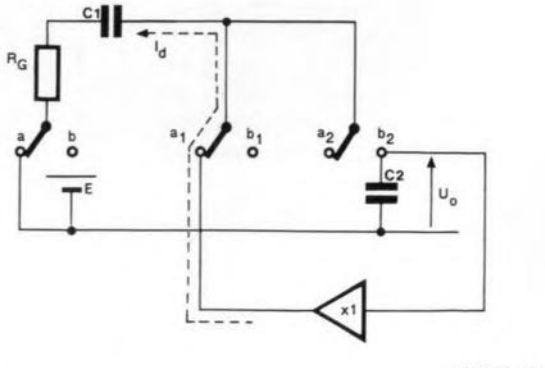


Fig. 12. Equivalent circuit interpreation of Fig. 11.

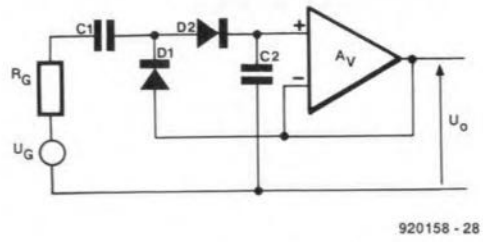


Fig. 13. 'Bootstrap' step equalization circuit.

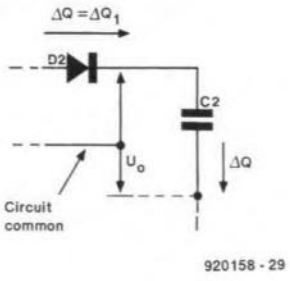


Fig. 14. Charge-transfer circuit requirement for fixed source characteristic and $\Delta Q_1 = C_1 E$.

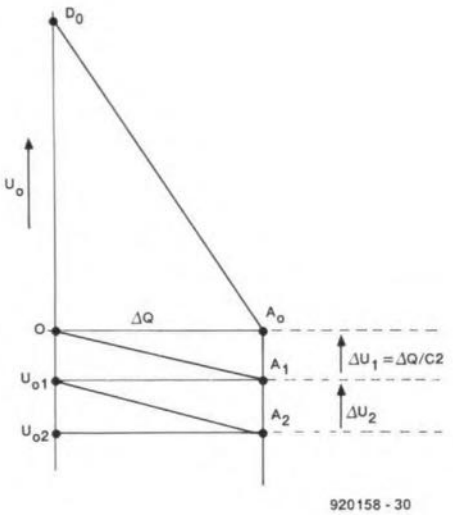


Fig. 15. $U_0/\Delta Q$ plot for Fig. 14.

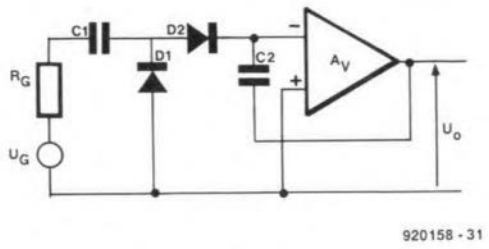


Fig. 16. 'Miller' step equalization scheme.

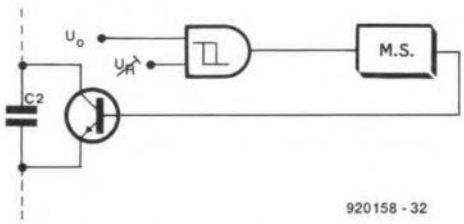


Fig. 17. Block schematic of reset circuit suitable for use with circuits of Fig. 1 and Fig. 13. Reverse the polarity of the transistor for use with Fig. 16.

a logical approach to the solution of the problem of how to modify the basic circuit to obtain the required result.

Looking at Fig. 9a, it follows that for equal steps the circuit must be changed so that the intersection points $A_1 \ldots A_r$ are equidistant from the U_0 axis. This is possible if the vertical shift in the load characteristic associated with a given pulse is matched by an equal vertical shift in the corresponding source characteristic. As indicated in Fig. 11, this means having *s.c.*‹2› located a distance ΔU_1 above *s.c.*‹1›, and so on. To produce this effect, C_1 must be charged up to the output voltage on the trailing edge of each pulse. Figure 12 shows the required equivalent circuit and Fig. 13 gives a hardware implementation, the 'bootstrap' scheme. In this, a high input-impedance opamp, A_v, is strapped as a voltage-follower, the low output impedance of which is suitable not only for driving an external load, but also for supplying the 'precharge' current, i_d, of C_1.

An alternative solution is to provide circuitry that keeps the source characteristic fixed but, at the same time, facilitates the extraction of the charge increments passing through D_2. This can be achieved if the cathode of D_2 is held at a constant potential, a sensible choice for which is 'circuit common '. The required circuit must, therefore, be able to perform the function indicated in Fig. 14. The related $U_0/\Delta Q$ plot is in Fig. 15. From the viewpoint of the load, the source characteristic $D_0 A_0$ appears to be a vertical line through A_0, corresponding to $\Delta Q = C_1 E$. The load characteristics are now required to have a slope $-(1/C_2)$.

An elegant hardware implementation of this is the 'Miller' scheme of Fig. 16. The cathode of D_2 is held at circuit-common potential by the feedback action of the inverting opamp configuration. Hence,

$$U_{01} = -\Delta U_1 = -(C_{1E}/C_2)$$

and

$$U_{0r} = -r\Delta U_1 = -r(C_1 E/C_2).$$

Reset circuit

As mentioned in the beginning, ancillary circuitry is required to set the initial conditions. In practice, this means the use of a reset arrangement such as that shown in block-schematic form in Fig. 17. A Schmitt trigger senses the output voltage and triggers a monostable, M.S., when a preset level, determined by U_r is reached. The output pulse of the monostable drives a discharge transistor connected across C_2.

Concluding comments

This article has described the development of a graphical procedure for sketching, rapidly, the output voltage waveform of a diode pump circuit driven by a train of rectangular input pulses. It may at first seem odd to be plotting voltage versus charge because it is so rarely done other than in, perhaps, early physics laboratory work with capacitors; nevertheless, nothing could more nearly describe the essential behaviour of a capacitor.

The plotting procedure itself does not necessarily require a knowledge of the small amount of algebra that has been included here to justify the method.

Acknowledegments

Thanks are due to Mr R H Pearson for incisive comments.

COMPRESSOR/LIMITER

The compressor is based on two series-connected attenuator networks, whose attenuation is controlled by light-dependent resistors (LDRs) that are illuminated by light-emitting diodes (LEDs).

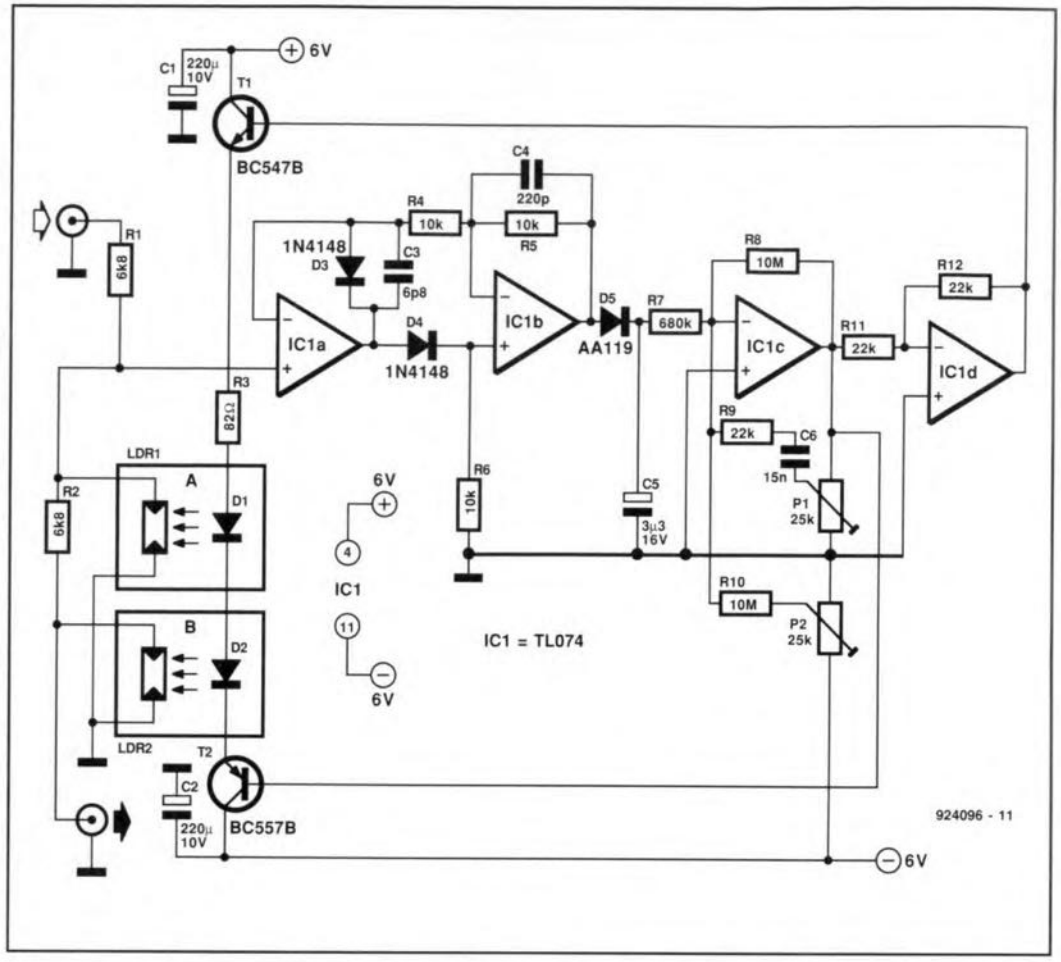
The input signal is applied to the non-inverting input of opamp IC_{1a} via R_1. Circuit IC_{1a}, in conjunction with D_3, D_4 and IC_{1b}, provides full-wave rectification of the signal. The resulting direct voltage is used to charge C_5 via D_5. The diode allows fast charging of the capacitor, which can discharge only via R_7.

Compression proper is provided by IC_{1c}. Depending on the setting of P_1 and P_2, the output voltage of IC_{1c} drops when the potential across C_5 reaches a certain value. This causes T_2 and, via IC_{1d}, T_1 to conduct, whereupon the LEDs light and the input signal is attenuated.

The attack time of the circuit is determined by the speed of the LDRs and the setting of P_2.

The amplification of IC_{1c} and the setting of P_1 determine the point at which voltage limiting commences. The output voltage is held constant when the input signal is above a certain level until the current through the LEDs reaches its maximum (about 40 mA).

The circuit as shown acts as a limiter; if the +ve input of IC_{1a} is connected to the output of the circuit, a standard compressor is obtained.



The circuit is able to process signals between about 10 mV r.m.s. and 2 V r.m.s. This range can be extended by adding one or more attenuator sections or by increasing the value of R_1 and R_2.

The LDR/LED combinations must be housed in a light-tight enclosure.

The current drawn by the circuit is determined largely by the LEDs and is 50 mA maximum.

(J. Barendrecht – 924096)

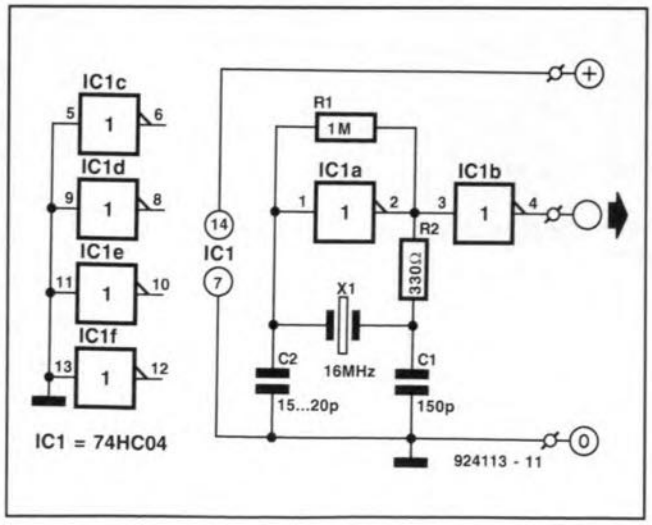
MINIATURE CRYSTAL OSCILLATOR

Nowadays, with the advent of SMD (surface mount design), it is possible to construct tiny circuits. In the case of crystal oscillators that may, however, not always be feasible because of the size of the crystal. Fortunately, Statek, a specialist crystal manufacturer, produces crystals measuring only 8×4×1 mm for SMD. Together with a single inverter and four passive components, such a crystal makes it possible to make a truly miniature, stable oscillator as shown.

The circuit works very well up to frequencies of 16 MHz if an HC-IC is used. With an HCT-IC, the maximum frequency was found to be about 8 MHz.

Finally, the circuit works perfectly all right with standard components as well.

(Statek Application – 924113)



VIDEO DEMODULATOR

The demodulator is based on a Type TDA8341 chip, which is the successor of the well-known Types TDA2541 and TDA3541. Apart from a demodulator, the chip contains an AGC (automatic gain control) section for tuners whose AGC voltage is directly proportional to the gain, and an AFC (automatic frequency control) facility. In the present design, the AFC is used merely as a tuning indicator.

The control range of the AGC is 67 dB. Because of internal supply regulation, the input sensitivity of the IC is 40 µV.

The IC provides a video signal at a level of 2.7 V at pin 12, from where it is passed to a Toko low-pass filter, Fl_1, which removes any residual carrier frequencies from the video signal. The filter has an attenuation of 6 dB over its pass-band. To obtain a standard video signal of 1 V_{pp} into 75 Ω, the filter may be followed by a video amplifier/buffer, for instance, a Type NE592. Note that the output impedance of the filter is 1 kΩ.

The AGC operating point is set with P_1. The AGC control voltage is taken from pin 4 via R_2. The level of the current through the AGC output is limited to about 10 mA. Network R_7-C_{11}-C_{12} forms an AGC detector, which also provides pulses for a sample & hold circuit. That circuit ensures that no video information is present in the AFC output.

The reservoir capacitor for the S&H circuit is C_6. If pin 6 is connected directly to earth, the AFC is disabled and the potential at pin 5 is then roughly half the supply voltage.

The AFC requires a synchronous demodulator with its own tuned circuit: L_2-C_8.

Because of (parasitic) capacitive coupling (C_9-C_{10}) with the tuned circuit for the reference amplifier, L_1-C_7, the skirt of the AFC characteristic becomes steeper. Since the AFC voltage here provides a tuning indication, a steep characteristic is not really desirable, so that C_9 and C_{10} must be kept as small as possible. The tuning indicator is formed by centre-zero meter M_1.

Tuning the reference circuit (to remove any residue of the carrier) is tricky and can really be done properly only if an r.f. analyser or modulated r.f. generator and frequency meter are available. If crystal-controlled PLL (phase-locked loop) tuning is used, however, the adjustment can be carried out without this test equipment.

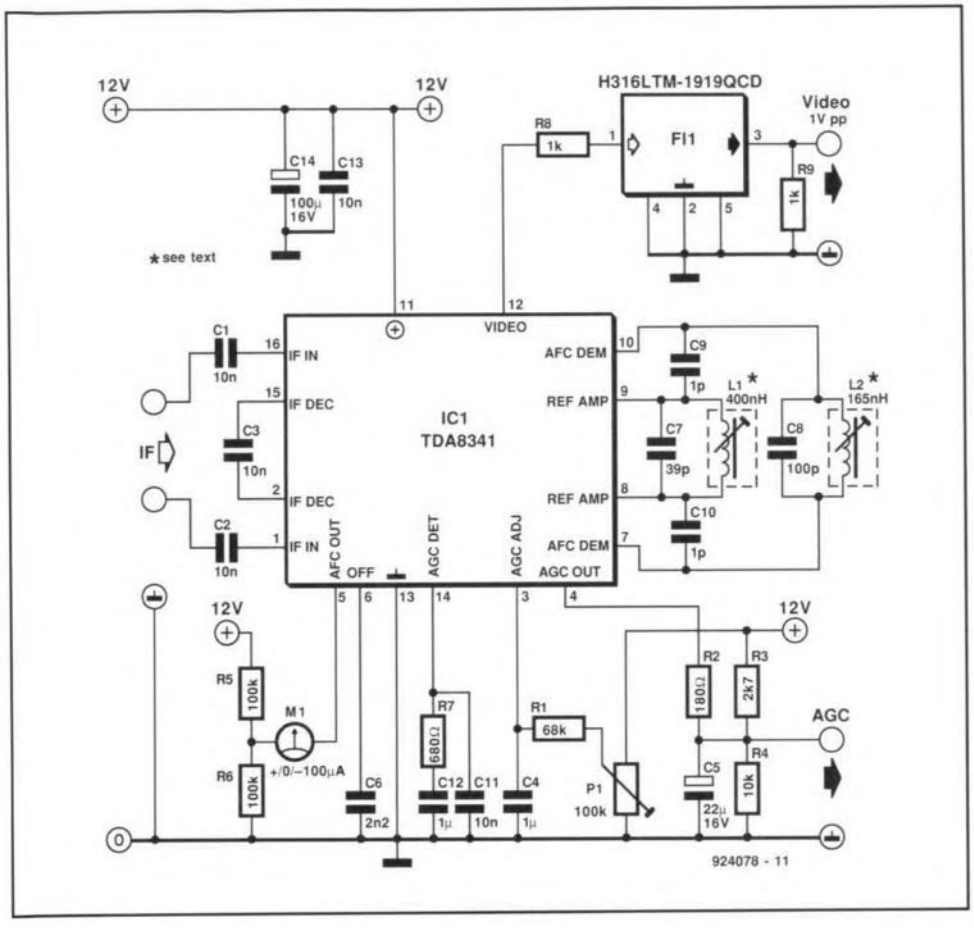
Once the channel tuning and the adjustment of L_1-C_7 are correct, the AFC circuit, L_2-C_8, may be tuned for centre-zero reading of the meter (half supply voltage at the AFC output). Resistors R_5 and R_6 hold the other terminal of M_1 at half the supply voltage and at the same time limit the current through the meter to about 100 µA.

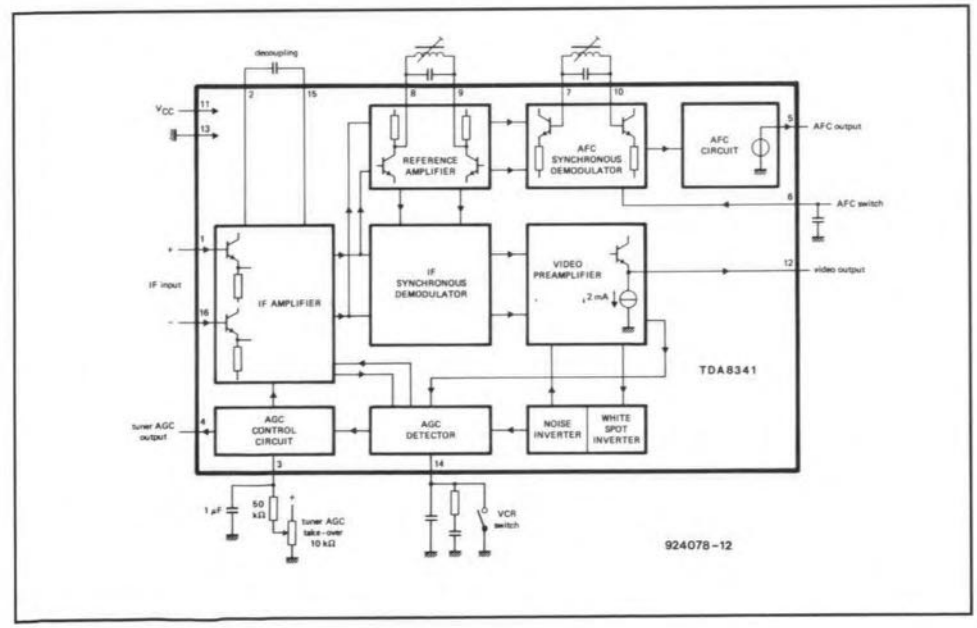
Because of the circuit layout, there may be cross-talk between the video output and the i.f. input. This may, however, be cured by connecting a 6.8 µH choke in series with pin 12 (as close to the IC as feasible).

The demodulator draws a current of about 45 mA.

The input signal may be taken from a SAW (surface acoustic wave) filter, which is readily available nowadays. Most tuners—although this must be checked—are capable of driving a variety of SAW filters.

(T. Giesberts – 924078)





SOLID STATE T/R TRANSVERTER INTERFACE

This little circuit is intended for UHF transverters in combination with a 2-m band transceiver. It is simple to build and much cheaper than a coax relay.

Design by Pedro Wyns, ON4AWQ

A problem with the use of a 70-cm or 23-cm transverter in combination with a 2-m transceiver is that the former nearly always has two IF (intermediate frequency) connections: the transmitter input and the receiver output. By contrast, the 2-m rig has only one RF connection. But there are more pitfalls: usually, the transverter can not cope with the normal output power of the transceiver, so that some attenuation is in order. Second, some means has to be devised to enable the transverter to switch between receiving and transmitting under the control of the 2-m transceiver. In most cases, this means that the transceiver has to be opened to bring out a transmit/receive switching voltage that can be used to energize a coax relay. All of these problems may be overcome one way or another, and radio amateurs are not the most faint hearted of electronics enthusiasts. However, one of the most awkward problems tied up with 'getting on the air' on 70 or 23 is not, strictly speaking, a technical one: it is the cost of a suitable coax relay at the input of the transverter (well, yes, there may be the odd technicality to sort out with the YL or XYL regarding finance matters, but these will not be gone into here).

The circuit shown in Fig. 1 is an all-solid-state equivalent of an expensive coax relay at the transceiver side of a 70-cm or 23-cm transverter. Evidently, a coax relay is still required at the output of the transverter, nothing we can do about that! The operation of the circuit is fairly simple. The RX (receive) and TX (transmit) supply voltages of the transverter are brought under the control of the PTT (push-to-talk) switch of the 2-m transceiver. This is achieved with a pair of complementary (npn/pnp) medium-power transistors Type BD139/BD140. In receive mode, the transverter output signal arrives at the transceiver input via two pieces of coax, Z_2 and Z_1. When the 2-m transceiver starts to transmit, the +TX transverter supply line switches to +12 V. The resulting direct voltage that arrives on the PIN diodes causes the transceiver's RF output energy to be fed to a pi-type attenuator consisting of three resistors. Also, the two quarter-wave pieces of coax, Z_1 and Z_2, then form a notch (band-stop filter) for the 2-m signal, so that virtually no RF signal arrives at the transverter's receiver output. The two pairs of anti-parallel PIN diodes also protect the transverter's receiver output against RF power when the supply voltage happens to be off.

The value and the power rating of the resistors in the pi-attenuator, R_7-R_8-R_9, depend on the degree of attenuation required, and must, therefore, be calculated on the basis of the transceiver output power and the maximum transverter input power.

The RF losses introduced by the PIN diodes are negligible since the switch is inserted at the IF (intermediate frequency) output of the transverter. As is well known from UHF and SHF receiver engineering, it is the **input** stage, not the IF stage, of a receiver that determines the overall noise figure (provided there is sufficient conversion gain).

The transverter interface should not be too difficult to build using 'dead bug' techniques familiar from experimental RF constructing. The transistor pair is conveniently accommodated on a piece of stripboard.

The length of the coax pieces is about 0.66 times the quarter-wave length of the IF signal. If a 2-m rig is used, the length is

$\lambda = 300/145 \text{ MHz} \approx 2 \text{ m}$
$\frac{1}{4}\lambda \approx 50 \text{ cm}$
length $= 0.66 \times 50 \text{ cm} \approx 33 \text{ cm}$

The factor 0.66 is the so-called velocity factor of the coax cable, and applies to most types of 50-Ω cable. The four cable ends must be grounded via the shielding braid. The author used RG58 coax for the prototype, although other cables may be used as well, for instance, RG174U, which is much thinner. Teflon (PTFE) coax is even better, but check the velocity factor to make sure that the physical lengths of Z_1 and Z_2 are correct. Finally, the +12V Rx and +12V Tx outputs of the circuit are capable of supplying up to about 300 mA. Where higher currents are required, T_1 and T_2 must be replaced with power darlingtons. ■

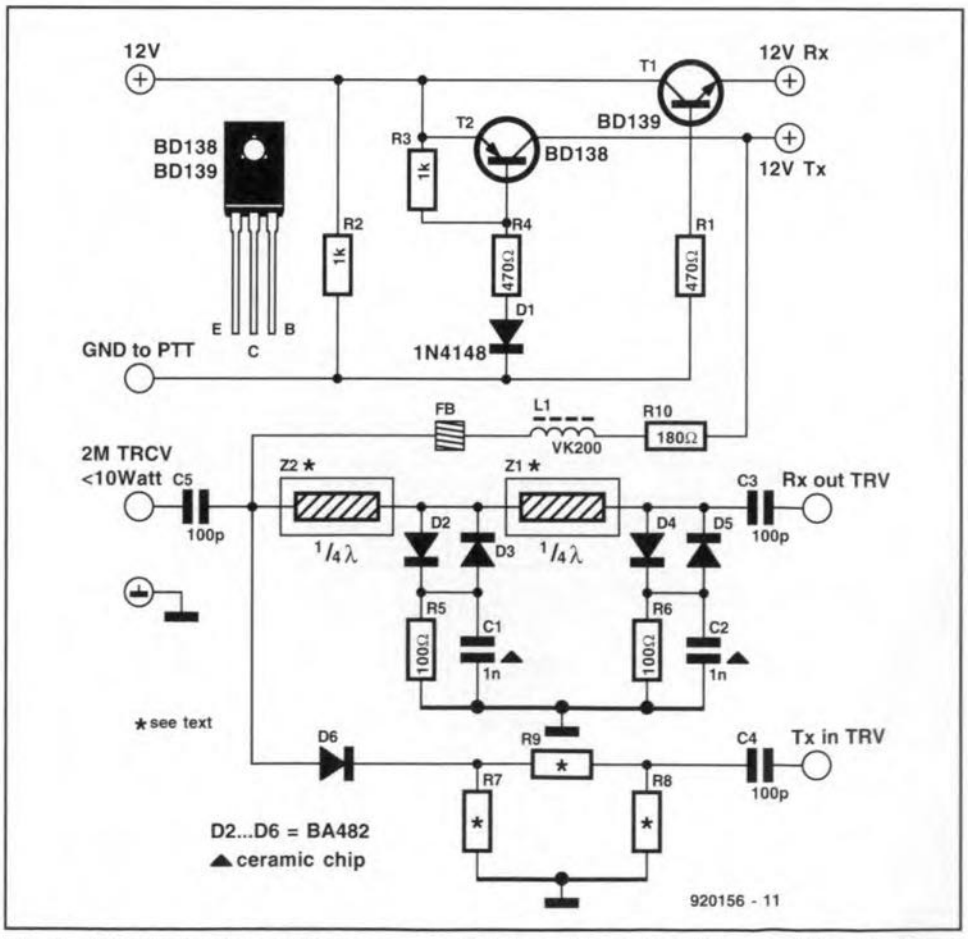


Fig. 1. Circuit diagram of the transverter interface. The value of the resistors in the pi-attenuator depends on the power supplied by your 2-m transceiver. FB is a small ferrite bead.

DISKETTE-SIDE CHOOSER

This small auxiliary circuit enables either of the two sides of a $3^1/_2$ in diskette used in an Atari ST drive to be chosen. Some LEDs show which side has been selected, while others indicate whether a read or a write operation is in progress.

In Fig. 1, bistable IC_{1b} serves to choose one of the two sides of the diskette. A sensor, formed by a small disk of conducting material, is connected to its clock input via inverter IC_{2f}. The input of the inverter is linked to the +5 V rail via two 10 MΩ resistors.

When the sensor is touched, the input of IC_{2f} is pulled low via the skin resistance. This results in a positive leading transition (edge) to the clock input of IC_{1b}, whereupon the levels at pins 12 and 13 of the bistable change state.

Network R_4-C_1 suppresses spurious pulses during operation and prevents the bistable continually changing state if the sensor remains touched.

Pin 13 of IC_{1b} is linked to inverters IC_{2d} and IC_{2e}, each of which controls an LED: D_1 for side I and D_2 for side II. Since D_1 is connected to the +5 V supply rail and D_2 to ground, only one of the two diodes can light at any one time.

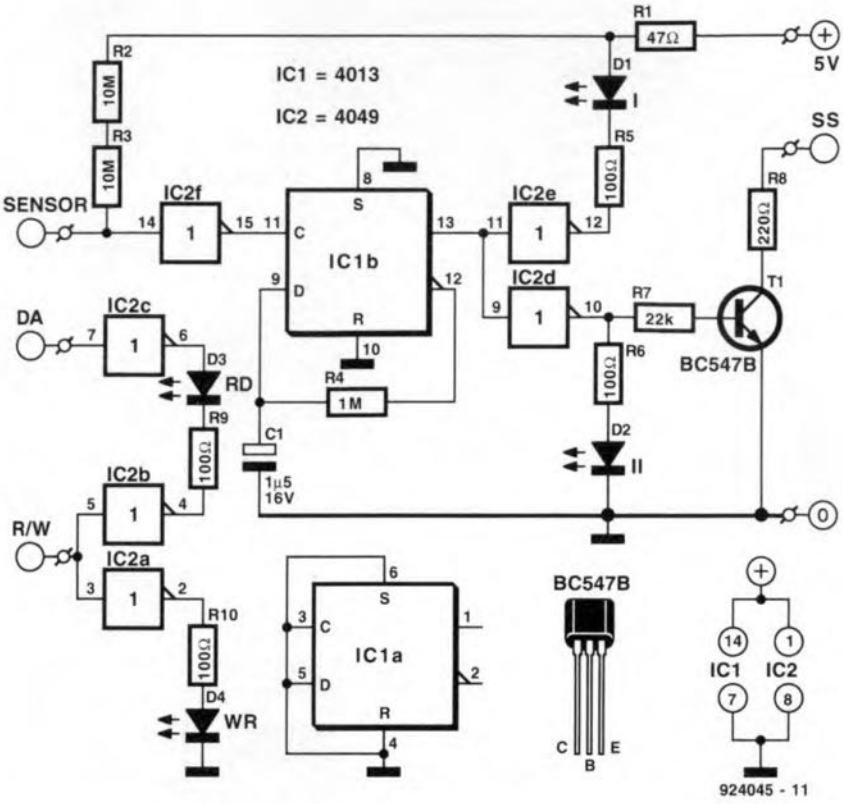
Transistor T_1 serves to alter the level on the Side Select—SS—line of the Atari.

Inverters IC_{2a}–IC_{2c} control D_3 and D_4. The inputs of IC_{2a} and IC_{2b} are linked to the R/W signal of the Atari, while that of IC_{2c} is coupled to the 'disk LED' above the keyboard. This ensures that the 'read' LED lights only when the drive is in motion.

The supply for the auxiliary circuit may be taken from the Atari, since a current of only a few mA is drawn.

Populating the small PCB is simplicity itself. Most of the work will involve fitting the board inside the Atari. The board must be located in the upper part of the keyboard beside the drive LED.

1



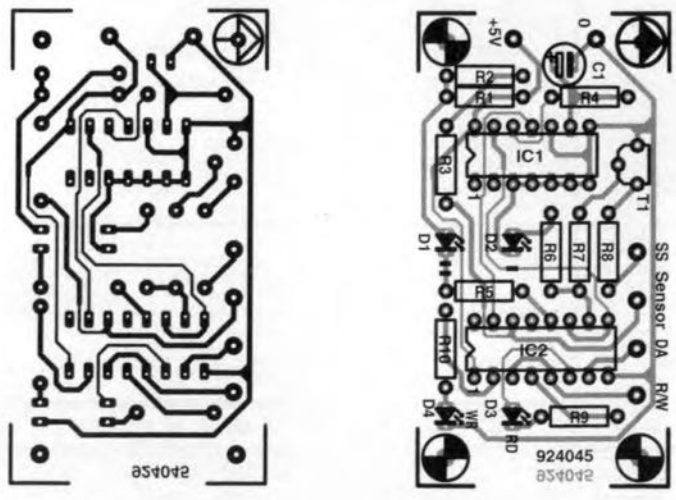
A small front panel as shown in Fig. 2 will be found useful. Note that the LEDs protrude through the small holes in this panel. This means that five holes need to be drilled in the upper panel of the Atari: four for the LEDs and one for the connection to the sensor.

The following connections must be made:

- earth of the PCB to pin 10 of the 74244 underneath the keyboard;
- 5 V line from pin 20 of the 74244 underneath the keyboard to the present circuit;
- SS line to pin 21 of the YM2149;
- R/W line to pin 25 of the DMA controller adjacent to the YM2149 underneath the drive;
- pin DA to the upper terminal of the resistor in series with the drive LED, just to the left of the 74244;
- sensor to the associated pin on the present PCB.

(P. Leroux – 924045)

2



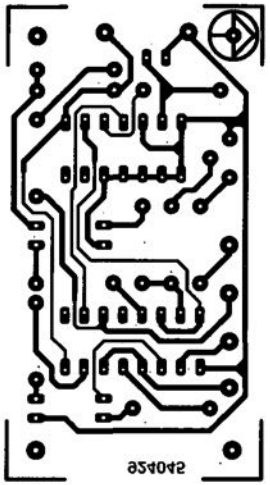
PARTS LIST

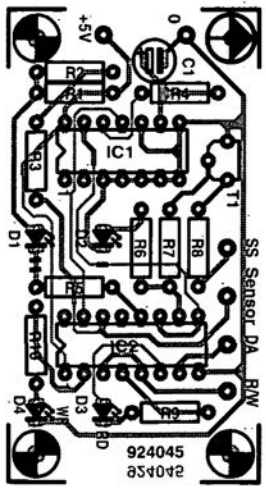
Resistors:
R1 = 47 Ω
R2, R3 = 10 MΩ
R4 = 1 MΩ
R5, R6, R9, R10 = 100 Ω
R7 = 22 kΩ
R8 = 220 Ω

Capacitors:
C1 = 1.5 µF, 16 V

Semiconductors:
D1, D3 = LED, 3 mm, gree
D2, D4 = LED, 3 mm, red
T1 = BC547B
IC1 = 4013
IC2 = 4049

2





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4-DIGIT COUNTER MODULE

This compact four-digit counter is suitable for many applications, such as clocks, frequency meters, digital voltmeters, tachometers, stopwatches, score boards, etc. The counter module provides a reset switch and a carry output signal.

The maximum count of the module depends on which version of the IC used:

- the MM74C926 pulls its carry output high when counter state 6000 is reached. The IC counts to 9999.
- the MM74C927 is like the MM74C926, but the second most significant digit divides by 6 rather than by 10. Thus, if the clock input frequency is 10 Hz, the display would read minutes, seconds and tenths of seconds. e.g. 9:59.9.
- the MM74C928 is like the MM74C926, but the most significant digit divides by 2 rather than by 10. Also, the carry-out is an overflow indicator that goes high at counter state 2000, and goes low only when the counter is reset. Thus, this is a $3^1/_2$ digit counter.

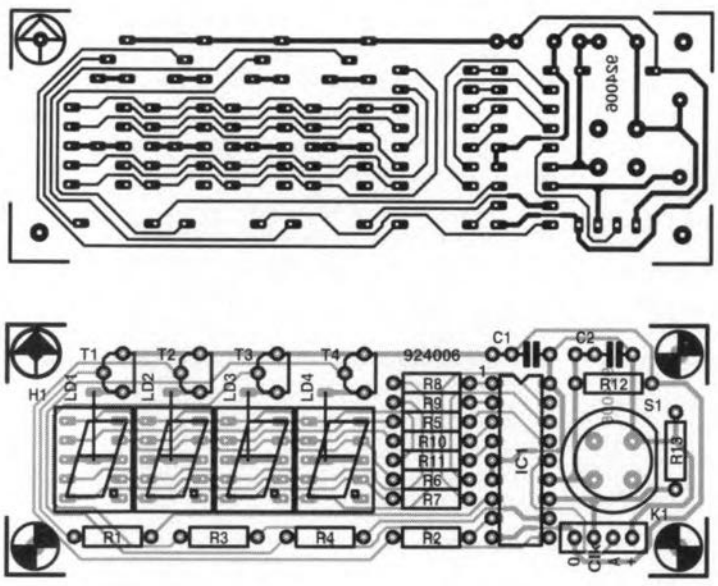
All three MM74C92x ICs are CMOS devices. Each has an on-board display multiplexer, which requires only four external switching transistors at the common cathode connections of the 7-segment LED displays. The multiplex frequency is about 1 kHz.

The carry-out terminal may be used to cascade counter modules.

Current consumption is of the order of 100 mA.

Finally, it should be noted that clock input signals exceeding the module supply voltage are not clamped, and should not be allowed to exceed 15 V. The supply voltage range of all three MM74C92x ICs that may be used here is 3–6 V (data taken from National Semiconductor data sheets).

(A. B. Tiwana – 924006)



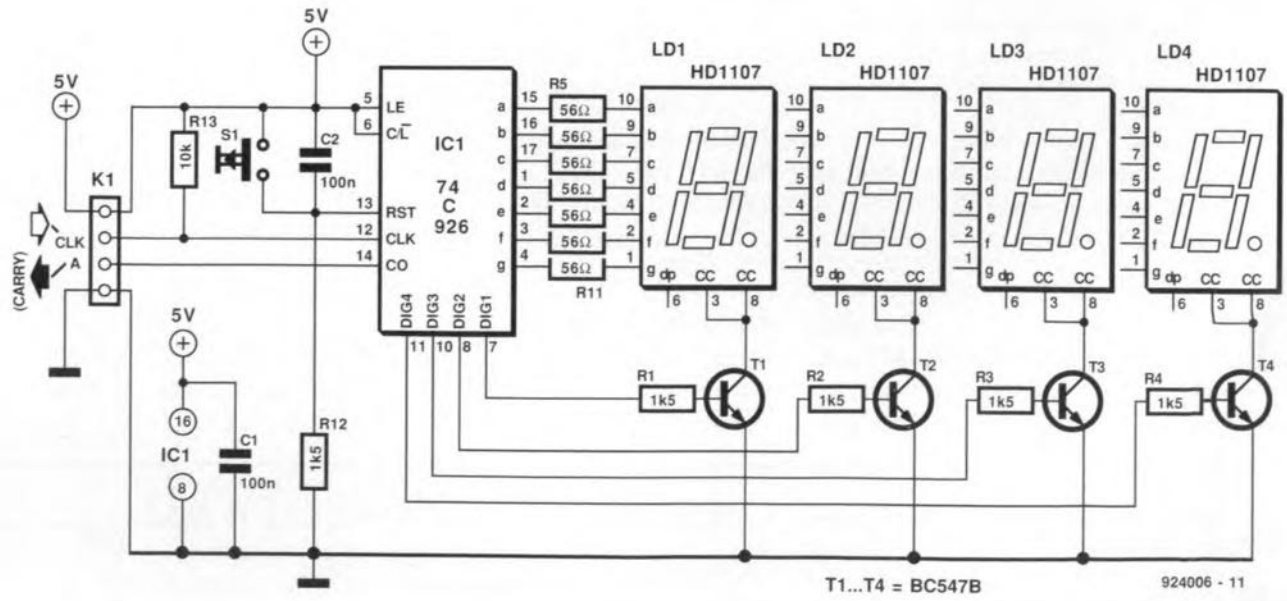
PARTS LIST

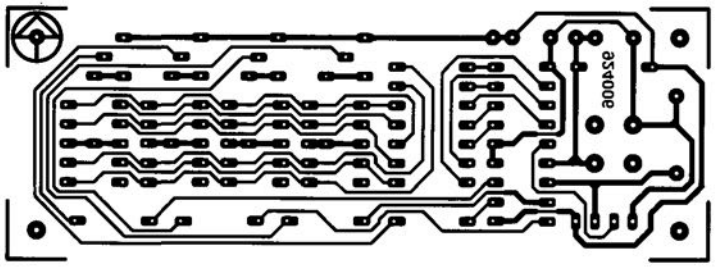
Resistors:
R1-R4;R12 = 1kΩ5
R5-R11 = 56Ω
R13 = 10kΩ

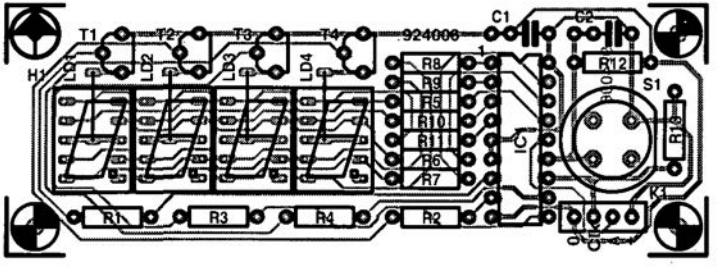
Capacitors:
C1;C2 = 100nF

Semiconductors:
T1-T4 = BC547B
IC1 = 74C926/927/928 (see text)
LD1-LD4 = HD1107

Miscellaneous:
S1 = PCB-mount push-button
K1 = 4-way PCB header







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THERMOCOUPLE-TO-DMM INTERFACE

Thermocouples are economical and rugged devices for temperature measurements. Because of their small size, they respond quickly, and are good choices where fast response to temperature changes is important. Type K thermocouples have a wide temperature range, and are used from cryogenics to jet engine exhaust analysis. The present circuit converts the thermocouple outputs into a direct voltage with a gradient of 10 mV °C^{-1}, which is just about all that is needed to enable a digital multimeter (DMM) to be used for a read-out. Alternatively, the interface output signal may be fed to a computer system for more advanced temperature recording applications.

The AD595A from Analog Devices is a complete instrumentation amplifier and thermocouple cold junction compensator on a monolithic chip. It combines an ice point reference with a precalibrated amplifier to produce an output of 10 mV °C^{-1} directly from a thermocouple signal. The AD595A is laser trimmed for type K (chromel-alumel) thermocouples.

The application of the AD595A shown here could not be simpler. The Type K thermocouple is connected to a special socket, K_1. Resistor R_1 is included to ensure that common-mode voltages induced in the thermocouple loop are not converted to normal mode. The AD595A features an alarm output, +ALM (pin12), which is used here to drive a low-current LED. The +ALM output goes low when one or both of the thermocouple leads are interrupted. It should be noted that the cold junction compensation provided by the AD595A will be affected whenever the alarm circuit is actuated. This means that readings taken when the alarm output is actuated are invalid.

Because a thermocouple output voltage is non-linear with respect to temperature, and the AD595A linearly amplifies the compensated signal, the following transfer function must be used to determine the actual output voltage:

$$U_o = 247.3(U_{th} + 0.011)$$

where U_o is the output of the AD595A and U_{th} is the thermocouple output in mV.

Since ANSI Type K and DIN NiCr-Ni thermocouples are composed of identical alloys, both may be used with the present interface.

Construction of the interface is straightforward since very few parts are involved. Note the copper area under the converter chip to improve the thermal contact between the thermocouple socket and the IC. A low thermal resistance is important here to ensure that the on-chip ice point reference operates correctly.

The interface may be powered from a symmetical or an asymmetrical power supply. In the first case, the '0' and 'ground' terminals are interconnected, and taken to the '–' terminal of the battery. Note, however, that temperatures below 0 °C cannot be measured if a single-ended supply is used. When a symmetrical supply is used, the full temperature range becomes available. A symmetrical supply is best provided by two 9-V batteries.

The current drain of the circuit is not greater than 1 mA with the thermocouple connected, and not greater than 10 mA with the thermocouple disconnected (alarm LED lights).

(J. Ruiters – 924052)

Further reading:

"Temperature measurement techniques", *Elektor Electronics*, December 1991.

"A fast, precise thermometer", *Elektor Electronics*, January 1992.

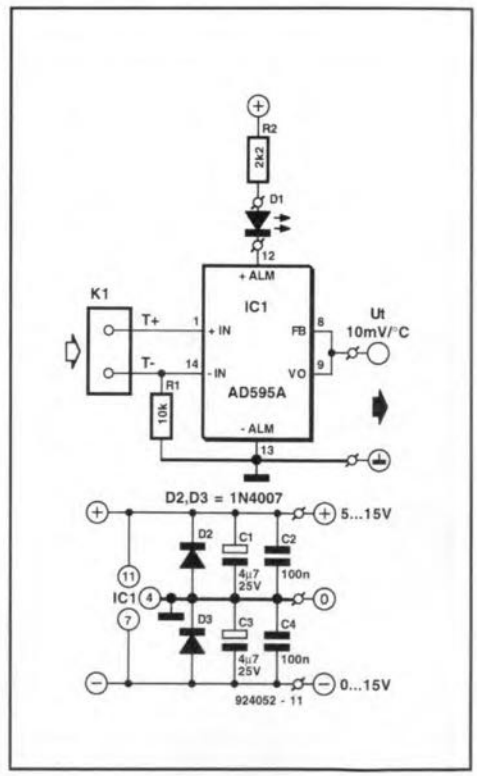
PARTS LIST

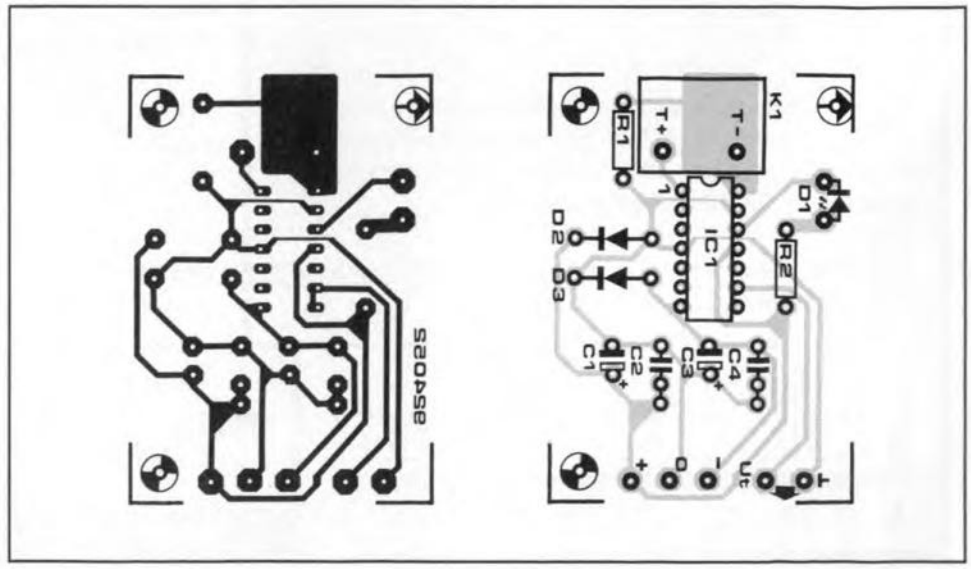
Resistors:
R1 = 10kΩ
R2 = 2kΩ2

Capacitors:
C1;C3= 4μF7 25V radial
C2;C4 = 100nF

Semiconductors:
D1 = LS3369EH (low-current LED; red)
D2;D3 = 1N4007
IC1 = AD595A (Analog Devices)

Miscellaneous:
K1 = special thermocouple type-K socket, e.g. RS Electronics 473-127. Plastic enclosure with battery compartment; approx. size 80x60x20mm; e.g., Prapu 6029 (Conrad order code S23950-22)





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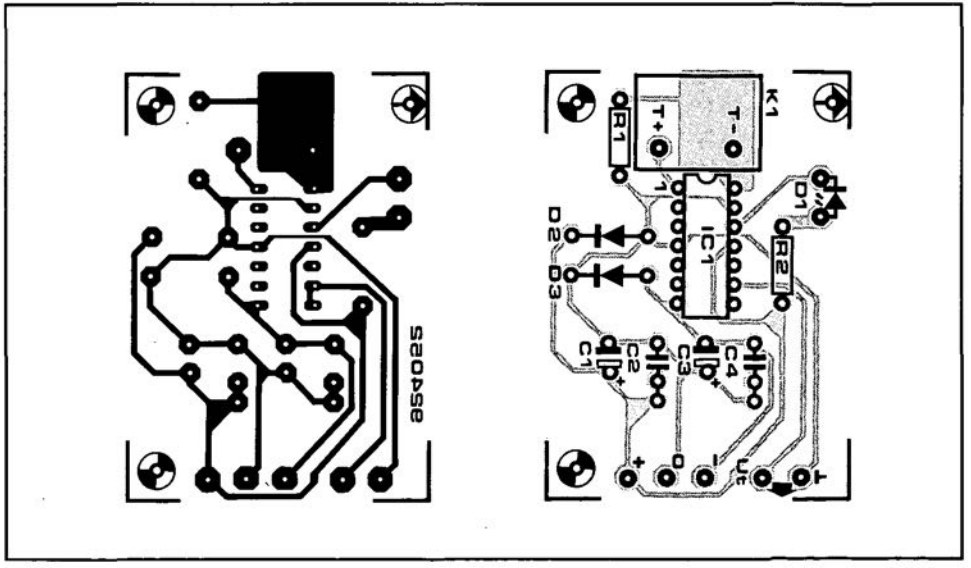


RELATIVE HUMIDITY SENSOR

The Type NH-02 humidity sensor from Figaro consists of a capacitive humidity sensor, Z_s, in series with a thermistor, Z_t on an aluminium substrate. The parameters of the thermistor ensure that it compensates the temperature-dependence of the dielectric of the sensor almost completely. Over the temperature range 15–35 °C, the temperature dependence of the NH-02 is about 0.3% K^{-1}.

Before the sensor can operate, it needs to be energized by an alternating voltage with a frequency of 50–1000 Hz. In the present circuit, that signal is generated by a Wien oscillator based on IC_{1a}, whose frequency is set to about 1 kHz by bridge R_3-R_4-C_3-C_4. The two diodes in the feedback loop ensure amplitude stability. The level of the alternating signal, and thus the maximum output voltage, can be set over a wide range with P_2. This preset is coupled to the sensor by buffer IC_{1b}, which prevents the impedance of the sensor influencing the set voltage.

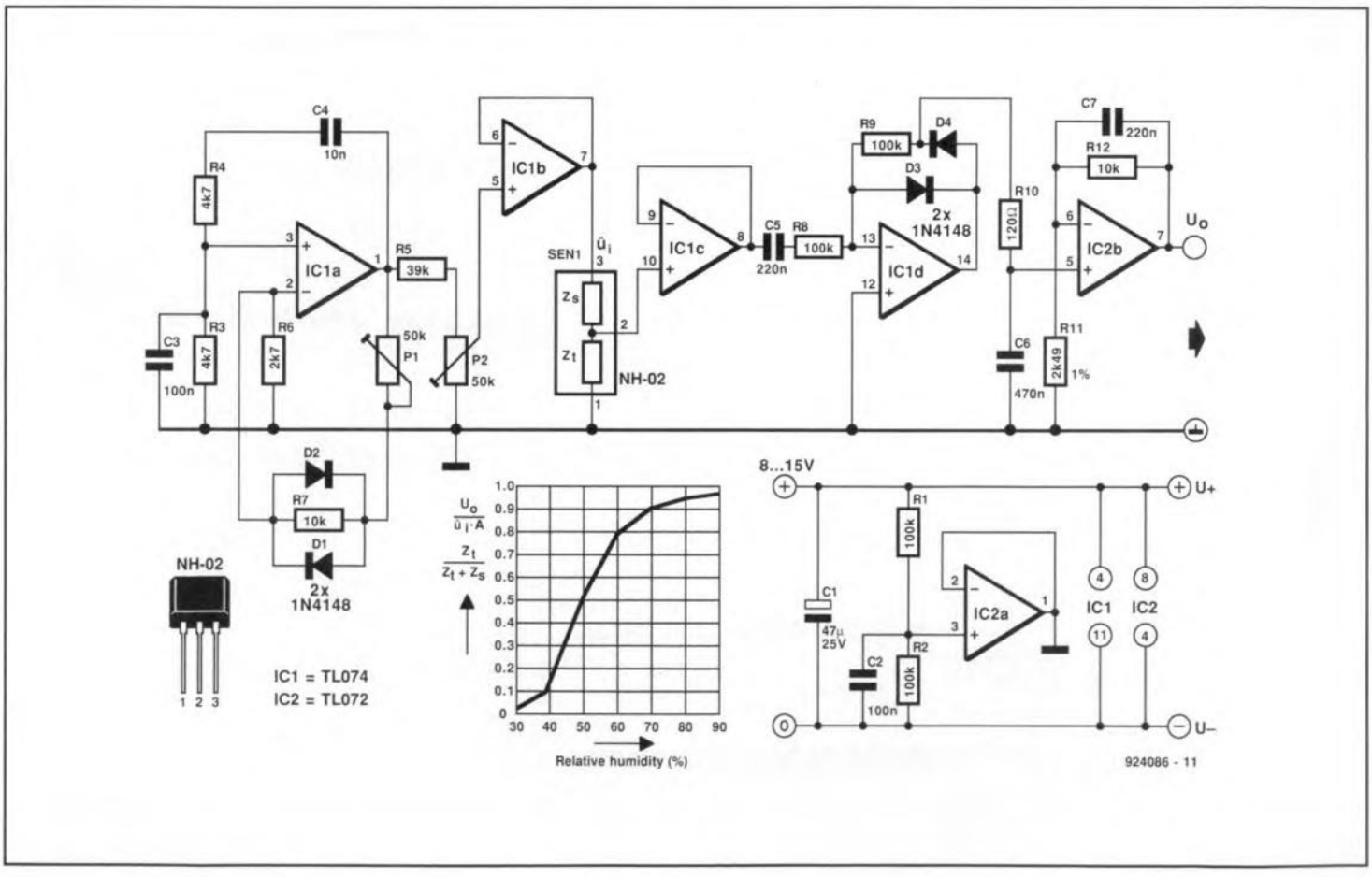
The output voltage of the sensor is buffered by IC_{1c} and then applied to peak rectifier IC_{1d}-D_3-D_4. The output voltage of the rectifier is smoothed by R_{10}-C_6, after which the direct voltage is amplified ×5 by IC_{2b} ($\alpha = 1 + R_{12}/R_{11}$).

The characteristic of the relative humidity vs the output voltage is not linear as shown in the graph. For simple on-off switching applications that does not matter, but for others it may be necessary to make the gradient linear. This is best done with a computer and suitable software.

The power supply may be an asymmetric stabilized 8–15 V type. Opamp IC_{2a} produces an artificial earth at half the supply voltage, so that the circuit is powered by a symmetric 4–7.5 V supply. Note that the supply voltage must be larger than the wanted output voltage.

The circuit is best aligned with the aid of an oscilloscope. With P_1, set the amplitude of the oscillator to a peak value of 2 V (measured between pin 1 of IC_1 and earth). Then, with P_2, set the wanted peak value of the supply to the sensor. In many cases, a peak value of 1 V will be found suitable; the output voltage then varies between 0 V and 5 V.

(J. Ruiters – 924086)



Figaro products are available from

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Figaro Inc.
Oststrasse 10
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Telephone +49 211 358 128
Fax +49 211 359 538

40 W OUTPUT AMPLIFIER

Although there are a number of hybrid output modules on the market, very few of them combine compactness with reasonable price and good performance. One of these few is SGS's used in the present amplifier.

The design of the amplifier is straightforward: a power opamp followed by two output transistors.

The audio signal is applied to the non-inverting input of power opamp IC_1 via socket K_1 and capacitor C_1. The supply current to the IC varies in accordance with the input signal. Consequently, there will be a similarly varying voltage drop across resistors R_6, R_7, R_8, and R_9 since these are in the supply lines to the opamp.

As long as the current is lower than about 1 A, the voltage drop across the resistors will be insufficient to switch on transistors T_1 and T_2. This means that outputs up to 2 W into 4 Ω are provided entirely by the opamp. Once the output current exceeds a level of 1 A, the transistors are on and contribute to the power output.

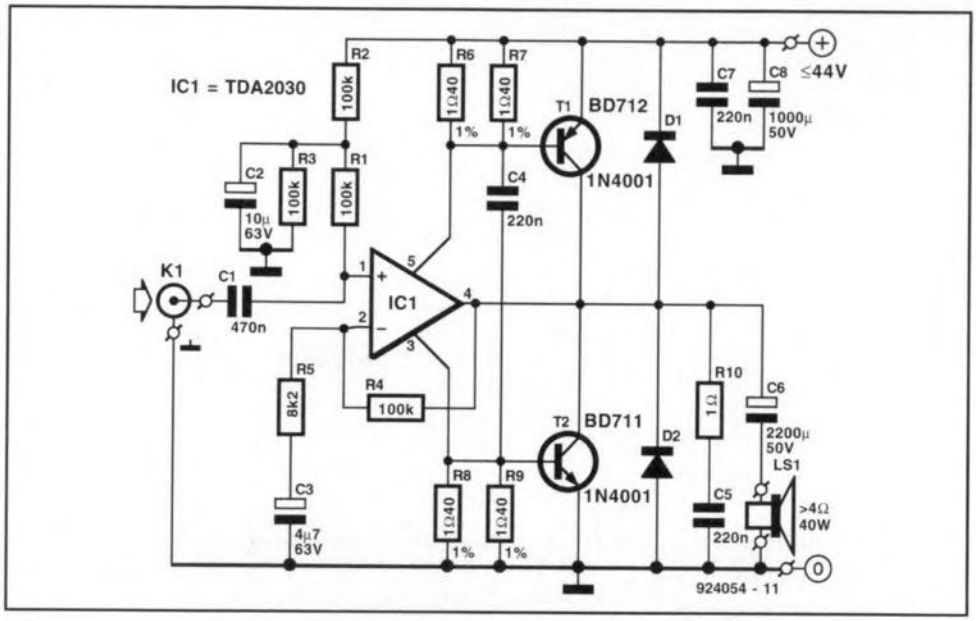
When the input signal is small, there is no quiescent current through the transistor, but there is through the opamp. Crossover problems are thus obviated. Since the IC also provides thermal compensation, stability of the operating point is ensured.

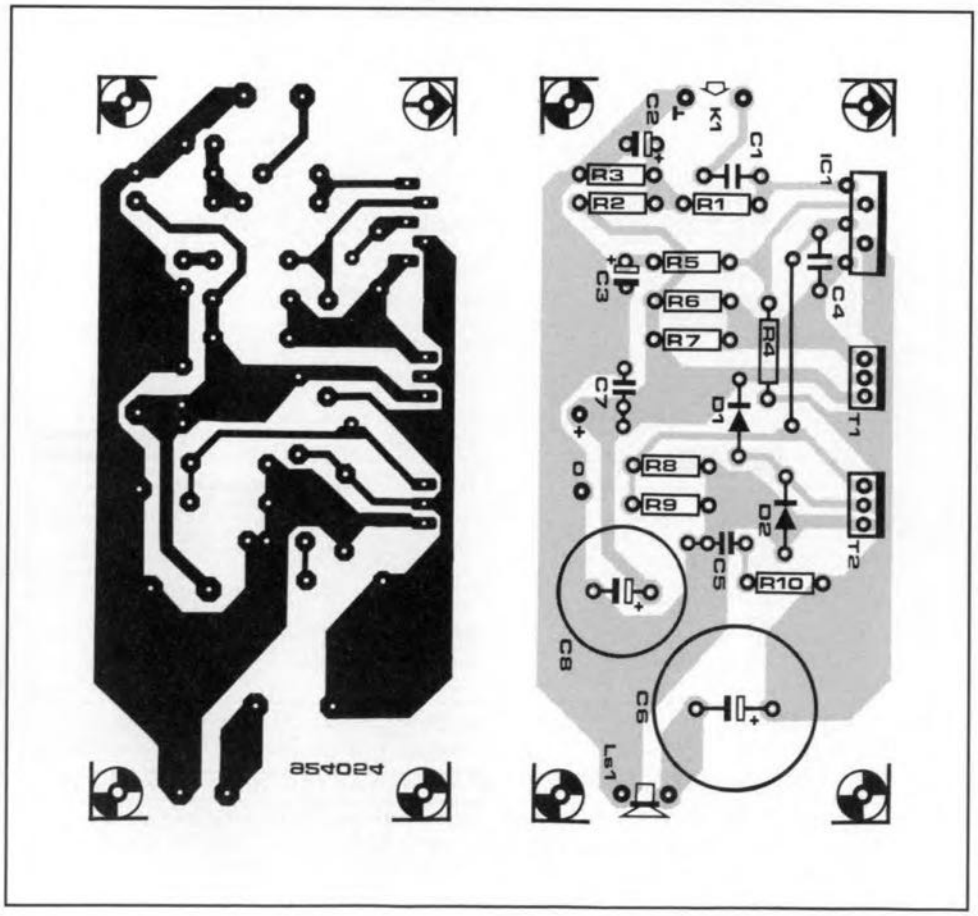
The supply voltage may lie between 12 V and an absolute maximum of 44 V.

Construction of the amplifier on the printed-circuit board should be straightforward. The transistors as well as the IC must be fitted insulated on to a heat sink of about 2 k W^{-1}. Use plenty of heat conducting paste.

The supply line should be protected by a 3.15 A fuse.

(SGS application – 924054)





Technical Data

Supply voltage		44 V
Maximum output		22 W into 8 Ω
(for THD=0.1%)		40 W into 4 Ω
Hamonic distortion		
1 kHz/8 Ω/11 W		0.012%
1 kHz/4 Ω/20 W		0.032%
20 kHz/8 Ω/11 W		0.074%
20 kHz/4 Ω/20 W		0.2%
1 kHz/8 Ω/1 W		0.038%
1 kHz/4 Ω/1 W		0.044%
Quiescent current		about 38 mA
Efficiency	8 Ω	62.5%
(maximum load)	4 Ω	64%

Parts List

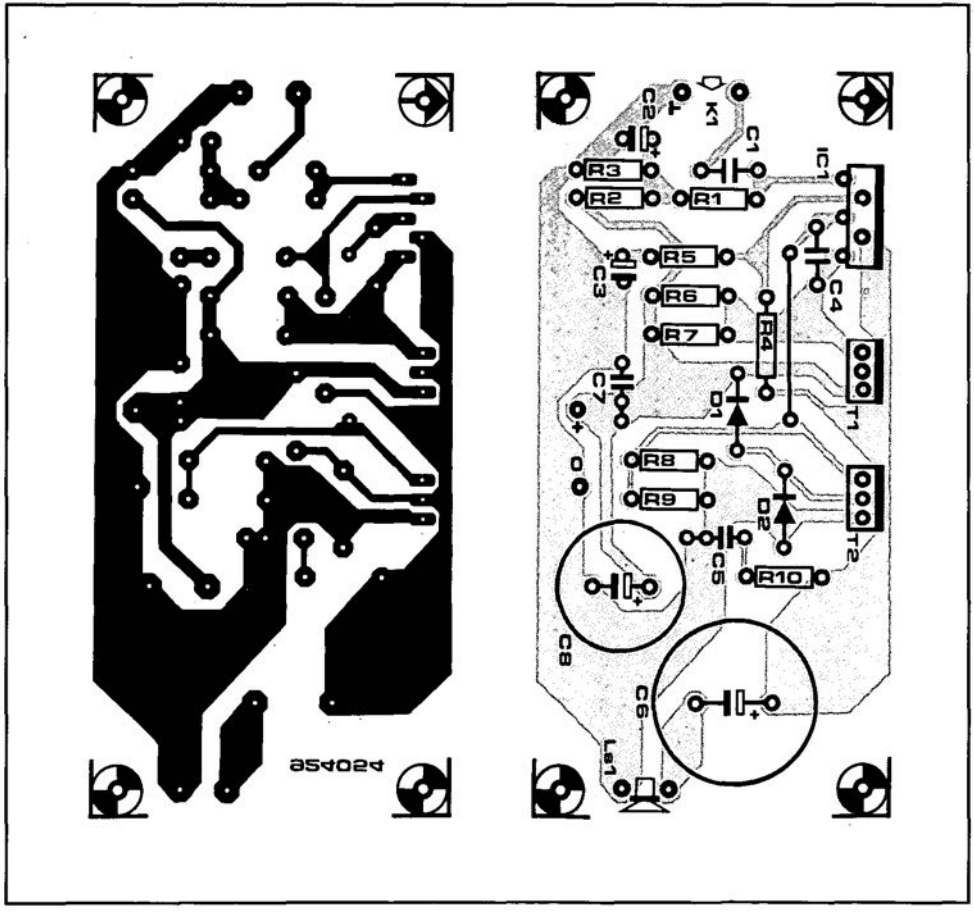
Resistors:
R1–R4 = 100 kΩ
R5 = 8.2 kΩ
R6–R9 = 1.4 Ω, 1%
R10 = 1 Ω

Capacitors:
C1 = 470 nF
C2 = 10 µF, 63 V, radial
C3 = 4.7 µF, 63 V, radial
C4, C5, C7 = 220 nF
C6 = 2200 µF, 50 V, radial
C8 = 100 µF, 50 V, radial

Semiconductors:
D1, D2 = 1N4001
T1 = BD712
T2 = BD711
IC1 = TDA2030

Miscellaneous:
K1 = audio socket
Heat sink 2 K W^{-1}
Insulating washers, etc, for IC1, T1, T2

Quiescent current		about 50 mA
Efficiency	8 Ω	62.5%
(maximum load)	4 Ω	64%



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PULSE GENERATOR FOR AV RECORDERS

AV recorders used in audio-video presentations contain an additional head to read and write the control pulses for the slide projector. These pulses are normally used to actuate a relay that operates the projector. The pulse data are usually written on one of the audio tracks at the non-used side of the tape. Since the extra head in modern recorders does not make use of the two standard audio tracks, it becomes possible to have stereo sound for the presentation. This does mean, however, that only one side of the cassette can be used.

The pulse generator is a complete circuit—see diagram—for utilizing the extra head (L_1) of an AV recorder. The pulses are written on the tape with the aid of S_1, while S_2 is used to select on/off, record, and play. When S_2 is set to its centre position (play), the pulse signal is applied to amplifier T_5-T_6 via C_5. At a certain signal strength the level at the collector of T_6 goes high, whereupon T_7 is switched on via C_{10} and S_{2d}. The relay is then actuated; C_{11} ensures that it does not clatter.

With S_2 in position 3, 6 (record), T_3 is connected to amplifier T_5-T_6. As long as S_1 is not operated, T_2 is on and T_3 is off. However, the stage based on T_1 causes T_2 to switch off for a short time. During that time, T_3 is on and amplifier T_5-T_6 oscillates owing to the feedback via R_5. Since the emitter of T_3 is linked to L_1, the oscillatory signal is written on the tape. During the remainder of the time, T_2, and thus T_4, is on and the tape is erased.

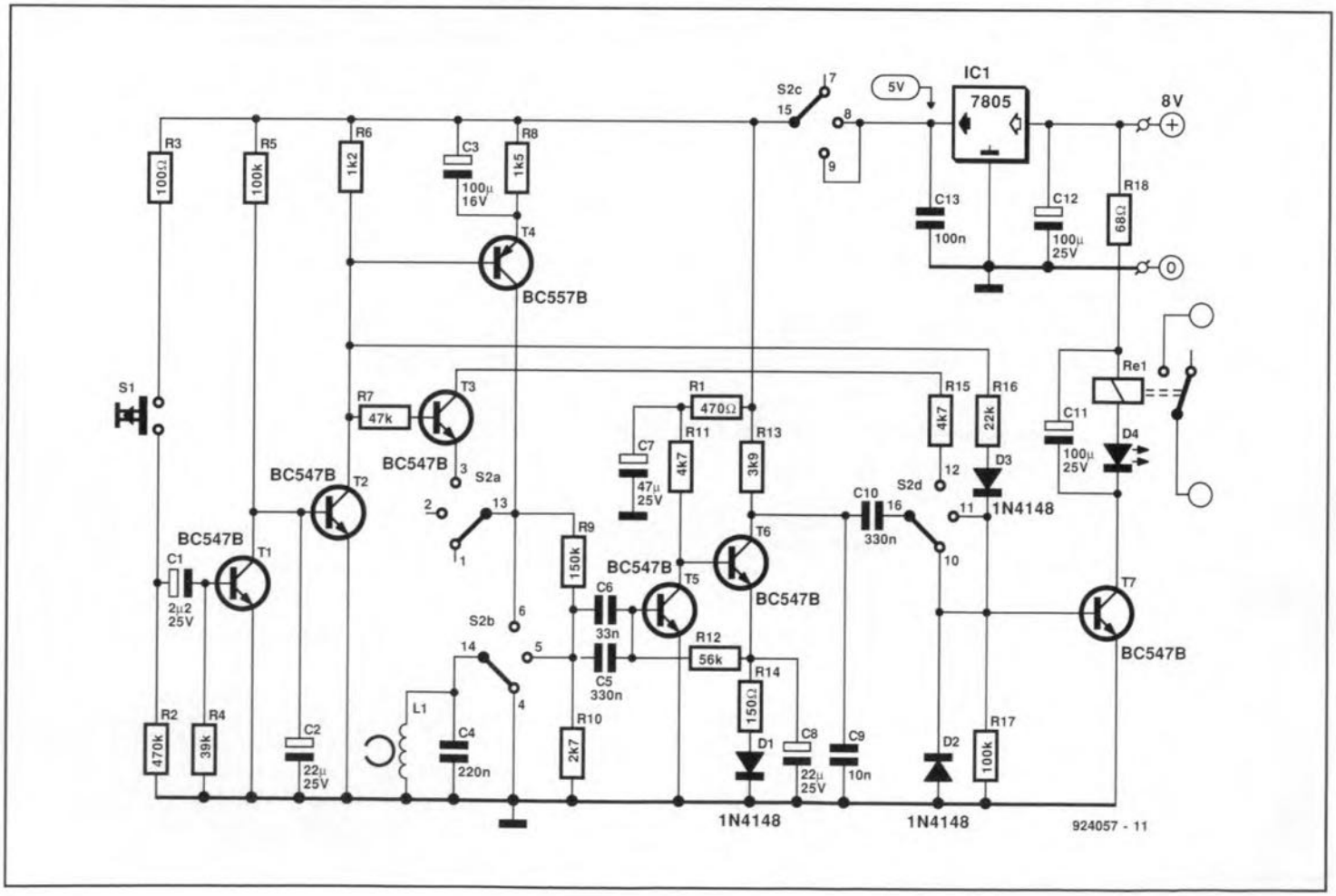
When S_1 is pressed, T_1 conducts for a period determined by the time-constant R_4-C_1 (here 100 ms). Because of this, C_2 is discharged rapidly, and T_2 is switched off. As soon as T_1 is off again, C_2 is charged via R_5. After about one second, the potential across C_2 has risen to a level at which T_2 begins to conduct again. Thus, pressing S_1 causes a one-second pulse to be written on the tape.

Because the collector of T_2 is connected to T_7 via R_{16} and D_3, the relay is actuated when S_1 is pressed, irrespective of whether S_2 is in position play or record.

If for a given projector the pulse duration is too long, it may be shortened by reducing the value of C_2.

The ITT AV recorder shown in the photograph contains a circuit similar to the one described here.

(A. Rietjens – 924057)



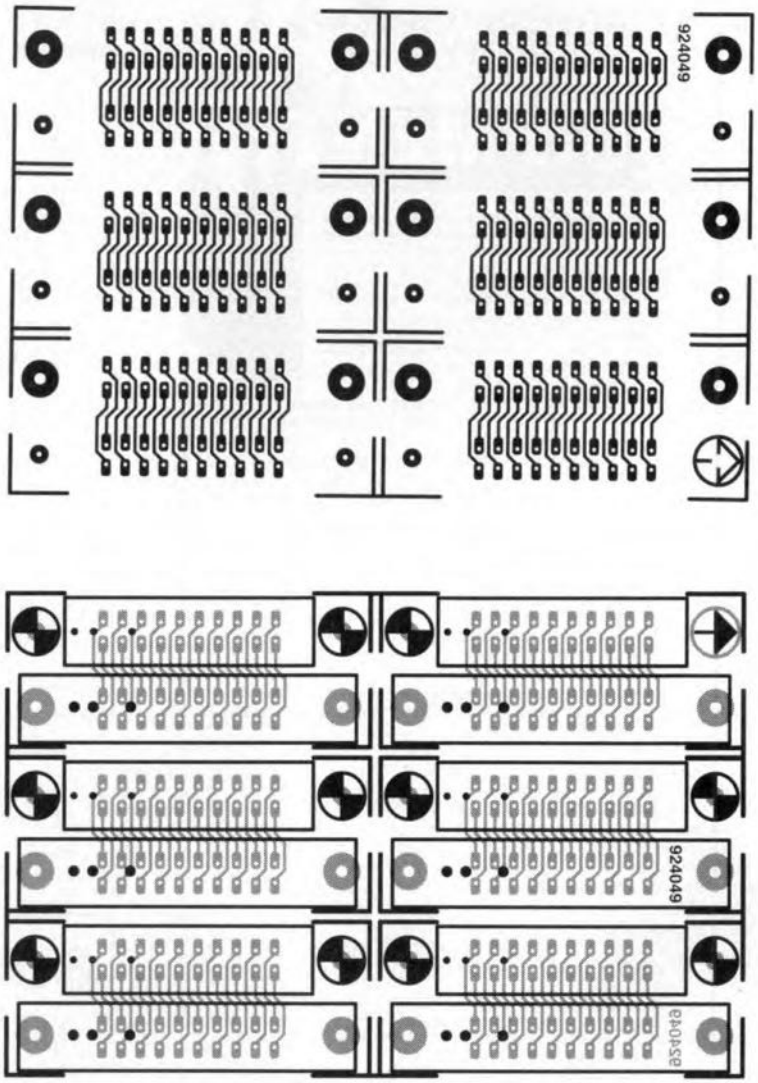
IDC TO BOX HEADER ADAPTOR

Those of you who have ever worked with flatcables will know that IDCs (insulation displacement connectors) are simple to use, and give reliable connections. IDCs are available as sockets and plugs, and used extensively to connect flatcables to double-row box headers or pin-headers on computer cards that offer just about any type of interface to the outside world (a good example is the multi-purpose Z80 card described in Ref. 1).

The present adaptor boards (there are six of them contained on the PCB shown here) are, for instance, perfect for 'changing' from IDC to eject-header style connectors (as illustrated by the photographs) when a flatcable runs from a board to a connector on the rear panel of the enclosure. Also, in many cases, an adaptor board fitted with an eject-style header will be cheaper and more flexible (when it comes to connecting and disconnecting flatcables) than a press-on (IDC style) sub-D socket or plug.

The spots on the component overlay indicate the position of the holes that have to be drilled when smaller types of eject header are used. Straight headers with 10, 14, 16, 18 or 20 pins may be fitted. If you fit two box headers on an adaptor board, you can use it to couple flatcables terminated into IDC sockets. In that way, you can make IDC extension cables, which are particularly useful when a PCB with lots of flatcable connections is removed from an enclosure for repair or inspection.

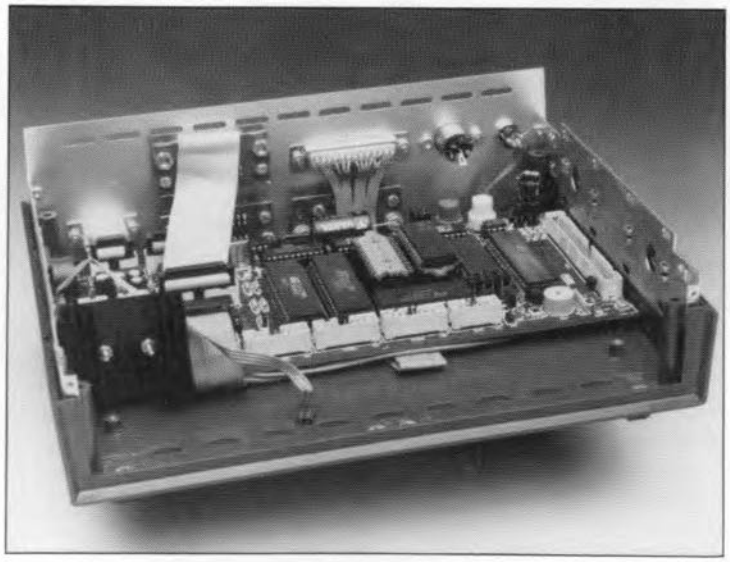
(A. Rietjens – 924049)

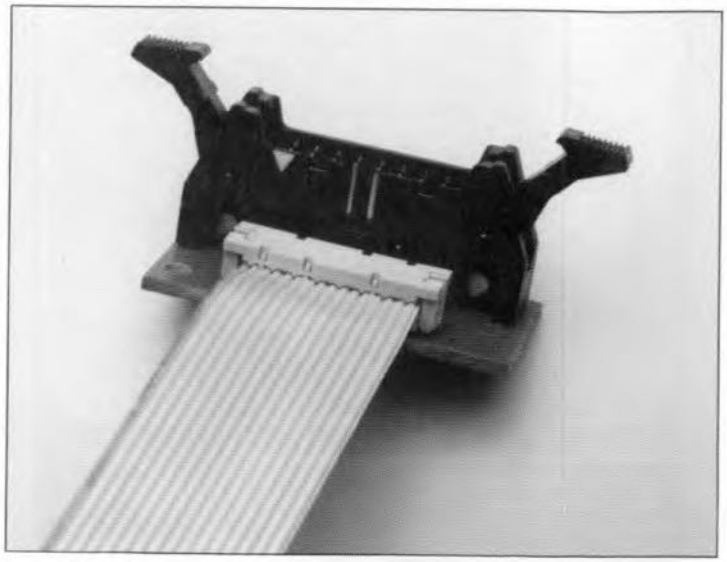


Reference:

1. "Multi-purpose Z80 card", *Elektor Electronics*, May and June 1992.

Printed-circuit board Type 924049 is available through our Readers' services (p. 110)





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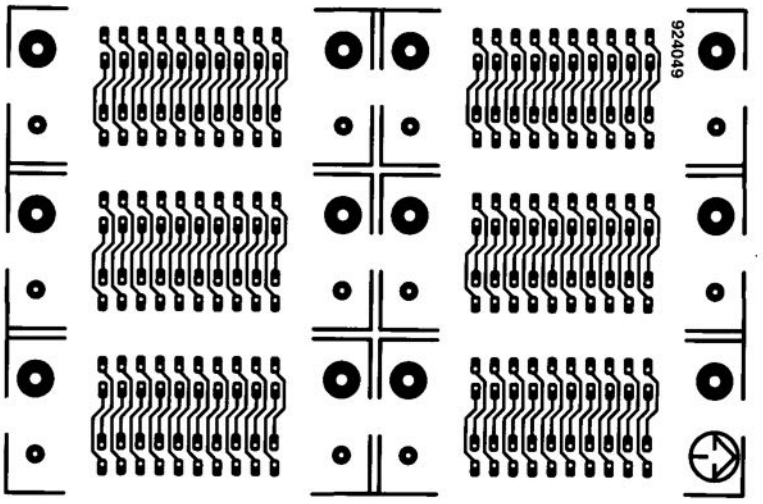
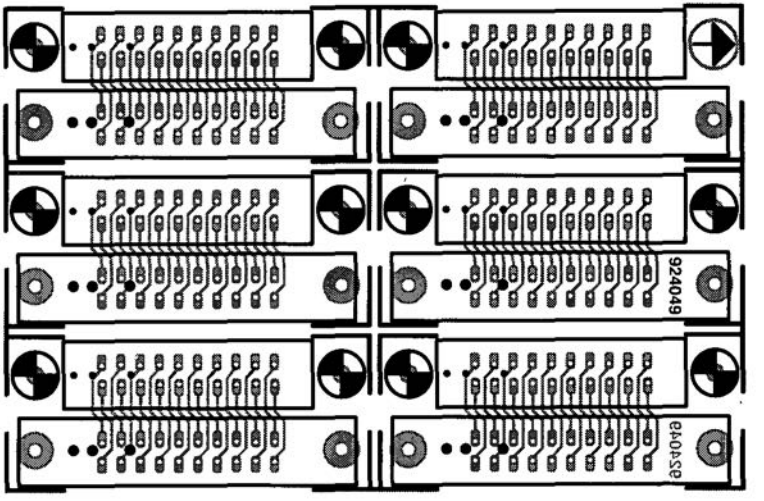
(A. Rietjens – 924049)





LOW NOISE AMPLIFIER I

One way of designing a low-noise amplifier is the shunting of several input stages. This reduces the overall noise, $u_n = u_i n^{-1/2}$, where u_n is the total noise potential of n stages; u_i is the noise voltage of one stage; and n is the number of stages. This design is entirely feasible because noise is a randomly composed signal. Therefore, the noise signals of a number of stages at any one moment are highly likely to have a diferent frequency and phase, so that they partly neutralize one another.

In the present amplifier, three low-noise opamps, IC_1–IC_3, are connected in parallel. According to the manufacturers' data sheet, the noise of a single LT1028 amounts to 0.9 nV $Hz^{-1/2}$. To this must be added the thermal noise generated by resistors R_2–R_{11}. Circuit IC_4 sums and amplifies the output signals of IC_1–IC_3.

Measurements on the prototype show a total noise of 0.67 nV $Hz^{-1/2}$. According to the earlier formula, the three opamps have an overall noise of 0.52 nV $Hz^{-1/2}$. The difference of 0.15 nV between this and the measured figure is caused by the resistors. This is a low figure bearing in mind that a 1 Ω resistor at room temperature generates a thermal noise of 0.13 nV $Hz^{-1/2}$.

The amplification, α, of the circuit is computed from

$$\alpha = -n(1+R_3/R_2)\cdot R_{11}/R_8.$$

It is necessary that the three resistors in groups R_3, R_5, and R_7; R_2, R_4, and R_6; and R_8, R_9, and R_{10}, have identical values. With values as shown, the circuit has an amplification of ×600.

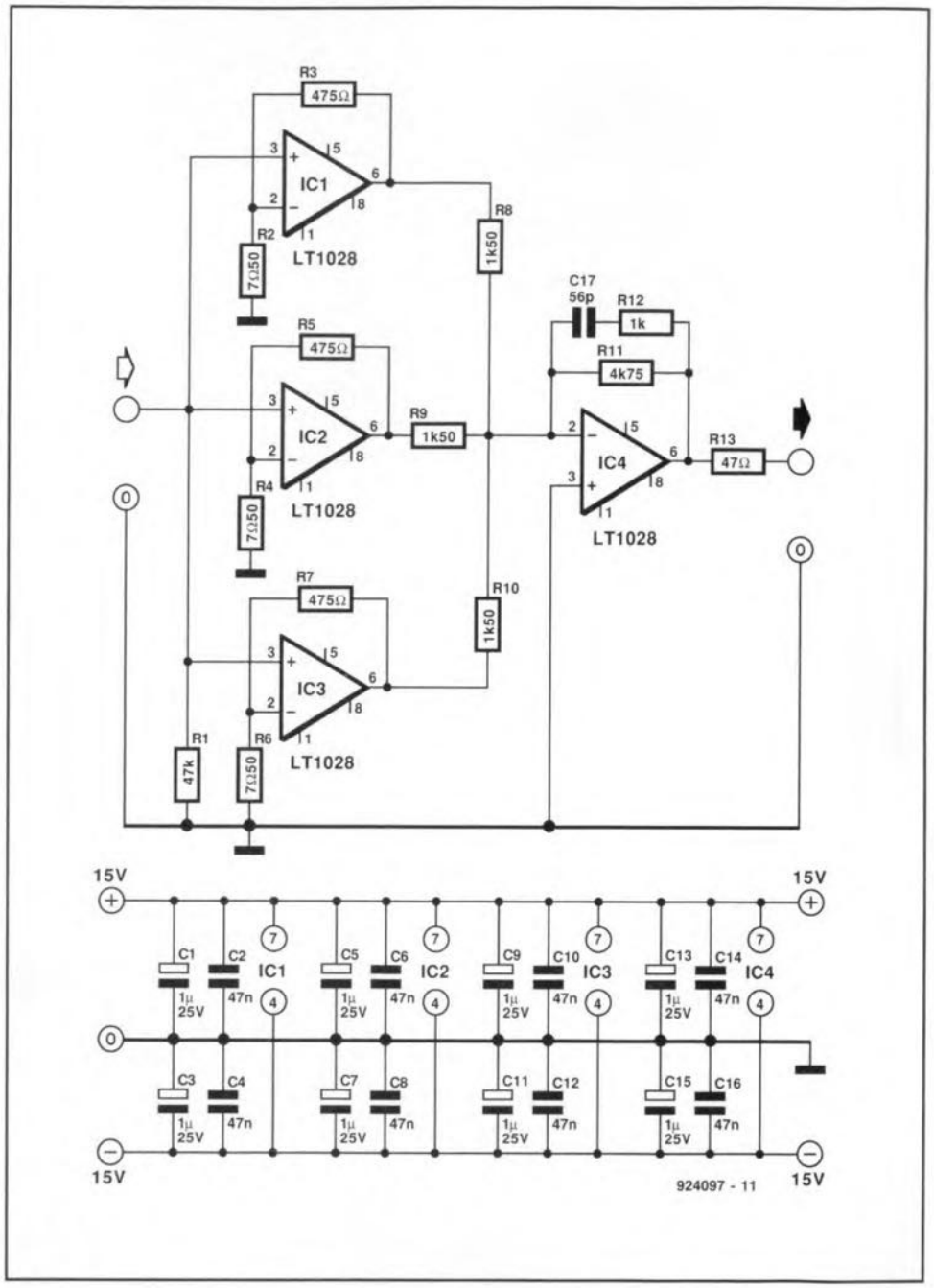
Apart from having a low noise output, the Type LT1028 opamp is also fast: it has a slew rate of 15 V μs^{-1} and a bandwidth of 75 MHz for $\alpha = -1$. Even when the amplification is ×63, the bandwidth of the circuit as a whole, but without R_{12} and C_{17}, is 1.2 MHz. However, to avoid signal overshoot, the bandwidth is limited by R_{12}–C_{17} to 500 kHz, which is more than adequate for even the most demanding audio application.

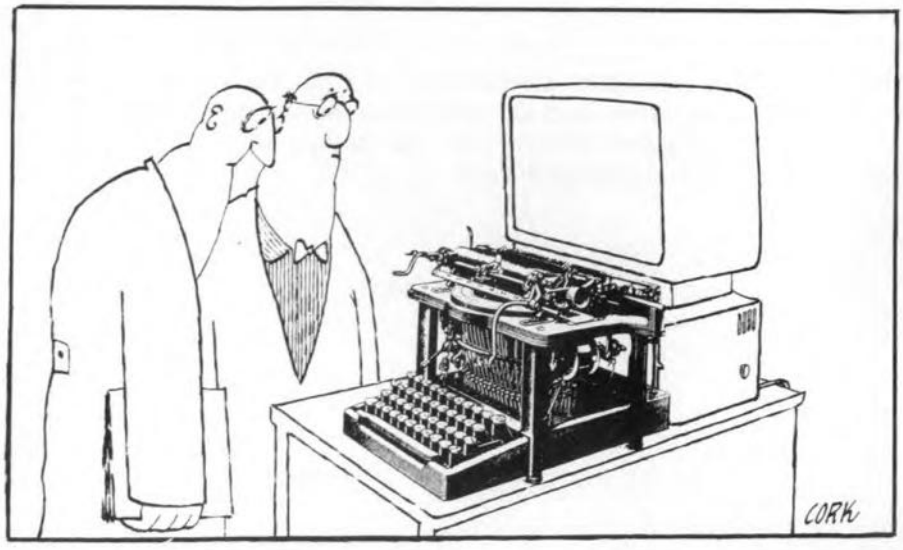
The THD+noise ratio at a 1 kHz output at a level of 1 V is only 0.008%.

If you wish to experiment with the LT1028, bear in mind that its stability is internally compensated for amplifications of >×2. Since resistors R_2, R_4, and R_6 contribute most to the overall noise, it is necessary that their value is kept as low as possible. Naturally, all resistors used should be metal film types.

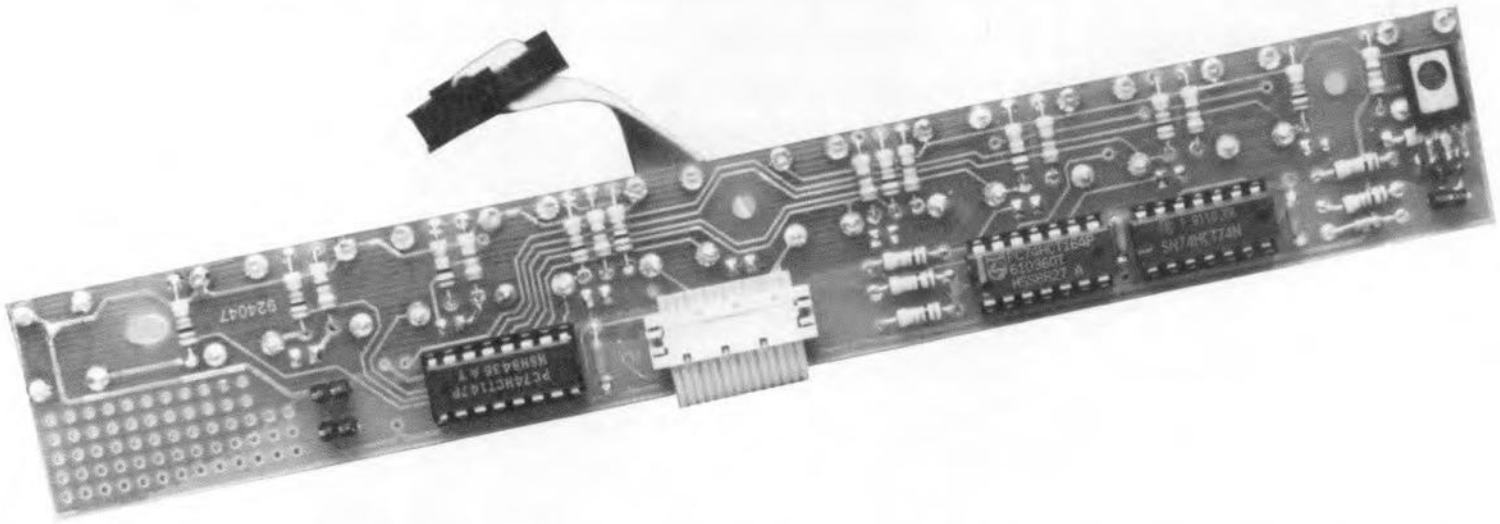
With a supply voltage of ±15 V, each IC draws a current of about 7.5 mA.

(T. Giesberts – 924097)





MINI KEYBOARD FOR Z-80 CARD



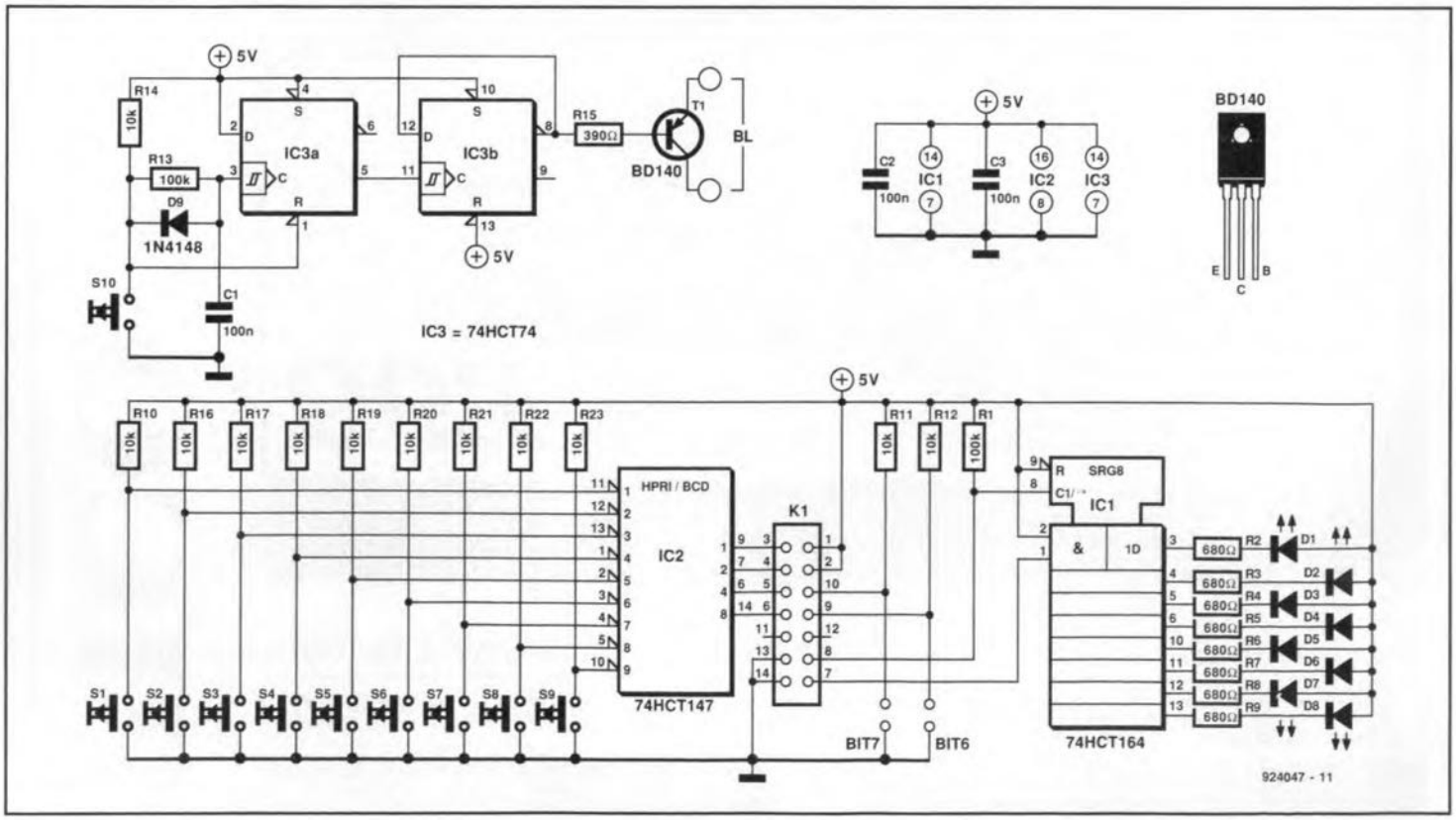
Depending on the application of the 'Multifunction Z80 card' (Ref. 1), a basic set of switches to control the program flow may be required. Also, in some cases, the PC/XT keyboard that can be connected to the card may prove a little too bulky to be carried around. The keyboard plus LED indication described here is connected to PIOA on the multi-function Z80 card. The 10 keys are arranged horizontally (see PCB layout) on a board fitted behind the enclosure front panel, and serve to control functions determined by the user software. With the exception of S_1 and S_{10}, each key has an associated LED to indicate the key status.

The number of the key pressed is conveyed to the PIO in the form of an inverted 4-bit binary number supplied by IC_2, a 10-to-4 line priority encoder Type 74HCT147. No key pressed gives output value 15 (binary), while, for instance, key 2 gives 15–2=13.

Bits 6 and 7 are normally logic high, but can be strapped low if desired by fitting jumpers. They may be used as required by the application. A suggestion: the Z80 software, on reading the key number, causes the PIO on the Z80 card to pull line PA4 high, which enables shift register IC_1. Next, the PIO causes one of the LEDs to light by outputting the appropriate number of clock pulses via line PA5. Since the LED activity is controlled by the keyboard decoder software, rather than directly by the keys, the user has a good indication that the selected function has been accepted by the system.

In principle, K_1 on the keyboard unit can be connected to any of the three PIOs on the Z80 card: K_4, K_5 or K_6. The keyboard/LED routines in the BIOS EPROM (ESS6121—see p. 110), however, are based on connection to K_4 (PIOA). The routines 'READEXTRAKEY' and 'LED-OUTPUT' provided in the BIOS, and a demonstration program on the project diskette (ESS1711—see p. 110), make life easy for the Z80 programmer by offering simple ways of reading the keys, and controlling the LEDs, respectively.

The user is, of course, free to determine the functions of the keys and LEDs,



or, indeed, to omit one or more keys or LEDs not required for his application.

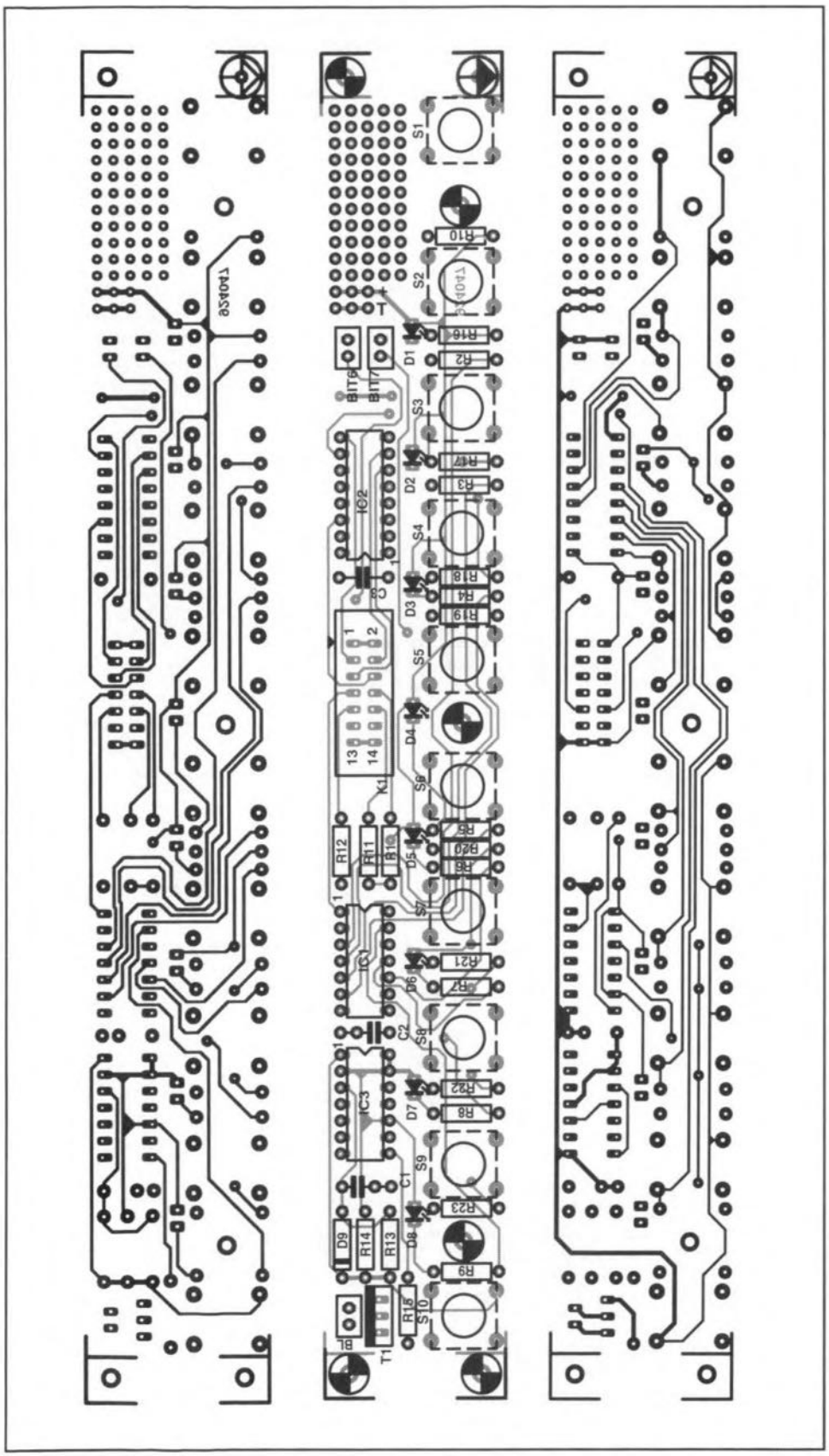
Switch S_{10} has a special function, and is not read by the Z80: it is the LCD back light control switch that uses two bistables (IC_{3a} and IC_{3b}) to provide a toggle function.

Transistor T_1 is effectively connected in series with the back light supply and the back light input of the LCD (more details on this may be found in Ref. 1). The outputs marked 'BL' are connected to the jumper marked 'LCD' on the Z80 card. If the back light is very weak, the BL connections should be interchanged. In this application, the BD140 will happily work in both directions, but its current gain will be much lower when the collector functions as the emitter.

Construction of the keyboard unit is simple. As indicated by the dashed outlines on the component overlay, **the keys and LEDs are fitted at the solder side of the board**.

Finally, the unit is connected to the Z80 card via a length of 14-way flat-cable fitted with IDC sockets. Connector K_1 may be either a 14-way box header or a 14-way male IDC connector. The latter may be soldered permanently to the PCB, if the other end of the cable is fitted with an IDC socket. Alternatively, if a box header is used in position K_1, the flatcable will have IDC sockets at both ends. Power is supplied via this cable by the Z80 card.

(A. Rietjens – 924047)



Reference:

1. "Multipurpose Z80 card", *Elektor Electronics* May and June 1992.

PARTS LIST

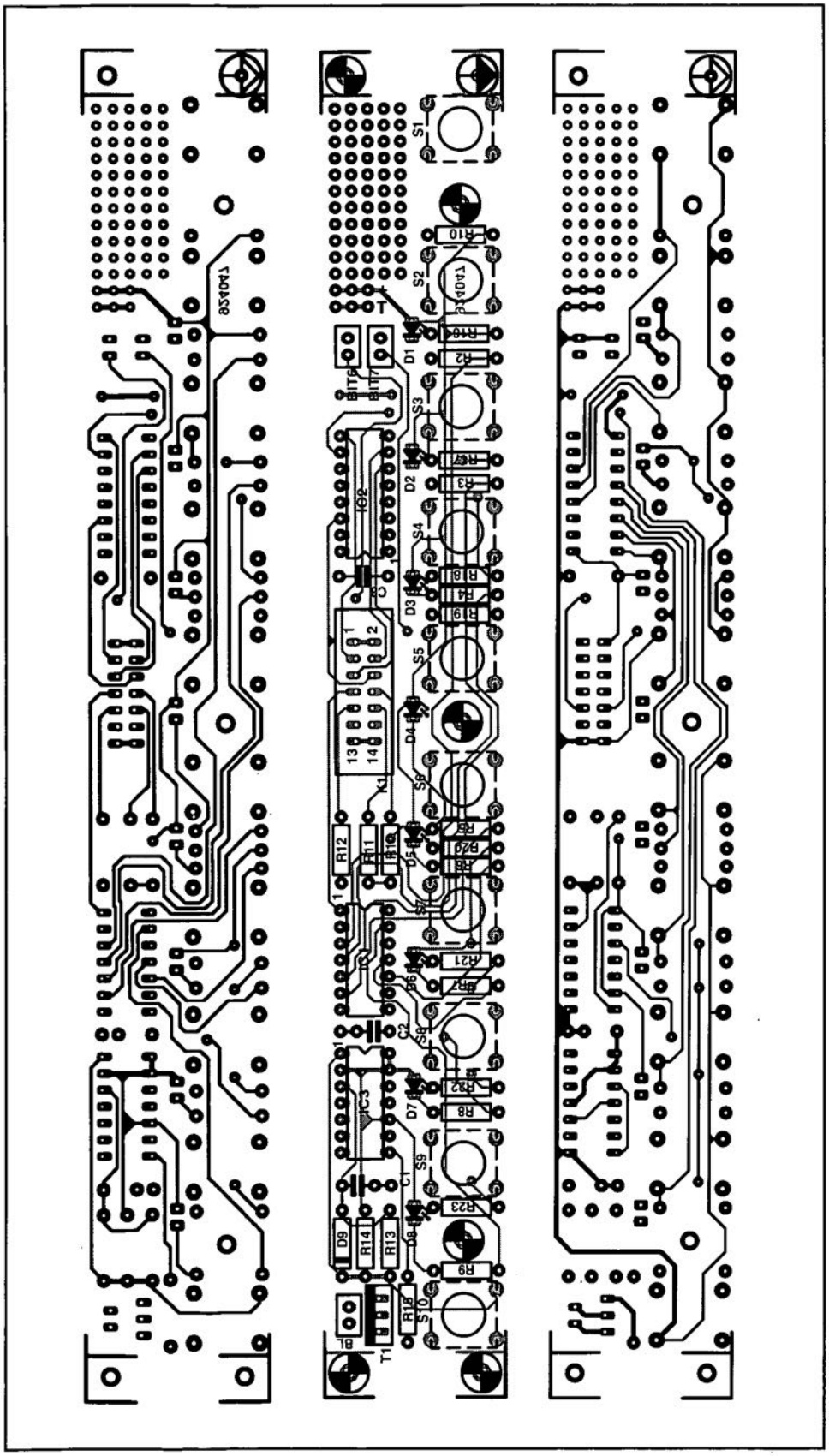
Resistors:
R1;R2 = 100kΩ
R2-R9 = 680Ω
R10;R11;R12;R14;R16-R23 = 10kΩ
R15 = 390Ω

Capacitors:
C1;C2;C3 = 100nF

Semiconductors:
D1-D8 = LED, 3mm, red
D9 = 1N4148
T1 = BD140
IC1 = 74HCT164
IC2 = 74HCT147
IC3 = 74HCT74

Miscellaneous:
K1 = 14-way box header or male IDC connector (see text).
S1-S10 = PCB-mount push-to-make button, Type 3CTL3 (Amroh).
PCB Type 924047.

(A. Rietjens – 924047)



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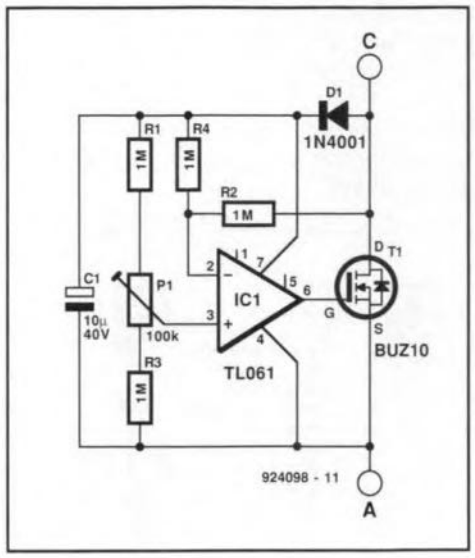
PCB Type 924047.

LOW-DROP DIODE

At high currents, many silicon diodes have a forward voltage of 1 V or more. There are types whose drop at currents of up to 2–3 A is limited to 0.5–0.6 V, but even that may cause unacceptably high losses. The circuit described here offers a possible remedy.

The cathode, C, of T_1, a SIPMOS FET, is connected to a sinusoidal-voltage source. The anode, A, thus functions as a reference point. Capacitor C_1 is charged to the peak value of the sinusoidal voltage, U_s, via D_1. This ensures that the opamp is provided with power even during the negative half-periods of U_s.

The non-inverting input of IC_1 is set to half the peak value of U_s via potential divider R_1-P_1-R_3. Because of voltage divider R_2-R_4, the potential at the inverting input of the opamp will be higher than that at the non-inverting input only during the positive half-periods of U_s. This means that the drain-source channel of T_1 is switched on by the opamp when the voltage at the cathode tends to become lower than that at the anode. In that case, the current through the FET flows



from source to drain, parallel to the internal protection diode. In other words, the FET is used the wrong way round. The forward voltage of the FET diode so created is the product of the current through it times the on resistance (0.07 Ω).

The setting of preset P_1 determines the anode-cathode potential at which the output voltage of the (mainly) linearly operating opamp begins to rise and thus drive T_1 into conduction. The preset can be adjusted accurately only with the aid of an oscilloscope connected to the drain and source of hte FET. It is set to that position where for the nominal forward current the voltage across T_1 is as small as possible during the half-periods when the FET is on. In the prototype, the forward voltage so measured was 0.5 V with an alternating current of 10 A at a frequency of 50 Hz. At 3.3 A, the drop was only 0.2 V and at 300 mA just 0.1 V. Note that the forward voltage remains constant with currents below the level at which P_1 was set.

The circuit draws a current that is not much higher than the supply current to IC_1. Although the maximum supply voltage of the opamp is 36 V, the cathode-anode voltage, that is, the 'reverse' voltage of the 'diode' must not exceed 20 V, which is the maximum permissible gate-source voltage of the BUZ10.

(B. Zschocke – 924098)

DECIBEL STEPPER

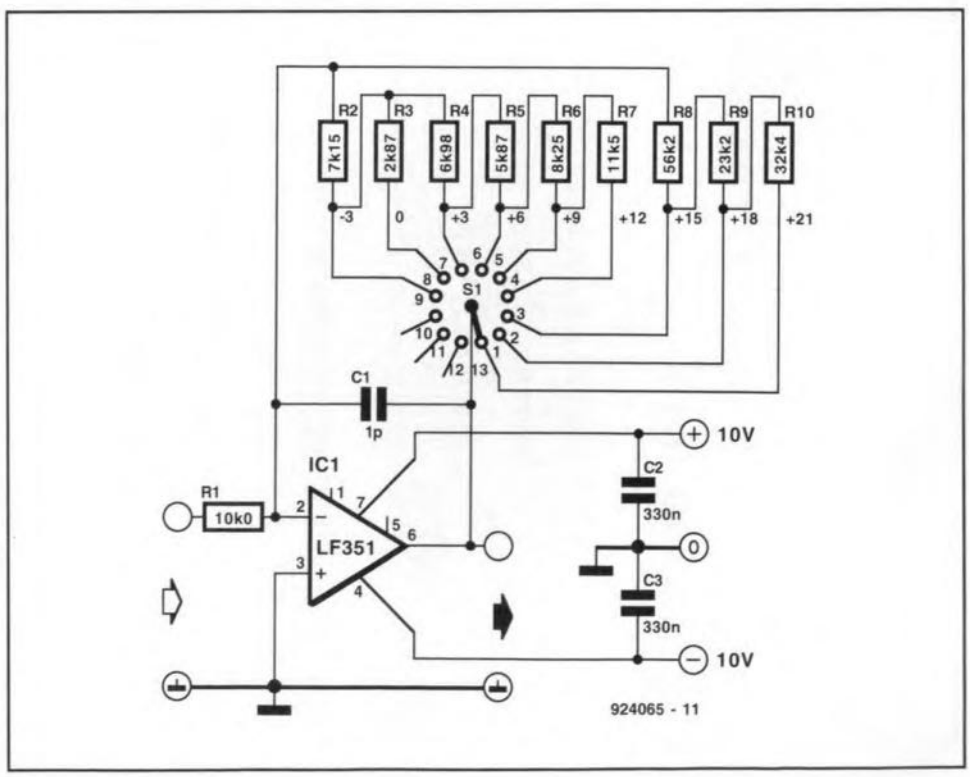
The stepper presented here makes use of nine positions of a 12-position rotary switch. It is, of course, possible to add the omitted steps. As usual, the amplification factors are arrived at by connecting a number of resistors in series in the feedback circuit. The resistors used here are from the E-96 series, which enable a fairly accurate approximation of the wanted amplification. If greater precision is required, combinations of two resistors may be used. This has the drawback, however, that a make-before-break switch must be used to prevent the output constantly being switched to the supply line.

The bandwidth of the amplifier is determined by the set gain and the gain-bandwidth product of the opamp. If an LF351 is used as shown, the gain-bandwidth product is 4 MHz, while the slew rate is 13 V μs^{-1}.

The circuit draws a current not exceeding 2 mA.

Capacitor C_1 improves the stability when the amplification factor is large.

(Amrit Bir Tiwana – 924065)

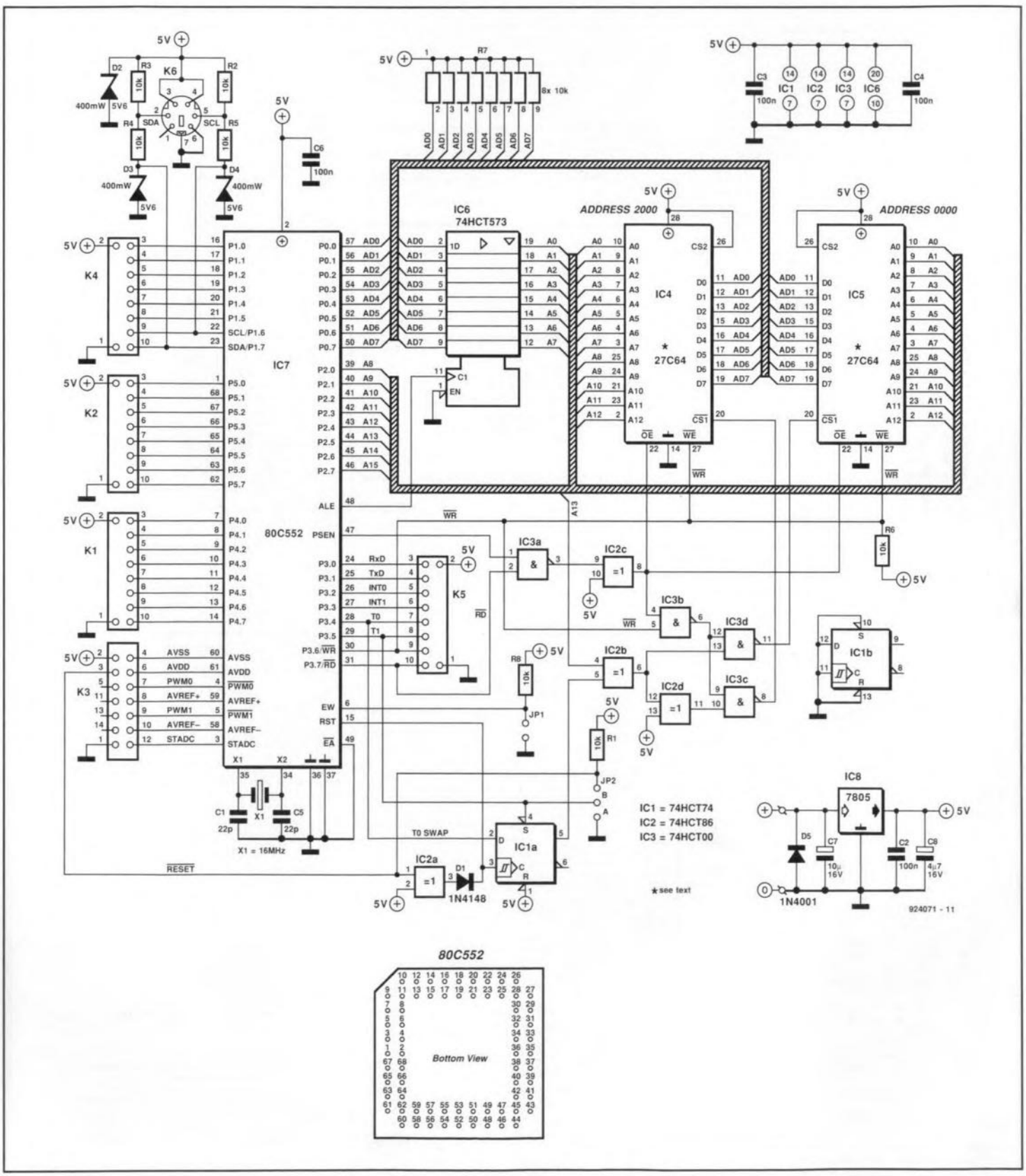


80C552 MICROPROCESSOR SYSTEM

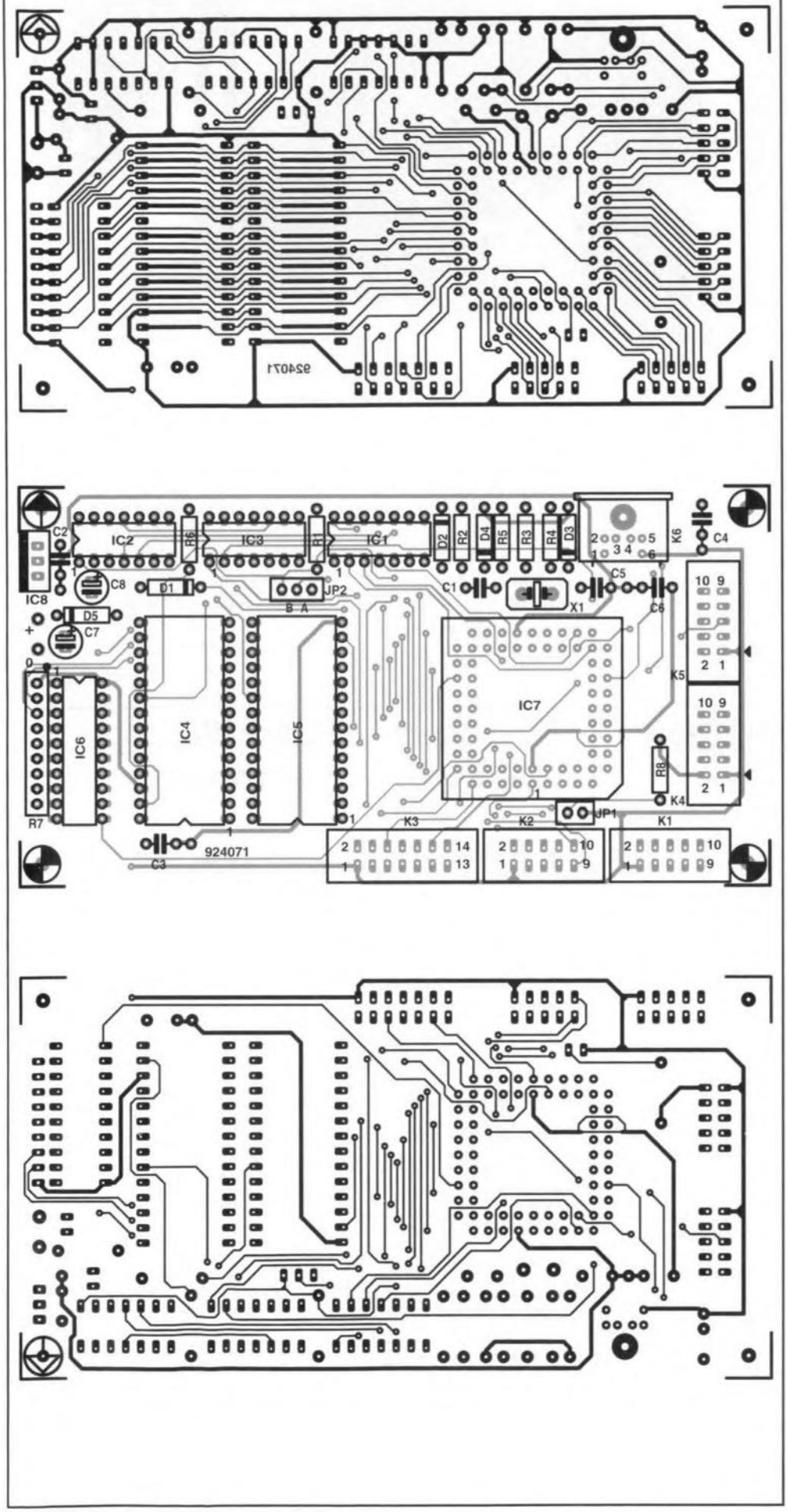
Here is something for microcontroller enthusiasts to grind their teeth on. The 80C552 microcontroller from Philips Components is an upgraded derivative of Intel's 8032. It costs little more than the 8032, yet offers the following extras: (1) eight analogue inputs; (2) a 10-bit A-D converter; (3) a 'Timer2' with many extra features; (4) a 'Timer3' watchdog function; (5) an on-board I²C interface; (6) 16 I/O lines; (7) two pulsewidth modulation outputs; and (8) a 16-MHz clock.

Here, the 80C552 is used in a single-board microcontroller application, which is intended as an experimental system rather than a replacement for an existing processor. The board is aimed at versatility, and accepts EEPROMs, EPROMs, or RAMs, or a combination of these, as memory devices.

The 80C552 board offers a multitude



80C552



of I/O connections for your own applications. All I/O lines, except P0 and P2, are accessible via connectors K_1, K_2, K_4 and K_5. The I²C lines, $P_{1.6}$ and $P_{1.7}$, are taken to a simple I²C interface around a 6-way mini DIN connector, K_6. The TxD and RxD lines are available for TTL-level serial communication via two pins on connector K_5, which also carries read, write, interrupt and timer signals.

Those of you familiar with the 8032 processor will find that the address decoding circuit used here is fairly extensive. Also, unusually, the reset input of the CPU is connected to a bistable. As to the address decoding, this must meet a number of special requirements: it must be possible to read instructions (using PSEN\) as well as read data (using RD\), and write data (using WR\). Further, it is possible to swap the address ranges of the IC_4 and IC_5 positions, with the CS1\ (chip enable) inputs of the respective EPROMs (or EEPROMs) used to select and de-select them, so that the de-selected EPROM hardly consumes power. When the processor is switched to 'idle' mode, its current consumption is only one-third of the normal value, while the CS1\ inputs of both EPROMs are automatically taken high, thus reducing power consumption even further.

Bistable IC_{1a} and XOR gate IC_{2b} serve to swap the positions, 0000H-1FFFH

PARTS LIST

Resistors:
R1;R2;R3;R6;R8 = 10kΩ
R4;R5 = 330Ω
R7 = 8-way 10kΩ SIL

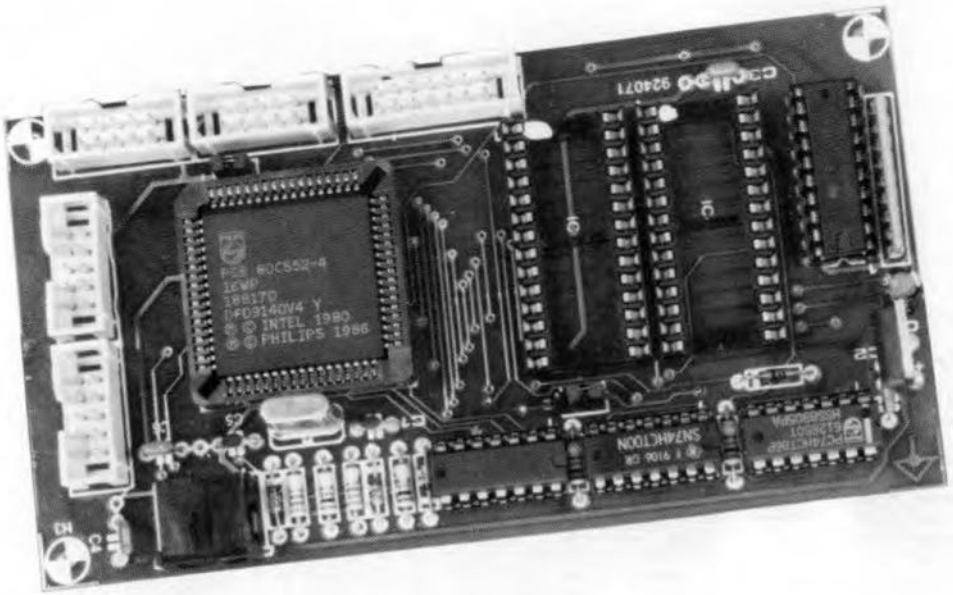
Capacitors:
C1;C5 = 22pF
C2;C3;C4;C6 =100nF
C7 = 10µF 16V radial
C8 = 4µF7 16V radial

Semiconductors:
D1 = 1N4148
D2;D3;D4 = 5.6V 0.4W zener diode
D5 = 1N4001
IC1 = 74HCT74
IC2 = 74HCT86
IC3 = 74HCT00
IC4;IC5 = 27C64 (EPROM) or 28(C)64 (RAM) or 64(C)64 (EEROM)
IC6 = 74HCT573
IC7 = PCB80C552-4WP (16-MHz 68-PLCC)
IC8 = 7805

Miscellaneous:
K1;K2;K4;K5 = 10-way box header.
K3 = 14-way box header.
K6 = 6-way PCB-mount mini DIN socket.
X1 = 16MHz quartz crystal.
68-way PLCC socket.
PCB Type 924071.

and 2000H-3FFFH, of the two EPROMs in the address map. Provided EEPROMs are used, this allows an interesting programming trick: reload the 'upper' EEPROM (i.e., the one with the highest address) with the aid of a program run from the 'lower' EEPROM. *Look, no hands*! No opening of cases, no extracting of EPROMs, and no more time wasted on erasing and reprogramming EPROMs. For instance, the program in the 'lower' EEPROM may read the data supplied by the I²C or the serial input, organize it, and store it into the 'upper' EEPROM. Next, the program causes the T0 line to be pulled low and also stops triggering the watchdog. After some time, the watchdog will force an internal reset, which also pulls RST (pin 15) high for three clock cycles. This works as a clock for bistable IC_{1a}. The bistable copies the level on T0 to its Q output. This enables IC_{2b} to swap the EEPROM address ranges by inverting address line A13, so that the program just loaded into the 'upper' EEPROM is executed.

Because interrupt vectors are always located from address 0000H, address ranges have to be swapped physically rather than in software. However, this swapping is not allowed while the CPU is about its normal business of fetching and executing codes, because an address might change in the middle of an opcode fetch action. At a clock of 6 MHz, this can be done with impunity, but definitely not at a clock of 12 MHz or 16 MHz as used here, which forces us to use the 'hardware reset' trick.

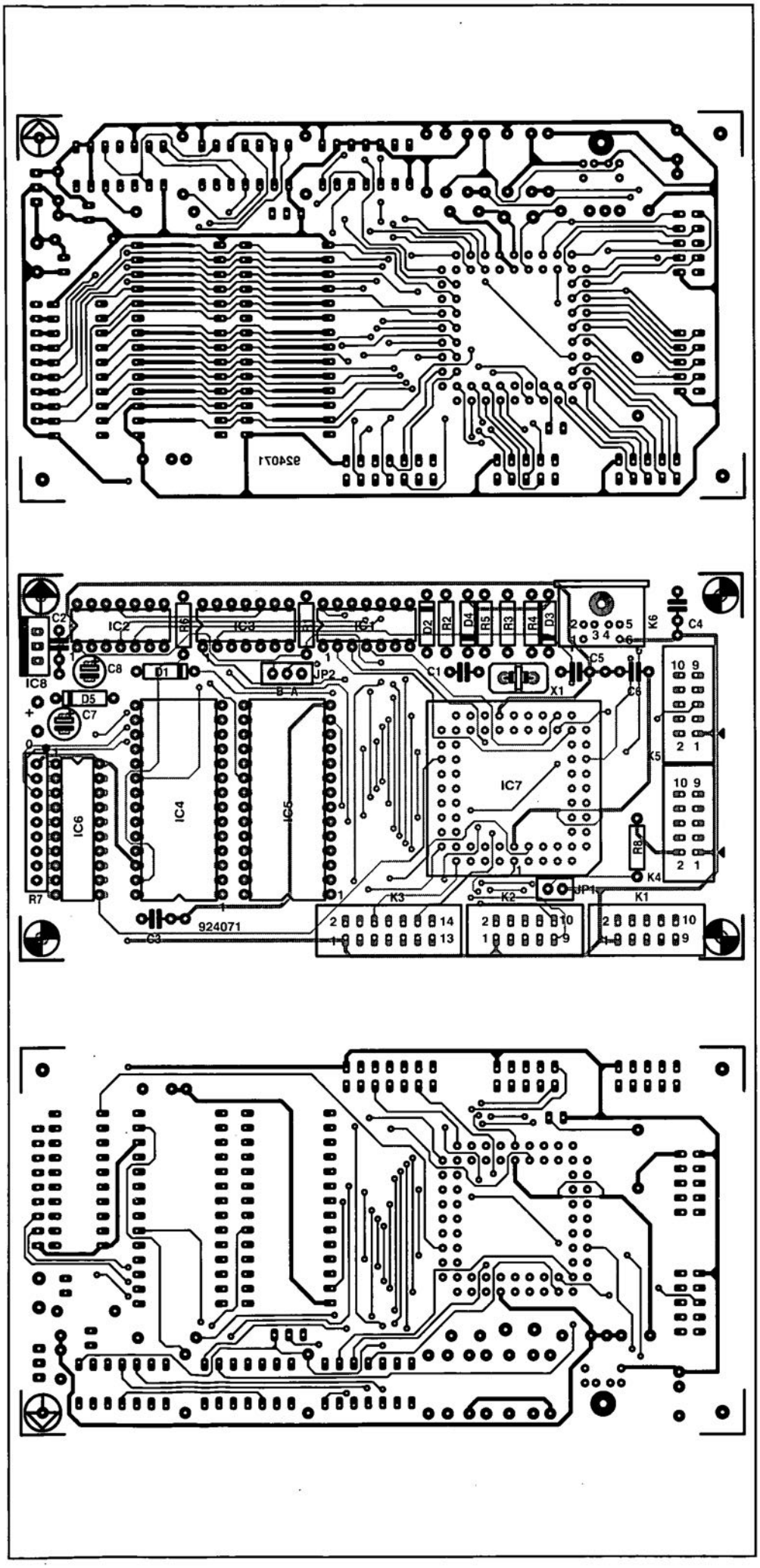


It should be noted that the analogue port, P_5, may function as an input only (it may also be used to accept digital levels). The two I²C pins, SCL and SDA ($P_{1.6}$ and $P_{1.7}$), may be used as an input or an output. Contrary to the other I/O pins, they do not have internal pull-up resistors. Further, it is recommended not to use $P_{3.7}$ and $P_{3.6}$, as this will interfere with the normal opcode fetch operations.

If you intend to connect an LCD (liquid crystal display) module to the 80C552 system, it is best to use the LCD in 4-bit mode, because that allows the display to be connected to 7 port lines only.

A direct bus connection is not possible at clock speeds higher than 10 MHz.

(K. Walraven – 924071)



of I/O connections for your own applications. All I/O lines, except P0 and P2, are accessible via connectors K_1, K_2, K_4 and K_5. The I^2C lines, $P_{1.6}$ and $P_{1.7}$, are taken to a simple I^2C interface around a 6-way mini DIN connector, K_6. The TxD and RxD lines are available for TTL-level serial communication via two pins on connector K_5, which also carries read, write, interrupt and timer signals.

Those of you familiar with the 8032 processor will find that the address decoding circuit used here is fairly extensive. Also, unusually, the reset input of the CPU is connected to a bistable. As to the address decoding, this must meet a number of special requirements: it must be possible to read instructions (using PSEN\) as well as read data (using RD\), and write data (using WR\). Further, it is possible to swap the address ranges of the IC_4 and IC_5 positions, with the CS1\ (chip enable) inputs of the respective EPROMs (or EEPROMs) used to select and de-select them, so that the de-selected EPROM hardly consumes power. When the processor is switched to 'idle' mode, its current consumption is only one-third of the normal value, while the CS1\ inputs of both EPROMs are automatically taken high, thus reducing power consumption even further.

Bistable IC_{1a} and XOR gate IC_{2b} serve to swap the positions, 0000H-1FFFH

PARTS LIST

Resistors:
R1;R2;R3;R6;R8 = 10kΩ
R4;R5 = 330Ω
R7 = 8-way 10kΩ SIL

Capacitors:
C1;C5 = 22pF
C2;C3;C4;C6 =100nF
C7 = 10µF 16V radial
C8 = 4µF7 16V radial

Semiconductors:
D1 = 1N4148
D2;D3;D4 = 5.6V 0.4W zener diode
D5 = 1N4001
IC1 = 74HCT74
IC2 = 74HCT86
IC3 = 74HCT00
IC4;IC5 = 27C64 (EPROM) or 28(C)64 (RAM) or 64(C)64 (EEROM)
IC6 = 74HCT573
IC7 = PCB80C552-4WP (16-MHz 68-PLCC)
IC8 = 7805

Miscellaneous:
K1;K2;K4;K5 = 10-way box header.
K3 = 14-way box header.
K6 = 6-way PCB-mount mini DIN socket.
X1 = 16MHz quartz crystal.
68-way PLCC socket.
PCB Type 924071.

SPEECH/SOUND MEMORY

OKI's Series MSM6372–6375 enable the reproduction of speech or other sound stored in their internal ROM. The capacity of the ROM lies between 128 kbit and 1024 kbit, depending on the type. The type and the sampling frequency specified (4 kHz, 6.4 kHz or 8 kHz) determine the length of the stored speech, which is 4–64 seconds. This time may be divided into 111 words that can be addressed individually.

Each IC contains a 12-bit digital-to-analogue converter (DAC) and a fourth-order low-pass filter. The customer can specify the words that must be stored on the mask-programmable ROM. As an example, the Type MSM6374-007 is programmed to tell the time in English.

Based on this IC, the circuit shown in Fig. 1 is intended to be connected to the I²C I/O card published earlier this year of which the two converters have been omitted. The card then serves as interface between the I²C bus and IC_2.

The wanted word is selected via inputs 10–16. Since the MSM6374-007 contains only words at addresses where 13 is zero, the corresponding input is strapped to earth. This arrangement leaves two of the eight available I/O bits for starting and timing of the words. These bits are available at ST (start input) and NAR (next address request output). Briefly, the control is

- wait until NAR is high;
- key in the address;
- wait not less than 10 seconds;
- briefly render ST low (pulse duration 0.35–350 µs).

Normally the NAR signal indicates that the next address may be keyed in before the entire word has been spoken. This arrangement provides a smooth transition between words or parts of words.

To simplify the control of the synthesizer, the start pulse is not generated by software, but by monoflop IC_{1a}. This stage is triggered by both the first and last transition of the start start signal, which is applied to the trigger inputs via differentiating networks R_5-C_7 and R_7-C_8. The timing diagram in Fig. 2 shows what happens. Every time the computer writes data to IC_2, the software inverts bit P6. It then takes 30 µs before the onset of the start signal, which is 250 µs long. In this way, the control computer can start the 'utterance' of a word in one write operation. Without IC_{1a}, the computer would have to write the address first, then, after 10 µs, the start signal, and finally end the start signal.

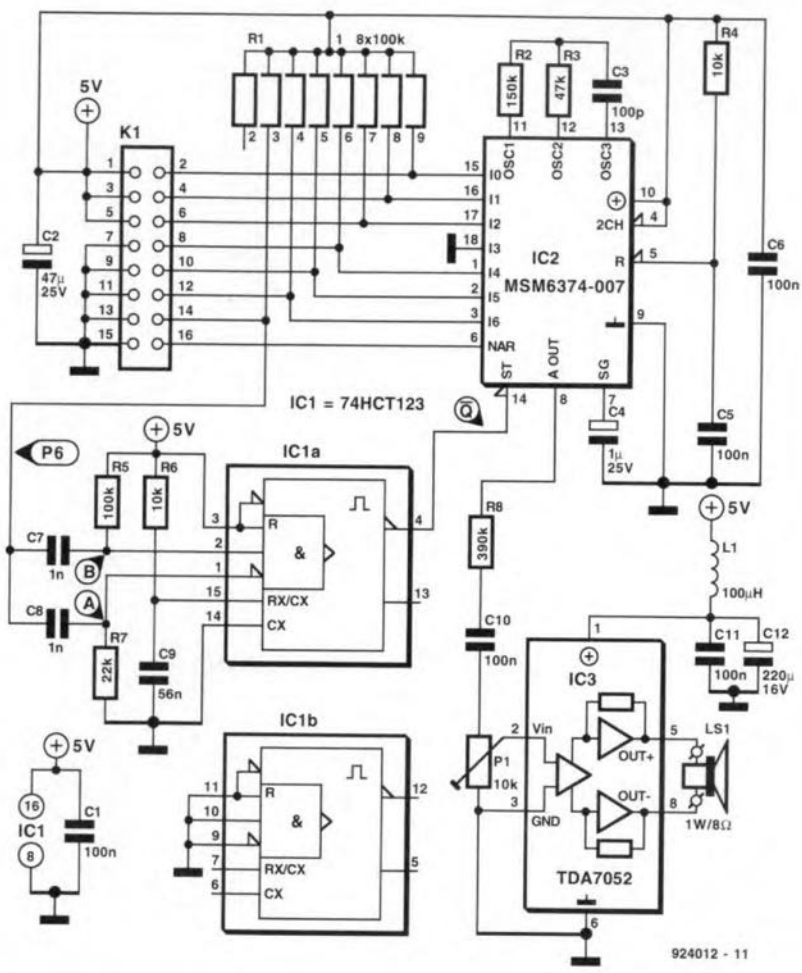
Resistors R_2, R_3, and capacitor C_3, set the oscillator frequency to 64 kHz, resulting in a sampling frequency of 6.4 kHz.

Resistor R_4 and capacitor C_5 provide a power-up reset.

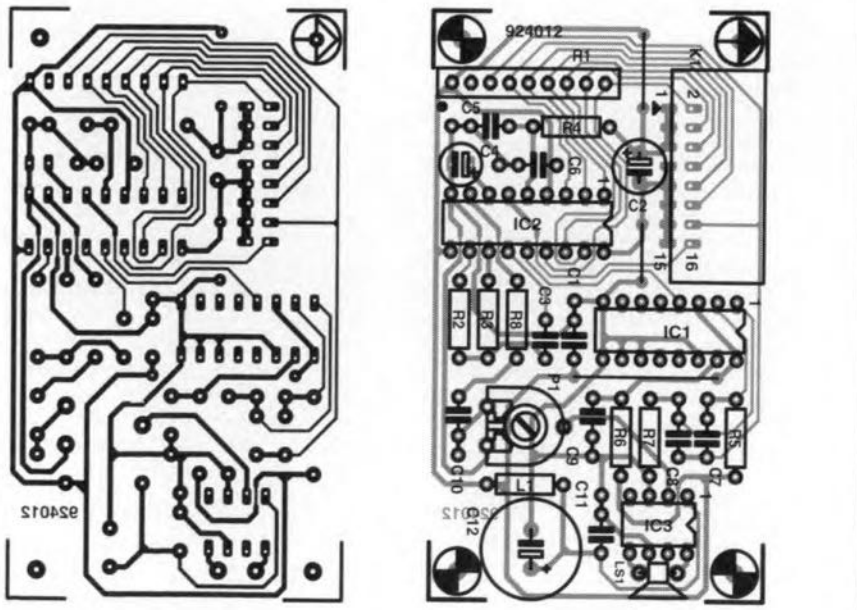
Capacitor C_4, which forms part of the output filter, provides an improvement of the signal-to-noise ratio.

A second channel enables the IC to

1



2



give speech with echo, two tones, or a tone with three different volumes. This facility cannot be used in this application owing to lack of I/O bits. Input 2CH is, therefore, disabled by strapping it to the positive supply line.

The output signal is raised to about 1 W into 8 Ω by integrated bridge amplifier IC_3.

The circuit may be controlled via the computer-to-I^2C interface by software that, once installed, may be enabled by a suitable key combination. It is possible for either the time to be spoken or an alarm time to be set. The use of this software presupposes that the I^2C driver (Type 1671—see p.110) has been installed. When Program 177 is run, it installs itself, after which it is enabled (even if another program is being run) by the simultaneous pressing of keys CTRL and F1. If that combination cannot be used, for instance, because it is used by another program, another combination may be chosen by loading the program with TALKTIME/H. You will then be asked to key in the alternative combination. Note that in the combination the program can recognize only the left-hand shift key.

When the combination has been keyed in, a self-evident menu appears after about a second, provided the screen is not in the graphics mode. In that case, a high tone is emitted, whereupon only functions 'tell time' and 'alarm on/off' are available.

The circuit draws a current of not more than 300 mA.

(OKI application – 924012)

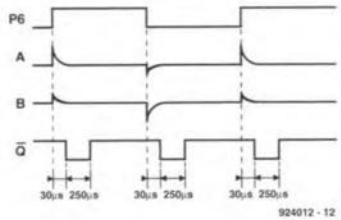
PARTS LIST

Resistors:
R1 = array, 8×100 kΩ
R2 = 150 kΩ
R3 = 47 kΩ
R4, R6 = 10 kΩ
R5 = 100 kΩ
R7 = 22 kΩ
R8 = 390 kΩ
P1 = 10 kΩ preset

Capacitors:
C1, C5, C6, C10, C11 = 100 nF
C2 = 47 µF, 25 V, radial
C3 = 100 pF
C4 = 1 µF, 25 V, radial
C7, C8 = 1 nF
C9 = 56 nF
C12 = 220 µF, 16 V, radial

Semiconductors:
IC1 = 74HCT123
IC2 = MSM6374-007
IC3 = TDA7052

Miscellaneous:
K1 = 16-way box header, right-angled
L1 = 100 µH
LS1 = loudspeaker, 8 Ω, 1 W
Software Type 1771 (see p. 110)

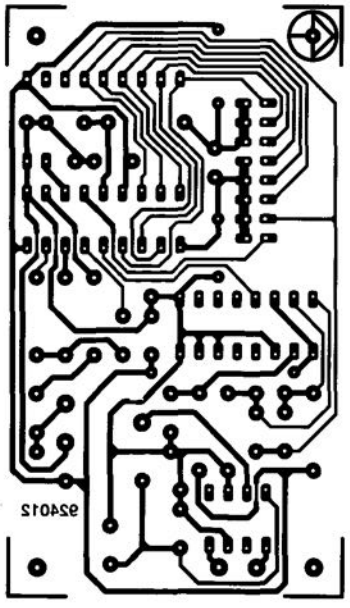


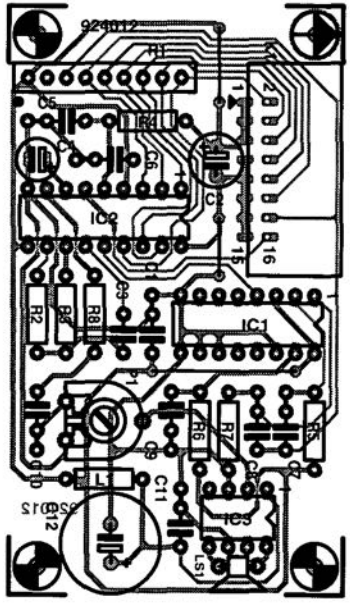
before the entire word has been spoken. This arrangement provides a smooth transition between words or parts of words.

To simplify the control of the synthesizer, the start pulse is not generated by software, but by monoflop IC_{1a}. This stage is triggered by both the first and last transition of the start start signal, which is applied to the trigger inputs via differentiating networks R_5-C_7 and R_7-C_8. The timing diagram in Fig. 2 shows what happens. Every time the computer writes data to IC_2, the software inverts bit P6. It then takes 30 µs before the onset of the start signal, which is 250 µs long. In this way, the control computer can start the 'utterance' of a word in one write operation. Without IC_{1a}, the computer would have to write the address first, then, after 10 µs, the start signal, and finally end the start signal.

Resistors R_2, R_3, and capacitor C_3, set the oscillator frequency to 64 kHz, resulting in a sampling frequency of 6.4 kHz.

2



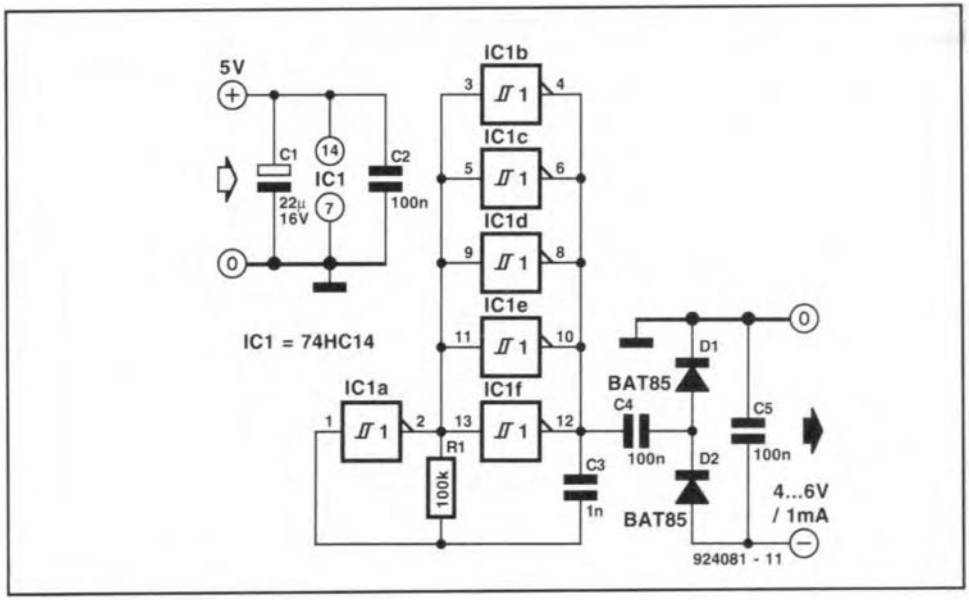


VOLTAGE INVERTER

A negative supply voltage may be obtained easily with the use of a special inverter IC. Such ICs are not always readily available, however. Fortunately, if the current drawn is not excessive, a standard HC-MOS chip may be used. The present circuit is based on a Type 74HC14, which contains six Schmitt triggers, whose combined gates can deliver a fairly high output current. Moreover, such devices can be made to oscillate easily.

Parallel switching is, however, a problem with Schmitt triggers, even if they are contained in the same chip. This problem is particularly acute in the case of slow input signals. In the present circuit this problem is resolved by driving the parallel-switched input via a gate that is not part of the parallel circuits. Since this is also a Schmitt trigger, the output signal has steep (fast) transitions.

The parallel-switched gates together with IC_{1a} form a rectangular-wave generator, whose output frequency is about 125 kHz. The output signal is converted by a charge pump into a negative supply voltage. The diodes used for that purpose are Schottky types which, owing to their low threshold voltage, do not lower the load voltage by as much as silicon diodes.



Under no-load conditions, the output voltage is about 6 V and the IC draws a quiescent current of around 100 µA. When the load current is about 1 mA, the output voltage drops to 4 V. If this voltage can drop even further (down to half the supply voltage), a load current of up to 10 mA is possible. A higher load current or a smaller drop in the output voltage cannot be obtained by raising the value of the capacitors in the charge pump, since the IC cannot cope with this. Note also that the circuit is not short-circuit proof: the IC will not give up the ghost immediately, but it does not take all that long.

(L. Pijpers – 924081)

60 WATT MUSIC AMPLIFIER

This is a robust, no-frills medium power amplifier that is particularly suited to use in 'combo' type portable amplifiers used by guitar players and jazz musicians. The amplifier is a straightforward combination of an integrated audio driver IC, the LM391-80, and a push-pull power output stage designed with bipolar transistors.

A few peculiarities of the design will be discussed. The NTC, which is in thermal contact with the power output transistors, enables the LM391 to switch off the power stage when this gets too hot. The onset point of this thermal protection lies at an NTC current of about 200 µA. The electrolytic capacitor shunting the NTC serves to provide a 'soft start', that is, to prevent a loud click or other disconcerting noise from the loudspeaker when the amplifier is switched on. It may happen that the protection is too sensitive, in which case some experimenting with the value of R_4, or that of the NTC, should be tried.

It is possible to implement feedback in the amplifier by connecting R_{23} to series network C_5-R_7. The latter parts, together with R_{10}, determine the frequency response of the amplifier, which may need adjusting to meet individual requirements. The component values given here will, however, be all right for most applications.

The effect of different values of C_5 and R_7 is simple to measure (or hear) by shorting out R_{23} temporarily. For 4-Ω loudspeakers, R_{23} must be lowered to 0.18 Ω. Unfortunately, the LM391-80 is prone to oscillation, which is suppressed by components R_x, C_6, C_8 and C_9 (in most cases, C_6 may be omitted). Resistor R_x in particular reduces the open-loop gain. If R_x is used, R_y must be fitted to compensate the resulting off-set voltage. Components R_{22} and C_{12} form a Boucherot network that serves to stabilize the amplifier at high frequencies.

The input of the amplifier should be driven by a low-impedance source capable of supplying 'line' level audio signals (0 dB). Network R_1-C_1 attenuates signals above 50 kHz or so.

The quiescent current of the amplifier is set by preset P_1. Set this control to 0 Ω initially, and adjust it until a qui-

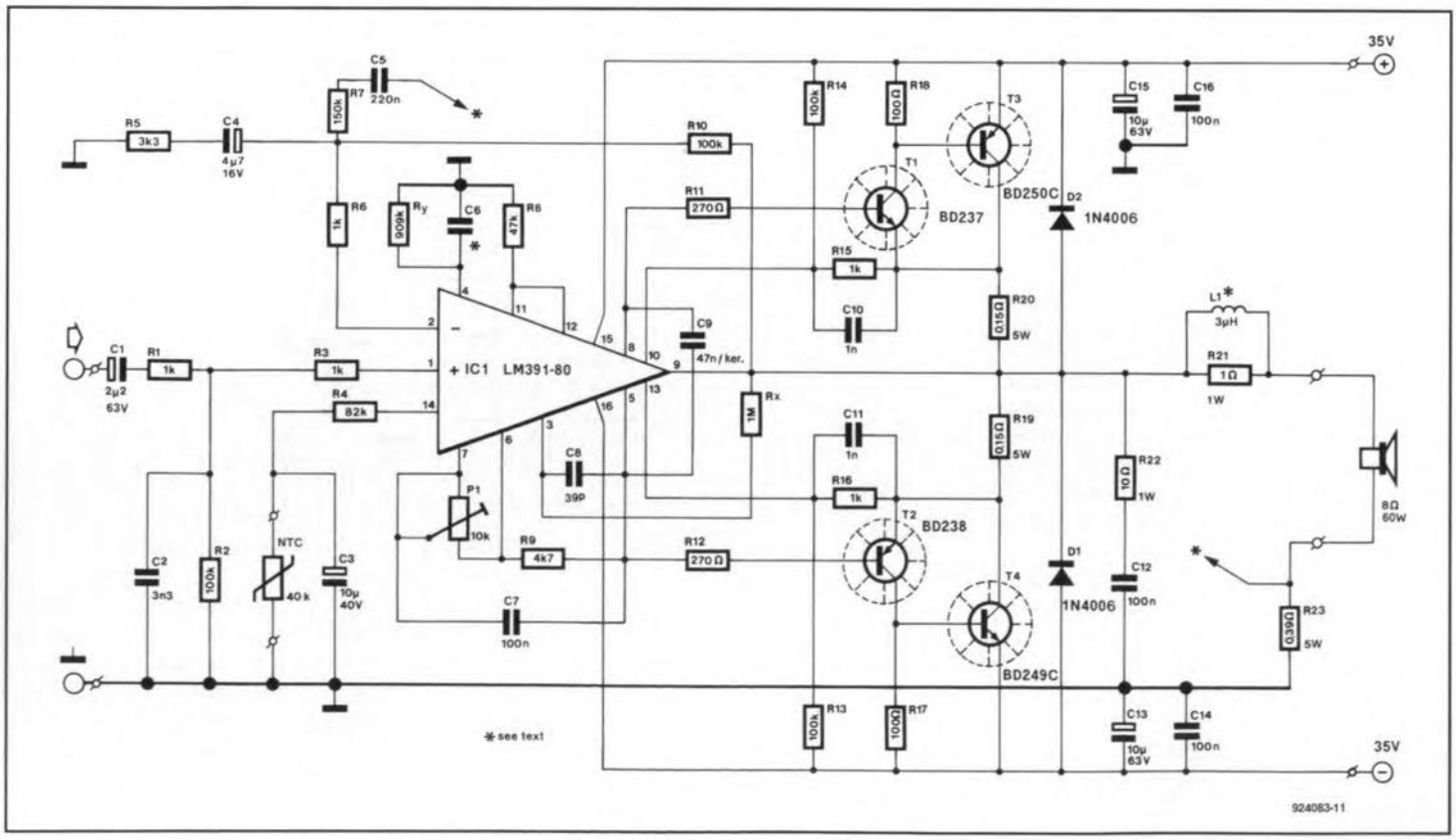
PARTS LIST

Resistors:
R1;R3;R6;R15;R16 = 1kΩ
R2;R10;R13;R14 = 100kΩ
R4 = 82kΩ
R5 = 3kΩ3
R7 = 150kΩ
R8 = 47kΩ
R9 = 4kΩ7
R11;R12 = 270Ω
R17;R18 = 100Ω
R19;R20 = 0Ω15/5W
R21 = 1Ω/1W
R22 = 10Ω/1W
R23 = 0.39Ω/5W
Rx = 1MΩ (see text)
Ry = 909kΩ (see text)
P1 = 10kΩ preset H

Capacitors:
C1 = 2µF2 63V
C2 = 3nF3
C3 = 10µF 40V
C4 = 4µF7 16V
C5 = 220nF
C6 = not fitted (see text)
C7;C12;C14;C16 = 100nF
C8 = 39pF
C9 = 47nF ceramic
C10;C11 = 1nF
C13;C15 = 10µF 63V

Semiconductors:
D1;D2 = 1N4006
T1 = BD237
T2 = BD238
T3 = BD250C
T4 = BD249C
IC1 = LM391-80

Miscellaneous:
L1 = see text
NTC = 40kΩ stud type
Heatsink 1 K/W



escent current of 50 mA flows. This may be increased to 400 mA if you are after low distortion.

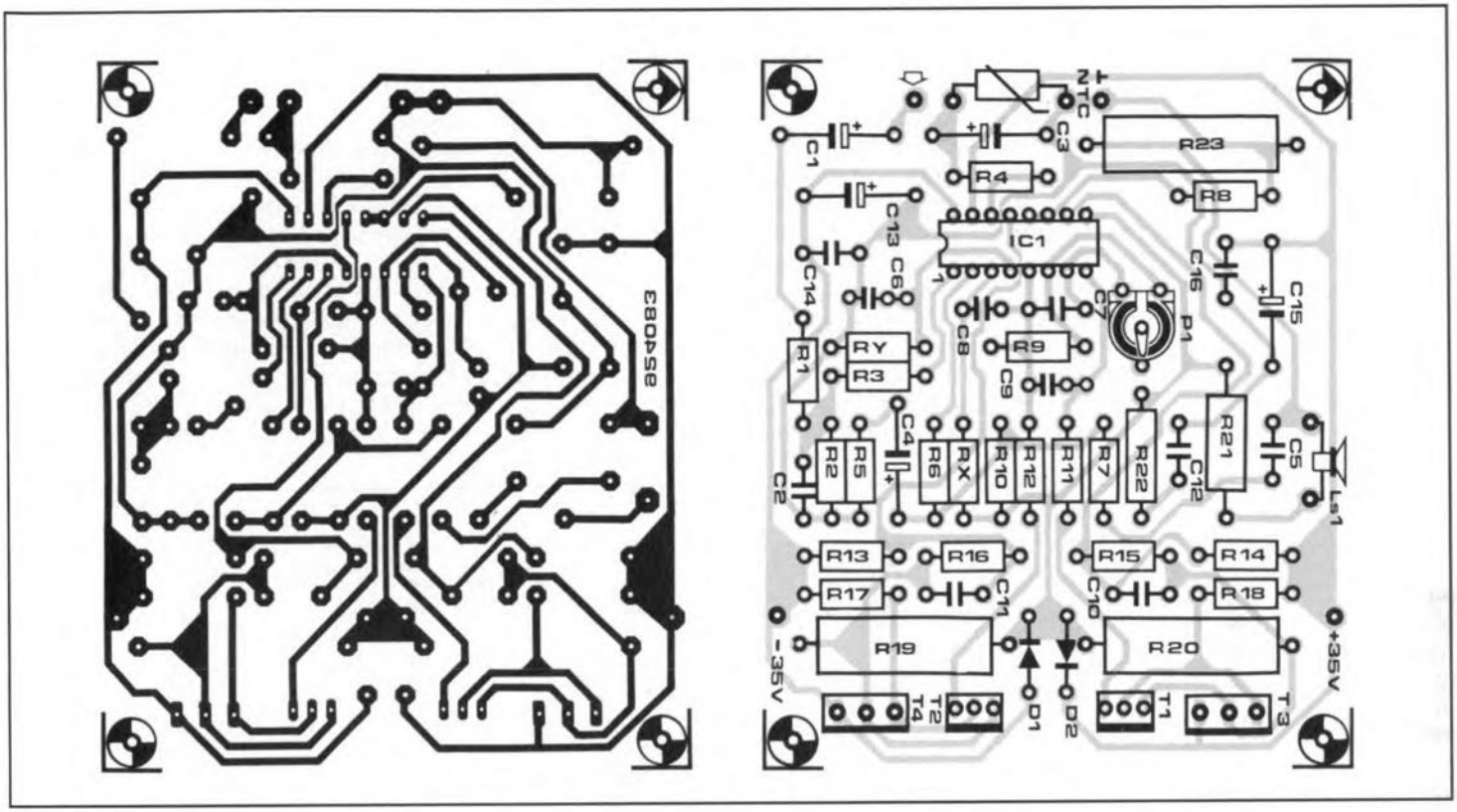
The power transistors are all located at the same side of the PCB so that they can be bolted on to a common heatsink, together with the NTC. The heat sink should be fairly large and have a thermal resistance of 1 K W^{-1} or smaller.

Note that L_1 consists of 20 turns of 0.8 mm dia. enamelled copper wire wound around R_{21}. C_9 is a ceramic capacitor.

Finally, some measured data (supply voltage: ±35 V; R_{23} short-circuited):

- 3-dB bandwidth (8 Ω): approx. 11 Hz to 20 kHz
- THD (transient harmonic distortion) at 1 kHz:
  1 W into 8 Ω: 0.006% (I_q ≈ 400mA)
  1 W into 8 Ω: 0.02% (I_q ≈ 50 mA)
  65 W into 8 Ω: 0.02% (U_{in} = 873 mV)
  80 W into 4 Ω: 0.2% (U_{in} ≈ 700 mV; onset level of current limit)

(W. Teder – 924083)



ESP083

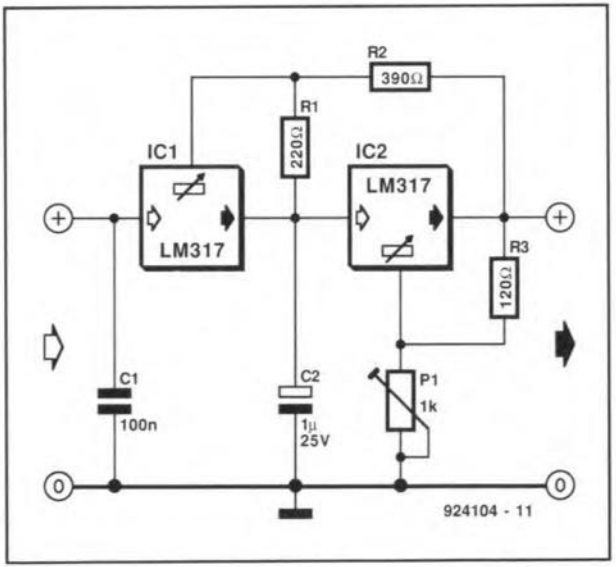
NTC
C1
C3
R4
R23
R8
C13
C14
C6
IC1
C16
C15
P1
C7
C8
C9
R1
RY
R3
R9
R2
R5
C4
R6
RX
R10
R12
R11
R7
R22
R21
C12
C5
C2
Ls1
R13
R16
R15
R14
R17
C11
C10
R18
R19
R20
-35V
+35V
T2
T4
D1
D2
T1
T3

IMPROVED LM317 REGULATOR

Although the properties of the LM317 regulator are excellent, they can be improved by cascading two of these devices. There is then a constant difference between the output voltages of the two regulators and, consequently, a constant voltage across the input and output of IC_2. This arrangement results in an appreciable improvement of the regulating characteristics of IC_2. Moreover, its dissipation is reduced so that the stability of the output voltage with temperature is improved. Other properties, such as the maximum output current of 1.5 A, do not change, of course.

The output voltage, U_o, of the circuit depends on the ratio R_3:P_1 as follows:

$$U_o=1.25(1+R_3/P_1) \quad [V].$$



With values of these components as shown, the output voltage may be varied over the range 1.25–11.5 V. The voltage drop, U_d, across IC_2 depends on the operating point of IC_1 and may be calculated from:

$$U_d=1.25(1+R_2/R_1) \quad [V].$$

With values of these components as shown, U_d=3.5 V. It should be noted that this voltage must not drop below 3.0 V. Moreover, the value of R_2 must be about twice that of R_1, and the minimum drop across the entire circuit must not be lower than U_d+3 V.

The circuit is highly suitable for use as a 5-V power supply. It is, however, important that the direct voltage at the input is not lower than 12 V.This means that the secondary voltage of the mains transformer must be 12 V instead of the usual 9 V.

(L. Lemmens – 924104)

CHARGING TEMPERATURE MONITOR

THE monitor is particularly intended as an aid in the rapid charging of NiCd batteries. Most commercially available fast chargers have no temperature sensor, although temperature is an important factor in the fast charging of NiCd batteries.

According to manufacturers' data sheets, temperatures for various states of a NiCd battery should roughly be: (a) 30 °C when half charged; (b) 37 °C when fully charged; and (c) 48 °C when 20% over-charged.

The monitor is connected in series with the battery and the charger. The temperature is assessed by a couple of NTCs (resistors with a negative temperature coefficient). The output of these devices is compared with reference levels in IC_{1b}–IC_{1d}. The output of comparator IC_{1d} goes low when the temperature—measured by R_{13} and R_{14}—rises above 25 °C, whereupon D_7 lights. The output of IC_{1c} goes low when the temperature reaches 38 °C, whereupon D_8 lights. This signals that the battery is fully charged. Finally, the output of IC_{1b} goes low when the temperature reaches 45 °C, whereupon D_9 lights. This is an alarm signal calling attention to the battery being over-charged. At the same time, T_1 is switched on, whereupon relay Re_1 is energized and its contact disconnects the charging current. The charging current can be reconnected only after the temperature has dropped to well below 45 °C.

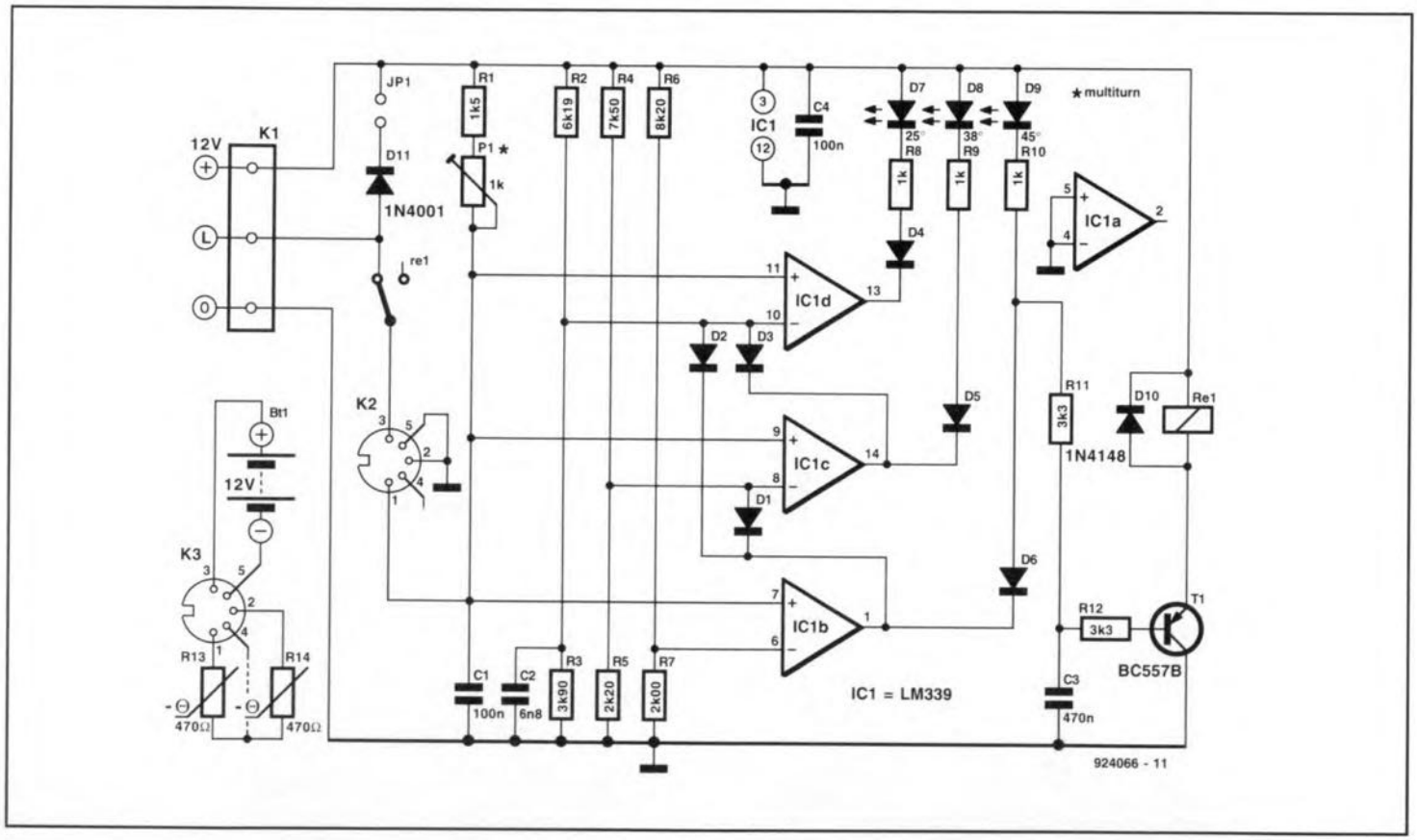
Diodes D_1–D_3 ensure that only one of the three LEDs can light at any one time. The circuit is calibrated with P_1 to make certain that the LEDs light at the correct temperatures.

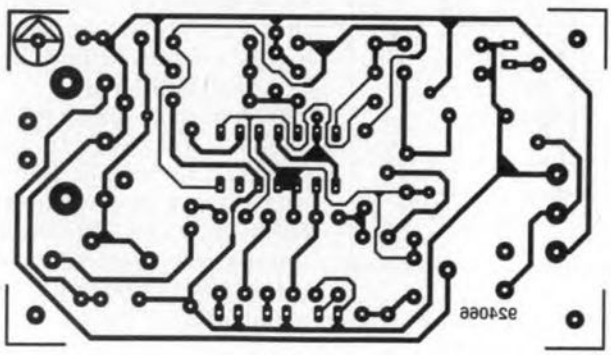
When the monitor is connected to the charger, it is essential that the charging current, originally flowing via K_1, flows via K_2 and K_3. The batteries must, therefore, be connected to K_2 and K_3. The terminals of the NTCs are also coupled to these connectors.

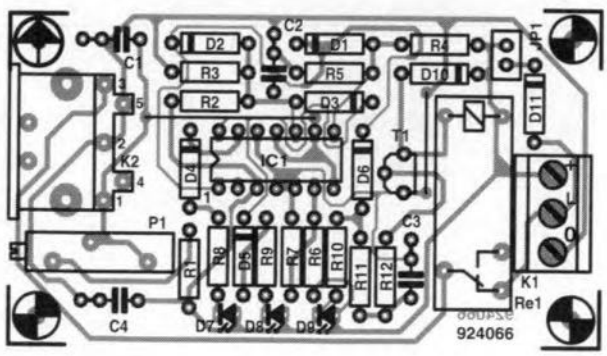
The NTCs must be coupled to the batteries in a manner that ensures good contact. It is good practice to fit them permanently to the batteries.

The supply for the monitor may be taken from the charger, either via the 12 V pin or the L pin. In the latter case, wire link JP_1 must be short-circuited. The monitor draws a current of about 15 mA when the relay is not energized.

Variations in the supply voltage do not affect the monitor since the NTCs are connected in a bridge arrangement.







PARTS LIST

Resistors:
R1 = 1.5 kΩ
R2 = 6.19 kΩ, 1%
R3 = 3.9 kΩ, 1%
R4 = 7.5 kΩ, 1%
R5 = 2.2 kΩ, 1%
R6 = 8.2 kΩ, 1%
R7 = 2 kΩ, 1%
R8–R10 = 1 kΩ
R11, R12 = 3.3 kΩ
R13, R14 = NTC, 470 Ω
P1 = 1 kΩ multiturn preset

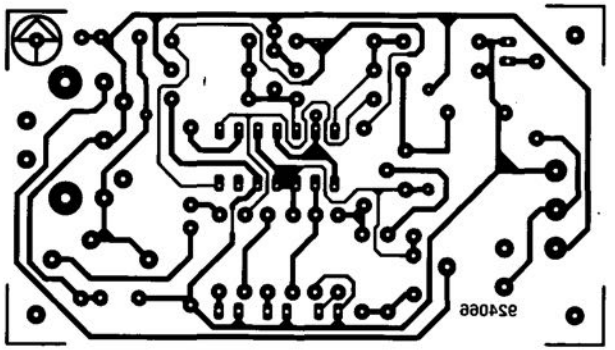
Capacitors:
C1, C4 = 100 nF
C2 = 6.8 nF
C3 = 470 nF

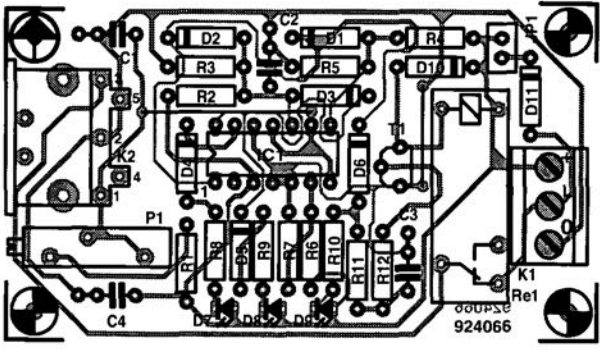
Semiconductors:
D1–D6, D10 = 1N4148
D7 = LED, 3 mm, green
D8 = LED, 3 mm, yellow
D9 = LED, 3 mm, red
D10 = 1N4001
T1 = BC557B
IC1 = LM339

Miscellaneous:
K1 = 3-way terminal block, pitch 5 mm
K2 = 5-pin DIN socket
K3 = 5-pin DFIN plug
Re1 = 12 V relay for PCB mounting

As shown, the monitor is intended for use with 12 V batteries. It can be modified for use with 6 V batteries merely by using a 6 V relay instead of a 12 V type.

(C. Millasson – 924066)


924066


D2
R3
R2
C2
D1
R4
R5
D3
D10
D11
C1
K2
IC1
T1
D6
P1
C3
K1
Re1
C4
924066

DIGITAL PATTERN GENERATOR

During the construction and testing of digital circuits, there is often a need of an accurately defined bit pattern. The generator described here uses an EPROM to store the bit information for the desired pattern.

When switch S_1 is pressed, a given pattern is generated once; seven different patterns can be generated simultaneously. The eighth data output of the EPROM is used to mark the end of a pattern.

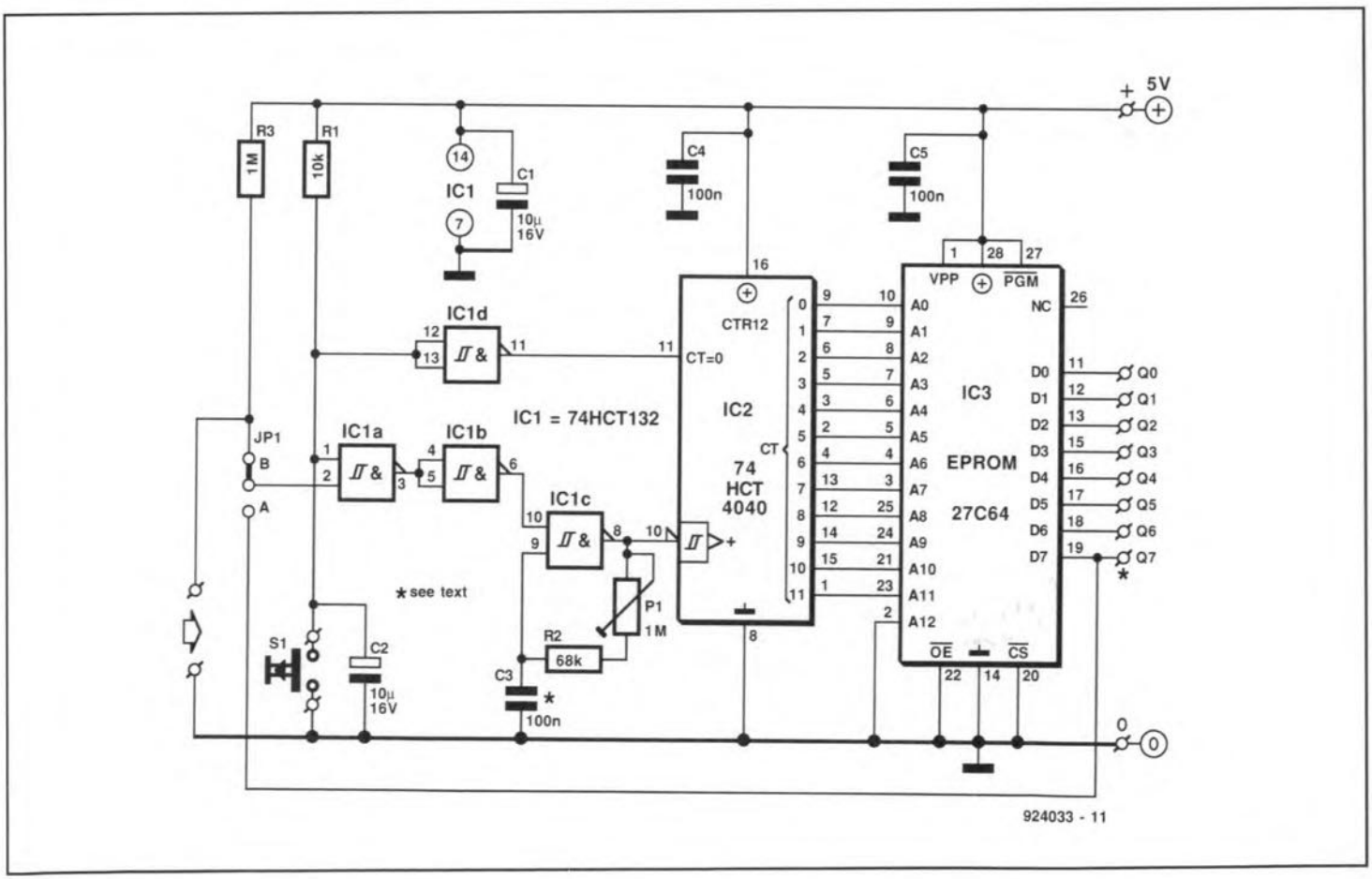
After S_1 has been pressed, gate IC_{1d} arranges the resetting of address counter IC_2. Gate IC_{1c}, which is connected to the input of the address counter, functions as a start-stop oscillator that is switched by two NAND gates. These gates are designed to keep the oscillator disabled until the switch is released. Only then are pulses fed to the address counter. The frequency range of the clock can be varied to individual requirements by altering the value of C_3. With values as shown, the frequency can be set with P_1 between 15 Hz and 150 Hz.

When bit patterns are being generated, data line D7 must be logic high. At the end of the pattern, this line goes low, whereupon the clock is stopped.

The maximum length of a bit pattern in the circuit as shown is 8191 clock pulses (8×1024–1 stop pulse). If link JP_1 is set to position B, an external stop pulse can be used.

The circuit draws a current of about 8 mA.

(G. Kleine – 924033)



PLL SYNTHESIZER FOR TV RECEIVERS

Modern TV tuners normally contain means to scale down the VCO (voltage-controlled oscillator) signal. The one used in the proposed synthesizer is a Philips Type UV816/6456, whose scale factor can be set to 64 or 256. It operates over the low VHF band, the high VHF and hyperbands, and the UHF band.

The proposed circuit is based on a Siemens Type SDA3002 frequency synthesizer IC that may be controlled by a computer. It works exclusively with a :64 scaler. This is ensured by leaving pin 15 of the tuner open.

Network R_2-C_2-C_1 forms the filter for the phase-locked loop—PLL. The level of the charging current for the filter is determined by the value of R_1 and bit 14—see the table. In the prototype, both low and high levels of current gave stable PLL operation, but the loop reacted faster with a high current.

The SDA3002 has a unique oscillator for providing a reference frequency. The frequency of crystal X_1 is scaled down internally by 4096, so that the reference frequency for the PLL is 976.5625 Hz.

The PLL is set by entering a data word into the SDA3002, for which a clock, CPL, an enable signal, PLE, and a data signal, IFO, are needed. At each trailing transition (edge) of the clock, a bit is shifted into the IC, provided PLE is high—see Fig. 3. Only when PLE has become low will the PLL accept the entered data into a latch.

A total of 18 bits must be shifted into the chip. Fourteen of these contain the frequency setting of the PLL. The 15th bit determines the charging current. When this bit is high, the current is $10I_r$, where I_r is the reference current; when it is low, the charging current is I_r. The 16th bit controls the NORM output. The final two bits determine the state of the band selector outputs: pins 4–7, see the table.

The first 14 bits are computed fairly easily once the desired channel frequency, f_c, the intermediate frequency, *i.f.* (=38.9 MHz), the scale factor, z_a (=64) of the tuner, and the reference frequency, f_r, of the PLL are known. The overall scale factor, z, is then

$$z=(f_c+i.f.)/z_a f_r.$$

The result should be rounded to the nearest whole number, and then split into two parts (IC_1 contains a dual-mode prescaler) to obtain the bits needed by IC_1. The nine most significant bits—MSBs—are calculated by dividing z by 32 and ignoring the digits following the decimal point. The remainder of z:32 forms the five least significant bits—LSBs.

As an example, assume that channel 29 is wanted; the carrier frequency is then 535.250 MHz. The scale factor is

$$z=(535.25+38.9)/64\times976.5625=$$

$$=9186.$$

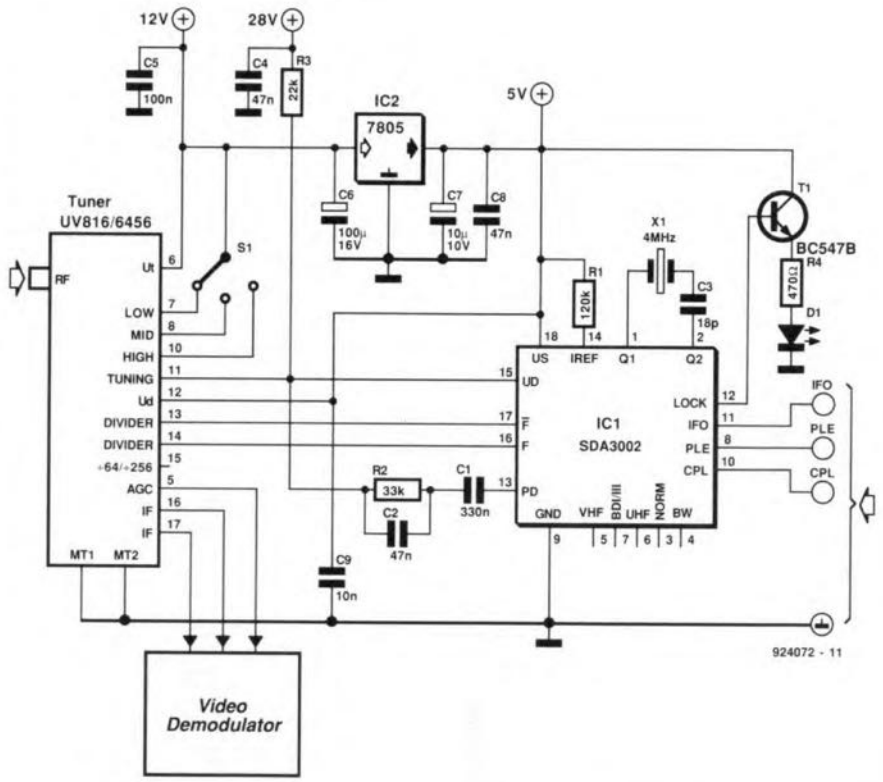
Dividing that number by 32 gives 287, remainder 2. In binary form, that is (MSB)10001111100010(LSB). However, the data must be entered in inverted form, that is, a logic 1 corresponds to low and a logic 0 to high. Taking the LSBs first, the following levels must appear at the data input

HLHHHLLLLLHHHL.

Diode D_1, which is controlled by the LOCK output via T_1, then lights to indicate that the PLL is locked.

The maximum tuning voltage is determined by the supply voltage, which is connected to the loop filter via R_3. The UV816 needs a tuning voltage of 0.7–28 V. The SDA3002 can handle a maximum voltage of 33 V at its UD output.

1



IFO bit 2^{14}	pump current
L	Ir
H	$10I_r$

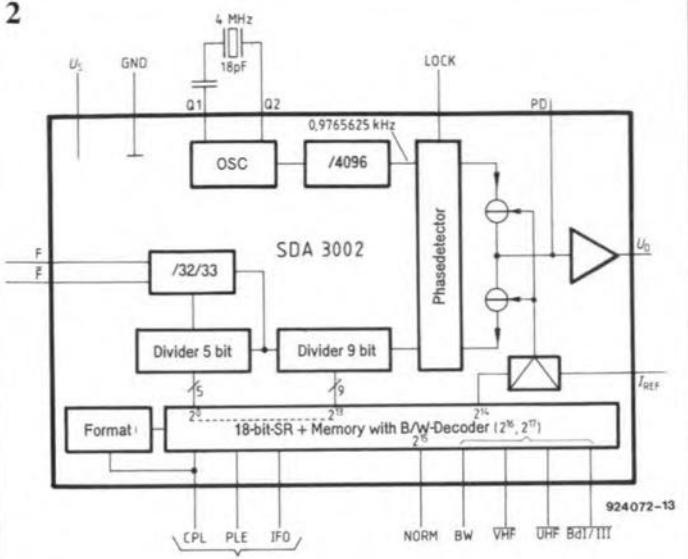
IFO bit 2^{15}	NORM output
L	L
H	H

IFO bit 2^{16} 2^{17}	band selection output			
	band I/III	VHF	UHF	BW
L L	H	H	L	H
L H	H	L	H	H
H L	L	L	H	H
H H	L	L	H	L

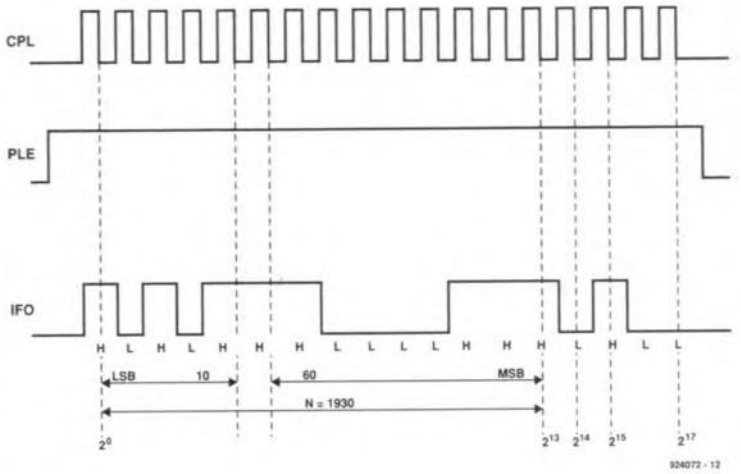
Two further supplies are needed: 12 V for the tuner and 5 V for IC_1 and the prescaler in the tuner. Since the combined current drain of IC_1 and D_1 (lighted) is only 29 mA, the 5 V rail is easily obtained from the 12 V supply via 5 V regulator. That regulator can at the same time provide the current—about 25 mA—for the prescaler in the tuner. Additionally, the 12 V supply must provide the current for the tuner, which in case of the UV816 is about 85 mA. A total current of some 140 mA is, therefore, required.

(T. Giesberts – 924072)

2

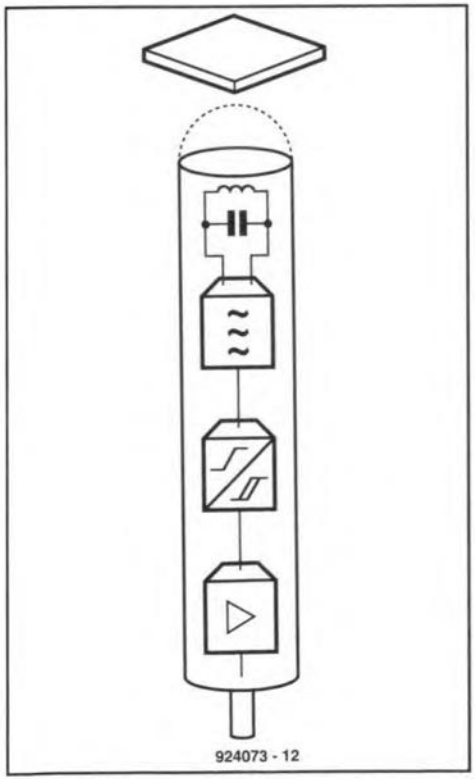


3



INDUCTIVE PROXIMITY SWITCH

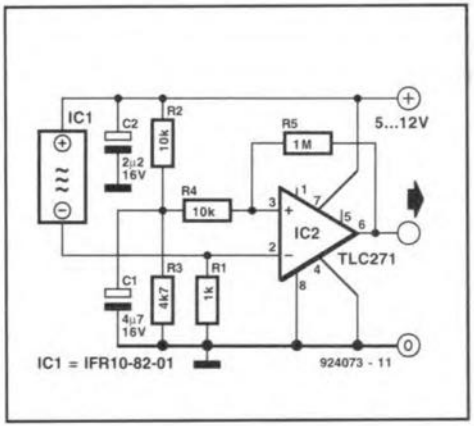
Inductive proximity switches are used, for instance, for measuring motor speeds or determining the position of metal objects. They do not suffer from mechanical wear or sparking contacts . The latter is particularly important in spaces where explosive materials are stored.



Virtually all commercial proximity switches are constructed as shown in Fig. 1. An inductor in the resonant circuit of an oscillator serves as the sensor. If a conducting object enters the magnetic field of the coil, eddy currents are set up in the inductor. This damps the resonant circuit so that the voltage across it drops. This voltage drop is monitored with a Schmitt trigger. When the object gets very close to the inductor, and the voltage across the circuit drops sufficiently, the Schmitt trigger changes state. The trigger is followed by an output stage.

The sensor, IC_1, used in the present circuit translates the approach of an object into a falling current through the sensor. In the absence of an object, the current is about 4 mA; when an object is at a distance of 4 mm from the sensor, the current is only 1 mA.

The sensor current is converted into a voltage by R_1. This voltage is applied to the non-inverting input of Schmitt trigger IC_2. Actually, since the hysteresis is small, IC_2 functions more as a comparator that likens the voltage across R_1 to that across R_3. When an object is within the proximity limit of 5 mm of the sensor, the potential across R_3 is larger than that across R_1, whereupon the output of IC_2 becomes logic high.



The potential across R_3 is dependent on the supply voltage, of course, but over the range of supply voltages stated in the diagram, it is always greater than the smallest drop across R_1 and always smaller then the largest drop across R_1. This ensures correct switching of IC_2 in all situations.

The only quantity affected by the supply voltage is the output potential of the circuit.

The sensor is a Type IFR10-82-01 from Baumer Electric. It has a diameter of 10 mm and is 5 mm long.

(K. Mossbauer – 924073)

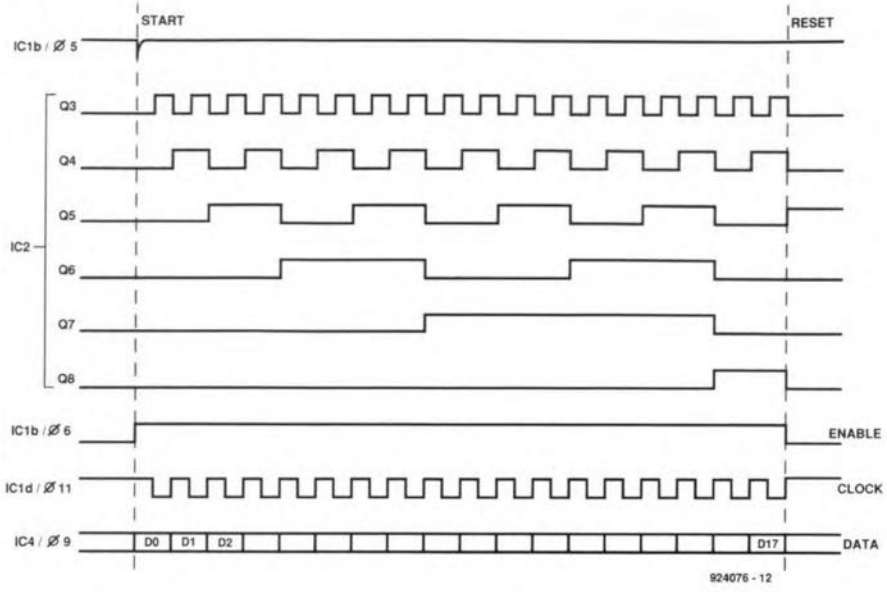
SERIAL DATA GENERATOR

The data generator offers a simple means of testing a circuit.There is no need of software for some microprocessor and all the components are readily available. The design is based on the timing of a Type SDA3002 circuit. In contrast to the two-wire I²C format, a three-wire connection is used. If only one fixed data word needs to be sent, DIP switches S_2 and S_3, and the eight-fold pull-down resistor arrays, may be omitted; the inputs of IC_3 and IC_4 are then held at fixed levels.

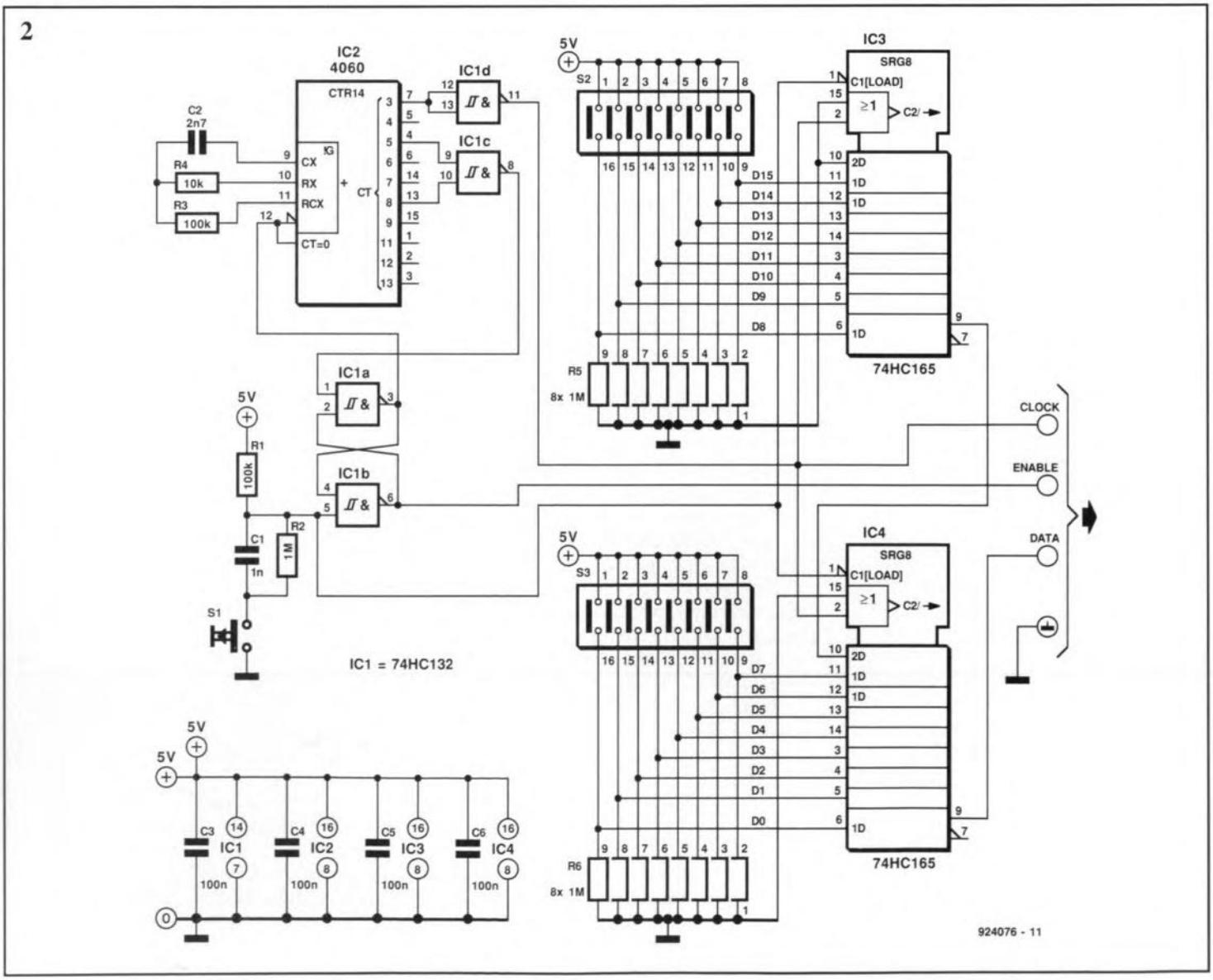
The generator is based on two cascaded shift registers, IC_3 and IC_4, that are used as 16-bit parallel-to-serial converters.

The clock is provided by IC_2, which is started by setting bistable $IC_{1a,b}$ with press button switch S_1. When this switch is pressed, a 100 µs pulse is applied via differentiating network R_1-C_1 to the set input of the bistable. The capacitor is discharged via R_2. The pulse duration is not changed by keeping S_1 depressed; this is necessary because if it were to exceed

1



2



a half clock period, the timing would go astray. The output of IC_{1b} is the ENABLE signal for the circuit to be tested.

The start pulse is used also to load the logic levels set with the DIP switches on to shift registers. The registers accept the parallel data as long as the signal at their pin 1 is low. This is another reason that the start pulse has to be short.

The start pulse begins the entire test cycle—see the timing diagram in Fig. 1. Output 2^3 (Q3, pin 7) of IC_2 is inverted by IC_{1d} to provide the clock for the shift registers. This ensures that D0 is present at the output for an entire clock period (1.25 ms).

After output 2^3 of IC_2 has been high 18 times, the bistable is reset and the enable line is pulled low by IC_{1c}, which is connected to outputs 2^5 (Q5, pin 4) and 2^8 (Q8, pin 13) of IC_2. This completes the cycle.

In this example, 18 bits are shifted. The two MSBs are determined by the serial input (pin 10) of IC_3. If this input is high, D16 and D17 are '1'. If these bits are required to be variable, one or two additional D-type bistables, connected as shift registers, must be added.

The current drawn by the generator, determined primarily by the pull-down resistors, is very low: if all bits are high, it is about 80 µA. After S_1 has been pressed, the oscillator is started briefly, which doubles the current.

(T. Giesberts – 924076)

TEMPERATURE-FREQUENCY CONVERTER

THIS little circuit converts temperature measured by an NTC (negative temperature co-efficient) resistor into a digital signal. The resistance of the NTC, which is an inverse function of the ambient temperature, determines the frequency of an oscillator built around the familiar TLC555 timer. The astable circuit is designed to give a pulse repetition frequency (p.r.f.) of about 250 Hz at 25 °C that rises with temperature. The non-linear relationship between temperature and oscillator frequency is not a problem here, because it is relatively simple to 'straighten' by arithmetic operations performed by a computer or a microcontroller system.

Basically, three temperatures are measured, and the corresponding oscillator frequencies stored as reference points, which serve to interpolate other values in between.

The converter is built from SMA (surface-mount assembly) components on the printed circuit board shown here. It is, however, possible to use a standard NTC in position R_1.

To ensure fast response to temperature changes, the completed PCB is fitted into a small metal tube with a diameter of 13 mm or larger. Great care should be taken to isolate the board and the components from the metal tube; if necessary, use heat-shrink sleeving! The tube is sealed hermetically with potting compound or two-component resin glue, through which three wires are passed: + supply; output signal; ground.

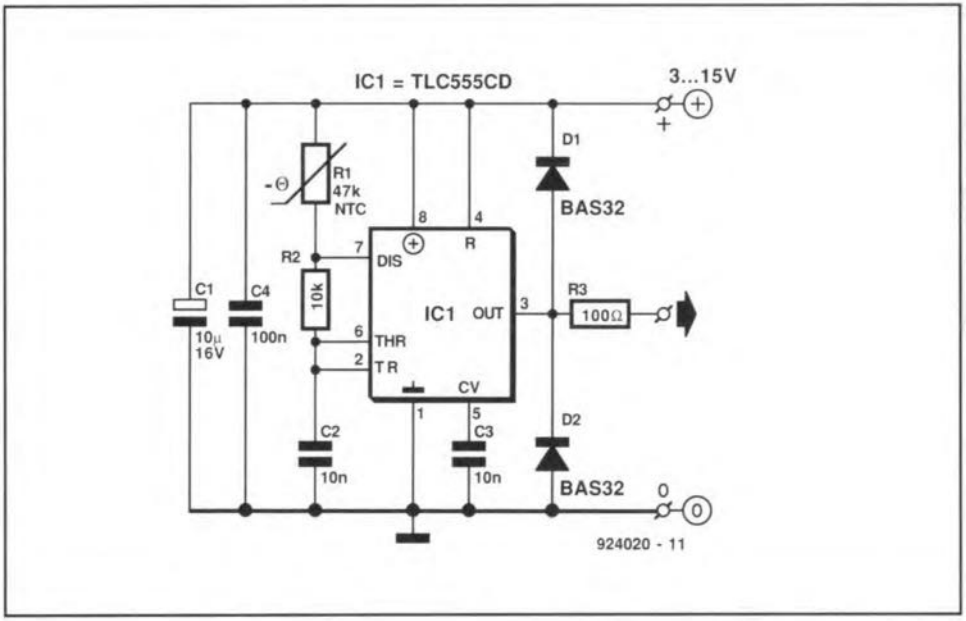
Current consumption of the converter is smaller than 1 mA.

The multifunction measurement card for PCs (Ref. 1) is perfect for processing the converter output signal. Use is made of the frequency meter input and the program modules found in the Turbo Pascal library 'PMEASURE.PAS' on diskette ESS1751—see p. 110, and in Borland's 'Numerical Toolbox', which provides some handy interpolation routines.

(U. Kunz – 924020)

Reference:

"Multifunction measurement card for PCs", *Elektor Electronics* January and February 1991.



PARTS LIST

(all parts surface-mount assembly)

Resistors:

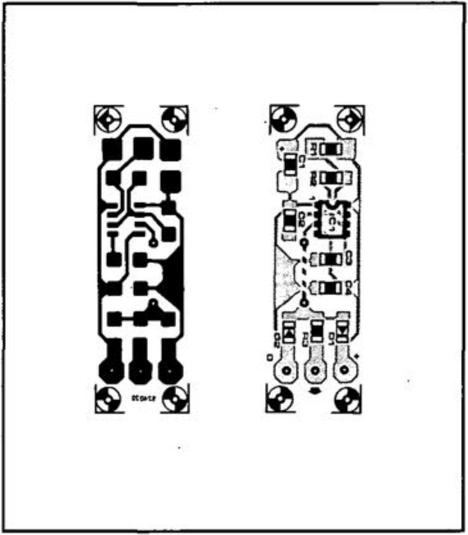
R1 = 47kΩ NTC
R2 = 10kΩ
R3 = 100Ω

Capacitors:

C1 = 10µF 16V
C2;C3 = 10nF
C4 = 100nF

Semiconductors:

D1;D2 = BAS32
IC1 = TLC555CD


R1
R2
C1
IC1
C2
C3
C4
D2
R3
D1
0
+

MAINS-POWER-ON DELAY

This circuit provides a simple means of implementing a 'soft-start' on heavy mains loads. Basically, this is achieved with the aid of high-power series resistors and a relay. The circuit also enables the load to be switched on with a small (light-duty) switch.

Two relays are used to connect or bypass a series of power resistors inserted between the mains 'live' wire and the load. The 'soft start' is achieved by first connecting a resistor between the mains and the load, and then short-circuiting the resistor again so that the full mains voltage is applied to the load (equipment). The purpose of 'soft' switching is to prevent fuses blowing as a result of very high surge currents.

The relay coils are connected in series; the reactance of capacitors C_1 and C_2 keeps the current through them at about 27 mA. The direct voltage across the coils is 48 V. When the delay is switched on with S_1, relay Re_2 comes on well after Re_1 because its coil is shunted by two large electrolytic capacitors, which take some time to be charged from the current source formed by the mains and capacitors C_1 and C_2. When Re_2 is energized, its contact short-circuits the power resistors.

The simplicity of the circuit gives rise to a minor disadvantage: some time must be allowed between switching off and switching on again to enable C_4 and C_5 to discharge. Depending on the length of the switch-on delay required, the values of C_4 and C_5 may be changed a little. It should be noted, however, that the surge current is limited to about 5 A (at a mains voltage of 240 V) by R_3-R_6, and that the resulting dissipation equals about 1 200 W in four 5-watt resistors! Therefore, when a longer switch-on delay is wanted, higher-wattage resistors (the PCB can accommodate fairly large types, which may be fitted vertically) must be used.

The current drain of the circuit is practically that of the two relay coils in series, that is, about 27 mA. The current through the neon lamp is negligible.

The specified relays have contacts rated at 16 A. If there is reason to fear that the PCB mounted terminal blocks and

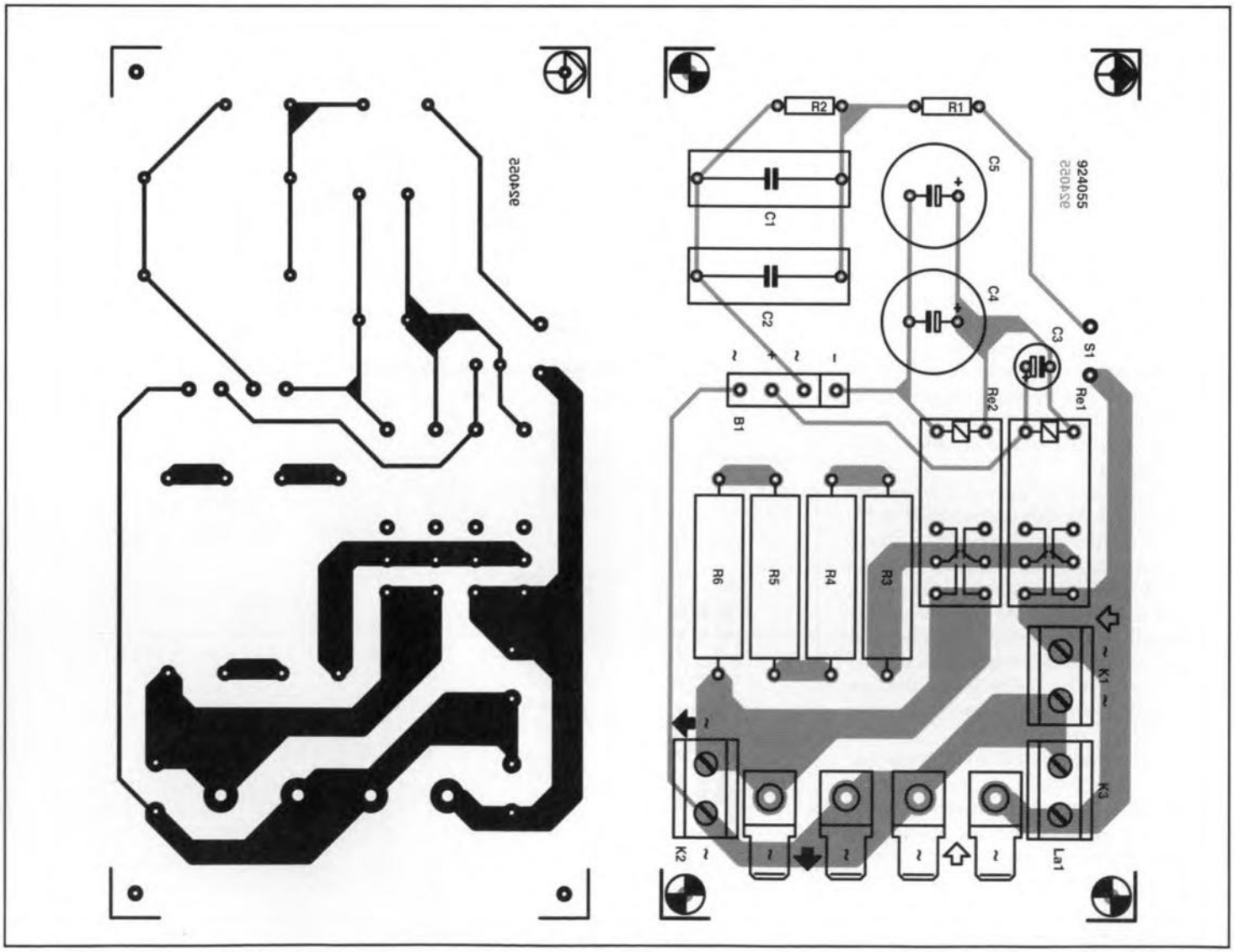
PARTS LIST

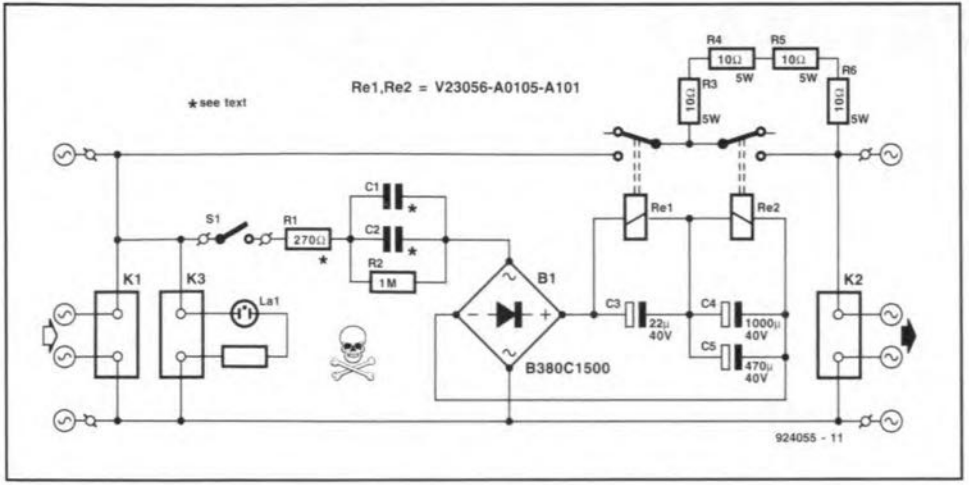
Resistors:
R1 = 270Ω
R2 = 1MΩ
R3-R6 = 10Ω 5W

Capacitors:
C1 = see text
C2 = see text
C3 = 22µF 40V radial
C4 = 1000µF 40V radial
C5 = 470µF 40V radial

Semiconductors:
B1 = B380C1500 (380V piv, 1.5A)

Miscellaneous:
K1;K2;K3 = 2-way PCB terminal block, pitch 7.5mm.
S1 = on/off; mains-rated 1A.
Re1;Re2 = V23056-A0105-A101 (Siemens).
La1 = chassis-mount neon lamp with integral resistor.
4 spade (fast-on) screw-on type plug for PCB mounting.





their solder connections are not up to the load current, parallel-connected spade terminals ('fast-on' type) should be used instead.

Finally, the values of some components depend on the mains voltage and frequency as follows:

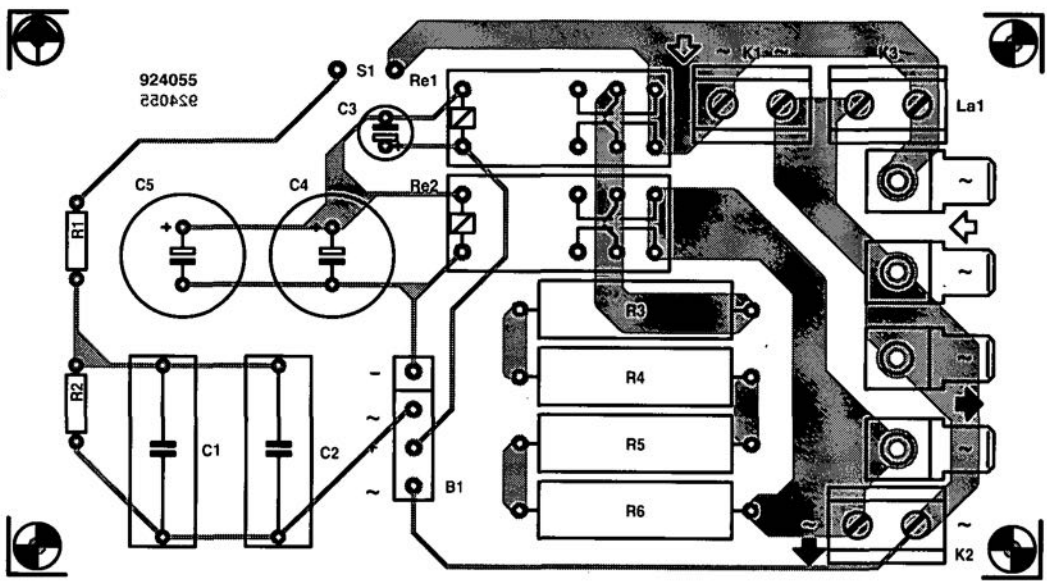
220V, 50Hz: C_1=330 nF; C_2=220 nF
230V, 50Hz: C_1 = 470 nF; C_2 = not fitted
240V, 50Hz: C_1 = 470 nF; C_2 = not fitted
(Capacitor working voltage: 630 VDC /250 VAC)

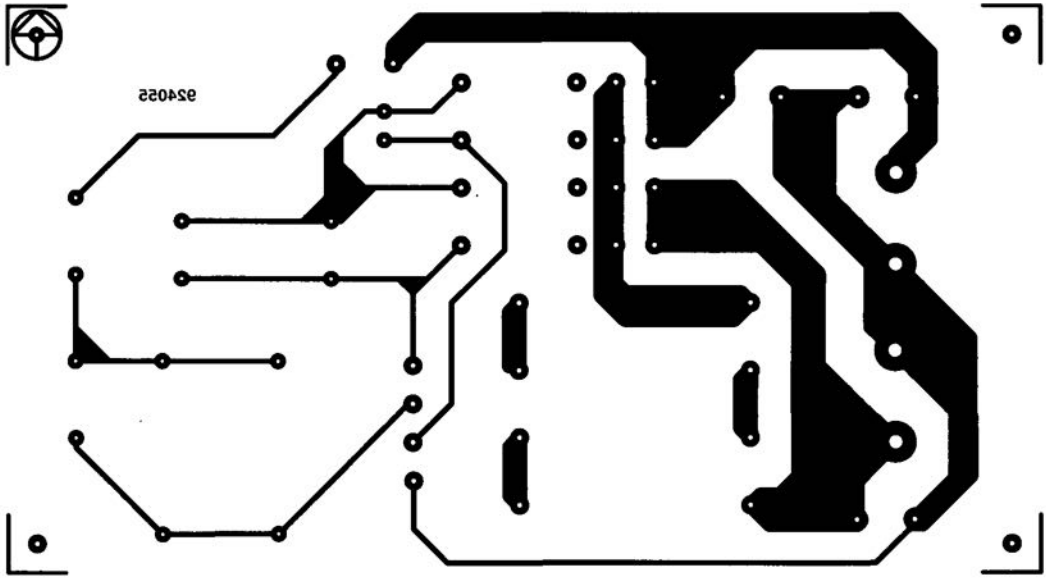
110V, 60Hz: C_1 = 680 nF; C_2 = 470 nF; also R_1 = 120 Ω.
(Capacitor working voltage: 400 VDC /130 VAC)

WARNING

This circuit is connected directly to the mains, and carries potentially lethal voltages. Never work on the circuit, or adjust it, while it is connected to the mains. Observe all precautions relevant to working with equipment or components connected to the mains.

(T. Giesberts – 924055)


924055
S1
Re1
C3
C5
C4
Re2
R1
R2
C1
C2
R3
R4
R5
R6
B1
K1
K3
La1
K2


924055

CAPACITANCE METER

The simple capacitance meter described here is able to measure capacitances between 100 pF and 1 µF over five ranges.

The circuit consists of a variable oscillator, a scaler and a measuring stage.

The oscillator is based on an inverter contained in a Type 74HC14 and generates a frequency, f, that is inversely proportional to the capacitance between terminals C_X. Roughly,

$$f=1.2RC_X,$$

where R depends on the position of S_1. With values as shown, the frequency lies between 240 Hz (C_X=1 µF) and 12 kHz (C_X=100 pF).

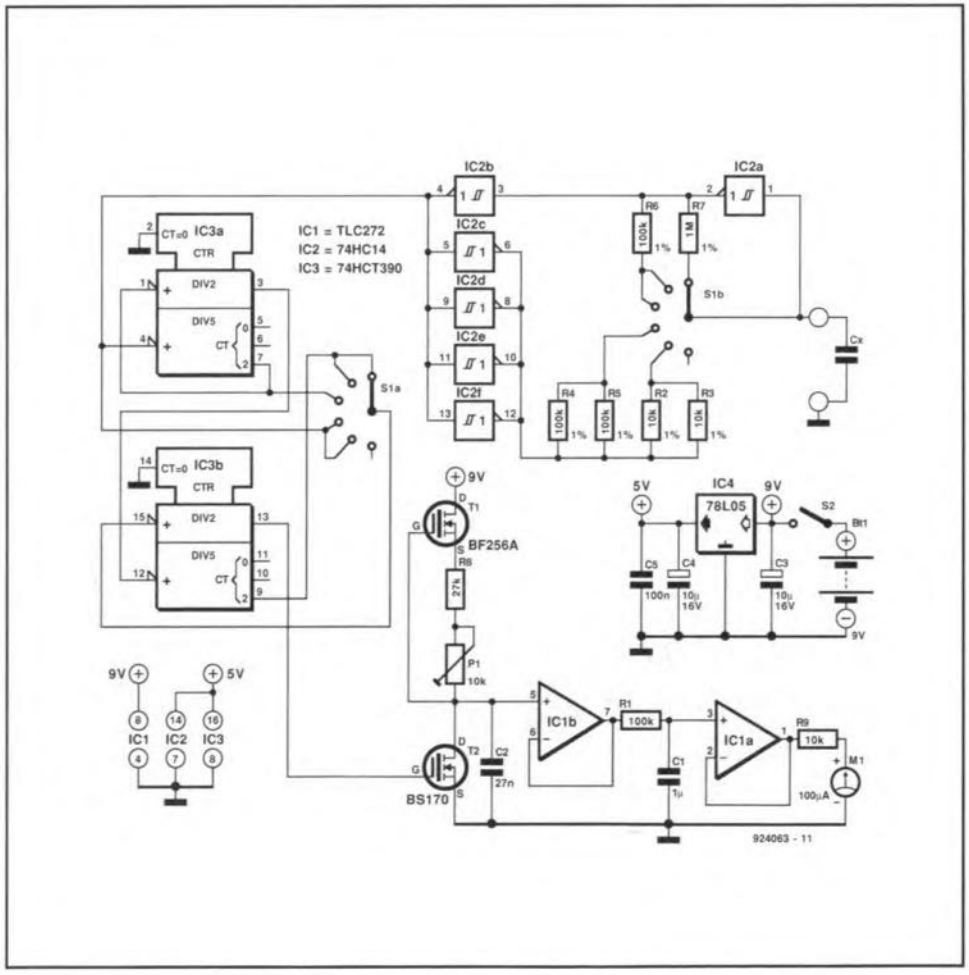
Scaler IC_3 divides the output frequency of the oscillator in a manner which ensures that the maximum output frequency in each range is 120 Hz.

The measuring stage is driven by current source T_1. During one half of each period of the output signal of IC_3 capacitor C_2 is charged via T_1. During the other half of the period T_2 is switched on by the signal, so that C_2 is short-circuited. In this way, the maximum potential across C_2 depends on the frequency of the signal. The potential is buffered by opamp IC_{1b} and integrated by R_1-C_1. The resulting direct voltage is used to deflect the meter via opamp IC_{1a}.

The circuit is calibrated by connecting a known capacitance of about 100 nF (0.1 µF) across the measurement terminals and adjusting P_1 so that the meter reading corresponds to the capacitance.

Since normally the meter is used only occasionally, it may be powered simply by a 9 V PP3 (6F22) battery.

(R. Shankar – 924063)



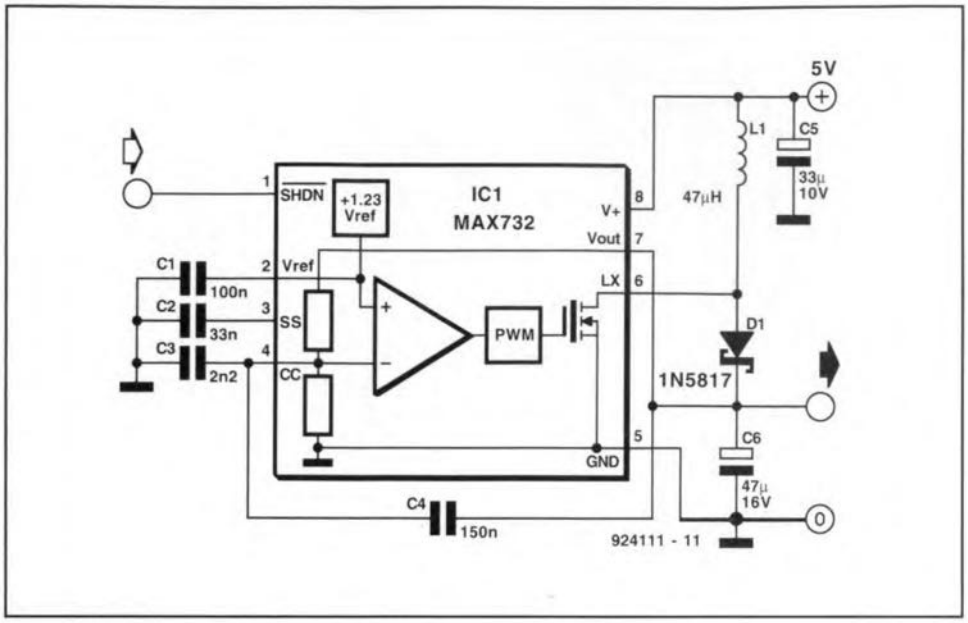
FLASH EPROM CONVERTER

Flash-EPROMs are becoming increasingly popular, in spite of their being harder to reprogram than EEPROMs. That difficulty is, however, countered by their lower price, greater density and higher programming speed.

Maxim, a specialist manufacturer of all sorts of small converter, produces a special IC for generating the necessary programming voltage of 12 V at 50 mA: the MAX732.

The MAX732 contains virtually everything to make a mini switch-mode power supply. Its input voltage requirement is 5 V, from which it produces an output of 12 V. Since that output is needed only during programming, it may be disabled via the shutdown input (pin 1).

A problem encountered in producing switch-mode supplies is the availability of certain passive components, particularly the inductor. That used here is the Sumida Type CD54-470KC, which is available from a number of retailers and also from Maxim dealers as Type MAX-L001. If neither of these can be obtained, however, a triac choke may be used, but that will lower the efficiency of the converter to some extent. It is always possible to add or remove turns if the inductance is incorrect. Bear in mind that the inductance is proportional to the square of the number of turns.



Diode D_1 must be a Type 1N5187 as indicated or equivalent; note that a 1N4001 is not fast enough.

The prototype delivered 12 V and an output current, I_o, of up to 200 mA, more than enough for a flash-EPROM. The current drawn from the 5 V supply was about $2.4I_o$.

Use a single earthing point and decouple the IC directly at its pins.

(Maxim application – 924111)

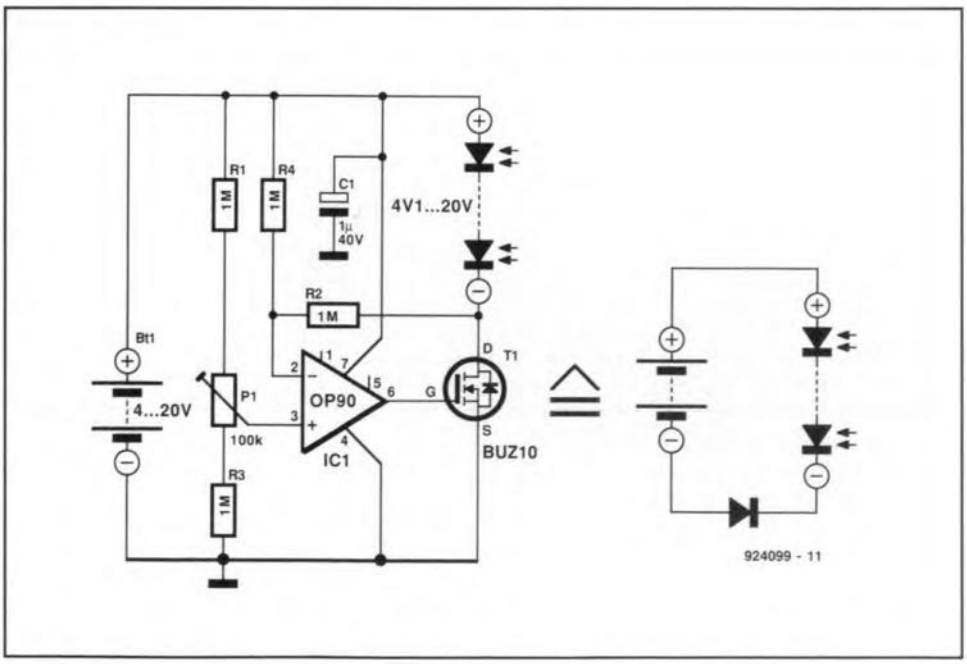
The subscription rates are on page 112 this month

SOLAR-CELL SUPPLY

The simplest solar-cell supply system consists of three parts: a diode, a solar-cell panel, and a rechargeable battery. The diode prevents the battery being discharged through the solar panel when no or little sunlight falls on to the panel. Although the diode is usually a Schottky type, the forward drop of this type may cause an appreciable loss of energy. Since the low-drop diode on page 52 can avoid most of this loss, it has been incorporated in the present circuit.

The opamp draws only a tiny current: on average 20 µA. Although it can operate with a supply voltage of as low as 1.6 V, the gate of T_1 requires at least 3.0 V to be switched on. For that reason, the nominal battery voltage is specified as 4.0 V.

To align of the circuit, replace the solar panel by a variable regulated power supply with its current limiting set to a value that is safe for the battery. Set the power supply output to a level that is 0.1 V higher than the current battery voltage. Next, adjust P_1 so that the output of IC_1 just becomes logic high. Finally, check with an ammeter that the battery is not being discharged when the power supply voltage is set to below the current battery voltage.



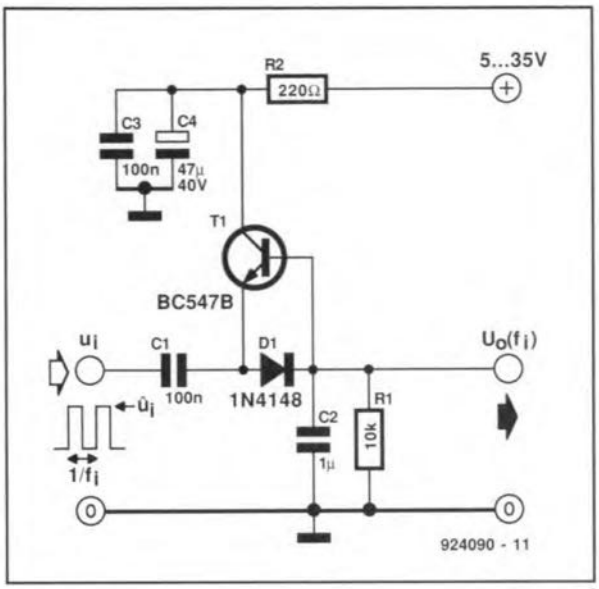
(B. Zschocke – 924099)

DISCRETE FREQUENCY-VOLTAGE CONVERTER

Although there are a number of ICs available that convert frequency to voltage, this can also be done with discrete components as shown in this circuit. Such a simple design has, of course, its limitations: the input signal must be a square wave, must have a constant amplitude, and be provided by a low impedance source (≤50 Ω).

The circuit is called a transistor pump and is related to the charge pump that is used, for instance, in a voltage doubler or voltage inverter. Here, the added transistor arranges for C_1 to be charged very rapidly (U_i=low) when the left-hand side of that capacitor is pulled toward zero because of u_i. The right-hand side of C_1 is thus clamped to a potential of $U_{C2}-U_{BE}$. This means that the circuit is not dependent on the pulse width of the input signal. During the leading transition (edge) of U_i the charge on C_1 is transferred to C_2, which discharges through R_1.

The transfer function of the circuit is derived from the balance in which the increase of U_o during a leading transition (edge) must be equal to the voltage reduction caused by R_1 in each period. This yields the following formula



$$U_{o(fi)}=(\hat{u}_i-0.7)R_1C_1f_i.$$

With component values as shown in the diagram, the output voltage increases by about 4.3 mV Hz^{-1} if the level of the input signal is 5 V. The speed with which the output voltage reacts depends on the time constant of the circuit:

$$\tau=R_1(C_1+C_2).$$

Since the value of both R_1 and C_1 is fairly large, the reaction is not very fast. There are a number of applications where that does not matter, however.

The ripple on the output voltage may be calculated from

$$\hat{u}_r=(\hat{u}_i-0.7)C_1/(C_1+C_2).$$

With values as before, the ripple is 400 mV.

The supply voltage for the circuit must be at least 2 V higher than the output voltage at the highest input frequency to be measured. The circuit draws a current of not more than a few mA.

Filter R_2-C_3-C_4 smooths current peaks during the charging of C_1 and thus limits the RF interference the circuit produces.

The output must be terminated into a high impedance (digital voltmeter or buffer). If that is not possible, a high-value terminating resistor (≥10R_1) should be used.

(A. de Zwaluw – 924090)

synoniem voor A.A. de Veel

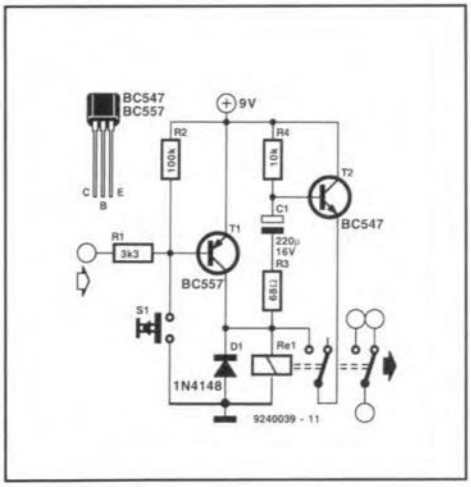
PULSE-OPERATED RELAY

With the aid of a few components, a standard relay can be made to change state every time a pulse is applied (or a switch is pressed).

When the relay is not actuated, transistor T_1 is off because its base and collector are at the same potential via R_2. Capacitor C_1 is charged via R_4, R_3 and the relay coil. When a short pulse (logic zero, shorter than 0.5 s) is applied to the input, or S_1 is pressed, T_1 conducts and the relay is energized. The relay contact changes state, whereupon T_2 also delivers current to the relay coil. Capacitor C_1 is then discharged until its potential is equal to the base-emitter voltage of T_2.

When the pulse ceases, or the switch is released, T_1 is off again, but the relay remains energized by T_2.

A slightly longer input pulse is needed



to deactuate the relay: it needs to be long enough for C_1 to be discharged completely (or very nearly so) via R_3. When the switch is released, or the input becomes high again, T_1 stops conducting. Simultaneously, C_1 is charged again, so that within a short time the base current of T_2 drops to nearly zero.; T_2 then switches off and the relay is deenergized.

Short pulses at the input have no effect when the relay is actuated.

If fairly long pulses are input with the relay inoperative, the circuit functions as a standard relay that is actuated almost immediately by the pulse and is disabled as soon as the pulse ceases.

The hold voltage of the relay should be not more than half the supply voltage. The lower the hold voltage, the shorter the pulse required to actuate the relay can be.

(K. Lorenz – 924039)

SINGLE IC TIMER

Timer chip ICM7250 from Maxim enables a very simple timer to be designed. The IC has eight programmable inputs for connecting to, say, two thumb wheel switches. Units are set in BCD code on the four lowest inputs, pins 1–4, and tens on the highest, pins 5–8. Thus, the user can select any time between 00 and 99 units.

The length of each time unit is determined by P_1-R_2-R_3-C_1. In this particular application time units of one second have been assumed. Other units are easily selected by a few small changes.

According to the relevant data sheet, the maximum overall resistance value of the timing network must not exceed 22 MΩ, while the value of the capacitor must not be smaller than 10 pF. Note that if longer units are set, capacitors with small leakage currents must be used.

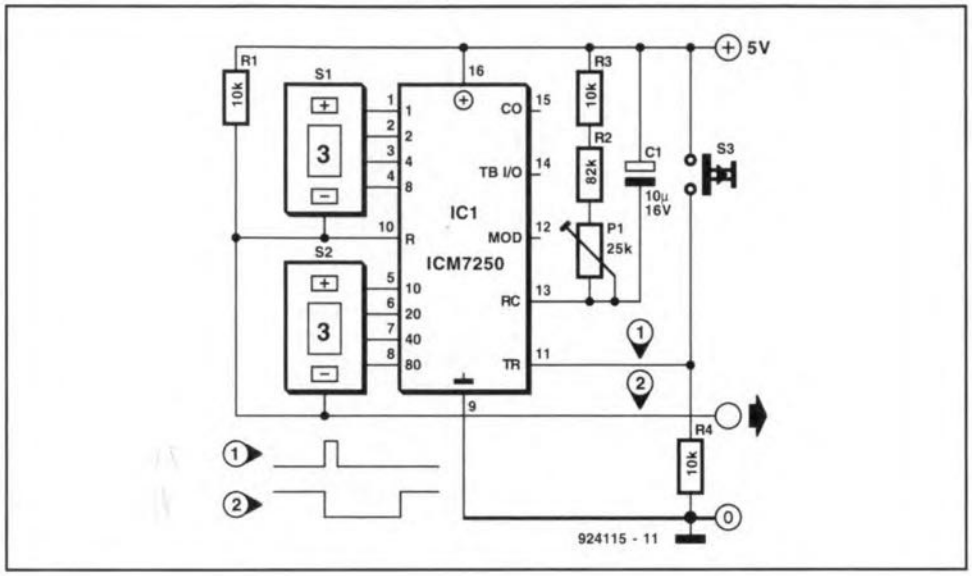
When switch S_3 is pressed, an internal bistable is reset and the counter is started. The output of IC_1 (pin 10) then changes state (becomes low). After the elapsing of the set number of time units, the output becomes high again.

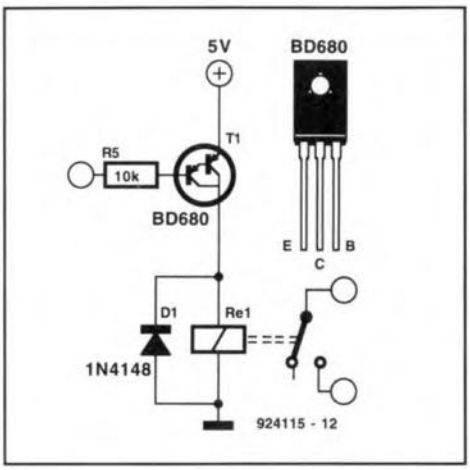
The supply voltage for the timer may be 2–9 V, in spite of the data sheet stating that up to 16 V is permitted. In the prototype, the output was permanently high with supply voltages of 9.5–16 V.

The relay connected to the output is switched by a power transistor, T_1. This darlington can switch currents of up to 4 A.

The circuit itself draws a current of only 1 mA.

(A. Rietjens – 924115)





MIDI (CABLE) TESTER

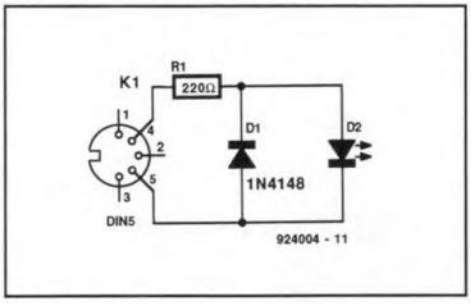
A tester for MIDI connections is a real asset for many constructors. The one presented here is kept fairly simple as shown in the diagrams.

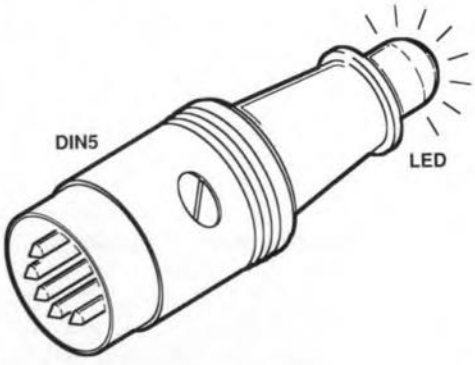
The LED shows whether MIDI data are present where the tester is connected. Since these data consist of very short pulses, the LED must be a high-efficiency type.

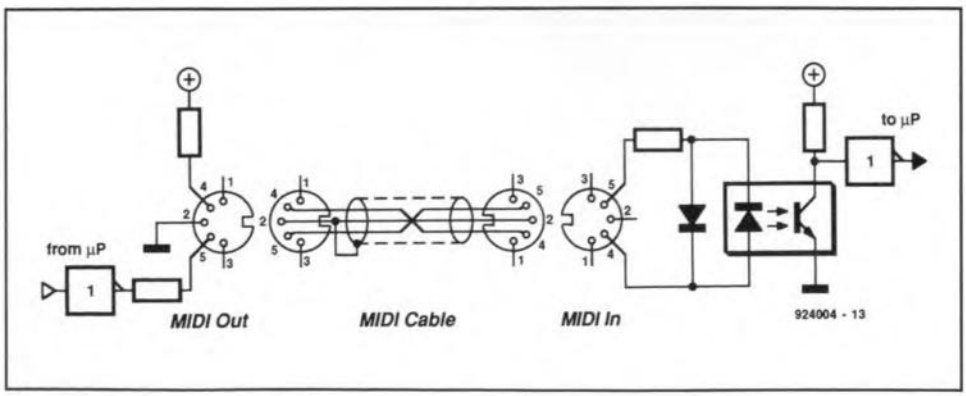
To test both ends of a cable, the tester must be built in duplicate: one terminated into a socket and the other into a plug. A possible design is shown diagrammatically in the lower diagram.

The connectors should preferably be metal DIN types. The LED can be housed in the rubber support sleeve as shown in the top right-hand figure. The connecting wires to the LED must, of course, be well insulated.

(R. Swusten – 924004)







PWM GOVERNOR

The governor described in this article is intended primarily for small 12 V motors that draw a current of not more than 2 A. Many governors limit the current through the motor, which also reduces the torque. Since it is controlled by pulse-width modulation (PWM), the present governor preserves most of the torque. The control is based on a sextuple CMOS inverter, IC_1 (Type 40106). Three of the inverters are not used here. The motor is driven via a discrete darlington, T_1-T_2.

Inverter IC_{1a} functions as an oscillator, whose on time (when T_2 conducts so that the motor is provided with power) is determined by R_2-C_2-D_3. The off time of the oscillator (when T_2 is also off) is determined by R_3-P_1-C_2-D_4, and may thus be varied with P_1.

Parallel-connected inverters IC_{1b} and IC_{1c} form a buffer between the oscillator and the power darlington.

The motor is connected across the + and 0 terminals in the diagram.

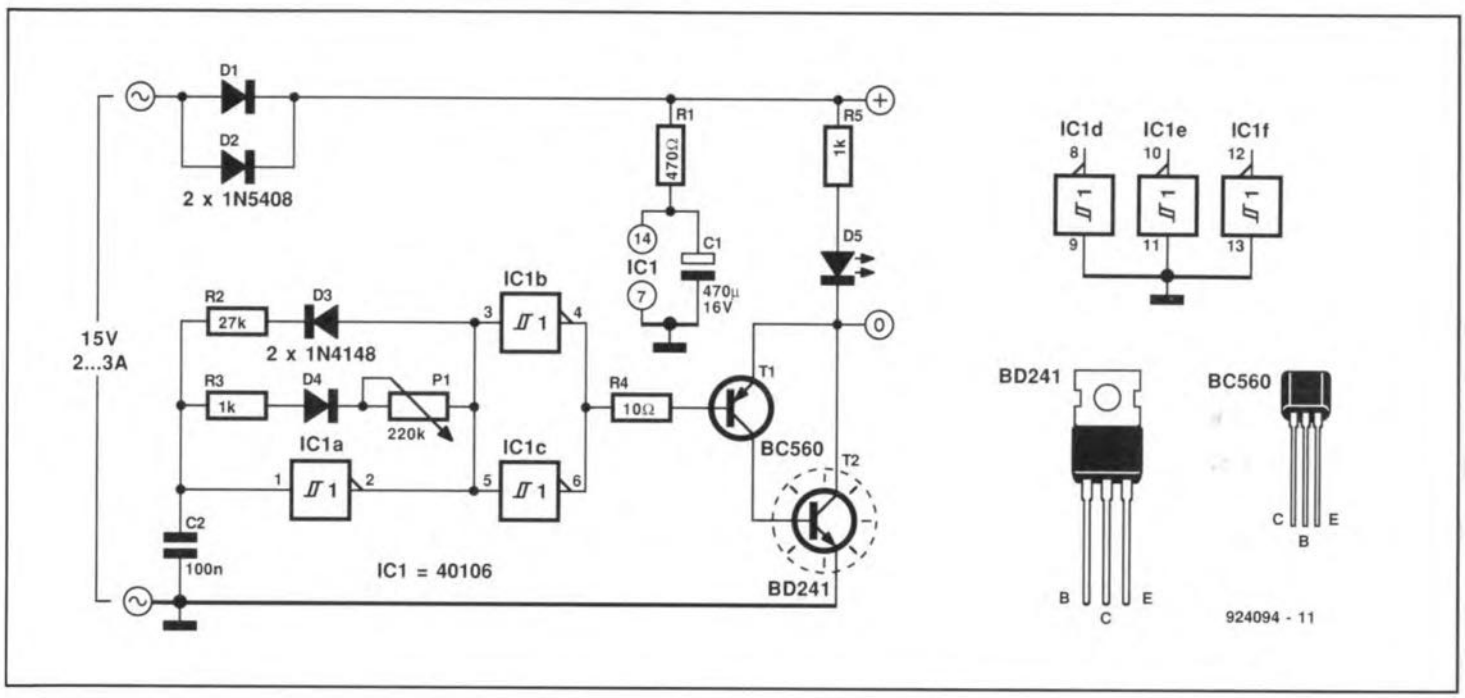
Power for the governor and the motor is provided by a mains transformer, whose secondary voltage is single-phase rectified by D_1 and D_2.

An indicator LED with current limiting resistor is connected across the motor terminals.

Network R_1-C_1 smooths the supply voltage to IC_1.

Finally, T_2 must be fitted on a suitable heat sink.

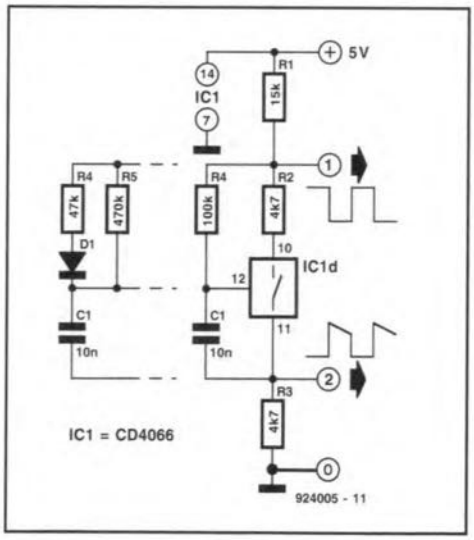
(Amrit Bir Tiwana – 924094)



REPEATING PULSE GENERATOR

THE circuit uses one of the four bilateral switches contained in a CD4066, and is a kind of astable multivibrator. The main limitations of the circuit are the relatively poor shape of the output signal, and the output signal swing, which is not digitally compatible. These drawbacks are easily overcome, however, by a buffer at the output. When the switch closes, the current in the chain produces a voltage across R_3, which raises the switching level at the trigger point by about one volt. Likewise, R_1 reduces the voltage applied to R_4 to a level below the switch-off voltage.

The mark-to-space ratio (duty factor) of the output signal may be varied by using parallel charging resistors, one with a series diode (preferably a germanium type), as shown in the circuit diagram.



In the prototype, the component values shown resulted in an output frequency of 957 Hz with a supply voltage of 5 V exactly. The duty factor was about 0.4 without the parallel *R-D* network. With the network fitted, the output frequency and duty factor were 317 Hz and 0.06 respectively.

The current drain varied between 0.12 mA and 0.39 mA.

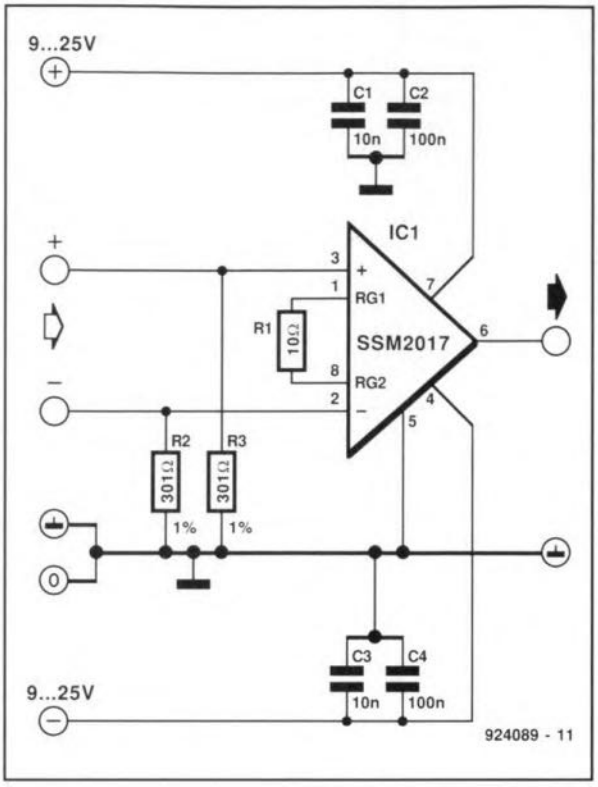
(M.I. Mitchell – 924005)

LOW-NOISE AMPLIFIER II

Opamp Type SSM2017 from PMI is eminently suitable for designing a very-low-noise microphone preamplifier. According to the manufacturer's data sheet, the input noise is only 750 pV $Hz^{-1/2}$. The amplification ($\alpha=1+10^4/R_1$) may be set to a value of 1–1000 with a single resistor, R_1.

The internal compensation of the IC is such that stability is retained even at unity amplification, yet, when the amplification is ×1000, the bandwidth is 300 kHz.

The circuit in the diagram has a symmetrical input and a standard input impedance of 600 Ω. The amplification is ×1001, so that a microphone signal is converted directly into a line level. If the output of the amplifier is conveyed via a long cable (capacitive load), it is advisable to insert a 47–100 Ω resistor in series with it to obviate any likelihood of oscillation. Also, at high amplification the output may have an offset voltage, which, in certain applications may give rise to problems. If that is so, an output capacitor should be used.



The maximum output voltage of the IC is 9 V r.m.s. when the supply voltage is ±15 V. At a 1 kHz output at a level of 1 V r.m.s., the harmonic distortion does not exceed 0.005%. When the supply voltage is lower than ±9 V, the distortion rises to 0.01%. Th noise factor of the prototype (including the noise contribution of R_1) was measured at 1 nV $Hz^{-1/2}$. The current drawn by the amplifier from a ±15 V supply is about 11 mA.

(T. Giesberts - 924089)

SWITCHED 5 V SUPPLY

If you everneed to derive a 5 V line from, say, a 15–25 V supply, National Semiconductor's LM1575 and LM2575 are ideal. These switched 5-V regulators need only a choke, a freewheeling diode and a couple of electrolytic capacitors to meet your requirements. In fact, these regulators go a long way to prove that the industry has overcome most of the problems switched power supplies have suffered from; both the regulators mentioned worked first time without any problems whatsoever.

The only thing that is still not as good as in linear power supplies is the ripple: in the the prototypes this amounted to 20 mV_{pp}.

The measured efficiency of the prototypes is 75%, whereas National Semiconductors give a figure of 82%. This figure does, of course, depend to some extent on the components used.

The diode is a Type 1N5822 or BYW29 from Philips: any fast diode will do, however but do not use a common-or-garden 1N4001 or similar.

The choke is a ready-made 330 µH type that must be able to handle currents of at least 1 A.

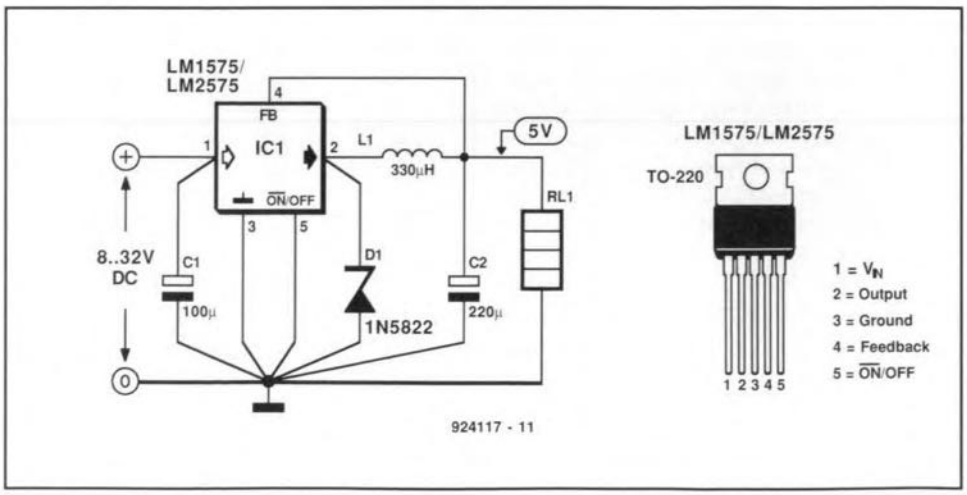
Build the supply with a central, star-shaped common earthing point as indicated in the diagram. Use good-quality electrolytic capacitors (perhaps two in parallel). The more compact you keep the supply, the better it will work.

The input voltage can lie between 8 V and 32 V. The maximum current the regulator can provide is about 1 A.

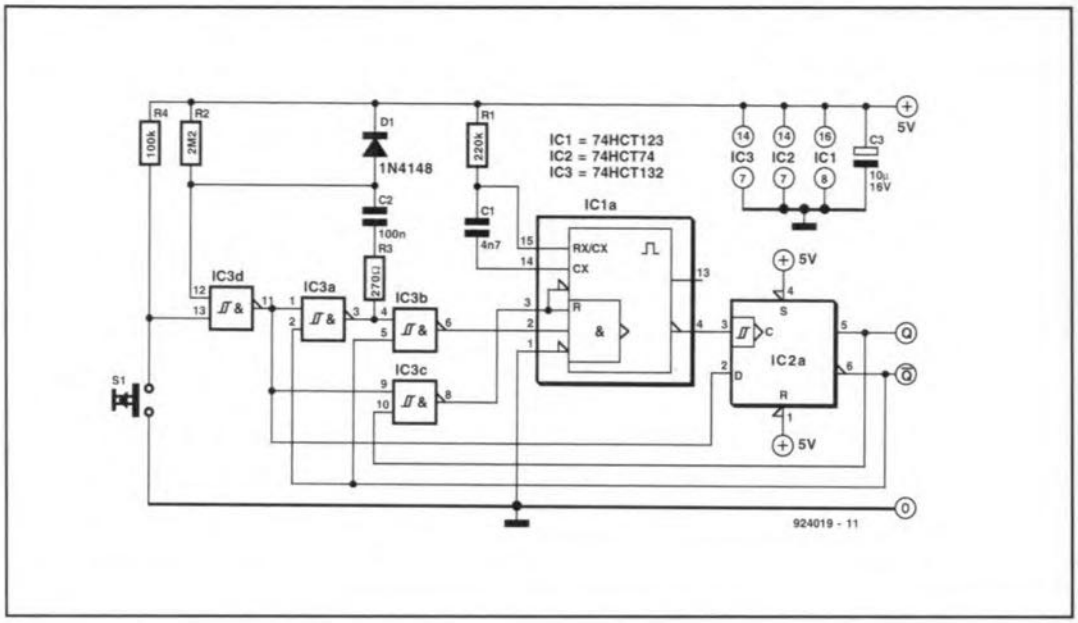
Pin 4 is the feedback input.

Pin 5 may be used for switching the supply on/off; if that is wanted, connect this pin to a 2.4–15 V potential instead of to earth.

(National Semiconductor – 924117)



REAL-TIME SWITCH DEBOUNCE



Most debounce circuits shorten or lengthen the time a switch is pressed to obviate interference pulses caused by switch bounce. The present circuit does **not** affect that time: the pulse at the output is exactly in accordance with the time elapsed between the depressing and the releasing of the switch.

When switch S_1 is pressed, monostable IC_{1a} is triggered via gates IC_{3d}, IC_{3a}, and IC_{3b}. The feedback from IC_{3a} to IC_{3d} ensures that the monostable cannot be triggered again during the pulse duration.

When the mono time has elapsed, bistable IC_{2a} is clocked. If at that moment the output of IC_{3d} is still high, the $\overline{Q}$ output of IC_{2a} goes high and the Q output becomes low. The bistable keeps IC_{3a} and IC_{3b} off, while IC_{3c} passes the output signal of IC_{3d} to the reset input of the monostable.

As long as S_1 remains depressed, the monostable is reset via IC_{3c}. When the switch is released and its contact opens, the monostable is retriggered. If the key stays open for the length of the mono time, bistable IC_{2a} is reset after that time. If the switch contact closes during the mono time, IC_{2a} remains set.

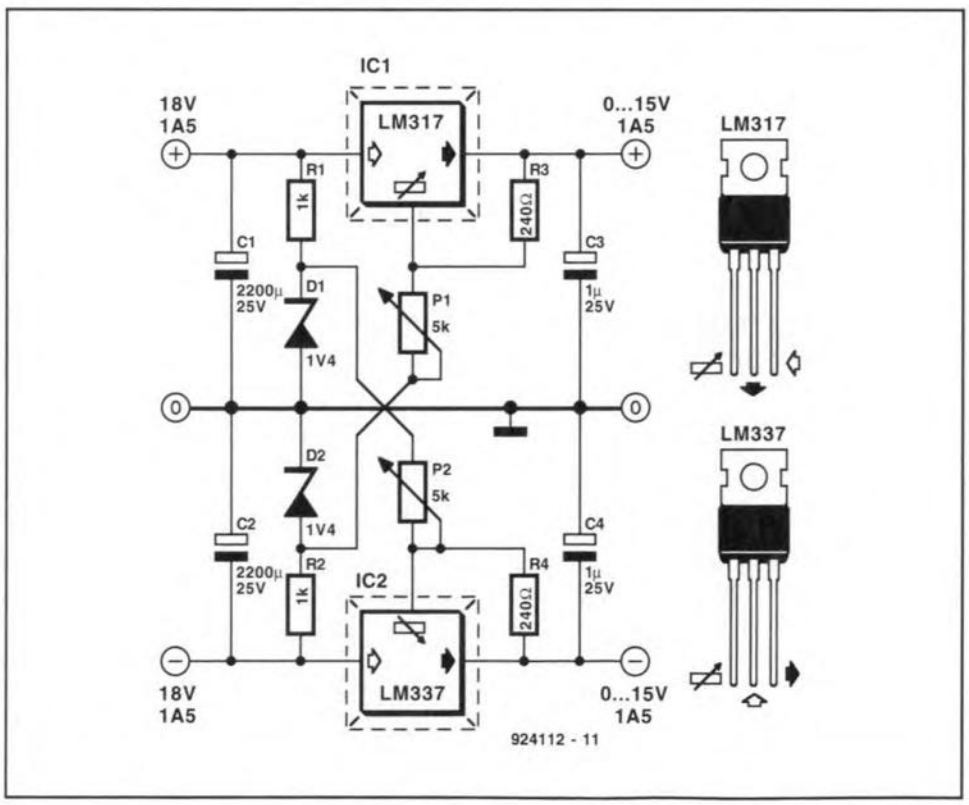
The mono time needs to be longer than the longest open time of the switch during bounce.

Time constant R_2-C_2 must be considerably longer than the mono time, so that the feedback from IC_{3a} to IC_{3d} is available during the entire mono time.

The circuit draws a current of about 1 mA.

(B. Zschocke – 924019)

SIMPLE SYMMETRICAL POWER SUPPLY



Integrated voltage regulators LM317 and LM337 enable a simple, regulated, symmetrical power supply as shown in the diagram to be designed. This supply is variable from 0 V to ±15 V, can provide a current of up to 1.5 A, is short-circuit proof, and has thermal protection. Moreover, the regulators have internal dissipation limiting which ensures, irrespective of their cooling, that the dissipation does not exceed 20 W.

To enable the output voltage being varied from 0 V, auxiliary voltages of ±1.4 V are created with the aid of two zener diodes, D_1 and D_2. Although technically inelegant, this arrangement is the most cost-effective in a simple power supply.

The regulators must be fitted on a heat sink with a thermal resistance of 1.75 K W^{-1}.

The maximum current of 1.5 A is available only if the maximum dissipation of 20 W has not been reached and (with an input voltage of ±18 V as shown), the output voltage is above 5 V. At lower output voltages, the maximum output current drops to 1.1 A (at U_o=0 V).

(L. Lemmens – 924112)

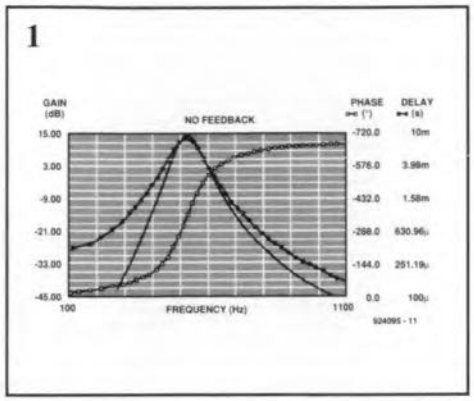
BANDPASS FILTER WITH EXTRA FEEDBACK

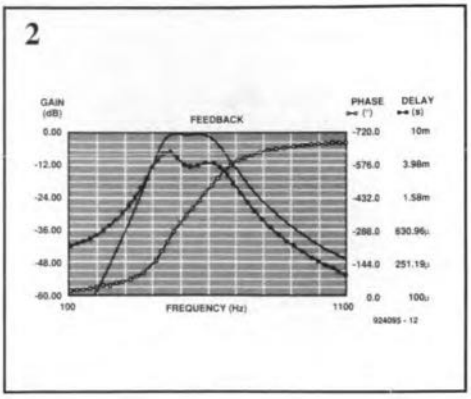
An important property of a bandpass filter is its shape factor, which is the ratio of its bandwidth at high attenuation to that at low attenuation. The smaller the shape factor, the better the filter.

Another important parameter is the group delay time, which determines how fast pulse-shaped and sinusoidal signals can traverse the filter. Within the pass band, the delay time should be constant to ensure the faithful transfer of the signal.

These parameters often do not show up very well in the usual active filter with local feedback for each second-order section (multiple feedback filter).

The magic word in electronics is 'feedback'. The graphs in Fig. 1 and 2, pertaining to the circuit in Fig. 3, show the importance of feedback. Figure 1 gives the frequency vs gain response if R_{14} and R_{16} are omitted (no feedback). The bandwidth at –3 dB is 50 Hz and that at –40 dB is 450 Hz. That gives a shape factor of 9.



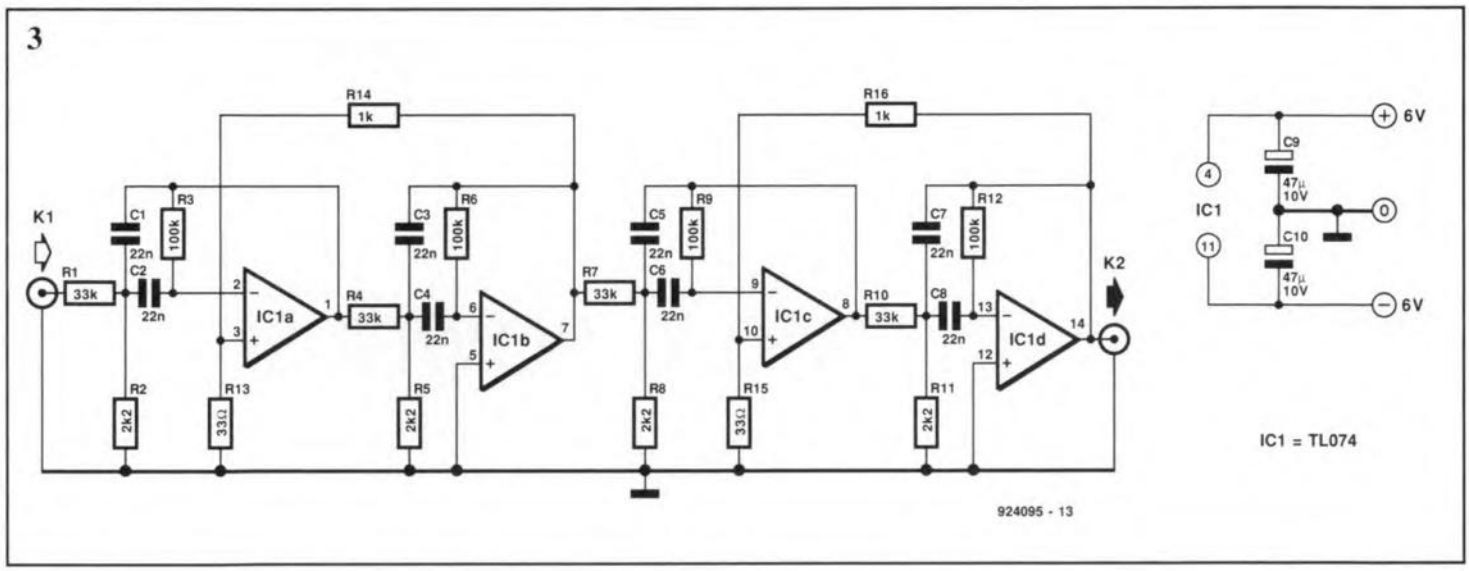


With the extra feedback provided by R_{14} and R_{16}, the filter has a bandwidth of 200 Hz at –3 dB and of 660 Hz at –40 dB. That gives a shape factor of 3.3.

Moreover, the group delay in the pass band is constant within acceptable limits.

This shows that with the extra feedback the filter gives a better performance than in its traditional set-up.

(J. Barendrecht – 924095)



AUTOMATIC NiCd BATTERY CHARGER

The charger makes cunning use of the properties of a Type 555 timer. The internal window comparator of the IC is set to 4.7 V by zener diode D_1. If the potential at pin 6 exceeds that level, the output voltage at pin 3 becomes low. If the potential at pin 2 drops below half the reference voltage, that is 4.7/2=2.35 V, the output voltage becomes high.

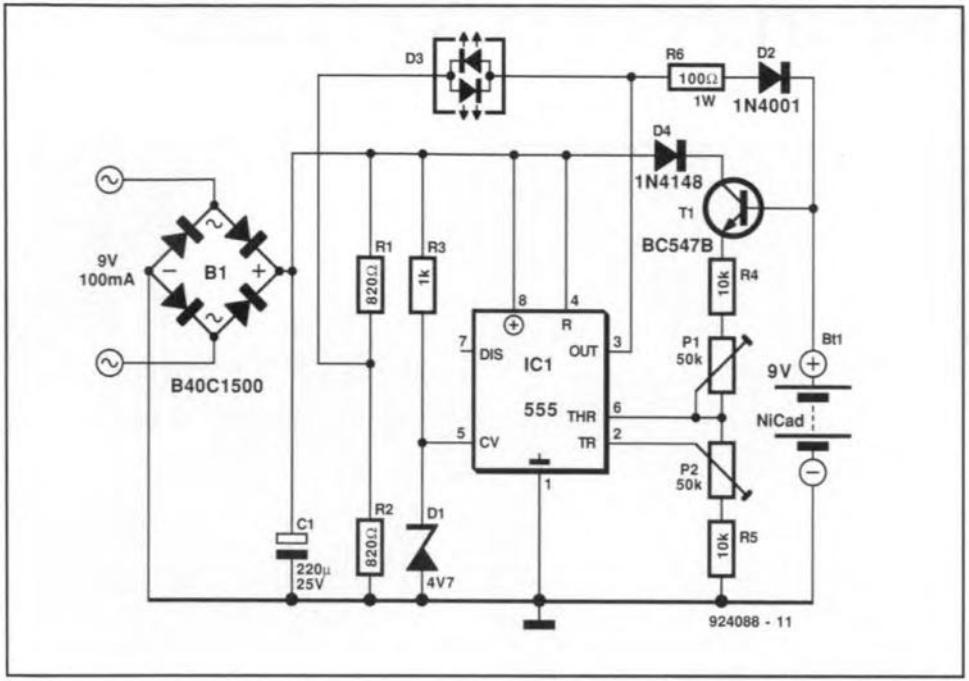
When the voltage of the battery to be charged is low, and the output potential of IC_1 is thus high, the battery will be charged via R_6 and D_2 until the 'fully charged' voltage, set with P_2, is reached. The output of the IC then changes state and charging ceases. However, the IC continues monitoring the battery voltage with the aid of T_1.

When the output of the battery, owing to self-discharge, has dropped below the level set with P_2, the IC causes charging to recommence. Dual LED D_3 lights red when charging is in progress and green during the quiescent periods.

In this way, the battery can be left in the charger for any period you like: it will always be fully charged for use when required. It will never be overcharged, nor will it dischargemore than a little.

With values as shown in the diagram, the charger is suitable for 6 V and 9 V batteries.

Nine-volt types with 6 or 7 cells are charged at about 20 mA; P_1 should be set to arrange for the charger to switch off after 14 hours. The lower window



level is set to about 1 V below that value with P_2.

Six-volt types with 4 or 5 cells are charged at 55 mA. Again, P_1 should be set so that the charger switches off after about 14 hours. The lower window level is set to about 0.8 V below that value.

It should be noted that NiCd battery manufacturers do not recommend 'fully charged' voltage measurements, but prefer time or temperature measurements. Nevertheless, the auhor has used the present circuit for charging small NiCd batteries to good effect for some time.

(Amrit Bir Tiwana – 924088)

DIGITAL TAPE COUNTER

Here is a simple way of making a tape counter that gives a ten-step indication with the aid of two ICs and a seven-segment display. Its great advantage is that it can be connected to a recorder in a straightforward manner, since it records the length of time the motor runs.

The motor of the cassette player is connected to the reset input of IC_2 and to the circuit earth. It is necessary for the motor to run only when the tape runs: in two- and three-motor decks the capstan motor usually runs continuously. At the instant the reset input of IC_2 goes high, the timer begins to deliver very-low-frequency pulses: one pulse every 3 minutes with S_2 in position C60 as shown in the diagram, and one every 4.5 minutes in position C90.

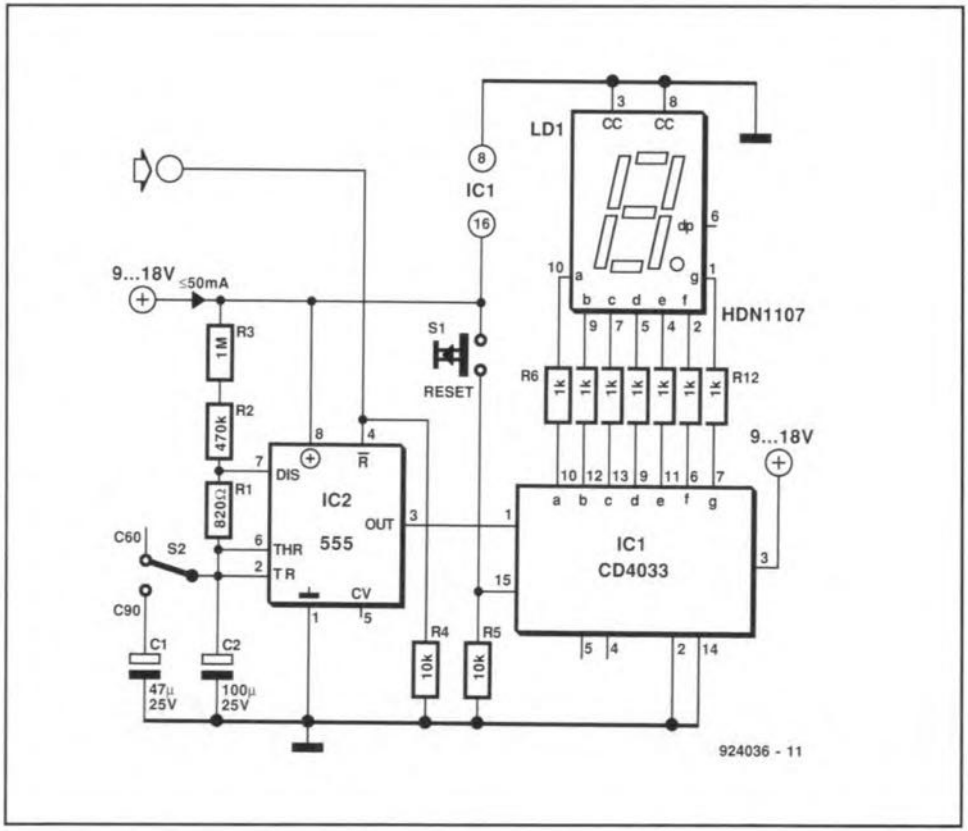
The pulses are applied to decade counter-display driver IC_1. This stage raises the display position by 1 for every pulse so that at the end of a C60 or C90 cassette the display has gone through positions 0–9. The display is reset by pressing S_1.

Owing to leakage currents and the tolerances of the electrolytic capacitors in the timing network, R_3-R_2-R_1-C_2 (or R_3-R_2-R_1-C_3), it may be necessary for the value of R_2 to be changed (empirically).

Because the first cycle of a Type 555 timer is always longer than the next, repeated stopping and starting of the tape may result in an appreciable error in the displayed time.

It is essential that the input voltage is free of noise pulses to prevent the 555 being reset spuriously.

The counter draws a current of not more than 50 mA.



(Amrit Bir Tiwana – 924036)

COPYING WITH AV RECORDERS

Cassette recorders like ITT's SL537 AV or SL837 AV, used by tape-slide producers, have a four-track head. A pulse circuit is connected to one of these tracks. Pulses recorded on to the tape can be used to actuate a relay to control the slide projector.

The cassette that contains both the sound and the control pulses must be handled carefully and it is for that reason wise to make a copy of it for normal use. Making such a copy is not so easy, however, because the pulses need to be copied precisely. When two AV recorders are available, making a copy becomes appreciably easier, provided that a small modification can be made to one of them.

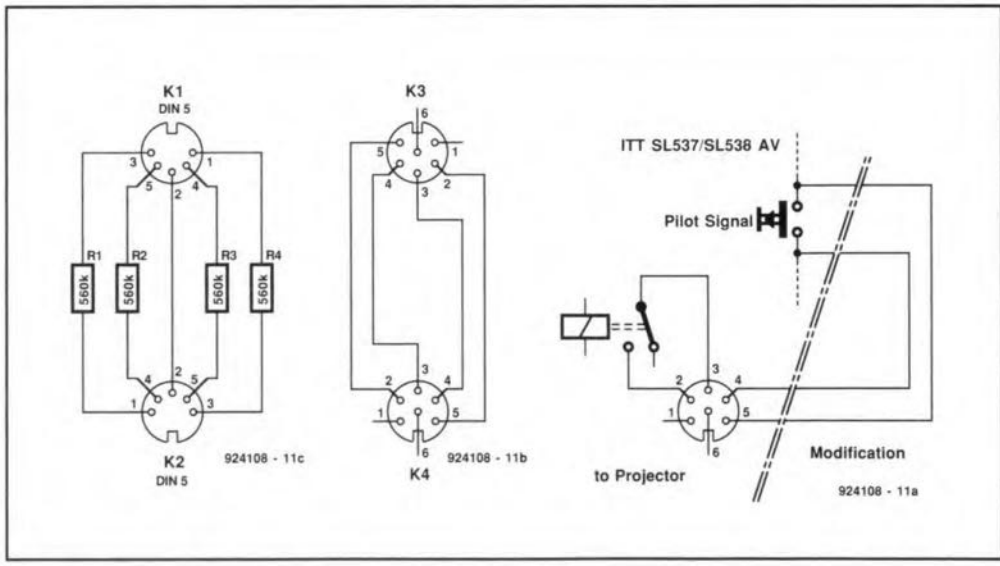
The ITT recorders have a remote control input socket that is in parallel with the 'to projector' socket. Both sockets are 6-way DIN types. If only the relay contacts in the recorder are used to send control pulses to the projector, the 'tact sw' can be linked to one of the unused pins of the remote control socket (pins 1, 4, 5 and 6).

When remote control is used, it needs to be ascertained whether there are free pins available. In the prototype, pins 4 and 5 are used—see Fig. 1a. If you cannot be certain, it is safer to bring out the two relay contacts via a 3.5 mm jack socket.

Once this work is done, pulses can be recorded on the tape from a second recorder with pulse output. But first a short cable has to be made to connect the contacts on the second recorder (pins 2 and 3 of the 'to projector' socket) to the modified socket on the first recorder In the case of two ITT recorders, this cable is shown schematically in Fig. 1b.

Furthermore, for copying a second short (record/playback) cable as shown in Fig. 1c is needed. This cable should be matched to the input levels of the recorders.

With the modified recorder set to record (audio as well as AV), the second recorder plays back the original cassette. The modified recorder will then make a perfect copy of the original tape.



The cable connections in the diagram have been chosen so that two modified recorders can copy back and forth ad infinitum.

(A. Rietjens – 924108)

BIAS COMPENSATION FOR BIPOLAR OPAMPS

One advantage bipolar opamps have over FET types is that their input noise level is appreciably lower. However, when a bipolar opamp is used in a high-impedance circuit, its bias current often presents a problem. For instance, the bias current of the well-known NE5534 opamp is typically 0.5 µA with a variation of about 5 nA °C^{-1}. Temperature variations of ±10 °C would thus cause current changes of almost 10%, which would make it impossible to hold the output voltage at zero volts d.c.

The circuit presented here compensates the bias current with a current source. Its design ensures a high input impedance. In practice the current source is not entirely stable with temperature variations, but that is largely nullified by placing it in a control loop.

The current source, T_2, is connected

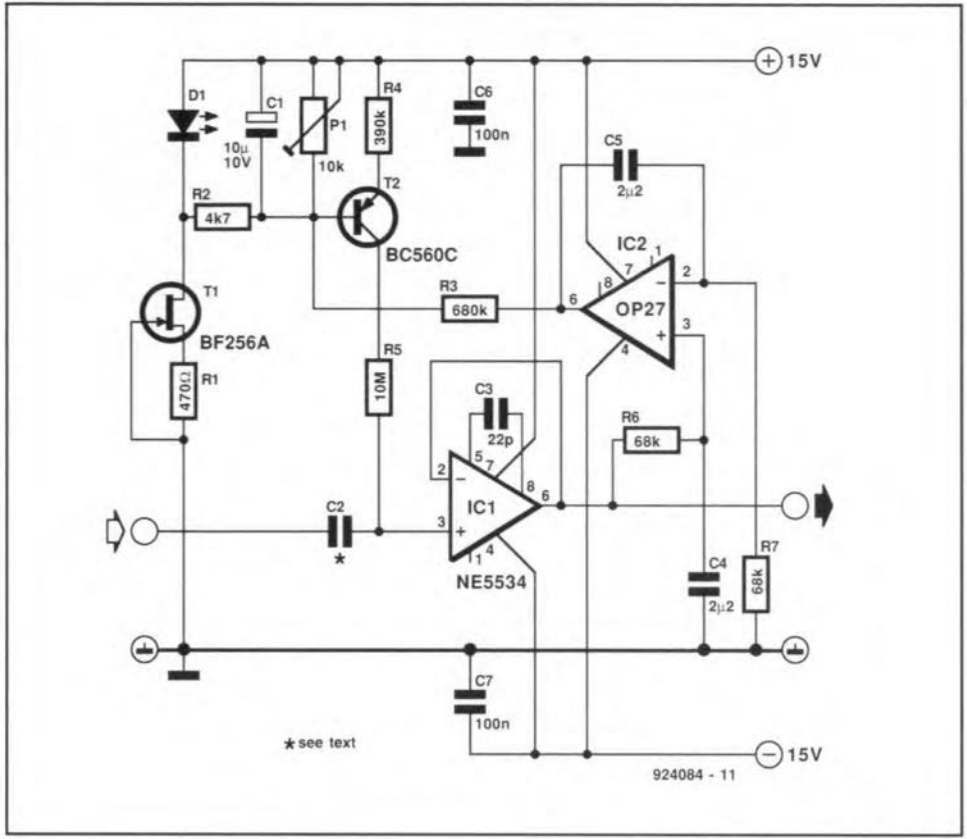
to the non-inverting input of IC_1 via a 10 MΩ resistor. The reference voltage for T_2 is established by a 2 mA ancillary current source, T_1 and D_1. This arrangement ensures that noise on the supply lines hardly affects the circuit.

To keep the noise of T_2 to a minimum, the 'reference voltage' of D_1 is divided by R_2-P_1.

Opamp IC_2 measures the direct voltage at the output of IC_1 and regulates the current source via R_3 in such a way that there is no direct voltage at the output of IC_1. This means, of course, that IC_1 cannot be used as a d.c. amplifier.

To ensure that the bias compensation is not nullified or affected by the output resistance or output offset of the preceding stage, a capacitor, C_2, is necessary at the input. It might be thought that, in view of the high input impedance, this should have a small value. For a 20 Hz cut-off point and an input impedance of 25 MΩ, a value of 330 pF would be sufficient. But this is wrong, because the high reactance of such a capacitor would cause a noise level of about 640 nV $Hz^{-1/2}$ at 20 Hz. Beause of this, the reactance of the capacitor must match the output impedance of the preceding signal source.

Preset P_1 must be set so that the output voltage of IC_2 is zero, or nearly so, at the centre of the wanted ambient temperature range.



The circuit draws a current of about 11 mA.

(T. Giesberts – 924084)

CURRENT PROBE FOR PCB TRACKS

Current tongs are instruments for measuring alternating currents in cables. Their great advantage over most other methods is that the circuit need not be broken. Their action depends on the same principle as that of a transformer: after the tongs (transformer core) have been placed around one or more current-carrying conductors (primary winding), magnetic fields arise in the core material. Because of the alternating magnetic field components a voltage is induced in the coil wound around the core (secondary winding). In accordance with Faraday's law of induction, this voltage is a measure of the vector sum of the currents through the wires in the cable.

A frequent requirement is the measurement of an alternating current in the supply lines on a printed-circuit board. In that case, technicians are often more interested in the waveform than in the r.m.s. value. Traditional current tongs can, of course, not be used then. It is, however, not too difficult to construct a current probe for this purpose. All that is needed is a short length of ferrite material,a few metres (yards) of thin enamelled copper wire,a BNC plug, and a metre (yard) of 50-Ω coaxial cable, for instance, Type RG58/U.

Ferrite has a low magnetic resistance and attracts the fields around the track. To ensure optimum coupling, the ferrite must be placed as close as possible to the track. The most convenient shape of the ferrite is a bead cut in half lengthwise: the hollow inside can then envelop the track at an angle of 180°—see diagram.

About 40 turns of the copper wire are wound around the half bead as shown. The terminals of the winding are soldered to the coax cable. Solder one terminal of the coil to the conductor of the cable, insulate the connection with tape and then fold the earth braid back over the conductor. Then solder the second

terminal of the winding to the braid.

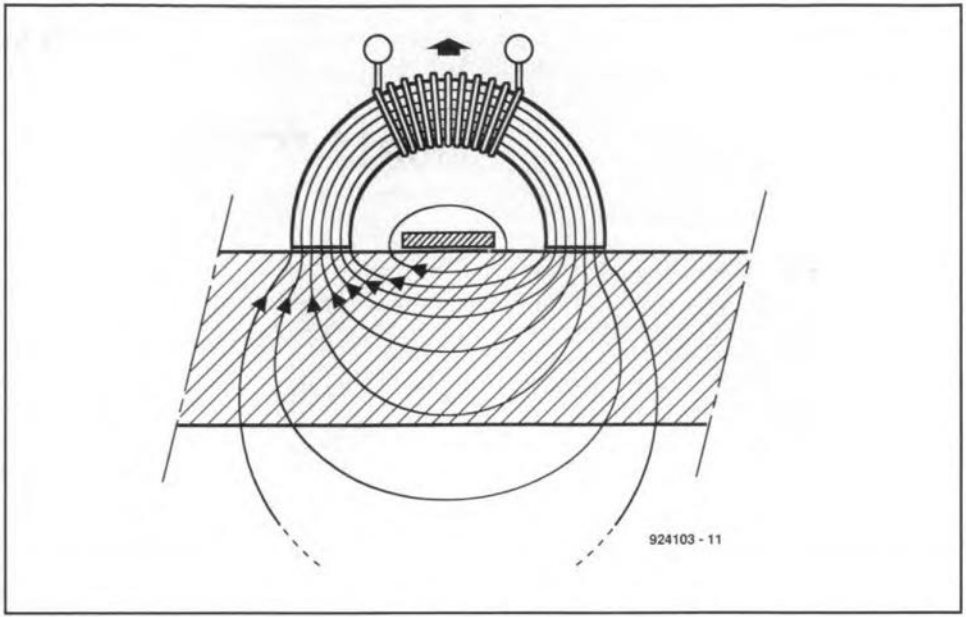
To give the probe some mechanical rigidity, push a narrow tube (such as an empty ballpen) over the cable on to the winding. When that is done, fit the tube to the sensor with superglue or epoxy resin.

Terminate the other end of the coaxial cable into the BNC plug.

The self-inductance of the sensor winding is some 20–30 μH, which gives a reactance ($=2\pi fL$) in the wanted frequency range that is much greater than 50 Ω. The voltage measured with a spectrum analyser or oscilloscope is thus virtually independent of the signal frequency.

The core of the prototype shown in the photograph is 4 mm thick and 15 mm long. The self-inductance of the sensor winding is 80 μH, which makes the probe suitable for frequencies >500 kHz. As long as the core material is not saturated, the sensitivity of the probe is about $0.2\,VA^{-1}$.

(B. Danker – 924103)



COMPACT RS232 ISOLATOR

The MAX252 from Maxim is a special IC for designing an electrically isolated RS232 connection. Such links are particularly important when several pieces of equipment (which may or may not be isolated from the mains) are to be interconnected even when they have different earth potentials.

The chip is available in two modes: A (expensive) and B (inexpensive). Note, however, that even inexpensive is relative, because the B type still costs more than £30.

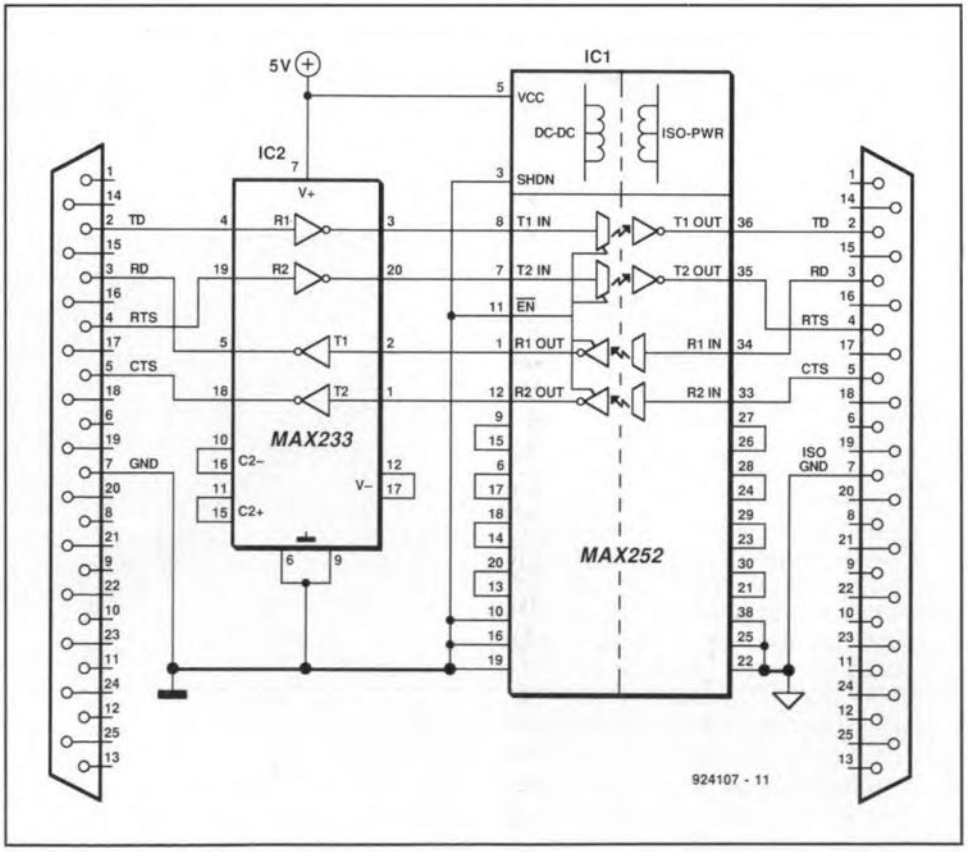
The maximum isolation voltage that the B-type can handle for one minute is 500 V, whereas the A-type can handle up to 1250 V. Moreover, the A-type can have a constant voltage across its terminals of 130 V. The maximum transmission speed of both types is 9600 baud.

The internal transformer of the chip provides the supply voltage for the right-hand side of the diagram. The input and output levels at the left-hand side are TTL compatible. The inputs have a hysteresis of roughly 0.5 V and pull-up current sources of 0.4 µA for the suppression of noise signals.

The inputs and outputs at the right-hand side are RS232 compatible. Outputs $T1_{out}$ and $T2_{out}$ deliver a voltage of 7.5 V to a load of 3 kΩ.

With a supply voltage of 5 V, the IC draws a current of 90 mA.

Pin 11 of the MAX252 is an active-low, output-enable input and pin 3 an active-high shut-down input. A high level at pin 3 causes the 130 kHz oscillator of the integrated supply to be switched off, $T1_{out}$ and $T2_{out}$ to become high-impedance, the 4 µA pull-up inputs to be deactuated, and the power acceptance to be reduced to 50 µW.



RS232 compatible levels at the left-hand side can be provided by the MAX233 as shown in the diagram. This IC also arranges the necessary inversion of the various signals.

(Maxim application – 924107)

DUMMY LOADS

ARTIFICIAL AERIALS FOR TRANSMITTER TESTING

A dummy load is an artificial aerial that is used for making measurements and performing tests on radio transmitters without actually radiating a signal into the air. Radio operators should routinely use dummy loads to tune up on crowded channels, and only when the tuning is completed transfer power to the live antenna. In some countries, this procedure is not merely good manners, but required by law (even if often ignored).

By Joseph J. Carr, K4IPV

ANOTHER use for dummy loads is in troubleshooting antenna systems containing multiple elements (e.g. tuners, coaxial cable, low-pass filters, and so forth). Suppose, for example, we have an antenna system in which the VSWR (voltage standing wave ratio) is high enough to adversely affect the operation of the radio transmitter. Modern transmitters, with solid-state final RF power amplifiers, have VSWR-sensitive power shutdown circuitry. We can test such a system by disconnecting each successive element in sequence, and connect the dummy load to its output. If the VSWR goes down to the normal range, when a particular element is replaced with the dummy load, the difficulty is probably distal to the point where the dummy load was inserted (i.e., towards the antenna). You will eventually find the bad element (which is usually the antenna itself).

Another use for dummy loads is in testing for television, broadcast radio or audio system interference. Once it is established that it is your transmitter that is causing the problem, it is necessary to determine whether or not the route of transmission is through the antenna, around the cabinet flanges or through the AC power mains connection. If the offending signal is from the antenna, then the root cause might be not the signal or transmitter, but improper filtering or shielding of the television or other appliance, or the inability to handle local overload conditions created by (but not the fault of) your transmitter. If the interference persists in the face of using an RF dummy load substituting for the aerial, then the problem is in the power connection or flanges ...and you must do something further to find and suppress the fault.

Forms of dummy load

A common, but irregular, form of dummy load is shown in Fig. 1. It consists of a 40 to 100-watt electric light bulb that is connected to a length of 52-Ω coaxial cable and a connector that mates with the transmitter. The centre conductor of the coaxial cable is connected to the centre button of the light bulb, while the shield of the coaxial cable is connected to the outer threads or base (depending on country of origin) of the bulb.

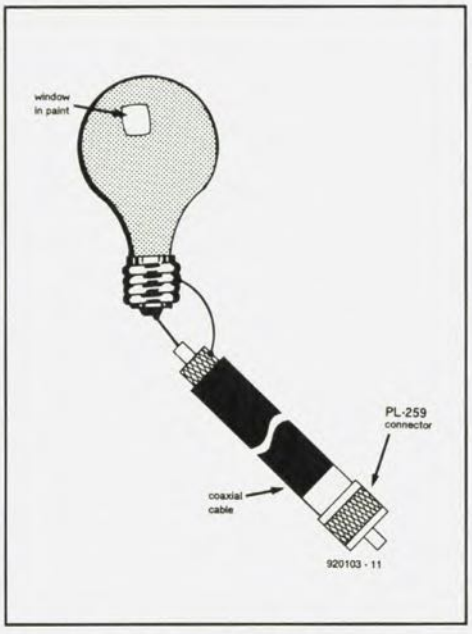


Fig. 1. Light bulb dummy load.

It was once common practice to paint the bulb with either aluminium or copper conductive spray paint, except for a small window to see the light level. The paint supposedly shields the bulb and thereby prevents RF radiation. That supposition, however, is highly optimistic. One day about 30 years ago, I used this type of dummy load to test my Heathkit DX-60B 90-watt CW transmitter. A friend of mine answered my 'call' (supposedly made to a dummy load), and reported an S7 signal strength...from a distance of nearly ten kilometers! That is not exactly how a dummy load is supposed to work.

Another defect of the light bulb dummy load is that its resistance changes with light brightness. Hence the bulb is not stable enough to be seriously considered as a dummy load except in the crudest sense.

The light bulb dummy load, while cheap and easy to obtain, is too much of a problem for all but impromptu emergency situations. It is *not* recommended.

Figure 2 shows the most elementary form of regular dummy load which consists of one or more resistors connected in series, parallel, and/or series-parallel as needed to make the total resistance equal to the desired load impedance (usually 50 Ω).

The power dissipation of the dummy load in Fig. 2 is the sum of the individual power dissipations. By using ordinary 2-watt carbon composition resistors, it is possible to make reasonable dummy loads to powers of about 50 watts. Above that power level, one must consider the effects of stray capacitance and inductance from all of the resistor leads and interconnecting wires. Higher levels can be accommodated, however, if care is taken to keep capacitances and inductances low.

It is essential that non-inductive resistors be used for this application. For this reason, carbon composition or metal film resistors are used. There are actually two forms of non-inductive resistors on the

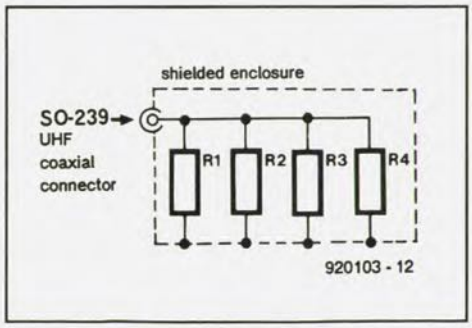


Fig. 2. Simple, low-power dummy load made from carbon composition or metal film non-inductive resistors.

Fig. 3. Commercial 5-watt dummy load.

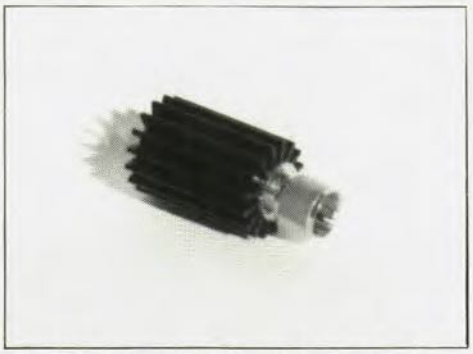


Fig. 4. Commercial 50-watt dummy load.

Fig. 5. Commercial 50-watt, 50-ohm dummy load (courtesy Bird Electronics).

market. The carbon composition and metal film types are intuitively obvious. The other form are wirewound resistors in which adjacent turns are wound in opposite directions so that their mutual magnetic fields cancel each other out. These are called 'counter-wound' resistors. For very low frequency (< 20 kHz) work, it is permissible to use such counter-wound wire low-inductance resistors. These resistors, however, cannot be used over a few hundred kilohertz.

Several commercial dummy loads are shown in Figs. 3 through 10. The dummy load in Fig. 3 is a 5-watt model, and is typically used in Citizen's Band and other low-power (QRP) HF transmitters. The resistor is mounted directly on a PL-259 coaxial connector. These loads typically work to about 300 MHz, although many are not really useful over about 150 MHz because of stray capacitance and inductance. A higher power version of the same type is shown in Fig. 4. This device works from VLF to the low VHF region, and is able to dissipate up to 50 watts. I have used this dummy load for servicing high VHF landmobile rigs, VHF-FM marine rigs, and low-VHF landmobile rigs, as well as ham radio rigs.

The load resistor in Fig. 5 is a Bird Electronics *Termaline* load that works at power levels to 50 watts, while presenting a 50-Ω load.

A 300-watt amateur radio 50-ohm dummy load is shown in Fig. 6. This one is made by MFJ Enterprises in the USA. Unlike the other two models, above, it is built inside a sheet metal cabinet, and is low in cost.

An MFJ *Versaload* is shown in Fig. 7. This dummy load is similar in form to the old (now off the market) Heathkit *Cantenna*. It consists of a high-power, 50-Ω non-inductive resistor element mounted inside a paint can that is filled with ordinary motor oil. The oil increases the dissipation capability of the resistor, but tends to seep out of the load if it is not well sealed.

Very high powered loads are shown in Figs. 8 and 9. These devices are Bird Electronics 'coaxial resistors', and operate to power levels of several kilowatts or more. The high power load of Fig. 9 is cooled by flowing water through the body of the resistor, and then exhausting the heat in an air-cooled radiator.

Our final dummy load resistor is shown in Fig. 10. The actual resistor, made by R.L. Drake Co. in the USA, is shown in Fig. 10a, while a schematic view is shown in Fig. 10b. The long, high-power non-inductive resistor element is rated at 50 Ω, and can dissipate 1000 W for several minutes. If longer times, or higher powers, are anticipated, then forced air cooling is applied by adding a blower fan to one end of the cage (on the Drake product, a removable mounting plate for a 3.5-inch fan is provided).

Providing an output level indicator

The dummy load in Fig. 10 was modified by the author by adding the BNC jack (J2) for RF signal sampling. This jack is connected internally to either a two-turn loop made of 22 AWG (approx. 0.8 mm dia.) insulated hook-up wire, or a 25-cm brass rod that is positioned alongside the resistor element (as shown in Fig. 10b). The loop or rod will pick up a sample of the

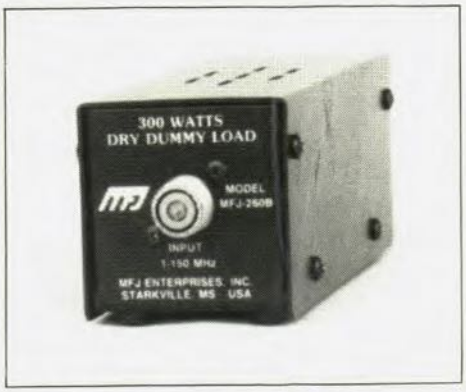


Fig. 6. Amateur radio dummy load for VLF to 150 MHz (courtesy MFJ Enterprises, Inc.).

Fig. 7. Dummy load mounted inside a paint can (Courtesy MFJ Enterprises, Inc.).

Fig. 8. High power dummy loads (Courtesy of Bird Electronics).

Fig. 9. High power, water-cooled dummy load (courtesy Bird Electronics).

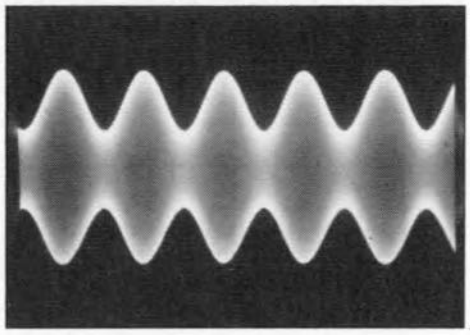


Fig. 11. Typical RF display on an oscilloscope from pick-up unit inside dummy load.

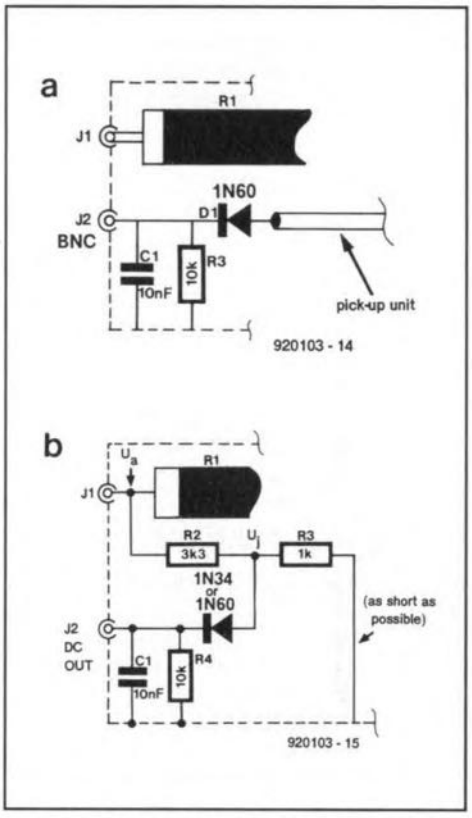


Fig. 12. a) diode detector circuit for circuit of Fig. 10; b) resistor voltage divider for detecting RF signal.

signal so that it can be viewed on an oscilloscope, or used for other instrumentation purposes. Figure 11 shows an oscilloscope photograph of an amplitude modulated RF signal taken from my modified dummy load. The transmitter was a 60-watt AM rig modulated by a 400-Hz sine wave from a bench signal generator.

Another approach to providing an output indicator is shown in Fig. 12a. In this case, a germanium signal diode (1N34 or 1N60 is suitable) is connected to the end of the signal sampling rod that connects to the output BNC jack. The diode rectifies the signal picked up by the rod, or sampling coil if one is used, and the *R-C* network R3-C1 filters it to remove residual RF signal.

A variation on the theme is shown in Fig. 12b. This circuit, which is like one that was used in the Heathkit *Cantenna*, uses a resistor voltage divider (R2-R3) connected across the dummy load (R1). A germanium signal diode (1N34 or 1N60) is attached to the junction of the two voltage divider resistors.

The voltage at the junction (U_j) is related to the RF output power applied to the dummy load by the voltage divider equation:

$$U_j = \frac{R3}{R2+R3}\sqrt{R1 \times P}$$

or,

$$U_j = 0.23\sqrt{50 \times P}$$

where P is the RF power in watts. The output voltage from the circuit of Fig. 12b is quite reasonable. With the values shown, a 100-watt transmitter signal produces an RMS (root-mean-square) voltage of the order of 16 V.

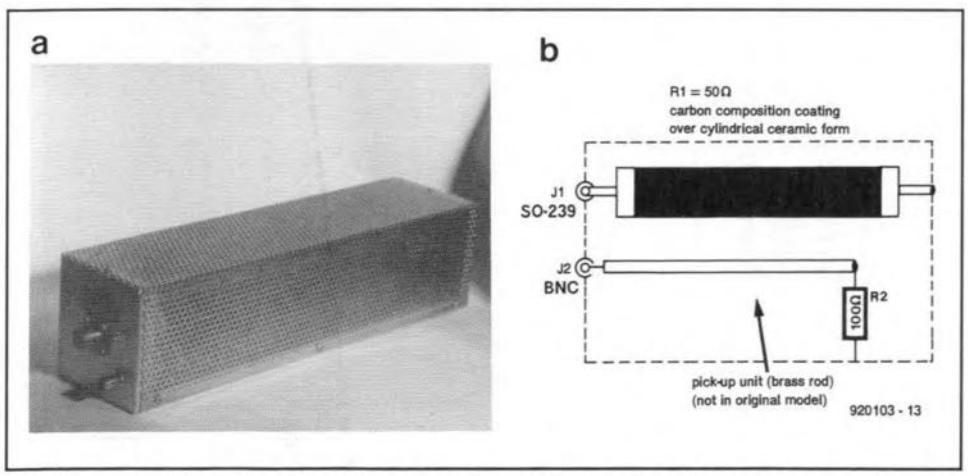


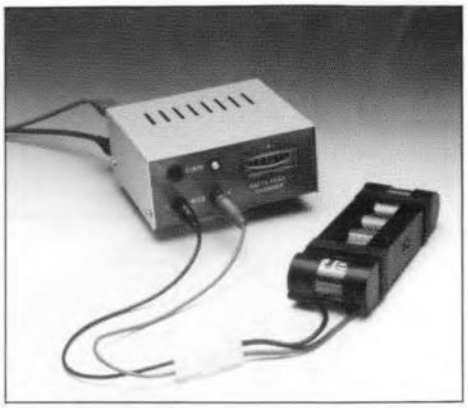
Fig. 10. a) amateur radio dummy load, 50-ohm, 1000-watts intermittent (constant when optional fan is added); b) circuit of dummy load, with author's modifications.

Conclusion

Dummy loads are used as artificial aerials that permit one to energize a radio transmitter for testing, troubleshooting or adjustment without actually radiating a signal. Their use is good engineering practice, is good manners for good radio neighbours, and is legally mandated in most countries. Use them, and we will all be better off. ■

DELTA-PEAK NiCd CHARGER

Design by L. Pijpers



Fast charging high-capacity NiCd batteries with large currents does not only save time, but also prolongs their useful life. Moreover, if the charger operates on the delta-peak principle, the batteries are always charged timely and to full capacity.

High-capacity NiCd batteries from which large currents are drawn benefit from being charged with large currents. Owing to the large discharge currents free metal ions in the electrolyte are produced in the course of time. This raises the internal resistance of the battery so that it can no longer provide such large currents. If the battery is charged with a large current, the ions are eliminated so that the internal resistance of the battery returns to its normal value. It should be borne in mind, however, that not all NiCd batteries can be charged with large currents. Moreover, even if the battery is capable of being fast-charged, this should never be attempted when it is not fully discharged. Finally, to ensure that the battery has a long life, it is recommended that every fifth fast charge is followed by a standard 14-hour charge.

Delta-peak principle

In standard practice, NiCd batteries must be charged at $^1/_{10}$ of their Ah capacity for 14 hours, which means a slight overcharge. Fast charging requires special measures. As shown in Fig. 1, the cell voltage during charging initially rises rapidly and then, after a certain level has been reached, only slowly. When the battery is almost fully charged, the cell voltage rises more rapidly again until it is fully charged, after which the voltage actually drops. This can be explained as follows. The charging current not only charges the battery, but also decomposes the electrolyte, whereby gases (particularly oxygen) are produced that cannot combine with the electrode material. The consequence is that the pressure in the (sealed) battery rises slowly. When the battery is nearly fully charged, the charging current produces primarily gas and contributes little to the charge. This results in a rapid rise of the pressure and the cell voltage. Because of that pressure, part of the oxygen combines with the material of the negative electrode which produces heat. Since NiCd batteries have a negative temperature coefficient of about –4 mV °C^{-1}, shortly after the battery has reached full charge, the cell voltage drops again. Figure 1 shows that the **peak** voltage is reached just after the battery is fully charged.

The **delta** comes about because the principle used here depends on the monitoring of small voltage changes, which are denoted mathematically by the Greek letter d(elta). With this principle, as soon as the cell voltage shows signs of dropping, charging is discontinued.

The circuit

The prime function of the circuit in Fig. 2 is the monitoring of small changes in the battery voltage. To this end, the battery voltage is applied to an integrator, consisting of R_3 and C_2, via protection diode D_4 and R_2. The integrator has a time constant, τ, of 5 s. As long as the battery voltage rises, the potential across C_2 remains slightly below the voltage at junction R_2-R_3. When the battery voltage drops, the potential across C_2, owing to the delay, becomes higher than the voltage at junction R_2-R_3. This comes about because of the charging current of C_2, which flows through R_3 and thus causes a voltage drop across this resistor. The small drop across R_3 is applied to IC_1 (a FET that has very high impedance inputs). When the voltage at pin 3 of this opamp is higher than that at pin 2, the output of the amplifier is high, but T_2 does not yet conduct because T_1 is off since its base-emitter voltage is held at 0 V via the relay contact and R_6-R_8. When S_1 is pressed, T_1 conducts, T_2 switches on and the relay is energized, after which T_1 is held on by R_7: the charging process has commenced.

When the peak cell voltage is reached, the potential at pin 3 of IC_1 drops below that at pin 2. This results in the output of IC_1 going low, whereupon T_2 is switched off. The relay is then deenergized so that T_1 is off: charging has ended.

This would be true in an ideal world: in the real world opamps have offset voltages at their inputs so that they don't switch at exactly 0 V. The offset voltage of IC_1 is 'nullified' by setting P_1 so that the IC changes state when the voltage at pin 2 is about 2 mV higher than that at pin 3. The printed-circuit board in Fig. 3 has two terminals ('off') where the offset voltage can be measured with a digital voltmeter.

The charger operates either from a 12 V (car) battery or a 12–14 V mains adaptor that can deliver the necessary high currents.

Construction and setting up

The charger is intended to be constructed on the PCB shown in Fig. 3. All components bar the relay and P_1 must be fitted upright. It is, therefore, necessary to fit the seven soldering pins before the components. Power resistors R_{11} and R_{12} are not fitted on the board. The board should preferably be mounted in a small metal case to which R_{11} and R_{12} may be fixed for good heat condcution.

During setting up, a discharged NiCd battery must be connected to K_3 (but it must not

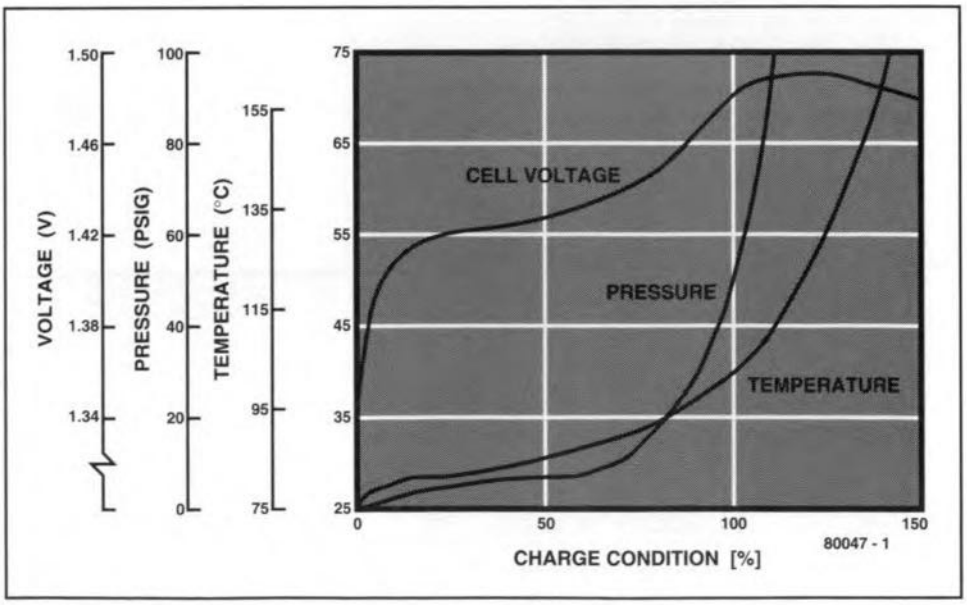
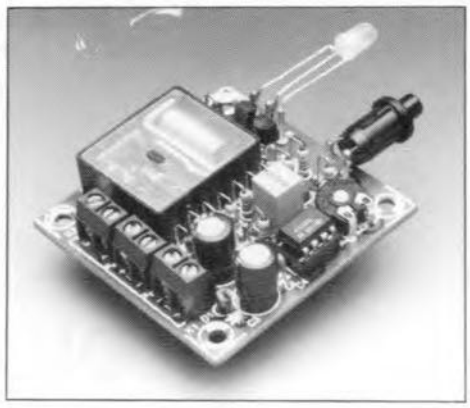


Fig. 1. Charge condition vs voltage/pressure/temperature characteristics.

be charged, which it is not as long as S_1 is not pressed). Since the maximum current drawn is then 500 mA, the charger may be powered from a simple 12 V mains adaptor or battery. Link JP_1 must be set and a DVM, set to its lowest voltage range, connected to 'off'. Set P_1 for a reading of –2.0 mV. Remove the link and the DVM, whereupon the charger is ready for use.

As a refinement, a suitable 5 A ammeter for monitoring the charging current may be fitted permanently in the +12 V supply line.



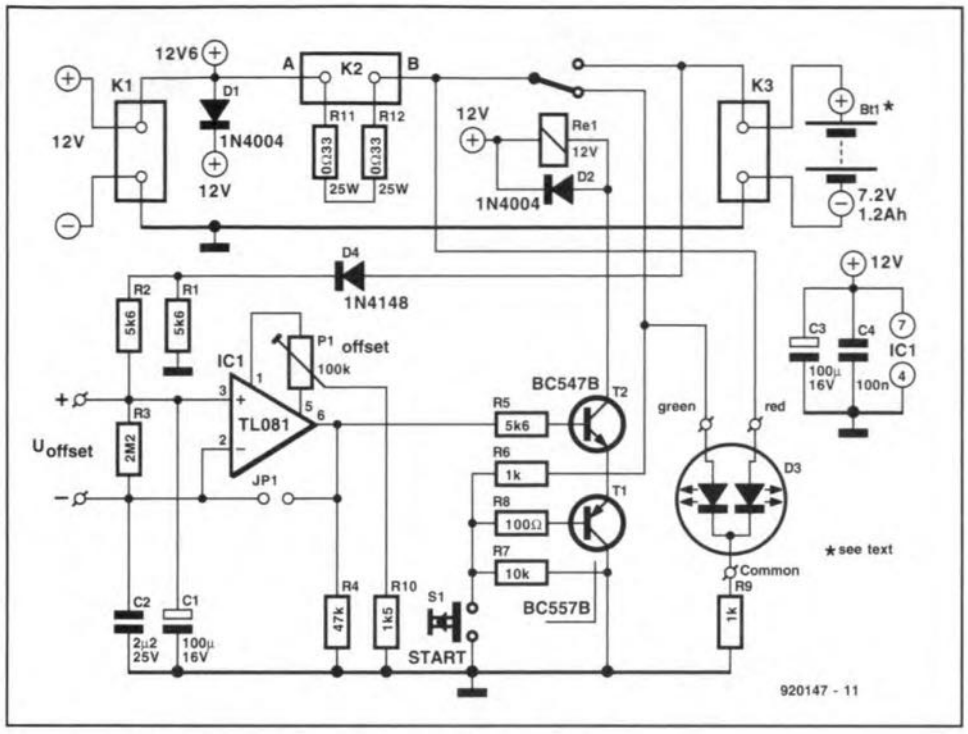


Fig. 2. Circuit diagram of the delta-peak NiCd battery charger.

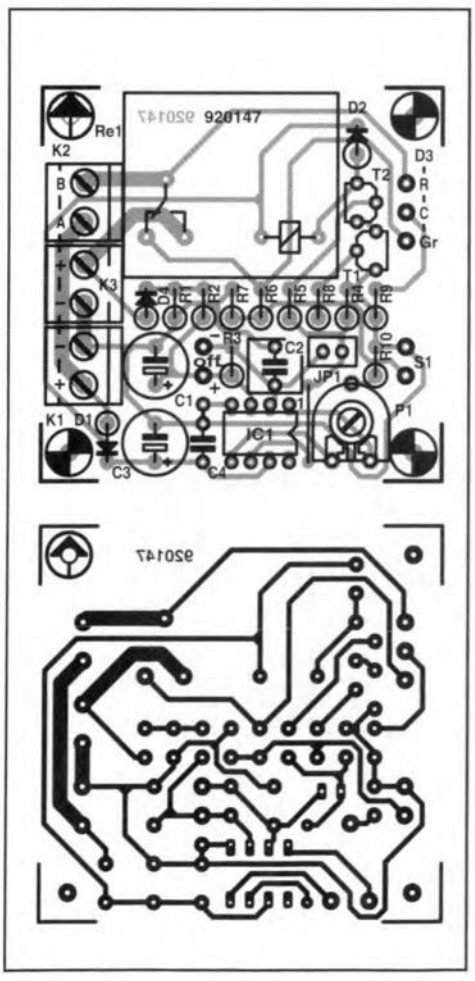


Fig. 3. Printed-circuit board for the delta-peak NiCd battery charger.

PARTS LIST

Resistors:
R1, R2, R5 = 5.6 kΩ
R3 = 2.2 MΩ
R4 = 47 kΩ
R6, R9 = 1 kΩ
R7 = 10 kΩ
R8 = 100 Ω
R10 = 1.5 kΩ
R11, R12 = 0.22 Ω, 25 W (see text)
P1 = 100 kΩ preset

Capacitors:
C1, C3 = 100 µF, 16 V, radial
C2 = 2.2 µF, 25 V
C4 = 100 nF (0.1 µF)

Semiconductors:
D1, D2 = 1N4004
D3 = two-colour LED
D4 = 1N4148
T1 = BC557B
T2 = BC547B
IC1 = TL081

Miscellaneous:
K1, K2, K3 = 2-way terminal block for PCB mounting, 5 mm grid
Re1 = 12 V, 8 A (car type) relay
S1 = single-pole push-button make switch

Operation

When the 12 V supply is on, but no charging is taking place, D_3 lights orange. When S_1 is pressed to start charging, and during charging, D_3 lights red. On completion of the charging, when the relay is deenergized, D_3 lights orange again. If something is wrong, D_3 does not light at all, of course.

If the NiCd battery to be charged is connected with incorrect polarity, the relay will clatter for an obvious remedy.

When a battery has been charged, wait about 20 seconds (to give C_2 time to discharge) before connecting the next battery to be charged to K_3.

Options

The circuit as shown in Fig. 2 is designed for a 7.2 V, 1.2 Ah NiCd battery. If batteries with a different voltage or capacity are to be charged, R_{11} and R_{12} must be suitably adapted. That requires some arithmetic, for which the stated battery properties can be used.

A 7.2 V, 1.5 Ah, 6-cell NiCd battery is fast-charged at 3.5–4.0 A. At that current, the charging voltage is some 1.6 V per cell. Together with the drop across the connecting cables and contacts, a total charging voltage of some 10 V is therefore required. Since the supply is 12–13 V, the resistors have to drop, say, 2.5 V. At a charging current as stated, that would need a resistance value of 0.72–0.63 Ω. This requirement is met by two 0.33 Ω resistors in series.

If another type of NiCd battery, say, a 6 V, 600 mA type, were to be charged the charging voltage would be around 8 V at a current of some 2 A. The power resistors would thus have to drop about 4.5 V; in other words, their combined resistance would have to be 2.25 Ω and this would be met by two 1.2 Ω resistors in series. Their rating, P, is calculated from $P=I^2R$, where I is the charging current and R the resistance. In the case stated, the rating of each resistor would have to be 5 W. ■

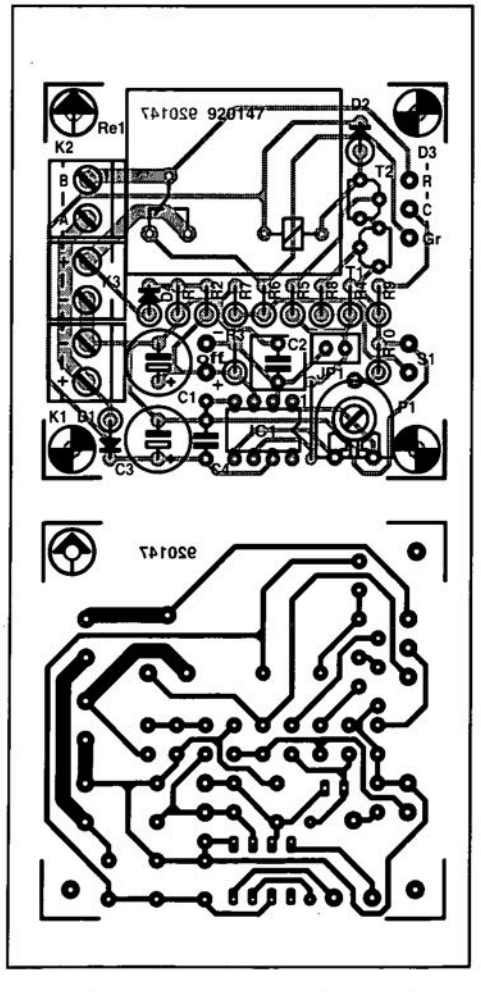


Fig. 3. Printed-circuit board for the delta-peak NiCd battery charger.

PARTS LIST

Resistors:
R1, R2, R5 = 5.6 kΩ
R3 = 2.2 MΩ
R4 = 47 kΩ
R6, R9 = 1 kΩ
R7 = 10 kΩ
R8 = 100 Ω
R10 = 1.5 kΩ
R11, R12 = 0.22 Ω, 25 W (see text)
P1 = 100 kΩ preset

Capacitors:
C1, C3 = 100 µF, 16 V, radial
C2 = 2.2 µF, 25 V
C4 = 100 nF (0.1 µF)

Semiconductors:
D1, D2 = 1N4004
D3 = two-colour LED
D4 = 1N4148
T1 = BC557B
T2 = BC547B
IC1 = TL081

Miscellaneous:
K1, K2, K3 = 2-way terminal block for PCB mounting, 5 mm grid
Re1 = 12 V, 8 A (car type) relay
S1 = single-pole push-button make switch

The circuit as shown in Fig. 2 is designed for a 7.2 V, 1.2 Ah NiCd battery. If batteries with a different voltage or capacity are to be charged, R_{11} and R_{12} must be suitably adapted. That requires some arithmetic, for which the stated battery properties can be used.

A 7.2 V, 1.5 Ah, 6-cell NiCd battery is fast-charged at 3.5–4.0 A. At that current, the charging voltage is some 1.6 V per cell. Together with the drop across the connecting cables and contacts, a total charging voltage of some 10 V is therefore required. Since the supply is 12–13 V, the resistors have to drop, say, 2.5 V. At a charging current as stated, that would need a resistance value of 0.72–0.63 Ω. This requirement is met by two 0.33 Ω resistors in series.

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DESIGN IDEAS

The contents of this article are based solely on information supplied by the author and do not imply practical experience by *Elekor*

DIGITAL BLACKJACK

AN EXERCISE IN SEQUENTIAL CIRCUIT DESIGN

This article describes each step in the design process of a digital machine that plays the card game of blackjack (also known as *vingt-et-un*). The machine is a synchronous sequential circuit, the functions of which are based on the rules of

By Robert F. Hodson

AS a teacher of digital systems I have found the game of blackjack to be an instructive example for individuals beginning to learn the principles of sequential circuit design. Choosing a game as a design project makes the circuit design fun for all. Typically at the end of a semester, the students will try to beat the dealer and their fellow classmates in a design contest. This gives added motivation for students to implement, not only a working system, but a design that proves itself superior. In this article I will describe the game of digital blackjack, and then present a typical solution to the problem. The solution will take the form of a synchronous sequential circuit, which will be explained shortly. The design process has a number of steps, but each step in itself is straightforward. After discussing these steps, I will endeavour to present some circuit implementations using typical digital devices.

What is digital blackjack?

Most people have played, or at least heard of, the card game blackjack. In the actual card game, the player gets one card face down and any number of cards face up. The object of the game is to get up to 21 points without going over 21. The point values for the cards are: 10 points for face cards, 1 point or 11 points for an ace (it is the player's choice) and the face value for all other cards. Going over 21 is called 'busting' and results in loosing the hand. The player requests another card by saying 'hit', and tells the dealer to stop dealing cards by saying 'stay'. The dealer also plays a hand, and the person closest to 21 is the winner. In the event of a tie score, the dealer wins. If you ask a serious card player, I am sure you will get a much longer description of the game, however for our purposes I think the above description is adequate.

Digital blackjack is a modified version of the card game. In this version, the dealer plays against a digital circuit with the card strategy built in. The circuit inputs the values of the cards, and determines whether another card is needed (take a hit), or to stop playing (stay). Since the actual card game would require a large number of inputs to represent all the different type cards in a deck, the modified game is played with only three types of cards: jacks worth 10 points, aces worth 11 points, and fives worth 5 points. I realize that this limits the strategy of the game considerably, but remember, the objective is to learn sequential circuit design, and if the problem is too large to fit on paper it does not make for a good working example. Also, as it turns out, this modified game is sophisticated enough to make a good competition. One more thing: as in regular blackjack, the players get to know the dealer's playing strategy. This allows the players to make informed choices in determining their own strategy. For your game, the dealer's strategy will be as follows:

1. If the dealer has less than 16,

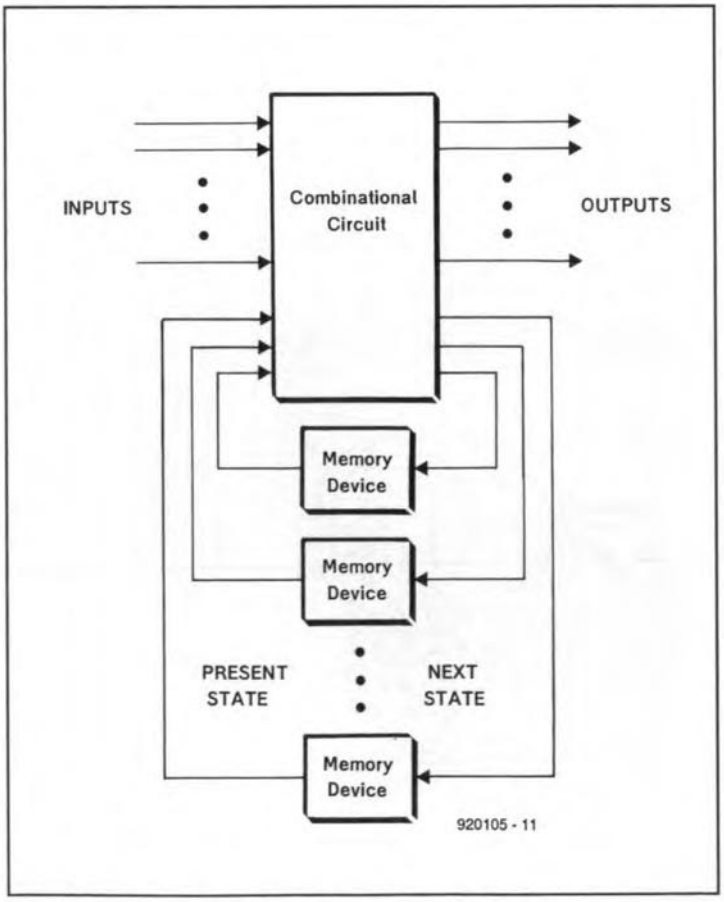


Fig. 1. Block diagram of a sequential circuit.

he will take a HIT;
2. If the dealer has 16 or more he will STAY.

With an understanding of the game and the strategy involved, let us now clarify the concept of sequential logic.

Sequential circuits

Before getting started on the design process, it is important that the overall concept of a sequential circuit is understood. Digital circuits can be classified as either combinational or sequential. The difference between these two is that the sequential circuit can 'remember'. In mathematical terms, this means that, for a sequential circuit, the outputs are a function of its present state and its inputs. In a combinational circuit, the outputs are a function of the inputs only. If you are not comfortable with the mathematical description, do not worry about it. I will explain it another way. The present state of a digital circuit is what the circuit remembers at any given point in time. The outputs of the circuit are dependent on the circuit's inputs and its present state. For example, a counter is a sequential circuit because to be able to go to the next count value, the circuit must remember its current count value. For a counter to count up to three, its present state must be two. Circuits that have outputs that depend on the current inputs and some state information are sequential circuits.

The other type of digital circuit is a combinational circuit. The outputs of combinational circuits are dependent only on the current inputs to the circuit. An adder would be an example of a typical combinational circuit. The output, which is the sum of the input values, only depends on the current input values. In generating a sum with a digital adder circuit, there is no need to remember past sums. Since there is no remembering of past inputs in determining the sum, the adder is a combinational circuit.

Figure 1 shows a block diagram of a sequential circuit. Note that the circuit consists of a combinational circuit connected with some memory devices. The memory devices hold the present state of the system. The inputs of the circuit are combined with present state signals to generate the outputs and the next state to be stored in the memory devices. Let us take the counter example again, and see how it fits into this general block diagram for a sequential circuit. Assume the counter has one digital input called COUNT. When COUNT is a logic 1, the counter increases — otherwise, when COUNT is a logic 0, the counter holds its current value. The current value of the counter is the present state of the sequential circuit, and is stored in the memory devices. The present state and COUNT are inputs to the combinational circuit, which is the next value in the counting sequence. In this simple example, the outputs of the circuit are equal to the next state of the circuit. In general, this may not be the case. The outputs may depend on both the inputs and the present state. One characteristic of sequential circuits worth noting at this point is the feedback path from the outputs of the combinational circuit, through the memory devices, back to the inputs of the combinational circuit. Whenever you see a digital circuit with a feedback path like this, you can immediately classify that circuit as a sequential circuit. The feedback in a sequential circuit is critical in making the circuit work. New information is stored in the memory, and is then input back into the circuit. This feedback mechanism is what makes a counter count from one, two, three, and so on.

One last point about sequential circuits. There are actually two types of sequential circuit: synchronous and asynchronous. Synchronous sequential circuits are more commonly found in systems today. The fundamental difference between a synchronous and an asynchronous sequential circuit is the presence of a clock signal. The clock is a periodic timing signal that coordinates the loading of the memory devices. When the memory devices are synchronized with the clock, the next state of the circuit changes at discrete intervals in time. Synchronous sequential circuits are, in general, easier to design, have fewer noise problems and are less critical as regards timing. The rest of this article will focus on synchronous sequential circuits.

The design process

I will now proceed with the design of the digital blackjack circuit. The following is a list of the steps in the design process. The list looks fairly long, but do not let that deter you, because each step is straightforward. Due to the number of steps involved in the design of sequential circuits, it is not a bad idea to make yourself a check list to ensure you do not overlook a step in the deign process.

Design step	Completed
1. Understand the problem	❑
2. Determine a strategy	❑
3. Identify inputs and outputs	❑
4. Determine the state diagram	❑
5. Make a state assignment	❑
6. Derive the state table	❑
7. Minimize the state table	❑
8. Select a memory device	❑
9. Determine next state equations	❑
10. Determine the output equations	❑
11. Implement the circuit	❑

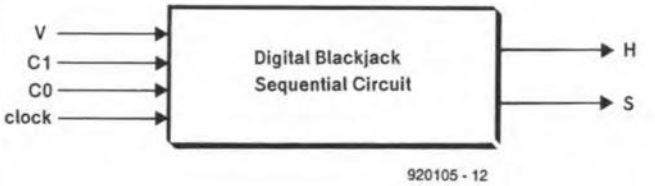
Understanding the problem

I know this is obvious. Who would design a digital circuit to solve a problem they did not understand? Most people would not deliberately do this, but it is all too common that people proceed with a design without fully understanding what is asked for. Misunderstandings early in the design process cause costly revisions later on. In every design, the bulk of the design effort should be spent at the beginning. This requires the designer to be patient. The designer should think through the problem several times before proceeding. Just like programmers like to go right to coding a solution, hardware designers love to get to a circuit implementation. Avoid the temptation! Think through your design and proceed slowly.

Determining a strategy

In the description of the digital blackjack game, the dealer's strategy is given. In this problem, you need to determine a playing strategy to try and beat the dealer. This in itself is not a trivial problem. Just like in the regular blackjack game, there are odds to be considered. There are a number of ways to determine a successful playing strategy, including statistical analysis, simulations or simply playing experience. Since the focus of this exercise is not card playing, but circuit design, I will simply state the strategy implemented in this design.

1. If the point total is 16 or



Input description

V	C1	C0	Meaning
0	X	X	Card input not valid
1	0	0	Card is a Five
1	0	1	Card is a Jack
1	1	0	Card is an ace
1	1	1	Unused input combination

Output description

H	S	Meaning
0	0	Do nothing (undefined)
0	1	Stay (stop requesting cards)
1	0	Hit (request a card)
1	1	Invalid output combination

Fig. 2. Input-output definitions.

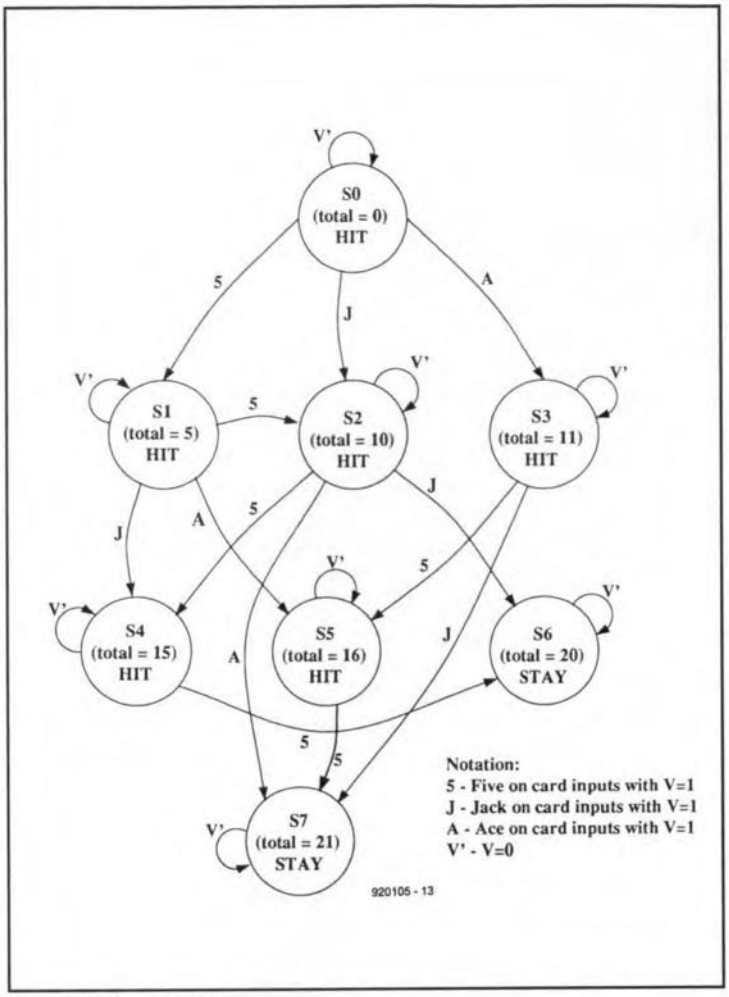


Fig. 3. State diagram.

State	Q2 Q1 Q0	Meaning
S0	0 0 0	Point total = 0, start state
S1	0 0 1	Point total = 5
S2	0 1 0	Point total = 10
S3	0 1 1	Point total = 11
S4	1 0 0	Point total = 15
S5	1 0 1	Point total = 16
S6	1 1 0	Point total = 20
S7	1 1 1	Point total = 21

Table 1. State assignment.

less, the circuit will request a HIT.
2. Otherwise, STAY.

In general, determining the playing strategy in this design corresponds to determining a control algorithm in a more sophisticated system. Again, you should take your time, and verify the algorithm you want to implement before proceeding.

Identify inputs and outputs

Figure 2 is a high-level block diagram showing the inputs and outputs of the circuit. In playing digital blackjack, there are three types of cards: jacks, aces and fives. These three classes of cards can be encoded with two digital signals, C1 and C0, which represent the card information. A third input, V, is use as a qualifier for the card inputs. When V is a logic 1, the card inputs are said to be valid. I will assume V goes to a logic 1 for only one clock period when a new card is played. If you do not understand the need for V right now, bear with me, and it will become apparent later on in the design. Hold it right there! '*It will become apparent later on in the design*', I bet you think I am trying to pull a fast one on you. To tell you the truth, the first time I designed this circuit, I did not see the need for the V signal until later on in the design. That is not uncommon. A good idea is often an iterative process. You should notice two other features in Fig. 2. First, the clock is shown as an input. Remember that all asynchronous sequential circuits require a periodic clock signal to control the transition between states. Second, notice the X's in the input description — they are a shorthand notation that means the input can take on any value.

With a feeling for the inputs, let us proceed to identify the output signals. The digital blackjack circuit must be able to respond HIT or STAY. I chose to use two correspondingly named outputs, H for HIT, and S for STAY. These signals are mutually exclusive, meaning only one is logic 1 at any time. This makes sense since it would be an error if the game requested a HIT at the same time it indicated STAY. The HIT/STAY output information can actually be encoded in a single output signal, but I kept the outputs separate so they could independently drive LED indicator lights.

Determine the state diagram

The next step in the process is to determine the state diagram for the system. A state diagram is a graph that has circles which represent the states of the sequential circuit, and shows the output for each state. Remember that the states are just what the circuit has in its memory at any point in time, and for this system the outputs are H (HIT) and S (STAY). Directed arcs are used to show valid next states from any given state for the various input combinations of C1, C0 and V. Let us take a specific example. In this circuit, the information associated with each state will be the current point total of the cards that have been played. Assume a game is just beginning, and the circuit is in the starting state, S0 (refer to Fig. 3). While in S0, the circuit sets the H signal requesting a HIT. Say that the first card received is a Five. The card input combination (C1, C0) will represent a Five, and V will go to logic 1 indicating there is a valid card. On the state diagram, this state transition is represented by an arc from S0 to S1, where S0 'remembers' the initial point total is zero, and S1 indicates the new point total is five. The other arcs coming from S0 indicate the other next state transitions from this initial state. The label 'J' indicates a valid Jack on the card inputs, while the arc labelled 'A' indicates a valid Ace. The arc labelled 'V' indicates that the circuit will wait in S0 until a valid card is given. The circuit continues to request cards until it reaches a state with a point total of more than 16. This sets the S signal, indicating to the dealer that no more cards are required (STAY).

The reason for the V input can now be explained. Notice that V is used to make the circuit wait in a state until a valid card input is given. In a synchronous sequential circuit, a state transition can be made every clock period. The V signal is one clock period long, therefore only allowing one state transition each time the V signal qualifies the card input. This is a subtle point, but it is important to understand to see how the circuit operates. Without the V signal, the card inputs would be sampled each clock period, and the circuit would move from state to state, accumulating an incorrect total score. These inappropriate state transitions would happen rapidly, since digital clock frequencies typically are in the megahertz (MHz) range. The end result would be a circuit that did not perform as expected.

For clarity, several arcs are left off Fig. 3. In general, a state diagram would have an arc leaving each state for each input combination. Since the digital blackjack circuit has three inputs (C0, C1 and V), the complete state diagram would require eight arcs leaving each state. Since this would quickly become difficult to read, the arcs travelling back to the start state, S0, are omitted. Also, the arcs labelled V' actually indicate four arcs, one for each card combination while V=0.

Make a state assignment

The state diagram of Fig. 3 is

an abstract description of how the circuit will operate. The symbols A, J, 5 and V' were used to represent the inputs of the circuit; HIT and STAY to represent the outputs, and S0 through S7 to represent the states of the system. Definitions of the inputs and outputs were given earlier. The state information must also be encoded in binary form for implementation in a digital circuit. There are eight states in this circuit. A unique binary code must be assigned to each state of the system. Three bits (binary digits) are needed to encode eight (2^3) states. Refer to Table 1 for the state assignment. This is somewhat arbitrary, but it is a good idea to make the initial state of the system zero. By assigning zero to the start state, we will find out later that it is very easy to reset the circuit. The three new terms, Q2, Q1 and Q0, introduced in the state table are called state variables. Eventually, these will be the output signals of the circuit's memory devices. If you think about that, it makes sense: the circuit's memories hold the state information, and this information is encoded in three memory outputs by the values of Q2, Q1, Q0.

With the state assignment complete, all of the inputs, outputs and states have been given a binary encoding. The binary patterns can be represented as digital signals in the final circuit. The next logical step in the design sequence is how to combine the binary input, output and state information with the playing strategy defined in the state diagram. This combined information will be put in the state table.

Q2 Q1 Q0	C1 C0 V	Y2 Y1 Y0	H S	Comment
0 0 0	x x 0	0 0 0	1 0	S0, waiting for valid card input, output HIT
0 0 0	0 0 1	0 0 1	1 0	S0, valid 5 on card inputs, next state S1, output HIT
0 0 0	0 1 1	0 1 0	1 0	S0, valid Jack on card inputs, next state S2, output HIT
0 0 0	1 0 1	0 1 1	1 0	S0, valid Ace on card inputs, next state S3, output HIT
0 0 0	1 1 1	0 0 0	1 0	S0, undefined input, next state S0, output HIT
0 0 1	X X 0	0 0 1	1 0	S1, waiting for valid card input, output HIT
0 0 1	0 0 1	0 1 0	1 0	S1, valid 5 on card inputs, next state S2, output HIT
0 0 1	0 1 1	1 0 0	1 0	S1, valid Jack on card inputs, next state S4, output HIT
0 0 1	1 0 1	1 0 1	1 0	S1, valid Ace on card inputs, next state S5, output HIT
0 0 1	1 1 1	0 0 0	1 0	S1, undefined input, next state S0, output HIT
0 1 0	X X 0	0 1 0	1 0	S2, waiting for valid card input, output HIT
0 1 0	0 0 1	1 0 0	1 0	S2, valid 5 on card inputs, next state S4, output HIT
0 1 0	0 1 1	1 1 0	1 0	S2, valid Jack on card inputs, next state S6, output HIT
0 1 0	1 0 1	1 1 1	1 0	S2, valid Ace on card inputs, next state S7, output HIT
0 1 0	1 1 1	0 0 0	1 0	S2, undefined input, next state S0, output HIT
0 1 1	X X 0	0 1 1	1 0	S3, waiting for valid card input, output HIT
0 1 1	0 0 1	1 0 1	1 0	S3, valid 5 on card inputs, next state S5, output HIT
0 1 1	0 1 1	1 1 1	1 0	S3, valid Jack on card inputs, next state S7, output HIT
0 1 1	1 0 1	0 0 0	1 0	S3, valid Ace on card inputs, next state S0, output HIT
0 1 1	1 1 1	0 0 0	1 0	S3, undefined input, next state S0, output HIT
1 0 0	X X 0	1 0 0	1 0	S4, waiting for valid card input, output HIT
1 0 0	0 0 1	1 1 0	1 0	S4, valid 5 on card inputs, next state S6, output HIT
1 0 0	0 1 1	0 0 0	1 0	S4, valid Jack on card inputs, next state S0, output HIT
1 0 0	1 0 1	0 0 0	1 0	S4, valid Ace on card inputs, next state S0, output HIT
1 0 0	1 1 1	0 0 0	1 0	S4, undefined input, next state S0, output HIT
1 0 1	X X 0	1 0 1	0 1	S5, waiting for valid card input, output STAY
1 0 1	0 0 1	1 1 1	0 1	S5, valid 5 on card inputs, next state S7, output STAY
1 0 1	0 1 1	0 0 0	0 1	S5, valid Jack on card inputs, next state S0, output STAY
1 0 1	1 0 1	0 0 0	0 1	S5, valid Ace on card inputs, next state S0, output STAY
1 0 1	1 1 1	0 0 0	0 1	S5, undefined input, next state S0, output STAY
1 1 0	X X 0	1 1 0	1 0	S6, waiting for valid card input, output HIT
1 1 0	0 0 1	0 0 0	1 0	S6, valid 5 on card inputs, next state S0, output HIT
1 1 0	0 1 1	0 0 0	1 0	S6, valid Jack on card inputs, next state S0, output HIT
1 1 0	1 0 1	0 0 0	1 0	S6, valid Ace on card inputs, next state S0, output HIT
1 1 0	1 1 1	0 0 0	1 0	S6, undefined input, next state S0, output HIT
1 1 1	X X 0	1 1 1	0 1	S7, waiting for valid card input, output STAY
1 1 1	0 0 1	0 0 0	0 1	S7, valid 5 on card inputs, next state S0, output STAY
1 1 1	0 1 1	0 0 0	0 1	S7, valid Jack on card inputs, next state S0, output STAY
1 1 1	1 0 1	0 0 0	0 1	S7, valid Ace on card inputs, next state S0, output STAY
1 1 1	1 1 1	0 0 0	0 1	S7, undefined input, next state S0, output STAY

Table 2. State table.

Derive the state table

Now it is time to combine all the bits and pieces of the design into a single unified form, the state table. This step requires rewriting the information you already know. The state table shows the next state and output of the circuit for each present state and input. That is not so bad. We know that all the input combinations, we know how many states there are, and their state assignments. We also know the encoding of the output signals, and the state diagram shows the relationships between states, inputs and outputs.

Table 2 is a state table for the digital blackjack circuit. All possible present states are listed under 'Q2 Q1 Q0', along with each output combination under 'C1 C0 V'. On the right half of the table, the next state, denoted Y2 Y1 Y0, and outputs 'H' and 'S' are given. Let me explain the entries made for one of the states to clarify the meaning of the state table. I will explain the five rows associated with present state S3 as an example. You will need to refer back to Fig. 2, the input/output definitions, Figure 3, the state diagram, and Table 1, the state assignment.

The state assignment for S3 is 011. If you look under 'Q2 Q1 Q0' for the five rows beginning with present state 011, you will be at the right place in the state table. Let us starts with the second row of these five with the entry:

011 001 101 10

This row can be read back as: 'while in state S3, output HIT, and if a valid Five is input, go to the next state of S5'. To see how I came up with this interpretation, decode the binary patterns to their original meaning. 'Q2 Q1 Q0' = 011 means the present state is S3; 'C1 C0 V' = 001 means a valid Five is input; 'Y2 Y1 Y0' = 101 means the next state is S5, and 'H S' = 10 means HIT. Note that the action described corresponds directly to the state diagram. Actually, that is how I figured out what to put in the state table. I started with the state diagram, and displayed it in tabular form using the signal encoding presented previously. The meanings of all five rows associated with present state S3 are as follows:

011 XX0 011 10:
while in state S3, output HIT and if V=0 stay in state S3.

011 001 101 10:
while in state S3, output HIT and if a valid Five is input go to the next state of S5.

011 011 111 10:
while in state S3, output HIT and if a valid Jack is input go to the next state of S7.

Q2	Q1	Q0	C1	C0	V	Y2	Y1	Y0	H	S	Comment
0	0	0	x	x	0	0	0	0	1	0	S0, waiting for valid card input, output HIT
0	0	0	0	0	1	0	0	1	1	0	S0, valid 5 on card inputs, next state S1, output HIT
0	0	0	0	1	1	0	1	0	1	0	S0, valid Jack on card inputs, next state S2, output HIT
0	0	0	1	0	1	0	1	1	1	0	S0, valid Ace on card inputs, next state S3, output HIT
0	0	0	1	1	1	0	0	0	1	0	S0, undefined input, next state S0, output HIT
0	0	1	X	X	0	0	0	1	1	0	S1, waiting for valid card input, output HIT
0	0	1	0	0	1	0	1	0	1	0	S1, valid 5 on card inputs, next state S2, output HIT
0	0	1	0	1	1	1	0	0	1	0	S1, valid Jack on card inputs, next state S4, output HIT
0	0	1	1	0	1	1	0	1	1	0	S1, valid Ace on card inputs, next state S5, output HIT
0	0	1	1	1	1	0	0	0	1	0	S1, undefined input, next state S0, output HIT
0	1	0	X	X	0	0	1	0	1	0	S2, waiting for valid card input, output HIT
0	1	0	0	0	1	1	0	0	1	0	S2, valid 5 on card inputs, next state S4, output HIT
0	1	0	0	1	1	1	1	0	1	0	S2, valid Jack on card inputs, next state S6, output HIT
0	**1**	**0**	**1**	**0**	**1**	**1**	**1**	**1**	**1**	**0**	**S2, valid Ace on card inputs, next state S6, output HIT**
0	1	0	1	1	1	0	0	0	1	0	S2, undefined input, next state S0, output HIT
0	1	1	X	X	0	0	1	1	1	0	S3, waiting for valid card input, output HIT
0	1	1	0	0	1	1	0	1	1	0	S3, valid 5 on card inputs, next state S5, output HIT
0	**1**	**1**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**0**	**S3, valid Jack on card inputs, next state S6, output HIT**
0	1	1	1	0	1	0	0	0	1	0	S3, valid Ace on card inputs, next state S0, output HIT
0	1	1	1	1	1	0	0	0	1	0	S3, undefined input, next state S0, output HIT
1	0	0	X	X	0	1	0	0	1	0	S4, waiting for valid card input, output HIT
1	0	0	0	0	1	1	1	0	1	0	S4, valid 5 on card inputs, next state S6, output HIT
1	0	0	0	1	1	0	0	0	1	0	S4, valid Jack on card inputs, next state S0, output HIT
1	0	0	1	0	1	0	0	0	1	0	S4, valid Ace on card inputs, next state S0, output HIT
1	0	0	1	1	1	0	0	0	1	0	S4, undefined input, next state S0, output HIT
1	0	1	X	X	0	1	0	1	0	1	S5, waiting for valid card input, output HIT
1	**0**	**1**	**0**	**0**	**1**	**1**	**1**	**1**	**0**	**1**	**S5, valid 5 on card inputs, next state S6, output HIT**
1	0	1	0	1	1	0	0	0	0	1	S5, valid Jack on card inputs, next state S0, output HIT
1	0	1	1	0	1	0	0	0	0	1	S5, valid Ace on card inputs, next state S0, output HIT
1	0	1	1	1	1	0	0	0	0	1	S5, undefined input, next state S0, output HIT
1	1	0	X	X	0	1	1	0	1	0	S6, waiting for valid card input, output STAY
1	1	0	0	0	1	0	0	0	1	0	S6, valid 5 on card inputs, next state S0, output STAY
1	1	0	0	1	1	0	0	0	1	0	S6, valid Jack on card inputs, next state S0, output STAY
1	1	0	1	0	1	0	0	0	1	0	S6, valid Ace on card inputs, next state S0, output STAY
1	1	0	1	1	1	0	0	0	1	0	S6, undefined input, next state S0, output STAY

Table 3. Reduced state table.

011 101 000 10:
while in state S3, output HIT and if a valid Ace is input go to the next state of S0.

011 111 000 10:
while in state S3, output HIT and if an undefined card input is given go to the next state of S0.

The first, fourth and fifth of these descriptions require a little further explanation. The first row shows the circuit will stay in state S3 as long as V is a logic 0. This signifies that present card inputs are not valid. This one table entry is actually a shorthand notation for four rows in the table. The X's can be written out explicitly as the four possible combinations of the card inputs. Note also that the fourth row does not directly correspond to an arc on the state diagram. If you remember, to make the state diagram more readable, I left off the arcs returning to the initial state, S0. The fourth row of the table corresponds to one of these arcs. In the context of the game, this would mean that two aces were received, resulting in a 'bust' condition, and the circuit would reset to state S0. The fifth row also does not correspond to an arc leaving S3 in the state table. Notice I set the next state to state S0, just like in the previous case. This works just fine, but was not a required state transition for the circuit to operate correctly. I could have just as easily defined the next state in this case to be some other value. The flexibility in state assignment exists in this case because the input combination should never occur if the circuit is being operated correctly. Remember that the card inputs equal to logic combination '11' were left undefined.

Minimize the state table

The next step in the process is to minimize the state table. As it turns out, this step is optional in obtaining a working design, but does serve to minimize the hardware in the final circuit. In any design, it is always possible that the designer introduced redundant states in making the state diagram. A state is redundant if it can be combined with another state without losing any information. The rule for combining redundant states has the following two parts. Two states can be combined to a single equivalent state if for every input combination (1) the outputs produced by the two original states are the same, and (2) the next states are equivalent.

Figure 4 shows the initial (a) and final (b) implication tables for the digital blackjack circuit. An implication table is used to identify equivalent states that can be combined. Each block in an implication table represents one of all the possible state pairs. The initial ✗'s in Fig. 4a represent state pairs that can not be combined based on part one of the above rule. The table shows that state S0 through S5 can not be combined with either S6 or S7 because their outputs differ. The other blocks in the implication table are used in applying part two of the state equivalency rule. Each block lists the pairs of next states that must be equivalent for the two associated present states to be equivalent. Let us take a closer look at the top block in Fig. 4a. The meaning of the block is: 'S0 and S1 are equivalent states if S0 and S1 are equivalent, S1 and S2 are equivalent, S2 and S4 are equivalent, and S3 and S5 are equivalent. The next state pairs for that block were determined by looking at the next states for S0 and S1 for each possible input combination. For example, in S0 with input 001, the next state is S1, and for S1 with input 001, the next state is S2. Therefore for S0 and S1 to be equivalent, so must S1 and S2. This is represented by putting the pair (1,2) in the block for the S0/S1 pair.

After I completed the initial implication table, I made successive passes over the table, placing an ✗ in any block that had at least one state pair that had already been shown not to be equivalent. The final implication table is given in Fig. 4b. The final table shows that only states S6 and S7 can be combined. If you think about how states S6 and S7 are used, this makes sense. Both S6 and S7 output STAY, and return to the initial state S0 on all valid card combinations. The state table can now be reduced. I chose to combine states S6 and S7 by removing S7 from the state table, and replacing all references to S7 with references to S6. The new state table is given in Table 3. The changes from the original state table are given in bold print.

I should note before proceeding that, in general, multiple states can be combined into single states. This requires merging equivalent states into larger equivalency groups. Also, in this example, I defined

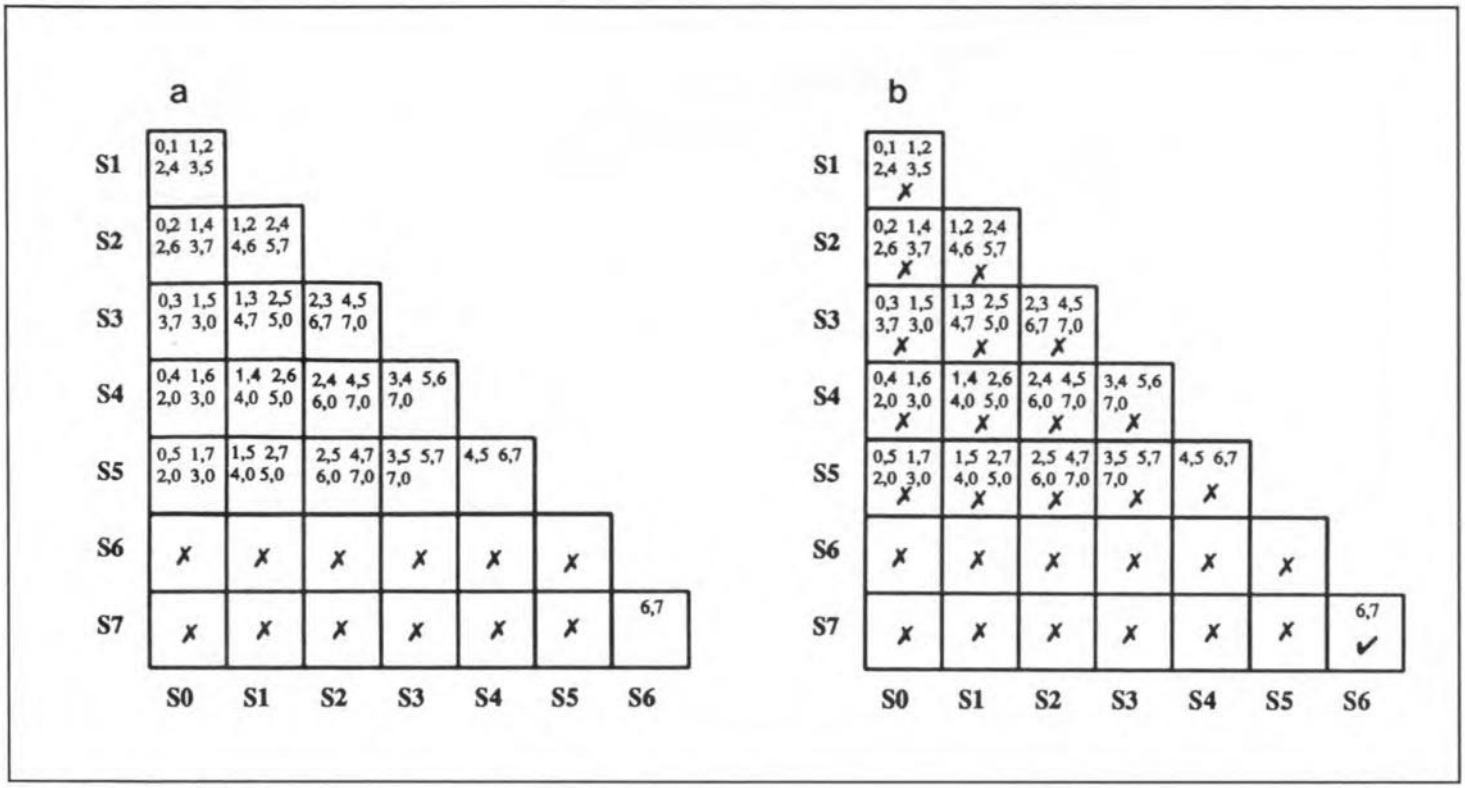


Fig. 4. Implication tables.

all next states and outputs for each combination. When all next states and outputs are defined, this circuit is said to be completely specified. When a circuit is not completely specified, a similar approach using the concept of compatible states can be used for the state reduction process.

Determine the next state equations

Now is good place for a sanity check. Take a deep breath. If you have gotten this far you are doing great. Trust me, it is down hill from here, mostly just a little combinational circuit design is left. For the next step, determining the next state equations, you must select a memory device. Memory devices that store a single bit of information in synchronous sequential circuits are called flip-flops. A designer actually has several types of flip-flop to select from: S-R, J-K and D flip-flops, to name a few. In this example I chose to use D flip-flops because they simplify the derivation of the next state equations. In the case when D flip-flops are the memory devices, the state table directly describes the input functions for the flip-flops. The next state variables Y2, Y1 and Y0 are presented in the state table as a function of the present state (Q2, Q1, Q0) and the inputs (C1, C0, V). The 1's of the functions appear as product terms in the next state equations. The individual present state and input variables associated with each product term are complemented or left uncomplemented to correspond to their respective 1 and 0 patterns. The next state equations are given in Table 4.

Notice that these equations have not been minimized. A variety of techniques can be used to minimize the equations. There are computer programs to perform Quine-McClusky minimization, or you could always algebraically minimize, or use a six-variable Karnaugh map. I will leave the equations in their present form since this is suitable for some implementations.

Determine output equations

The output equations, like the next state equations, can be derived directly from the state table. The observation that the outputs are only a function of the present state greatly simplifies the number of terms in the output equations. Had you not made this observation, minimizing the equations would have shown this to be the case. The equations given here are still not minimal, but their form nicely reflects the expected output function of the circuit. The equation for 'H' can be stated as 'give me a hit if I am in state S0 (total=0) or S1 (total=5) or S2 (total=10) or S3 (total=11) or S4 (total=15) or S5 (total=16)'. Notice that this corresponds to the original playing strategy of taking a card for a total of 16 or less. Similarly, the equation for 'S' can be stated as 'I want to stay if I am in state 6'. Remember, S6 was the original S6 (total=20) and S7 (total=21). You should always try to make physical sense out of your equations to help you catch errors. The first time I designed this circuit, I caught a design error right at this point by noticing that my output equations did not correspond to the playing strategy. The output equations are given in Table 5.

$$
\begin{aligned}
Y2 = {} & Q2'\cdot Q1'\cdot Q0\cdot C1'\cdot C0\cdot V + Q2'\cdot Q1'\cdot Q0\cdot C1\cdot C0'\cdot V + Q2'\cdot Q1\cdot Q0'\cdot C1'\cdot C0'\cdot V + \\
& Q2'\cdot Q1\cdot Q0'\cdot C1'\cdot C0\cdot V + Q2'\cdot Q1\cdot Q0'\cdot C1\cdot C0'\cdot V + Q2'\cdot Q1\cdot Q0\cdot C1'\cdot C0'\cdot V + \\
& Q2'\cdot Q1\cdot Q0\cdot C1'\cdot C0\cdot V + Q2\cdot Q1'\cdot Q0'\cdot V' + Q2\cdot Q1'\cdot Q0'\cdot C1'\cdot C0'\cdot V + Q2\cdot Q1'\cdot Q0\cdot V' + \\
& Q2\cdot Q1'\cdot Q0\cdot C1'\cdot C0'\cdot V' + Q2\cdot Q1\cdot Q0'\cdot V' \\
\\
Y1 = {} & Q2'\cdot Q1'\cdot Q0'\cdot C1'\cdot C0\cdot V + Q2'\cdot Q1'\cdot Q0'\cdot C1\cdot C0'\cdot V + Q2'\cdot Q1'\cdot Q0\cdot C1'\cdot C0'\cdot V + \\
& Q2'\cdot Q1\cdot Q0'\cdot V' + Q2'\cdot Q1\cdot Q0'\cdot C1'\cdot C0\cdot V + Q2'\cdot Q1\cdot Q0'\cdot C1\cdot C0'\cdot V + \\
& Q2'\cdot Q1\cdot Q0\cdot V' + Q2'\cdot Q1\cdot Q0\cdot C1'\cdot C0\cdot V + Q2\cdot Q1'\cdot Q0'\cdot C1'\cdot C0'\cdot V + \\
& Q2\cdot Q1'\cdot Q0\cdot C1'\cdot C0'\cdot V + Q2\cdot Q1\cdot Q0'\cdot V' \\
\\
Y0 = {} & Q2'\cdot Q1'\cdot Q0'\cdot C1'\cdot C0'\cdot V + Q2'\cdot Q1'\cdot Q0'\cdot C1\cdot C0'\cdot V + Q2'\cdot Q1'\cdot Q0\cdot V' + \\
& Q2'\cdot Q1'\cdot Q0\cdot C1\cdot C0'\cdot V + Q2'\cdot Q1\cdot Q0\cdot V' + Q2'\cdot Q1\cdot Q0\cdot C1'\cdot C0'\cdot V + Q2\cdot Q1'\cdot Q0\cdot V' + \\
& Q2'\cdot Q1'\cdot Q0\cdot C1\cdot C0'\cdot V + Q2'\cdot Q1\cdot Q0\cdot V' + Q2'\cdot Q1\cdot Q0\cdot C1'\cdot C0'\cdot V + Q2\cdot Q1'\cdot Q0\cdot V'
\end{aligned}
$$

Table 4. Next state equations.

$$
\begin{aligned}
H = {} & Q2'\cdot Q1'\cdot Q0' + Q2'\cdot Q1'\cdot Q0 + Q2'\cdot Q1\cdot Q0' + Q2'\cdot Q1\cdot Q0 + Q2\cdot Q1'\cdot Q0' + \\
& Q2\cdot Q1'\cdot Q0 \\
\\
S = {} & Q2\cdot Q1\cdot Q0'
\end{aligned}
$$

Table 5. Output equations.

Implementation

Once the next state and output equations have been determined, there are a variety of

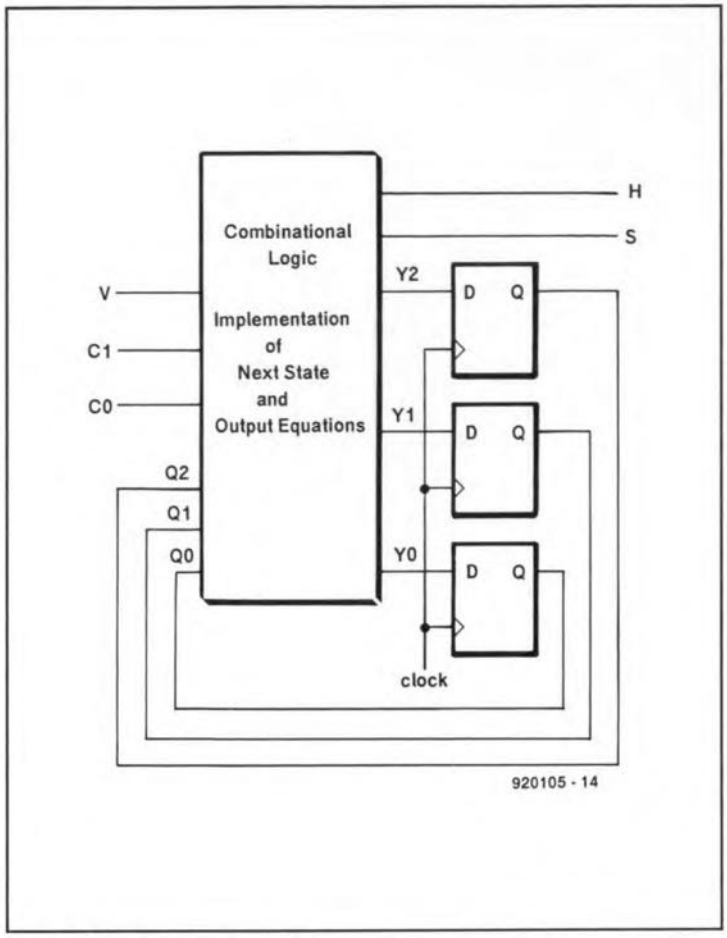


Fig. 5. Circuit implementation.

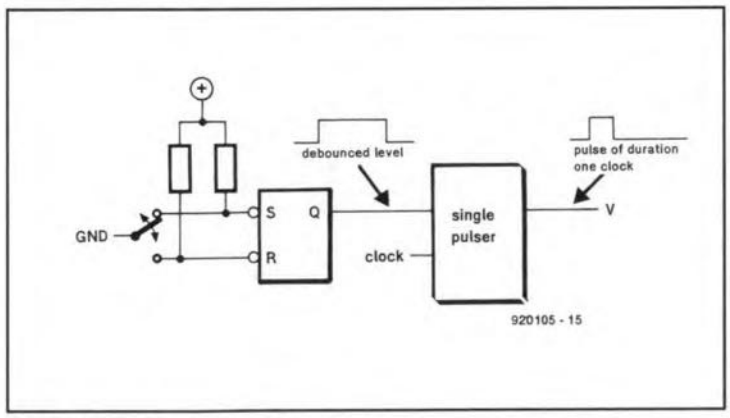


Fig. 6. Circuit to generate V.

methods available for circuit implementation. The basic structure of the circuit with D flip-flops is given in Fig. 5. The combinational logic can be implemented in any of the following methods:

1. Discrete components
2. PAL or PLD
3. PROM or EPROM

If you choose to implement the circuit in discrete components, the ANDs and ORs of the next state and output equations translate directly to gates. For a discrete component implementation, it is recommended that you first minimize the equations.

For PAL or PLD implementation, most development systems have an equation entry method which allows you to directly enter the logic equations. The development systems will also perform logic minimization if you choose to enable that option. Therefore, there is no need to reduce the equations by hand. Many PLDs also allow for registered outputs. If you use a registered PLD, the external flip-flops shown in Fig. 5 would actually be inside the PLD. Furthermore, some PLD development systems allow you to directly enter a state diagram or state table. If you have a development system with state entry and state minimization capability, the design process can be significantly shortened.

One last implementation method would be a PROM (or EPROM) based combinational logic circuit. In a PROM implementation, the inputs and present state variables are connected to the address inputs of the PROM. The PROM's outputs become the circuit's next state variables and outputs. The program for the PROM can be taken directly from the state table since that describes the next state and output for each present state and input (PROM addresses).

Practical considerations and loose ends

At last, the sequential circuit design process is complete. Let me conclude with just a few final suggestions. If the H and S outputs are used to drive LEDs, you should buffer the signals with high-current inverters, and put current limiting resistors in series with the LEDs. The card inputs can be connected to simple switches that connect to power or ground.

Any sequential circuit may initially power up in a random state. For the circuit to operate properly, it must start in state S0. The way the circuit was designed, it can easily be reset by setting the input to C1 C0 V = 111. All the states of the system are designed to go back to state S0 in this case. In general, there may not be unused input combinations to use as a reset condition. An alternate method for initializing the system to the reset state is to use flip-flops with 'clear' inputs. If you make the state assignment with the circuit's starting state equal to zero, clearing the flip-flops resets the circuit.

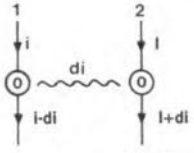
The V input is a little trickier than the other inputs. Remember, V should go valid for only one clock period to qualify the card inputs. You can connect a switch to an S-R latch used to debounce the switch (Fig. 6). The output of the S-R latch will be a level that is valid for the time the switch is closed. Next, you need to change the level into a single clock pulse. Well, it turns out that the single pulse circuit is a very simple synchronous sequential circuit with one input and one output. So why not try putting into practice the design method you just read about, and design yourself a 'single pulser'? Remember, just proceed one step at a time! ■

SCIENCE & TECHNOLOGY

A MODEL ANALYSIS
Scaling: the control element method for electronics

By Michael Soper, MA (Keele)

Control elements in electronics often use a small current to control a large one. In fact, this is such a common situation that there is a need for general methods. The common situation is



where system 1 donates a very small current to node 2. Although this may seem obvious and simple, note that di is so small that d^2 is neglectable; d is therefore termed square-neglectable. In this article, a control element logic will be developed and tied in with a calculus of square-neglectable qualities.

Why is this best?

General methods have always proved themselves more powerful than particular ones, mainly because they can more easily be adapted to new situations. Thus, this new approach should prove both flexible and useful.

Let $a=I+\mathrm{j}\mathrm{d}I$; then, $|a|=\sqrt{(I^2+0)}=I$. As usual, $a\bar{a}=|a|^2$. Also, $a^2=I^2+2\mathrm{j}\mathrm{d}I\cdot I=I(2a-I)$. Thus, a is the geometric mean of $|a|$ and $2a-|a|$.

Let $b=i+\mathrm{j}\mathrm{d}i$; then, $ab=iI-\mathrm{d}^2iI+\mathrm{j}(I\mathrm{d}i+i\mathrm{d}I)$. Thus, $ab=\mathrm{j}(I\mathrm{d}i+i\mathrm{d}I)+iI$, $R\ell(ab)=R\ell(a)R\mathrm{l}(b)$, and $I_m(ab)=R\ell(a)I_m(b)+R\ell(b)I_m(a)$.

The second feature is that di=id, where d is the square-neglectable quantity. Hence, we may also write: $ab=iI+\mathrm{j}(I\mathrm{d}i+i\Lambda I)$, since d$\Lambda$ is also square-neglectable where $a=I+\mathrm{j}\Lambda I$.

Care must be taken not to divide by the difference of square-neglectable quantities. We are then dealing with a quantity like a tolerance which cannot indefinitely be summed or multiplied, and definitely cannot be subtracted when the plan is next to divide by the result. Note that 'nd' is not square-neglectable when n is large.

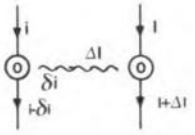
For example, if d–Λ has a value, then $1/(\mathrm{d}-\Lambda)$ is defined and $(\mathrm{d}+\Lambda)/(\mathrm{d}^2-\Lambda^2)$ exists, but $\mathrm{d}^2=0$ and $\Lambda^2=0$, so that $(\mathrm{d}+\Lambda)/(\mathrm{d}^2-\Lambda^2)$ is arbitrarily large. This contradicts the assumption that $1/(\mathrm{d}-\Lambda)$ was defined, since these two terms are both equal in standard arithmetic (similarly, tolerances cannot be subtracted). Thus, the calculus of control element analysis has already diverged from the usual system of arithmetic and this has some benefits. One benefit is that a.c. signals are dealt with naturally; another is flexibility as will be shown.

Let $ab=iI[1+\mathrm{j}(\mathrm{d}+\Lambda)]$, where d+$\Lambda$ is square-neglectable in comparison with 1. Consider quantities $U_\mathrm{d}=1+\mathrm{j}\mathrm{d}$; $U_\mathrm{d}U_\Lambda=U_{\mathrm{d}+\Lambda}$ since dΛ is neglectable; $U_\mathrm{d}+U_\Lambda=1+U_{\Lambda+\mathrm{d}}$; $U_\mathrm{d}+U_\Lambda=1+U_\mathrm{d}U_\Lambda$.

By the ordinary process of arithmetic, writing x for U_d and z for U_Λ, we have $x+z=1+xz$ or $x(1-z)=1-z$, so that $x=1$ when $z\neq1$ and, similarly, $z=1$ when $x\neq1$.

Therefore, either x or $z=1$ is against hypothesis. This means that ordinary processes of arithmetic cannot be used: division reciprocal and hence multiplicative cancellation do not exist. Thus, we can add three of the quantities, but the rule $(a+b+c)+d=a+(b+c+d)$ four-associativity (adopted) does not work for addition (or for multiplication). But apart from this, how simple: $1+U_\mathrm{d}U_\Lambda=U_\mathrm{d}+U_\Lambda$.

In spite of these restrictions, we can define a conjugate

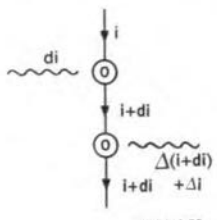


$\bar{U}_\mathrm{d}=1-\mathrm{j}\mathrm{d}$ and $\bar{U}_\mathrm{d}=U_{-\mathrm{d}}$,
so that $U_\mathrm{d}U_{-\mathrm{d}}\approx U_0\equiv1\approx U_\mathrm{d}U_{-\mathrm{d}}$;
$U_\mathrm{d}\bar{U}_\Lambda=U_{\mathrm{d}-\Lambda}=\bar{U}_\Delta U_\mathrm{d}$;
$1+U_\mathrm{d}\bar{U}_\Lambda=U_\mathrm{d}+\bar{U}_\Lambda=U_\mathrm{d}-U_\Lambda+2$;
$U_\mathrm{d}\bar{U}_\Lambda=U_\mathrm{d}-U_\Lambda+1$.

Using these results, d$i=\Lambda I$; $(i-\mathrm{j}\mathrm{d}i)=i\bar{U}_\mathrm{d}$, and $I+\mathrm{j}\Lambda I=IU_\Lambda$.

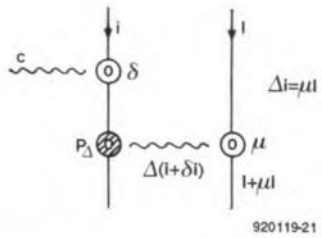
$i\bar{U}_\mathrm{d}+IU_\Lambda=i+I$; $\bar{U}_\mathrm{d}U_\Lambda=U_{\Lambda-\mathrm{d}}$; and
$iIU_{\Lambda-\mathrm{d}}=iI+\mathrm{j}\mathrm{d}i(i-I)$.
But also, $U_\Lambda U_{-\mathrm{d}}=U_\Lambda+U_{-\mathrm{d}}-1$, so that
$-iI+iIU_\Lambda+iIU_{-\mathrm{d}}=iI+\mathrm{j}\mathrm{d}i(i-I)$.

Elements in series: $i+\mathrm{d}i+i\Lambda$:



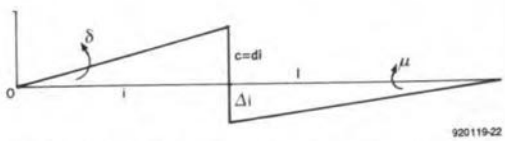
Thus, U_d and U_Λ in series act like $U_{\mathrm{d}+\Lambda}$ and are equivalent regardless of order.

From this connection



we have a cascade of two stages with $\mu I=c\Lambda/\mathrm{d}$, where μ and d are associated with a active elements and Λ with a passive one; c is the input and I may be viewed as the output.

In practice, Λ and d may not be square-neglectable. To show how the calculus may be used, we draw an Argand diagram



in which δ and μ are small enough for $\delta=\sin\delta$ and $\mu=\sin\mu$. From geometry: $\mu I=\Lambda c/\mathrm{d}$. We can consider d$i$ and ΛI to lie at right angles because δ and μ are square-neglectable.

Note that the above zigzag route from 0 to A, $0B$, C, A results in moving on average in a real direction equivalent to $i+I$, the sum of the input currents.

Current control was chosen because flow in any situation is **basic**, whereas potentials are **derived**. Even if the device is a voltage-controlled current switch, then the voltage control can be changed to current control by a single component.

Thus we have outlined the system and shown how it can be used.

Advantages

The advantage of the system is that all types of control element can be modelled. The method is to make $I=f(\mathrm{d})$, where f is the appropriate function. For a switching function, we might use

$f=(1000\mathrm{d})^{100}/(1+[1000\mathrm{d}]^{100})$,

but for a linear function we can use something else. Thus, by choosing some appropriate f, we can model any behaviour we wish by se-

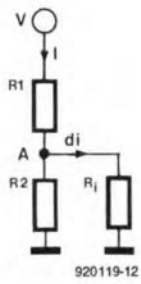
lecting standard functions for that purpose.

For a single transistor or darlington pair with gain α', let k be the maximum current excursion for linear operation; then

$I=f(\upsilon)=\alpha' k[\upsilon(1+\upsilon^{99})/(1+\upsilon^{100})]$

(where $\upsilon=i\alpha'$) is a suitable function which has almost exactly linear amplification over a range with saturation. In practice, of course, to design a circuit account must be taken of knee voltage, that current cannot be supplied from a point sitting at a lower voltage, and so forth. But methods like this supply the functional design, not the details; and because they are simple, they supply a quicl outline that can be adapted to the kind of circuit or system required.

When low-gain germanium transistors were in use, a method like this could be employed, because the reciprocal gain, $1/\alpha'$, could not be considered square-neglectable. With a darlington pair, and also with high-gain silicon transistors, the method definitely can be used. Hence, let us now consider the use of resistor networks that are also necessary in a practical design. Consider the network



and suppose that d is square-neglectable and that R_l is high compared with R_1 and R_2. Then we may assume that the current is closely the same in R_1 and R_2. Hence, point A sits at $VR_2/(R_1+R_2)=IR_2$. Also, by Ohm's law, $dIR_l=R_2I$, so that $d=R_2/R_l$. The accurate formula is $d=R_2/(R_l+R_2)$.

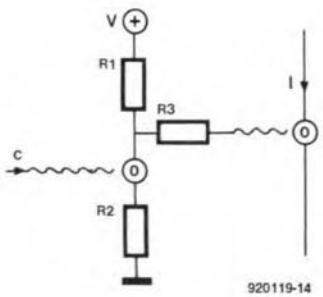
Note that

$R_2/R_l-R_2/(R_l+R_2)=(R_2/R_l)^2/(1+R_2/R_l)=$

$=(R_2^2/R_l)/(R_l+R_2)=$

$=d^2$ (closely),

so that our approximation is justified. Thus, our formula $I=R_2c/(\mu\Lambda R_l)$, where c is the input current and μ and Λ are parameters of two amplifying devices. Thus, the stage gain is $R_2/(R_l\mu\Lambda)$. By cascading stages, alternating active and passive stages, we can build an analysis of



which circuit is a basic building block.

We must now introduce the complex inner product of two complex numbers:

$(a+jb)\cdot(c+jd)=ac+bd$.

If $a+jb=z_1$ and $c+jd=z_2$, this can also be defined as

$(A+B)/2+j(A-B)/2=z_1\cdot z_2$, so that

$A=R\ell(z_1z_2)$ and $B=R\ell(z_1z_2)$.

Note that $u\cdot v=v\cdot u$, where u, v are complex numbers, and $u\cdot v\cdot w$ is defined.

Let δ be not square-neglectable in comparison with unity; then, $U_\delta\cdot U_\Lambda=U_{\delta\Lambda}$. When δ and Λ are square-neglectable, $U_\delta\cdot U_\Lambda\approx 1$ defines $U_{1/\delta}$ by $1-1/(U_\delta-1)=(U_\delta-2)/(U_\delta-1)$. Then,

$U_\Lambda\cdot U_{1/\delta}=U_{\Lambda/\delta}$, and

$U_{\delta/\Lambda}=(U_{\Lambda/\delta}-2)/(U_{\Lambda/\delta}-1)$, so that,

$U_{\delta/\Lambda}U_{\Lambda/\delta}-U_{\delta/\Lambda}=U_{\Lambda/\delta}-2$, or,

$U_{\delta/\Lambda}U_{\Lambda/\delta}=U_{\delta/\Lambda}+U_{\Lambda/\delta}-2$.

Note here that δ/Λ and Λ/δ are not square-neglectable, so that no conflict subsists between this and $U_\delta U_\Lambda=U_\delta+U_\Lambda-1$ found previously.

There is now motivation for defining square-square-neglectable (sqsq-neglectable) quantities. These are quantities whose fourth power is neglectable with respect to unity. Thus, when d and Λ are sqsq-neglectable,

$U_\delta U_\Lambda=U_{\delta+\Lambda}-\delta\Lambda$;

$U_\delta\cdot U_\Lambda=U_{\delta\Lambda}$;

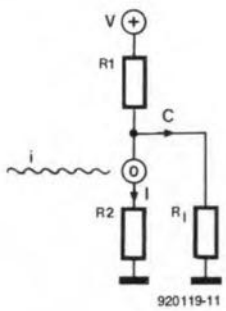
$U_\delta+U_\Lambda=1+U_{\delta+\Lambda}$.

However, $\delta\Lambda$ is square-neglectable and so, naturally, is δ^2, so that $U_{\delta\Lambda}U_{\delta\Lambda}=U_{2\delta\Lambda}$.

We may treat sum resistor networks as sqsq-neglectable; using this distinction, design becomes easier, since $U_{\delta\cdot\Lambda}=U_{\delta\Lambda}$ when one of the quantities δ, Λ is sqsq-neglectable.

To give values: 1/500 (and also any larger quantity) may be considered square-neglectable with respect to one; 0.045 or less may be considered sqsq-neglectable. Ratios greater than this can be treated as usual quantities, that is, $U_y=1+jy$ can be treated as any standard complex number of this form.

Practical circuits for powering control units or actuators also require to work out of phase sometimes, and this can be arranged, too, since δ, Λ can be made negative, but if this is not possible:



Since an increase of i increases I, which increases voltage drop across R_l, so that the current flowing in R_l is less. Thus, out-of-phase switching is possible.

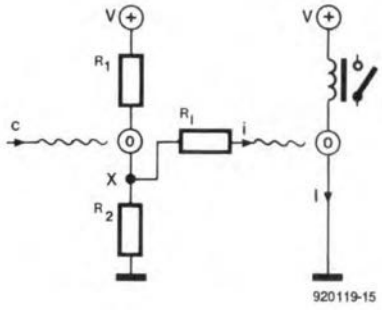
The chief advantage of this method is that the method can be: (a) graphical; (b) algebraic; (c) logical as required.

Outline now, specific later

Control element analysis, as this method is called, is blessedly free from particular details. Thus, the method can be used to 'block out' the operational structure required before the fine details need to have precise determination. The U_y can be used to model sum points for current flow so that feedback can be considered when this is necessary. However, the gain-lowering property of negative feedback can be a problem sin ce the equivalent parameter d' of a control element in a feedback system can be moved away from the square-neglectable class; thus, the calculus of the introduction cannot be used in the equivalent form.

To deal with a negative sum, the sign of y can be changed, of course. Thus, three basic types of node are used: active, passive and sum.

Example. A darlington (high power) has $h_{fe}=500$ and is used to switch a relay (4 Ω) which requires 2 A to pull in. Design a coetrol element so that 0.5 mA input current when **not** present will result in the relay pulling in.(in other words, the relay will detect the absence of the 0.5 mA current).



Let $R_2/R_l=\Lambda$, not square-neglectable. We have to relate here a horizontal input current c to a vertical output current. In control element analysis, the distinction between a vertical and a horizontal current is 'j'; that is, $|I+j\mu I|\approx I$, and $I(U_\mu-1)=j\mu I$. Thus, in the above diagram, using the fact the current in R_l is known in two different ways, we have $(c/j)(U_d-1)>IR\ell(1-U_\mu U_{1/\Lambda})$ (considering point 'x'). For the action of the relay, the $R\ell$ function is included to clean up the neglectable approximations involved in the method.

Alternatively, $(U_\mu+U_{1/\Lambda}-U_\mu U_{1/\Lambda}-1)$ may be used; the problem is that Λ is not square-neglectable. Thus, $cd>I\mu/\Lambda$. Note that $\Lambda=R_2/R_l$. Set $10R_1=R_2$; then,

$2<(0.0005)/R_l(0.002\cdot 0.002)=500R_2/4R_l$.

Say, $R_2=100\ \Omega$, then $R_l<62.5R_2$

Make $R_l=5000\ \Omega$.

This design uses a slightly more expensive darlington, but the gain is simplicity of design, and we can use the U calculus.

Complex analysis to represent circuits

One more advantage of this system is that we can combine some resistor networks continuously with cascade control elements and thus each control element can be represented or specified by a complex number in the plane, with the convention that two complex numbers at positions of the plane with the same j component (height). If there is no spec-

ified point in between, then from each complex number a vertical line extends both up and down till a real number or complex number not representing a control element is reached, which is considered a series impedance in the vertical line. Two control elements represented by 1+μj and 1+dj, where μ and d are square-neglectable quantities compared with one, and which are on the same horizontal line vertically or horizontally with no other point in between, are just linked. Therefore, a complex function where all but a finite number of points are non-zero is capable of representing any control element circuit.

We also need junctions with no device where horizontal and vertical lines meet; these can be denoted by complex roots of unity; the order of the root describes the number of lines joining in the star. Thus, W_3 is a T-junction; W_4 is a place where four lines meet, and so forth. Should some complex impedance be equal to a complex root of unity, slightly alter this component value (in fact, none are exactly, thus no generality is lost). The previous circuit can be represented by

10		A
1+0.012j		
W_3	5000	1–2E–3j
100		
0		0

For purposes of storage (suitable for computers, for instance) and description, the circuit can also be represented by a matrix with, say, 0' used for empty spaces:

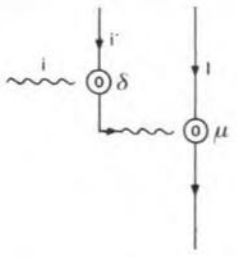
10	0'	A
1+0.012j	0'	0'
W_3	5000	1–2E–3j
100	0'	0'
0	0'	0

Pushing control element analysis

We now have a control element calculus and a way of representing a control element circuit as a matrix (which is for summarizing, not for calculation). Of course, a matrix **can** be used to calculate with control elements if required (2,3).

Logic circuits, regardless of their implementation (which logic series?), are used for logic design, and here we have a scheme that can be used to describe control element analysis also. The circuits are used for switching or for any other use. However, the system is not specific about what kind of control element is being used: just that a small flow determines a large flow and that, therefore, the intrinsic nature of a general and practical requirement is encapsulated nicely in this very simple system that uses square-neglectable quantities.

Conversion to simpler analysis



920119-16

Note the rules:

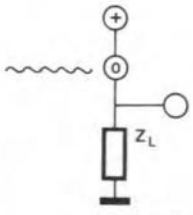
Series: $U_\Lambda U_d = UI_{d+\Lambda}$ and $U_\Lambda + U_d = 1 + U_\Lambda U_d$, where d, Λ are square-neglectable quantities.

Cascade: $\mu d I = c$, where c is the input current. Hence, $U_{d\Lambda}$ may be used to represent the cascade connections, but this applies only when dΛ is square-neglectable and can be used for the darlington connection. Remember also the rule $(c/j)(U_d - 1) > IR_1(1 - U_\mu U_{1/\Lambda})$ used for the solved problem earlier.

We have, therefore, a natural calculus for series and cascade: a non-device-specific calculus. The advantage of the system is the feature of square-neglectable properties that simplify calculations. When two elements are used in cascade (U_d, U_Λ), and d, Λ are square-neglectable, in our system $U_{d\Lambda} = 1$ so that the load current can be considered to pass through the output device unchanged. Approximate, yes; but of simple utility when transformed into this form.

Output impedances

When we consider switching circuits, the control devices we think of have very low output impedances when on; these may be ignored in practice so that the output current is set by the load impedance in this state and the control elements can be considered to route current.



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If our control element is not a switching device, the quiescent output impedance of the device must be considered, of course. If the load is current-operated (an actuator, relay, motor, lamp), this is not a problem with careful design.

There are other, special considerations for high-quality designs, such as those similar to the emitter-follower which is known to distort the output waveform under some conditions. But these are all the details of special cases.

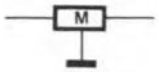
Adjusting to this approach

We have described the following concepts:

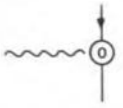
- square-neglectable;
- control element representations;
- U_d and the conjugate $U_{\bar{d}}$,
- cascaded control elements;
- a matrix to encode a circuit.

Thus, we have an economical way of describing control elements so that we can calculate how they are put in series and cascaded, the concept of the conjugate of a control element, and a numerical matrix to encode an entire circuit.

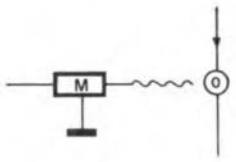
Suppose we have a current mirror



then



is represented by U_d and



920119-17

is represented by $\bar{U}_d$. Thus, by the use of a current mirror we can conjugate our control elements. ■

References:

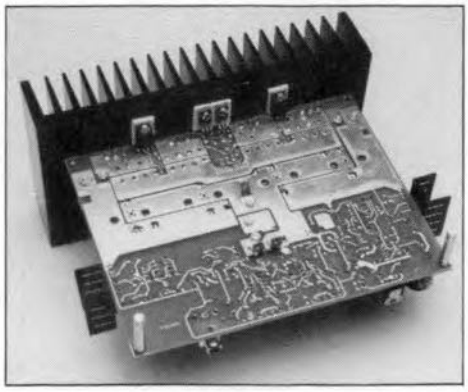
'Augmented A-matrices', by M.C. Soper, *Elektor Electronics*, May 1991.

'Matrix Algebra – 2', by G.H. Olsen, *Wireless World*, April 1965.

'A simple and adaptable logic', by M.C. Soper, *Elektor Electronics*, December 1991.

Cybernetics, by N. Weiner, Wiley, New York, 1938.

OUTPUT AMPLIFIER FOR RIBBON LOUDSPEAKERS PART 2 (FINAL)



Design by T. Giesberts

Because of the special requirements of the amplifier, its construction is somewhat different from that of more traditional output amplifiers. For instance, the large currents cause such strong stray magnetic fields that a wrongly connected supply line can cause problems. It is, therefore, essential, for instance, that the buffer capacitors are located between the drivers and the power amplifiers so that the output transistors are as close to their supply points as possible. If this were not done, there would be a strong likelihood that the power lines would be 'modulated' by the strong amplifier signals.

Specification

The power was measured with a standard transformer; if a heavier-duty type, 2×12 V, 20 A is used, the power goes up to about 140 W into 0.4 Ω. However, it is felt that the price of that transformer is too high for the small gain in output power.

The low-frequency end of the bandwidth of the amplifier is limited to 9 Hz, primarily by the input capacitor. If the amplifier is to be used in a full-range system, the value of C_1 and C_{23} should be increased to 1 µF.

The signal-to-noise ratio does not appear very good, but bear in mind that a power of 1 W into 0.4 Ω corresponds to a (relatively) very low voltage of 632 mV. The amplifier generates very little noise, but owing to that low voltage the ratio is somewhat lower than in traditional amplifiers.

The same goes for the distortion figures: the figures are good as they stand, but compared with a 4 Ω or 8 Ω load they are excellent. The distortion of an amplifier normally decreases with a rising load value, because the amplifier then delivers less current. This is very clear from a comparison of the figures for loads of 0.4 Ω and 1 Ω respectively.

Again, owing to the low output voltage, the slew rate does not seem very good. It might be better to state the rise time for full drive instead of a number of volts per microsecond, because that is independent of the supply voltage, and, therefore, of the output power.

The damping factor (ratio of the loudspeaker impedance to the amplifier source impedance) is very high; even at 20 Hz it was impossible to measure. The stated figure of 600 is a cautious estimate.

The characteristics shown in Fig. 5, 6 and 7 are measured with an Audio Precision System One analyser. The dotted lines pertain to a 0.4 Ω load and the solid lines to an 8 Ω load. The upward slope of the characteristic at higher frequencies in Fig. 5 is caused mainly by the large output currents and the consequent stray magnetic fields. With standard loads of 4 Ω or 8 Ω, the characteristic is nearly horizontal up to 20 kHz.

The increase in distortion at low power shown in Fig. 6 is something that happens in all amplifiers; it is caused by noise beginning to play a larger role (whence THD+noise). A conspicuous point is the sharp bend in the curve when the amplifier begins to clip. There is thus no soft clipping: once clipping sets in, the only remedy is to lower the volume.

The slight drop below 100 Hz in Fig. 7 is caused by the buffer capacitors. When the value of these capacitors is increased, the dip may be lowered to about 20 Hz. In the prototype this was not felt necessary since the ribbon loudspeaker used had a frequency response down to a few hundred hertz.

Construction

The amplifier is best built on the two printed-circuit boards shown in Fig. 8 and 9. On the amplifier board, first mount the standard components, then the transistors, and finally the buffer capacitors. Mount diodes D_1–D_4 as close as possible to current sources T_5–T_8. Before soldering them, tie them together with a length of wire.

The dual transistors may have different cases. The MAT types are housed in a round TO-78 case. Note that the numbering in Fig. 3 (Part 1) does not correspond to the numbering of the DIP transfer on the board. SSM types in an eight-pin DIP housing fit in only way on the board.

Mount the emitter resistors for the output transistors upright if standard 5-W types are used. The special block-shaped inductance-free types fit directly on to the board; they are, however, very difficult to obtain.

The coil shown on the board is not used; simply replace it by a wire link.

For the connections of the power supply and output use car type connectors. Moreover, use car type fuse holders. All these carry heavy currents.

Bend transistors T_{12} and T_{13} slightly sideways to enable a heat sink to be fitted to these devices.

Connector K_1 is not really required and may

TECHNICAL DATA

Input sensitivity	720 mV r.m.s.
Input impedance	45 kΩ
Supply voltage	±15 V
Quiescent current	1 A
Output power (1 kHz, 0.1% THD)	110 W into 0.4 Ω
Mains transformer 2×12 V, 12.5 A	70 W into 1 Ω
Music power (500 Hz burst, 5 periods on,	130 W into 0.4 Ω
5 periods off)	85 W into 1 Ω
Power bandwidth (50 W into 0.4 Ω)	9 Hz–250 kHz (±3 dB)
Slew rate	>14 V µs^{-1}
Signal-to-noise ratio (1 W into 0.4 Ω)	>95 dB (A weighted)
Harmonic distortion	
at 1 W into 0.4 Ω	<0.01% (1 kHz)
at 100 W into 0.4 Ω	<0.005% (1 kHz)
	<0.05% (20 Hz–20 kHz)
Intermodulation distortion	<0.004% (1 W into 0.4 Ω)
50Hz:7 kHz; 4:1)	0.006% (100 W into 0.4 Ω)
Dynamic IM distortion (block 3.15 kHz	<0.008% (1 W into 0.4 Ω)
with 15 kHz sine wave)	<0.003% (100 W into 0.4 Ω)
Damping factor (0.4 Ω)	>600

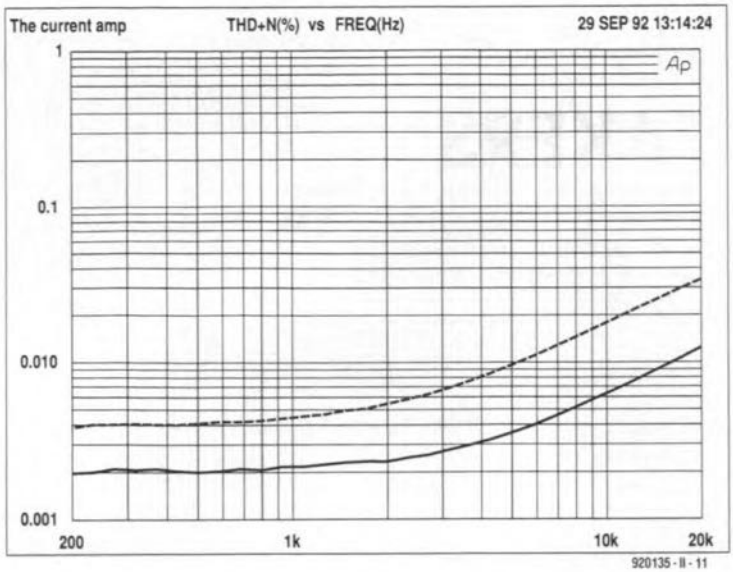


Fig. 5. Harmonic distortion over 200 Hz to 20 kHz range at an output power of 50 W. Solid line: 1 Ω load; dotted line: 0.4 Ω.

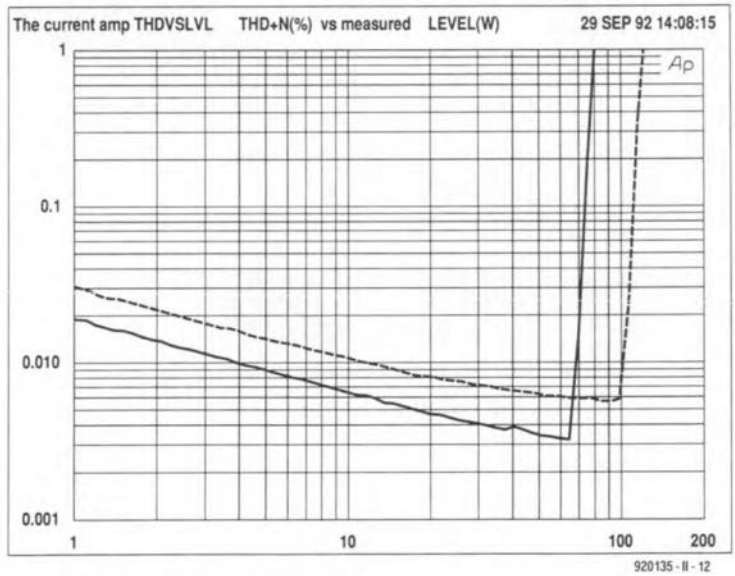


Fig. 6. Harmonic distortion vs drive at 1 kHz. Solid line: 1 Ω load; dotted line: 0.4 Ω.

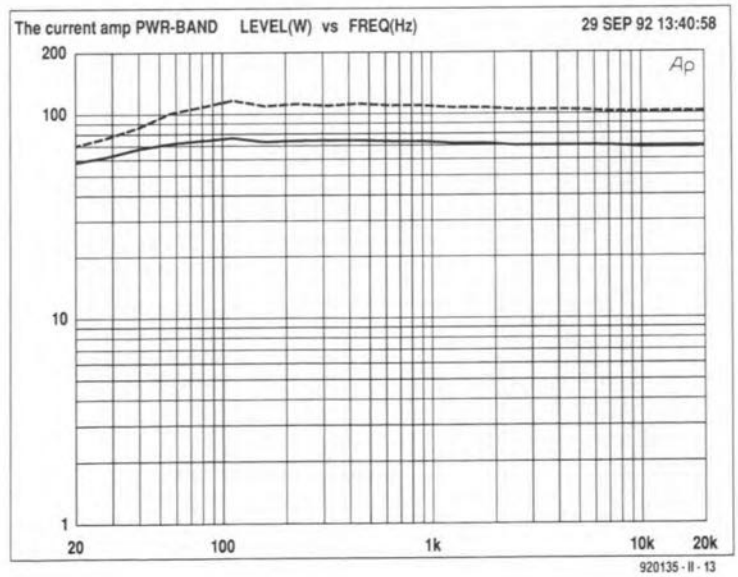


Fig. 7. Maximum power for 0.1% distortion. Solid line: 1 Ω load; dotted line: 0.4 Ω.

be replaced to advantage by two solder pins to which later a length of screened cable is soldered.

A template for the fixing holes in the heat sink for the transistors is given in Fig. 11. The output transistors go to the top of the board, and the drivers and smaller transistor to the underside. The smaller transistors should be insulated with the aid of ceramic washers and the output transistors with mica washers (since for these—the better—ceramic washers are unfortunately not available).

First, screw the power transistors to the heat sink and bend their pins slightly forward so that they fit nicely into the holes on the board. Fix the board to the heat sink with two small brackets. Only then solder the output transistors in place.

Make a loop in the terminals of the smaller transistors at the underside of the board to allow for mechanical stress during temperature variations.

Populating the protection board is straightforward. Do not yet fit T_{12}, hower—see Alignment. Use heavy-duty terminals alongside Tri_2 because these are used in the short-circuiting of the supply in an emergency.

A wiring diagram for the complete amplifier is shown in Fig. 10. Be sure to use wire of at least 4 mm² cross-section for all power lines. Standard circuit wire may be used for all other cabling.

Interconnect terminals A on the two boards with a short length of screened cable; connect the screen of this cable to earth only on the amplifier board.

Position the bridge rectifier as close to the amplifier as possible to keep the interconnections short. The final layout depends, of course, on where the amplifier will be installed. If it is fitted in the loudspeaker enclosure. the heat sink must be at the outside; the transformer can then be placed behind the heat sink. In a stand-alone installation, the heat sink may be in the centre of the amplifier housing, which should be provided with an adequate number of ventilation holes.

In its standard form, the mains entry, fuse, and so on, may be as shown. If additional buffer capacitors and a heavier-duty transformer are used, it is recommended to add a mains power-on delay unit (for instance, the one described on page 70).

The connecting cable between amplifier and loudspeaker must not be longer than 50 cm (20 in). If it is longer, problems may arise with the sense wires. Note that the cable is connected direct to the amplifier board to prevent additional contact resistance.

Alignment

Set P_1 to maximum resistance: check this with an ohmmeter. Switch on the mains. With a digital voltmeter (DVM) measure the direct voltage across one of the emitter resistors of the output transistors and adjust P_1 to obtain a reading of about 10 mV.

With a DVM, measure the direct voltage at the base of T_1 or T_3. Adjust P_2 for a reading of excactly 0 V.

Again, using a DVM, measure the drop

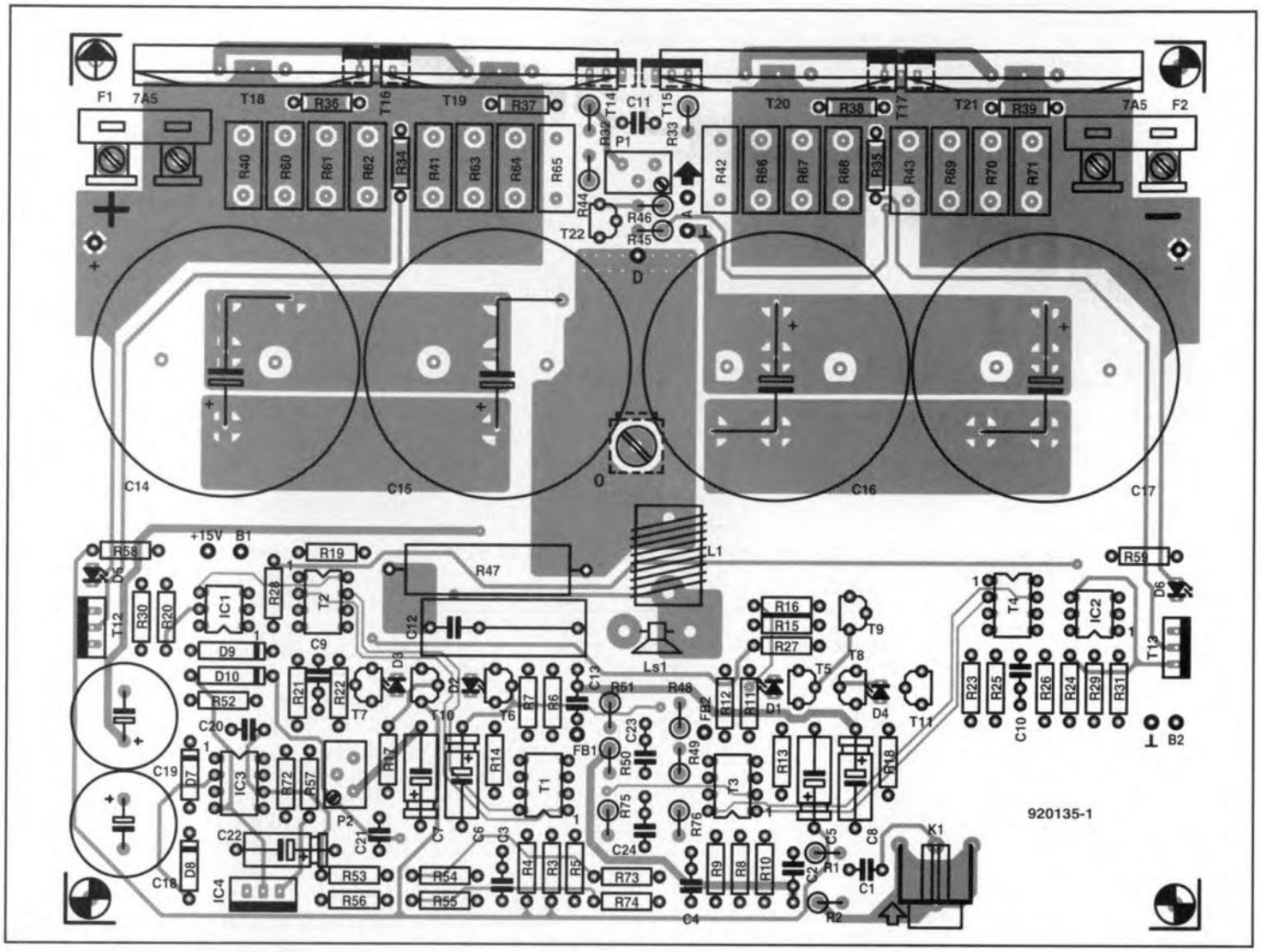


Fig. 8. The through-plated printed circuit board for the amplifier – see also pages 101 and 102.

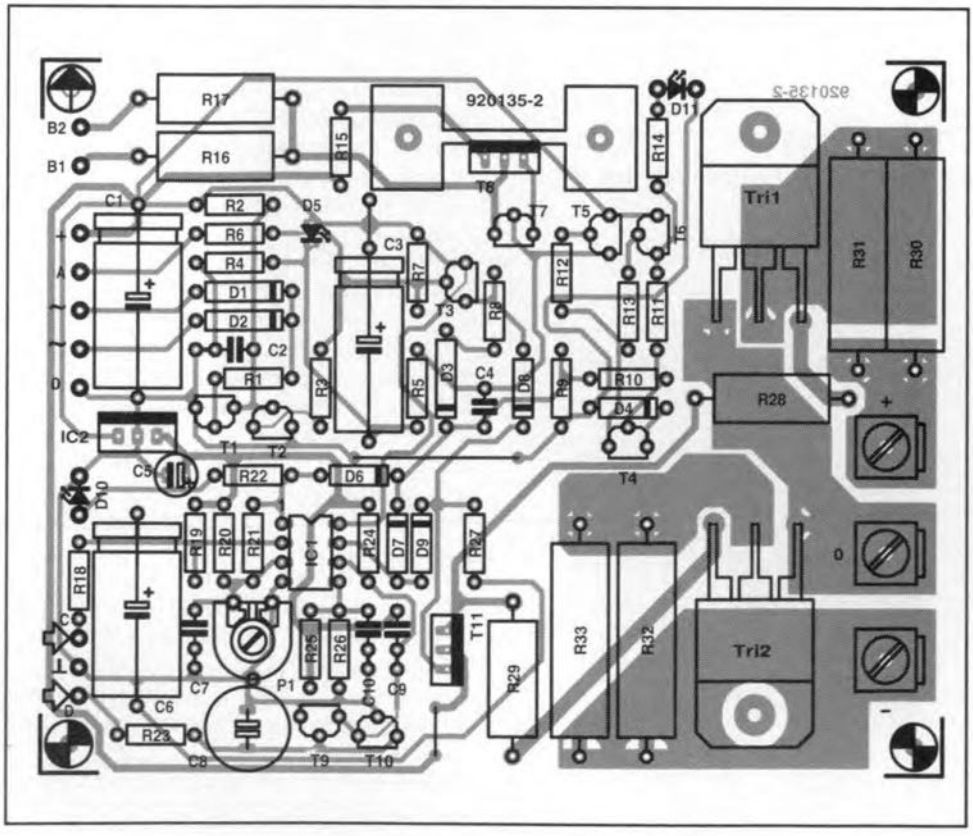


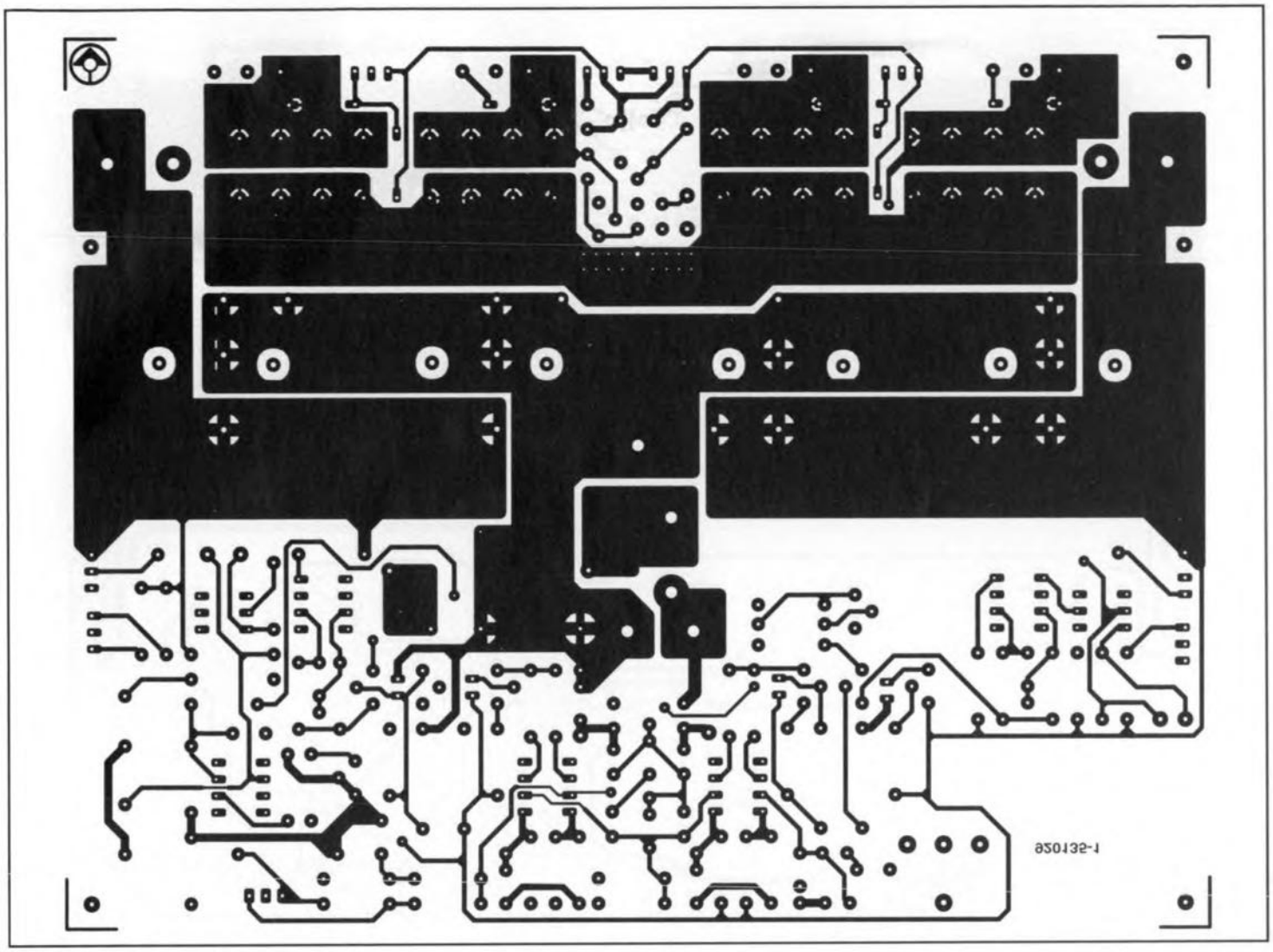
Fig. 9. Printed circuit board for the protection circuit – see also page 101.

PARTS LIST

(Amplifier circuit)

Resistors:

R1, R34, R35, R75 = 562 Ω, 1%
R2, R76 = 47.5 kΩ, 1%
R3, R4, R8, R9 = 1.21 kΩ, 1%
R5, R10 = 8.2 Ω
R6, R7, R11, R12 = 12.1 Ω, 1%
R13, R14 = 124 Ω, 1%
R15 = 820 Ω
R16 = 1.8 kΩ
R17, R18 =180 Ω
R19, R20, R23, R24 =121 Ω, 1%
R21, R22, R25, R26 = 5.62 Ω, 1%
R27 = 100 Ω, 1%
R28, R29, R45 = 390 Ω
R30, R31 = 4.99 Ω, 1%
R32 = 470 Ω
R33 = 330 Ω
R36–R39 = 56.2 Ω. 1%
R40–R43, R60–R71 = 0.22 Ω, 5 W
R44 = 1 kΩ
R46 = 10 kΩ
R47 = 0.39 Ω, 5 W
R48, R51 = 100 Ω
R49 = 402 Ω, 1%
R50 = 46.4 Ω
R52, R53, R72 = 56 kΩ

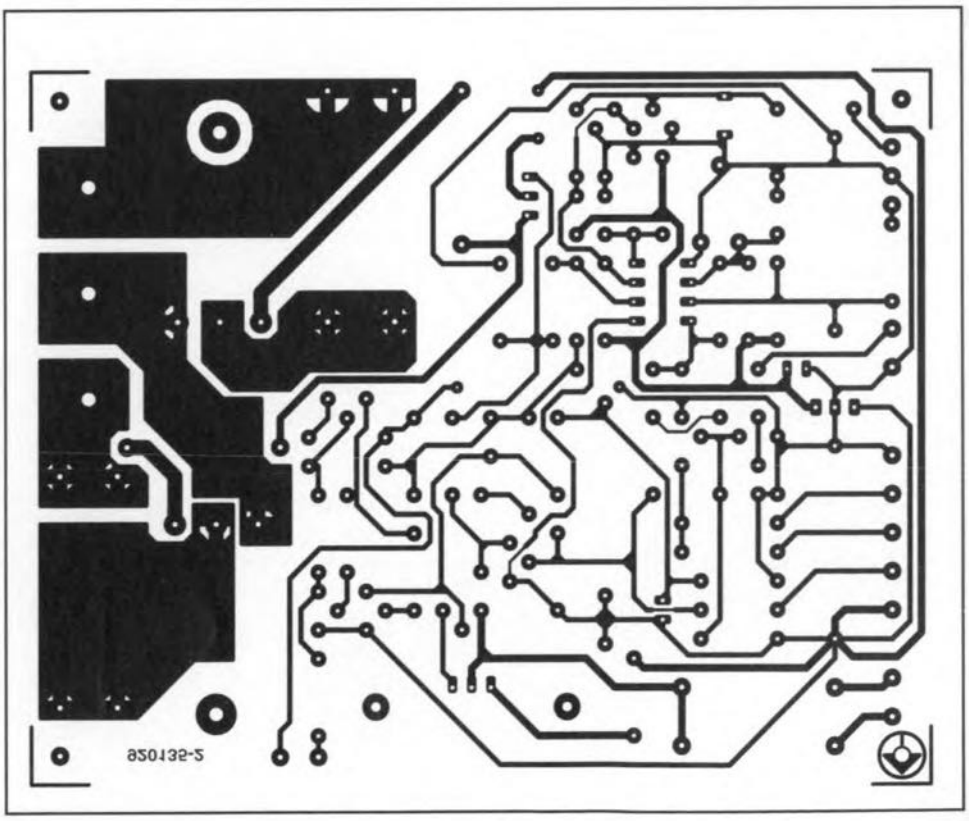


Printed circuit board for the amplifier.

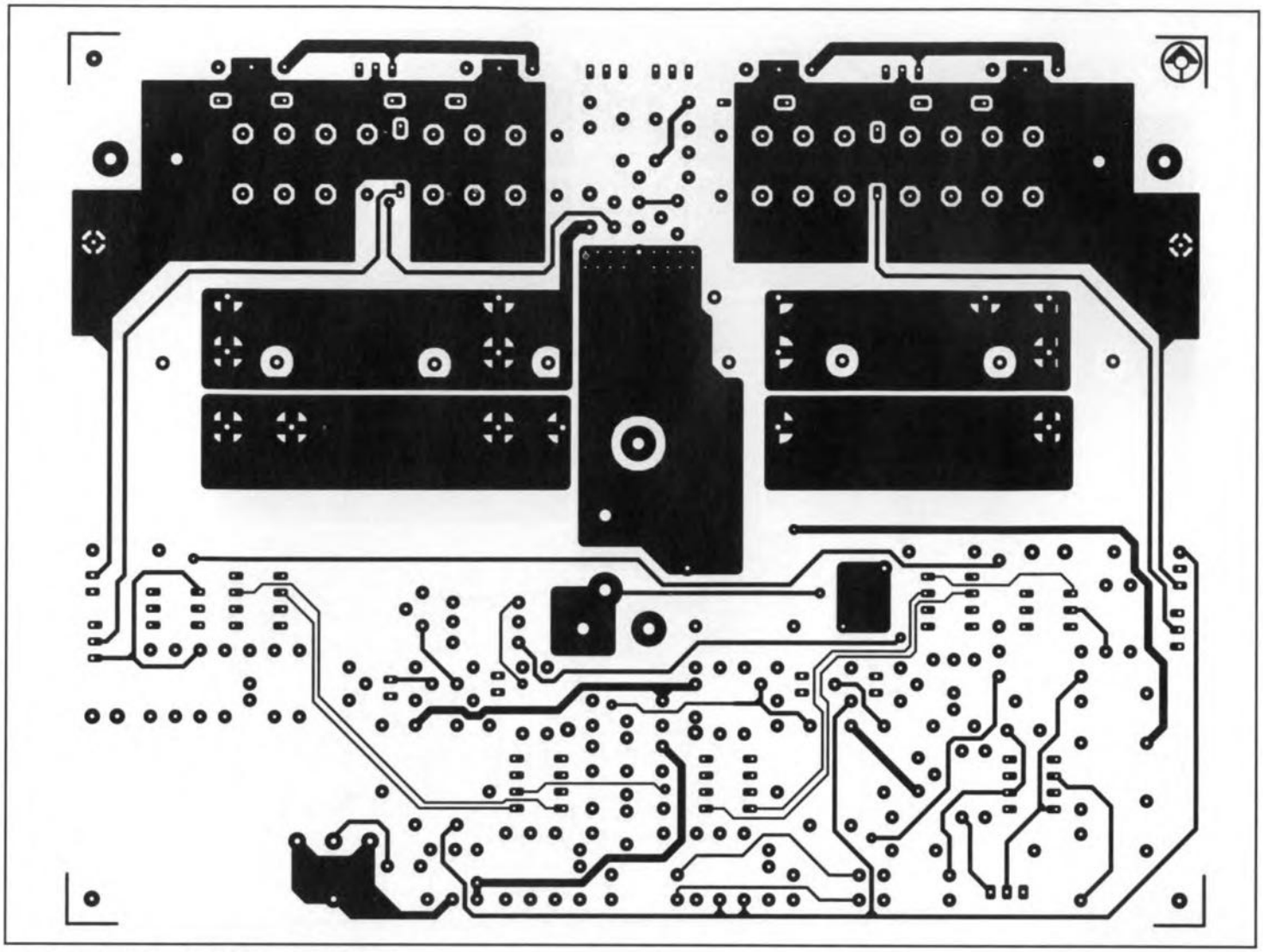
R54, R73 = 15 MΩ
R55, R74 = 825 kΩ, 1%
R56, R57 = 270 Ω
R58, R59 = 2.7 kΩ
P1 = 500 Ω multiturn preset for vertical mounting (e.g., Bourns 3269Y)
P2 = 2 kΩ multiturn preset for vertical mounting (e.g., Bourns 3296Y)

Capacitors:
C1, C23 = 390 nF
C2 = 1 nF, polystyrene
C3, C4 = 39 nF
C5–C8 = 47 µF, 10 V
C9 = 2.2 nF
C10 = 1 nF
C11, C20, C21 = 1 µF
C12 = 2.2 µF, 100 V, MKT
C13 = 5.6 nF
C14–C17 = 10 000 µF, 40 V, radial
C18, C19 = 1000 µF, 25 V, radial
C22 = 10 µF, 25 V
C24 = 4.7 nF

Inductors:
L1 = not required for ribbon loudspeakers, see text in Part 1



Printed circuit board for the protection circuit.



Printed circuit board for the amplifier.

Miscellaneous:
F1, F2 = car-type fuse, 7.5 A
K1 = audio socket for PCB (but see text)
Heat sink (×2) for T12 and T13
Heat sink, 0.5 K W^{-1} or less
PCB Type 920135-1
Bridge rectifier, 35 A, 40 V
Mains transformer, 2×12 V, 12.5 A
Mains entry with integral switch and fuse
Fuse 2.5 A
7 car-type connector blades and receptacles

Semiconductors:
D1–D5 = LED, red
D6 = LED, green
D7, D8 = 1N4148
D9, D10 = 1N4001
T1, T2 = MAT02
T3, T4 = MAT03
T5, T8 = BC560C
T6, T7, T22 = BC550C
T9 = BF256C
T10, T11 = BF256A
T12 = BD140
T13, T14, T15 = BD139T16 = MJE15030
T17 = MJE15031
T18, T19 = 2SC2922
T20, T21 = 2SA1216
IC1, IC2 = 4N35
IC3 = OP77
IC4 = LM337

(Protection circuit)

Resistors:
R1 = 33 kΩ
R2 = 1 MΩ
R3, R7, R9, R25, R26 = 100 kΩ
R4 = 15 kΩ
R5 = 100 Ω
R6, R22, R23 = 1 kΩ
R8 = 47 Ω
R10 = 1.5 MΩ
R11 = 3.9 MΩ
R12, R13 = 56 kΩ
R14, R27 = 4.7 kΩ
R15 = 10 Ω
R16, R17 = 390 Ω, 1 W
R18 = 15 Ω
R19 = 3.3 kΩ
R20 = 180 kΩ
R21 = 22 MΩ
R24 = 220 kΩ
R28, R29 = 220 Ω, 1 W
R30–R33 = 0.47 Ω, 5 W
P1 = 47 kΩ preset

Capacitors:
C1 = 220 µF, 25 V
C2, C7 = 100 nF
C3 = 470 µF, 6.3 V
C4 = 1 µF
C5 = 10 µF, 10 V, radial
C6 = 220 µF. 16 V
C8 =10 µF, 40 V, bipolar radial
C9 = 15 nF
C10 = 220 nF

Semiconductors:
D1–D3 = 1N4001
D4 = zener diode 5.6 V, 400 mW
D5 = LED, green
D6–D9 = 1N4148
D10 = LED, orange
D11 = LED, red, high efficiency
T1, T2, T4, T10 = BC547B
T3 = BC516
T5, T6, T7 = BC557B
T8 = BD14T9 = BC547A
T11 = BD679
T12 = BD139
Tri1, Tri2 = TIC263M
IC1 = CA3240
IC2 = 7805

Miscellaneous:
3 blades and receptacles (car type)
Heat sink for T8 (e.g., SK104)
PCB Type 920135-2

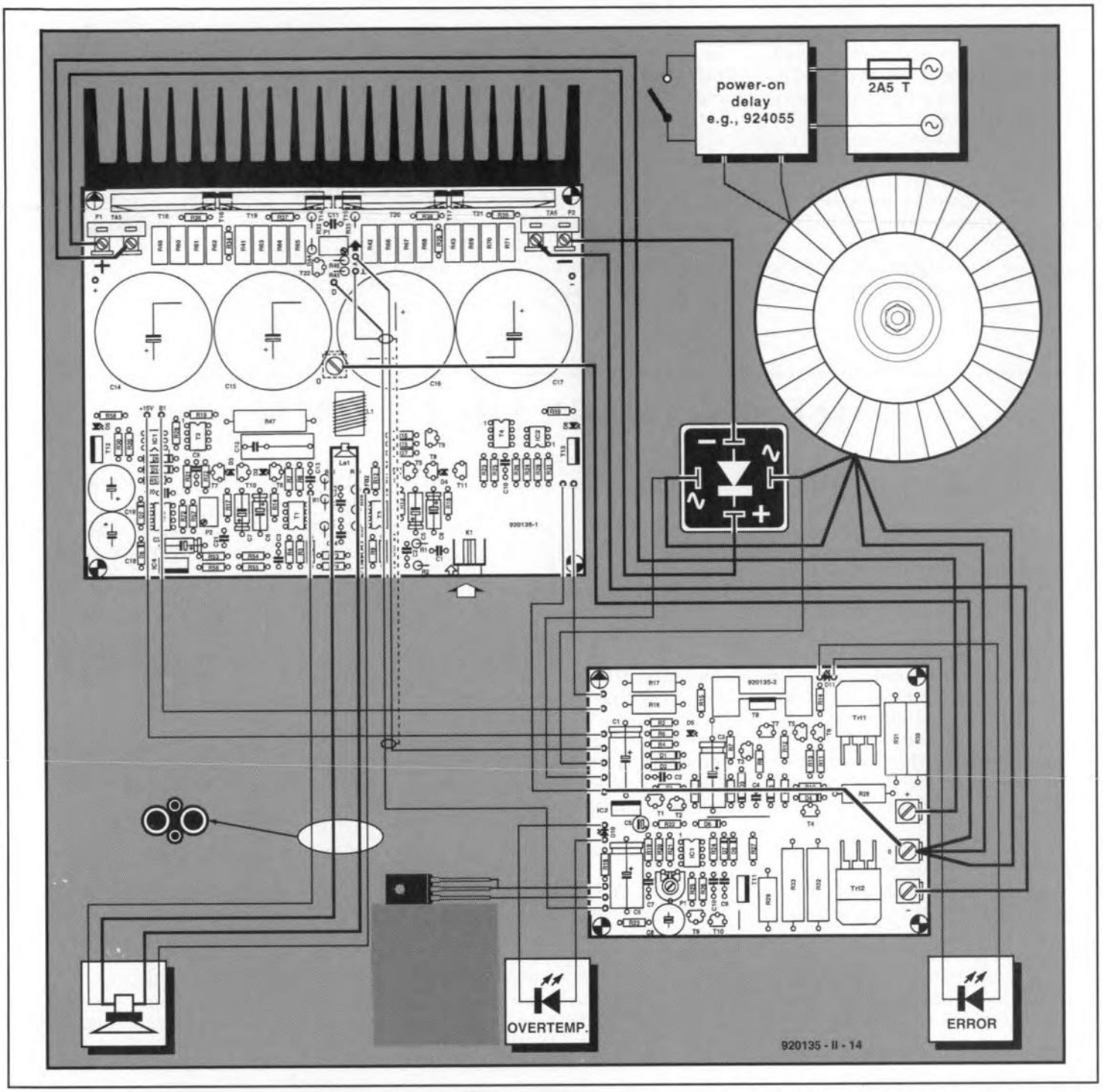


Fig. 10. Wiring diagram for the complete output amplifier.

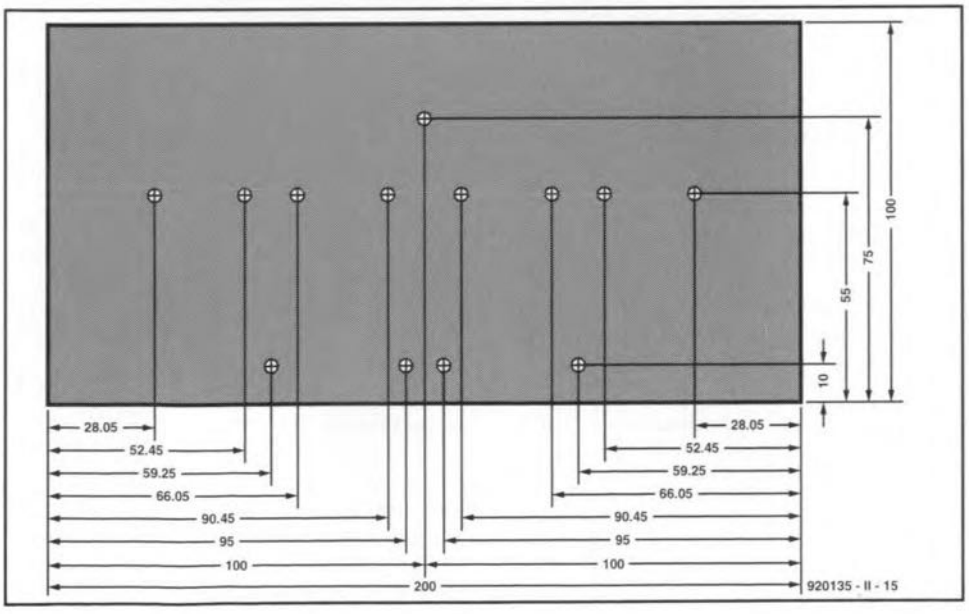


Fig. 11. Template for drilling the heat sink.

across one of the emitter resistors of the output transistors and adjust P_1 to obtain a reading of 27.5 V. This corresponds to a quiescent current of 500 mA through each of the output transistors.

Again measure the direct voltage at the base of T_1 or T_3 and readjust P_2 if required.

Measure the output voltage of IC_4, which should be between 0 V and –11 V. If the level is greater than –11 V, switch off the mains and replace resistors R_{55} and R_{74} by lower-value ones, perhaps up to 100 kΩ lower.

Measure the output voltage of IC_3 (pin 1), which may vary between –10 V and +10 V. If the voltage is higher, increase the value of

R_{73} to the next standard value. Note that this voltage immediately after power-on rises gradually from 0 V to a certain operating level, which may vary a few volts owing to temperature and supply voltage changes.

Connect T_{12} via a short length of cable to terminal C and earth on the protection board and lay it in a dish of warm water, say, 60 °C, making sure, of course, that the device's terminals are not short-circuited by the water. Adjust P_1 until D_{10} on the protection board just lights. Then, fit T_{12} on to the relevant heat sink. Bear in mind that the temperature of the heat sink even in normal operation becomes at least 20 °C higher than ambient.

The interconnection between loudspeaker and amplifier consists of a heavy-duty cable (cross-section not less than 4 mm²) and the two sense wires (thin, flexible wire). Strap the cable and wires firmly together. Connect the sense wires direct to FB1 and FB2 on the amplifier board and to the loudspeaker terminals. Keep all wiring as short as possible.

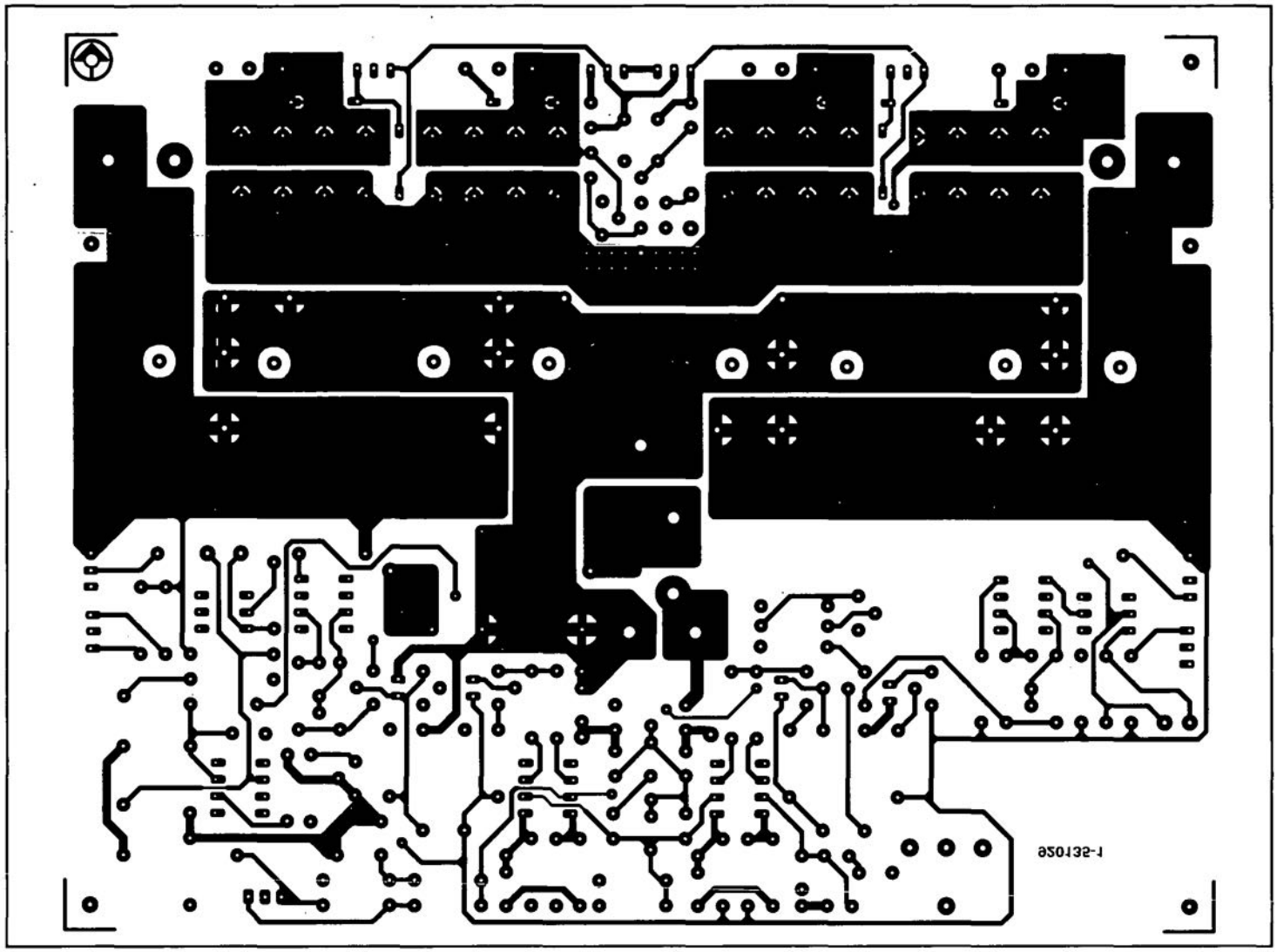
In view of the low impedance, the cross-over filter between amplifier and loudspeaker must be an active type, several of which have been published in this magazine during the past few years. If a first-order, high-pass passive filter is deemed sufficient, adapt the value of C_1 according to:

$$C_1 = 1/2\pi f_c M,$$

where f_c is the cut-off frequency in Hz and $M = 45 \times 10^3$.

The output impedance of the active filter, or preamplifier if used, must be ≤50 Ω; if it is higher, the common-mode behaviour of the amplifier deteriorates. This may be remedied, however, by increasing the value of R_{75} to the output impedance of the filter or preamplifier.

It may interest a number of readers that in a forthcoming issue we will publish a modified version of this amplifier that is suitable for use with standard loudspeaker impedances of 4–8 Ω. ■

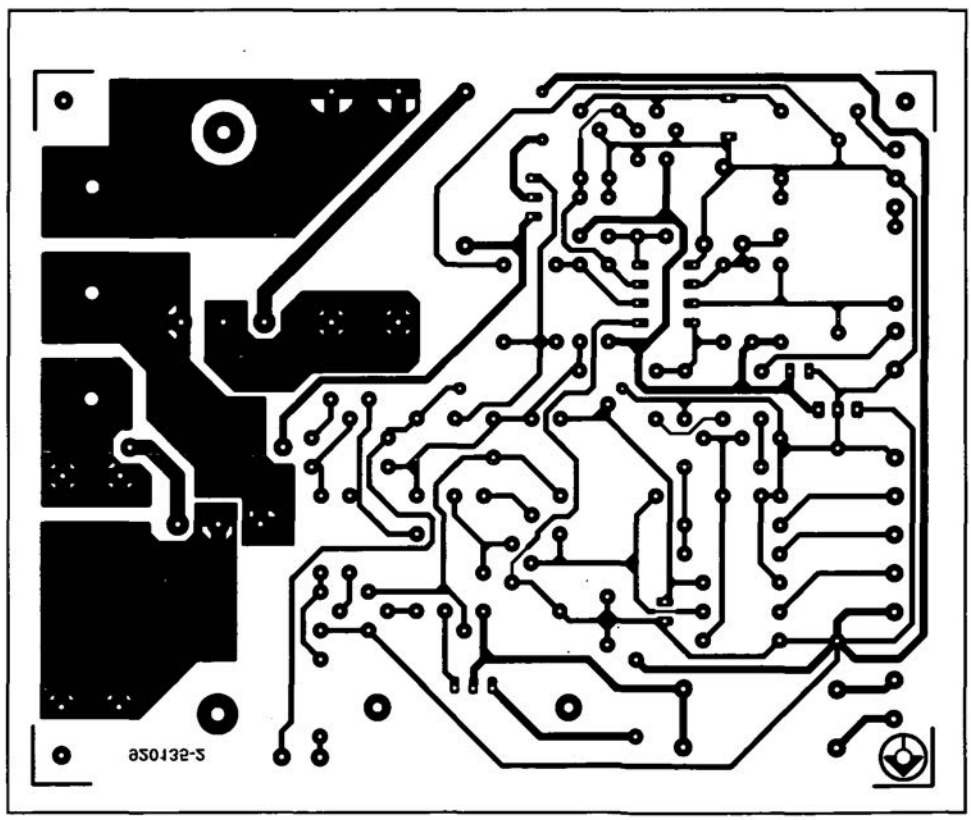


Printed circuit board for the amplifier.

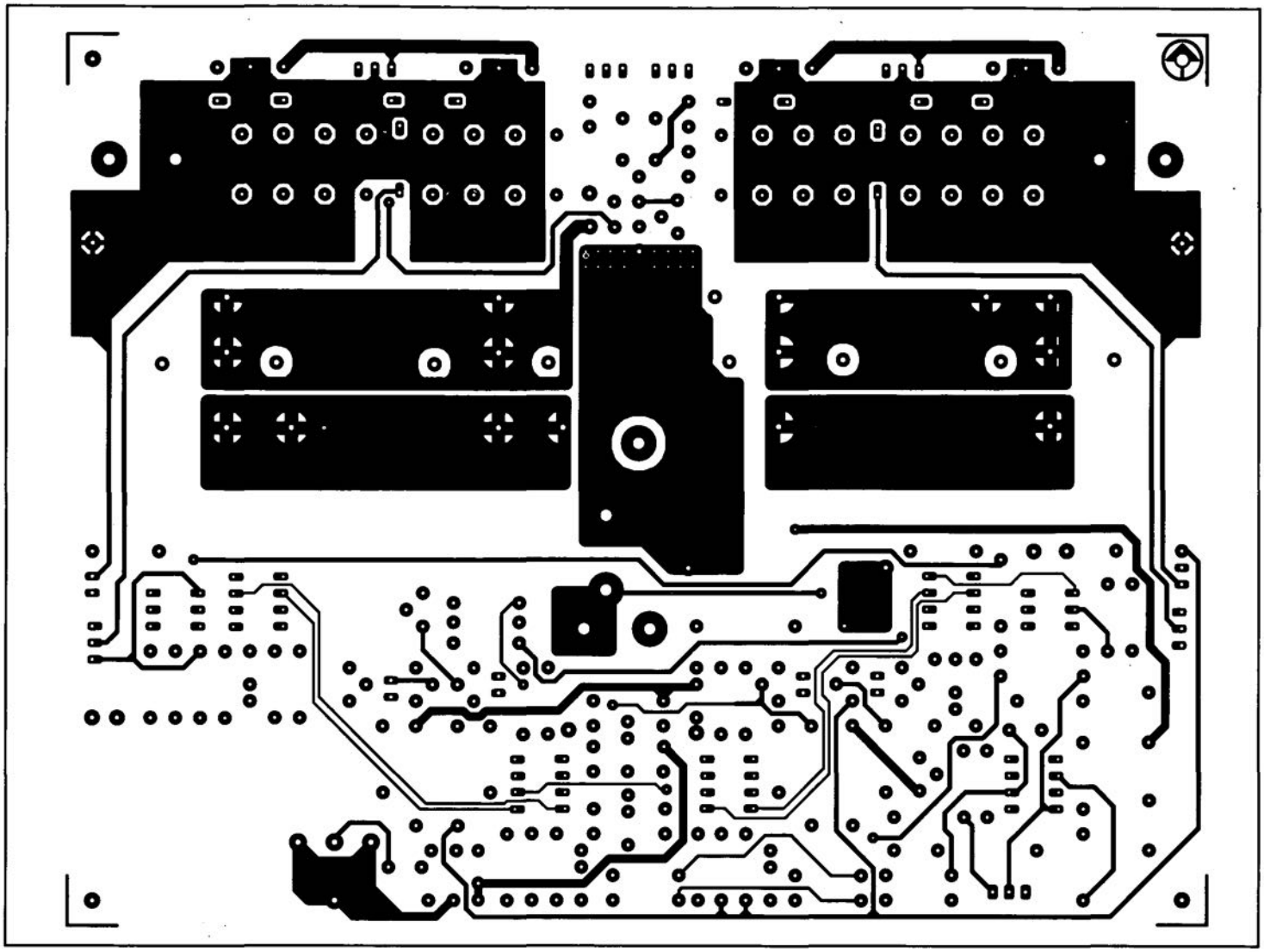
R54, R73 = 15 MΩ
R55, R74 = 825 kΩ, 1%
R56, R57 = 270 Ω
R58, R59 = 2.7 kΩ
P1 = 500 Ω multiturn preset for vertical mounting (e.g., Bourns 3269Y)
P2 = 2 kΩ multiturn preset for vertical mounting (e.g., Bourns 3296Y)

Capacitors:
C1, C23 = 390 nF
C2 = 1 nF, polystyrene
C3, C4 = 39 nF
C5–C8 = 47 µF, 10 V
C9 = 2.2 nF
C10 = 1 nF
C11, C20, C21 = 1 µF
C12 = 2.2 µF, 100 V, MKT
C13 = 5.6 nF
C14–C17 = 10 000 µF, 40 V, radial
C18, C19 = 1000 µF, 25 V, radial
C22 = 10 µF, 25 V
C24 = 4.7 nF

Inductors:
L1 = not required for ribbon loudspeakers, see text in Part 1



Printed circuit board for the protection circuit.



Printed circuit board for the amplifier.

Miscellaneous:
F1, F2 = car-type fuse, 7.5 A
K1 = audio socket for PCB (but see text)
Heat sink (×2) for T12 and T13
Heat sink, 0.5 K W^{-1} or less
PCB Type 920135-1
Bridge rectifier, 35 A, 40 V
Mains transformer, 2×12 V, 12.5 A
Mains entry with integral switch and fuse
Fuse 2.5 A
7 car-type connector blades and receptacles

Semiconductors:
D1–D5 = LED, red
D6 = LED, green
D7, D8 = 1N4148
D9, D10 = 1N4001
T1, T2 = MAT02
T3, T4 = MAT03
T5, T8 = BC560C
T6, T7, T22 = BC550C
T9 = BF256C
T10, T11 = BF256A
T12 = BD140
T13, T14, T15 = BD139T16 = MJE15030
T17 = MJE15031
T18, T19 = 2SC2922
T20, T21 = 2SA1216
IC1, IC2 = 4N35
IC3 = OP77
IC4 = LM337

(Protection circuit)

Resistors:
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