ELEKTOR ELECTRONICS

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8051 SINGLE-BOARD COMPUTER

History of the valve

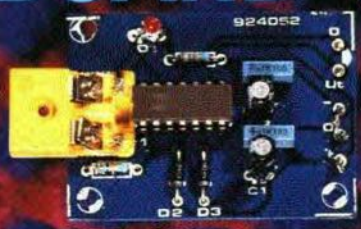
Mains sequencer

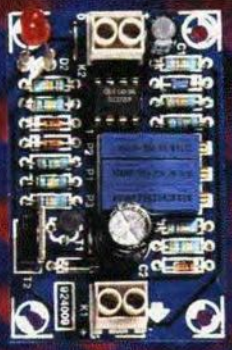
Flash EPROMs

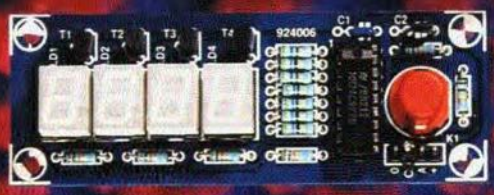
Active antenna for 10 kHz to 220 MHz

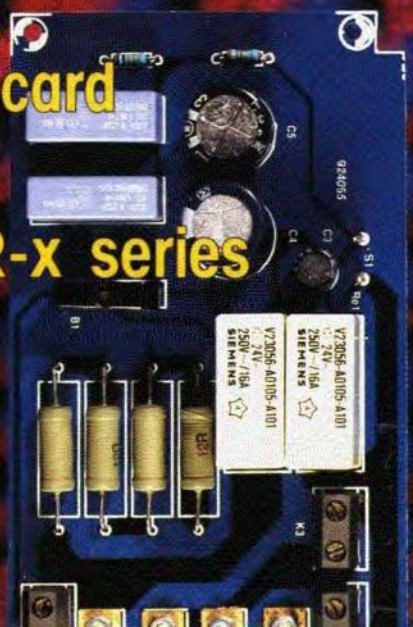
Pascal routines for measuring card

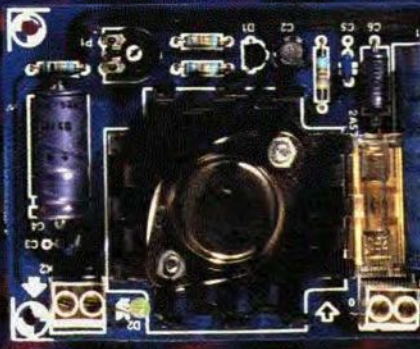
Using the MAR-x series











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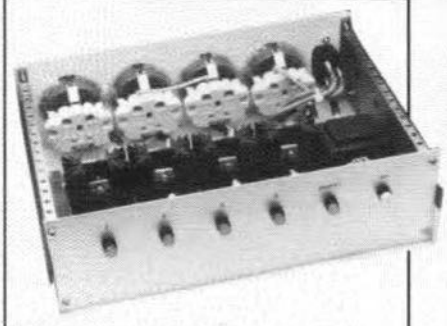
- Compact spiral antenna
- Unblocking the pump
- Sound sampler for Amiga
- Wheatstone bridge
- Model analysis

Front cover
The collage symbolizes the variety of projects we publish throughout the year and the technology used in them. In the past 12 issues, we have published no fewer than 74 large projects (a number of them multi-part) and over 100 smaller projects. These were backed up by descriptive articles on new components, new techniques and new applications. Also in that period we started the 8051/8032 assembler course which has proved popular beyond expectations.

ABC
MEMBER OF THE AUDIT BUREAU OF CIRCULATIONS



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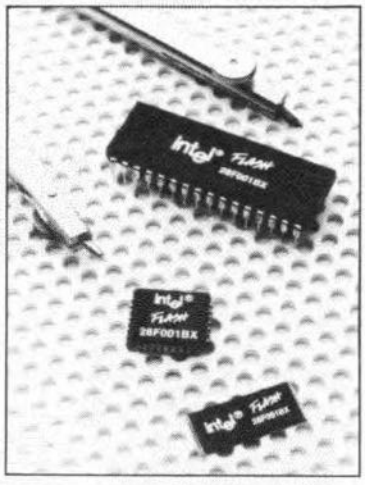

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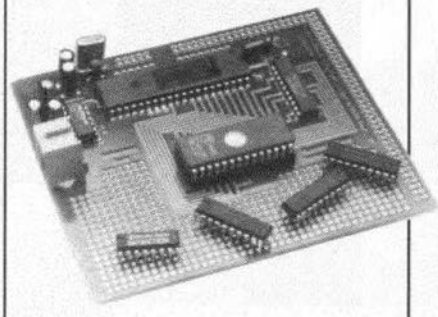

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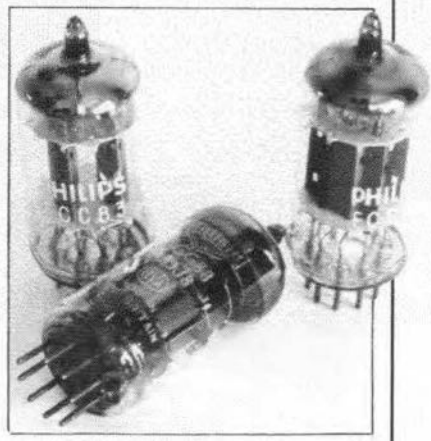


A brief history of the valve – p. 60

WIDEBAND ACTIVE ANTENNA FOR 10 kHz - 220 MHz

This design goes to show that low noise and substantial amplification can go hand in hand in a single amplifier with excellent wideband characteristics. Ideal for use with car radios and communication receivers, or as an active probe for a high-frequency sampling oscilloscope, the design presented here is simple to build from a handful of components.

Design by J. Barendrecht

MOST wideband antenna amplifiers are simply impedance converters that provide some gain. The impedance of a whip or telescopic rod antenna is relatively high because these antennas are short with respect to the wavelength of the received signal. Obviously, this high impedance needs to be transformed down to 50 Ω or 75 Ω to match the receiver input, and that is why most wideband antenna amplifiers 'begin' with an old faithful: the J-FET based source follower.

Now while a J-FET is a nearly ideal impedance converter, its use in a wideband active antenna has two major disadvantages. First, it has a relatively large input capacitance (typically 10 pF), which easily creates a filter in combination with the high antenna impedance. Second, one of the rules of good antenna amplifier design is that the first active stage should provide at least some amplification to ensure the lowest overall noise figure of the design. Unfortunately, this requirement can not be met by the source follower, because it forms an attenuator, and so degrades the overall noise figure considerably.

A different approach

Thus, at the input of a wideband antenna amplifier we require a device that (1) has a low input capacitance; (2) is capable of very high frequency operation at low noise; (3) has a very high input impedance; (4) can cope with high signal levels without running into high intermodulation figures; and (5) provides some gain. That may seem a lot to ask from a single active device, but fortunately a good compromise can be struck by using a dual-gate MOSFET at the amplifier input.

The amplifier discussed here is one of the 'overall feedback' type, of which every one of the three stages provides amplification. Actually, it is a two-stage amplifier with an emitter follower at the output.

As opposed to the J-FET source follower, the MOSFET used here functions as an amplifier, and has an input capacitance of only 2 pF. As shown in the circuit diagram, Fig. 1, a BF981 is used.

The second stage is coupled direct to the MOSFET drain, and is built around the BF979 pnp UHF transistor. A medium-power wideband cable TV driver transistor Type 2N5109 (from Motorola) is used in the emitter follower stage.

Feedback is created by taking the emitter signal of T3 back to the source of T1, via network R7-C4. Without feedback, the gain of the amplifier lies between 15 dB and 20 dB (measured at an output impedance of 50 Ω). With the feedback parts fitted, the gain starts to rise a little at about 100 MHz. The increase amounts to about 2 dB towards the end of the mobile communications section of the VHF band, at about 160 MHz. This effect is caused by the increased phase shift at lower frequencies, which result in a less effective feedback.

The amplifier is powered by a 12-V regulated supply via the downlead coax cable. This so-called phantom supply is shown separately in the circuit diagram. If you are lucky, your receiver has a 12-V power supply, in which case it is conveniently used to power the antenna amplifier. It should be noted that the components in the phantom supply, i.e., the two connectors (K3 and K4), the choke (L2) and the decoupling capacitor (C7) are not fitted on the PCB.

The inductance of chokes L1 and L2 depends on the frequency that is of interest to you. The highest inductance value, 4.7 mH, is used for VLF reception; the lowest value, 470 µH, for VHF/UHF reception. Finding the best value may require some experimenting. In all cases, the d.c. resistance of the chokes must be smaller than 10 Ω.

The output of the amplifier is connected to the phantom supply via BNC connectors and a length of 50-75 Ω coax cable. Inexpensive TV coax cable will be adequate for this application.

The current consumption of the antenna amplifier is not more than 60 mA.

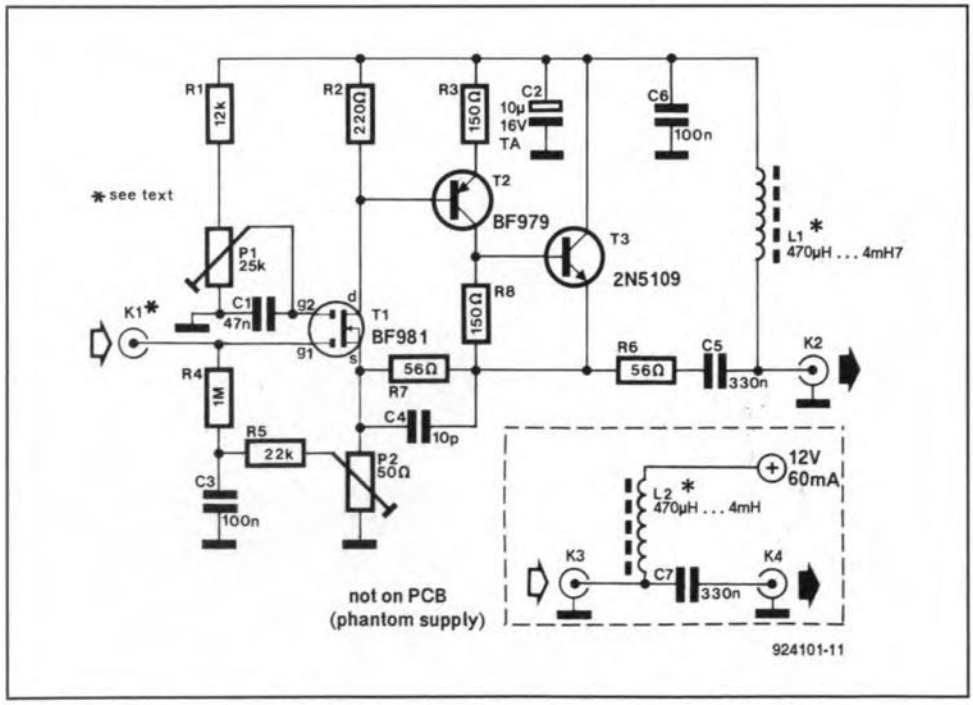


Fig. 1. Circuit diagram of the antenna booster and its phantom power supply.

Construction and adjustment

The amplifier is constructed on the small single-sided printed circuit board shown in Fig. 2. Note that the **dashed parts indicated on the component overlay are fitted at the track side of the board**. The whip or telescopic rod antenna is connected to the amplifier input via a banana socket. The antenna should not be longer than strictly

COMPONENTS LIST

Resistors:

1	12kΩ	R1
1	220Ω	R2
2	150Ω	R3;R8
1	1MΩ	R4
1	22kΩ	R5
2	56Ω	R6;R7
1	25kΩ preset H	P1
1	50Ω preset H	P2

Capacitors:

1	47nF	C1
1	10µF 16V tantalum	C2
2	100nF	C3;C6
1	10pF ceramic	C4
1	330nF	C5

Semiconductors:

1	BF981	T1
1	BF979	T2
1	2N5109	T3

Inductor

1	choke 470µH to 4mH7 (see text)	L1

Miscellaneous:

1	Banana socket, insulated, for chassis mounting, receptacle dia. 2.6 mm	K1
1	BNC socket	K2
1	Printed circuit board	924101

Phantom supply (not on PCB)

2	BNC socket	K3;K4
1	330nF	C7
1	choke 470µH to 4mH7 (see text)	L2

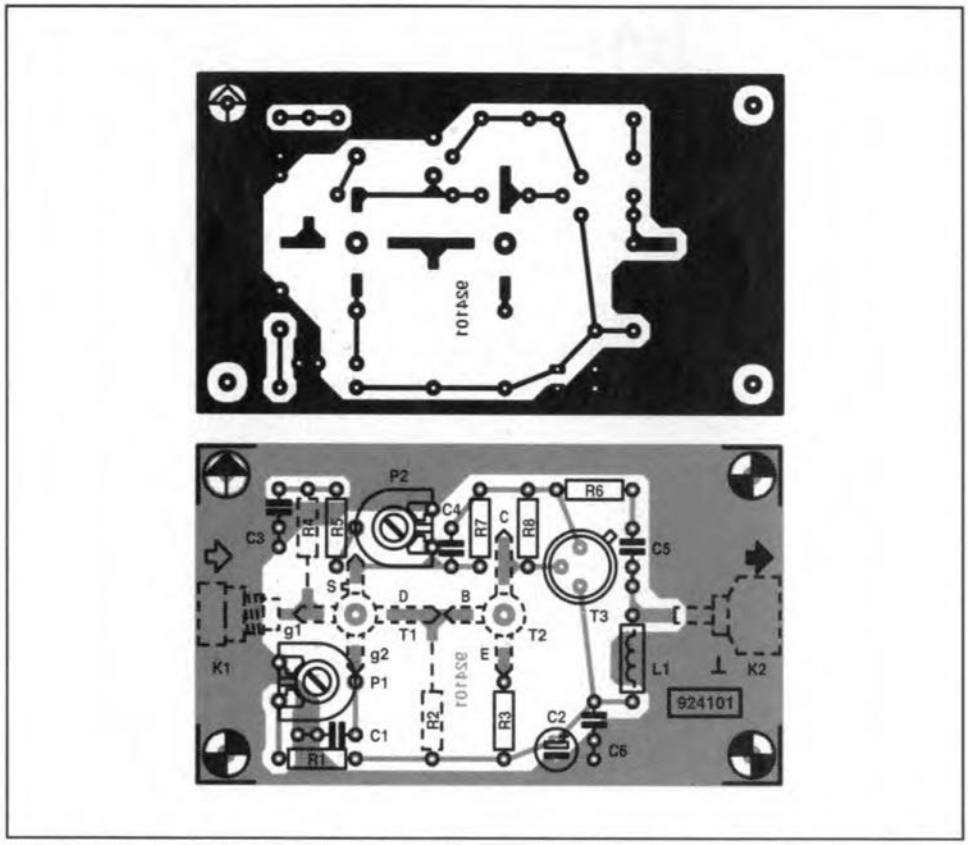


Fig. 2. PCB artwork for the project. Note that a number of components are fitted at the track side of the board.

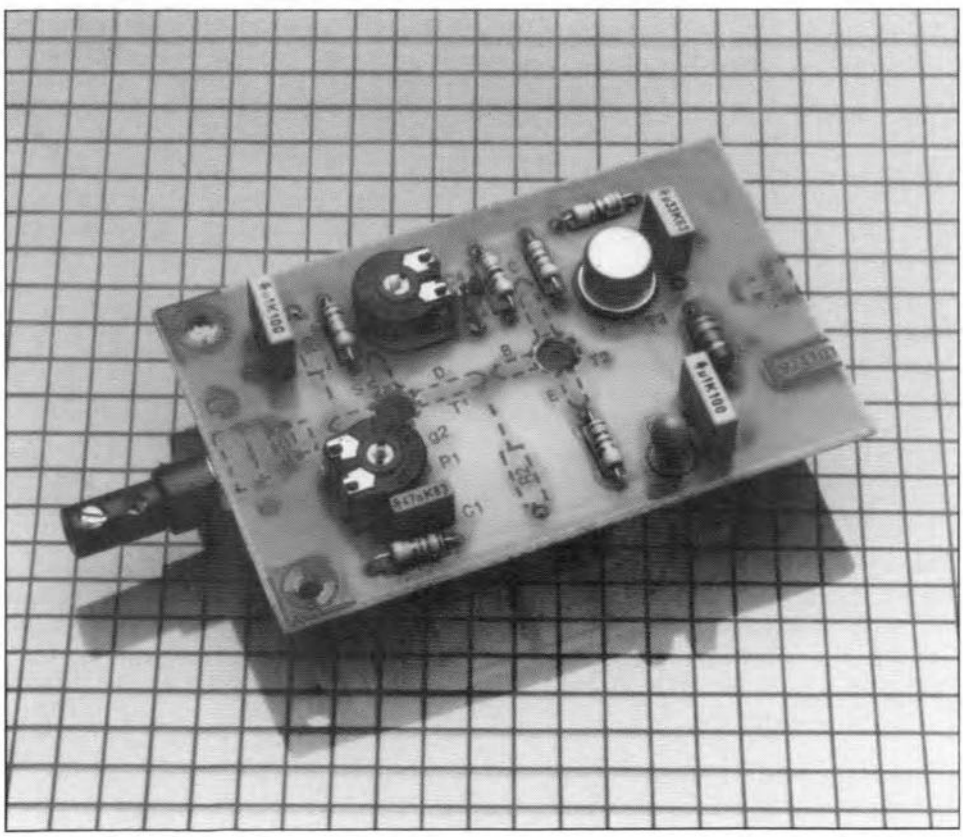
necessary — 30 to 50 cm is long enough in most cases. The prototype used a bicycle spoke cut to about 40 cm and secured to a banana plug. When your reception area is 'infested' with hum (e.g., from nearby mains wiring), the antenna should be coupled to the amplifier input via a 10-pF capacitor.

To ensure proper screening, the completed printed circuit board is fitted in a metal box.

The d.c. setting of the amplifier is dependent on a number of factors, and may require some experimenting for best results. In general, P1 and P2 should be adjusted for a voltage of 6-8 V at the emitter of T3. When the amplifier is used for daytime short-wave or medium-wave reception, the best possible S/N ratio is required. Hence, preset P1 must be adjusted for a gate2-to-source voltage ($U_{g2\text{-}s}$) of between 3 V and 6 V. The lowest voltage that gives adequate reception of a weak station should be used.

For night-time reception, a different setting is required to cope with the much higher signal levels. In that case, we require the smallest possible IM (inter-modulation) distortion, which can only be achieved by passing more current through the MOSFET, so that $U_{g2\text{-}s}$ will be nearer 6 V than with daytime reception. Adjust P1 for minimum IM distortion when very strong signals are received. IM distortion will not occur easily, and a good way to pick up extremely strong signals is to tune to the 21-MHz band (14 m) in the late evening hours, or couple the amplifier input to a large antenna via a very small capacitance (a piece of wire wound around the 'outdoor antenna' cable and connected to K1 will be adequate). Remember, the amplifier input forms a very high impedance, which does **not** allow coax cable to be connected.

Finally, the prototype of the amplifier worked right up to 220 MHz, at which frequency a gain of 5 dB was achieved. ■



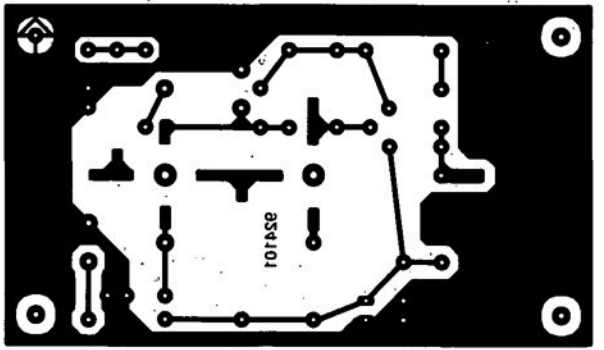
COMPONENTS LIST

Resistors:

1	12kΩ	R1
1	220Ω	R2
2	150Ω	R3;R8
1	1MΩ	R4
1	22kΩ	R5
2	56Ω	R6;R7
1	25kΩ preset H	P1
1	50Ω preset H	P2

Capacitors:

1	47nF	C1



MAINS SEQUENCER

Design by T. Giesberts

When a group of mains-operated electrical or electronic appliances is switched on simultaneously, it may very well happen that the mains fuse(s) blow or the circuit-breakers cut out. This is caused by the peak currents that flow at switch-on, which can be many times larger than the nominal current. A circuit is described that obviates such an unwelcome happening.

WHEN an electrical or electronic apparatus is switched on, a peak current much larger than the nominal one flows, particularly in the case of motors and transformers. If a group of such equipment is switched on at the same time, it is quite likely that the relevant fuse in the consumer unit or distribution board gives up the ghost. Modern circuit breakers react even more quickly to peak currents than fuses. The load already connected to the consumer unit or distribution board must, of course, also be taken into account. The circuit proposed here obviates that risk by switching on the units in a group in a predetermined order at intervals of one second.

The circuit does more than just spreading the switch-on times. It also has a facility that enables determining the switch-on instant with respect to the zero (voltage) crossing of the mains supply. The zero (voltage) crossing is just about the most unfavourable instant for switching inductive loads if it comes to preventing high peak currents. Assuming a pure inductance, voltage and current are 90° out of phase, so that the zero crossing occurs at the instant when the current is maximum. If the appliance is switched on at the zero (voltage) crossing, the current will be extra large because it has a tendency to make up for the lag. If it is switched on at maximum voltage, however, the current will almost immediately assume its nominal value—see Fig. 1. In the upper half of the figure, the appliance is switched on at the zero (voltage) crossing. The current is then initially 'lifted' well above the base line, after which it drops back slowly until equilibrium is reached. In this theoretical case, the current at switch-on has about twice the nominal value. In the bottom half, equilibrium is reached immediately, because the appliance is switched on at maximum voltage. In practice, of course, the correct switch-on moment will lie somewhere between the zero crossing and maximum voltage. Two examples will illustrate the point.

1. A problem occurs when iron-cored transformers and inductors are switched on. The core will have to become magnetized before it functions properly. That means that at switch-on the impedance is determined mainly by the primary winding. This may vary from a few ohms to several hundreds of ohms, depending on the nominal rating of the transformer. For instance, the impedance of a 300 VA toroidal transformer is 2–3 Ω, which could result in a peak current at switch-on of about 100 A. Although that current is limited to some extent by the mains supply, in practice, peak currents of 60 A can nevertheless arise.
2. Another problem occurs when inductors are switched off and then on again. Owing to residual magnetism, the core may have a weak magnetic field before switch-on. When switch-on occurs 90° after a zero (voltage) crossing, a large current will result. It is, therefore, better to ensure that no magnetic field exists just prior to switch-on.

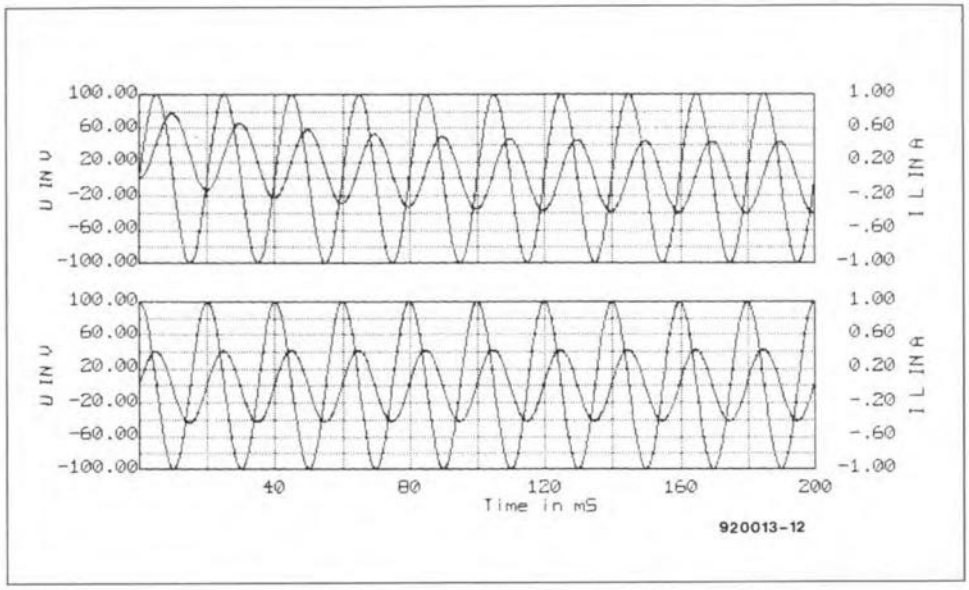


Fig. 1. When a sinusoidal voltage across an inductance is switched on, the phase angle at which this happens determines the level of the peak current through the inductance.

In the proposed circuit, the instant of switch-on can be preset to enable the user to choose the best (or rather, the least bad) moment for the particular appliance(s).

Circuit description

Although the design can handle four outputs drawing a current of 5 A each, in the UK it is best to limit this to 3–4 A each, because the maximum rating of the fuse in the usual ring mains plug is 15 A. That means loads of 800–1000 W per output.

The ±5 V for the circuit is provided by a small power section that uses regulators Type 7805 and 7905. The transformer specified in the parts list is short-circuit-proof, so that a fuse is not needed.

There is no on/off switch, because that would have to be rated at 20 A, which is not a standard part. Instead, D_5 indicates whether the unit is plugged into the mains or not. This diode and its bias resistor, R_{39}, form a minimum load for the positive voltage regulator, while R_{40} provides the same function for the negative voltage regulator. This arrangement means that the regulators always deliver at least a small current, so that regulation is ensured. If no, or only a tiny, current flows, the output voltage tends to rise to the level of the input voltage.

The zero (voltage crossing) is determined by IC_2, a sort of comparator with a small hysteresis. Its output is a square-wave voltage that is in phase with the mains voltage. The hysteresis can be set with P_1 to a value where the trailing edge of the square-wave voltage

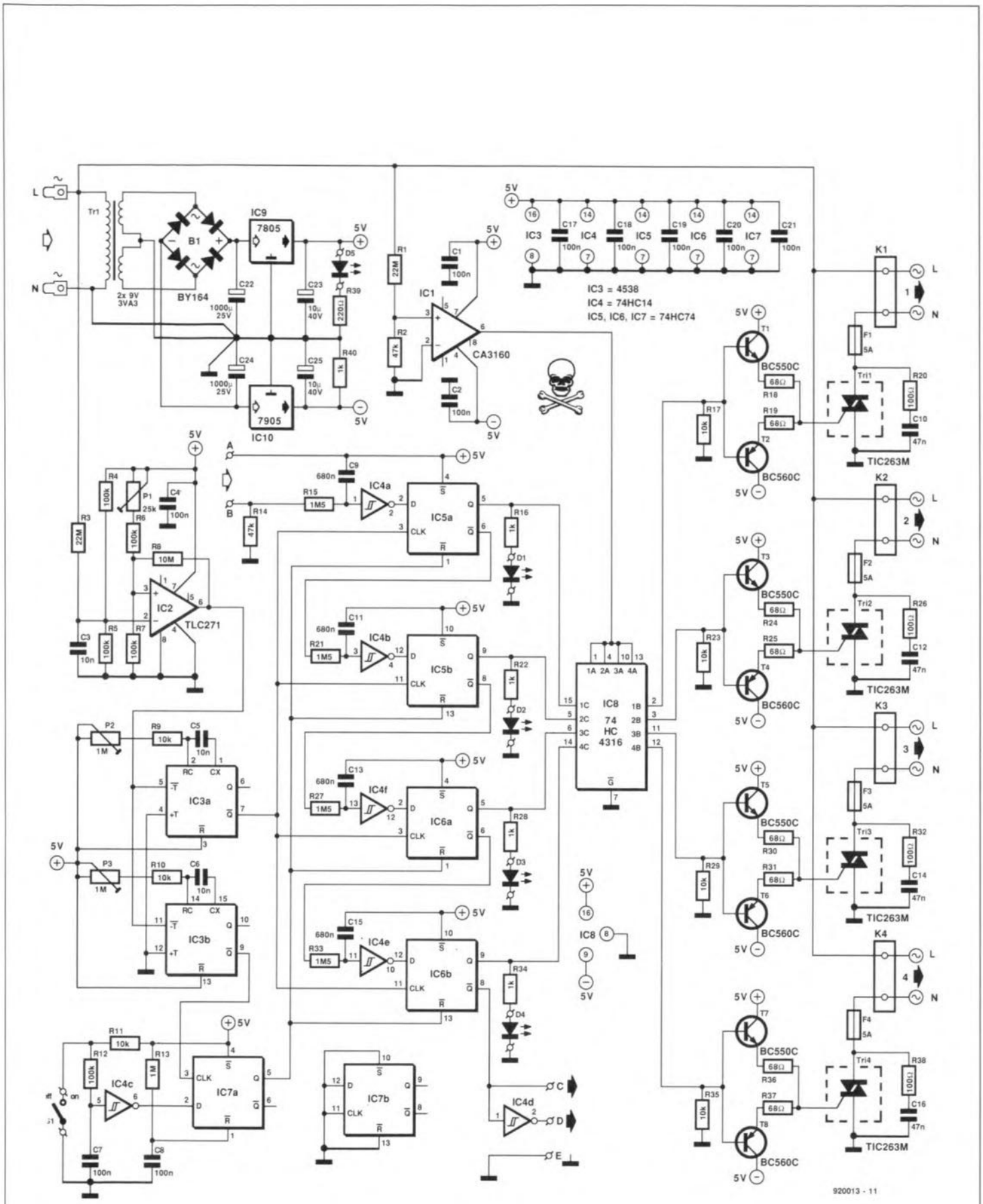


Fig. 2. Circuit diagram of the mains sequencer.

PARTS LIST

Resistors:
R1, R3 = 22 MΩ
R2, R14 = 47 kΩ
R4–R7, R12 = 100 kΩ
R8 = 10 MΩ
R9–R11, R17, R23, R29, R35 = 10 kΩ
R13 = 1 MΩ
R15, R21, R27, R33 = 1.5 MΩ
R16, R22, R28, R34, R40 = 1 kΩ
R18, R19, R24, R25, R30, R31, R36, R37 = 68 Ω
R20, R26, R32, R38 = 100 Ω
R39 = 220 Ω

Capacitors:
C1, C2, C4, C7, C8, C17–C21 = 100 nF
C3, C5, C6 = 10 nF
C9, C11, C13, C15 = 680 nF
C10, C12, C14, C16 = 47 nF, 630 V
C22, C24 = 1000 µF, 25 V, radial
C23, C25 = 10 µF, 40 V, radial

Semiconductors:
D1–D4 = LED, high efficiency*
D5 = LED*
B1 = BY164
T1, T3, T5, T7 = BC550C
T2, T4, T6, T8 = BC560C
IC1 = CA3160
IC2 = TLC271
IC3 = 4538
IC4 = 74HC14
IC5–IC7 = 74HC74
IC8 = 74HC4316
IC9 = 7805
IC10 = 7905
Tri1–Tri4 = TIC263M

* Use only with approved insulated holder.

Miscellaneous:
K1–K4 = 2-way terminal block, 7.5 mm pitch
S1 = single-pole mains switch
Tr1 = mains transformer; 2×9 V, 3.3 VA secondary (e.g. Monacor VTR3209)
F1–F4 = fuse, 5 A
4 fuse holders for PCVB mounting
2 heavy-duty mains terminals for screwing on to PCB
4 heat sinks for Tri1–Tri4, 5 K/W (e.g. Fischer SK129, available from Dau, Barnham, Sussex, Telephone 0243 553 031)
4 Mains outlet chassis socket
1 mains inlet chassis plug
5 insulated LED holders
4 LED lenses, red
1 LED lens, green
1 enclosure (e.g., LC860 from Telet)
1 PCB Type 920013 (see page 70)

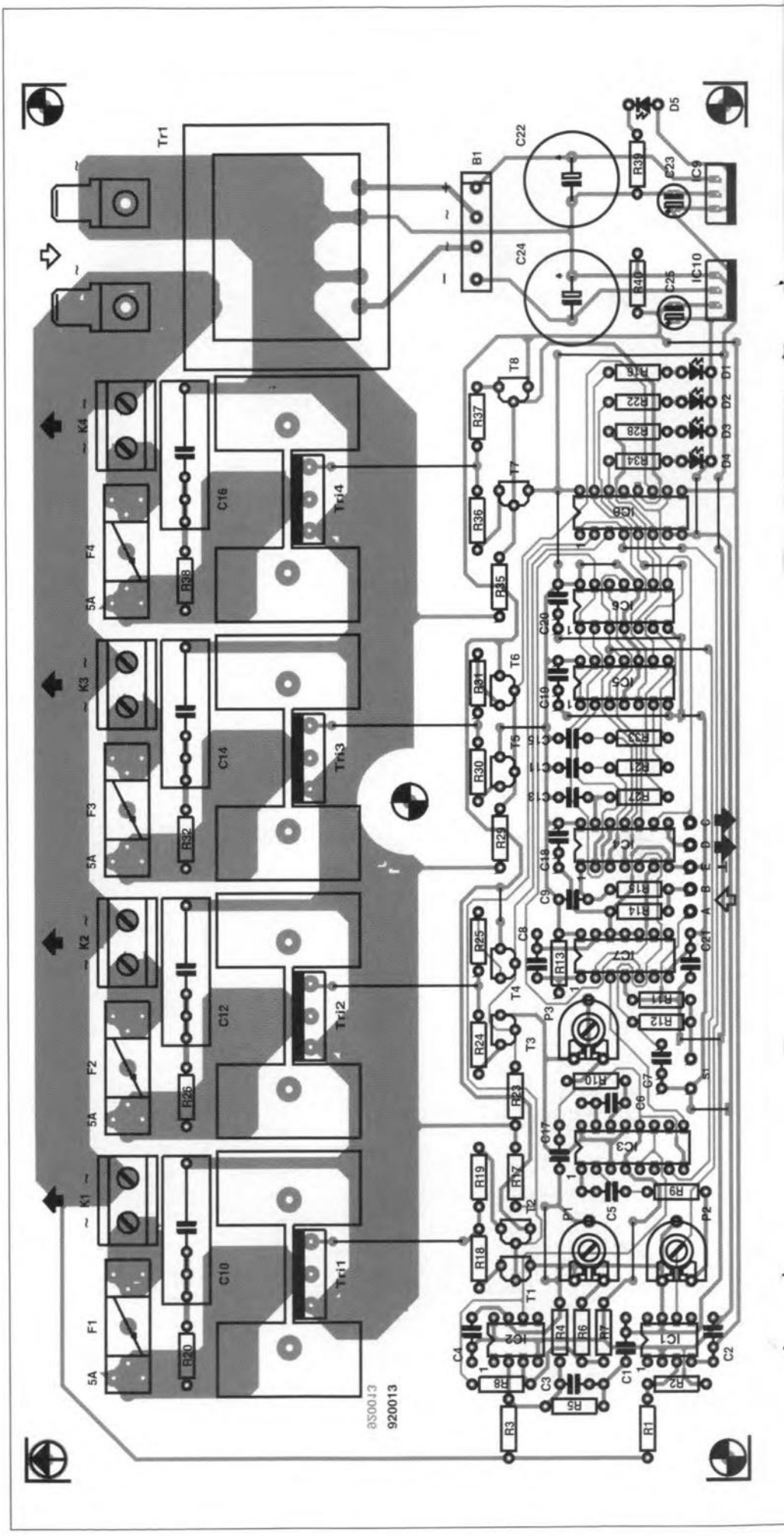
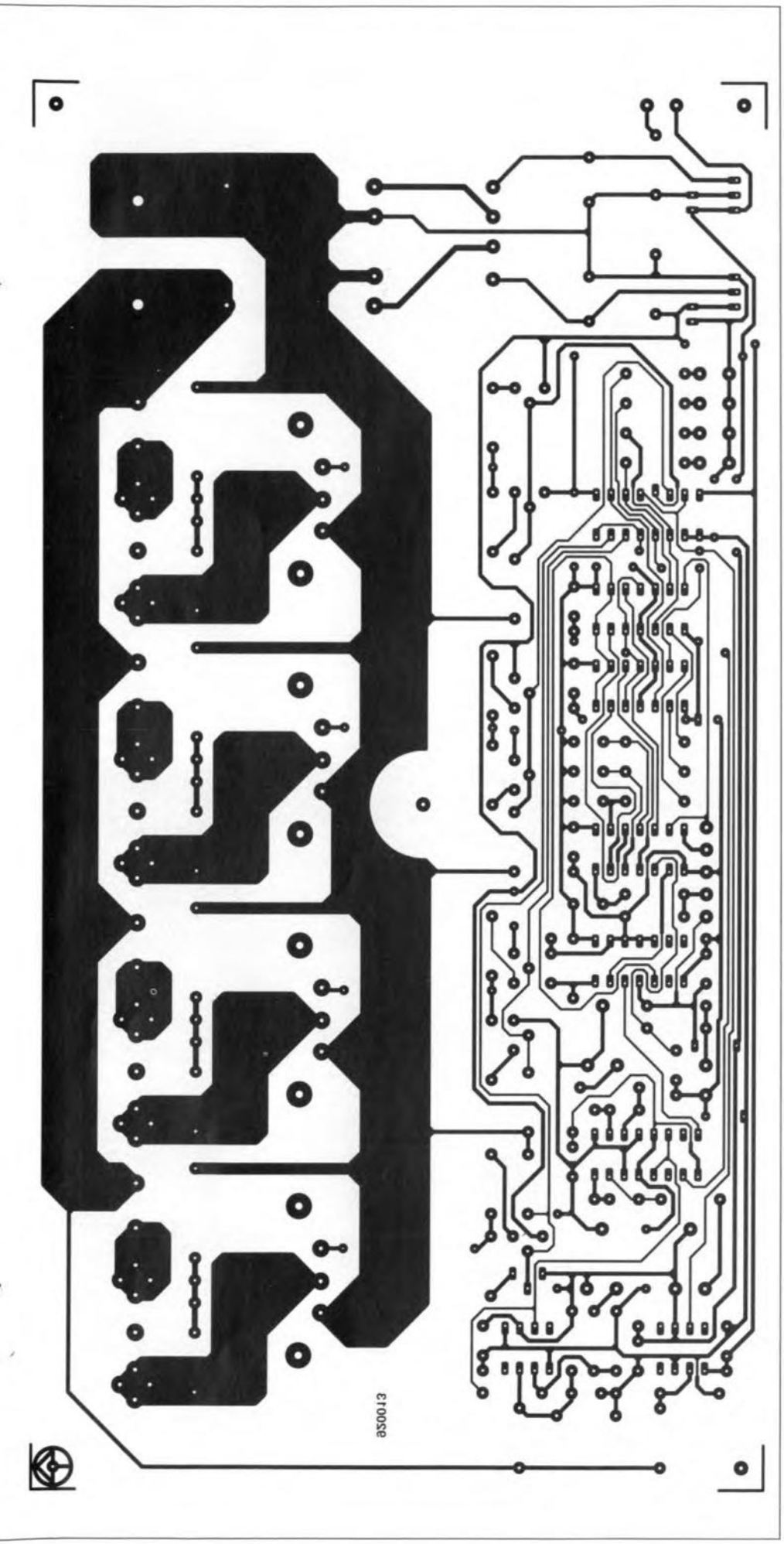


Fig. 3. Printed circuit board for the mains sequencer.



coincides exactly with the zero crossing at the start of a positive half cycle of the mains voltage.

The hysteresis, in conjunction with filter R_3–C_3, ensures that IC_2 is virtually not affected by noise on the mains.

The trailing edge of the output signal of IC_2 triggers two monostables, IC_{3a} and IC_{3b}, which, respectively, determine the switch-on and switch-off moment relative to the zero (voltage) crossing. The mono times may be set between 0.1 ms and 10 ms, which, in practical terms, means between a minute part of a period and a half period.

The sequential switching of the loads is effected by bistables IC_{5a}, IC_{5b}, IC_{6a}, and IC_{6b}. In the following, it is assumed that S_1 is closed and IC_{7a} reset. The bistables are chain-linked via an *RC* network and a Schmitt trigger/inverter that ensures a 1 second delay between their being switched. Bistable IC_{5a} is the first in the chain. When it is switched on, the D-input of IC_{5b} goes high; when this bistable is clocked, its Q output goes high and the associated output is switched on. At the same time, the D input of IC_{6a} goes high. The clock is provided by IC_{3a}, which, as we have seen, is triggered at a zero (voltage) crossing after every period. The four bistables are not clocked, however, until the mono time of IC_{3a} has elapsed. In other words, setting the pulse width also determines the delay between the zero crossing and the switch-on instant.

Switching off the outputs may be effected in two ways. The first is via IC_{3b}, IC_{7a} and S_1. This action is similar to that at switch-on: IC_{3b} clocks IC_{7a} in step with the mains voltage, so that the switch-off instant can also be set relative to the zero crossing. When S_1 is opened, the D input of IC_{7a} goes low via IC_{4c}, which causes the bistable to be reset. This results in the resetting of bistables IC_{5a}, IC_{5b}, IC_{6a} and IC_{6b}, so that all outputs are switched off. A power-up reset is arranged by IC_{7a} in conjunction with filter R_{13}–C_8.

The second way of switching off the outputs is by closing a switch between A and B, in which case the switching off is sequential.

The signals at the Q outputs of IC_{5a}, IC_{5b}, IC_{6a} and IC_{6b} indicate whether an output is on or off. This can be made visible by connecting an LED to each of these pins.

Unfortunately, these signals cannot be used directly to drive the gates of the triacs. This is because, if the mains has a polarity relative to ground different from that of the gate voltage, part of the gate current will not flow directly to ground, but via the load and the mains. That means that a small direct current will flow through the load, to which mains transformers react adversely.

The design of the sequencer ensures that the gate current always flows directly to ground. The output signal of IC_1 indicates the polarity of the mains relative to ground. This signal is fed to four 'output stages', T_1–T_8, via four analogue CMOS switches contained in IC_3 and controlled by IC_{5a}, IC_{5b}, IC_{6a} and IC_{6b}. Depending on the output signal of IC_1, each of the output stages drives the associated gate with a current of ±50 mA. A switched-

on triac is, therefore, driven constantly via its gate, so that it remains on. This design has the advantage over pulse-driving the gate that not only ohmic, but also reactive, loads can be switched without any problems.

Construction

It must be borne in mind at all times that the entire circuit is electrically connected to the mains supply. As long as the circuit has not been built into a suitable enclosure, no mains should be supplied to it or, if it is for test purposes, extreme care should be taken not to touch the circuit with your bare hands or non-insulated tools.

Furthermore, under no circumstances must the ground of the sequencer be connected to earth (mains or otherwise).

Populating the ready-made printed-circuit board should present no problems. Although the triacs may be mounted uninsulated on to the heat sinks, it is better to use an insulating washer to keep the heat sinks free of mains voltage (but not safe!). Note also that the LEDs should be fitted in holders as specified in the parts list, because a 'bare' LED does not meet safety requirements.

Do not use screws thicker than 4 mm (4 BA) to prevent them getting too close to voltage-carrying parts of the board.

Fix the board with *five* screws: the fifth is essential at the centre of the board in view of the length of the board and the weight of the heat sinks.

Fit the board on to 10 mm ($^{13}/_{32}$ in) long insulated (man-made fibre) spacers (metal ones might come too close to voltage-carrying parts, which would make protruding screws unsafe).

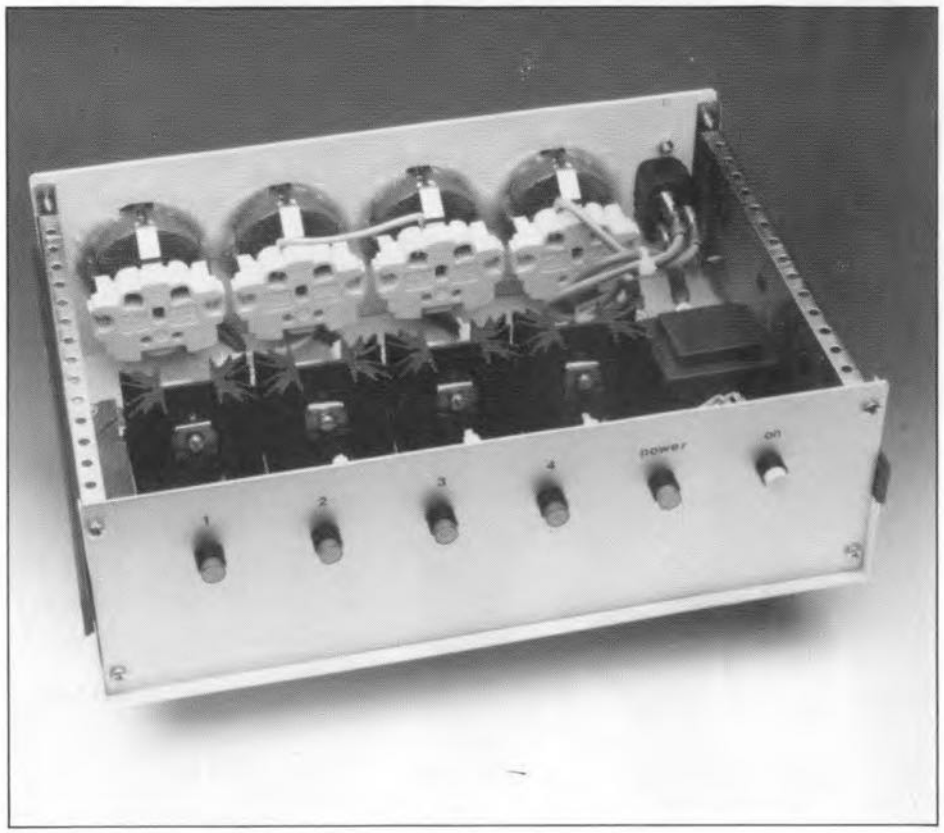
Keep conducting parts of the enclosure (also any metal parts of a man-made fibre one) that can be touched from the outside well away (at least 3 mm—$^{1}/_{8}$ in— preferably 10 mm—$^{13}/_{32}$ in) from voltage-carrying parts of the board.

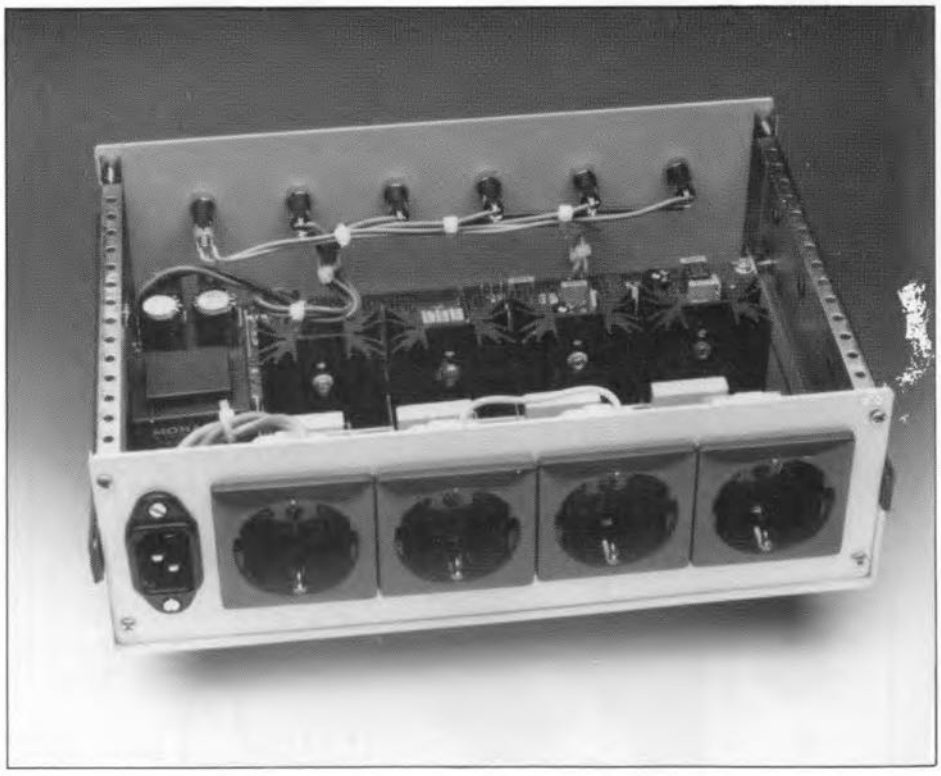
When you link two boards, make absolutely sure that the mains connections are not interchanged, since the neutral line is connected to ground.

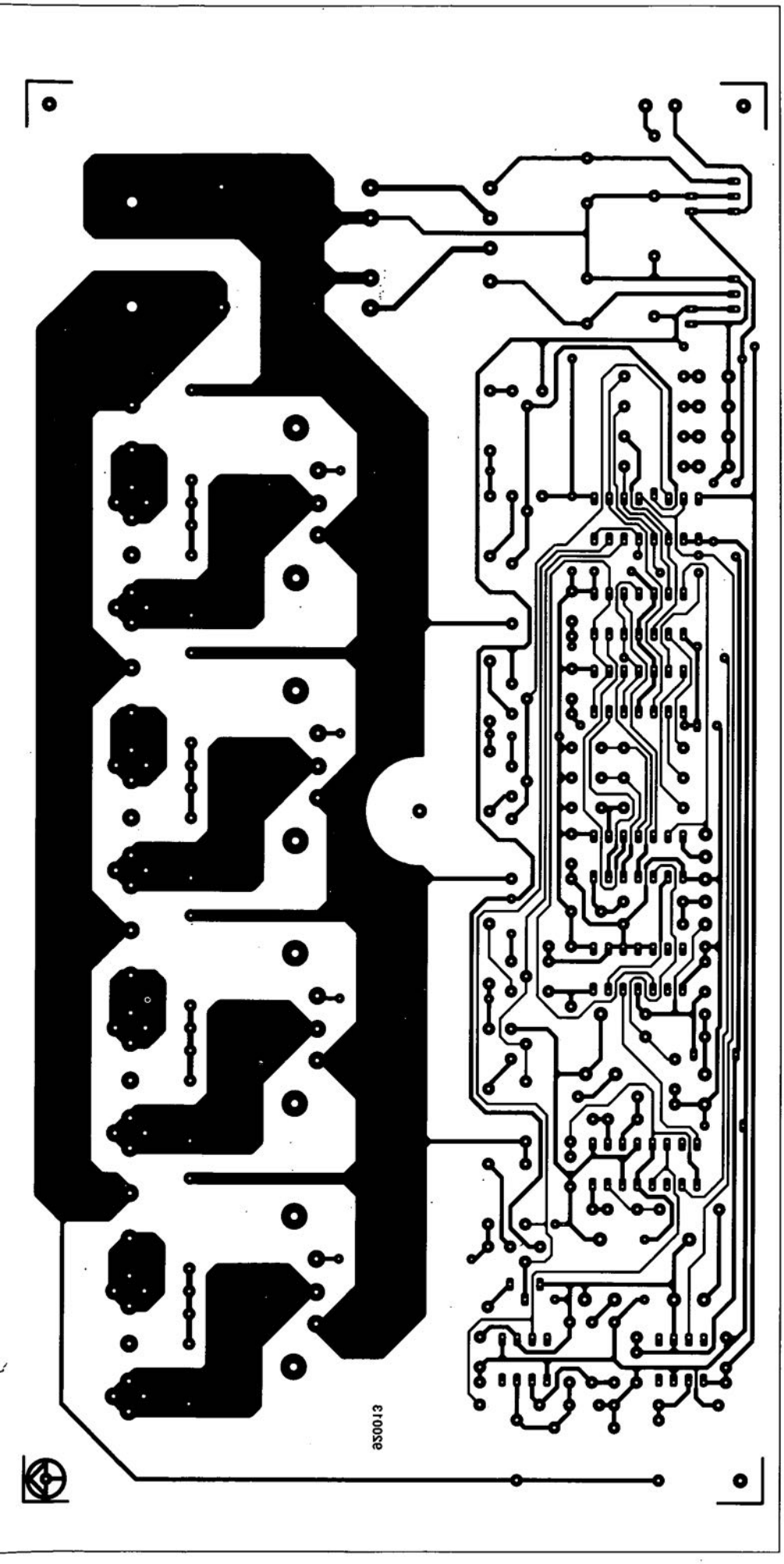
When choosing an enclosure, make sure that the ventilation holes are not larger than 5 mm ($^{3}/_{16}$ in), but preferably 3 mm ($^{1}/_{8}$ in).

Any metal parts of the enclosure that can be touched should be connected to mains earth.

The insulation of switch S_1 must conform to the relevant safety regulations for mains-operating switches. ■







coincides exactly with the zero crossing at the start of a positive half cycle of the mains voltage.

The hysteresis, in conjunction with filter R_3–C_3, ensures that IC_2 is virtually not affected by noise on the mains.

The trailing edge of the output signal of IC_2 triggers two monostables, IC_{3a} and IC_{3b}, which, respectively, determine the switch-on and switch-off moment relative to the zero (voltage) crossing. The mono times may be set between 0.1 ms and 10 ms, which, in practical terms, means between a minute part of a period and a half period.

The sequential switching of the loads is effected by bistables IC_{5a}, IC_{5b}, IC_{6a}, and IC_{6b}. In the following, it is assumed that S_1 is closed and IC_{7a} reset. The bistables are chain-linked via an *RC* network and a Schmitt trigger/inverter that ensures a 1 second delay between their being switched. Bistable IC_{5a} is the first in the chain. When it is switched on, the D-input of IC_{5b} goes high; when this bistable is clocked, its Q output goes high and the associated output is switched on. At the same time, the D input of IC_{6a} goes high. The clock is provided by IC_{3a}, which, as we have seen, is triggered at a zero (voltage) crossing after every period. The four bistables are not clocked, however, until the mono time of IC_{3a} has elapsed. In other words, setting the pulse width also determines the delay between the zero crossing and the switch-on instant.

Switching off the outputs may be effected in two ways. The first is via IC_{3b}, IC_{7a} and S_1. This action is similar to that at switch-on: IC_{3b} clocks IC_{7a} in step with the mains voltage, so that the switch-off instant can also be set relative to the zero crossing. When S_1 is opened, the D input of IC_{7a} goes low via IC_{4c}, which causes the bistable to be reset. This results in the resetting of bistables IC_{5a}, IC_{5b}, IC_{6a} and IC_{6b}, so that all outputs are switched off. A power-up reset is arranged by IC_{7a} in conjunction with filter R_{13}–C_8.

The second way of switching off the outputs is by closing a switch between A and B, in which case the switching off is sequential.

The signals at the Q outputs of IC_{5a}, IC_{5b}, IC_{6a} and IC_{6b} indicate whether an output is on or off. This can be made visible by connecting an LED to each of these pins.

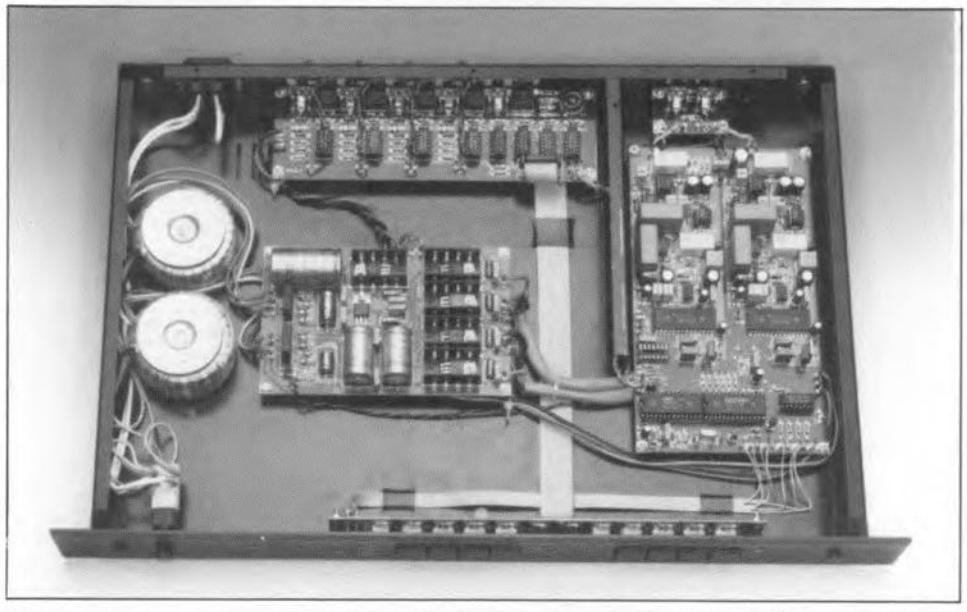
Unfortunately, these signals cannot be used directly to drive the gates of the triacs. This is because, if the mains has a polarity relative to ground different from that of the gate voltage, part of the gate current will not flow directly to ground, but via the load and the mains. That means that a small direct current will flow through the load, to which mains transformers react adversely.

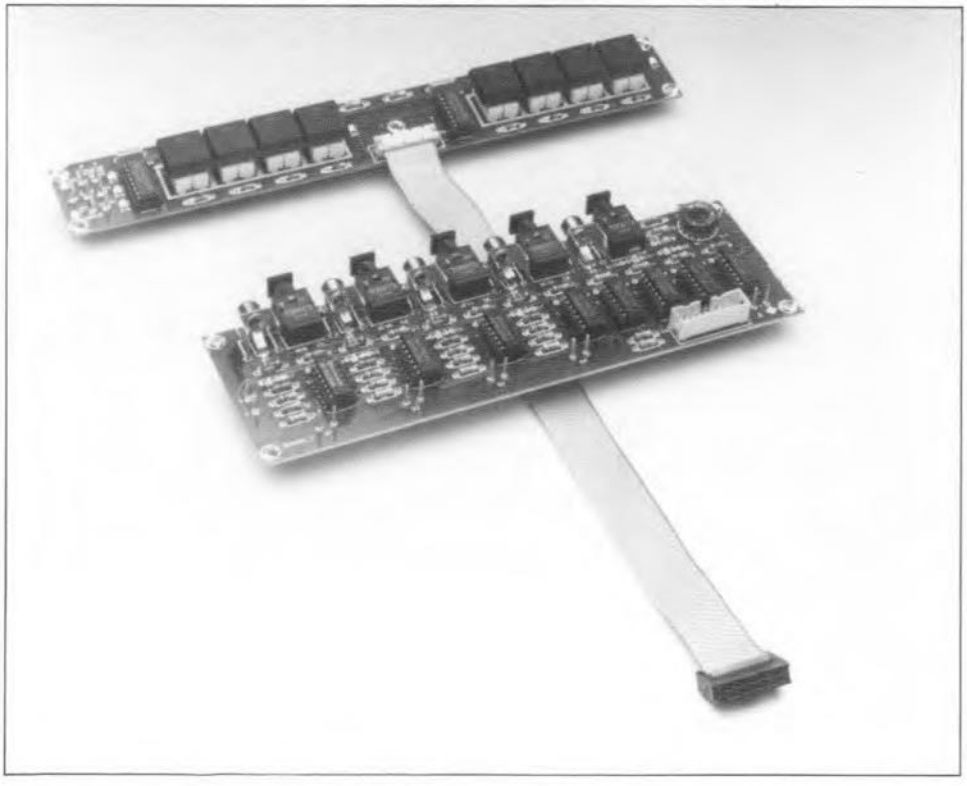
The design of the sequencer ensures that the gate current always flows directly to ground. The output signal of IC_1 indicates the polarity of the mains relative to ground. This signal is fed to four 'output stages', T_1–T_8, via four analogue CMOS switches contained in IC_3 and controlled by IC_{5a}, IC_{5b}, IC_{6a} and IC_{6b}. Depending on the output signal of IC_1, each of the output stages drives the associated gate with a current of ±50 mA. A switched-

A.F. DIGITAL-TO-ANALOGUE CONVERTER

PART 3 (FINAL)

Design by T. Giesberts





STRICTLY speaking, the converter described so far does not need switching logic, since it can simply be connected direct to a CD player. However, developments in digital audio equipment make it a wise decision to fit the converter with the input/output selector circuit described in this final part of the article. This circuit enables the selection of one of four different digital input signals. Moreover, a tape out facility makes it possible to connect one of the four inputs to a digital recorder, while one of the other three can be listened to at the same time. All inputs and outputs can be linked to either coaxial or optical lines. The inputs are selected with key switches. Four more of these switches facilitate the looping of one of the inputs to the tape record output. The selected source and record inputs, as well as the various settings of the converter, are indicated on the front panel—see Fig. 18.

Circuit description

The circuit will be described with reference to channel 1: the design of the other three channels is identical—see Fig. 16.

The coaxial input is terminated into a 75 Ω resistor, R_1. The bi-phase signal is fed via C_1 and R_2 to inverter IC_{1a}, which operates as an amplifier. Capacitor C_{31} suppresses any tendency of the gate to oscillate. Feedback resistor R_3 enables an amplification of ×6 to be obtained, so that the output of the inverter is about 3 V_{pp}. Note that the design of the circuit is identical to that of the input circuit in Fig. 5 (in Part 1).

The level of the output of IC_{1a}; which is applied to IC_{1b}, is exactly half-way between that of the supply voltage and earth. This enables IC_{1b} to produce rectangular signals with minimal displacement of the transitions (edges) of the signal. This is important for an optimum reconstruction of the original digital signal.

The signal is then applied to three-state buffer IC_{3b}, which processes it if switch S_1 is open. If S_1 is closed, IC_{3b} is off and buffer IC_{3a}, which is fed with the signal from the optical input circuit, IC_9, is on.

The three-state buffers are followed by two more buffers, IC_{5d} and IC_{6d}, which are operated by the key-switch logic. In that way it is determined which of the input signals drives the converter (IC_{5d}) or the tape output (IC_{6d}).

The optical input consists of a receive diode and a components contained in a small plastic module called a Toslink (named after its manufacturer, Toshiba). Externally, the circuit, whose output is TTL compatible, only needs a power line decoupler, here consist-

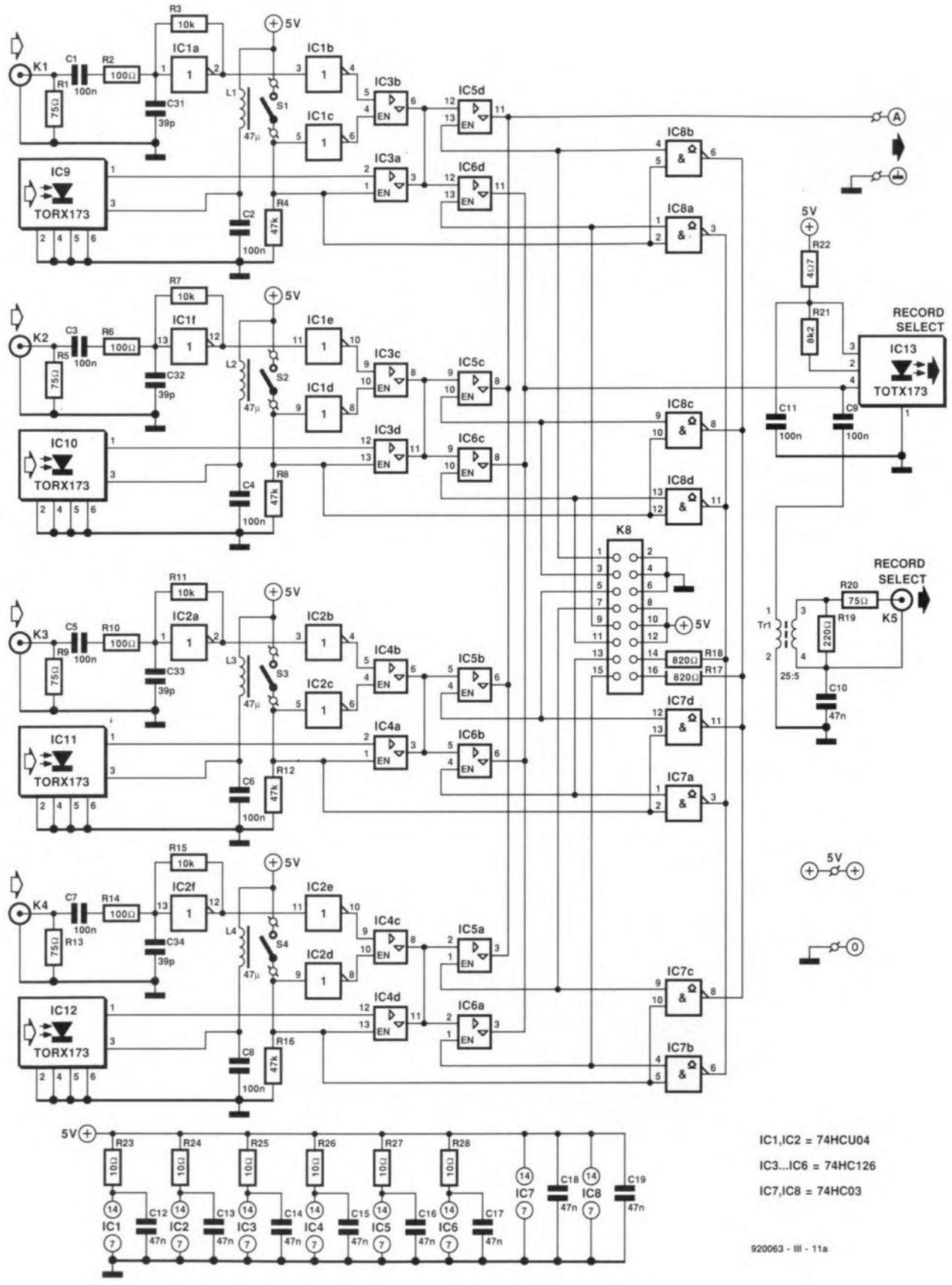
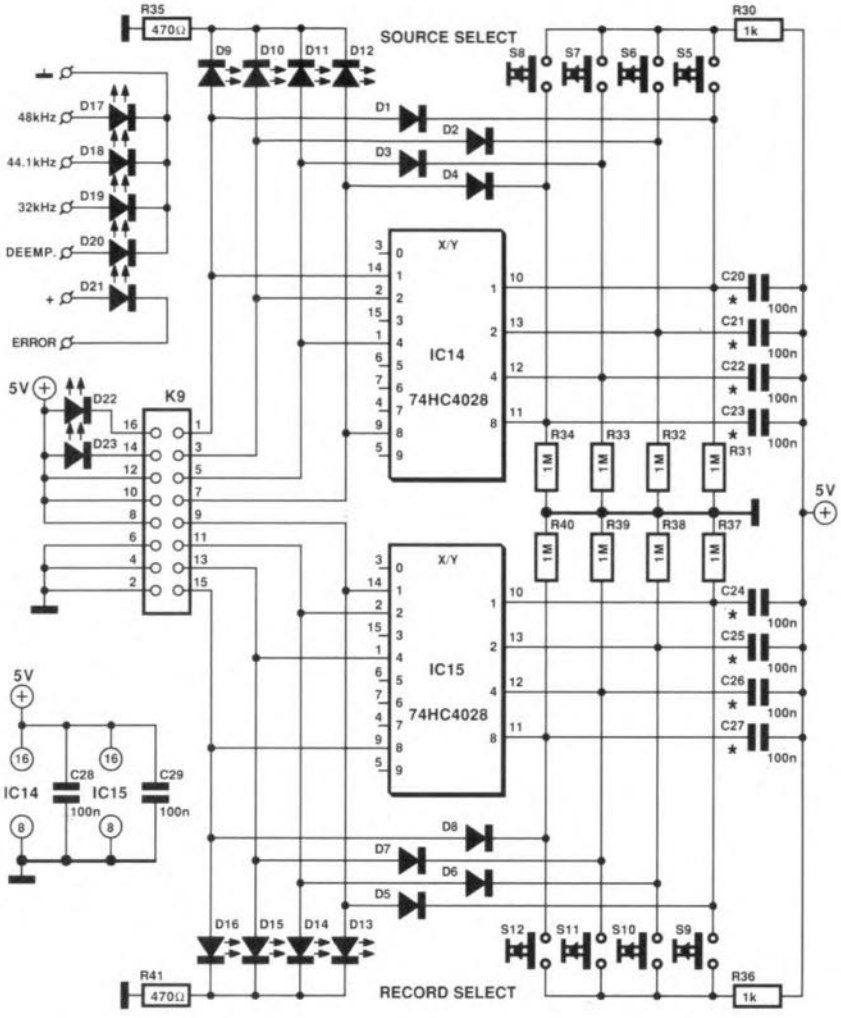


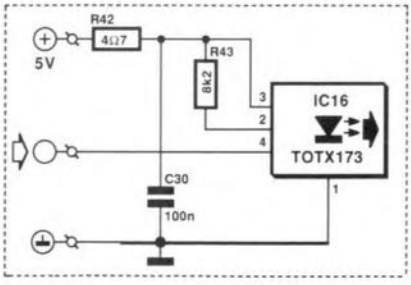
Fig. 16. Circuit diagram of the input/output selector.

Toslinks

The TORX173 and TOTX173 devices are available from

Highland Electronics Ltd
Albert Drive
Burgess Hill RH15 9TN
England
Telephone (0444) 236 000





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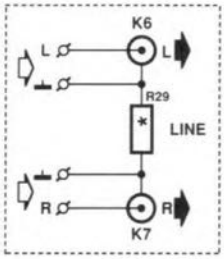
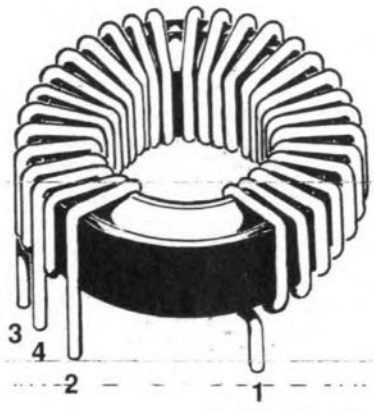


920063 - III - 11b



920063 - III - 12

ing of L_1 and C_2.

The tape output, too, is coaxial or optical, the latter again with the aid of a Toslink. Here, this circuit externally needs two resistors, R_{21} and R_{22}, and a capacitor, C_{11}. The coaxial output needs to be isolated (to ensure that no earth loop can arise via the ground line of the digital connection) and this is achieved by a small transformer, Tr_1. In the CD player a special Philips transformer was used, but here a wind-it-yourself type is used—how it is made is described later. Note already, however, that its bandwidth is far greater (at least in our prototype) than that of any ready-made type that was tried.

The switching signals are provided by two identical circuits, IC_{14}, which determines which signal is applied to the converter, and IC_{15}, which ensures that one of the input signals is applied to the tape output. Only the circuit based on IC_{14} will be described.

Four key-switches, S_5–S_8, are connected to the inputs of the circuit, a BCD-to-decimal decoder. When a key-switch is operated, the associated input becomes logic high. The decoder translates this into the relevant decimal level to render the appropriate output high (input A is associated with output Q_1, pin 14; input B with output Q_2, pin 2 and so on).

The outputs are fed back to the inputs via diodes D_1–D_4 to ensure that an output remains high when the relevant key-switch is released.

The outputs are connected to LEDs that indicate which output is active.

Of the four capacitors C_{20}–C_{23}, only that in the output associated with the input selected on power-up is used.

In the same way, only one of capacitors C_{24}–C_{27} in the tape select circuit is needed.

Gates IC_7 and IC_8 serve to show the user (on the front panel) which type of input (optical or coaxial) is in use with the selected source and record signal. To this end, each gate is connected with the control input of one of the three-state buffers and with one of the selector switches, S_1–S_8. When a given source or record input is selected, D_{22} or D_{23} indicates whether a coaxial (LED out) or optical connection (LED on) is in use with that input.

Five more LEDs at the front panel indicate which of the three sampling frequencies is being used, whether the deemphasis correction is on, and when there is an error in the digital transmission chain.

Audio output connectors K_6 and K_7 are shown separately on the diagram, because they are housed on a discrete small PCB. Resistor R_{29} is for use only if earth loops occur between the left-hand and right-hand channels. Its value (anywhere between a short circuit and a few ohms) must be determined empirically. If, as should be expected, there are no earth loops, R_{29} is simply omitted.

Also shown by itself is the optical output based on IC_{16}, which too is housed on a separate small PCB. This board is really intended for installation in the CD player (the output board of the player already has provision—in the shape of three solder pins—for receiving it).

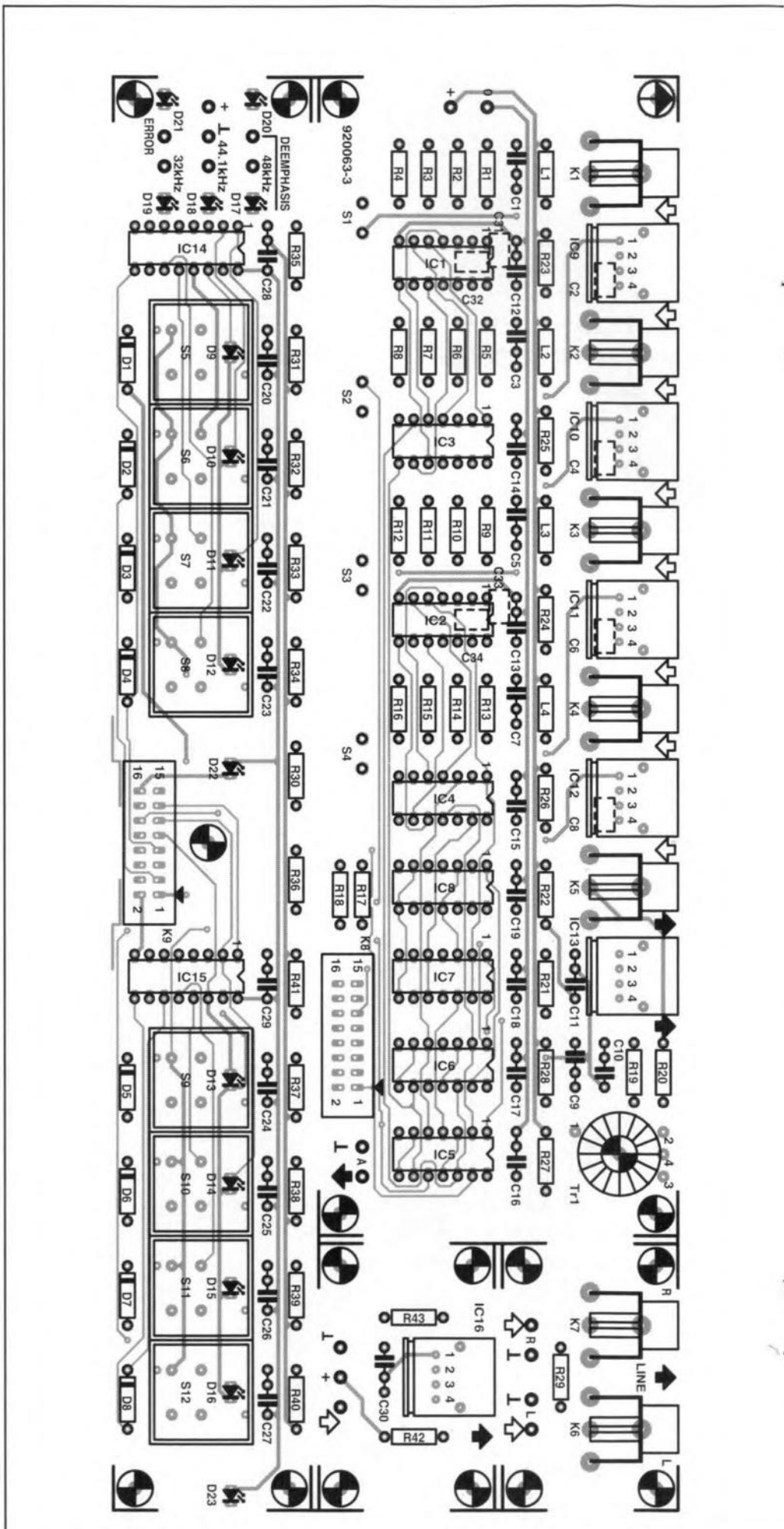
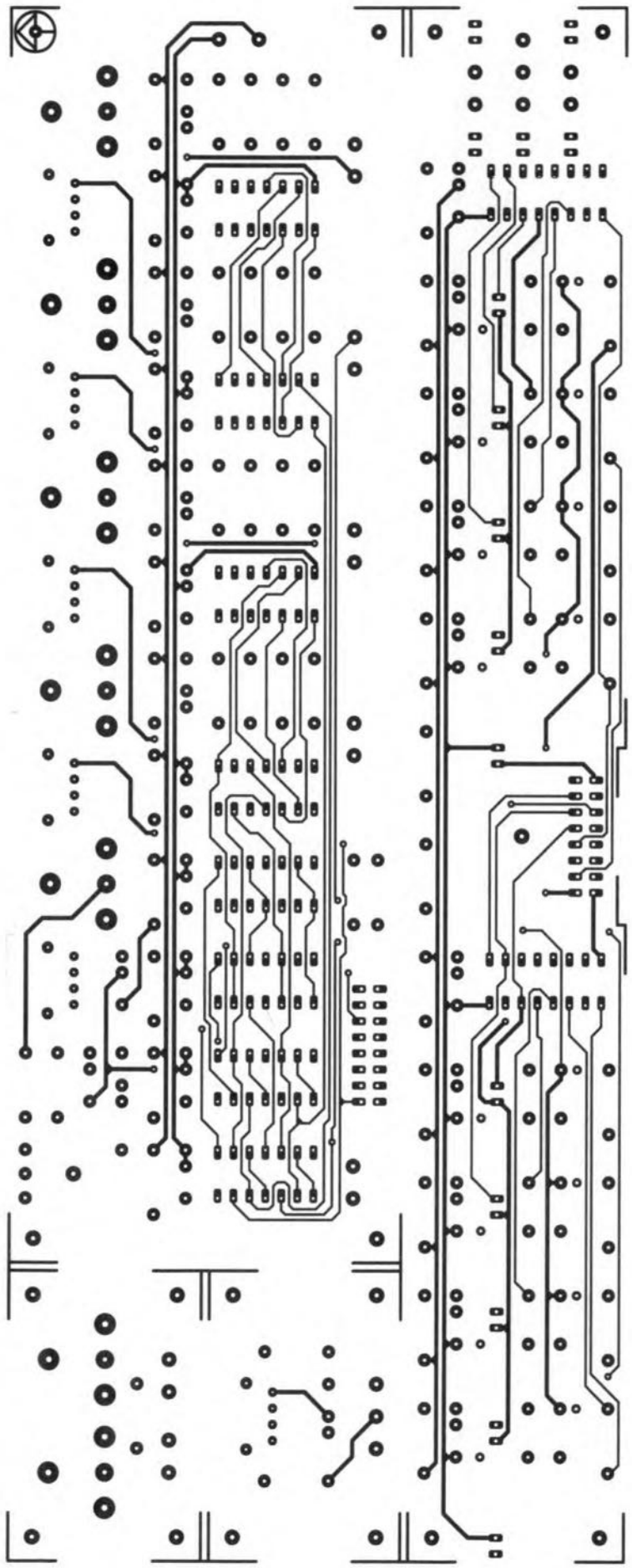


Fig. 17. Printed-circuit board for the input/output selector (continued on pages 25



and 26).

Construction

The printed-circuit board in Fig. 17 should be snapped into four along the relevant seams. The resulting parts are: the busboard with the digital inputs and outputs, the switching board, the analogue output board, and the board for the optical output of the CD player. The analogue board is not needed if insulated audio sockets are used at the rear panel of the converter, and a number of users will not want the optical output for the CD player.

Before buying any LEDs, note that some of them alreay appeared on the mother board (see Fig. 15 in Part 2).

The core for Tr_1 (see inset at bottom right of Fig. 16) must be as indicated in the parts list or the transformer will not perform satisfactorily. Close-wind 25 turns of 1 mm² enamelled copper wire on to the core. Then wind five turns of the same type of copper wire over a width of about 5 mm ($^3/_{16}$ in) over one end of the primary 25 turns. The numbers at the terminals correspond with numbers on the PCB.

Capacitors C_2, C_4, C_6, and C_8, are SMD (surface mount design) types that must be soldered at the track side of the board beneath the Toslinks.

The key-switches should preferably be types with integral LEDs, but this is, of course, not essential.

The switching board and the busboard are linked by a short length of 16-core flatcable; normally a length of 30 cm (12 in) will suffice, but this does, of course, depend on the way the boards are fitted in the enclosure. This cable is fitted to the switching board via a flatcable connector with solder tags, while its other end is terminated into a connector that mates with the 16-way header on the busboard.

How everything should be installed into the 19-inch enclosure and what connections are necessary are shown in Fig. 18. Mount the switching board directly behind the front panel. Note the central fixing hole, which is provided to prevent the board bending unduly when the keys are pressed. Run the flatcable under the board to the rear of the enclosure.

Fit the busboard to the rear panel of the enclosure to ensure that all plugs and sockets are easily accessible. The rear panel may be given individual holes for the various connectors or a common rectangular slot. Mount a small slide switch above each audio connector/Toslink combination in such a way that, when open, it points in the direction of the audio connector. It is, of course, not mandatory to fit the Toslinks.

Mount the two transformers at the left of the enclosure and the power supply board roughly at the centre immediately adjacent to the transformers—see photo on page 21.

Fit the busboard at the extreme right of the enclosure in such a way that the analogue output board can just be mounted behind it. It is advisable to screen the left-hand side of the busboard with a small piece of tin

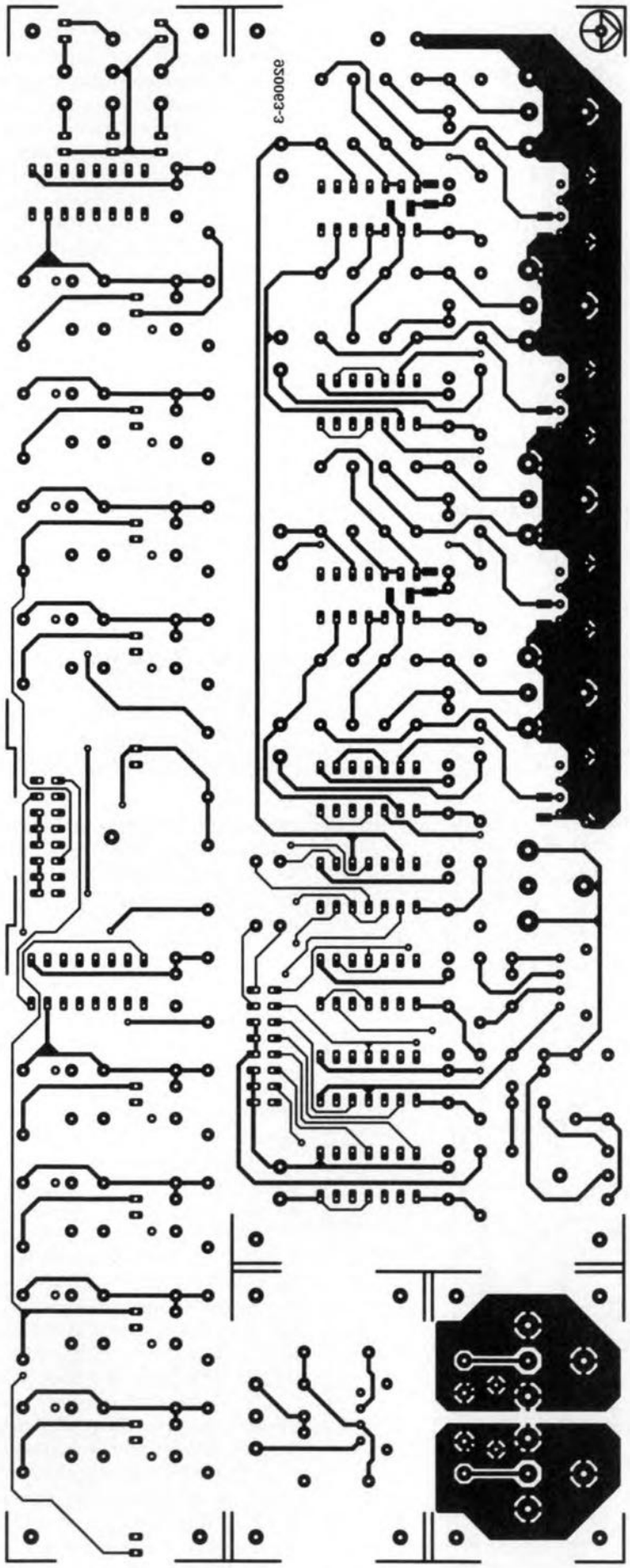


plate running from the rear panel to the power supply connections, that is, only along the analogue section of the board.

First connect the power lines to the boards and then the signal cables. For the mains inlet use a fused type. When all connections are made as shown in Fig. 18, you should have a correctly working converter. ■

PARTS LIST

Resistors:
R1, R5, R9, R13, R20 = 75 Ω
R2, R6, R10. R14 = 100 Ω
R3, R7, R11, R15 = 10 kΩ
R4, R8, R12, R16 = 47 kΩ
R17, R18 = 820 Ω
R19 = 220 Ω
R21 = 8.2 kΩ
R22 = 4.7 Ω
R23–R28 = 10 Ω
R29 = see text
R30, R36 = 1 kΩ
R31–R34, R37–R40 = 1 MΩ
R35, R41 = 470 Ω

Capacitors:
C1, C3, C5, C7, C9, C11 = 100 nF, ceramic
C2, C4, C6, C8 = 100 nF, SMD
C10, C12–C19 = 47 nF, ceramic
C20–C29 = 100 nF (see text)
C31–C34 = 39 pF, SMD

Inductors:
L1–L4 = 47 µH

Semiconductors:
D1–D8 = 1N4148
D9–D16 = LED (in S5–S12?)
D17, D21–D23 = LED, 3 mm, red*
D18, D20 = LED, 3 mm. yellow*
D19 = LED, 3 mm, green*
IC1, IC2 = 74HCU04
IC3–IC6 = 74HC126
IC7, IC8 = 74HC03
IC9–IC12 = TORX173
IC13 = TOTX173
IC14, IC15 = 74HCV4028

Miscellaneous:
K1–K7 = audio socket bus for PCB
K8 = 16-way header
K9 = 16-way flatcable connector for PCB mounting
S1–S4 = mini slide switch, 1 make
S5–S12 = key switch, 1 make
Tr1 = see text (core = LAB G2-3FT12)
PCB Type 920063-3
Front panel foil Type 920063-F

Optional (for optical output):
R42 = 4.7 Ω
R43 = 8.2 kΩ
C30 = 100 nF, ceramic
IC16 = TOTX173

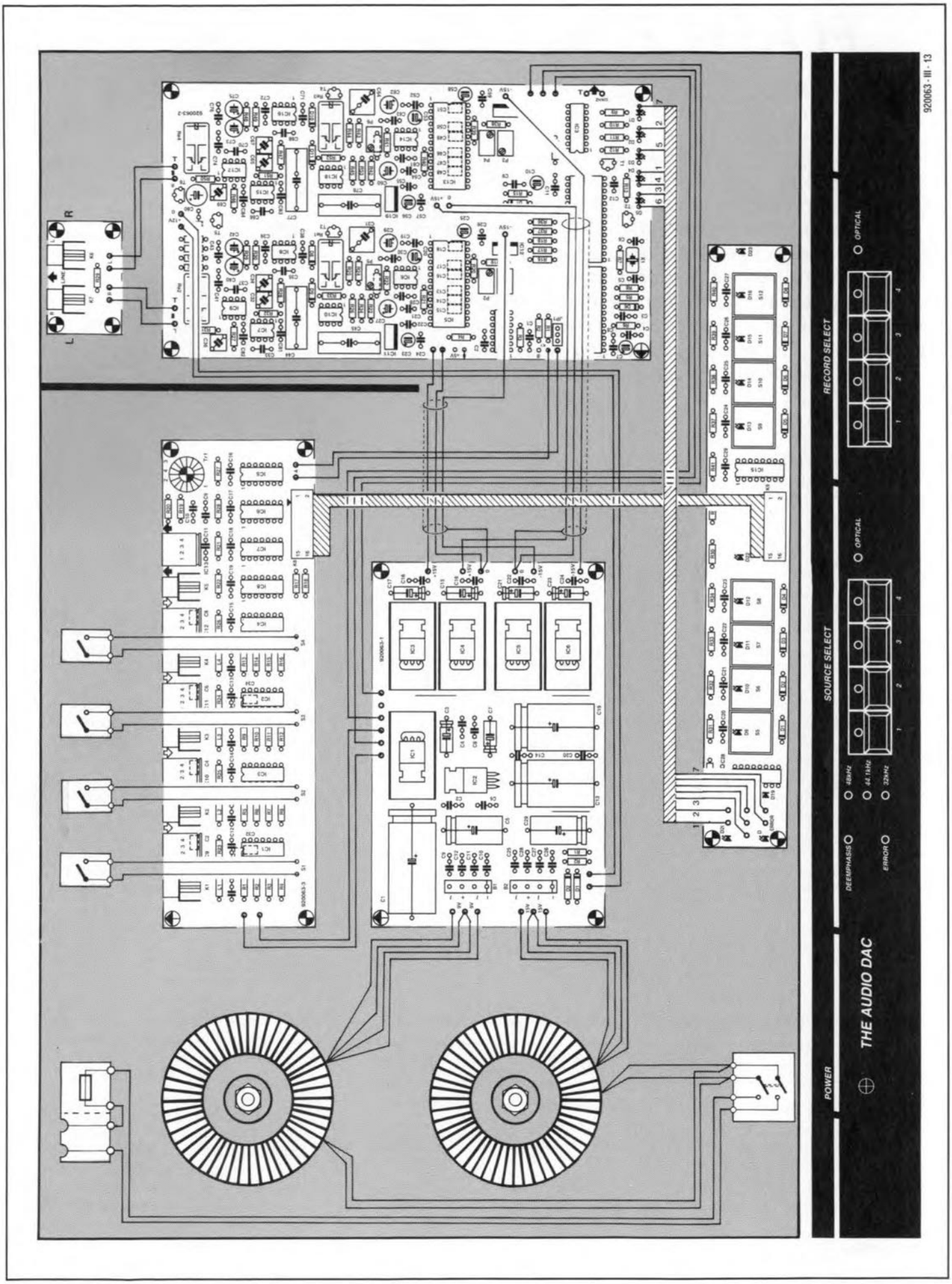
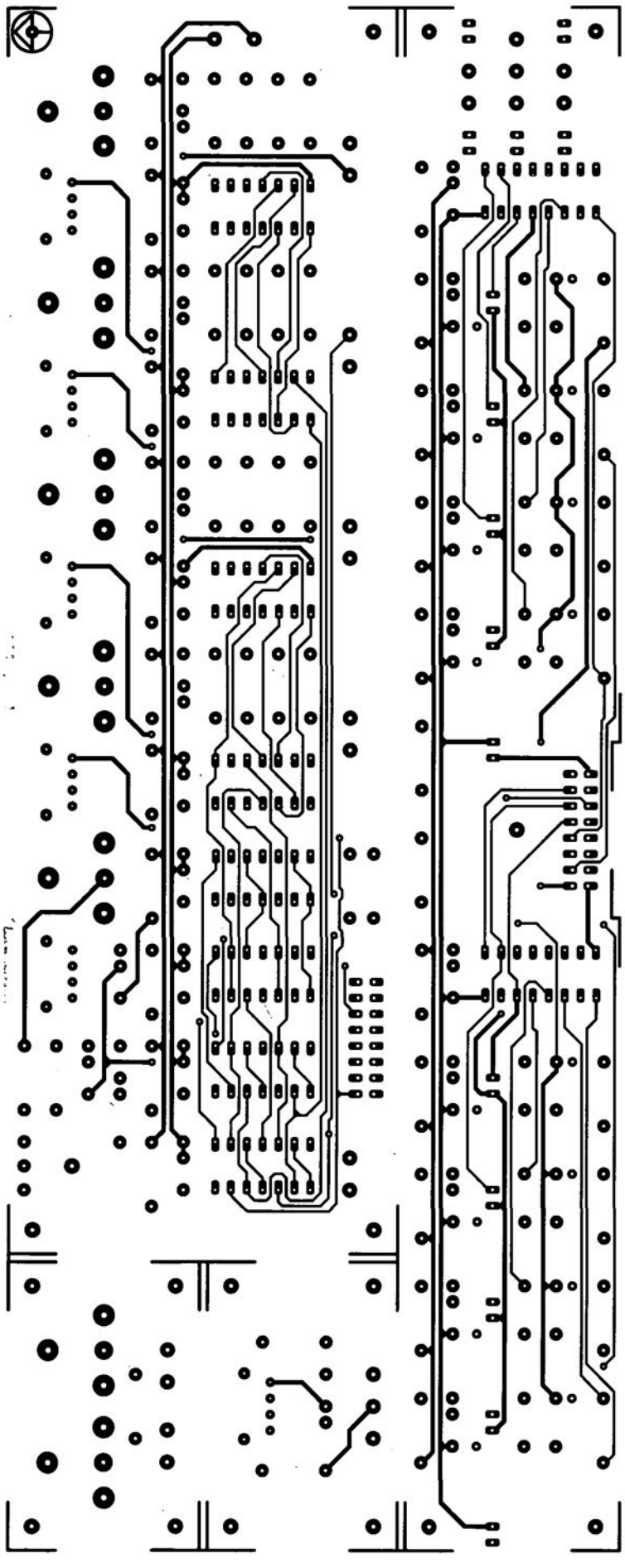


Fig. 18. Wiring and interconnecting diagram of the entire converter, and the suggested front panel (scaled down to half size).



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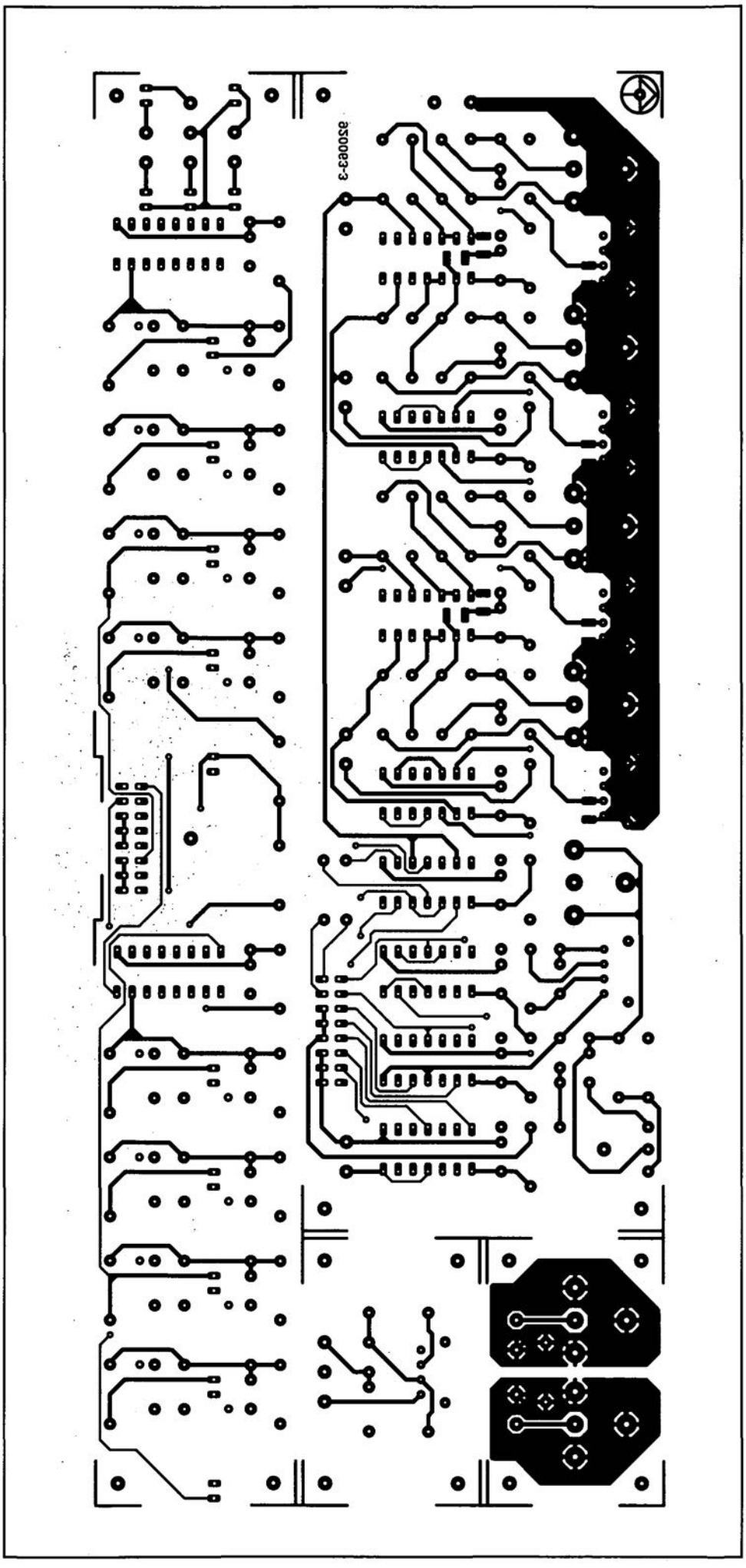

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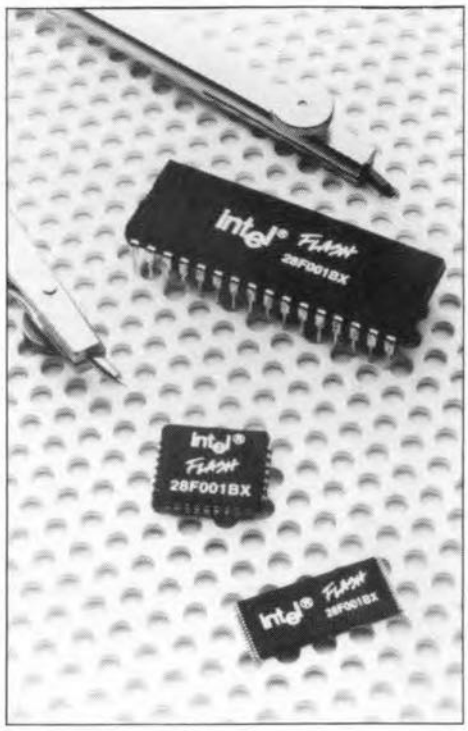
FLASH EPROMS

by T. Scherer

For years nothing much happened in the field of nonvolatile read/write memory components until the EEPROM (Electrically Erasable and Programmable Read Only Memory), followed within a short time by the Flash EPROM, came along. The EEPROM has (not yet) lived up to its early promise, but the Flash EPROM has made a more auspicious start. Already, within two years of its commercial introduction, these devices are readily available and have been used in some commercial equipment. Chip manufacturers say (and, no doubt, hope) that the Flash EPROM has a promising future.



IF you have followed the fortunes of the world's giant semiconductor manufacturers over the past few years, you will know that, because competition in the chip markets is fierce and price wars are rife, the manufacture of memory chips is profitable only if gigantic quantities are produced. The manufacturer who is the first to develop a new technique and who will, therefore, be the first to bring a new generation of chips on the market has a decided advantage.

Currently, this intense rivalry is particularly noticeable in the market for dynamic RAMs (or DRAMs). These devices occupy the largest sector of the market. Since their structure is fairly simple, new techniques can be readily applied to them.

Processors also have a large share of the market, but they have been handled differently for a long time. Manufacturers of these devices created so-called industry standards that have given them a virtual monopoly for most of the 1980s. However, this cosy setup has recently started to show signs of movement. Intel processors are now being cloned or produced under licence (Harris, AMD, Sun). The most exciting development in the past18 months was undoubtedly the Apple-IBM cooperative setup that will ensure a much larger future market share for IBM processors.

What has all this to do with Flash EPROMs you may ask. As we have seen, all semiconductor manufacturers are under pressure. The market for DRAMs is nearing saturation, that for processors is hard to penetrate and it offers only small niches for all other types of chip. Now, as everyone knows, all computers contain at least one ROM or EPROM. However, since the market for computers expands (at present) only slowly, no fortunes can be made (any more) with these memory chips. Furthermore, the techniques for producing current ROMs or EPROMs are not really suitable for further development. However, Flash EPROMs with their different properties have given manufacturers (and users) new opportunities.

A comparison

The fact that Flash EPROMs are electrically erasable alone does not make these devices attractive. After all, EEPROMs are also electrically erasable. The important advantages of Flash EPROMs over the current erasable memory chips, summarized in Table 1, are as follows.

Table 1. Comparison of the various properties of erasable memory cells.

	EPROM	Flash EPROM	EEPROM
relative size of cell	1	1.2–1.3	about 3
programming	by external means	internal	internal
technique	hot electron injection	hot electron injection	tunnel effect
voltage	12.5 V	12 V	5 V
resolution	byte	byte	byte
time taken	<100 µs	<10 µs	5 ms
erasing	by external means	internal	internal
technique	ultraviolet light	tunnel effect	tunnel effect
voltage	12.5 V	12 V	5 V
resolution	whole chip	whole chip or block	byte
time taken	15 min	1 s	5 ms

There is first of all the relative size of the memory cel (transistor) for one bit; this is an important factor, since the density of the chip, that is, bits per unit area, determines the quantity price of the memory. If the area occupied by one cell in a standard EPROM is taken as unity, that in a Flash EPROM is 1.2–1.3, and in an EEPROM about 3. Assuming equal production quantities, that would make the Flash EPROM 20–30% dearer than the standard EPROM. The EEPROM, particularly since its production quantities are much smaller, is much more expensive than these two. At the time of writing (spring 1992), the price of a 1 Mbit Flash EPROM, in quantities of 1000, is £10–£12 each, while that of Intel's 8 Mbit Flash EPROMs (which they call FlashFile™ memories—Type 28F008SA) in quantities of 10 000 varies from £18 for the 120 ns version to £24 for the 85 ns version. Those prices are expected to come down rapidly over the next 12–18 months as more players enter the field.

Another aspect of chip density is that with current 1 µm technology only a certain number of transistors can be deposited on to a given area. At present, most DRAMs, EPROMs and Flash EPROMs are manufactured with a density of 1 Mbit per chip (although Intel introduced an 8 Mbit type in early 1992), and most static RAMs and EEPROMs with a density of 256 Kbit per chip.

Other important factors are the technology and manner of, and time taken for, programming of the memories. Between the three types, there is no difference in resolution: all three types can be programmed byte by byte, although the standard EPROM has the disadvantage that this must be done by an external apparatus. The other two types can be programmed in the equipment in which they are used, since the most important parts of the programming logic have been integrated in them. To make updating of an EPROM at a later date possible, the chip must be fitted

in a socket, which increases manufacturing costs of the equipment in which it is used, ignoring for a moment the extra cost of updating to the user.

There is another aspect connected with programming: EPROMs and Flash EPROMs need an auxiliary voltage of 12 V, otherwise the hot electron injection technology does not work. An EEPROM can operate with the 5 V normally available in the computer: it raises this internally to 18 V. Since the load presented by a Flash EPROM on the 12 V supply is negligible (it draws no more than 30 mA), and most computers have a regulated +12 V line available, there is not likely to be a difficulty. If nevertheless there is no 12 V line available, a tiny voltage converter in a DIL package must be added at a cost of some £2.

It is also interesting to look at the time taken by the programming. A 1 Mbit EPROM needs not less than 15 s, whereas a Flash EPROM is programmed in about 1.5 s. An EEPROM may take minutes!

The technology and manner of erasing is also quite different. An EPROM must be removed from the apparatus in which it is used and be radiated for about 15 minutes with ultraviolet light in a special unit. Flash EPROMs and EEPROMs are electrically erasable and can, therefore, remain in the equipment in which they are used.

As far as the user is concerned, erasing an EEPROM is a normal read operation. Each byte can be erased and re-programmed separately. Since, as already mentioned, this can be a lengthy process, many (large) EEPROMs can be programmed in the so-called page mode at 16 or 32 times the normal speed.

A Flash EPROM is erased in a manner similar to that of an EEPROM, but it is not possible to do this byte by byte, that is, the entire memory or a block or blocks of bytes is erased. Erasure time for a 1 Mbit model is 1–4 s; moreover, before erasure can take place, all bits must be set to '0'.

It is clear that the Flash EPROM looks the most advantageous of the three memories. Its drawback of being erased completely, or in blocks, as compared with the byte-by-byte erasure of an EEPROM is more than made up by the speed with which it is erased (and re-programmed)—whence its name.

Construction and operation

The construction of a Flash EPROM differs not all that much from that of an EPROM. A bit is stored in the floating gate of a discrete MOS transistor—see Fig. 1. The figure also illustrates the manner in which programming and erasing take place. In the *p*-substrate are two n^+ zones that function as the drain and source of a MOSFET. Between the usual gate, that is, the select gate, and the channel there is another gate, the floating gate. The two gates are totally isolated from each other and from the substrate by a layer of silicon oxide. When the memory is erased, the floating gate is uncharged with respect to the source. When the drain is connected as normal to the Vpp line and the transistor is enabled via the select gate, the channel conducts and a logic 1 is available at the source. Programming such a cell requires a negative charge in or at the floating gate, which is not simple to arrange, since that gate is totally isolated.

That difficulty is overcome with the hot electron injection technique. Briefly, this process works as follows. If the cell is aranged as in Fig. 1a, the voltage at the drain and the gate is +12 V, and the source is at earth potential, a channel is formed through which a relatively high current flows. When that happens, a number of so-called hot electrons ensue and these capture other electrons from the substrate material; because of the high electron density, some of these electrons reach the oxide layer between substrate and floating gate. Because of the high potential of the select gate, several electrons actually pass through the substrate and reach the floating gate. The electron cluster so caused at the floating gate remains (according to the manufacturers for at least ten years) even when the +12 V programming voltage is removed. Thus, the floating gate is negative with respect to the source and the memory cell is inhibited.

In an EPROM there would be only one permissible way back: via ultraviolet light. For that reason, EPROMs have a window in the housing of the chip. Ultraviolet light has enough energy to remove the electrons from the floating gate.

A different process, based on the tunnel effect, is used in EEPROMs. Because of this effect, electrons are able to tunnel through a narrow potential barrier that would constitute a forbidden region if the electrons were treated as classical particles. However, quantum mechanics indicates that there is a definite probability of electrons tunnelling through the barrier. This technique, although slower than the injection process, has the advantage of permitting electrical erasing.

The Fowler- Nordheim variant of the tunnelling technique is used for erasing Flash EPROMs. Briefly, it operates as follows. If the memory cell is arranged as in Fig. 1b,

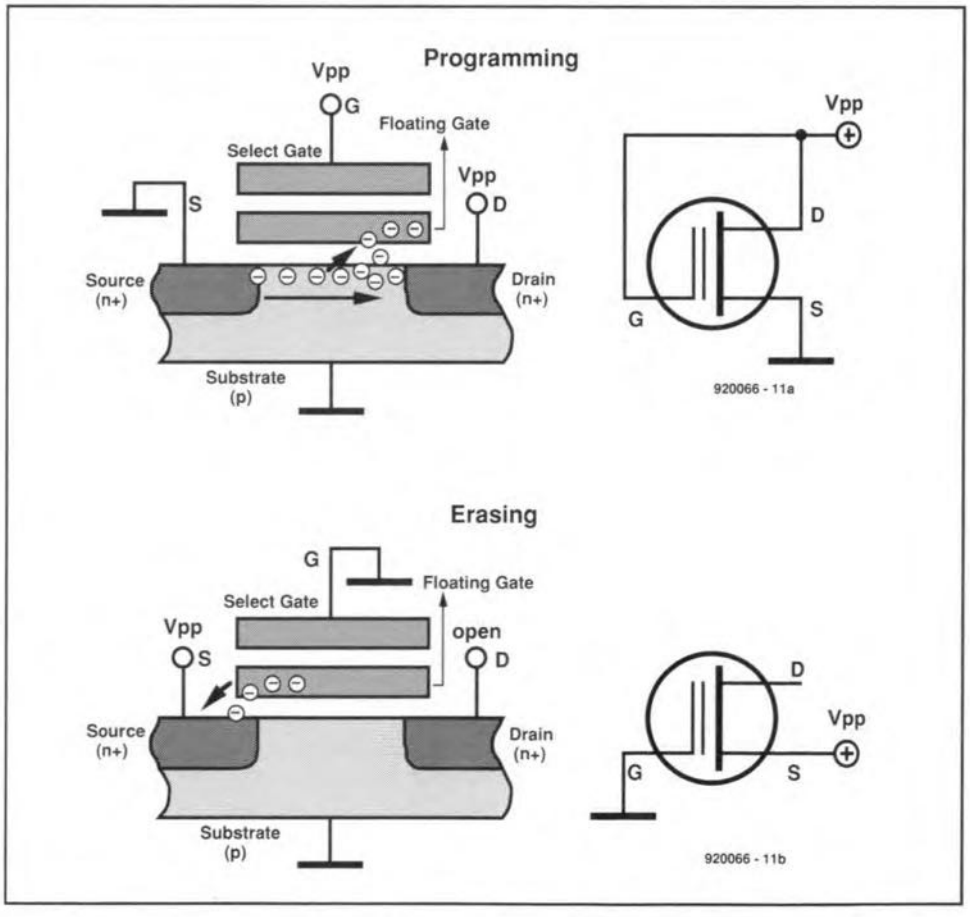


Fig. 1. Schematic representation of the construction and operation of a Flash EPROM.

the source is at +12 V, the drain is at earth potential, and the select gate is open, electrons will tunnel from the floating gate to the source. The floating gate will attain the same potential as the source so that the transistor is on, that is, erased.

The erasing process in a Flash EPROM is even slower than that in an EEPROM, because it happens at a lower internal potential. It is, however, kinder on the oxide layer and altogether more reliable. A Flash EPROM can therefore be cycled considerably more times (up to 100 000) than an EEPROM (a few thousand). The real difference between an EPROM and a Flash EPROM lies in the much thinner oxide layer between substrate and floating gate in the latter. Moreover, the architecture of the floating gate of a Flash EPROM is optimized for the tunnelling process, resulting in shorter write/erase times.

Types and properties

To prevent spurious voltage levels or voltage peaks, occurring when the apparatus in which a Flash EPROM is used is switched on or off, from modifying the stored information, the chip is provided with logic that enables the erasing or programming mode only if well-defined combinations of levels exist in a fixed sequence at the control pins of the chip. The algorithms needed for the erasing or programming are available from the manufacturers of the memory.

From a reliability consideration, it is important to know how a Flash EPROM behaves after a great many erase/write cycles. Manufacturers normally guarantee no fewer than 10 000, but Flash EPROMs usually still function properly after 100 000 cycles. It is interesting to note that with increasing cycling not one or more bytes become useless (which may, of course, happen once in a while), but that the erase/write times increase. Figure 2 shows the relevant correlations for a 2 Mbit (512 Kbyte capacity) Type 28F020 Flash EPROM from Intel.

Flash EPROMs are normally housed in 32-pin DIL cases (see Fig. 3) which makes it possible to substitute them for pin compatible EPROMs or static RAMs. There are other housings available, for instance, the 32-lead TSOP, which has the advantage of being very shallow (thickness 1.25 mm). The TSOP version is also available with a different pinout: standard E type, modified F type. As shown in Fig. 4, mixing these two types can simplify the layout of a printed circuit board greatly.

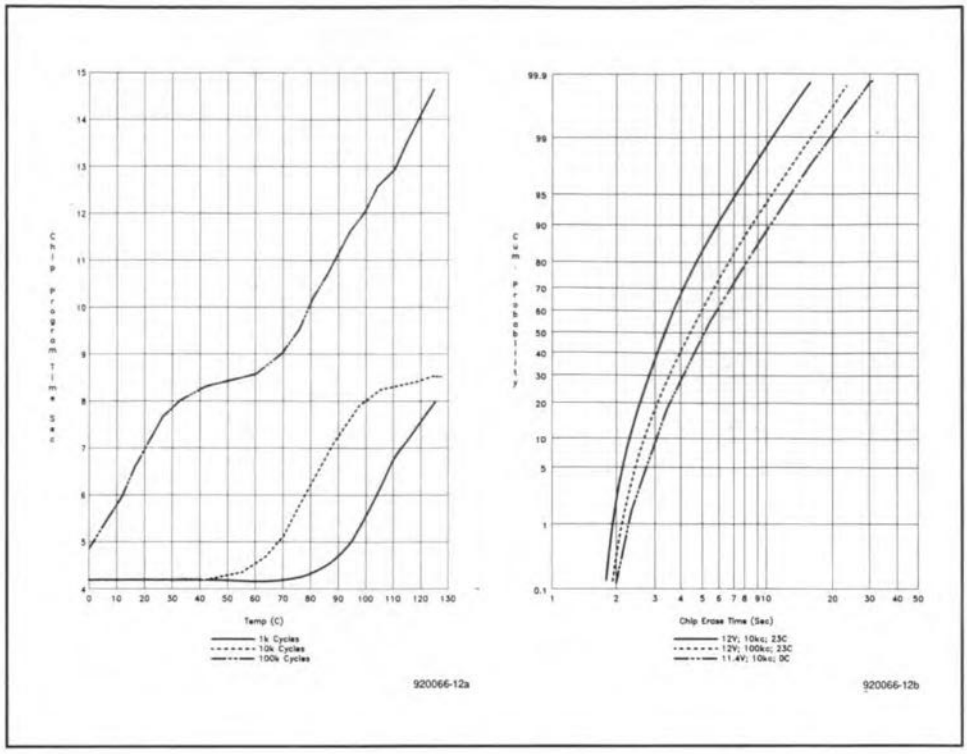


Fig. 2. Time taken by programming and erasing of Flash EPROMs as a function of the number of times the devices have been cycled.

At the time of writing (spring 1992), standard Flash EPROMs are available with capacities ranging from 256 Kbit to 8 Mbit. Like EPROMs they are organized in bytes (8-bit data). Indications are that within 18–24 months there will be 16 Mbit versions (2 Mbyte).

There are also special types available, for example, the Blocked Flash EPROM that contains a number of individually erasable blocks, such as Intel's 1 Mbit Type 28F001BX in which block 1 has a capacity of 8 Kbyte; blocks 2 and 3 one of 4 Kbyte; and block 4 one of 112 Kbyte. This type is particularly aimed at IBM compatible PCs, where block 1 would function as boot loader, blocks 2 and 3 as data store and block 4 as BIOS.

Finally, there are Flash EPROMs that function as SIMMs (Single Inline Memory Modules) or are used in memory cards with memories from 1 Mbyte up to 20 Mbyte.

Applications

When a Type 28F001BX is used in a PC, the BIOS of that computer can be updated at any time without the need for opening it. All the manufacturer has to do is to send his customers a diskette with the relevant program. Since this is a good sales point, many

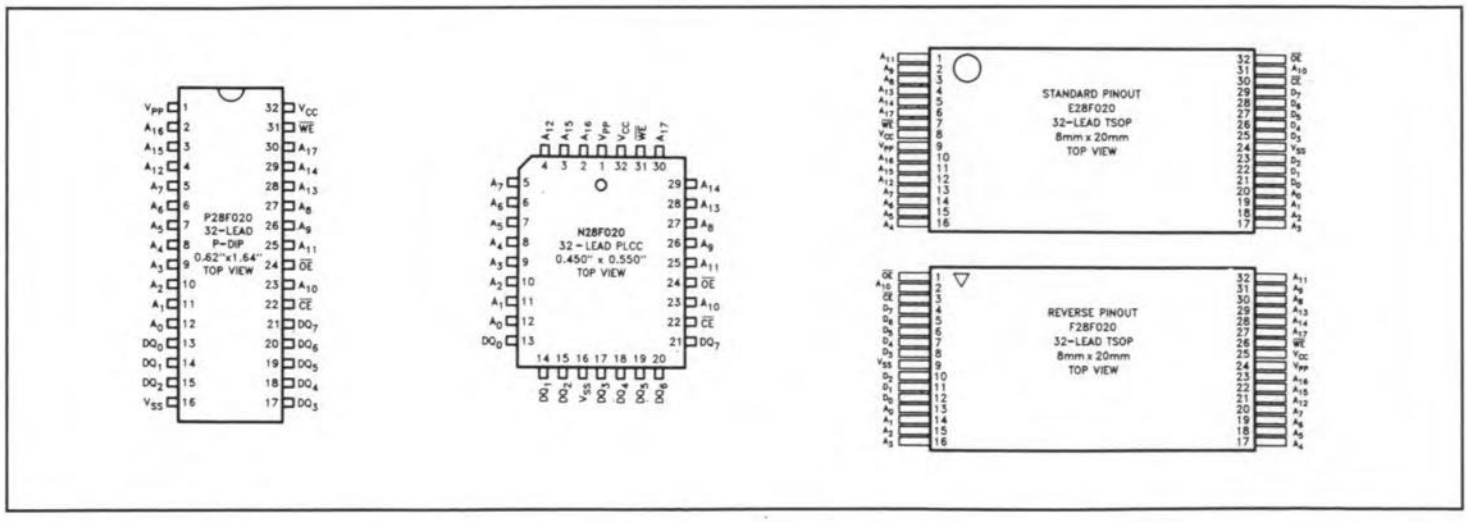


Fig. 3. Housings and pinouts of a 2 Mbit Flash EPROM (Intel's Type 28F020).

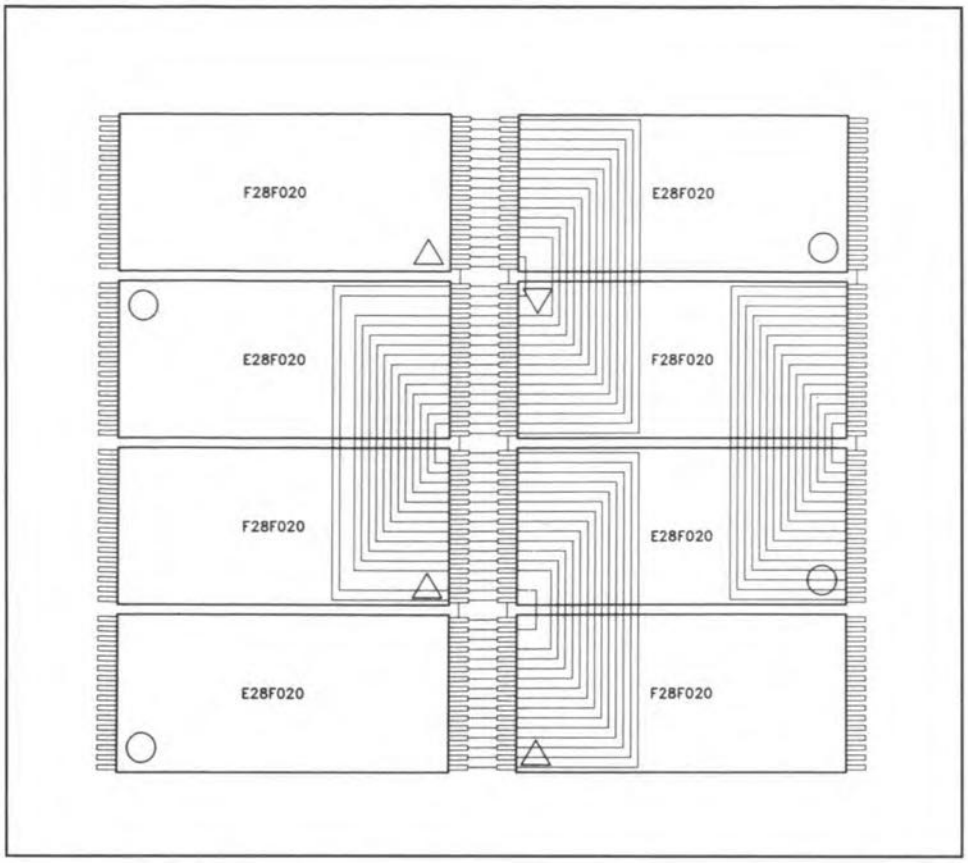


Fig. 4. The use of Flash EPROMs with mutually different pinouts simplifies the design of a printed circuit board greatly.

PCs have already been equippped with this Flash EPROM.

In Notebook computers, it is possible to incorporate the entire operating system in Flash EPROMs. The Notebook can then be updated as and when required. Manufacturers of operating systems such as Digital Research and Microsoft already offer their DOS in EPROM versions, and are now working on commercial operating systems using Flash EPROMs.

Flash EPROMs are also of great interest for industrial control equipment; they would enable such equipment to be reprogrammed without this having to be opened, which would reduce servicing costs.

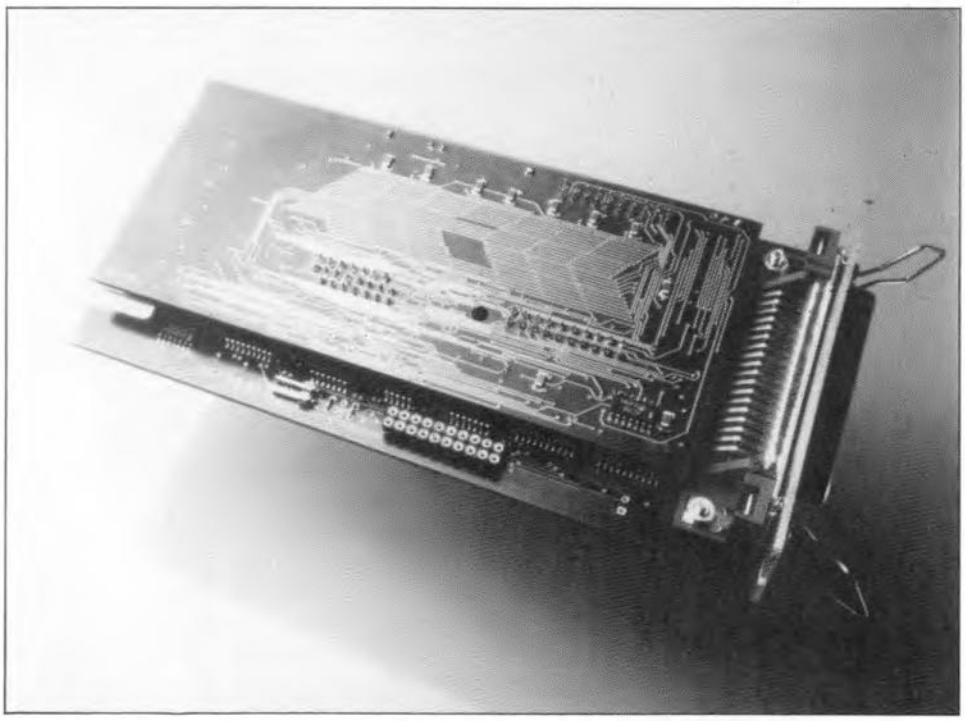


Fig. 5. The Mustang accelerator card from Pyramid Computer, intended primarily as a retrofit for HP Laserjet printers, uses Intel's Type 28F020 Flash EPROM.

Even more fascinating is the use of Flash EPROMs in apparatus whose operation depends on integrated software, such as modems and printers whose control software is normally contained in ROMs or EPROMs. With today's rapidly moving technology, such equipment is hopelessly out of date after about three years from purchase. This is particularly true of laser printers. Updated versions of page description languages, such as Adobe's PostScript or Hewlett Packard's PCL, appear at fairly short intervals. Many users would love to have a laser printer that can be updated easily. To meet that wish, the German firm Pyramid Computer has brought out an accelator card (see Fig. 5) for laser printers that contains a fast RISC (Reduced Instruction Set Coding) processor and a 2 Mbyte Flash EPROM. The latter device stores an easily updatable PostScript clone and the necessary fonts.

Manufacturers are also working on the replacement of the hard disk drive in laptop and notebook computers by a Flash EPROM, which would mean a reduction in current consumption (by a factor of 3–5) as well as in weight and size. Furthermore, the computer's reliability would increase tenfold.

The 16 Mbit chip, which is not far off, will enable the production of memory cards in the form of a 3.5 in diskette (or even smaller) with a capacity of 50 Mbyte. As yet, there are some drawbacks. First of all, the write speed of a current Flash EPROM is only about double that of an HD diskette, that is, roughtly ten times slower than a modern hard disk. Another one is the incompatibility with systems like MS-DOS™. However, Microsoft has already produced a DOS using Intel's FlashFile™ memory architecture.

Today's graphics oriented operating systems such as Microsoft Windows™, IBM's OS/2 and Apple's Finder may slowly but inexorably be replaced by solid-state architecture.

For the present, although technically Flash EPROMs can already replace diskettes, their price has to come down substantially before they can do so commercially. After all, 1 Mbyte on diskette today costs pence rather than pounds or just over a dollar. ■

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Thin Small Outline Package Data Book (296514-001), Intel

Mustang Accelerator Card for Laser Printers, Data Sheet, Pyramid

PASCAL ROUTINES FOR MULTIFUNCTION MEASUREMENT CARD

This article presents a collection of Turbo Pascal routines that should assist constructors of the Multifunction Measurement Card for PCs in writing their own application software.

Design by J. Ruiters

PART of the success of the Multifunction Measurement Card publication (Ref. 1) must be due to the application software developed for it, for instance, that for the multi-channel voltmeter/frequency meter, and the computer-controlled weather station modules. This application software is remarkable because they allow you to set up, say, an advanced data acquisition system built around a PC, without much knowledge of IBM PC hardware and programming languages such as C and Pascal.

None the less, 'low-level' programming remains of interest to many enthusiastic users of the measurement card, witness the large number of requests we received for hints on programming, for example, the ADC (analogue-to-digital converter) contained on the card. These requests are honoured by the present article, which presents software that shows how the various I/O protocols, A-D functions and frequency measurement algorithms may be put to use. In fact, we have thrown together, in a kind of library, a large number of elementary routines for the control of the measurement card. Both 'die-hard' programmers and beginners should find this library, written in Turbo Pascal 5.5, of great use in the development of their own application programs.

A typical feature of today's electronics is that hardware and software are efficiently combined to achieve target specifications. Depending on certain requirements (cost, speed, flexibility and available firmware), a system designer must consciously decide to implement a function either in hardware or in software. Such considerations have also existed in the early design stages of the measurement card. The large computing power of the IBM PC was the factor that made us decide to choose hardware (MSI and LSI building blocks) only for those applications that are impossible, or very difficult, to realize with the aid of software. This decision does have consequences: on the one hand, it means inexpensive hardware and a high degree of flexibility; on the other, a fairly complex piece of programming. Fortunately, the last point is not a problem any more thanks to the availability of the software we present here. This software is available on a diskette with order code ESS 1751.

The unit PMEASURE.PAS, or the compiled version of it, PMEASURE.TPU, con-

```
$300        BASE_IO_ADDRESS: Possible values are $300 (JP1=A) and $310 (JP1=B).
10000000    RefFreq        : Frequency meter (crystal-) reference in Hz.
10          MaximumGateTime: Typical 410 seconds (10 Mhz referency frequency).
2.5         RefVolt        : ADC full-scale voltage
2           IRQ            : Hardware interrupt (Possible values: 2 .. 7)
```

920067-11

Fig. 1. Parameters in the configuration file ADCF.CFG may be edited with any ASCII-compatible wordprocessor.

tains, among others, functions for PPI initialization, multiplexer control, A-D conversion, digital I/O and pulse time and frequency measurement. These and all other procedures and functions that are declared in the unit may be called directly from the associated source file using the command 'uses PMEASURE'.

Before discussing the programming routines, we take the opportunity to refresh your memory: the 'specs' box of the measurement card is repeated on this page. Also, we suggest to once more go through the whole article on the measurement card.

Pascal unit

The effect of a unit function is nearly always apparent from the name: e.g., SelectFreqChannel(Channel:ZeroToSeven) connects channel number 'Channel' of multiplexer IC22 to the frequency meter. Where necessary, the declared constants, variables, procedures and functions are described by a few words of 'comment'. This comment obviates the need of a detailed description to be rendered here: for more information, refer to the source code.

The peripheral interfaces (PPIs), IC13 and IC14, are read from and written to via the procedures ReadPPI and WritePPI respectively. Although these are really very basic routines, they form the nucleus of the card control system. ReadPPI and WritePPI are, therefore, frequently called by other procedures and functions. Among the 'users' are: InvertInput, CounterValue, GetCurrentAnalogChannel, SelectRatioIO and StartEventCounter.

During the initialization phase, PMEASURE automatically loads the hardware configuration file ADCF.CFG, and the presence of the measurement card at the set base address is checked. If the card is found, the PPIs are automatically initialized at the end of the test (see the InitPPI routine in PMEASURE.PAS). This is an important event, because it takes place **before** the control program proper (i.e., your software) is started. The Boolean variable 'HardwareFound' thus allows software to decide to go on (card found) or not (card not found).

```
function ADC(var Overflow:boolean):word;
(*************************************)

{-ADC samples the analogue input and returns the previous 12 bit
  conversion result through ADC.
  The high order byte must be read first because reading the low
  order byte starts the next conversion cycle.}

var
  X:word;

begin (* ADC *)
  if not HardwareFound
    then
      begin
        ADC:=2048;
        Overflow:=false;
      end
    else
      begin
        X:=portw[BIO_Address+1];
        X:=swap(X);
        if (X=$FFF) OR (X=$000)
        then Overflow:=true
        else Overflow:=false;
        ADC:=X;
      end;
end;  (* ADC *)
```

920067-12

Fig. 2. This ADC function is one of the many routines contained in PMEASURE.PAS.

MULTIFUNCTION MEASUREMENT CARD FOR PCs

MAIN SPECIFICATIONS

DC Voltmeter
Range: 0.1 V to 300 V
Inputs: eight
A-D converter: 12 bits, 3 µs, 0 to 5 V

Frequency meter
Range: 0.0025 Hz to 10 MHz
Inputs: eight (TTL)
Max. error: 0.0001%
Accuracy: 6 digits

Pulse time meter
Range: 0 to 400 s
Resolution: 0.1 µs
Adjustable measurement level

Event counter
Range: 32 bits
Max. frequency: 10 MHz
Adjustable trigger edge

Time related measurements

PMEASURE makes the best possible use of the available hardware facilities. Hence, the pulse time and frequency measurements are fully interrupt-driven. The IRQ input used in the PC needs to be set in hardware as well as in software. On the measurement card, one of the jumpers JP2 to JP7 is fitted in the X-row. Make sure to use a free IRQ line (usually IRQ2), and check that jumper JP8 is in position E. As to the software setting, the IRQ line must be identified in line 5 of the configuration file (see Fig. 1).

Depending on the type of measurement, a measurement cycle starts with a call to StartPulseTimeConversion or StartFrequencyConversion. The associated interrupt routine, HardwareIntHandler, starts automatically the moment hardware flag EOC-F is actuated. This happens at the end of each (sub-) conversion. By virtue of the interrupt procedure, the entire measurement remains fully transparent to the main program. Yet, the measurement results are simple to call up by subsequently reading the records called PulseTime and Frequency.

A second interrupt routine plays an important role when frequency measurement is used. A routine called TimeIntHandler monitors the time taken by the second phase of the measurement (f_m'), and verifies this time against the maximum conversion time calculated during the test measurement. When the time limit is exceeded, this is taken to mean that the fre-

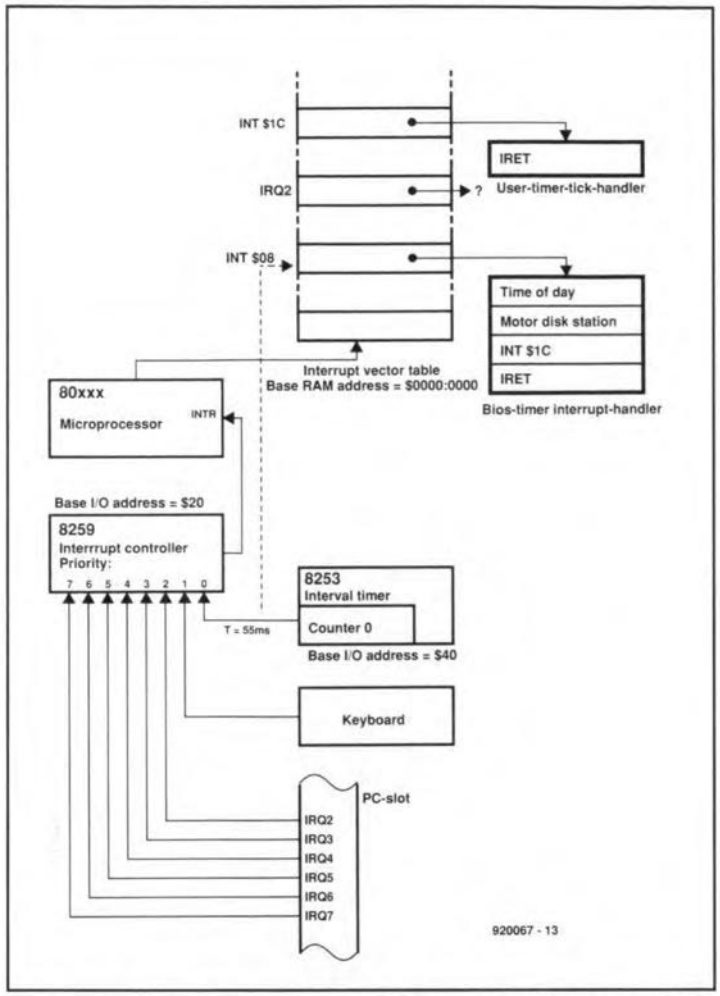


Fig. 3. Schematic representation of the standard PC interrupt network.

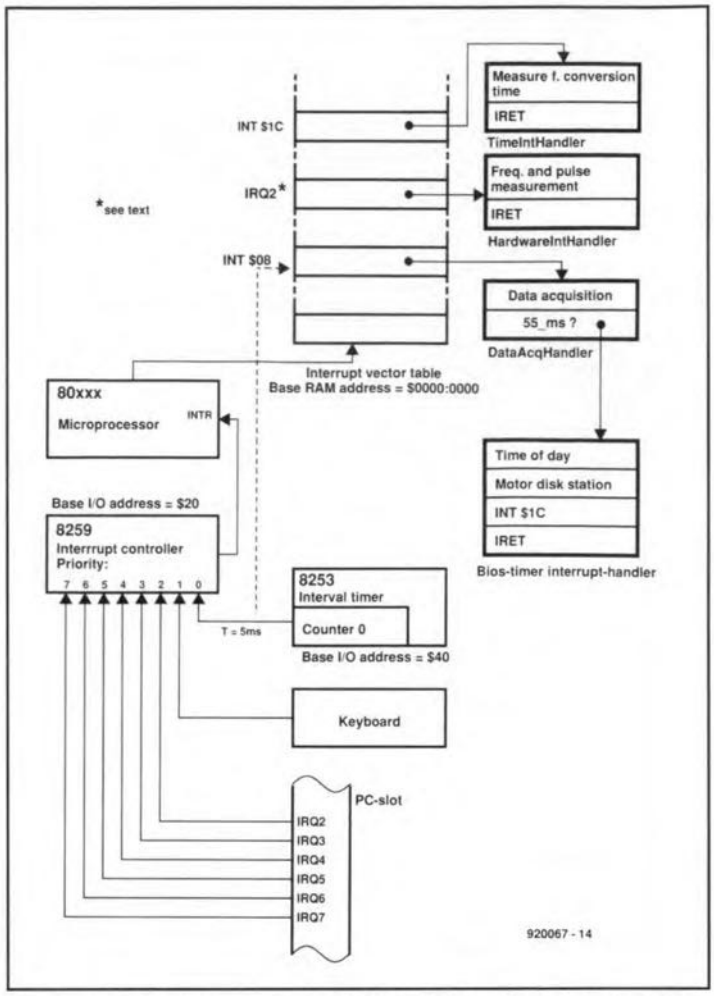


Fig. 4. As Fig. 3, but with the PMEASURE routines installed. Note the way the BIOS interrupt handler is given new parameters.

quency of the input signal has gone down so far that the test measurement and the set scale factor are no longer representative. To prevent frequency measurements taking up too much time, TimeIntHandler breaks off the current conversion, and starts a new test measurement. The procedure itself makes use of the PC-user-timer-tick-interrupt ($1C), and is therefore actuated every 55 ms.

DC measurements

The function 'ADC' (Fig. 2) allows a 12-bit binary representation of an analogue input voltage to be acquired. The important thing about ADC is that the A-to-D conversion operations are not started until at the end of the function. This means that the value of ADC is related to the previous conversion, and, inevitably, that the first conversion result is meaningless.

Functions SelectAnalogChannel and SelectRatioIO are intended for the control of the input multiplexer (IC_{10}), and the setting of the stepped attenuator (IC_{12}), respectively.

Since the analogue circuitry on the measurement card is designed for direct voltages, it would seem logical to base each measurement result on an average obtained from a number of samples. This so-called stochastic measurement enables noise pulses to be suppressed efficiently.

The ADC function is called from a periodic interrupt routine to make sure that the d.c. measurements can run in the background, just as the frequency and pulse time measurements. The TimeIntHandler is not suitable to control the timing: being started 'only' 18.2 times a second, it is too slow, and would cause a stochastic calculation using, say, 100 samples, to take far too long. A different data acquisition routine was, therefore, devised, to make sure that the selected input can be sampled at 200 Hz. This sounds simpler than it is, because the only periodic interrupt that is still available in the IBM PC is the user-timer-tick, which runs at a rate of 55 ms. Drastic measures are required to make sure that a much shorter interrupt period is available. This is achieved by replacing the BIOS timer interrupt handler (interrupt $08) by the data acquisition procedure 'DataAcqHandler'. After having reprogrammed the system clock prescaler, the handler is called at the desired rate, i.e., every 5 ms. The new scale factor (divisor) is supplied by ReProgTimer, while UnDoReProgTimer restores the default factor later.

To make sure that the real-time clock and the diskette station motors continue to function normally, the original BIOS timer interrupt handler (and, with it, interrupt $1C) is started with the original frequency, and from the DataAcqHandler. For clarity's sake, the usual interrupt network is drawn in Fig. 3, while Fig. 4 shows the configuration with the new interrupt routines installed.

Get cracking

Apart from the Pascal library, diskette ESS 1751 also contains an example program, PMDEMO.PAS. This program serves to demonstrate how the interrupt procedures are installed and removed, and show you how to get access to the measurement results. Incidentally, a nice feature of PMDEMO is that it makes use of the AutoScan mode. In this mode, the interrupt routines ensure that all channels defined in FChanScan and VChanScan are measured one by one.

As a matter of course, PMEASURE may be extended or adapted to meet your requirements. This will cause few problems as long as you keep to the rules of proper programming. Take care, however, with the special rules that apply to stack use and DOS interrupts, since these have many pitfalls in store for the 'unwary'. Once bitten, twice shy! ■

Reference:

1. "Multifunction measurement card for PCs", *Elektor Electronics* January and February 1991.

8051/8032 ASSEMBLER COURSE

PART 7: SERIAL INTERFACE PROGRAMMING

By Dr. M. Ohsmann

Perhaps unwittingly, you have been using the serial communication features of the 8051 or 8032, and the supporting routines contained in the system monitor, EMON51, ever since the 80C32 single-board computer (our 'course hardware') wrote its first 'welcome' message on your terminal. In this course instalment we will explore the not-so-simple operation of the serial interface with an aim to grasp the way it is programmed.

8051 serial interface

The serial interface contained in the 8051 family of microcontrollers is the most complex 'on-chip peripheral'. Hence, this instalment is probably the most difficult of all in the course, and should be studied thoroughly. This effort is also required, unfortunately, on part of those of you who intend to implement only very basic serial communication on a 8051-based controller system, and even if a range of examples of software building blocks is available in the system monitor, EMON51.

The serial interface can operate in a number of modes, some of which are of little interest here because they serve to implement 8051 network systems. We will concentrate on the simplest mode of operation: sending and receiving 8-bit data (asynchronously) with one start bit, one stop bit, and no parity. This mode allows the 80C32 SBC to communicate with a PC, as well as to exchange MIDI data (MIDI = musical instrument digital interface).

The special function register (SFR) identified as SCON (Serial CONtrol) at address 098H serves to control the on-chip serial interface, and determine its mode of operation. The function of the bits contained in the SCON register are shown in Fig. 44. The mode we require can be set by programming SM0=0 and SM1=1. As shown in Fig. 44, this is mode 1, in which bit SM2 may be used to signal transmission errors. The function of the remaining bits in SCON will be reverted to below.

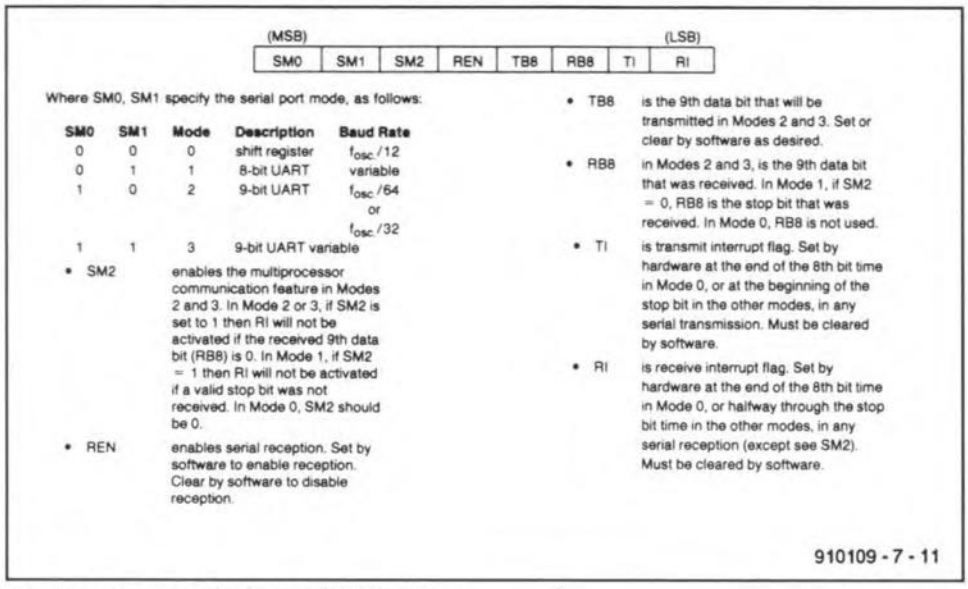


Fig. 44. Overview of SFR SCON bit functions.

The transmit and receive buffers

Inside the 8051, serial data is transmitted and received with the aid of a shift register. Bits are transmitted by first loading them, in parallel, into the shift register, and then shifting them out, one by one, at the programmed bit rate (baudrate). In receive mode, the bits are gathered, one by one, into the shift register, and are read out in parallel when all are in. In the 8051, the SFR called SBUF (at address 099H) is used as a receive and data buffer. It has the 'quasi-double' functions of a 'receive' buffer, and a 'data' buffer, the relevant function being selected by read or write operations on SBUF, respectively.

The transmit and receive functions are supported by their own shift registers, so that it is actually possible to transmit and receive simultaneously (full-duplex operation).

Configurations and functions

Figure 45 shows the internal structure of the serial interface contained in the 8051 family of microcontrollers. The baudrate generator is shown in the upper left-hand corner of the diagram. The overflow pulses produced by Timer 1 or Timer 2 (8052 only) may be used to clock the shift registers. The switch marked 'SMOD2' controls a divide-by-two scaler. The switches RCLK and TCLK (8032 and 8052 only!) select the receive clock and transmit clock respectively. The clock signals so obtained are divided by 16 before they are fed to the TX-CONTROL and RX-CONTROL sections.

The transmit control clocks and loads the transmit shift register, whose output is connected to the TXD terminal (pin 11) of the 8051 (upper part of the drawing). From the internal databus of the 8051, the databits are fed in parallel into the SBUF register. The 'zero-detector' finds out if all bits have been transmitted. If so, this is signalled to the transmit control section, which in return is capable of generating a serial port interrupt, TI. When this happens, the TI bit (SCON.1) is set.

The lower part of Fig. 45 shows the receive control section. Serial databits received on pin 10 (RXD) of the 8051 are gathered in the receiver shift register. The data simultaneously arrive in the 1-to-0 transition detector, which serves to recognize the start bit in the serial datastream, and to synchronize the receiver clock with the incoming bits. Data reception starts on a high-to-low level transition (falling pulse edge) at the RXD input, i.e., a start bit at pin 10 of the 8051. The incoming bits are clocked into the shift register. The last bit that is read is the stop bit (the receiver shift register has a width of 9 bits). Next, SBUF is loaded with the eight received bits, and the 'receiver full' bit is set (SCON.0=RI). This sequence does **not** take place, however, in the following two cases:

1). When RI is already set, which means that previously received data was not fetched.
2). When SM2=1, and the stop bit did not have the value '1'. Thus, by programming SM2=1, you can prevent bytes with a framing error (wrong stop bit) getting through.

The level of the RI bit thus allows us to check if a received byte is held ready in

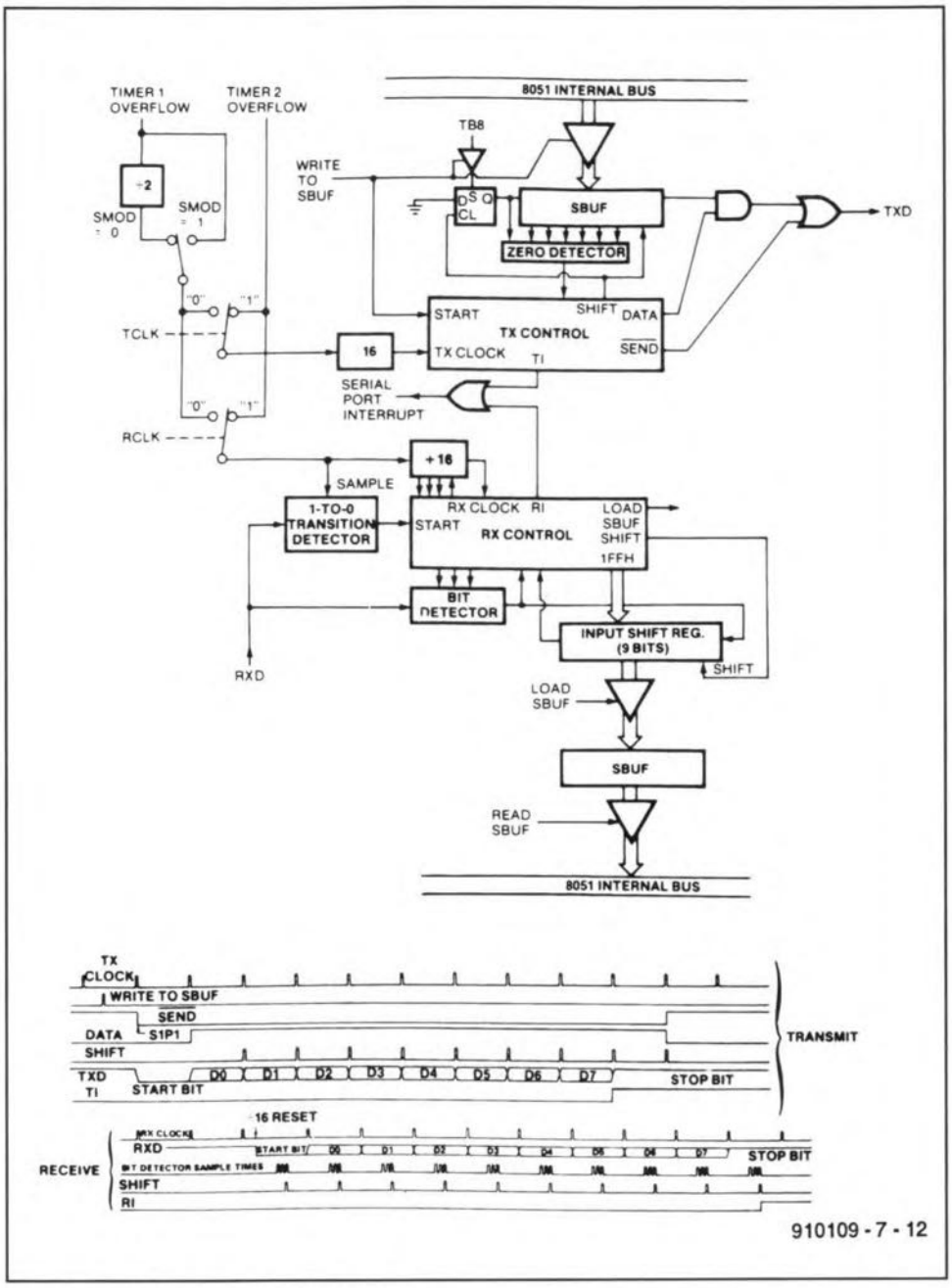


Fig. 45. 8051 serial interface architecture.

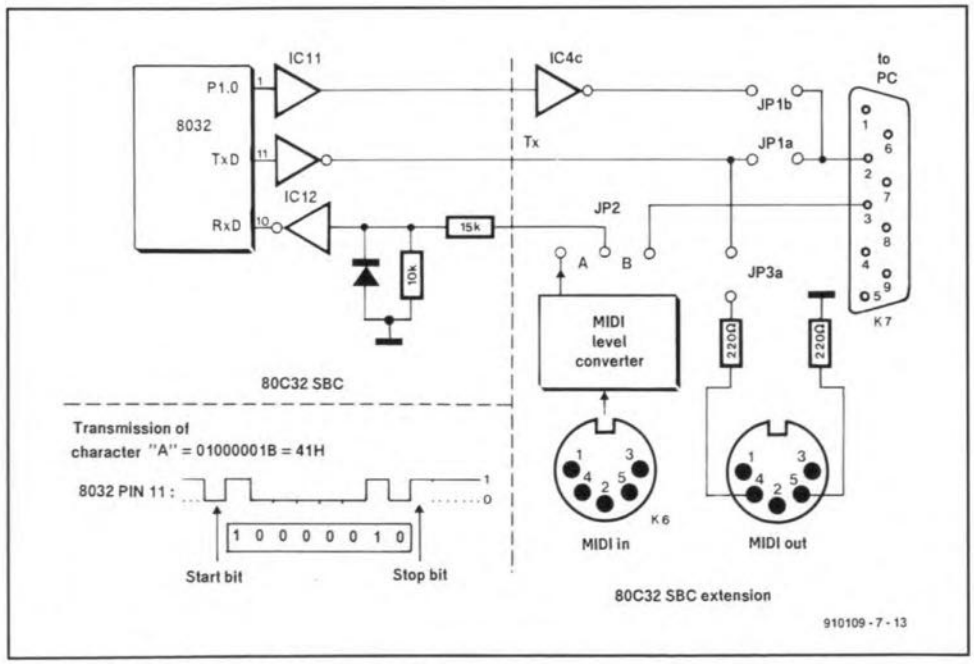
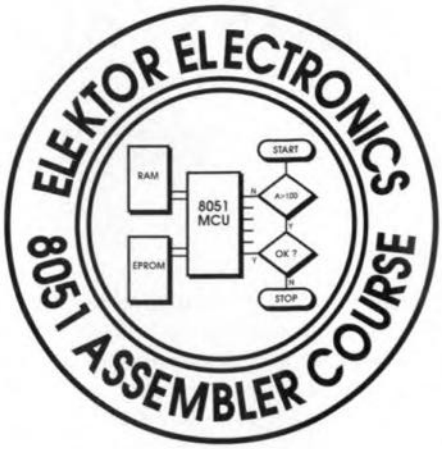


Fig. 46. V24 interface (80C32 single-board computer and extension board).



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What you need to follow this course:

- **a 8032/8052AH-BASIC single board computer as described in Elektor Electronics May 1991. The preferred CPU is a 8051 or 80C32. Alternatively, any other MCS52-based microcontroller system (but read part 1 of the course);**
- **a course diskette (IBM: order code ESS 1661; Atari: order code ESS 1681) containing programming examples, hex file conversion utilities, and an assembler;**
- **a monitor EPROM (order code ESS 6091);**
- **an IBM PC or compatible operating under MS-DOS, or an Atari ST with a monochrome display.**

Appeared so far:

Part 1: Introduction (February 1992)
Part 2: First 8051 instructions (March 1992)
Part 3: Hardware extensions for 80C32 SBC (April 1992)
Part 4: Flags, bit addressing, PSW, conditional jumps, logic operators (June 1992)
Part 5: Arithmetic instructions (July 1992)
Part 6: Analogue signal processing and stack management (September 1992)

SBUF. If so, the byte can be fetched (read) for further processing.

The two interrupt events, TI (transmitter interrupt) and RI (receiver interrupt) actually generate only one interrupt, of which the cause (data transmitted, or data received) must be established by the interrupt software. The serial interface only generates interrupts when bit IE.4 in the interrupt enable register is set (see Part 6 of this course).

Details of the TXD and RXD wiring and external circuitry on the 80C32 SBC

and the extension board (Part 3) are shown in Fig. 46. The diagram shows how the various jumpers enable the 8051 serial interface to be connected to a PC (via the 9-way sub-D connector) or a MIDI compatible instrument.

EMON51 communication

Studying a worked out example is probably the best way to familiarize oneself with the programming of the serial interface. Let us look at the listing in Fig. 47. This program is a series of subroutines contained in EMON51 relevant to communication via the serial interface, 'stitched together' to show how you can make use of them for your own programming work. Each of the points to be observed in programming the serial interface will be discussed below, with reference to certain parts of the listing. Note that this program is not contained on your course disk.

Baudrate generator

We wish to use mode 1 of the serial interface. In this mode, the baudrate is determined either by Timer1 or Timer2. Remember, Timer2 is not available if you use a 8031 or 8051 (i.e., TCLK=0 and RCLCK=0 in Fig. 45). In the interest of software compatibility we will, therefore, set the baudrate with the aid of Timer1. The 'counter overflow' pulses produced by this timer are fed to the transmit and receive controls. To ensure a continuous supply of pulses, the timer is operated in mode 2, i.e., as an 8-bit clock generator with automatic reload. In this way, the timer is capable of producing an overflow every *n* microseconds on the basis of the 1-MHz internal clock (quartz oscillator frequency 12 MHz), where *n* is a whole number between 2 and 256. Additionally, we can switch on the divide-by-two scaler by setting the SMOD bit (SFR PCON bit 7). The final baudrate clock is arrived at by dividing the clock signal by 16. If SMOD=1, we get:

Baudrate = (overflow rate Timer1)/16

alternatively, if SMOD=0,

Baudrate = (overflow rate Timer1)/32

In the system monitor software, EMON51, the following is done to obtain a baudrate of about 4,800. First, Timer1 is set to auto-preload mode with internal clock (here: 1 MHz). See line 22 in Fig. 47. The preload value is 243 (lines 4, 24 and 25), which causes Timer1 to divide by (256–243) = 13. SMOD is set to '1' in line 21 to disable the ÷2 scaler. Thus, the baudrate becomes

1 MHz/13/16 = 4,807.6923 bits/s

That is not exactly 4,800 baud, but sufficiently accurate for our application.

After being preloaded and set to the desired mode, Timer1 is switched on by setting TCON bit 6 (line 26). The baudrate generator is now running.

As an aside, Timer2 contained in the 8052 and 8032 may, of course, also be used as the baudrate generator. This can be achieved by setting bits TCLK and RCLK in the Timer2 control register, T2CON. Since T2CON contains the value 00H after a reset, the 8052 always starts with Timer1 as the baudrate generator (which ensures that programs written for the 8051 run on a 8052 too!).

The standardized baudrates (1200, 2400, 4800, etc.) can be achieved exactly by using a crystal clock of 11.0592 MHz rather than 12 MHz. However, a processor cycle then takes 0.9044225 µs rather than 1 µs exactly. Obviously, the deviation from 1 µs may be annoying in calculating loop times, since all the internal timing of the 8051 is derived from the quartz crystal clock oscillator. This dilemma, by the way, has resulted in the integration of on-chip baudrate generators in follow-up controllers such as the 80535 and 80537, whose serial interfaces are capable of operating at 4,800 baud and 9,600 baud exactly, while a 12 MHz quartz crystal is used. More about these interesting processors in future issues of *Elektor Electronics*.

Transmitting

Transmitting a byte is very simple: write it to the SBUF register. The write operation causes the transmitter control to start the shift-out operation. The transmit register has a ninth bit position, which is loaded with a '1' at the start of the transmit operation. Next, the start bit (0=low) is transmitted (Fig. 46).

Next, the eight databits are shifted out, starting with bit 0. The SBUF transmit register is filled with zeroes. When the ninth bit (i.e., the stop bit with value '1') has been sent, the TI bit in the SCON register is made '1' (Fig. 44) to mark the end of the transmission. This allows an interrupt to be generated (by setting the relevant bit in the interrupt enable register). It is also possible to interrogate this bit by software (polling), to check for the end of the transmission.

EMON51 contains a subroutine called SND (lines 30 to 39 in Fig. 47) that enables a character held in the accumulator to be transmitted via the serial interface.

```
***** LISTING of EASM51 (V24XAMPL) ******
INE LOC  OBJ        T       SOURCE
  1 0000                    ; taken from EMON51.A51
  2 0000                    ;-------------------------------------------------------------
  3 0000                    ;
  4 0000                    V24SPD  EQU 256-13        ; V24 speed: 1MHz/16/13 = 4807.69 baud
  5 0000                    ;-------------------------------------------------------------
  6 0000                    ;                         ; SFR definitions:
  7 0000                    PSW     EQU 0D0H
  8 0000                    ACC     EQU 0E0H
  9 0000                    ;
 10 0000                    PCON    EQU 087H
 11 0000                    TCON    EQU 088H
 12 0000                    TMOD    EQU 089H
 13 0000                    TL1     EQU 08BH
 14 0000                    TH1     EQU 08DH
 15 0000                    SCON    EQU 098H
 16 0000                    SBUF    EQU 099H
 17 0000                    ;-------------------------------------------------------------------
 18 0000                    CNT1    EQU 050H          ; in RAM: counter for CR/LF time
 19 0000                    ;-------------------------------------------------------------------
 20 0000                            ORG 0
 21 0000 75 87 80 [2] V24SET MOV PCON,#80H    ; SMOD = 1
 22 0003 75 89 22 [2]        MOV TMOD,#22H    ; both counters as timer
 23 0006                                      ; RCLK=0, RCLK=0 with 8051, and in TCON also
 24 0006 75 8D F3 [2]        MOV TH1,#V24SPD  ; preload value TIMER1 (baudrate generator)
 25 0009 75 8B F3 [2]        MOV TL1,#V24SPD
 26 000C D2 8E    [1]        SETB TCON.6      ; start counter 1
 27 000E 75 98 52 [2]        MOV SCON,#052H   ; MODE 1, REN=1, TI=1, RI=0
 28 0011                    ; etc.
 29 0011                    ;-------------------------------------------------------------------
 30 0011 30 99 FD [2] SND    JNB   SCON.1,SND ; wait until last char. finally gone
 31 0014 C2 99    [1]        CLR   SCON.1     ; TI=0
 32 0016 F5 99    [1]        MOV   SBUF,A     ; start transmit
 33 0018 B4 0A 0D [2]        CJNE  A,#10,OK2  ; LF sent?
 34 001B 75 50 64 [2] WAITCR MOV   CNT1,#100  ; if so wait for slow scrolling terminals
 35 001E 74 FF    [1] LOP1   MOV   A,#255
 36 0020 D5 E0 FD [2] LOP2   DJNZ  ACC,LOP2
 37 0023 D5 50 F8 [2]        DJNZ  CNT1,LOP1
 38 0026 74 0A    [1]        MOV   A,#10
 39 0028 22       [2] OK2    RET              ; all ok
 40 0029                    ;-------------------------------------------------------------------
 41 0029                    GETCHR EQU $              ; get character from serial port
 42 0029 30 98 FD [2] GETC1  JNB   SCON.0,GETC1; wait until  one available
 43 002C C2 98    [1]        CLR   SCON.0     ; signal: char. fetched
 44 002E E5 99    [1]        MOV   A,SBUF     ; fetch from buffer
 45 0030 22       [2]        RET              ; ready
 46 0031                    ;-------------------------------------------------------------------
 47 0031 20 98 03 [2] TSTC   JB    SCON.0,isther   ; test if character there return 1 else 0
 48 0034 74 00    [1]        MOV   A,#0            ; no
 49 0036 22       [2]        RET
 50 0037 74 01    [1] isther MOV   A,#1            ; yes
 51 0039 22       [2]        RET
 52 003A                    ;-------------------------------------------------------------------
 53 003A                            END
********* SYMBOLTABLE (21 symbols) **********
  V24SPD :00F3      PSW :00D0       ACC :00E0      PCON :0087
   TCON :0088      TMOD :0089       TL1 :008B       TH1 :008D
   SCON :0098      SBUF :0099      CNT1 :0050    V24SET :0000
    SND :0011    WAITCR :001B      LOP1 :001E      LOP2 :0020
    OK2 :0028    GETCHR :0029     GETC1 :0029      TSTC :0031
 isther :0037
                                                  910109-7
```

Fig. 47. Serial interface subroutines contained in EMON51.

This routine waits as long as bit 1 in the SCON register is '0'. This is necessary because a '0' means that the serial interface is still busy transmitting a character. When the TI bit changes to '1', the transmission is finished, and the serial interface is ready to start sending the current character. This is achieved by resetting the TI bit (line 31), and writing the current character to SBUF (line 32). Although TI remains '0' as long as it takes to transmit the current character, the processor already continues with the next instruction.

To make sure that it can be used with slow scrolling terminals, EMON51 is capable of providing a delay after the LF (line feed = 0AH = 1010) character. This delay allows the terminal (or terminal emulation software) to scroll the screen contents. Obviously, no character may be transmitted before the scroll operation is finished. EMON51 therefore checks if an LF was sent (line 33). If so, the loop WAITCR is called to introduce a delay of about 100×255×3 µs = 76.5 ms. This delay is sufficiently long for most terminals.

That completes the description of the SND subroutine contained in the system monitor EMON51. To enable it to function correctly, the TI bit must be set at the start of the program. After a reset, however, this bit is at '0' (refer back to Fig. 8 in Part 2). Therefore, if you want to use it as a 'transmitter empty' indicator, it must be set to '1' at the start of the program.

Interface control word SCON in EMON51

The above explains the value loaded into the SCON register in line 27. The control word, 52H (01010010B), is built as follows. To start with, bits 5, 6 and 7 (010B) select Mode 1. Next, we also wish to receive data. This requires the receiver enable bit (bit 4) to be set. Bits 2 and 3 are not of interest for the moment, and are left at '0'. Bit 1 (TI) is set to mark the SBUF register as 'empty' for the rest of the programming. This is necessary to be able to execute a subsequent transmit instruction. Since no byte has been received so far, RI (bit 0) is set to '0'.

That completes the initialization of the serial port for duplex operation at 4,800 baud, 8 databits, 1 stop bit and 1 start bit.

```
****** LISTING of EASM51 (XAMPLE13) ******
LINE LOC  OBJ          T        SOURCE
   1 0000                ; ****** FILE XAMPLE13.A51 ************************************
   2 0000                ;
   3 0000                ACC      EQU   0E0H
   4 0000                PCON     EQU   087H
   5 0000                TCON     EQU   088H
   6 0000                TMOD     EQU   089H
   7 0000                TL1      EQU   08BH
   8 0000                TH1      EQU   08DH
   9 0000                SCON     EQU   098H
  10 0000                SBUF     EQU   099H
  11 0000                ;
  12 0000                CH       EQU   090H            ; MIDI channel 0
  13 0000                ;
  14 0000                         ORG   4100H
  15 4100 75 87 80 [2]           MOV   PCON,#10000000B ; SMOD=1
  16 4103 75 89 22 [2]           MOV   TMOD,#00100010B ; both auto preset timer
  17 4106 75 8D FE [2]           MOV   TH1,#256-2      ; preset value for TIMER0
  18 4109 75 8B FE [2]           MOV   TL1,#256-2
  19 410C D2 8E    [1]           SETB  TCON.6          ; start TIMER0
  20 410E 75 98 52 [2]           MOV   SCON,#01010010B ; MODE 1 , enable receiver
  21 4111 90 C0 00 [2] START1    MOV   DPTR,#0C000H
  22 4114 E0       [2]           MOVX  A,@DPTR         ; read key
  23 4115 20 E7 F9 [2]           JB    ACC.7,START1    ; start when key pressed
  24 4118 90 41 4F [2]           MOV   DPTR,#NOTES     ; pointer to NOTES
  25 411B 74 90    [1] NOTELP    MOV   A,#CH
  26 411D 31 3F    [2]           ACALL SNDMIDI         ; send to MIDI ( MIDI channel )
  27 411F 31 2F    [2]           ACALL GETNXT
  28 4121 31 3F    [2]           ACALL SNDMIDI         ; ( MIDI NOTE )
  29 4123 31 2F    [2]           ACALL GETNXT
  30 4125 31 3F    [2]           ACALL SNDMIDI         ; ( MIDI VOLUME )
  31 4127 31 2F    [2]           ACALL GETNXT          ; duration
  32 4129 60 E6    [2]           JZ    START1          ; =0 means end
  33 412B 31 33    [2]           ACALL WAIT            ; otherwise wait this time
  34 412D 80 EC    [2]           SJMP  NOTELP          ; and on at next note
  35 412F                ;
  36 412F E4       [1] GETNXT    CLR   A               ; offset 0
  37 4130 93       [2]           MOVC  A,@A+DPTR       ; fetch byte
  38 4131 A3       [2]           INC   DPTR            ; increment datapointer
  39 4132 22       [2]           RET                   ; done
  40 4133                ;
  41 4133 7F 64    [1] WAIT      MOV   R7,#100         ; wait approx. ACC*100*200*2 microsec
  42 4135 7E C8    [1] WAIT1     MOV   R6,#200
  43 4137 DE FE    [2] WAIT2     DJNZ  R6,WAIT2
  44 4139 DF FA    [2]           DJNZ  R7,WAIT1
  45 413B D5 E0 F5 [2]           DJNZ  ACC,WAIT
  46 413E 22       [2]           RET
  47 413F                ;
  48 413F 30 99 FD [2] SNDMIDI   JNB   SCON.1,SNDMIDI  ; wait until transmitter empty
  49 4142 C2 99    [1]           CLR   SCON.1          ; clear bit
  50 4144 F5 99    [1]           MOV   SBUF,A          ; send
  51 4146 22       [2]           RET
  52 4147                ;
  53 4147 30 98 FD [2] GETMIDI   JNB   SCON.0,GETMIDI  ; wait until receiver full
  54 414A C2 98    [1]           CLR   SCON.0          ; clear bit
  55 414C E5 99    [1]           MOV   A,SBUF          ; fetch byte
  56 414E 22       [2]           RET
  57 414F                ;
  58 414F 30 64 06       NOTES   DB    48,100,6      ; Note 48 w. 100 on, wait 6 periods
  59 4152 30 00 01               DB    48,0  ,1      ; Note 48 off again, wait 1 period
  60 4155 34 64 06               DB    52,100,6      ; Note 52 on w. 100
  61 4158 34 00 01               DB    52,0  ,1      ; and off again
  62 415B 37 64 0A               DB    55,100,10     ; etc.
  63 415E 37 00 00               DB    55,0  ,0      ; length 0 means end
  64 4161                        END
********** SYMBOLTABLE (18 symbols) **********
       ACC :00E0      PCON :0087       TCON :0088       TMOD :0089
       TL1 :008B       TH1 :008D       SCON :0098       SBUF :0099
        CH :0090    START1 :4111     NOTELP :411B     GETNXT :412F
      WAIT :4133     WAIT1 :4135      WAIT2 :4137    SNDMIDI :413F
   GETMIDI :4147     NOTES :414F
                                                          910109-7-15
```

Fig. 48. Assembly language listing of the MIDI sequencer program.

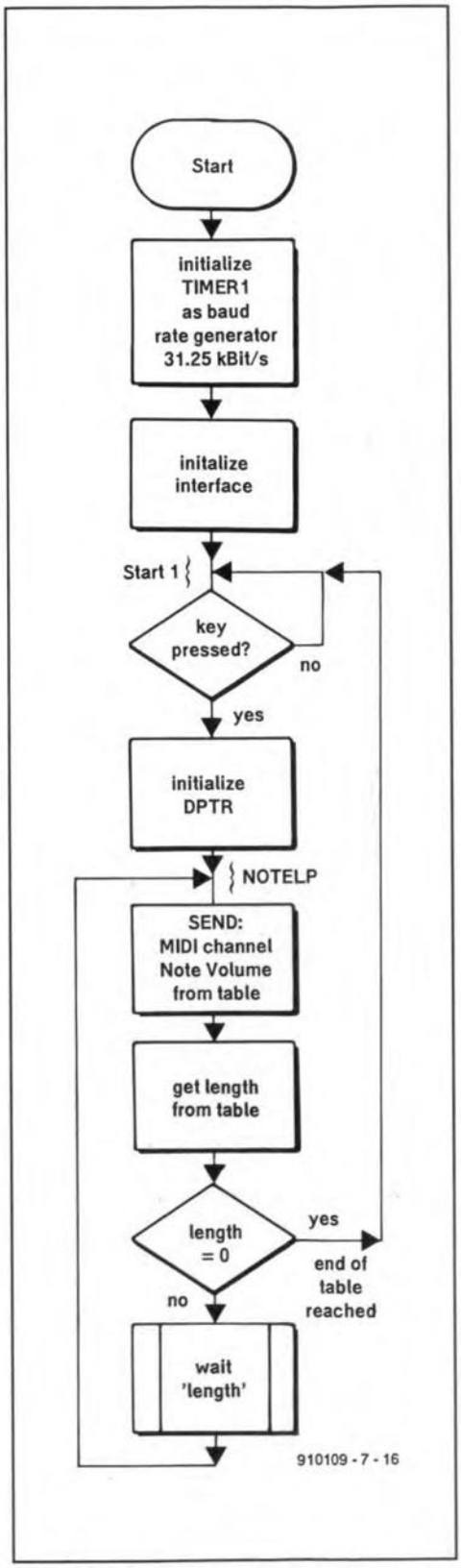

Fig. 49. Main MIDI transmit routine flowchart.

Receiving

Data reception is arranged by a subroutine called GETCHR (get character) contained in EMON51. Initially, this subroutine (line 42) waits until bit 0 in the SCON register is set. This position has the RI bit, and changes to '1' when a complete character has been received. Next, the program resets RI (in line 43). The received character is fetched from SBUF and copied into the accumulator. That is all there is to it.

In some cases, it is necessary to check if a character is ready to be fetched. For this purpose we have a subroutine called TSTC (lines 47 to 51), which returns a '1' to the accumulator when a character is ready. If not, it returns a '0'. The operation of TSTC will be clear at this point: it simply tests the RI bit.

MIDI transmit sequencer

To close off this instalment, let us look at how the serial interface can be used to send data to a MIDI compatible instrument. The aim is to develop a program that sends a series of note commands to the instrument when key S_2 on the extension board is pressed. This allows a simple melody to be played, or a rhythm box to be realized.

To be able to program different melodies in a simple manner, the data to be transmitted should be contained in a table. In that way, the program could form the basis for a small sequencer.

A MIDI 'note' command consists of three bytes. The first byte tells the instrument that a note command follows, and indicates on which channel the note is to be played. Here, we wish to use channel 1 (internal number 0), for which the byte must have the value 090H. The next byte indicates the note proper, while the third byte indicates the volume at which it is to be played (note that this requires a note to be switched on and off!). Thus, every note requires the interface to send three bytes, of which first is always the same, hence, need not be stored in the table. Yet, we store a third byte to form a MIDI command. This byte determines the time that elapses before the next MIDI command is sent. The table therefore has three bytes (entries) for every MIDI command:

[Note, volume, duration]

The end of the table is marked by 'duration = 0'.

In the listing of the MIDI driver (Fig. 48), the table starts at the label NOTES. The individual table entries are addressed in the usual way with the aid of the DPTR. The operation of the main program is simple to analyse by studying the flowchart in Fig. 49.

Since the MIDI operates at a speed of 31.25 kBit/s, the baudrate clock is readily obtained by dividing the 8051 internal clock (1 MHz) by 32. Since the serial interface clock is always divided by 16 (internally in the 8051), Timer1 must be programmed to divide by 2, while SMOD must be set to '1'. This is done in lines 15 to 19 of our example program. Next, the control word copied into SCON (line 20) sets mode 1, receiver switched on, TI=1, i.e., transmitter empty. Apart from the baudrate setting, the mode selection procedure is identical to that used in EMON51.

SNDMIDI is the MIDI transmit routine proper. It transmits the character contained in the accumulator. First, it tests TI (SCON bit 1) to check if the previous character is still being transmitted. If so, it waits. If not, the 'transmitter empty' bit, SCON.1, is cleared, and the transmission of the current character (table entry) is triggered by a write operation to SBUF. Again, the transmit routine proper is largely identical to that in EMON51.

Next time

Next month's final instalment of this course will discuss the connection of a liquid crystal display (LCD) and a keyboard to the SBC extension board. ❑

NEW BOOKS

WORLD SATELLITE TV AND SCRAMBLING METHODS
By Frank Baylin, Richard Maddox and John McCormac
ISBN 0-917893-11-5
Price $40 or £27 (soft cover)

This second edition of the 'Technician's Handbook' is again aimed at everyone with an interest in satellite TV reception, and, in particular, decoder operation. Although the larger part of the book deals with principles of encoding and decoding satellite TV signals, a number of quite sizeable other chapters discuss the hardware layout of a TVRO station, from the dish antenna to the video connectors.

Interestingly, both North American and European technology is discussed in great detail. The European contributions are by John McCormac, who is known as a columnist in *Satellite Trader*.

When comparing the second edition of the book with the first, it is salient to notice that the added sections (in which we find subjects like the SCART connector, SMARTcards, repair and service, and loopthrough decoder connections) are, firstly, nearly all European-oriented and, secondly, partly rewritten material already published in McCormac's book *European Scrambling Systems*, also known as 'The Black Book'.

The book has a wealth of illustrations, practical circuits, tables and overviews. It is also remarkable for its easy-going style. Unfortunately, some subjects are only covered superficially, although, admittedly, this can hardly be a serious criticism given the huge amount of information presented, and the large number of references to more detailed information.

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KU-BAND SATELLITE TV — THEORY, INSTALLATION AND REPAIR **(4th Edition)**
By Frank Baylin and Brent Gale
ISBN 0-917893-10-7
Price $30 or £23

This book is covers 11-GHz (Ku-band) satellite TV reception in virtually every detail. Remarkably, the authors are American, while the use of the Ku band for satellite TV is not nearly as widespread in the USA as it is in Europe. None the less, the coverage of the subject is outstanding, and the authors have succeeded in producing a manual with material that is understandable to anyone having a curiosity but not necessarily a technical background. Indeed, this reviewer agrees with them that there is no reason why laymen should not be able to participate in this exciting field in one way or another.

The particularly strong sections of the book are 'component operation', 'installation' and 'troubleshooting and repair'. Also, the collection of footprints of European, American, Australian and Japanese TV satellites in Appendix C is invaluable for a quick estimate of what can be received given your dish size and location. Solid material — well worth buying.

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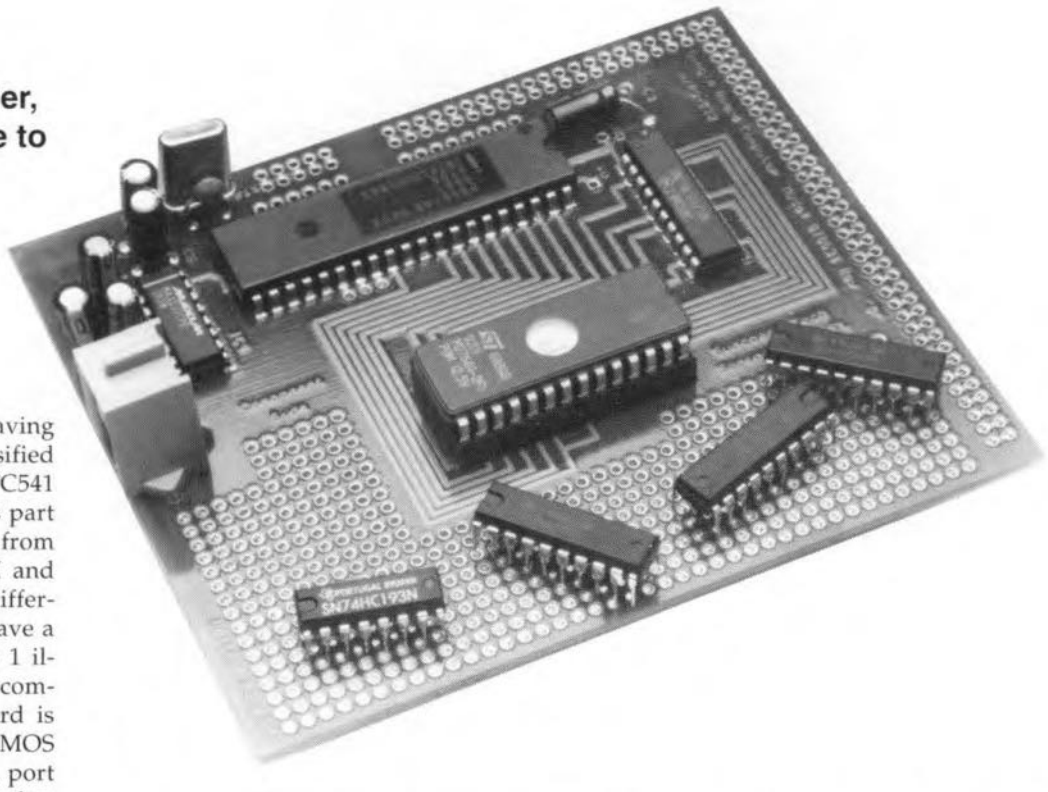
8051 SINGLE BOARD COMPUTER

This article describes an inexpensive single board computer based on the popular 8051 microcontroller, plus a bit of assembly code to get things going.



By Steve Sokolowski

NORMALLY, a number of ICs having features in common can be classified as a 'family'. Devices such as the 87C541 and the 80C525 can be considered as part of the 8051 family of microcontrollers from Intel. Although internal ROM/RAM and the added presence of EPROM are different between individual chips, they have a number of common features. Figure 1 illustrates the main blocks of the 8051 computer family. Our development board is based on the easily obtainable HMOS 8051, of which the basic architecture, port functions, programming, and many other features are discussed in great detail in our *8051/8032 Assembler Course*, of which part 7 appears elsewhere in this issue.

Circuit description

The circuit diagram of the 8051 SBC, Fig. 2, shows that very few components are required to build a versatile development system around the Intel controller. In fact, the circuit is probably the absolute minimum that you will need to start programming the device.

The 8051 clock oscillator is run at 11.0592 MHz to enable the serial interface of the controller to transmit and receive at any of the standard baud rates between 300 and 9600 bits s^{-1}.

The address latch enable (ALE) signal is used to separate the data bus signals from the multiplexed data/address bus signals on the AD0-AD7 pins of the 8051. The latch used is a Type 74LS373 octal D-type flip flop with 3-state output buffers. When the output enable (OE) pin is low, the latched data appears at the outputs. When OE is high, the outputs are in the high-impedance 'off' state. The enabling pulses are supplied by the 8051's ALE output. These pulses effectively enable the 74LS373 to strip the low-order address bus from the eight AD lines by turning on the latches' eight 3-state buffer outputs at the correct instant, thus allowing only the addressing information to be fed to the memory.

The external access enable (EA) input of the 8051 (pin 31) is made permanently low here to enable the controller to fetch program code from the external program memory locations in the address range between 0000H and 0FFFH. Here, the program code is stored in an EPROM, IC3.

The serial interface is formed by the well-known MAX232 RS232 level converter, which is connected directly to the serial input and output pins of the 8051. The MAX232 has on-board positive and negative step-up voltage converters that obviate a symmetrical supply. The IC gen-

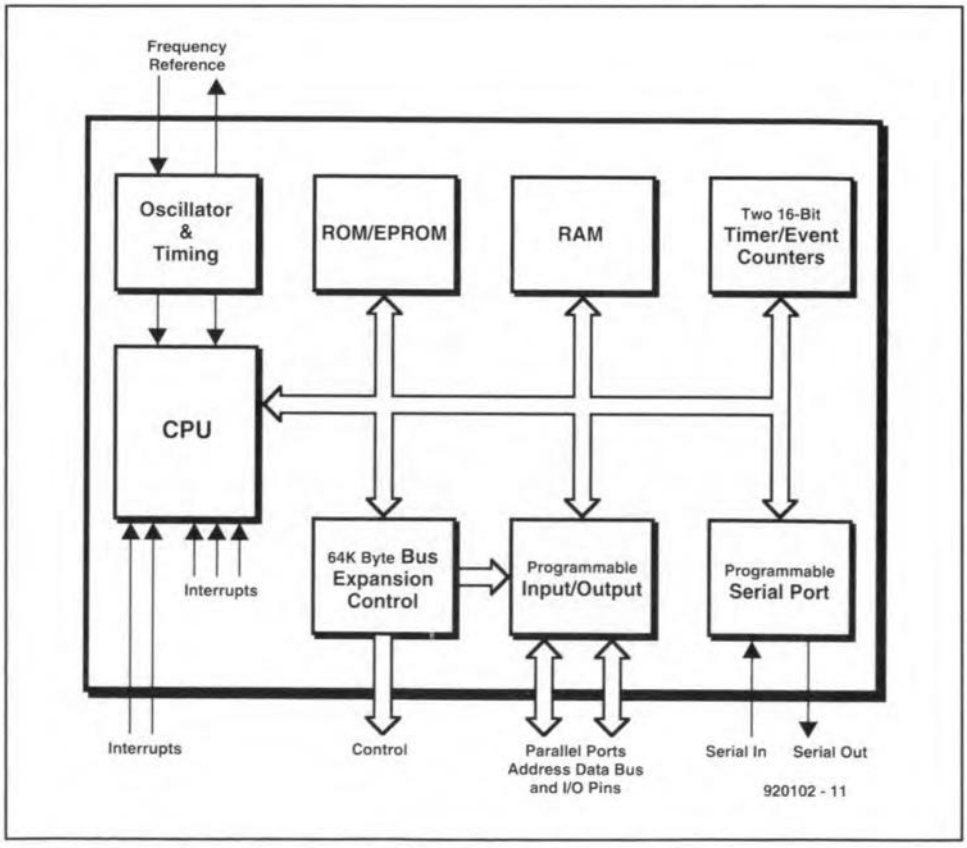


Fig. 1. 8051 family microcontroller architecture.

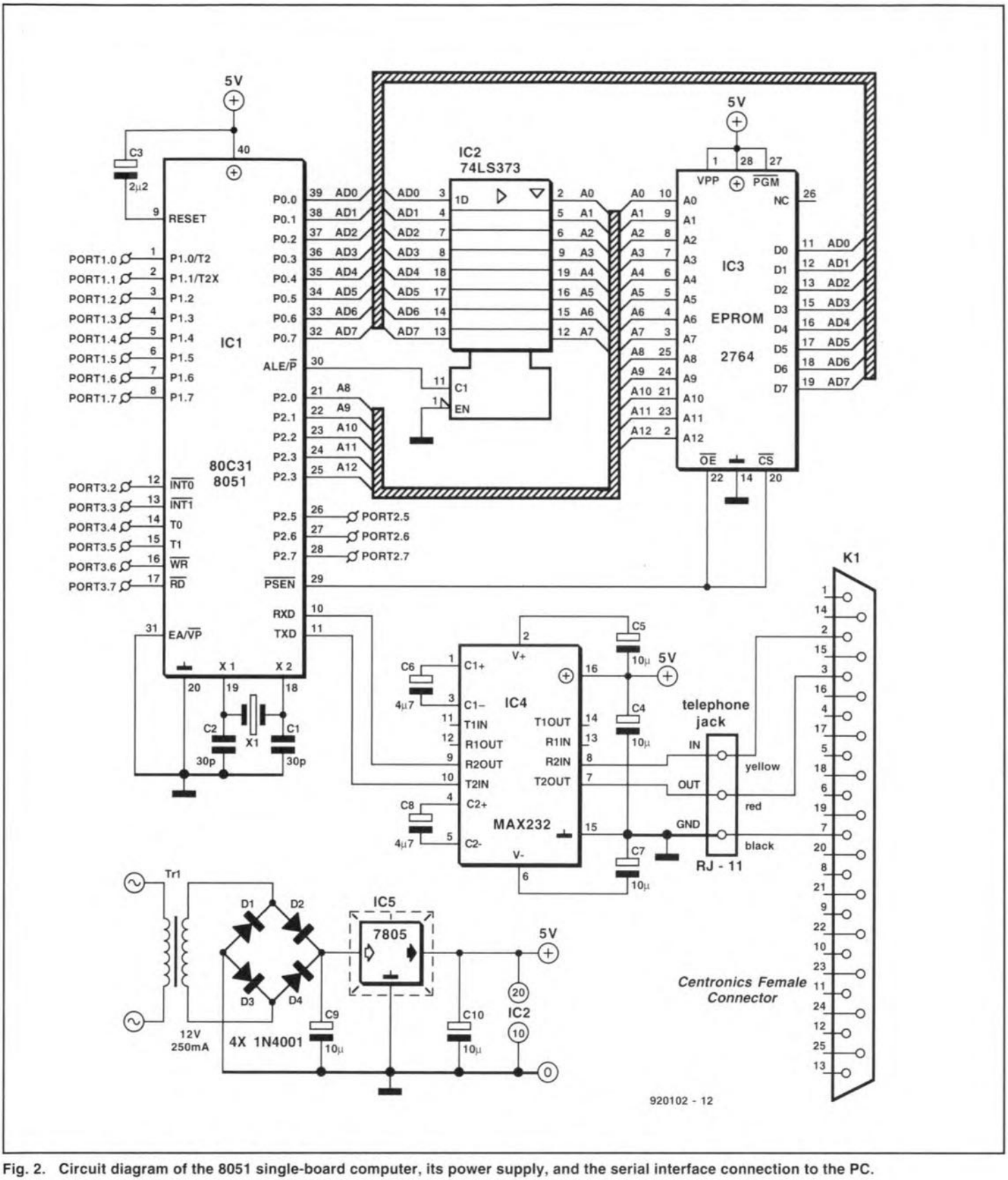


Fig. 2. Circuit diagram of the 8051 single-board computer, its power supply, and the serial interface connection to the PC.

erates internal supply voltages that result in a swing of 20 V (±10 V) on the RS232 output line.

A short length of inexpensive telephone cord is used to connect the 8051 board to the RS232 port on the PC. At the board side of the cable is a 4-way miniature latching telephone cord plug, while a standard D25 sub-D connector (female) is used at the computer side (for pinning details refer to the circuit diagram).

The power supply of the SBC is a classic one designed around the 7805. The mains transformer could be a small mains adaptor with a.c. output. Such and adaptor will in many cases be cheaper (and in all cases, safer to use!) than a discrete transformer. The current demand on the adaptor will be between 250 mA and 500 mA, depending on the circuit fitted in the extension area on the SBC board. In any case, the 7805 will run fairly hot, so it must be fitted with a heat-sink.

Building the SBC

If you are interested in building the present 8051 development system, you have two options: (1) produce the PCB yourself (using the artwork given in Fig. 3) and purchasing the components from your local stockist, or (2) purchase a complete kit from Suncoast Technologies.

The following few paragraphs are intended for those of you who wish to assemble the 8051 SBC on a home brewed printed circuit board, which will probably not be plated through, contrary to the one supplied by Suncoast Technologies. Since a fair number of PCB through connections is required, it is best to use Molex clip-type connectors for the IC sockets. These clips can be placed in the holes provided for the IC pins, and soldered at both sides of the board before they are removed from their metal carrier. The resulting pin strips then form an IC socket. To reduce cost, you may want to use Molex connector strips for the EPROM socket only, and solder the 8051, the 74LS373 and the MAX232 direct on to the board, making sure that all pins are soldered at both sides of the board.

Capacitors C4 and C8 are electrolytic types and require proper placement on the board. Mis-insertion of these polarity sensitive components can spell disaster for the part, so take care while fitting them.

The RJ-11 telephone jack was designed in such a way that it can be inserted on the board in only one way. Carefully line up the four 'pig-tail' terminals with their corresponding holes. When lined up, carefully press the jack on to the board until its mounting clips protrude on the opposite side of the board. Solder the four contacts at the solder side of the board. Finally, fit the crystal and the two ceramic capacitors.

Note that the SBC has a large prototyping area. To help eleminate the need for extra wiring of the voltage buses, the board also contains a common ground and positive supply bus etched in. It is this area where the required interfacing components for future projects can be mounted. The power supply may also be hand wired in this section.

Inspect the completed board for solder

COMPONENTS LIST

Capacitors:

2	33pF 16V disc ceramic	C1;C2
1	2µF2 16V radial	C3
3	10µF 16V radial	C4;C5;C7
2	4µF7 16V radial	C6;C8
1	470µF 35V radial	C9
1	100µF 16V radial	C10

Semiconductors:

4	1N4001	D1-D4
1	8051 or 8031	IC1
1	74LS373	IC2
1	2764 EPROM	IC3
1	MAX232	IC4
1	7805	IC5

Miscellaneous:

1	12V a.c. mains adaptor	Tr1
1	11.0592MHz quartz crystal	XTAL
1	25-pin female sub-D connector with hood	P1
1	4-conductor telephone line cord with clip (approx. 6 ft.)	
1	RJ-11 PCB mount telephone jack	
1	TO-220 heat-sink	
28	Molex connector pin or	
1	28-pin IC socket (see text)	
1	Printed circuit board (Suncoast Technologies)	

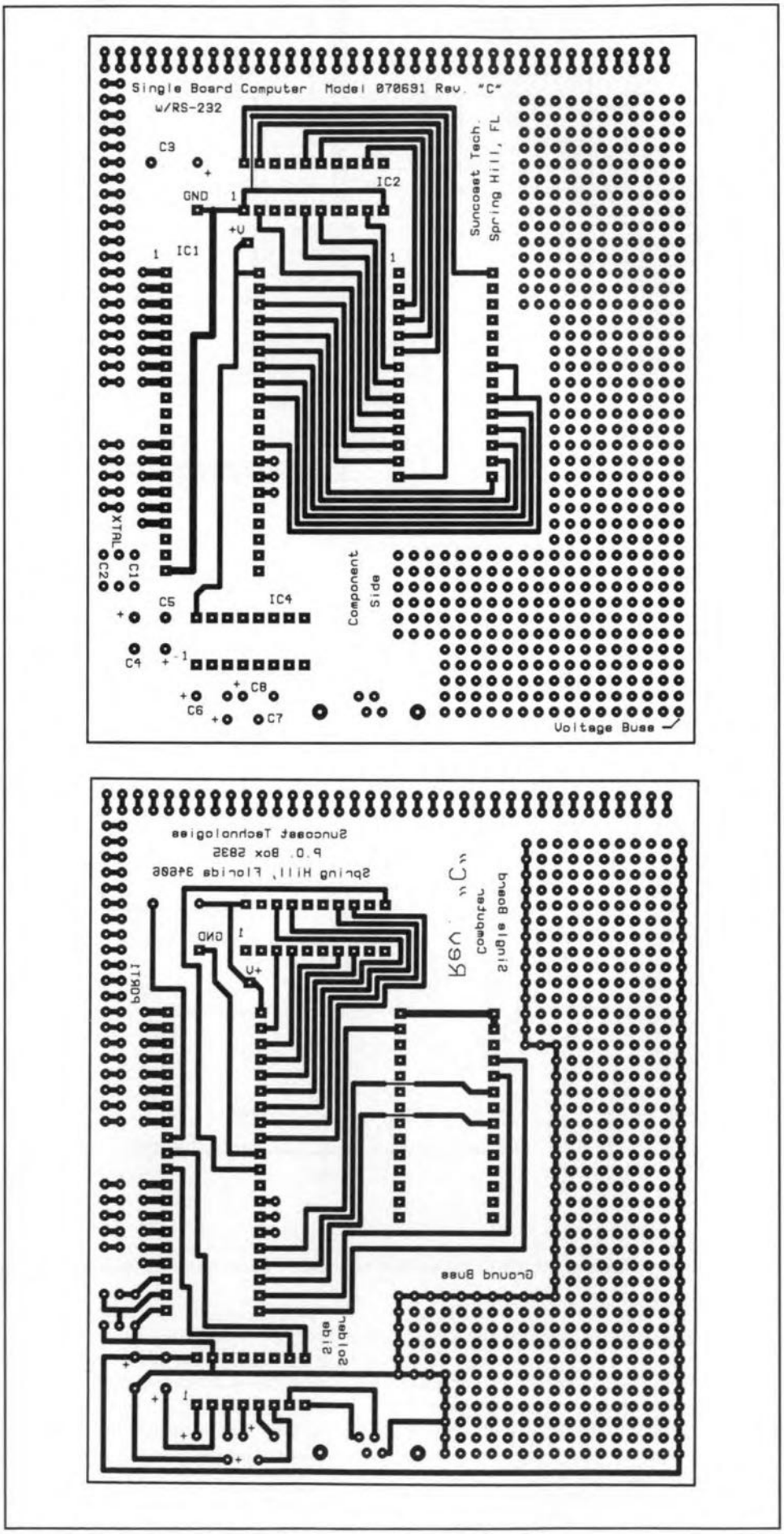


Fig. 3a. Component side and solder side track layout of the PCB.

splashes, dry joints and solder bridges. When all is to your satisfaction, the 5-volt power supply can be connected to the board.

Testing the SBC

Shown in Fig. 4 is a test program in assembly language. When programmed into a 2764 EPROM, TEST.ASM will determine if all address and data lines are wired correctly. It also checks the serial cable to the PC, and the wiring of the MAX232.

TEST.ASM uses the serial output feature (CHR_OUT) of the 8051 to print any character on the computer screen. It also allows keyboard input (CHR_IN) to be echoed to the screen. Both CHR_IN and CHR_OUT check out the operation of the MAX232 chip. If either feature does not work, double check the wiring of IC4 and that of the interface cable assembly (which also includes the RJ-11 telephone jack).

TEST.ASM was written to be assembled into machine code with the A51 assembler (version 1.4 or earlier), an inexpensive program that can be purchased from just about any shareware distributor. Once assembled, TEST.ASM is converted into a series of hexadecimal numbers (TEST.HEX). Although converted, TEST.HEX can not be loaded into an EPROM just like that. Further conversion is necessary, and for this HEXBIN.COM is proposed. HEXBIN.COM takes the hexadecimal format of TEST.HEX, and transforms it into a binary file (TEST.BIN), which is programmed into the 2764 EPROM.

```
;   8051 SBC Test Program
; by: Suncoast Technologies
;     Spring Hill, Florida
;
; Program set to 1200 Bauds
;
        .EQU    ESC,H'1B
        .ORG    H'0000
INIT:   MOV     A,#H'40
        MOV     SP,A
        CLR     A
        MOV     PSW,A
;
;  INITIALIZE SERIAL PORT
;
        MOV     SCON,#H'52
        MOV     TMOD,#H'20
        MOV     TH1,#H'E8
        SETB    TR1
;
;     PRINT GREETINGS
;
MENU:   LCALL   XSTRING
        .DB     "\n\r"
        .DB     "8051 Single Board "
        .DB     "Computer Test Program"
        .DB     "\r\n\n"
        .DB     ESC
LOOP_1: LCALL   XSTRING
        .DB     "Hit a key - I will echo "
        .DB     "the character \n\n\r"
        .DB     ESC
LOOP_2: LCALL   CHR_IN
        CJNE    A,#D'13,LOOP_2
        .DB     ESC
        LCALL   XSTRING
        .DB     "\n\r"
        .DB     ESC
        LJMP    LOOP_2
;
;     'PRINT'  PROGRAM
;
XSTRING: POP    DPH
        POP     DPL
SRT_1:  CLR     A
        MOVC    A,@A+DPTR
STR_2:  JNB     TI,*
        CLR     TI
        MOV     SBUF,A
        INC     DPTR
        CLR     A
        MOVC    A,@A+DPTR
        CJNE    A,#ESC,STR_2
        MOV     A,#1
        JMP     @A+DPTR
;
;       SERIAL  I/O
;
CHR_IN: JNB     RI,*
        CLR     RI
        MOV     A,SBUF
        ANL     A,#H'7F
        ACALL   CHR_OUT
        RET
;
CHR_OUT: JNB    TI,*
        CLR     TI
        MOV     SBUF,A
        RET
        .END
```

920102-13

Fig. 4. An assembly language program to test your new 8051 single board computer.

Once programmed, carefully insert the EPROM into its IC3 location on the board. With your PC running your favourite communication program (QMODEM, PC TALK, Procomm, etc.) at 1200 baud, take the mains adaptor and plug it in. Within an instant the SBC will display the following:

8051 Single Board Computer Test Program
Hit a key — I will echo the character

Now, just for fun, type "Hello there" on the PC keyboard, then press the ENTER or RETURN key. The keyboard input will be echoed and printed on the next line. When the 25th line is reached, all text is scrolled up by one line.

If you wish to start programming to 8051 single board computer, I suggest you obtain the collection of 'start up' programs contained on a floppy disk supplied by Suncoast Technologies. This 5¼-inch MSDOS floppy disk (3½-inch not available) contains the following conversion tools that can be run on any IBM PC or compatible running under DOS 2.11 or higher:

- simple communication program
- program editor
- A51 program assembler
- D51 program disassembler
- hex-to-binary conversion program
- 8051 test program in .ASM and .BIN

Final thoughts

TEST.ASM is not a very elaborate program, and was not meant to be. It is included here so that you can quickly and easily determine that your 8051 SBC is functioning. As the programming of the 8051 chip becomes easier, you will no doubt start to come up with your own state-of-the-art programs. ■

Price and ordering information relevant to the 8051 single board computer and the associated software is available from **Suncoast Technologies, P.O. Box 5835, Spring Hill, Florida FL 34606, U.S.A.**

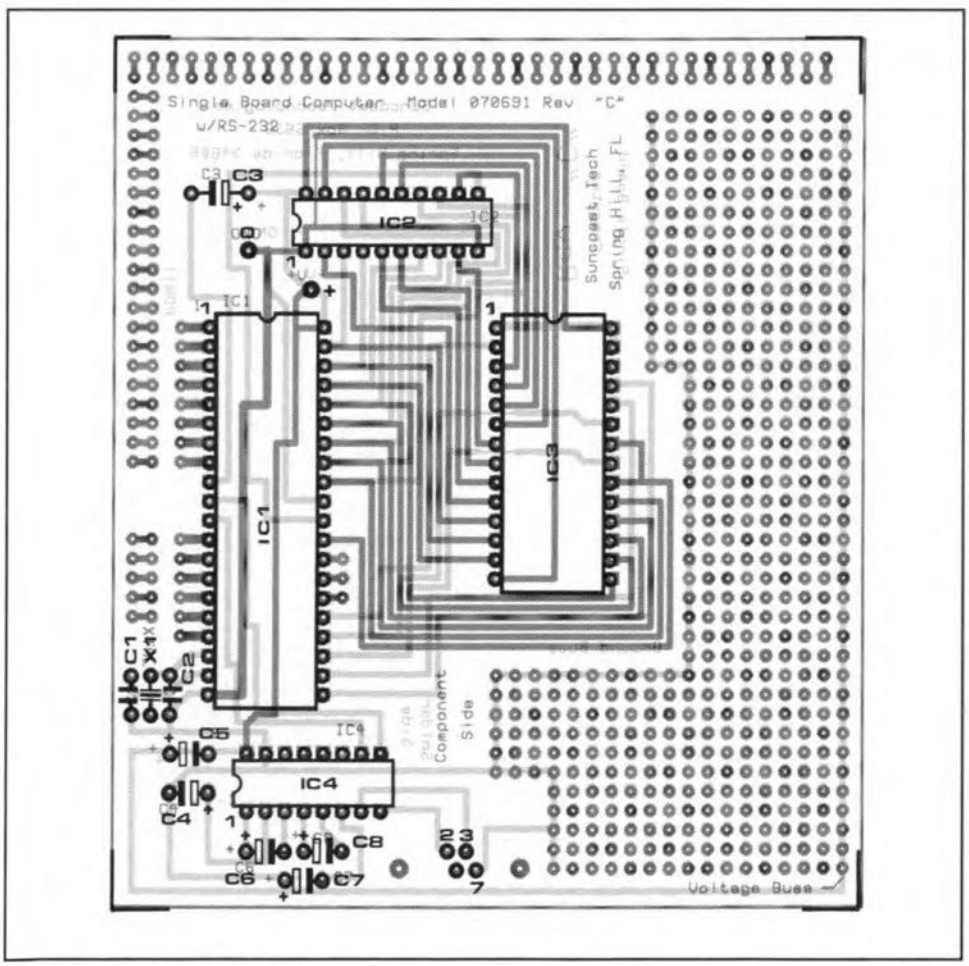
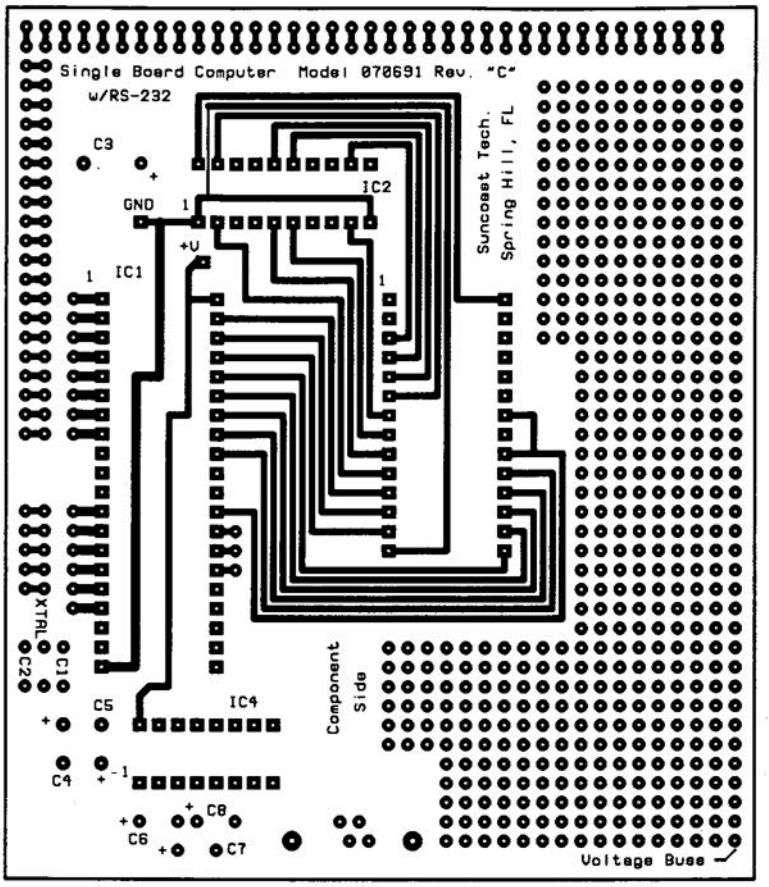
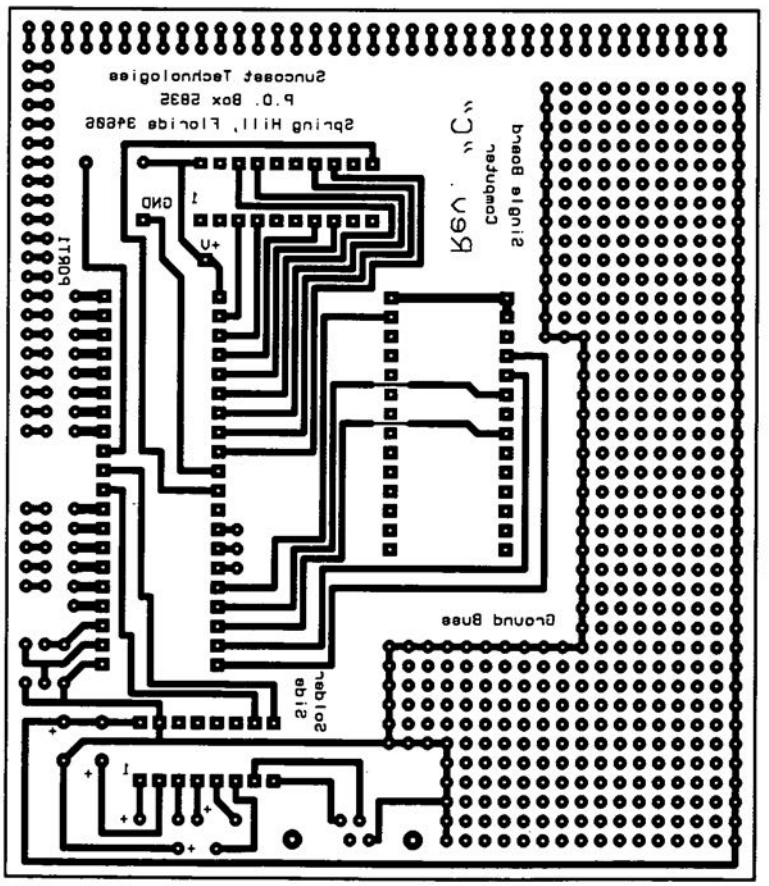


Fig. 3b. Component mounting plan.


Single Board Computer Model 070691 Rev. "C"
w/RS-232
Suncoast Tech.
Spring Hill, FL
C3
GND
IC2
+V
IC1
XTAL
C10
C22
C5
IC4
C4
C8
C6
C7
Component Side
Voltage Buss


Suncoast Technologies
P.O. Box 5895
Spring Hill, Florida 34606
Parallel BUS
Ground Buss
GND
+V
IC10

CORRECTIONS AND UPDATES

8751 Emulator

March 1992, p. 53.
(Corrections; component information)
While in emulation mode, the register contents are displayed with an offset of one vertical line from the associated register designations. This error occurs on early releases of the system software, item ESS 1741, and is caused by one superfluous 'space' character in the DEV.EXE program. This 'space' (20H) should be changed into a 'line feed' (0AH). First, make a backup copy of your original diskette. Next, use a hex editor to change the byte at address offset DE0DH from 20H into 0AH. Using the hex editor of PCTools V6, for instance, this byte is found in relative sector 111 (decimal!), at offset 0DH.

Pins 52, 53 and 54 of the SC80C451 must be connected to ground to give proper access to (simulated) Port 0. For no apparent reason, this is not indicated in the Signetics datasheets. Port 0 is actually simulated by Port 6 of the SC80C451. For further information on this compatibility problem with generic 8051 assembler files, consult the SC80C451 (Signetics) or 8xC451 (Intel) datasheets.

In addition to your local Signetics (Philips Semiconductors) distributors, two suggested suppliers of the controller Type SC80C451CCN64 are:

(1) Macro Marketing Ltd., Burnham Lane, Slough SL1 6LN. Telephone (0628) 604383.

(2) C-I Electronics, P.O. Box 22089, 6360 AB Nuth, Holland. Fax: +31 45 241877.

GAL programmer

May 1992, p. 55.
(Update)
The transistors Type BC369 in positions T6 and T7 are apparently difficult to obtain, and may be replaced by BC640s.

The most recent version of the software is V. 6.53dt, June 1992. The README file contains an update note on problems with the programming of certain GAL makes, as well as a suggestion to make GALs with a damaged electronic signature (type identifier) useable again.

8051 Single board computer

October 1992. p. 40.
(Update)
Since the publication of this article, we have been advised that the telephone number of Suncoast Technologies is +1 (904) 596-7599.

RDS DEMODULATOR WITH INTEGRATED FILTER

The RDS (Radio Data System) demodulator described in the May 1989 issue is based on the SAF7579T, and has an external 4-section 57-kHz bandpass filter ahead of it that is not easy to adjust. A follow-up type of the SAF7559T, the SAA6579T, has an on-chip pre-aligned RDS filter, which eliminates any adjustment.

Design by G. Kleine

BOTH the 'old' (Ref. 1) and the 'new' RDS demodulator are connected to a dedicated 80C32-based controller board (Ref. 2). The combination of the RDS demodulator and the controller board forms a stand-alone RDS decoder.

The SAF7579T requires an external bandpass filter to extract the RDS datastream from the baseband spectrum transmitted by the FM radio station the receiver is tuned to. Unfortunately, this filter is difficult to adjust because of the small bandwidth (approx. 5 kHz). Also, it adds to the total cost of the decoder, and takes up board space, which are important considerations in mass production (car radios!). Philips Components, the manufacturer of the SAF7579T, have, therefore, worked on an improved version of this RDS demodulator IC, and added an on-chip band filter that obviates the need for an external filter, and, importantly, filter adjustment. The follow-up type is designated SAA6579T, and is available in a 16-pin small outline SMA (surface mount assembly) package.

Operation

The internal organization of the SAA6579T is shown in Fig. 1. The multiplex signal supplied by the FM receiver is first taken through a second-order anti-aliasing filter. The main function of this filter is to prevent spurious products in the following filter, which is based on switched capacitors (SC filter). Without the anti-aliasing filter, the SC filter is prone to transform certain components in the input frequency spectrum into its pass-band (this effect is called 'aliasing').

The 57-kHz SC band-pass filter is an 8th order type with a bandwidth of about 3 kHz. It is followed by a reconstruction filter that serves to smooth and clean the output signal before it is fed to the SCOUT pin of the IC. Figure 2 shows the pass-band characteristic of the integrated SC filter (MUX-to-SCOUT).

The filter output signal is coupled capacitively to the input of a clocked comparator, which digitizes the biphase modulated 57-kHz signal. A so-called Costas loop recovers the suppressed 57-kHz carrier from the biphase-coded datastream. This recovered carrier provides a central clock signal that is locked on to the received RDS signal. It is used to clock the SC band-pass filter and the comparator, and also to recover the RDS data clock, RDCL.

The output signal of the Costas loop is taken to a biphase decoder, which turns the biphase-coded input signal into the original ones and zeros modulated at the transmitter side. Since these are still differentially coded, the biphase decoder is followed by a difference decoder that supplies the RDS data signal, RDDA.

A signal quality detector is implemented on the chip. It indicates whether the received RDS signal is valid (QUAL=H), or invalid (QUAL=L) because of interference or poor reception. The QUAL signal may be used by the RDS decoder to check that the bits on the RDDA line are error-free.

The central clock of the IC is provided by a quartz crystal oscillator (OSCI; OSCO). Depending on the level applied to the MODE input, the oscillator can work with either of two quartz frequencies: 4.332 MHz or 8.664 MHz.

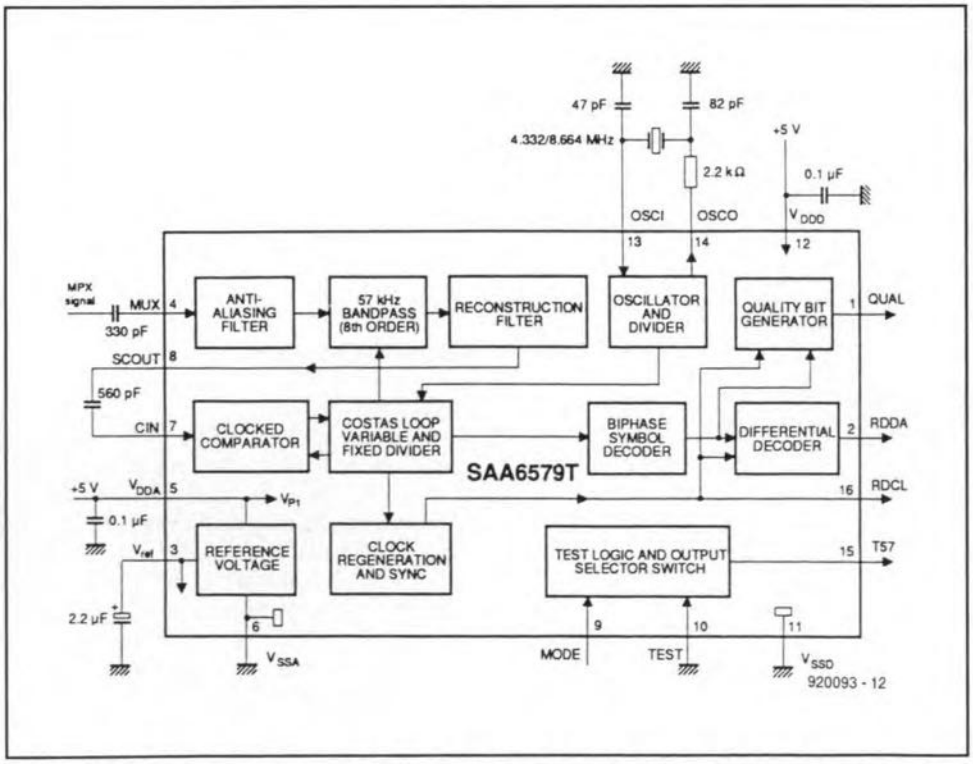


Fig. 1. Block diagram of the SAA6579T RDS demodulator (courtesy Philips Components).

A practical circuit

The circuit diagram of the 'new' RDS demodulator is shown in Fig. 3. This wonderfully simple circuit can be used as a

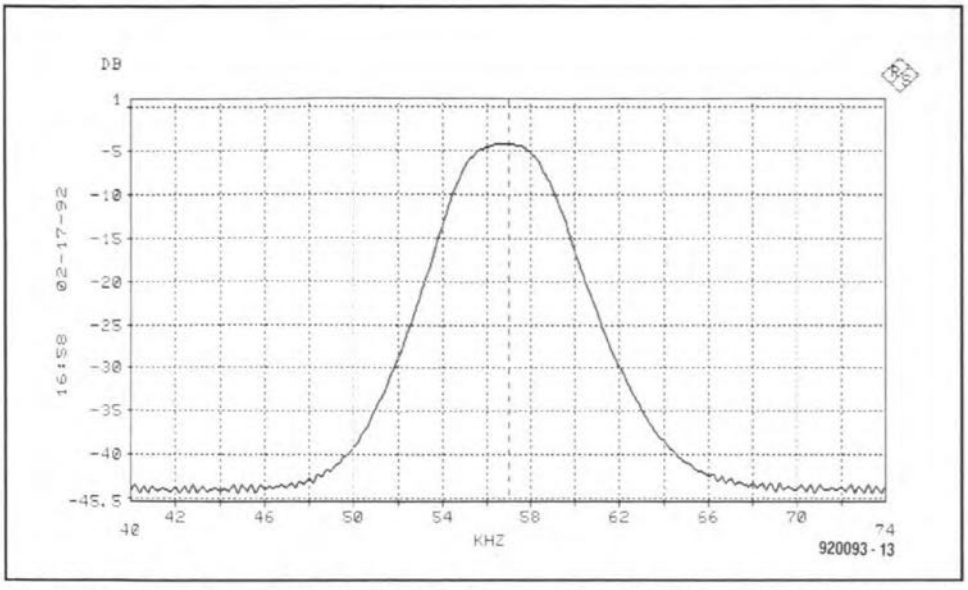


Fig. 2. Pass-band characteristic of the switched capacitor (SC) filter on board the SAA6579T. The dB levels are relative to the signal level at the MUX input.

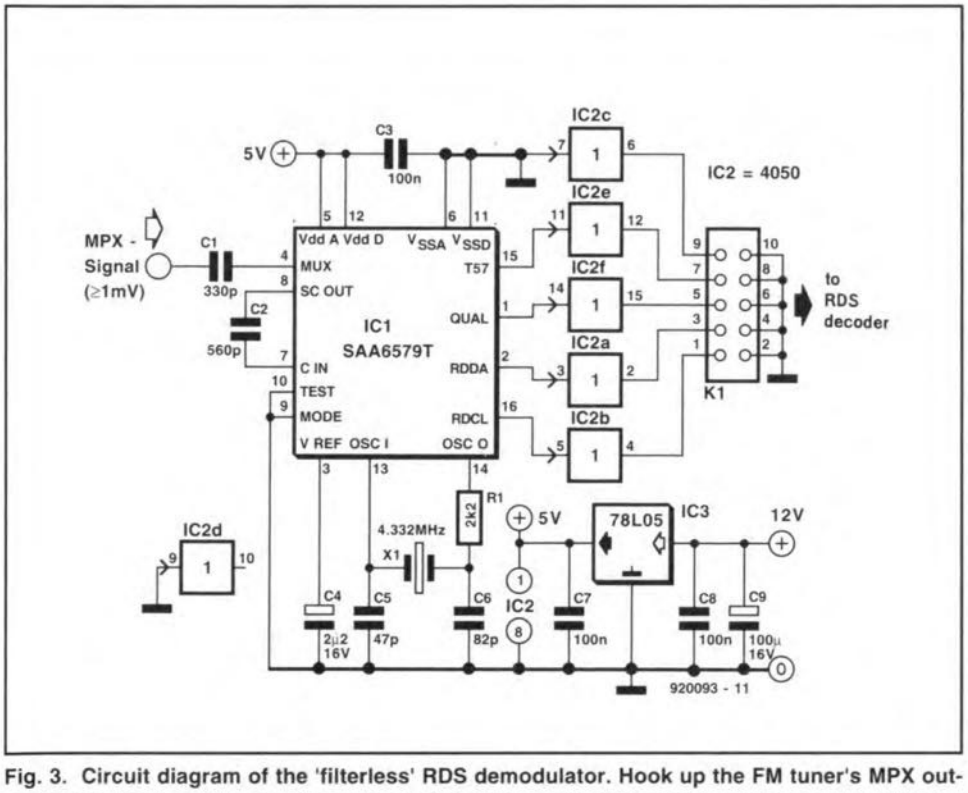


Fig. 3. Circuit diagram of the 'filterless' RDS demodulator. Hook up the FM tuner's MPX output to the input of this circuit, and an 80C32 RDS controller board to connector K1, and you have an experimental RDS decoder.

COMPONENTS LIST

Resistors:

1	2kΩ2	R1

Capacitors:

1	330pF	C1
1	560pF	C2
3	100nF	C3;C7;C8
1	2µF2 16V	C4
1	47pF	C5
1	82pF	C6
1	100µF 16V	C9

Semiconductors:

1	SAA6579T	IC1
1	4050	IC2
1	78L05	IC3

Miscellaneous:

1	4.332MHz or 8.664MHz quartz crystal (see text)	X1
1	10-way PCB pin header	K1
1	Printed circuit board	880209

replacement for the earlier SAF7579T-based version, and is compatible with the associated RDS controller board. Comprising only a handful of components, the SAA6579T-based demodulator can handle input multiplex (MPX) signals in the range from 1 mV to a couple of volts. Capacitor C1 couples the MPX signal to the input filter contained in the SAA6579T. The relatively small value of C1 suppresses the lower-frequency components in the MPX signal because it forms a high-pass filter in combination with the input impedance of the IC.

As described above, a capacitor (here, C2) takes the SCOUT signal to the input of the digital section contained in the SAA6579T. Output signals T57, QUAL, RDDA and RDCL reach the outside world via a Type 4050 CMOS buffer and a 10-way PCB header, just as in the earlier design based on the SAF7579T. Only the ARI (Autofahrer Rundfunk Information; Motorists Broadcast Information) signal is omitted (ARI is a traffic information service broadcast along with RDS in Germany). Hence, the relevant pin header connection is taken to ground.

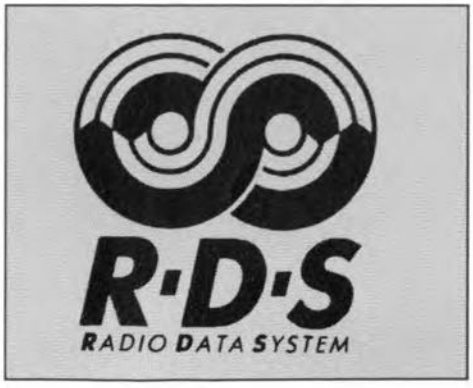
Apart from the components already mentioned there are two supply decoupling capacitors, C3 and C4, and two small capacitors, C5 and C6, that flank the quartz crystal. A resistor, R1, is connected in series with the OSCO output to minimize the quartz dissipation, and improve the oscillator stability. When an 8.664-MHz crystal is used, the mode pin (pin 9) is tied to +5 V instead of to ground.

A low-current 5-V regulator, IC3, is provided to allow the circuit to be powered from supplies with an output voltage between 7.5 V and about 30 V.

The circuit shown here can be constructed without problems on the printed circuit board originally designed for the SAA7579T-based demodulator. The filter components are, of course, not required in that case. The track layout and component mounting plan of this PCB (order code 880209) may be found in Ref. 1.

References:

1. "Radio Data System (RDS) demodulator". *Elektor Electronics* May 1989.
2. "Radio Data System (RDS) decoder". *Elektor Electronics* February 1991.



SCIENCE & TECHNOLOGY

AN ETERNAL ENIGMA:

THE APPLICABLE AND CONSTRUCTABLE FICTIONS OF ELECTRONICS

by M.C. Soper, MA

SOME methods used in electronics are based on models that cannot, in fact, be the case. For example, currents flow continuously and yet consist of the flow of objects: discrete objects, called electrons. Waveforms are commonly denoted by $e^{j\omega t}$, yet, $e^{j\omega t} = \cos\omega t + j\sin\omega t$, where j is defined by $j^2=-1$, which is not true for any real number: j is imaginary.

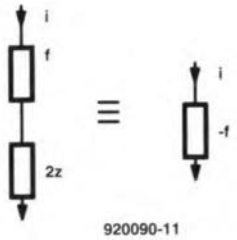
Fictional models like this build the theory on which circuit calculations are based. These fictions are all mathematical and are used to practical effect in calculations. Recently, fictional circuit elements have also been used, like the *nullor* and the *nullator*. Other fictional elements can be joined to the system for ease of circuit calculation; for example, *negative time delays* and *recursive components*.

Can we build it?

Evidently, theoretical use is made of circuit elements that either cannot be made or cannot be manufactured at our present state of knowledge, but may become possible at some future time. We can have physically difficult things to make or theoretically different things to make: a theoretically difficult thing to make is a single, infinitely fast, perfect active switch. A practically difficult thing to make is a minute, large-value, passive inductor. Our fictional elements can:
(a) make a theoretical construction of a practically difficult (or even theoretically difficult) elements possible;
(b) simplify complex calculations.

Why this option?

This approach may be preferred since diagrammatic rather than mathematical methods can be used; that is, a simple understanding of a diagram together with fairly basic computational skills can replace very complex techniques in some cases. One more reason for preferring the use of fictitional elements is that new circuit elements of a theoretical kind can be specified easily, whereas to describe them in other ways may well be lengthy. For example:



920090-11

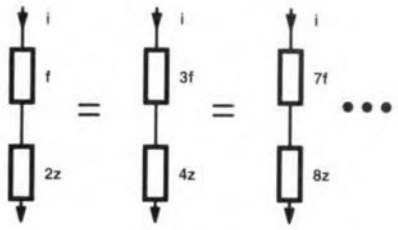
Since these are equivalent,

$$2z + f = -f,$$

where f is thought of like impedance, so that

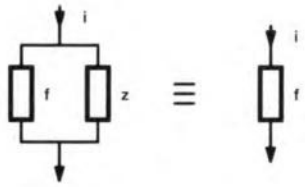
$$f = -z.$$

Thus, recursively we have defined a negative impedance. The recursion in this case is very simple. Note, however, that

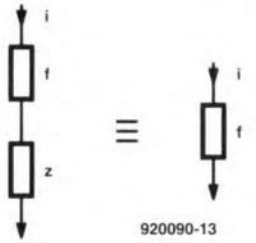


920090-12

As another example,

for any z 

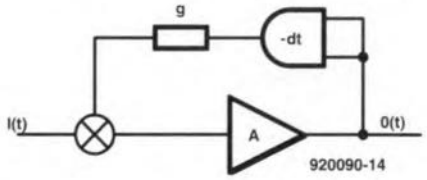
defines a short circuit

and 

defines an open circuit

920090-13

We can also introduce another fictional topic: instead of time delays, time increments. Obviously, these cannot exist, because a signal would be output before it had been input, but



920090-14

has this equation:

$$O(t) = A[I(t) + g\{o(t-dt)\}].$$

Assuming that A and g are reversible and linear:

$$A^{-1}[O(t)] = I(t) + g[O(t-dt)].$$

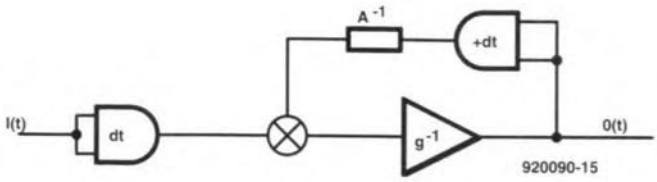
Since this is true at any time,

$$A^{-1}[O(t+dt)] = I(t+dt) + g[O(t)]$$

$$\therefore\ g[O(t)] = -I(t+dt) + A^{-1}[O(t+dt)]$$

$\therefore\ 0(t) = g^{-1}\{A^{-1}[0(t+dt)] - I(t+dt)\}$. [1]

This is a present output with respect to future events; it may be paradoxical, but it has been solved by Richard Feynman. Equation [1] may be obtained from this circuit, where the fictional positive time increment (pti) elements have been included.

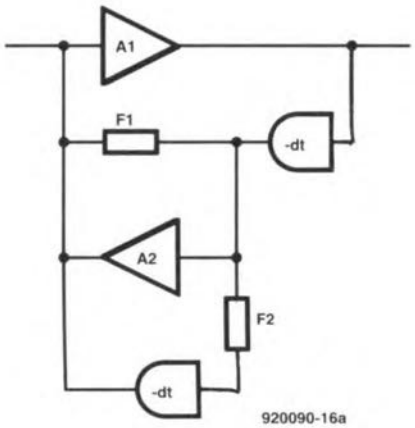


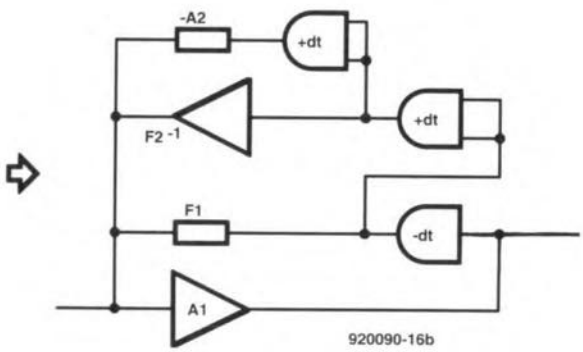
At this stage, the circuit looks merely eccentric, but consider how this type of transition may be used to reduce the complexity of circuits with active elements and delays in the feedback loop. Note also that we can write:

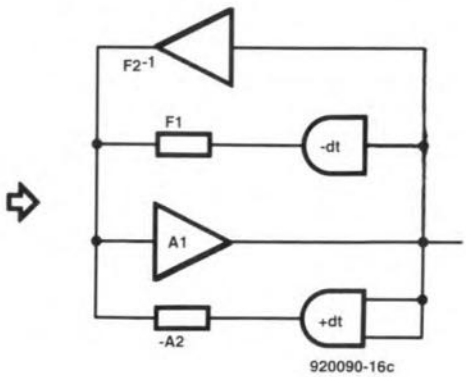
$0(t-dt) = g^{-1}A^{-1}[0(t)] - g^{-1}I(t)$.

Releasing practical constraints

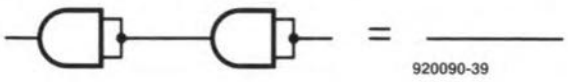
Consider



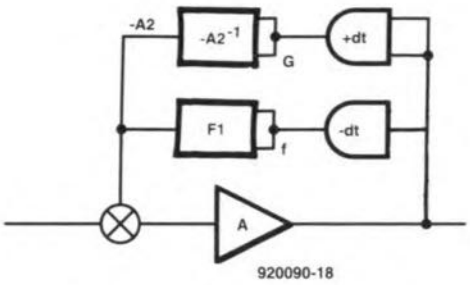




This can be simplified by introducing fictional ptis. The first step is from Equation [1]; the second step is from the fact that



and the third step is from standard and known properties of amplifiers in gfeedback loops. We have, therefore, this remarkable simplification, which is easy to calculate:

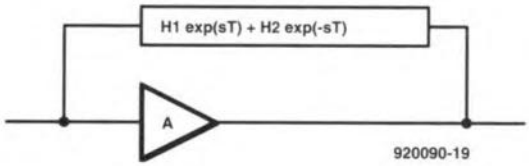


Let $A = A_1/(1+A_1F_2^{-1})$;

then

$0(t) = A\{I(t) + f[0(t-dt)] + g[0(t+dt)]\}$;

or,



Transfer function $A_0 = 1/[be^{-sT} - ae^{sT} + (1/A)]$.

To check further the equivalence of Eq. [1], here is a negative feedback form with linear amplifying and feedback elements:

$$\begin{aligned} 0(t) &= A\{I(t) - f[0(t-dt)]\} \\ &= AI - f\{I(t-dt) - f[0(t-2dt)]\} \\ &= A\textstyle\sum_r A^r f^r[(-1)^r I(t-rdt)], \end{aligned}$$

which, if I is constant,

$$= I_c A \textstyle\sum_r A^r f^r (-1)^r$$

$$= AI_c/(1+Af).$$

If $i = I_0\cos(2\pi ft)$, then, with $B=f$ (feedback) and $AB<1$, we get

$$0(t) = A\textstyle\sum_r A^r f^r (-1)^r \cos(2\pi ft - 2\pi fr dt)$$

$$= \frac{A^2 B\cos[2\pi f(t-dt)] + A\cos 2\pi ft}{A^2B^2 + 2AB\cos(2\pi f dt) + 1}$$

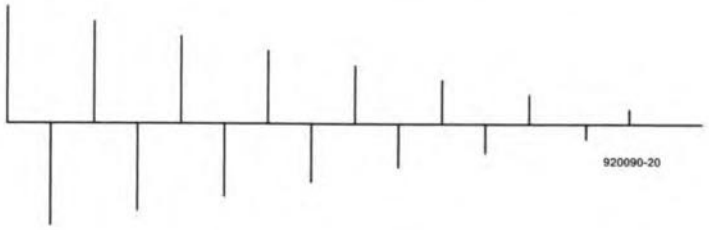
Note that this can also be written without reference to time as the equivalence of operators:

$$0() = \frac{A[AB\cos(2\pi f dt) + 1]\cos[2\pi f()] + A^2 B\sin(2\pi f dt)\sin[2\pi f()]}{1 + 2AB\cos(2\pi f dt) + A^2B^2}$$

Consider the reorganized equation:

$$0(t) = B^{-1}[I(t+\mathrm{d}t) + (-A^{-1})0(t+\mathrm{d}t)]$$
$$= B^{-1}\sum_r (-A^{-1}B^{-1})^r \cos[2\pi f(t+\mathrm{d}t)(1+r)]$$
$$= \frac{B^{-1}\cos(2\pi ft) + B^{-2}A^{-1}\cos[2\pi f(t-\mathrm{d}t)]}{1+2A^{-1}B^{-1}\cos(2\pi f\mathrm{d}t) + A^{-2}B^{-2}}$$
$$= \frac{A^2B\cos[2\pi f(t-\mathrm{d}t)] + A\cos(2\pi ft)}{1+2AB\cos(2\pi f\mathrm{d}t) + A^2B^2}$$

As expected, the reorganized equation, which gives the present output in terms of future inputs and outputs, is just as valid: this is because the signal is one unvarying sine wave and thus conveys no information. None the less, all wave forms can be made out of sine waves of a range of frequencies summed. Thus, this conclusion holds in general. The main intuitive problem is indicated by the response of a delayed negative feedback linear amplifier as shown.



Our analogue for this is a positive feedback amplifier with a pti of the same value, and the input passing through an input stage consisting of a pti before the feedback sum junction is reached. This will have the same response and diagram as above; but the problem for the intuition is that one would expect that a 'pulse-to-come' would create an infinite series of pre-pulses, not an an infinite series of post-pulses. The reason for this is that each of the post-pulses consists of the superimposed sine waves of appropriate frequency and phase. *Before* the stimulus pulse arrives, these sine waves cancel completely, but this cancellation is marred by the arrival of the stimulus pulse, which results in the chain of post-pulses normally seen.

From Fourier's Transform Theorem, linearity and the two identical sine wave formulae just shown, we know the outputs will be identical to those illustrated in the spike diagram.

Many people will feel very uneasy about including an impossibility in a circuit diagram, since this is something that cannot possibly be made. But, a perfect opamp can also not be made, yet it is frequenctly used in circuits. The opamp characteristic is approached closely, but never realized. In fact, we could argue that the utility of any opamp comes from the fact that the opamp cannot be made perfect, since we ensure in practice that external components determine the characteristic of the device. That is, the idealization serves a pedagogic and practical purpose. Similarly, a negative impedance is a dependent object, only defined where larger positive impedances exist, since the negative impedance would charge the power supply from no source: another impossibility. However, the understanding of oscillators was greatly facilitated by models using negative impedance. Similarly, positive time increments can exist only where there are normal time delays; they can be constructed by designing some of the circuit to have less delay than the rest. The theoretical utility remains however.

Fixed and passive components

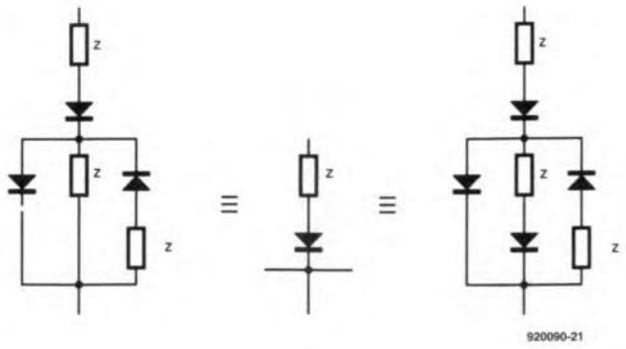
Let us define a passive circuit recursive definition for a perfect diode; for any value of Z—see Fig.11; and for an inverter, assuming we have a voltage summing circuit—see Fig. 12.

We can use the equivalence in Fig. 13, so that

out+in+f(out)+out+out=out

and

11



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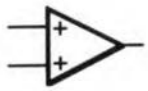
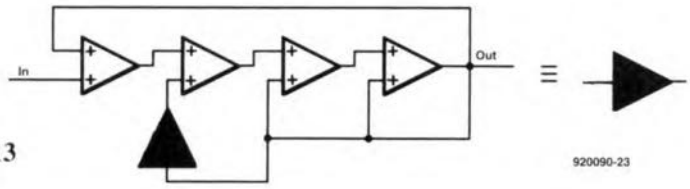


voltage summing circuit



13

f(in) = out.

In+F(out)+2out=0,

so that

in+f^2(in)+2f(in)=0.

Let in=x and $f(x)=a_1x+a_2x^2+a_3x^3+\ldots$

$x(a_1y+a_2y^2+a_3y^3)+2(a_1x+a_2x^2+a_3x^3\ldots)=0$,

and

$y^2=a_1(a_1x+a_2x^2)+a_2(a_1x+a_2x^2)+a_3(a_1x+a_2x^2)+\ldots$

Equating the coefficients gives

$1+a_1^2+2a_i=0$,

which implies

$a_1=-1$; $a_i=0$; and i>1.

Thus, $f(x)=-x$, and we have recursively defined an inverter.

Having defined an inverter, we can define a voltage-sum device (where output, $V=V_1+V_2$ at the inputs—see Fig. 14).
That is,

$f[f$(out, in), out]=out,

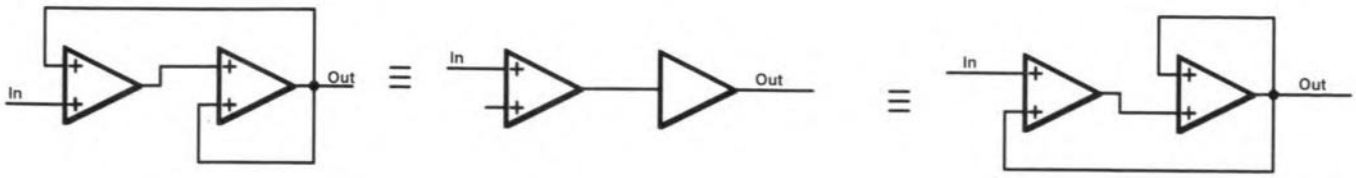
and

f(in, 0)=–out.

Thus, $y=f[f(y, x), y]$

and $-f(x, 0)=y$.

From this, the rule f(in, 0)=–in can be deduced (see note at end).



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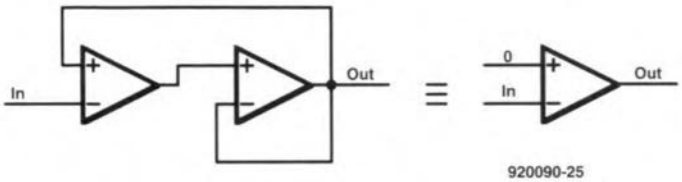
We may also define an opamp-like device: by a similar strategem:



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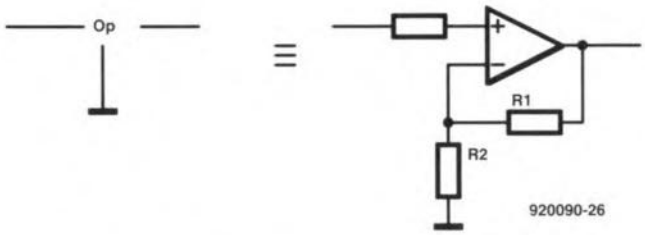
The usual opamp circuit:



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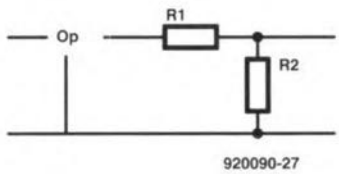
has a gain of $(R_1+R_2)/R_2$. Thus,



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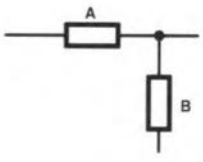
has a gain of 1. Therefore, we may describe the non-inverting mode of a *y* opamp as the inverse of a potential divider (which takes no current and is unloaded from a low impedance source).

In a repeated potential divider,



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let $r=B/(A+B)$; the new voltage ratio will be $Br^2/(B+Ar^2)$. When $A=B$, the sequence

$$1/2,\ 1/5,\ 1/13,\ 1/34,\ \ldots$$

is obtained for this cascaded potential divider. The sequence is the reciprocal of every other term of the Fibonacci series. The matrix (un-augmented A-matrix)

$$\begin{bmatrix} 2 & R \\ 1/R & 1 \end{bmatrix} = M$$

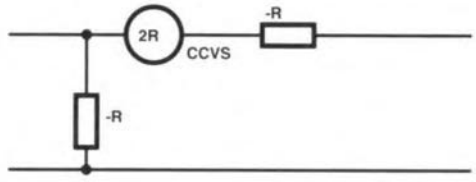
$$\begin{bmatrix} 5 & 3R \\ 3/R & 2 \end{bmatrix} = M^2$$

$$\begin{bmatrix} 13 & 8R \\ 8/R & 5 \end{bmatrix} = M^3$$

represents the situation. Note that the 0^{th} term of the series is

$$\begin{bmatrix} 1 & R \\ 1/R & 0 \end{bmatrix}$$

which is a matrix interesting in any case. It has the equivalent circuit



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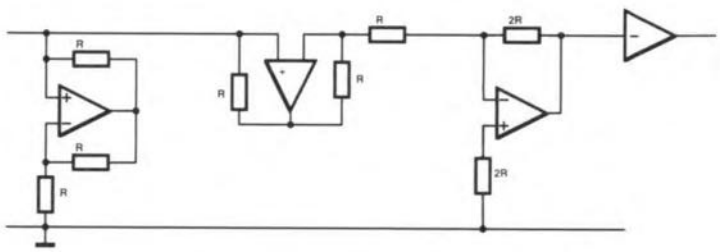
The practical circuit would be



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However, here we are concerned mainly with iterative schemes:

$$M_0 = \begin{bmatrix} 1 & R \\ 1/R & 0 \end{bmatrix}$$

Any voltage divider can then be written

$$\begin{bmatrix} 1 & \pm xZ \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & Z \\ 1/Z & 0 \end{bmatrix}^2$$

But consider first the iterated voltage divider with equal arms; let SET be the set we have:

$M_0 \varepsilon$ SET,

and if

$M \varepsilon$ SET, $MM_0 \varepsilon$ SET also.

Let

$$M_{-1}=M_0^{-1}.$$

We then have the iterative scheme:

1. M_0 is a potential divider of this sort;
2. $M_{-1}MM_0=M$.

Thus, we can characterize potential dividers by the extended scheme:

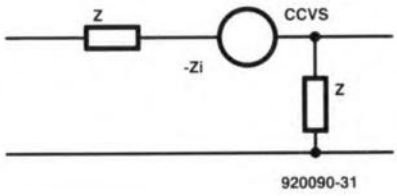
$$\begin{bmatrix}1 & xZ\\ 0 & 1\end{bmatrix} = X_X, \text{ where } x \text{ is real.}$$

1. $M_0 \varepsilon$ SET;
2. $M \varepsilon$ SET $\Rightarrow$ $X_x M \varepsilon$ SET;
3. $M_{-1}MM_0=M$;
4. These are all, the smallest set defines them.

Hence, we have recursively defined a set of potential dividers. Some types of active circuit can be defined as the inverse of this class.

Let $X_x M_0^n=A$ be a potential divider; the A^{-1} is a non-inverting opamp of a certain type. Thus, we can also recursively define opamp circuits:

M_0^{-1} is



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whose matrix is:

$$\begin{bmatrix}0 & Z\\ 1/Z & -1\end{bmatrix}$$

Thus, A^{-1} is $M_0^{-n}X_x^{-1}$ and

$$\begin{bmatrix}1 & xZ\\ 0 & 1\end{bmatrix}^{-1} = \begin{bmatrix}1 & -xZ\\ 0 & 1\end{bmatrix}$$

$$M_0^{-2n} = \begin{bmatrix}F_{n+1} & -F_nZ\\ -F_n/Z & F_{n-1}\end{bmatrix} \text{ where } F_n \text{ are the Fibonacci series.}$$

$$M_0^{-2n}X_x^{-1} = \begin{bmatrix}F_{n+1} & -xZF_{n+1}-F_nZ\\ -F_n/Z & F_{n-1}+xF_n\end{bmatrix}$$

Let us choose specific values for x and see what types of circuit emerge; the result may be constructive of a new approach. A negative value of x may be chosen to make a_{12} zero or a_{22} zero, so that we can choose either infinite mutual conductance or infinite current gain. If we choose infinite current gain, we are close to the opamp characteristic, choosing Z negative for this non-inverting case. The method can also be used for other circuit elements, for example, the ideal full rectifier obeys these rules—see below and Fig. 23. Clearly, the

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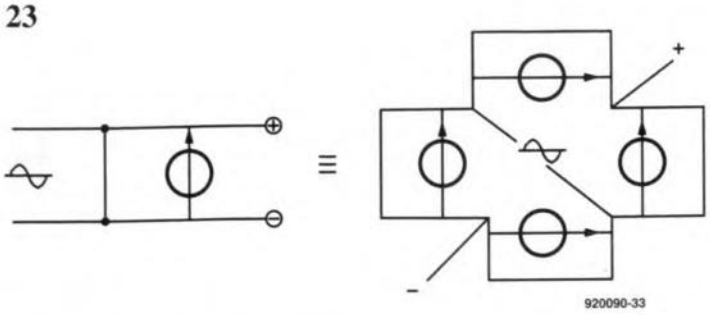

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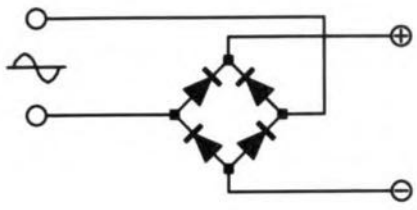
circuit is a form of idempotent.

The question of whether these relations are definitive must be checked and, in fact, the definition of a single diode can be used to define these by the obvious method:



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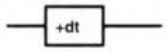
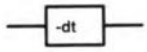
Here are some more facts—ptis again:

Let 

denote a pti with positive time increment of dt, and 

a normal time delay. Then,

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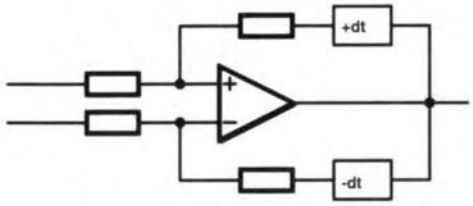
but a parallel connection is more fraught!



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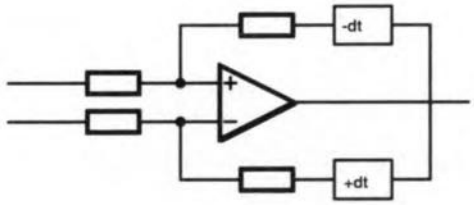
is unstable, whereas



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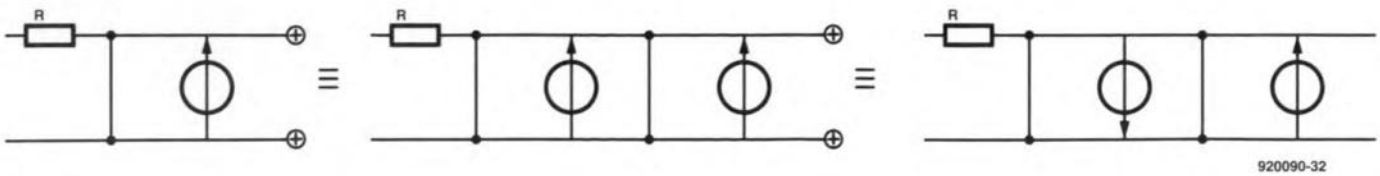
is, in some circumstances, not.



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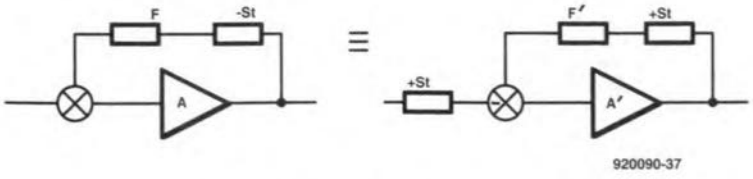
The simple relation



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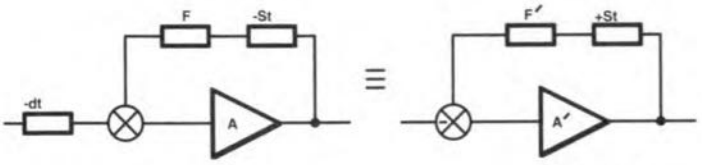
can be used to simulate the effect of a postive time increment element in feedback, since

$A'=g^{-1}$ and $F'=A^{-1}$.



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The effect is very baffling to understand for those waveforms that require an infinite number of Fourier components to synthesize them, but straightforward for single frequencies. The advantage is that a single frequency emerges with changed phase and can, therefore, be used to form a building block for any other waveform. ■

Note. Consider the conditions

$y=f[f(y, x), y]$ and $f(x, 0)=-y$.

From symmetry it can easily be shown that

$f(0, 0)=0$ and $f(x, y)=f(y, x)$.

Next consider

$f(x, y)=x+y$.

We then have $-y=x$ and $y=[(y+x)+y]$, which fit the two equations; thus, $f(x, y)=x+y$ is one answer.

Now consider $f(x, y)=x+y+\mathrm{d}(x, y)$ and let $\mathrm{d}(x, y)=ax+ay+bxy$ approximately for x, y very small. Then,

$$\mathrm{d}[x+y+\mathrm{d}(x, y), y]=-x-y-\mathrm{d}(x, y)$$

produces the result that $a=-1$, so that $-(cxy)-y+c(cxy^2)=-cxy$, which is impossible because x, y, though small, can vary independently of xy. The solution to this is that $\mathrm{d}(x, y)=0$.

Thus, $f(x, y)=x+y$.

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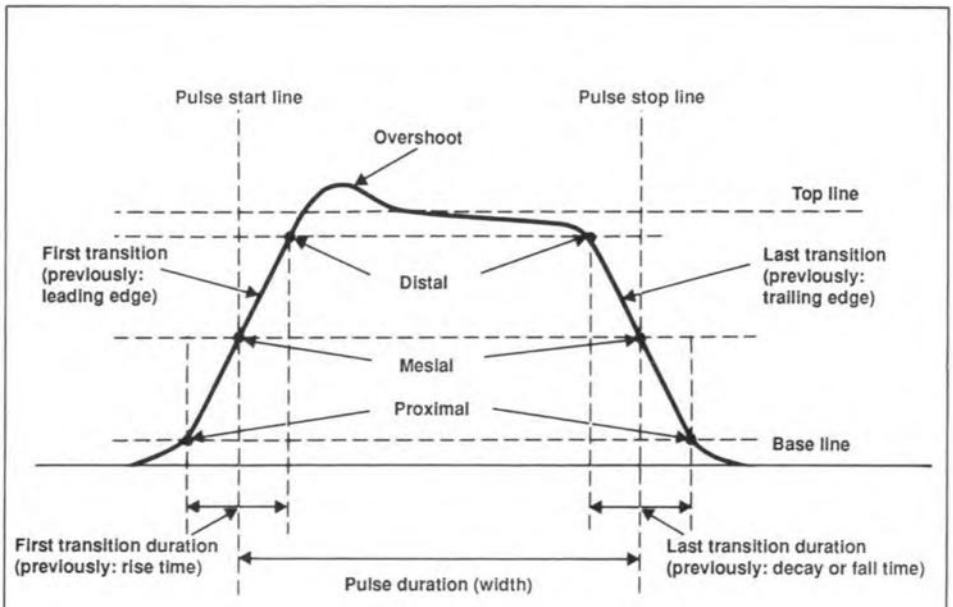
Anatomy of a practical pulse



Anatomy of a practical pulse

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When it comes to describing a 'simple' pulse, or properties thereof, technical literature is sprinkled with vague, misleading and ambiguous terms and definitions. What, for instance, does 'positive edge' mean when applied to a negative pulse? Is it the 'positive-going' edge, that is, in this case, the last transition, often called the 'trailing edge', or is it the first transition, often called 'leading edge'?

Why this confusion of terms and definitions has arisen is not clear. Both the British Standards Institution and the International Electrotechnical Commission have laid down agreed international terms and definitions, which are incorporated in the adjacent drawing. Further details may be obtained from British Standard BS 5698:1989 or IEC Standard IEC 469-1:1987. This magazine will continue using the standard terms and definitions applying to a pulse, although for a period the colloquial terms will be added in brackets where deemed necessary.

Note also that the term 'duty cycle' is not used in connection with pulses; the correct term for the ratio of the pulse duration (width) to the pulse repetition period (pulse spacing) of a periodic pulse train is 'duty factor'.

USING THE MAR-X SERIES OF VERY WIDEBAND MONOLITHIC MICROWAVE INTEGRATED CIRCUITS (MMIC)

BUILDING YOUR OWN VLF TO MICROWAVE BROADBAND AMPLIFIER

Very wideband amplifiers have a bandpass (frequency response) of several hundred megahertz, or more, typically ranging from sub-VLF to the low end of the microwave spectrum. An example might be a range of 100 kHz to 1,000 MHz (i.e., 1 GHz), although somewhat narrower ranges are more common. These circuits have a variety of practical uses: receiver preamplifiers, signal generator output amplifiers, buffer amplifiers in RF instrument circuits, cable television line amplifiers, and many others in communications and instrumentation. Unfortunately, as valuable as they are, they were not found in many electronics hobbyist situations until recently(1). One of the reasons that very wideband amplifiers are rarer than narrower band amplifier circuits is that they are difficult to design and build. A daunting technical task indeed.

By Joseph J. Carr

SEVERAL factors contribute to the difficulty of designing and building very wideband amplifiers. For example, there are too many stray capacitances and inductances in a typical circuit layout, and these form resonances that distort the frequency response characteristic. There are also circuit resistances that combine with the capacitances to effectively form low-pass filters that roll off the frequency response at higher frequencies, sometimes drastically. If the *R-C* phase shift of the circuit resistances and capacitances is 180 degrees at a frequency where the amplifier gain is ≤1 (and in very wideband circuits that is likely), and the amplifier is an inverting type (producing an inherent 180 degree phase shift), then the total end-to-end phase shift is 360 degrees — which is one of the criteria for self-oscillation.

If you have ever tried to build a very wideband amplifier, it was likely to be a very frustrating experience. Until now. Because of new, low-cost devices called silicon monolithic microwave integrated circuits (MMICs), reportedly developed in large part for the benefit of the cable television industry, it is possible to design and build amplifiers that cover the spectrum from near-DC to about 2,000 MHz, and that use seven or fewer components. These devices offer gains of 13 to 30 dB of gain (see Table 1), and produce output power levels up to 40 mW (+16 dBm). Noise figures range from 3.5 to 7 dB. Although several manufacturers offer products, those of Mini-Circuits (P.O. Box 350166, Brooklyn, NY, 11235-0003, USA) are the most easily obtained by electronics hobbyists and amateur radio operators. In this article we will examine the low-cost MAR-x series of MMIC amplifiers.

Drop-in amplifiers

Figure 1a shows the circuit symbol for the MAR-x devices. Note that it is a very simple device. The only connections are RF

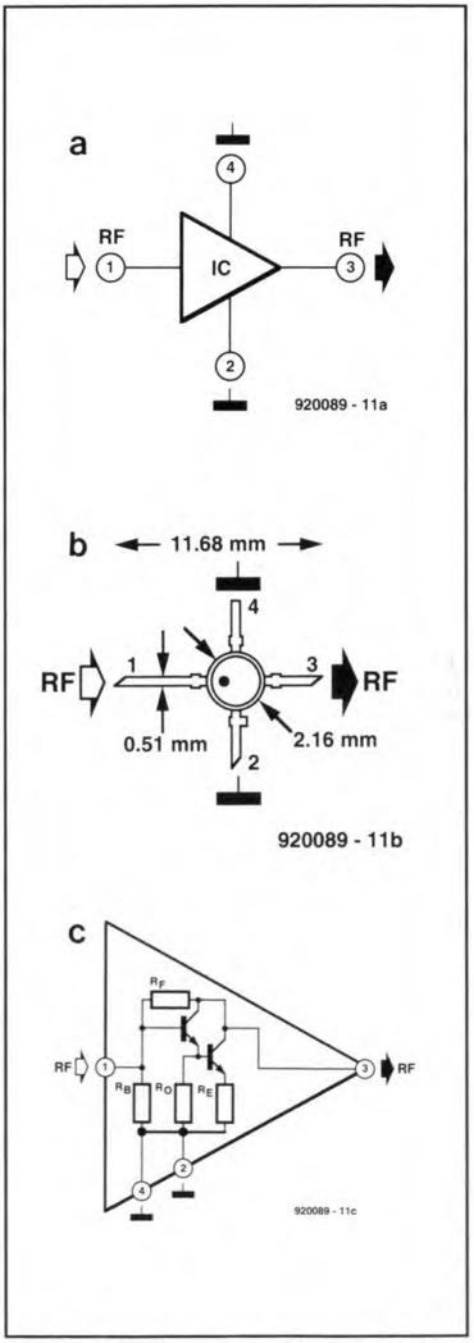


Fig. 1. (a) MAR-x circuit symbol; (b) MAR-x device package; (c) MAR-x internal circuitry.

(1). Note, however, that an article called 'MMICs revolutionize wideband RF amplifier design' was published in the January 1988 issue of *Elektor Electronics*. This introductory article was followed by a number of construction projects based on Avantek's MSA series of MMICs. (*Tech. Ed.*)

Table 1. Device selection overview

Type number	Colour dot	Gain (500 MHz) [dB]	Max. freq.
MAR-1	brown	17.5	1000 MHz
MAR-2	red	12.8	2000 MHz
MAR-3	orange	12.8	2000 MHz
MAR-4	yellow	8.2	1000 MHz
MAR-6	white	19	2000 MHz
MAR-7	violet	13.1	2000 MHz
MAR-8	blue	28	1000 MHz

input, RF output and two ground connections. The use of dual grounds distributes the grounding, reducing overall inductance and thereby improving the ground connection. Direct current (d.c.) power is applied to the output terminal through an external network. But more of that shortly.

The package for the MAR-x device is shown in Fig. 1b. Although it is an IC, the device looks very much like a small UHF/microwave transistor package. The body is made of plastic, and the leads are wide metal strips (rather than wire) in order to reduce the stray inductance that narrower wire leads would exhibit. These devices are small enough that handling can be difficult; I found that hand forceps ('tweezers') were necessary to position the device on a prototype printed circuit board. A magnifying glass or jeweler's eye loupe are not out of order for those with poor close-in eyesight. A color dot, and a beveled tip on one lead, are the keys that identify pin no. 1 (which is the RF input connection). When viewed from above, pin numbering (1,2,3,4) proceeds counter clockwise from the keyed pin.

Internal Circuitry

The MAR-x series of devices inherently matches 50 ohm input and output impedances without external impedance transformation circuitry, making it an excellent choice for general RF applications. Figure 1c shows the internal circuitry for the MAR-x devices. These devices are silicon bipolar monolithic ICs in a two transistor Darlington amplifier configuration. Because of the Darlington connection, the MAR-x devices act like transistors with very high gain. Because the transistors are biased internal to the MAR-x package, the overall gains are typically 13 to 33 dB, depending on the device selected and operating frequency. No external bias or emitter bias resistors are needed, although a collector load resistor to V_+ is used.

The good match to 50 Ω for both input and output impedances (R) is due to the circuit configuration, and is approximately:

$$R = \sqrt{R_f R_E} \qquad (1)$$

If R_f is about 500 Ω, and R_E is about 5 Ω, the square root of their product is the desired 50 Ω.

Basic circuit

The basic circuit for a wideband amplifier project based on the MAR-x device is shown in Fig. 2. The RF IN and RF OUT terminals are protected by DC blocking capacitors C1 and C2. For VLF and MW applications, use 0.01-µF (10-nF) disk ceramic capacitors, and for HF through the lower VHF (≥ 100 MHz) use 0.001-µF (1-nF) disk ceramic capacitors. But, if the project must work well into the high VHF through low microwave region (>100 MHz to 1000 MHz or so), then opt for 0.001-µF (1-nF) 'chip' capacitors. If there is no requirement for lower frequencies, chip capacitors in the 33 to 100 pF range can be used.

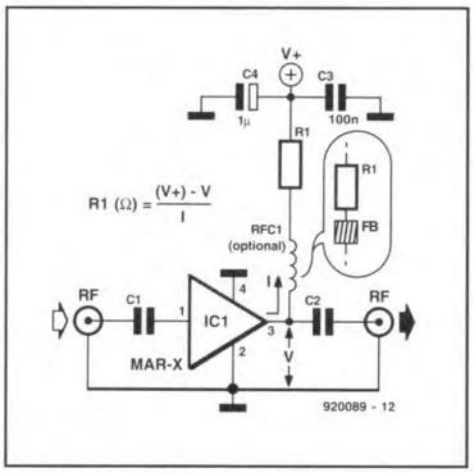


Fig. 2. Generic MAR-x circuit.

The capacitors used for C1 and C2 should be chip capacitors in all but the lower frequency (<100 MHz) circuits. Chip capacitors can be a bit bothersome to use, but their use pays ever greater dividends as operating frequency increases.

Capacitor C3 is used for two purposes. It will prevent signals from A1 from being coupled to the d.c. power supply, and from there to other circuits. It will also prevent higher frequency signals and noise spikes from outside sources from affecting the amplifier circuit. In some cases, a 0.001-µF (1-nF) chip capacitor is used at C3, but for the most part a 0.01-µF (10-nF) disk ceramic will suffice.

The other capacitor at the d.c. power supply is a 1-µF tantalum electrolytic. It serves to decouple low frequency signals, and smooth out short duration fluctuations in the DC supply voltage. Higher values than 1 µF may be required if the amplifier is used in particularly noisy environments.

Direct current is fed to the amplifier through a current limiting resistor (R1), via the RF OUT terminal on the MAR-x (lead no. 3). The maximum allowable d.c. potential is +7.5 V for MAR-8, +5 V for MAR-1 through MAR-4, +4 V for MAR-

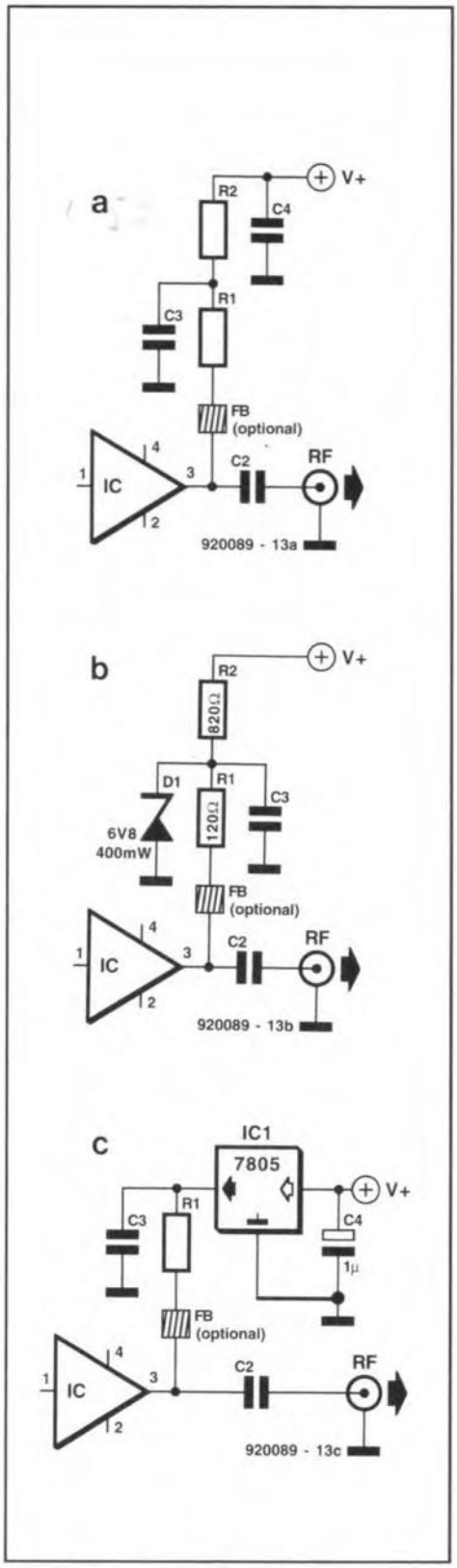


Fig. 3. Power supply schemes: (a) simple resistor circuit; (b) zener-stabilized circuit; (c) three-terminal 5-V voltage regulator stabilized.

7, and +3.5 V for MAR-6. If a minimum voltage V+ power supply is used, e.g. +5 V for MAR-1, make R1 a 47 Ω to 100 ohm resistor. Use only ¼-watt or ½-watt non-inductive resistors, such as the carbon composition or metal film types. The use of higher V_+ potentials (e.g. +9 to +12 V) is necessary, use a higher value non-inductive resistor for R1. To determine the value of R1, decide on a current level (I), and do an Ohm's law calculation:

$$R_1 = \frac{(V_+ - V)}{I} \qquad (2)$$

where R is in ohms. In most cases, a good operating current level for the popular MAR-1 is about 15 mA (or 0.015 A).

An example: when a MAR-1 circuit is to be powered from +9-V transistor radio battery, and a device current of 15 mA is required, the theoretical value of R is (9–5)/0.015 = 267 Ω.

In practice, a 270-ohm resistor is used.

An optional inductor, RFC1, is shown in the circuit of Fig. 2. This inductor serves two purposes. First, it improves the decoupling isolation of the MAR-x output from the DC power supply by blocking RF signals. Second, it acts as a 'peaking coil' to improve gain on the high frequency end of the frequency response curve. It does this latter job by adding its inductive reactance (X_L) to the resistance of R1 to form a load impedance that increases with frequency because $X_L = 2\pi FL$. Depending on application, suitable values of inductance range from less than 0.5 µH to about 100 µH, depending on the application and frequency range. Sometimes, however, the coil forms the total load impedance. In those cases, a decoupling capacitor is used at the junction of RFC1 and R1.

Inductor coils are not without problems in very wideband amplifiers because the stray capacitances between the coil windings form unintended self-resonances with the coil inductance. These resonances can distort the frequency response curve and may cause oscillations. A popular solution to this problem is to use a small ferrite bead ('FB' in the inset to Fig. 2). The bead acts as a small-value RF choke. These beads have a small hole in them that fits nicely over the radial lead of a ¼-watt resistor.

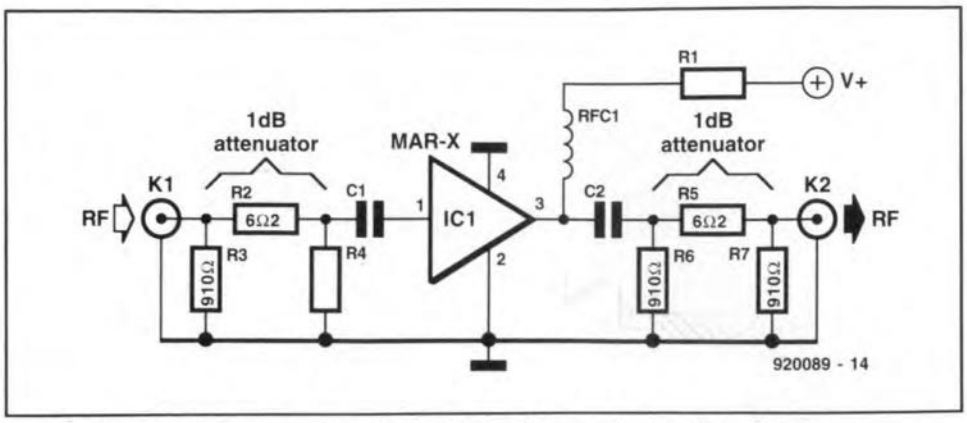


Fig. 4. Use of in-line 1-dB attenuators to stabilize input and output impedances.

Alternative DC power schemes are shown in Fig. 3. The circuit of Fig. 3a splits the load resistance into two components, R1 and R2. The value of R1 will represent most of the required resistance, with R2 typically being 33 to 100 Ω. This circuit, like the basic circuit, works well to V_+ voltages of 7 to 9 V, but is not recommended for $V_+ > 9$ V.

Power feed schemes that work well at V+ voltages greater than 9 V are shown in Figs. 3b and 3c. Both use voltage regulation to stabilize the supply voltage to the MAR-x device. In Fig. 3b, a 6.8-V zener diode holds the voltage applied to R1 constant, and within acceptable range, despite fluctuations in the source V_+ potential.

Other MAR-x circuits

The simple circuit of Fig. 2 will work well in most cases, especially where the input and output impedance are reasonably stable. But if the input source or output load impedances vary, the amplifier may suffer a degradation of performance, or show some instability. One solution to the problem is to use resistive attenuator pads in the input and output signal lines. Attenuators in an amplifier circuit? Yes, that's right. A 1-dB or 2-dB attenuator in the input and output signal lines will pseudo-stabilize the impedances seen by the amplifier, but only marginally affects the overall gain of the circuit. In vacuum tube days, we called this type of technique 'swamping'.

Figure 4 shows the circuit of Fig. 2 revised to reflect the use of simple resistive attenuator pads in the input and output lines. With resistor values of 6.2 Ω for the series element, and 910 Ω for the two shunt lines, the attenuation factor is 1 dB. A 2-dB version uses 12 Ω and 470 Ω, respectively. If 1-dB attenuators are used, the overall gain is the natural gain of the MAR-x device less 2 dB (or 4 dB if 2-dB attenuator pads are used). The resistors used for these attenuator pads must be non-inductive types, such as carbon composition or metal film types. If the amplifier is to be used at the higher end of its range, chip resistors are preferable to ordinary axial lead resistors.

An alternative approach is to use manufactured shielded RF 50-Ω attenuator pads. Another of Mini-Circuits products are the AT-1 and MAT-1 1-dB attenuators; they are suitable for the purpose, and match the frequency range of most of the MAR-x products. These low-cost devices are similar except for size, and are intended for mounting on printed circuit boards.

Keep in mind that the use of attenuators is not for free (TANSTAFL principle: *There Ain't No Such Thing As a Free Lunch*). The resistive attenuators reduce the gain (as mentioned before), but also increase the noise factor by an amount set by the loss factor of the attenuator pad.

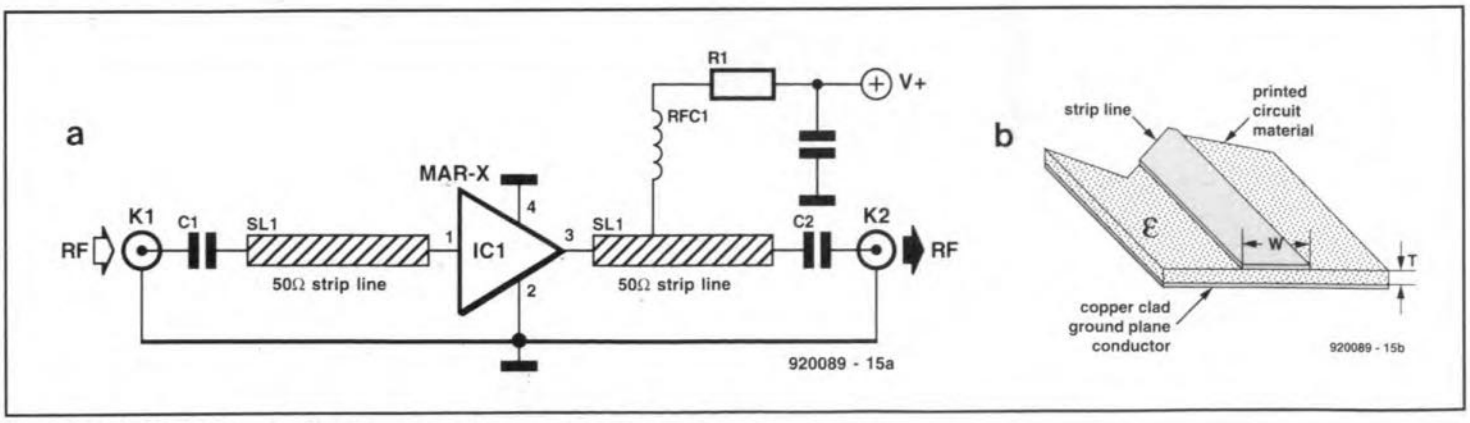


Fig. 5. (a) MAR-x amplifier with strip line input and output circuits; (b) strip line detail.

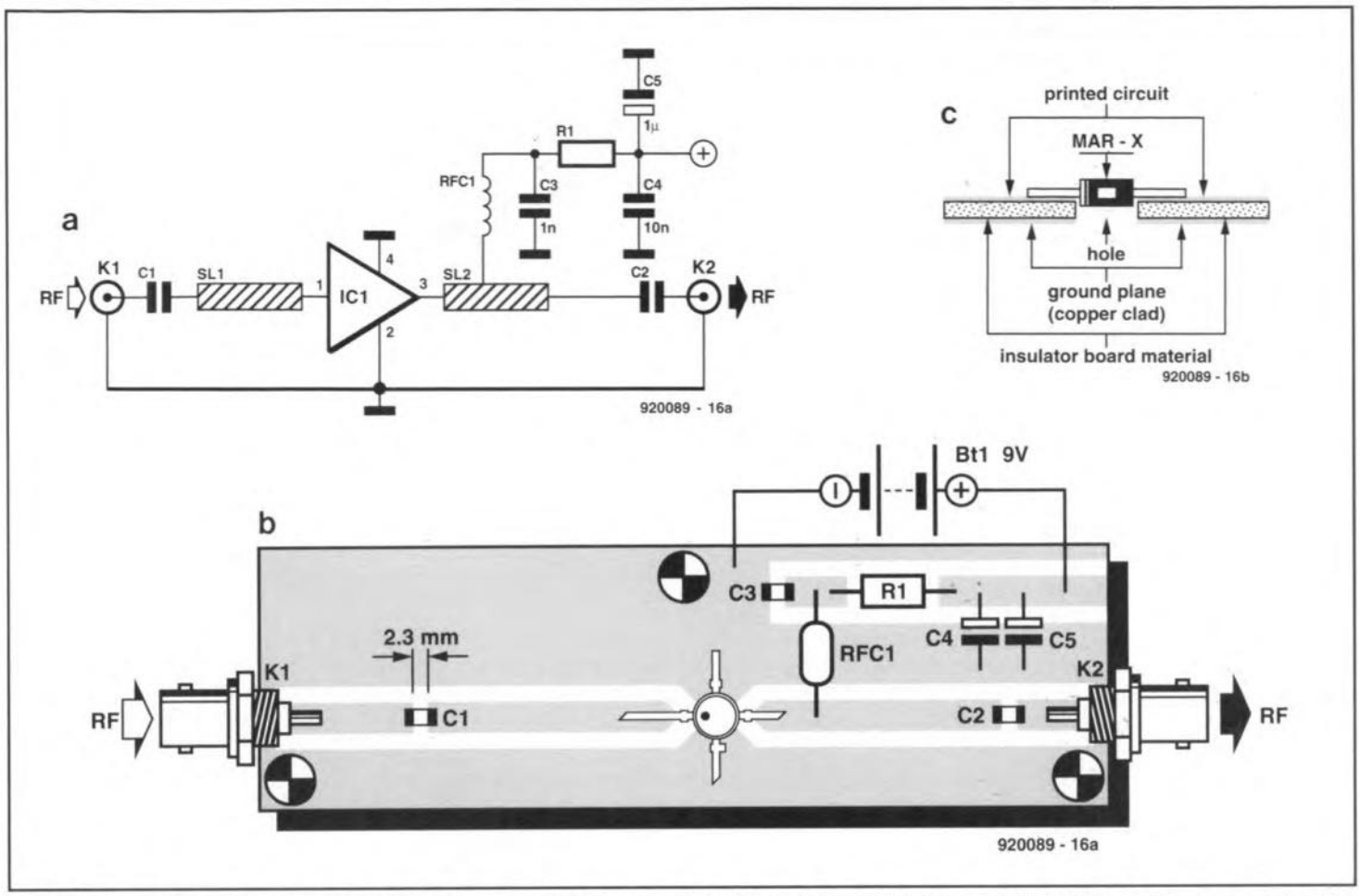


Fig. 6. (a) Typical circuit diagram and (b) PCB layout for a MAR-x amplifier; (c) a hole is cut into the printed circuit board to accommodate the MAR-x body.

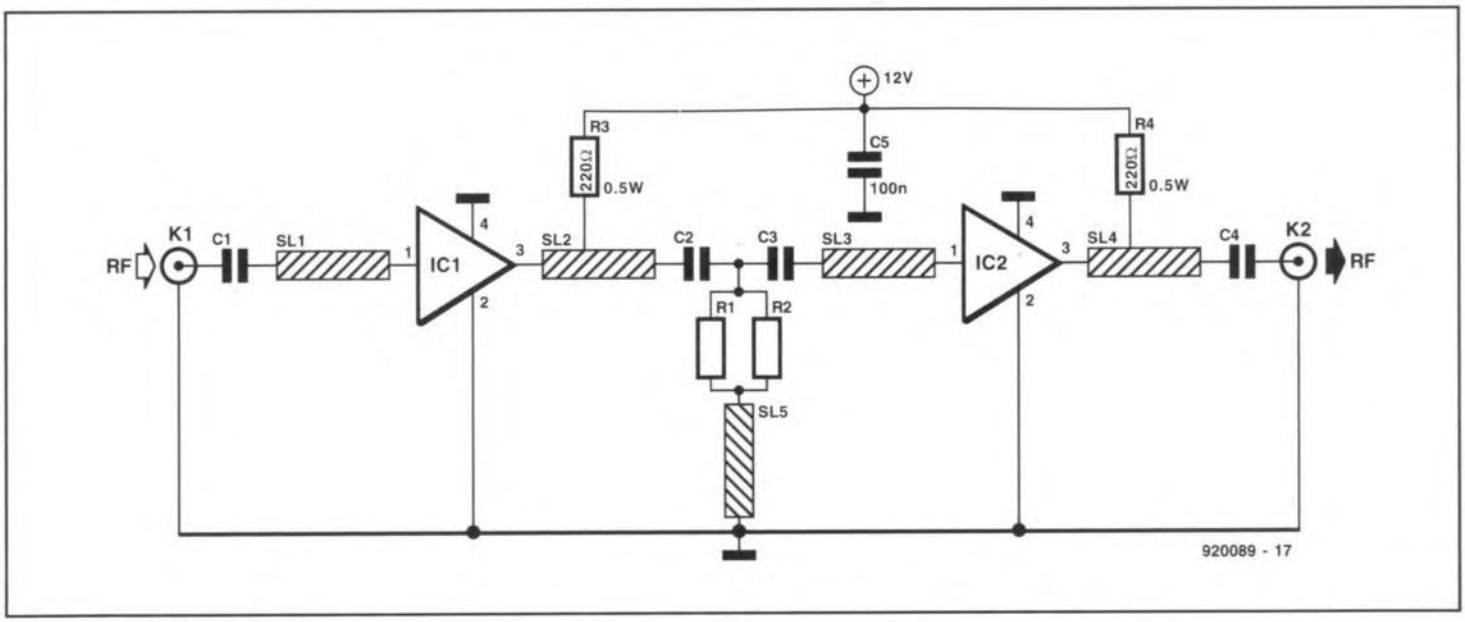


Fig. 7. Cascade MAR-8 amplifier.

For VHF, UHF and low-end microwave amplifiers it may be preferable to use a printed circuit strip line transmission line for the input and output circuits. Figure 5a shows such a circuit with input (SL1) and output (SL2) strip lines, while Fig. 5b shows detail of how these lines are made. The characteristic impedance (Z_o) of the line is a function of the relative dielectric constant of the printed circuit material (ε_r), the thickness of the material (*T* in Fig. 5b), and the width (*W* in Fig. 5b) of the strip line conductor. Common epoxy G-10 printed circuit boards ($\varepsilon_r \approx 4.8$) are usable to 1000 MHz and work well to about 300 MHz. Above 300 MHz the losses increase significantly. PTFE woven glass fiber printed circuit board ($\varepsilon_r \approx 2.55$) operate to well over 2,000 MHz, which is higher than the upper limit of the MAR-x devices. Widths required for 50 Ω strip lines for various printed circuit board materials are shown in Table 2.

Figure 6b shows the circuit layout of a typical printed circuit board for a MAR-x wideband amplifier. The circuit for the layout is shown in Fig. 6a. The printed circuit board should be double clad, i.e., clad with copper on both top and bottom. The strip lines at the input and output are etched from the component side of the printed circuit material, not the bottom

side as is common practice in lower frequency projects. The reason for this approach is to reduce the inductance of the leads to the MAR-x device.

Strip lines should not contain abrupt discontinuities, or else parasitic losses will increase. It is common practice to taper the line over a short distance from the strip line to the width of the MAR-x leads right at the body of the device.

Another tactic to keep stray lead inductances to a minimum is to drill a small hole in the printed circuit to hold the body of the MAR-x (Fig. 6b). The diameter of the MAR-x package is 0.085 inch (approx. 2.15 mm), and the hole should be only slightly larger.

The capacitors in the input and output circuit, as well as the decoupling capacitor at the junction of RFC1 and R1, are chip capacitors. The break in the strip line to accommodate these capacitors should be just wide enough to separate the ohmic contacts at either end of the capacitor body. For the 1-nF (0.001 µF) chip capacitors that I used in making a model in preparation for this article, the insulated center section between contacts on the capacitors averaged 0.09 inch (2.3 mm) as measured on a vernier caliper set.

It is essential to keep ground returns as short as possible, especially when the amplifier operates at the higher end of its range. If you opt to use the ground plane cladding for the d.c. and signal return, plated through holes are required between the two sides of the board. These plated through holes must be placed directly below the ground leads of the MAR-x package.

Multiple device circuits

The MAR-x devices can be connected in cascade, parallel or push-pull. The cascade connection increases the overall gain of the amplifier, while the parallel and push-pull configurations increase the output power available.

The simplest cascade scheme is to connect two stages such as Fig. 2 in series so that the output capacitor of the first stage becomes the input capacitor of the second stage. Figure 7 shows a somewhat better approach. This circuit uses strip line matching sections at the inputs and outputs, and between stages. Table 3 gives the dimensions of these lines for two different cases: Case-A is for a 100 to 500 MHz amplifier, and Case-B is for a 500 to 2,000 MHz amplifier. In both cases the MAR-8 device is used.

The parallel case is shown in Fig. 8. MAR-x devices can be connected directly in parallel to increase the output power capacity of the amplifier. In the case of Fig. 8, there are four MAR-x devices connected in parallel. Other combinations are also possible. I built a two-up version for a signal generator output stage recently. The output power in Fig. 8 will be four

Table 2. Values for 50-Ω strip line (see Fig. 5b)

Material	ε_r	*T*	*W*
G-10 epoxy fiberglass	4.8	0.062 in. 1.58 mm	0.108 in. 2.74 mm
PTFE woven glass fiber	2.55	0.010 in. 0.254 mm	0.025 in. 0.635 mm

Table 3. Cascade amplifier design details (see Fig. 7)

Component	Case-A	Case-B
R1	124 Ω	69.1 Ω
R2	69.8 Ω	69.1 Ω
C1, C4	470 pF	68 pF
C2	1.5 pF	2 pF
C3	7.5 pF	2 pF
Capacitors are chip type. Resistors are 1% chip type.		
	W × L	W × L
SL1	0.1 × 0.1 in. 2.54 × 2.54 mm	0.04 × 0.1 in. 1.02 × 2.54 mm
SL2	0.1 × 0.05 in. 2.54 mm × 1.27 mm	0.04 × 0.1 in. 1.02 × 2.54 mm
SL3	0.1 × 0.2 in. 2.54 × 5.08 mm	0.04 × 0.1 in. 1.02 × 2.54 mm
SL4	0.1 × 0.1 in. 2.54 × 2.54 mm	0.04 × 0.1 in. 1.02 × 2.54 mm
SL5	0.05 × 0.2 in. 1.27 × 5.08 mm	0.05 × 0.2 in. 1.27 × 5.08 mm

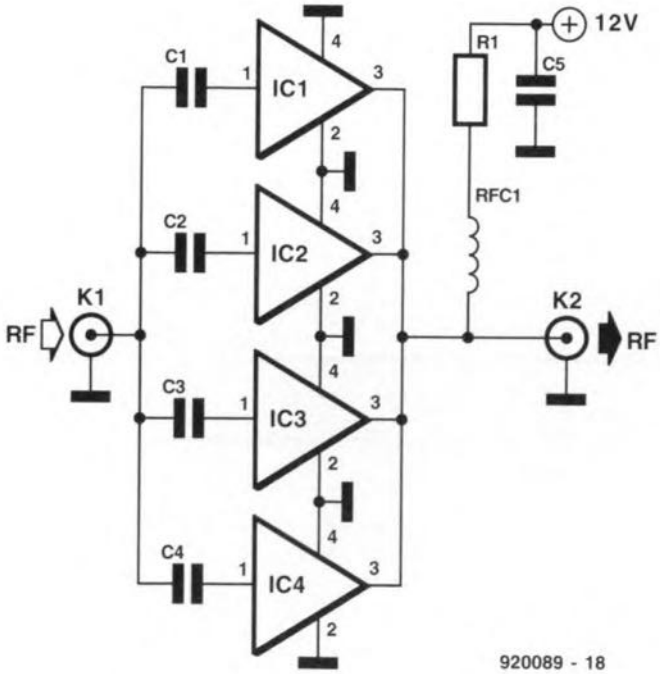


Fig. 8. Parallel combination increases output power fourfold for same gain, but cuts input and output impedances by four.

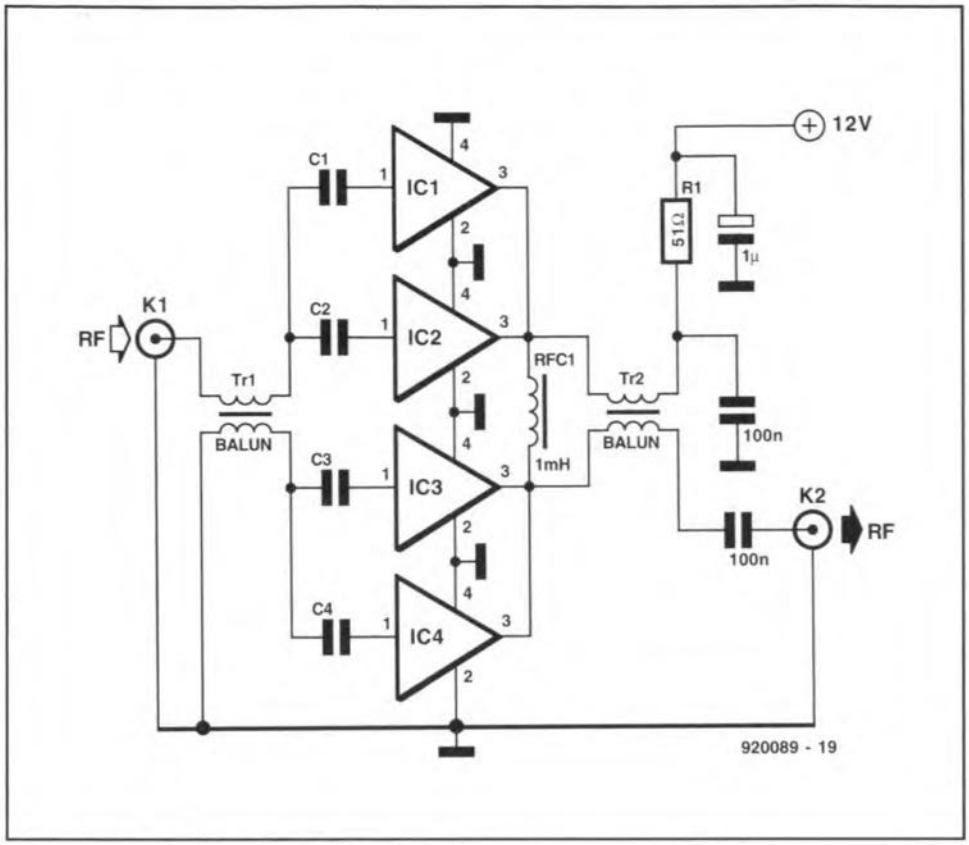


Fig. 9. Parallel push-pull amplifier.

times the power available from a single device.

Unfortunately, in the parallel amplifier the input and output impedances are no longer 50 Ω, but rather it is 50/*n* where *n* is the number of devices connected in parallel. In the case shown in Fig. 8, there are four devices to the input and output impedances are 50/4 or 12.5 Ω. An impedance matching device must be used to transform the lowered impedances to the 50 Ω standard for RF systems. Because most impedance transformation devices do not have the same wide bandwidth as the MAR-x devices, there is an obvious degradation of the bandwidth of the overall circuit.

The push-pull configuration is shown in Fig. 9. In this circuit there are two banks of two MAR-x devices each. The two banks are connected in push-pull, so this circuit is correctly called a push-pull parallel amplifier. This circuit retains gain and the increase in power level of the parallel connection, but improves the second harmonic distortion that some parallel configurations exhibit. Push-pull amplifiers inherently reduce even-order harmonic distortion.

The input and output transformers (T1 and T2) for the circuit of Fig. 9 are balun (BALanced UNbalanced) types, and are used to provide a 180-degree phase shift of the signals for the two halves of the amplifier. The balun transformers are typically wound on ferrite toroidal coil forms with #26 AWG or finer wire. Because the balun transformers are limited in frequency response, this circuit is typically used in medium wave and shortwave applications. A common specification for these transformers is to wind 6 or 7 bifilar turns on a toroidal form, the turns made of #28 AWG enameled wire wrapped together to form a twisted pair of about five twists to the inch (≈ 2 twists per cm). Suitable cores (and a catalog) are available from Amidon Associates (P.O. Box 956, Torrance, CA 90508, USA).

Conclusion

The MAR-x devices are an extremely easy way to build RF amplifiers from frequencies near d.c. to the low microwave region. They are easy to use, and well behaved. Hobbyists will find them very convenient for a wide variety of applications. ■

ULTIMATE CHALLENGER — A REVIEW

Ultimate Technology's Ultiboard and Ulticap

92059

By David J. Silvester

ABOUT a year ago I reviewed the Boardmaker2 software for the drawing of schematics and PCB layouts. This package does not allow the schematic unit to produce netlist information that can be passed on to the PCB drawing unit. Ultimate Challenger system purports to overcome this problem and is the subject of this review. The Ultimate Challenger consists of two units: the schematic capture, Ulticap, and the PCB drawing software, Ultiboard.

The design cycle

To assess any electronics design package, it is necessary to understand the idea of the design cycle to appreciate the usability of a piece of software to the electronics engineer. Having the design idea on a number of sheets of paper, the computer aided design (CAD) package comes into use.

Briefly, the schematic is drawn into the computer, giving all of the information for any device that may be needed. The wires will then be drawn on to complete the schematic. The schematic is captured, i.e., the schematic drawing along with all of the package details are converted into a form that the PCB layout software can understand. The package file and the netlist file are called to provide all of the layout shapes and connection details for the PCB. The board is then laid out, and the tracks drawn using whatever facilities best suit the designer.

It is very rare that a board will not need to be modified at some stage, and any good computer aided design package should have the necessary software so that modifications to the PCB can be put back into the schematic. The details of these changes need to be included on the schematic, or the service engineer will find it almost impossible to repair the board. Thus, the design cycle runs from schematic through PCB to schematic to ensure continuity at all stages.

Cost

Ultimate Technology offer Ulticap and Ultiboard at a combined price of £395, which compares well with Boardmaker2 as it offers a schematic capture as well as the PCB drawing set of software. It was only later when I started to fully investigate the software that I realised that an autorouter was also available, so that the Ultimate Challenger system should be compared to Boardrouter at £495, which it undercuts in price, whilst offering better facilities.

System requirements

The minimum system requirements to use the Challenger software are:
- IBM AT or compatible;
- 640 KBytes RAM;
- DOS 3.3 or higher;
- High density floppy disk drive;
- Hard disk; see later for available size needed;
- EGA or VGA display.

My machine running Ulticap at 8 MHz appears quite acceptable to work with, and I noticed no unreasonable delays in operation. Ultiboard will work with the same system if you are willing to accept that the hard disk will be running for a lot of the time. However, it only requires an additional 50 KBytes to stop this happening.

It is not the purchaser of a new PC who will run into problems, but the user with an established PC system a few years old which may need upgrading.

Hard disk size depends on the amount of other software you want to keep on the system. Fully loaded, Ulticap takes 7.7 megabytes of space, and Ulticap an additional 3.3 megabytes, ignoring the space needed for files that are created. In operation, the combined software creates a large number of files, amounting to 300 KBytes in the test case, so with a number of projects in use at one time you need to have a lot of free hard disk space.

Software installation

Installation is very simple using the install program. If you are loading both Ulticap and Ultiboard, you must install Ulticap first, or some of the drivers to enable the schematic-to-PCB interface to work properly will be left out. There are a few selections to be made concerning the available printers, plotters and displays after which the contents of the disk sets (three for Ulticap and two for Ultiboard) are unzipped and loaded on to the hard disk.

Initial inspection

Any idea that Challenger is a 'cut down' package should be dispelled at once considering the amount of disk space used. A look at Ulticap reveals 27 libraries, covering all the logic types you are ever likely to need, an excellent selection of microprocessors, memories and discrete devices and the opamp library had 456 different entries alone. The libraries include both the new IEE style drawings and the older, and for me more familiar, US style. To cut down the hard disk space used, it is possible to get the Install program to load only one type of style. The libraries for Ultiboard are less extensive, but as a 16-pin DIL symbol will cover a good percentage of the logic chips, it is not too surprising. What has been cut for the Challenger system is the total number of devices that can be used, amounting to 700 pins. In all other respects Challenger is identical to its bigger brothers.

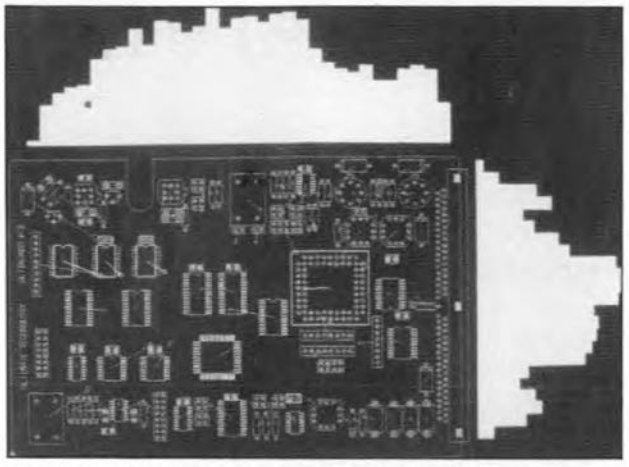
A thick manual accompanies the disks, as well as a thinner tutorial manual. The tutorial is easy to follow and gives a good basic grounding in the software's capabilities.

Using Ultimate for the design cycle

Ulticap and Ultiboard are operated from a main menu called Ultishell. From this, it is possible to set up the full system, and to use either of the main programs, or the interface between them.

The first thing to enter for the storage of the work is the file name to be used, and this is called from Ultishell. What surprised me was that the system jumps out of the software to a very 'DOS-looking' statement, rather than using the more familiar pick list with an option for a new name. Having entered the name, the operation does return to Ultishell, and the main program can be entered. What was more interesting is that if Ulticap is entered directly without a name, the pick list appears as expected once the software has loaded.

Challenger was first tried with the microprocessor schematic design which allowed two bus structures. The drawing screen uses the first press of the left mouse button to call up the pull down menu system to the upper left hand side of the screen. At the top, the 'MAIN' heading is highlighted in red. On calling a submenu, this is added to the red highlighted area with further options below in blue. This makes it easy to see just how far down the menu tree you are at any time. After laying the component symbols of a basic microprocessor system, I started to draw the bus. Laying the bus is simple as Ulticap automatically puts in junctions where they are needed. When laying out the wires from the component to the bus, the 'autowire' facility is a real gem. If you



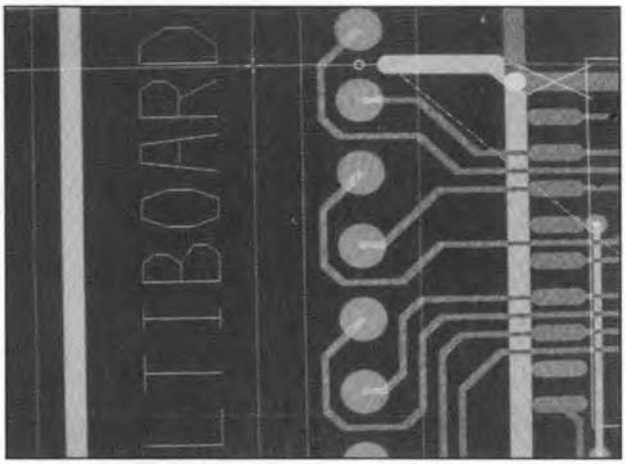
Early layout showing force vectors and histograms.

start at A0 for the address bus, when you get near to the pin on the IC the cursor snaps to the pin and marks it with a cross. Clicking the left mouse button starts the wire. The mouse is moved to the bus line, the left mouse button clicked and the wire is automatically joined to the bus. Starting the next wire, the label increments automatically to A1. It is thus very easy and quick to wire up all of the bus structures. The autowire also can be used for all the other connections finding what it thinks is the best placing for the wire. Wires can be easily moved, provided they are not required to move across the position of a symbol. If you have a wire below, say, a resistor symbol, it can not be moved to above the resistor without removing it completely and then drawing it again. Other than this, Ulticap is easy to use, much easier than Boardmaker, and very much quicker.

A circuit based on discrete devices was just as easy to place and route, and I felt quite at home using the software after a very short time. It was necessary to make an additional symbol, and this proved to be easy if taken slowly, since the symbol needs to have all of the information to allow it to be transferred to the PCB layout software. All of the pin numbers need to tally, or the device on the PCB layout will be incorrectly connected. Storing the symbol design proved more difficult until I discovered the way to start a new library. The manual proved difficult to understand in this area, for me at least.

The interface to the PCB software takes place in three stages: (1) the annotation of the schematic; (2) the conversion to symbol and connection (rat's nest) files; (3) entry into the Ultiboard software itself. All this is done from the Ultishell menu, but the screen seems to jump to DOS type statements once more for a lot of the operations. Other than this, everything proceeds as expected.

In the Ultiboard system, the components file and the rat's nest file are called on. Ultiboard is very much a real time operating program, so that the processor has a lot of work to do for each movement of a component. The rat's nest has to be recalculated so that the connections displayed are the shortest possible. In the microprocessor board, calling in the rat's nest shows that Ultiboard completely understands the bus structure needed for such a system — all of the connections are there. Thus, if you move one of the memory chips, the rat's nest has to be reworked for both buses. This results in a slowing of the operation, and AT type PCs will tend to slow down, causing delays that the user may find annoying. This is not a fault of the software, but due to the PC. Ultiboard is really designed for the latest high-speed 386 machines rather than the old 286s.



Close-up after tracking.

The autorouter in Ultiboard also understands bus structures, and is completely capable of drawing the memory section's bus tracks in a conventional manner. This is much more than can be said for some other autorouters that I have tried. In fact, Ultiboard's autorouter does not finish at the initial completion of the tracks for the board. With the test processor board, the initial autorouteing gave 65 vias and a fully routed board in 13 minutes, and then spent the next 30 minutes optimising the board by reducing the vias to 42.

During manual routeing it is impossible to connect a track to a wrong pin, or to pass too wide a track between two pins. From what I can see, it is impossible to draw the PCB incorrectly, provided the original schematic is correct. It is possible to overcome the protection devices in the case of reducing track lengths by swapping gates in one chip. After saving the PCB layout, the back annotation facility is used to correct the schematic. What I did find difficult was that Challenger does not use the keyboard to short cut some of the menu operations. To get from drawing a track to moving a symbol takes six mouse clicks to get there.

Output

Both Ultiboard and Ulticap can put out the drawings to a variety of printing devices. Of these, I tried the plotter options as I use this more frequently than the dot matrix printer option, and I do not have a laser printer. The drawing file has to be converted to a intermediate plotter file prior to entering the main output program. In the main plotter system, it is possible to alter some of the set-up for the plotter actions, but not all of them. To change the main actions, you have to write a new plotter file via a line editor (EDLIN). This seems very awkward, I would rather have just a menu to set up and then let the plotter go from the new set of directions. In fact, even when I told the plotter configuration to output to COM1, it would only output the plotter data to the LPT1 port. To get the data out of COM1, you have to create a file and then output this in another step. Why this complication is necessary I can not understand — in this respect Boardmaker is better than Ultimate's offering, being much simpler to use.

Conclusions

From the experience I have of the software, the Challenger package completely closes the design cycle, and as such must be regarded as low-cost professional software, rather than aimed at the amateur market. I have found it easy to use for all types of boards and capable of preventing the silly mistakes that so often ruin a board's design. The interface between schematic and layout is simple considering the work that is has to do, but is essential to take great care over the schematic symbol and the shape it calls up on the PCB layout. Considered against Boardrouter, Ultimate's Challenger wins hands down on facilities and price, but fails in the output section. I hope that Ultimate will seriously consider simplifying the output section, since I found it frustrating to use. It is just too complicated!

If you are going to buy PCB design software, Challenger needs serious consideration for the facilities it gives, provided you can put up with its method of working. ■

The Ultimate Challenger package is available from **ULTImate Technology UK Ltd., 2 Bacchus House, Calleva Park, Aldermaston, Berkshire RG7 4QW. Telephone: (0734) 812030, Fax: (0734) 815323.**

A BRIEF HISTORY OF THE VALVE

Like the age of steam to railway enthusiasts, for anyone interested in radio and electronics there is the same nostalgia associated with the thermionic valve. Its discovery heralded the beginning of the age of electronics, and it enabled radio to make some major strides forwards.

By Ian Poole, G3YWX

SINCE then, the warm glow of their heaters, the gentle aroma that rises from them, and the hum from the sets which use them have generated a feeling of life in them. Unfortunately, the superior technical performance of transistors and ICs sounded the death knell for valves. Despite this, many valves are still in use around the world today.

How it began

Although the first valve was not made until the beginning of this century, the foundations for its discovery were laid many years before. People like Ampère, Faraday and Volta all played their part, but one of the first direct contributions was made in 1873 by professor Guthrie. Investigating effects associated with charged objects, he showed that a red hot iron sphere which was negatively charged and held in a vacuum, would become discharged. He also found that the same did not happen if the sphere was positively charged.

The next major step forwards was taken by Edison in 1883. At the time, electric light bulbs were in their infancy, and had a comparatively short life. One of the major problems was that the bulbs became blackened. Initially, it was thought that this was caused by atoms of carbon from the element hitting the glass. As it was known that the particles leaving the element were negatively charged, experiments were carried out to prevent them hitting the glass. One method which was tried involved placing a second element into the envelope. By placing a positive charge on this new element, it would be able to attract the particles away from the envelope, and prevent them hitting the bulb.

In doing this, Edison noticed that when the second element was made positive relative to the main element, a current flowed in the circuit. When the potentials were reversed, he noticed that this did not happen.

Edison was fascinated by the effect, but surprisingly he did not find a use for it, although it became known as the Edison effect. He demonstrated it to many other leading scientific personalities including Preece, a well known British electrical engineer, and Ambrose Fleming, the Professor of Electrical Engineering at University College London. Despite this, no developments were made for some time.

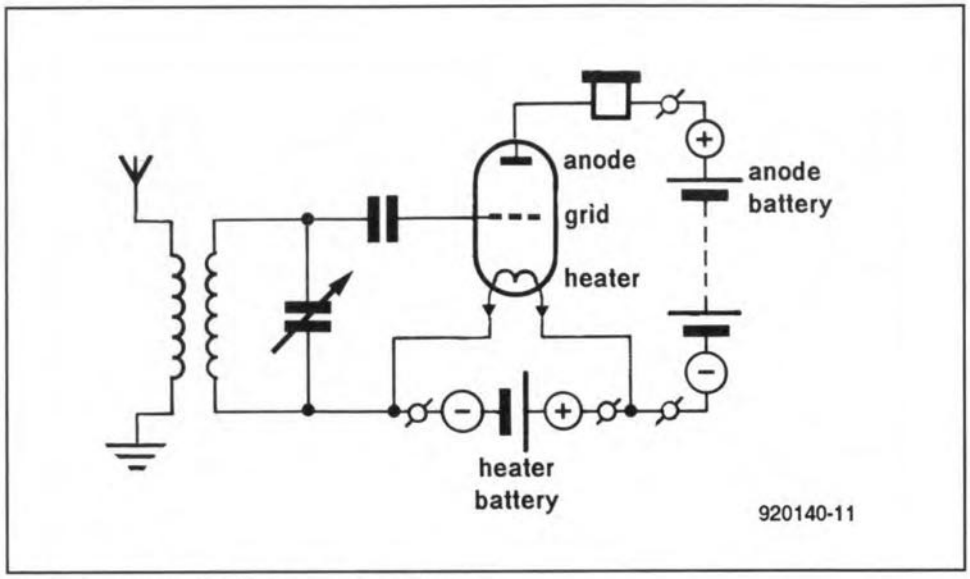


Fig. 1. A circuit using Fleming's oscillation valve.

More developments

Fleming was obviously fascinated by the effect, and experimented with it from time to time. In 1889, he had some bulbs made up for him by the Ediswan Company in the UK, and using these he reproduced the Edison effect. It was not until a few years later that he observed that if an alternating current of between 80 and 100 Hz was passed through the bulb, it became rectified. Finally, Fleming demonstrated this effect to the Physical Society in 1896.

One of the major problems that hampered any further developments was the lack of understanding of what was causing the Edison effect. Matters were made clearer when Sir Joseph Thomson discovered that atoms were made up from even smaller particles, which included negatively charged electrons.

A happy thought

Apart from being Professor of Electrical Engineering at University College

Fig. 2. An early triode.

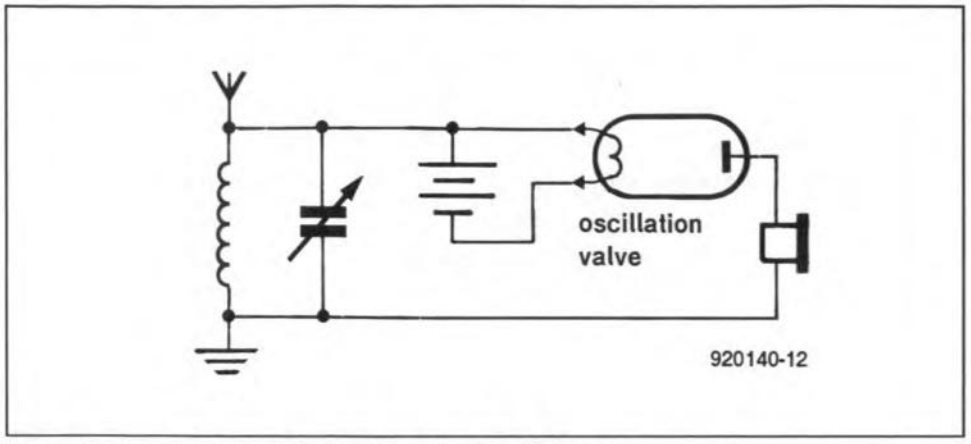


Fig. 3 De Forest's 'Audion' in circuit as a leaky grid detector.

London, Fleming was also a consultant to Marconi, who was pioneering wireless communications. In fact, it was Fleming who designed the transmitter to send the first message across the Atlantic. At this time, the main limitation in wireless communications was the lack of sensitivity of the apparatus which actually received the radio signals — both the coherers and the magnetic detectors were very inefficient.

It was with this problem in mind that Fleming was investigating methods of improving receiver sensitivity. In November 1904, he had what he called a 'sudden very happy thought'. He wondered if the Edison effect could be used to rectify what he called 'feeble to and fro motions of electricity from an aerial wire'. Fleming instructed his assistant to set up an experiment, and they were quickly able to prove that the idea indeed worked.

Fleming called the idea his 'oscillation valve' (Fig. 1) because it acted in a similar way to a valve in a pump which allows gas or water to move in only one direction. He quickly patented the idea, as it was clearly a major step forwards in wireless technology. Even though the diode was still in its infancy, it was still a major improvement over the coherers available at the time.

Other devices

Whilst Fleming's oscillation valve was a revolutionary idea, it did not become widely used. Valves were difficult and expensive to make, and their heaters consumed large amounts of power that had to be supplied by expensive batteries.

Then, in 1906, some cheaper devices were discovered. In fact, two different patents were filed, one by Ferdinand Braun for a crystal detector using hydrated crystals of manganese oxide, and the other by H. Dunwoody for a crystal detector using carborundum. These crystal devices were forerunners of the Cat's Whisker detectors which were used up until the mid 1920s. Although they had a number of limitations, they were much cheaper than valves, and this guaranteed their popularity.

Another electrode

Despite the success of crystal detectors, others still looked towards improving thermionic technology. One was a man named de Forest who had been working on various aspects of wireless, and saw himself as an American rival to Marconi. In his research, he made a number of copies of Fleming's valve, and obtained patents for some modifications and improvements to it. He experimented with a number of different configurations of electrodes, and from the records it can be seen that he took out patents for three-electrode devices in 1905 and 1906. However, it was not until 1907 that he took out a patent for a triode with a fine element between the cathode and the anode. It was this valve that he called his 'Audion' (a later version is shown in Fig. 2).

Slow road to success

Initially, valves were not widely used. They were expensive, and offered few advantages, partly because they were not used to their full potential. In fact, the triode was only used as a leaky grid detector (Fig. 3). The idea of using it to give amplification had not been considered.

It was not until 1911 that the valve was used as an amplifier or oscillator. After

Fig. 4. The famous 6L6 and 807 valves.

this discovery, people were quick to try to exploit it. De Forest built an amplifier using three Audions, and demonstrated it to the telephone company AT&T. Although the performance was poor, they saw its potential, and soon started to build repeaters using valves which they had improved.

It was not until 1915 when an American scientist named Langmuir discovered that gases were not required in the envelope. New, highly evacuated, valves (known as 'hard valves') were soon produced with much better performance. In addition to basic improvements, the full evacuation of the envelopes brought a number of other improvements. Filaments could now be coated to improve their electron emission. Previously, any coating would have been contaminated. Filament temperatures could also be reduced, and this improved reliability as well as reducing the heater current consumption.

The advantages of the new 'hard valves' soon became apparent, and large numbers were manufactured. One type manufactured in France by the military authorities under an engineer called Ferrie was called the TM, of which over 100,000 were produced. An English development of it, called the Type R triode, was equally successful. After the first World War, many of these valves came on to surplus market, and were snapped up by enthusiastic amateurs.

More electrodes

One of the major difficulties using the early triodes was to prevent them from oscillating, especially when they were used in high-frequency circuits of more than a few hundred kilohertz. The problem was caused chiefly by the inter-electrode capacitance between the anode and the grid. Many attempts were made to try to overcome this capacitance. In 1916, H.J. Round produced a low-capacitance valve known as the Type V24. In it, the anode lead was passed out of the glass envelope through a top cap on the valve, and not through the base. This idea has been used on many other radio frequency valves right up to recent times. Whilst this solution was reasonably successful, and Round managed to make his amplifier operate well for the day, it was by no means the answer to the problem.

Fig. 5. Three modern all-glass dual triodes.

Many further attempts were made to reduce inter-electrode capacitance. However, it was not until 1926 that the complete solution was found with the introduction of the tetrode. This used a second grid called the screen grid. This was placed between the normal control grid and the anode. Its introduction reduced the anode to control grid capacitance to almost zero, and solved the problem of instability.

Later, the tetrode itself was improved in 1929 by the introduction of the pentode. This valve had yet another grid called the suppressor grid, which improved the discontinuity in the characteristic of the tetrode caused by electrons bouncing off the anode when they hit it.

Heaters

Apart from making improvements in the operation of valves by creating additional grids, further improvements were made in the heater arrangements. It was discovered that the cathode could be indirectly heated, and this meant that the heaters could be electrically isolated from the cathode. This, in turn, had the advantage that the heaters did not need to be powered by a battery (d.c.) supply. A major improvement indeed, because it meant that size of radios could be considerably reduced, as could be their running costs.

Increase in use

During the 1930s, valve use increased dramatically. Their use within domestic radios grew, and in addition to this they were used in a variety of applications within industry. By the late 1930s, many thousands of different types of valve were being manufactured, and there was a large number of different manufacturers appearing both in the USA and in Europe.

Many of the valves introduced in this period have long since disappeared from common use. However, a few were very successful, and remained in new designs for a long time. One such valve was the Type 6L6 used in many guitar amplifiers until quite recently. In many ways, it was quite revolutionary, being the first beam tetrode. It used a new technique to overcome the discontinuity in the characteristic of the tetrode caused by electrons bouncing off the anode. Rather than using a suppressor grid, it had a new arrangement connected to the screen grid. This valve became so popular that it was later modified for RF applications by giving it a top cap for the anode. This valve was called the 807, and was widely used in transmitters in the Second World War and afterwards. The 6L6 and 807 are shown in Fig. 4.

Prior to the war, all valves had used special metal or plastic bases attached to the glass envelopes to hold the pins. After the war, miniaturization and improvements in manufacturing techniques enabled the pins to be mounted into the glass envelope. By doing this, much smaller valves were made (Fig. 5), and costs were reduced.

The Fall

The heyday of the valve could not last forever. The invention of the transistor in 1948 took a long time to affect the supremacy of the valve. However, in the 1960s, when prices of transistors started to fall, it became obvious that valves were no longer the best option for many applications. Transistors and, later, ICs totally overtook the use of valves in domestic appliances. Radios, televisions and many other items which had previously used valves all turned to semiconductors.

Despite all this, thermionic technology still survives in a number of areas where semiconductors have not been able to compete. One of the most obvious is the cathode ray tube (CRT) in televisions and computer monitors. Although some semiconductor alternatives are slowly appearing, they have not yet supplanted the dominance of the CRT.

Another area where transistors have not been able to compete is in high-power transmitting applications. Today, valves offer the only real solution for transmitters producing a few tens of kilowatts or more. As a result of this, many developments have been made in this area recently.

Finale

Valves have been used now for nearly 100 years. Their contribution to electronics has been enormous. In fact, there is no doubt that electronics would not be nearly as advanced as it is today, had it not been for the invention of Fleming's oscillation valve, and all the subsequent developments. ■