ELEKTOR ELECTRONICS

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8 extra pages
Results of our
May competition

EPROM EMULATOR II

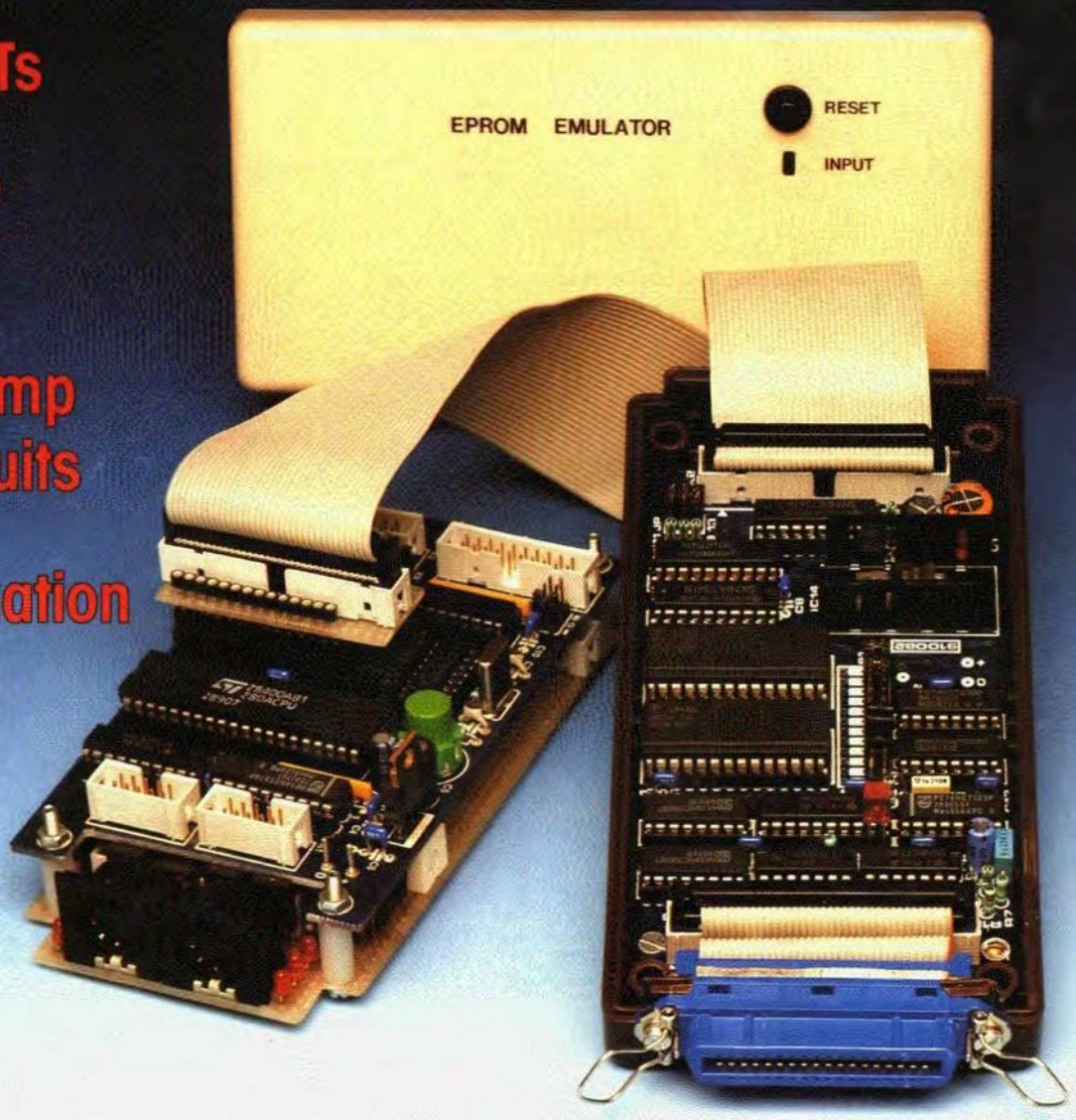
23 cm transmitter-receiver

Current-sense power MOSFETs

CAN-controller area network

Analogue opamp integrator circuits

Antenna evaluation transmitter



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* *It is regretted that, owing to circumstances beyond our control, this article has had to be postponed from the September to the October issue.*

Front cover
The photograph shows the updated version of the EPROM emulator we published about three years ago. In the present circuit, conventional rather than surface-mount (SMD) components are used, since a number of readers, particularly those outside Europe and North America, have found difficulty in obtaining and handling SMD devices. The updated version has 64 Kbyte of RAM and is capable of emulating Types 2764 through 27512.

ABC
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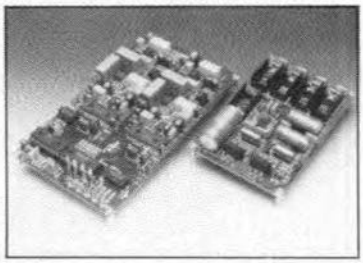

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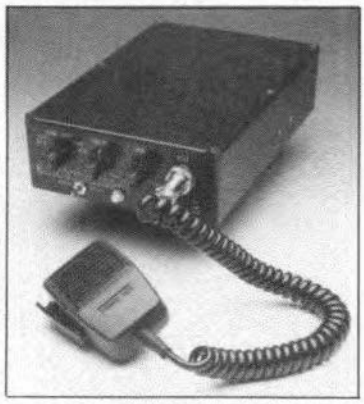

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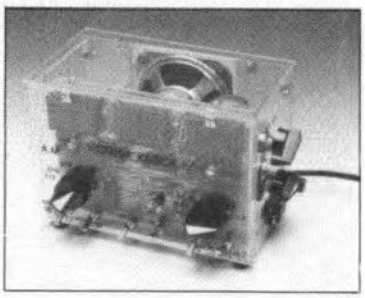

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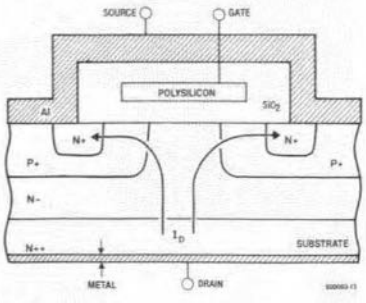

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EPROM EMULATOR II

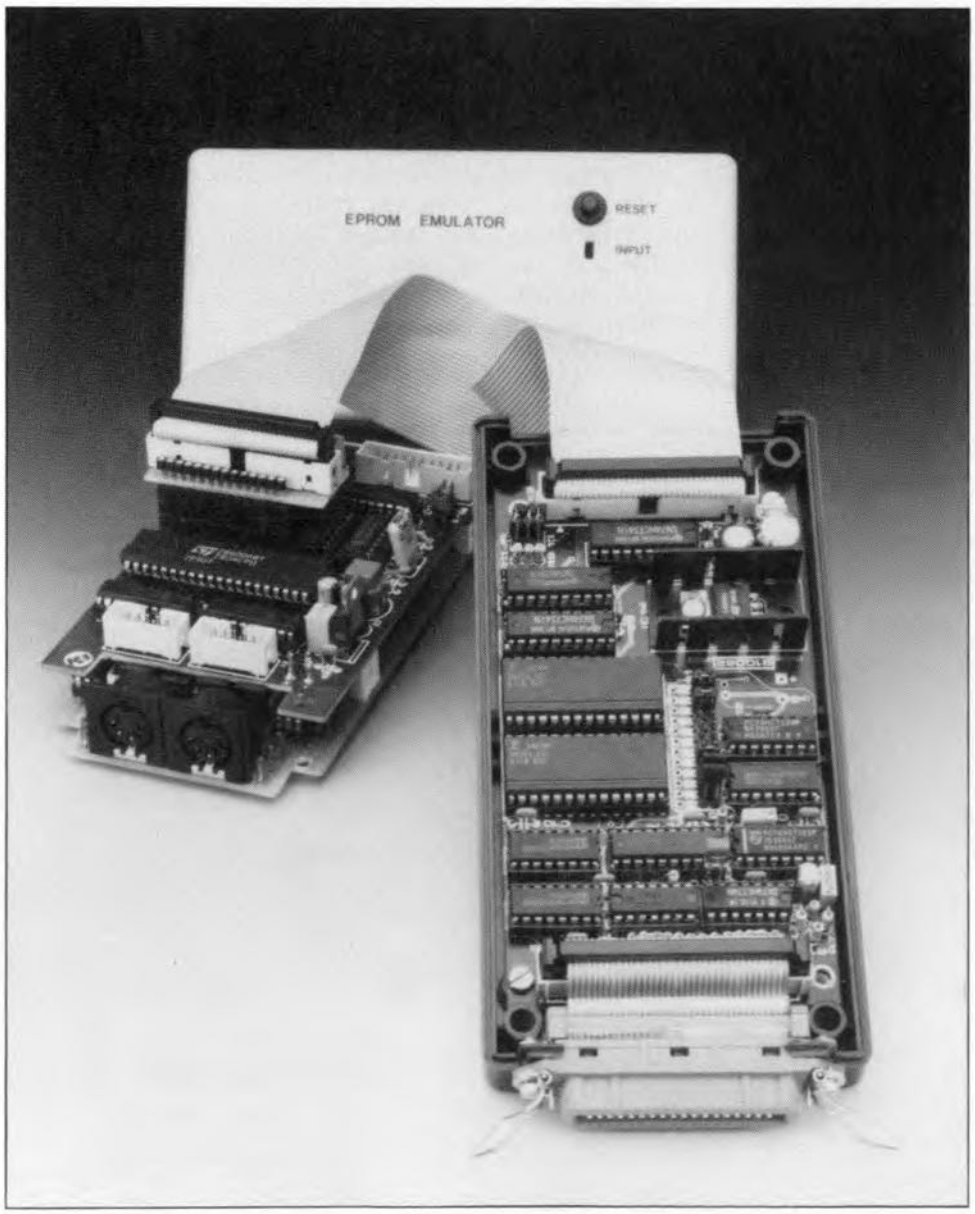
This is a revamped version of an EPROM emulator we published about three years ago. This time we propose to build the circuit with standard size components rather than SMA (surface mount assembly) components, which some of you have found difficult to obtain as well as handle. The present version of the emulator has a RAM of 64 KByte, and is capable of emulating 2764s up to and including 27512s. Also, by parallel connection of Centronics cables, extensions to bus widths of 16 bits or 32 bits are easier than before.

MAIN SPECIFICATIONS

- Emulates EPROMs 2764 through 27512
- Connected to Centronics port
- Auto-reset function
- 8-, 16- or 32-bit configuration
- No driver software required; use is made of existing system utilities (MS-DOS, Windows, ST and Amiga)

Design by B.C. Zschocke and N. Breidohr

AN EPROM emulator replaces the EPROM in a computer system (for which a program is to be developed) by a RAM that behaves like an EPROM. The advantages are well-known: the contents of the RAM can be overwritten as many times as you like, and the data transfer from the PC (running an assembler) to the target system is much faster. Errors in the object program are thus easily and quickly corrected, because it is no longer necessary to remove the EPROM, erase it, and reprogram it.



The data transfer from the PC to the emulator described here does not require special file formats like Intel-Hex, Tektronics or Motorola. Instead, standard system utilities can be used to output the previously prepared binary file via the Centronics port.

Application range

The present emulator replaces the byte-organized EPROMs with a capacity of 8 KBytes (2764) to 64 KBytes (27512). The now obsolete 2-KByte and 4-KByte EPROMs Types 2716 and 2732 may also be emulated with the aid of a specially prepared adaptor board. Up to four emulators may be connected in parallel to 'attack' systems with a bus width of 32 bits. The EPROM data may be furnished by any computer system with a Centronics port. The STROBE pulses supplied by the computer have four functions: (1) they indicate that the data is stable and valid; (2) they enable the emulator; (3) they clock three-state counters IC7, IC8 and IC9; and (4) they select a particular emulator in 16-bit or 32-bit systems.

The counter outputs address two RAM ICs with a capacity of 32 Kbyte each. The data applied to the input of the emulator is 'acknowledged', and copied directly into the RAM. The selection of the RAMs is accomplished via A15 of counter IC9, and one half of IC12. After the last byte has been stored in the RAM, the counter is switched to high-impedance output mode ('three-state'). The individual RAM addresses are then available for selection through the address buffer, and can be read via the data output buffer. The addressing of the RAM at this stage is accomplished by the host system, i.e., the computer system or (more generally) application circuit whose EPROM is emulated.

Circuit description

Essentially, the circuit consists of three blocks:

(1) A control section around IC10 and IC11, which serves to ensure the proper bus tim-

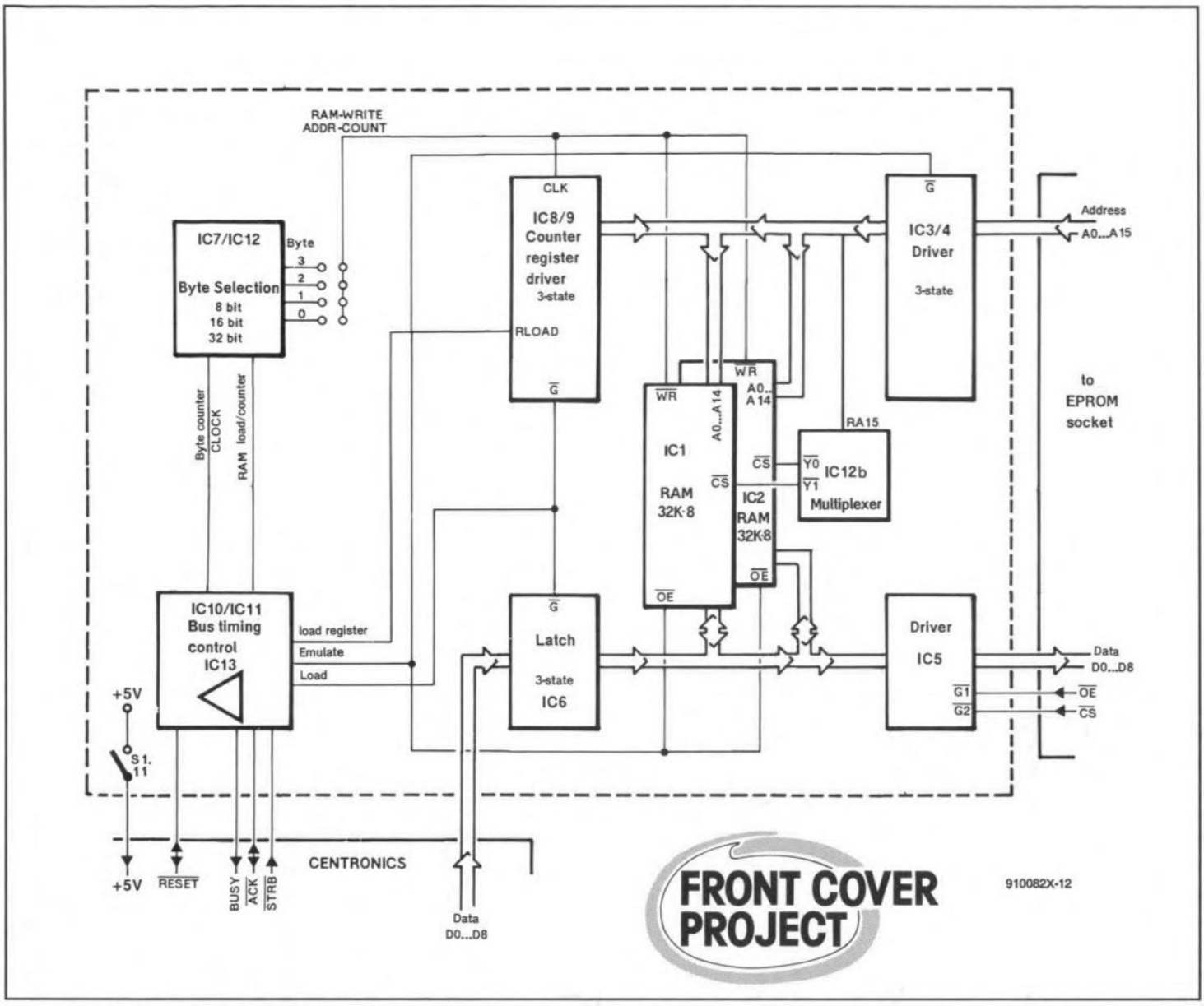


Fig. 1. Block diagram of the EPROM emulator.

ing on the Centronics interface, and generate a number of internal signals. This section also supplies the RESET signal for the application circuit (Auto-RESET). All signals are taken to the 'outside world' via open-collector buffers/drivers contained in IC13. One driver serves to generate the strobe signal.

(2) A byte selection circuit (IC7 and one half of IC12), which arranges the distribution of the received 8-bit data between parallel emulators in 16-bit and 32-bit applications. This circuit is required only if a 16-bit or 32-bit extension is envisaged.

(3) A RAM address and load address generator consisting of a counter (IC8 and IC9) that supplies the RAM addresses during loading, a latch (IC6) for intermediate storage of Centronics databytes, and drivers (IC3, IC4 and IC5) that interface to the EPROM socket in the application circuit. Depending on the mode of operation of the circuit (loading or emulating), either the counter/latch combination or the EPROM socket interface are in control of the EPROM addresses and data.

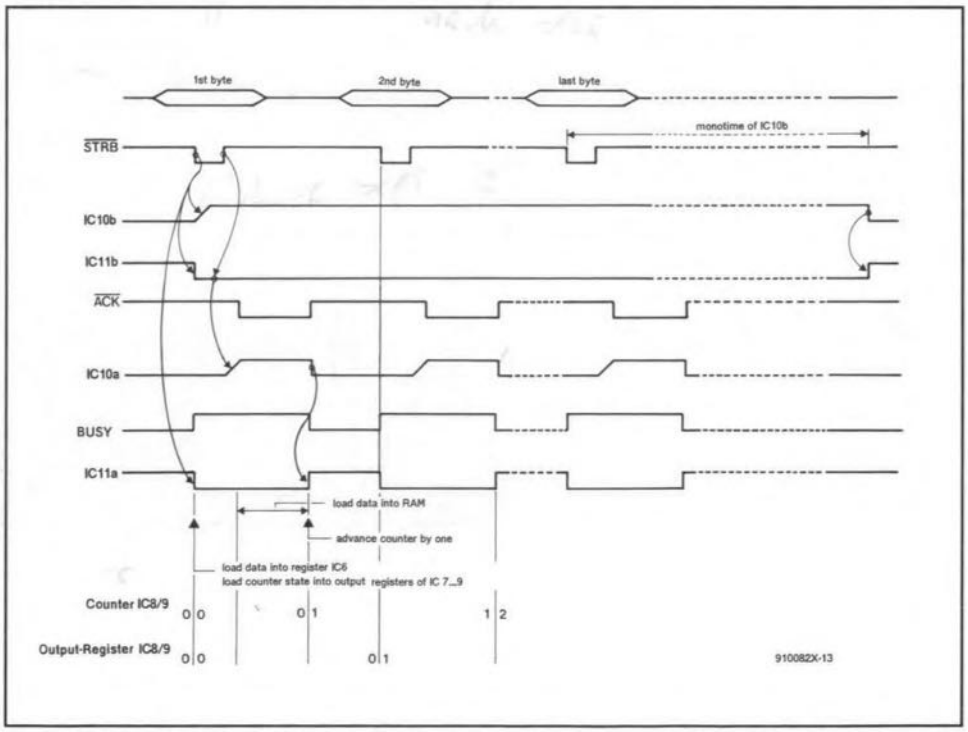


Fig. 2. This timing diagram should help you grasp the basic operation of the EPROM emulator. Note that both the positive and the negative edge of the STROBE signal are used.

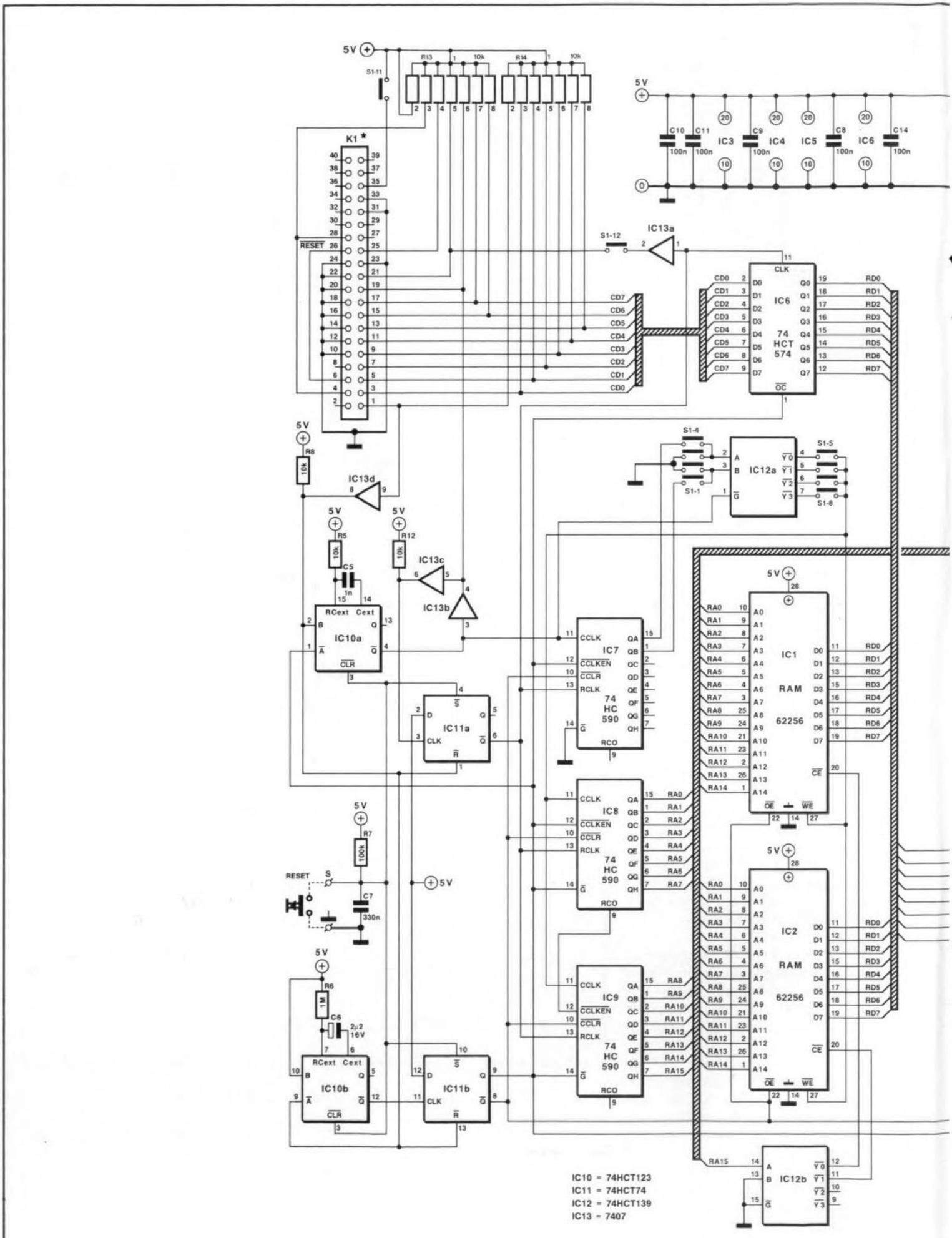
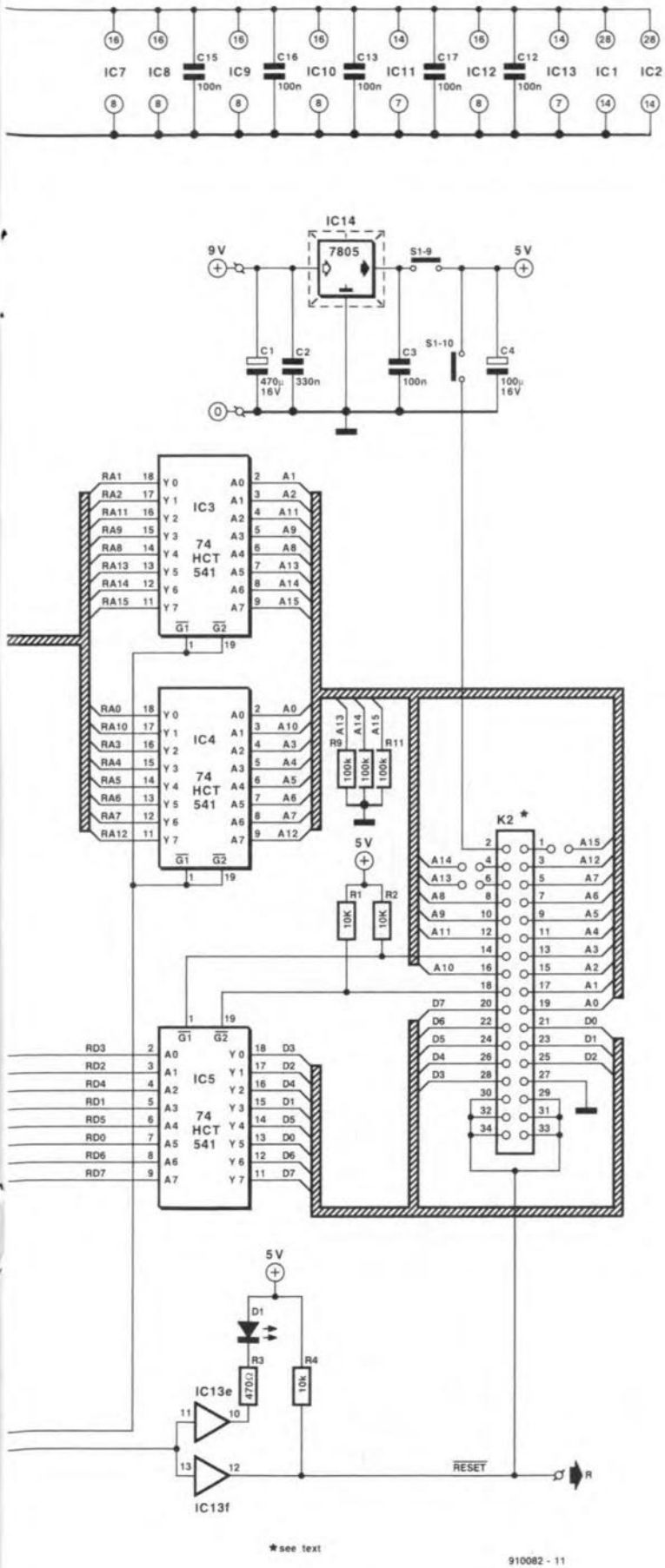


Fig. 3. Circuit diagram of the EPROM emulator.



Since 64-K×8-bit RAMs are not easily obtained at reasonable prices, the present emulator is based on two 32-K×8-bit RAMs. These offer a total storage capacity of 64 KByte, and allow the emulator to mimic EPROMs up to and including the 27512. When smaller EPROMs are used, address lines A15 (27256), A15/A14 (27128) or A15/A14/A13 (2764) must be tied to ground via the appropriate jumpers (see Table 1).

Operation in detail

The Centronics standard stipulates that data must be stable for a certain time before and after the STROBE pulse. This ensures freedom of using either the leading or the trailing edge of the strobe signal to capture data from the printer's Centronics input. In the emulator, both edges are used.

At power-up, R7 and C7 provide a defined state. Bistables IC11a and IC11b are set, while bistables IC10a and IC10b are reset. IC11b clears all counters, and switches the circuit to the emulate mode. With reference to the timing diagram of the 8-bit version (Fig. 2), the negative edge of the STROBE signal triggers IC10b, and resets IC11a and IC11b. Next, IC11b switches the circuit to load mode, and actuates the RESET line. IC11a actuates the Centronics BUSY line, and the positive edge at its output causes the counter state to be transferred to the counter register, and the Centronics databyte to be transferred to the latch. Data and address are allowed to stabilize at the respective RAM inputs while the STROBE pulse lasts. The positive edge of the STROBE pulse triggers IC10a, and actuates the RAM WRITE signal and the Centronics ACKNLG (acknowledge) signal during the monotime of IC10a. The signal edge that marks the monotime sets IC11a, and so clears the BUSY signal. At the same time, the counter is advanced one state. The first byte has been stored in RAM, and the circuit is ready to receive the next byte. A byte received within the monotime of IC10b causes this monostable to be triggered again. Otherwise, the above cycle starts again on detection of the negative edge of the STROBE pulse. If no databyte is received during the monotime of IC10b, the circuit switches to emulate mode, clears the RESET signal, switches the counters to three-state, and resets them. At this point, the RAM addressing is taken over by the application circuit.

To prepare the circuit for use in 16-bit or 32-bit applications, IC7 and one half of IC12 divide the internal RAM WRITE and counter output signals. Depending on the jumper setting, either the each first, second, third or fourth byte is copied into the latch, while the counters receive an appropriately reduced number of clock pulses. The RAMs are switched via their CS (chip select) lines, with the aid of address line A15 and the other half of IC12.

At first glance, the outputs of IC10b and IC11b behave identically. Why, then, are

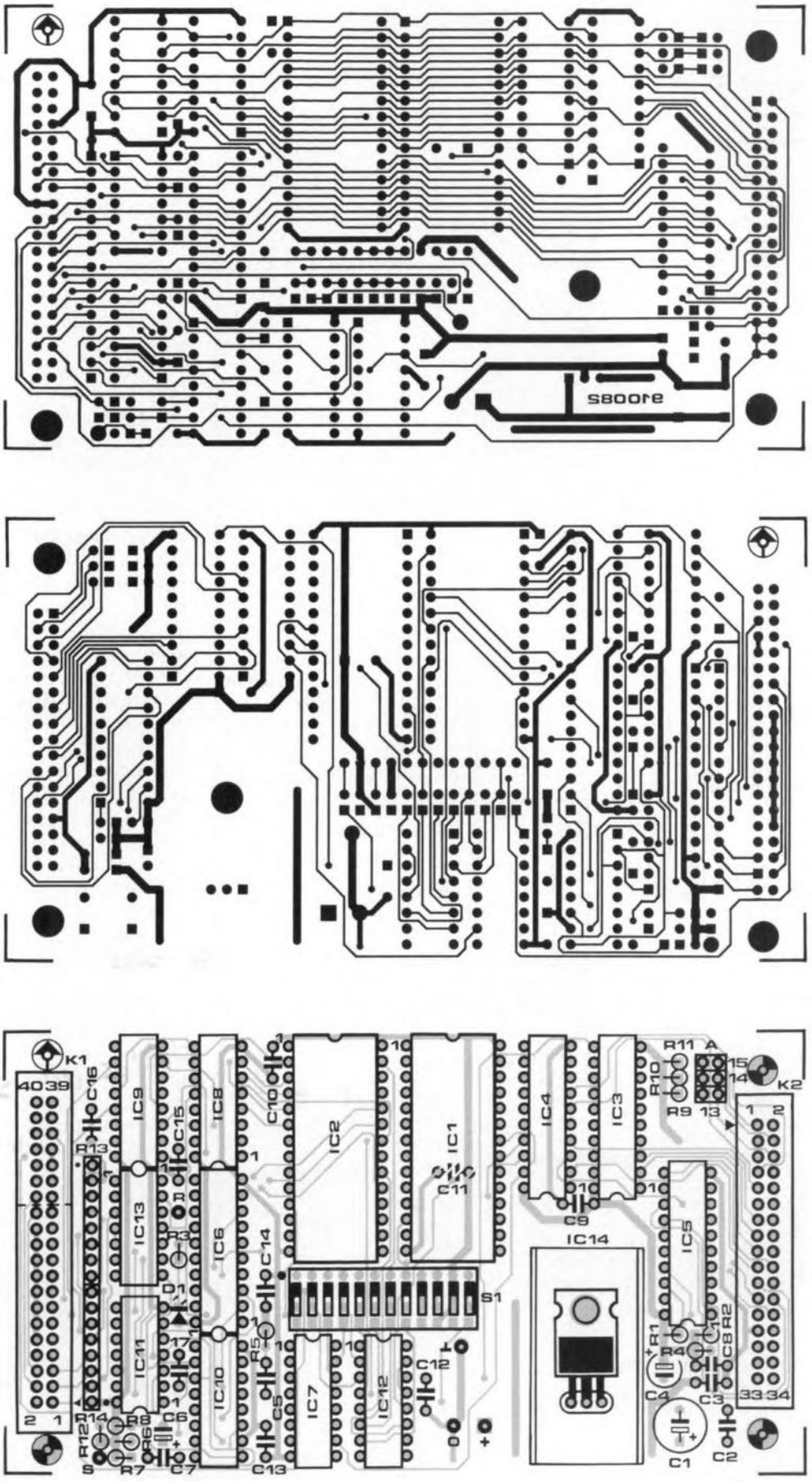


Fig. 4. Track layouts (mirror images) and component mounting plan of the PCB designed for the EPROM emulator.

COMPONENTS LIST

Resistors:

6	10kΩ	R1;R2;R4;R5; R8;R12
1	470Ω	R3
1	1MΩ	R6
4	100kΩ	R7;R9;R10; R11
2	7-way 10kΩ SIL	R13;R14

Capacitors:

Pitch 0.2 inch (5 mm):		
1	470µF 16V radial	C1
2	330nF	C2;C7
11	100nF	C3;C8-C18
1	1nF	C5
Pitch 0.1 inch (2.5 mm):		
1	100µF 16V radial	C4
1	2µF2 16V radial	C6

Semiconductors:

1	LED, green, 3mm	D1
2	62256 (<100ns)	IC1;IC2
3	74HCT541	IC3;IC4;IC5
1	74HCT574	IC6
3	74HC590	IC7;IC8;IC9
1	74HCT123	IC10
1	74HCT74	IC11
1	74HCT139	IC12
1	7407 (74LS07)	IC13
1	7805	IC14

Miscellaneous:

1	12-way DIP switch block, or 24-way pin header block with jumpers	S1
1	40-way box header	K1
1	34-way box header	K2
1	40-way IDC socket	
1	34-way IDC socket	
1	IDC Centronics socket	
1	TO-220 style heatsink	
1	Printed circuit board	910082
1	ABS enclosure; approx. size 160×80×32mm	

IC sockets
28-way DIL adaptor (see Fig. 5)
Approx. 50cm 36-way flatcable

S1:	1	2	3	4	5	6	7	8	9	10	11	12
8-bit		on	on									
16-bit		on		on								
32-bit	on			on								
Byte-#					0	1	2	3				
Power external									on			
Power from EPROM socket										on		
+5V on Centronics input											on	
BUSY on Centronics input												on

(Switch = OFF when not otherwise noted)

EPROM type	Jumper A13	Jumper A14	Jumper A15
2764 (8 KByte)	off	off	off
27128 (16 KByte)	on	off	off
27256 (32 KByte)	on	on	off
27512 (64 KByte)	on	on	on

Table 1. Jumper settings for emulator bus width and EPROM type.

both used? The timing diagram shows an unexpected, rather unwelcome, quirk of the monostable, IC10b. At the (relatively long) monotime, the time between the triggering instant and the output actuation instant is not short enough. This caused problems in a number of prototypes. The trigger signal supplied by IC10b actuates IC11b instantly, while IC11b is de-actuated again by the negative edge of IC10b. Capacitor C6 may also cause trouble if it can not be discharged quickly enough by IC10. Increasing its value must, therefore, be done with care.

LED D1 lights when the computer feeds data into the emulator. The (active low) RESET signal is taken to the application circuit via connector K2. On completion of the load activity, the emulator releases the RESET line, and so re-starts the application circuit, which subsequently runs its new software contained in the emulator RAM.

The emulator is powered either by the application circuit (via S1-10), or by the on-board stabilizer (via S1-9), whose input is connected to a small mains adaptor with d.c. output. Whether or not an external power supply is required is, of course, dependent on the capacity of the target system's power supply. A power supply conflict may arise when the emulator is powered by the application circuit, and this is switched off, or powered down during reset, while the 'other side' of the emulator is connected to the PC (which is still on) via a Centronics cable. If this happens, the emulator is powered via the protection diodes in the Centronics interface of the PC. This results in a supply voltage of about 3 V, which is sufficient for the RAMs to retain their data, but not for the TTL circuits to operate properly. If, in this condition, the application circuit is switched on, the emulator may go into an undefined state, which may be ended by pressing a button connected between point 'S' and ground. A better solution, however, is to power the emulator

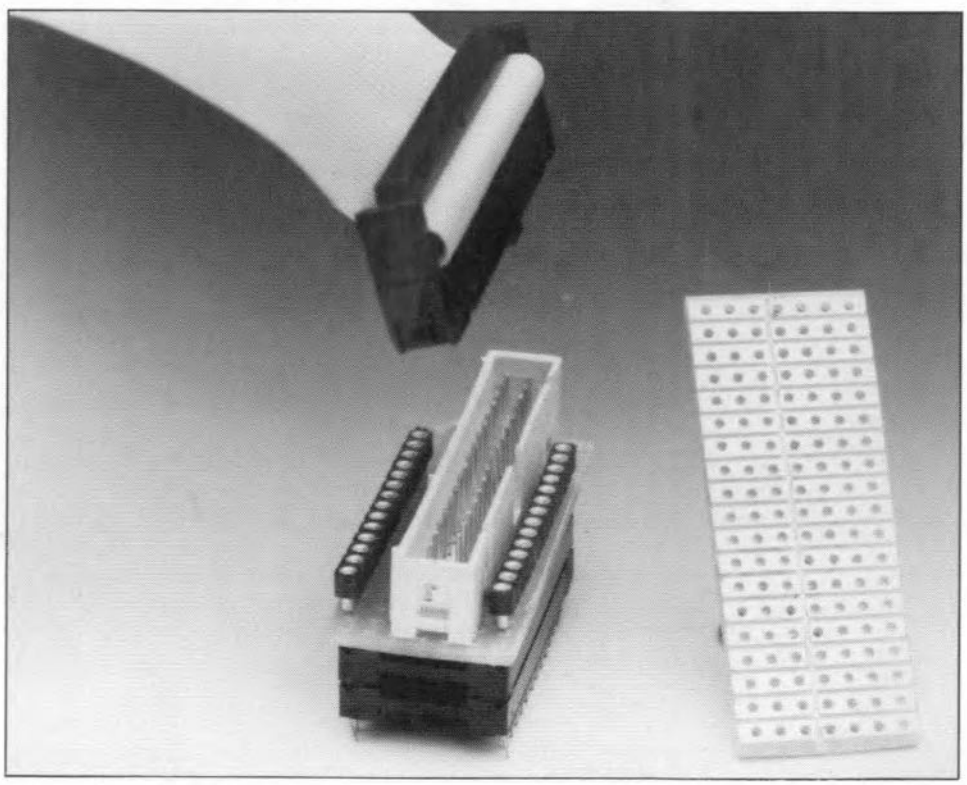


Fig. 5. Illustrating the construction of the home-made EPROM adaptor.

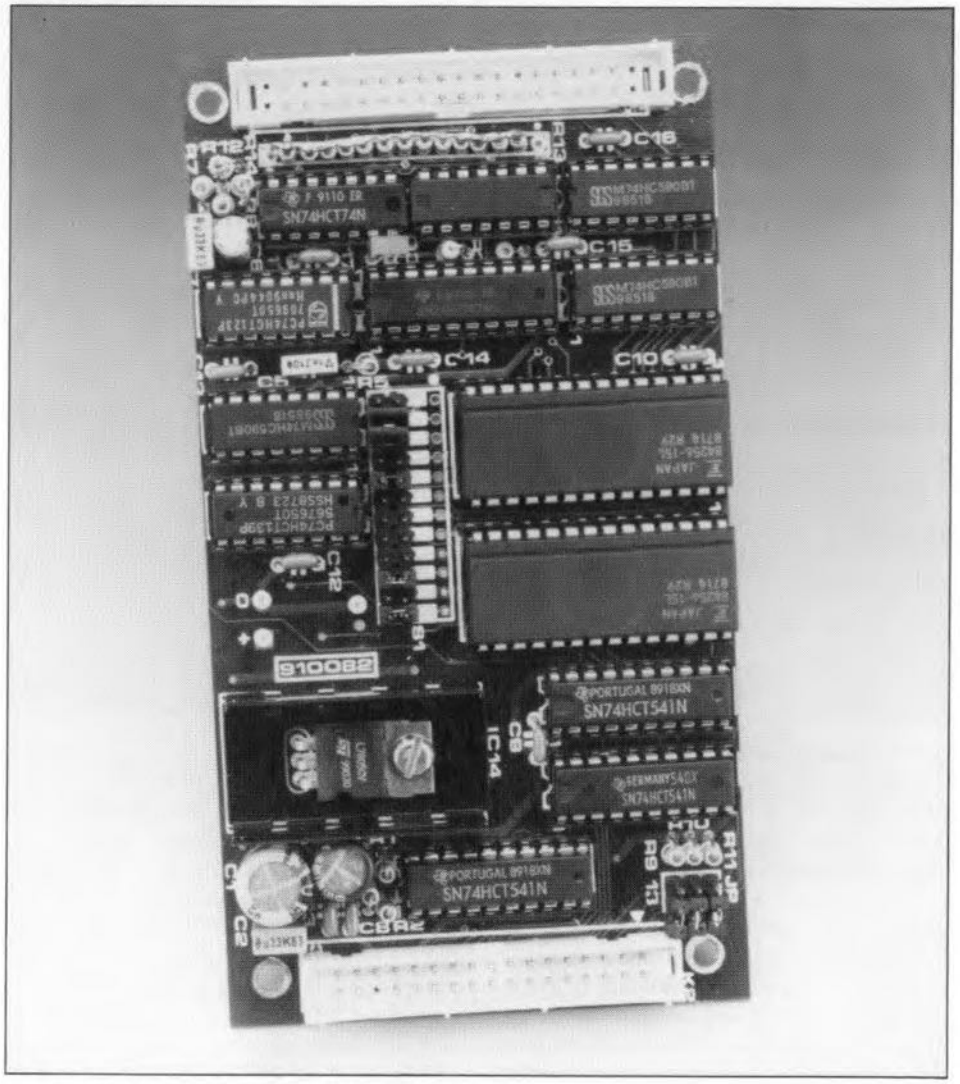


Fig. 6. Completed printed circuit board.

from an external source via IC14. The previously described power supply conflict may also damage the emulator, because the current sent into the application circuit via the EPROM socket may become so high that the driver ICs are destroyed.

Practical hardware

The printed circuit board designed for the EPROM emulator is a high-density double-sided, through-plated type, which is best purchased ready-made through our Readers' Services. Space is pretty tight on the board, so keep an eye on the pitch of the capacitors. Capacitor C11 is fitted at the solder side of the board, underneath IC1.

Pin header K1 is suitable for two types of connection: its pinning is compatible with a 25-way sub-D connector (allowing ready use of IDC-style connectors), as well as with a 36-way Centronics socket. When the latter is used, make sure to remove pins 4 and 6, or cut the relevant tracks. When a 25-way sub-D connector is used, it is, unfortunately, not possible to create a 'loop-through' connection for the supply voltage. To reduce cost, a 40-way IDC socket was used on the prototype — a 26-way type (for connection to a sub-D plug) is, of course, also possible.

The 16-bit and 32-bit versions of the EPROM emulator require two or four complete circuits, respectively, which are driven by a common line, for instance, via four IDC-style Centronics plugs. The jumper settings on each board may be found in Table 1. The emulators are mutually synchronized via the ACK line on the Centronics interface. The BUSY line may be connected on one board only (S1-12). In case the emulators are to be powered by a single, external, supply, this is connected to one board only, from where the supply voltage is distributed via pin S1-11 on each board. On the board from which the supply voltage is distributed, S1-9 must be closed. On all other boards, S1-9 is open. S1-10 must be closed on all boards.

Software

As already mentioned, special software is not strictly required. The emulator RAM can be loaded with the aid of any system utility capable of outputting binary files in binary form, via the Centronics port. This means that the EPROM emulator can be used with any computer sporting a Centronics-compatible printer port.

Users of MS-DOS PCs may want to obtain version 2.0 of EPROMSIM, a program which is available on disk through our Readers Services as item ESS129. EPROMSIM supports EPROMs up to 64 KByte, and is capable of handling the following 'intelligent' file formats:

- Intel Intellec-8;
- Tektronix hexadecimal;
- Motorola.

Construction

When building the circuit, remember to remove pins 4 and 6 of the Centronics socket, if used. To ensure ready access, the DIP switch array is best mounted on IC sockets. Alternatively, you may want to fit the switches at the solder side of the board, and cut a clearance in the back panel of the enclosure. The LED wires may be extended to enable the LED to be fitted in a hole in the cover panel. Further constructional points that deserve your attention are the mounting of the Centronics input socket, and the strain relief on the flatcable to the EPROM adaptor.

The EPROM adaptor is home-made. As shown in Fig. 5, it consists of a piece of stripboard, two lengths of IC pin strip, a box header and two 28-way IC sockets. The flatcable from the EPROM emulator is fitted with a 28-way IDC socket. You may want to make one adaptor for each EPROM type, and wire jumpers A13, A14 and A15 appropriately, direct on the socket. Wires 29 to 34 of the flatcable are connected to the RESET generator on the emulator board, and may also be taken to the adaptor socket to create a RESET connection for the application circuit. ■

DOWNLOADING TO THE EPROM EMULATOR

PC/MS-DOS	COPY <filename> LPT1:/B	(/B for binary output)
Amiga	COPY <filename> PAR:	(PAR:, not PRT:)
TOS	On the ST it is sufficient to double-click on the filename shown on the desktop, and then output to 'printer'. It should be noted, however, that the TOS appends a CR/LF sequence to each file. This means that the last two bytes of a 32-Kbyte file can not be used. However a simple printer manager that does not output the CR/LF sequence should not be too difficult to write in Pascal, C or BASIC.	

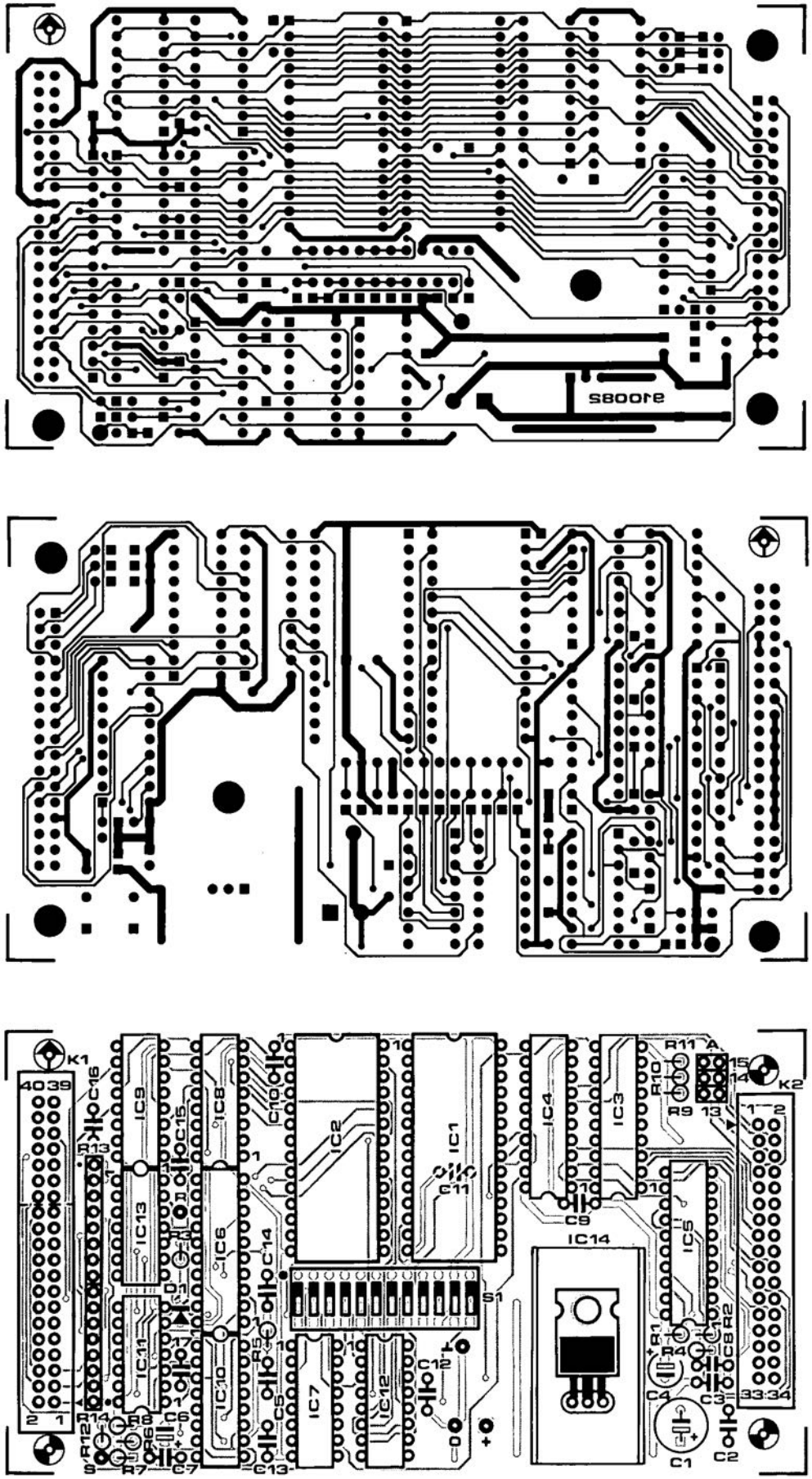


Fig. 4. Track layouts (mirror images) and component mounting plan of the PCB designed for the EPROM emulator.

A.F. DIGITAL-TO-ANALOGUE CONVERTER

PART 2

Design by T. Giesberts

BEFORE the construction is discussed, it was thought useful and interesting to have a look at the test results from our two prototypes. Note that both of them were K versions using Type 5534A opamps in the output filter and buffer section. The measurements were carried out with an Audio Precision System One analyser (with FFT option), while the signals were obtained from a number of special measurement-CDs (CD-1 from CBS; Test Sample 3 and Audio Signals Disc 1 from Philips; and Digital Test from Pierre Verany). For clarity's sake, all figures illustrating the measurement results pertain to one channel (the results of the other channel were, for all practical purposes, identical).

The –0.1 dB figure at 20 Hz (see Fig. 8) results from the effect of the servo control,

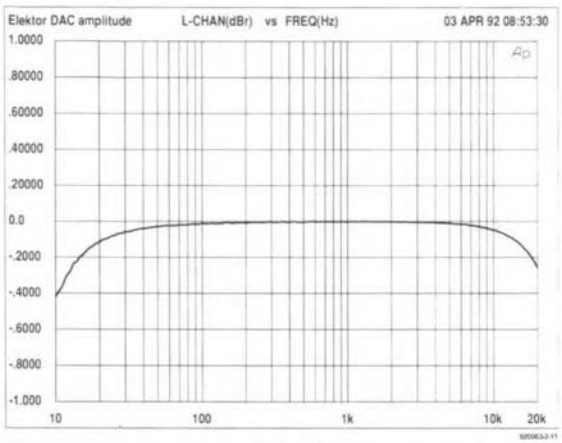


Fig. 8. Frequency characteristic.

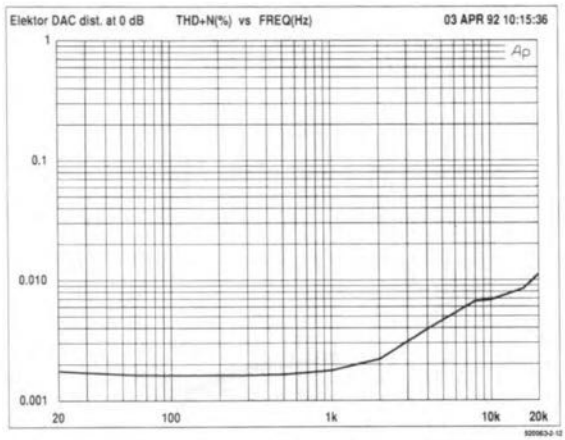


Fig. 9. THD+noise from 20 Hz to 20 kHz at full drive.

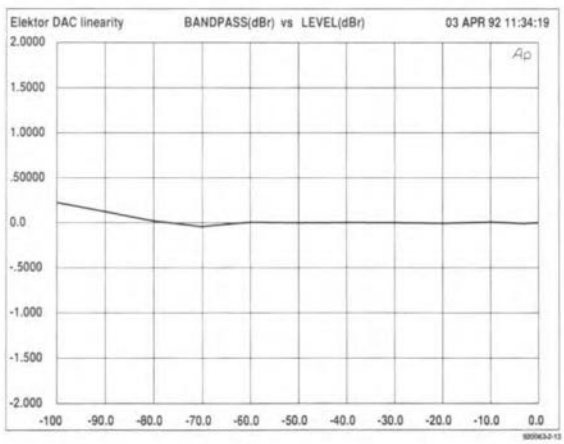


Fig. 10. Linearity deviation for signals to –100 dB.

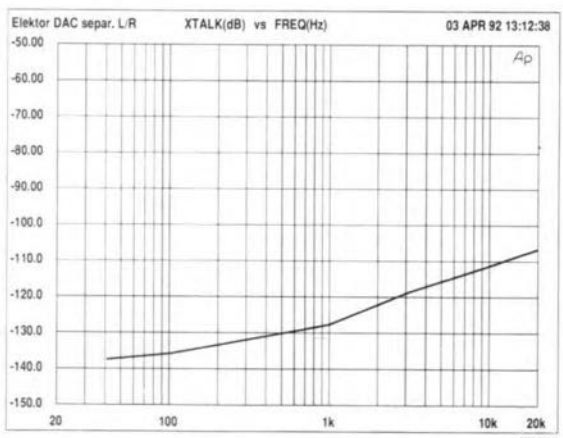


Fig. 11. Cross-talk over the audio range.

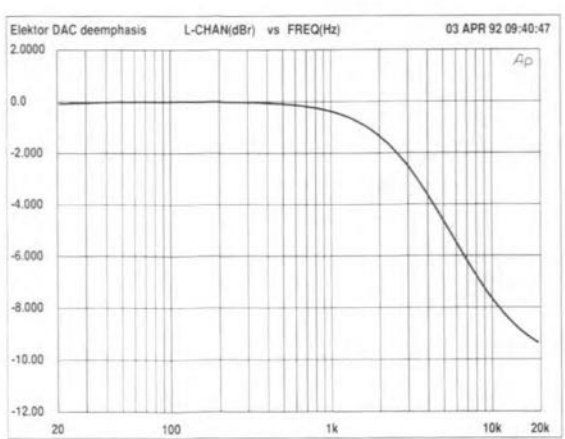


Fig. 12. The measured de-emphasis characteristics.

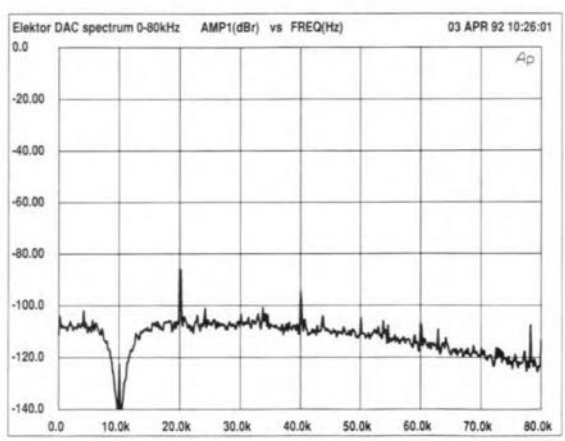


Fig. 13. Spectrum analysis of residual signals up to 80 kHz.

which acts as a high-pass filter. The 0.25 dB fall-off at 20 kHz is ensured by the analogue output filter. It would have been possible to straighten the curve here, but that would have meant a higher cut-off frequency and, consequently, worse suppression of the sampling frequency and worse phase behaviour in the pass-band (since a Cauer or Chebishev filter would then have to be used). The characteristic in Fig. 8 is virtually a Butterworth curve with a near-constant time delay in the pass-band up to 20 kHz.

The harmonic distortion (THD+noise) characteristic is shown in Fig. 9. At frequencies below 1 kHz, the distortion is identical to that specified by Burr-Brown for their K versions: –96 dB. Above 1 kHz, the distortion increases very slightly, owing to the effect of the number of samples per period and because frequencies above 20 kHz are suppressed (a sharp cut-off filter as, for instance, recommended by Philips for measurements above 20 kHz was not used).

The linearity deviation—see Fig. 10—was measured down to –100 dB (from –70 dB to –100 dB with dithering).

The cross-talk characteristic in Fig. 11 shows that the channel separation is excellent: –105 dB at 20 kHz and –135 dB at 100 Hz indicate that the curve is virtually the same as the noise characteristic of the converter.

The de-emphasis characteristic in Fig. 12 does not show its accuracy with respect to the theoretical curve, but the deviation between the two was measured at <0.15 dB over the 20 Hz to 20 kHz frequency range.

Figure 13 shows the spectrum analysis over the frequency range up to 80 kHz. The 10 kHz test signal was effectively suppressed by a band filter, so that the residual products are clearly indicated. Note the 2nd and 4th harmonics of the test signal and the mixing prod-

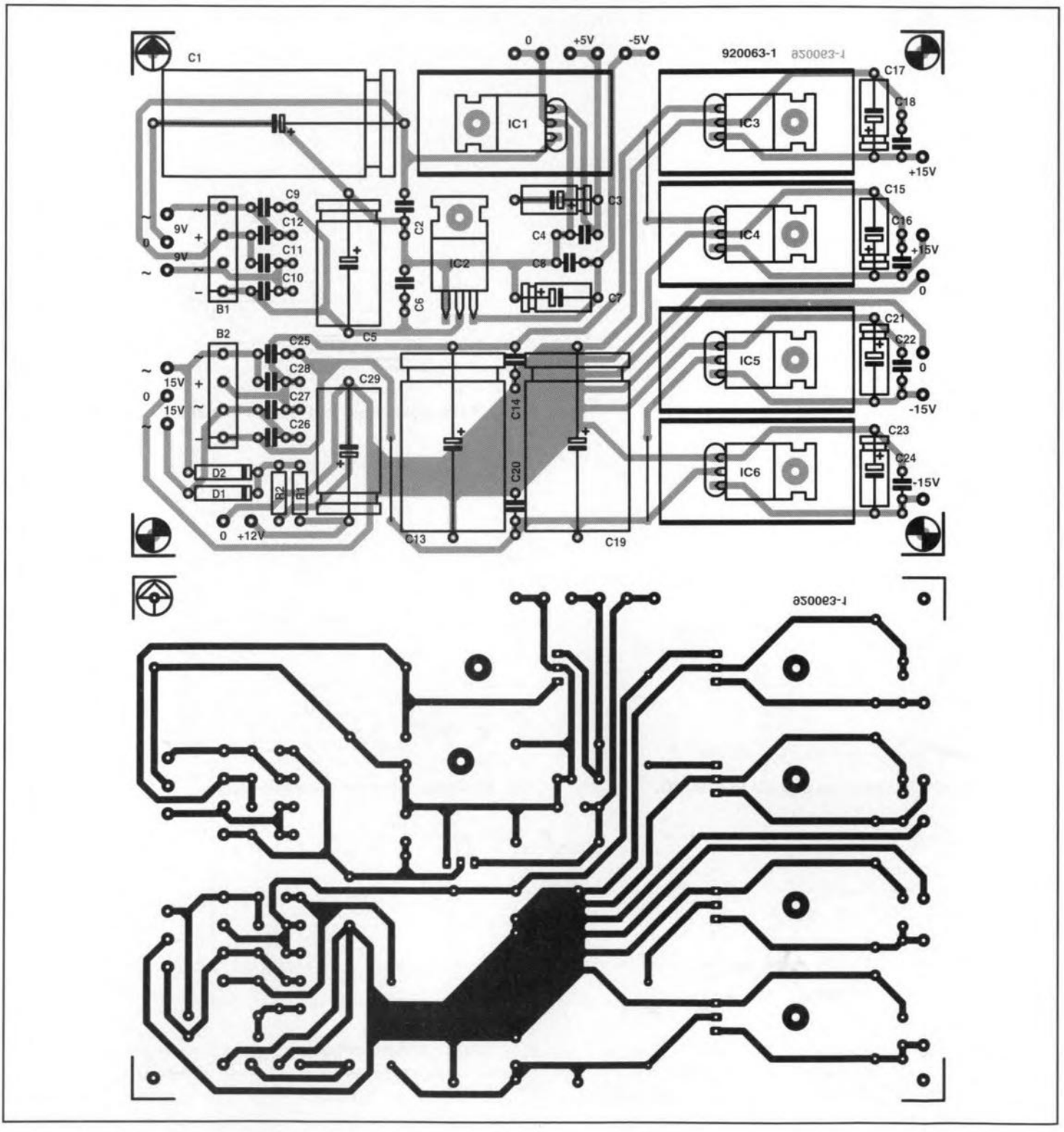


Fig. 14. The printed-circuit board for the power supply section.

uct (78.2 kHz) of the test signal and twice the CD sampling frequency (2×44.1 kHz), since the analogue filter does not have an infinite roll-off.

Construction

It is advisable to read carefully through this section before buying any components, because the design contains some fairly expensive ICs. As far as the YM3623B and DF1700P are concerned, there is not much choice, because these devices are made in only one version. The PCM63P, however, is available in three grades: that without suffix is the cheapest, the PCM63p-J is next and the PCM63P-K is the dearest. Depending on the market area, the difference between the first and the -K version can be £10–£15. The difference between these versions lies in the accuracy (that is, without calibration). At 1 kHz and full drive, the -K version has a THD+noise figure of –96 dB; the -J version, –92 dB; and the cheapest version, –88 dB.

Type OP27 opamps are specified for the IC_{10} and IC_{18} positions because of their offset voltage and low noise. Faster opamps are not recommended in the servo control.

The AD844, used in the IC_6 and IC_{14} positions, has properties that make it particularly suitable for use in D-A converters: good bandwidth (60 MHz at unity gain); high slew rate (2000 V/µs) and short settling time (100 ns to reach an accuracy of 0.1%). Moreover, it can drive low-impedance loads (50 mA into 50 Ω) and is reasonably priced.

There is a good choice as far as the remaining opamps are concerned. According to our measurements, the most suitable are the NE5534A, the LT1115, the TLE2027 and the OPA627. Although the OPA627 is much faster than the 'ordinary' 5534 and, moreover, has FET inputs, we found, in our measurements, that there is very little difference between the two. However, in listening tests, a number of people preferred the OPA627 in the output section (the opamp in the filter has less influence on the sound quality). Bear in mind that we are talking here of very small differences that become audible only on first class audio installations.

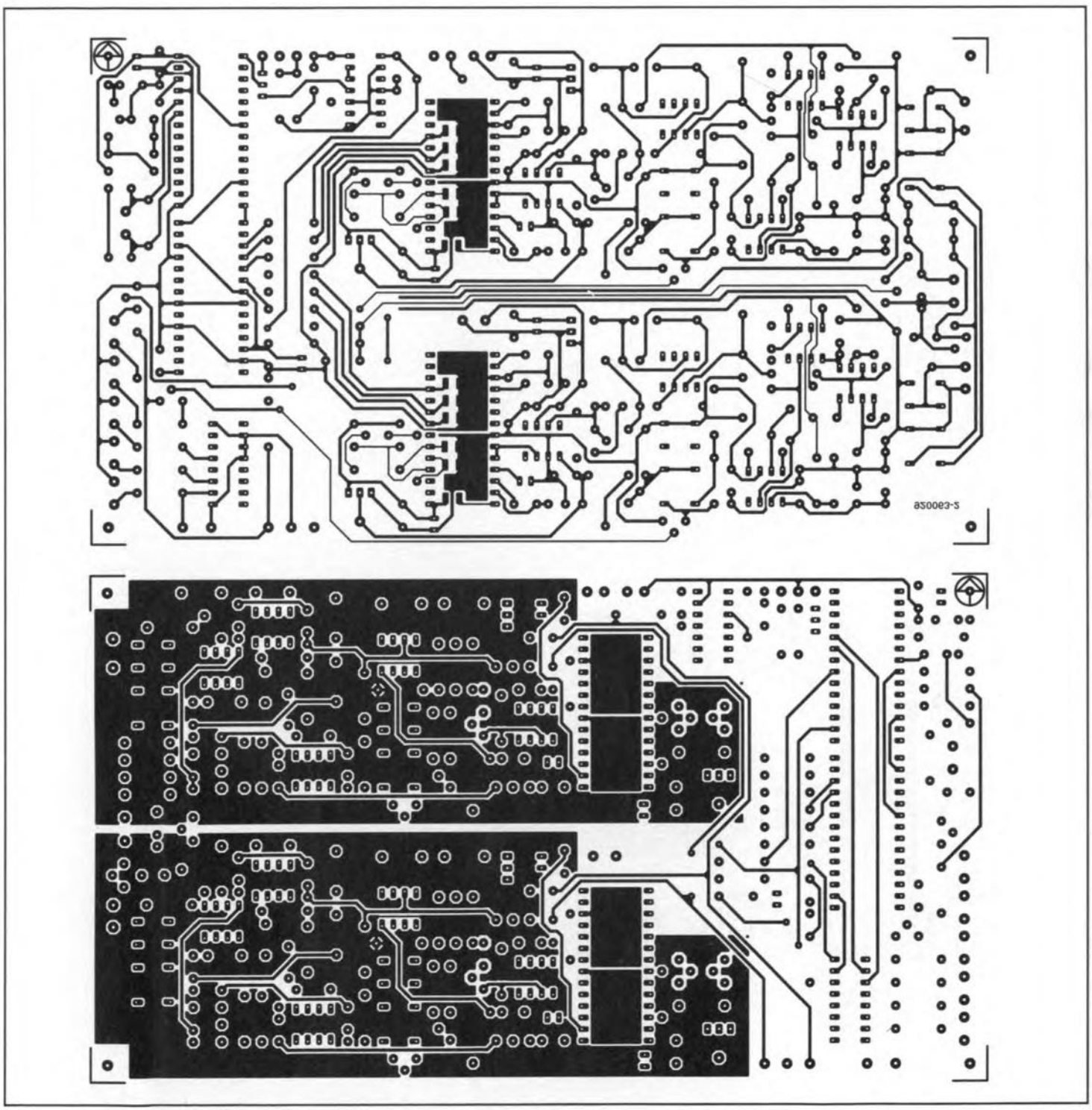


Fig. 15. Printed-circuit mother board, shown here at 80% of true size.

PARTS LIST

Power supply board

Resistors:
R1 = 68 Ω
R2 = 1.5 kΩ

Capacitors:
C1 = 2200 µF, 25 V
C2, C4, C6, C8, C14, C16, C18, C20, C22, C24 = 100 nF
C3, C7 = 10 µF, 10 V
C5 = 220 µF, 25 V
C9–C12, C25–C28 = 47 nF, ceramic
C13, C19 = 2200 µF, 35 V
C15, C17, C21, C23 = 10 µF, 25 V

Semiconductors:
D1, D2 = 1N4001
B1, B2 = B80C1500
IC1 = 7805
IC2 = 7905
IC3, IC4 = 7815
IC5, IC6 = 7915

Miscellaneous:
Mains transformer, 2×9 V, 830 mA
Mains transformer, 2×15 V, 500 mA
Heat sinks for IC1, IC3–IC6
PCB Type 920063-1 (see Readers' services)

Mother board

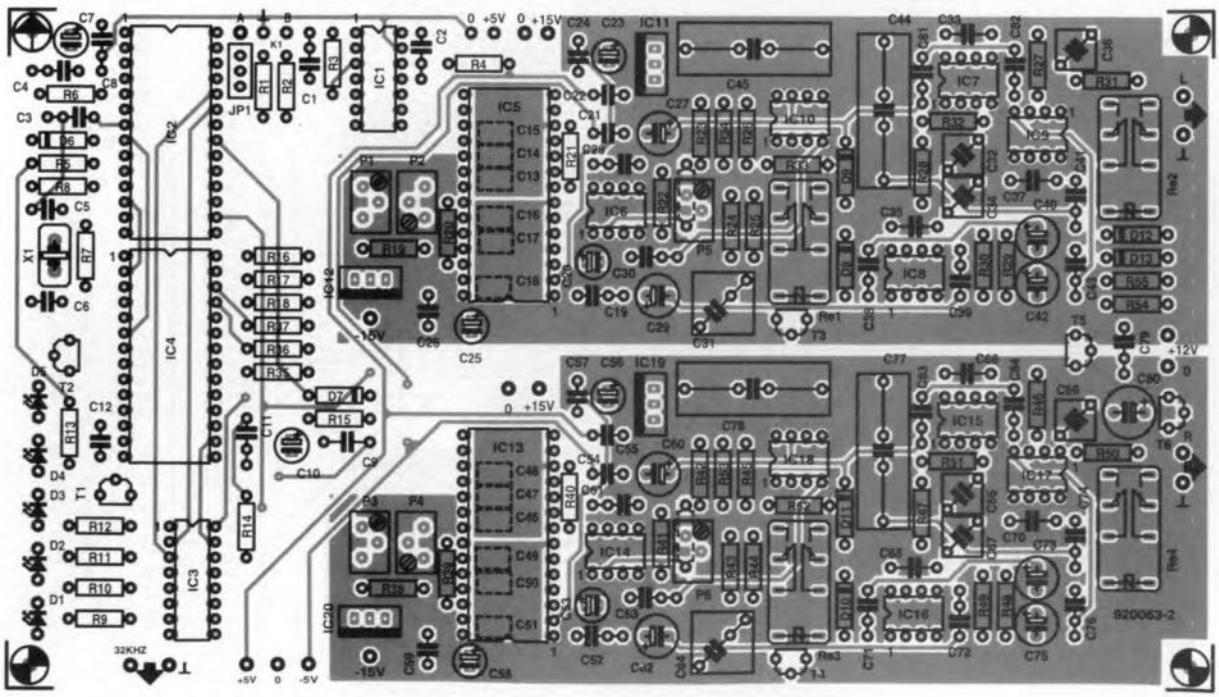
Resistors:
R1 = 75 Ω, 1%
R2 = 100 Ω
R3 = 10 kΩ
R4 = 4.7 Ω
R5 = 18 kΩ
R6 = 270 Ω
R7, R25, R44 = 1 MΩ
R8, R14 = 2.2 Ω
R9–R13 = 470 Ω
R15 = 22 MΩ
R16, R17, R18, R35, R36, R37 = 47 Ω
R19, R20, R38, R39 = 330 kΩ
R21, R40 =1 Ω
R22, R41 = 1.5 kΩ, 1%
R23, R42 = 1.07 kΩ, 1%
R24, R43 = 475 Ω, 1%
R26, R45 = 2.49 kΩ, 1%
R27, R46 = 931 Ω, 1%
R28, R29, R47, R48 = 2.43 kΩ, 1%
R30, R49 = 2.74 kΩ, 1%
R31, R50 = 49.9 Ω, 1%
R32, R33, R51, R52 = 6.81 kΩ, 1%
R34, R53 = 4.99 kΩ, 1%
R54 = 10 Ω
R55 = 47 kΩ
P1–P4 = 100 kΩ multi-turn preset, vertical mounting (e.g., Bourns Type 3296Y)
P5, P6 = 47 kΩ multi-turn preset, vertical mounting (e.g., Bourns Type 3296Y)

Capacitors:
C1 = 10 nF, ceramic
C2, C3, C19, C52, C79 = 100 nF
C4 = 8.2 nF
C5, C6 = 10 pF
C7, C10, C20, C53 = 4.7 µF, 10 V, radial
C8, C11, C28, C30, C38, C39, C41, C43, C61, C63, C71, C72, C74, C76, C81–C84 = 47 nF, ceramic
C9 = 15 nF
C12 = 100 pF
C13, C14, C15, C46, C47, C48 = 47 pF*
C16, C17, C18, C49, C50, C51 = 100 nF*
C21, C22, C56, C58 = 10 µF, 10 V, radial
C23, C25, C56, C58 = 10 µF, 10 V, radial
C24, C26, C57, C59 = 100 nF, ceramic
C27, C29, C40, C42, C62, C62, C73, C75 = 47 µF, 25 V, radial
C31, C64 = 33 nF, polystyrene, 1%
C32, C34, C36, C65, C67, C69 = 1.5 nF, polystyrene, 1%
C33, C35, C37, C66, C68, C70 = 22 pF, polystyrene (see text)
C44, C45, C77, C78 = 2.2 µF, 160 V, MKP (= polypropylene)
C80 = 220 µF, 6.3 V

Semiconductors:
D1–D5 = 3 mm LED, high efficiency
D6, D8, D10, D12 = 1N4148
D7, D13 = BAT85
D9, D11 = zener, 3 V, 400 mW
T1 = BC546B
T2–T5 = BS170
T6 = BC517
IC1 = 74HCU04
IC2 = YM3623B (Yamaha)
IC3 = 74HC239
IC4 = DF1700P (Burr Brown)
IC5, IC13 = PCM63P (Burr Brown)
IC6, IC14 = AD844AN (Analog Devices)
IC7, IC8, IC9, IC15, IC16, IC17 = NE5534A
IC10, IC18 = OP27
IC11, IC19 = 7805
IC12, IC20 = 7905

Miscellaneous:
JP1 = 3-way header with jump link
K1 = audio socket for PCB mounting (gold-plated contacts preferred)
2 audio sockets with gold-plated contacts) for analogue outputs
Re1–Re4 = 12 V miniature relay
X1 = crystal, 16 MHz
PCB Type 920063-2 (see Readers' services)

* Surface mount type



When choosing opamps, pay particular attention to the stability in the analogue section. If the chosen type is not stable at unity gain (in our tests, that was only true of the 5534), each IC *must* be provided with a compensating capacitor: in case of the 5534, a 22 pF polystyrene type between pins 5 and 8. There is provision for these on the PCB and they are shown in the circuit diagram (Fig. 5). Details of these capacitors, and where to place them, can be found in the data sheets of opamps not mentioned here.

Commence the construction with the power supply board—see Fig. 14. The only thing that needs to be noted here is that all regulators, except IC_2, must be fitted on a heat sink.

The mother board—see Fig. 15— requires rather more work. It has been designed to ensure good separation of the analogue sections of the two channels. The top of the board contains an earth plane for all analogue components: this plane (for each channel) is connected to analogue earth in only one place.

Remember that capacitors C_{33}, C_{35}, C_{37}, C_{66}, C_{68}, and C_{70} are only required if Type 5534 opamps are used.

In some case, surface-mount design (SMD) capacitors are specified, because these types can be soldered (as they should be) very close to the associated IC pins.

If a distortion meter is not available, omit P_1–P_4, R_{20}, R_{38} and R_{39}, because the MSBs of the converters then cannot be calibrated. Note that fitting these components and setting the potmeters to the centre of their travel may result in a worse performance than if the components had been omitted.

Presets P_5 and P_6 are optional and only required if it is felt that the output levels of the two channels should be absolutely equal. Even when these components are omitted, the output levels of the channels are within 0.25 dB of each other, although they may not be exactly, as preferred, 2.0 V r.m.s. The potmeters can, of course, set the level to exactly 2.0 V (if so, a 1 kHz, 0 dB, *digital* test signal must be used, *not* a digitized analogue signal: this is normally indicated on the test CD). Note that 23.7 kΩ resistors instead of the potmeters will keep the output level very close to 2.0 V.

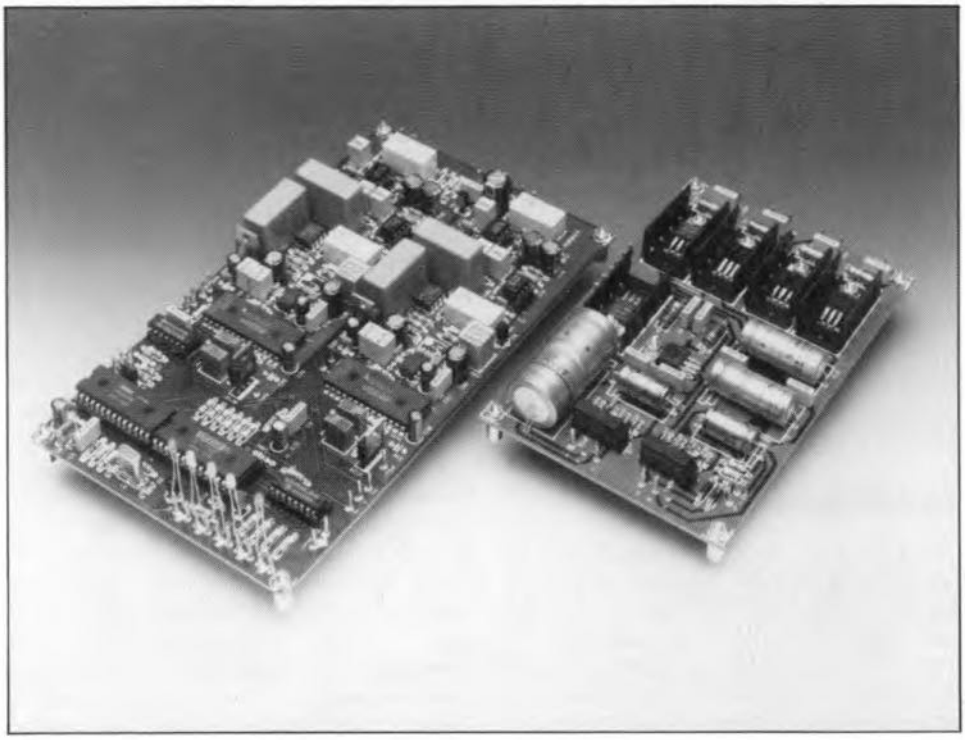
The crystal should be insulated at its underside before it is mounted on the board.

Circuits IC_1–IC_4 may be fitted in an IC holder, but IC_5 and IC_{13} *must be soldered directly to the board*. This is not only to prevent bad contacts, but also because it ensures that these devices are as close to the earth plane as possible. In our opinion, it is best to solder all directly to the board; whence our advice at the beginning of this section. If you must (for experimental purposes), only IC_7–IC_9 and IC_{15}–IC_{17} should be fitted in IC sockets, but these should be of prime quality (with gold-plated contacts). Note, however, that even such sockets show rapidly deteriorating contacts when the ICs are replaced frequently.

Before connecting the power supply board to the mother board, connect it to the mains and check that all voltage levels are as specified. If they are, connect the two boards together via not too long wires. Place jump lead JP_1 as far as possible from connection A. Solder some audio sockets to the digital input (between connection B and earth) and the analogue outputs. The input can then be connected via a coaxial cable to the digital output of, say, a CD player and the outputs, via a stereo cable, to the line inputs of an amplifier (or pre-amplifier).

When the mains is switched on, all should be well.

If you wish to use the converter in this form and feel that you will not need a digital selector, optical inputs and outputs, and a digital tape output (which will be described in our next issue), you can install it in a suitable enclosure now. Otherwise, wait and see the next and final instalment. ■



Technical Data

- Suitable for sampling frequencies of 32–48 kHz
- ×8 oversampling
- 20-bit D–A converters
- Integral de-emphasis circuit
- No capacitors in signal paths
- Servo control of d.c. setting in audio section
- Pseudo-passive GIC filter for suppressing sampling frequency
- Separate power supplies for analogue and digital sections

Dynamic range	>100 dB
Nominal input voltage, (digital input)	500 mV into 75 Ω
Nominal output voltage	2 V r.m.s.
Output impedance	50 Ω
Frequency range	20 Hz–20 kHz (+0 dB; –0.25 dB)
Signal-to-noise ratio	>115 dB
THD+noise (0 dB; 1 kHz)	<0.002%
Intermodulation distortion (60 Hz; 7 kHz; 0 dB)	<0.003%
Linearity deviation (signal levels to –100 dB)	<1 dB
Channel equalization	Within 0.1 dB
Deemphasis deviation	<0.15 dB

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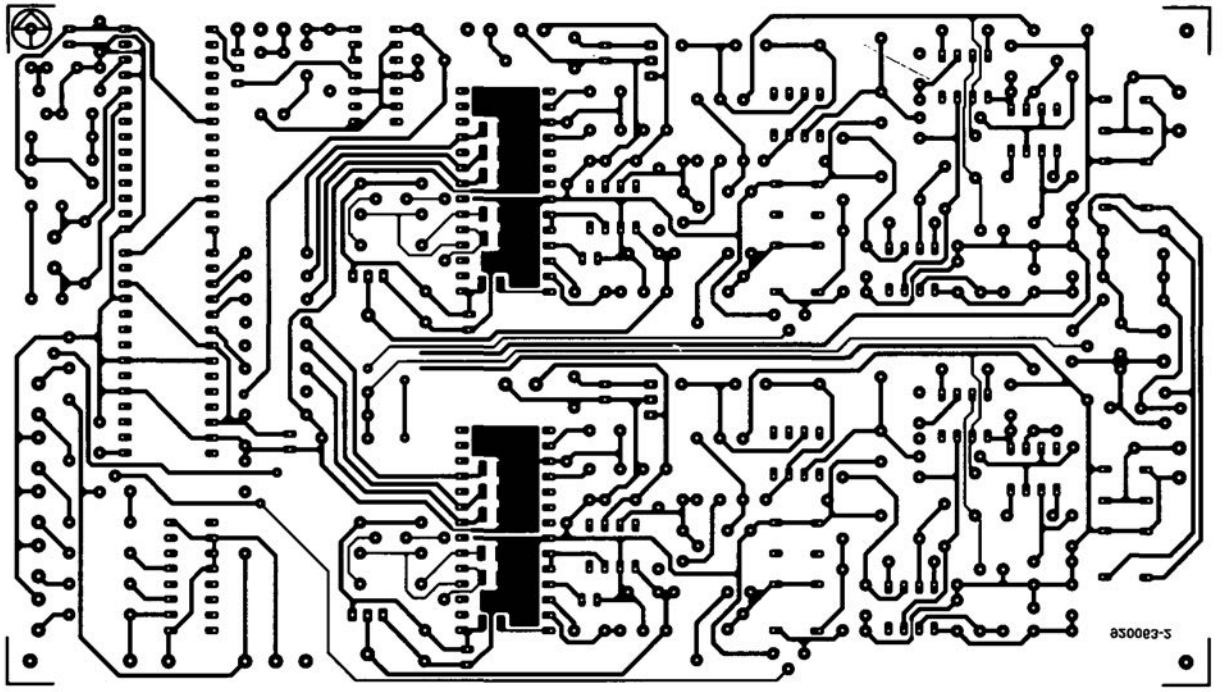
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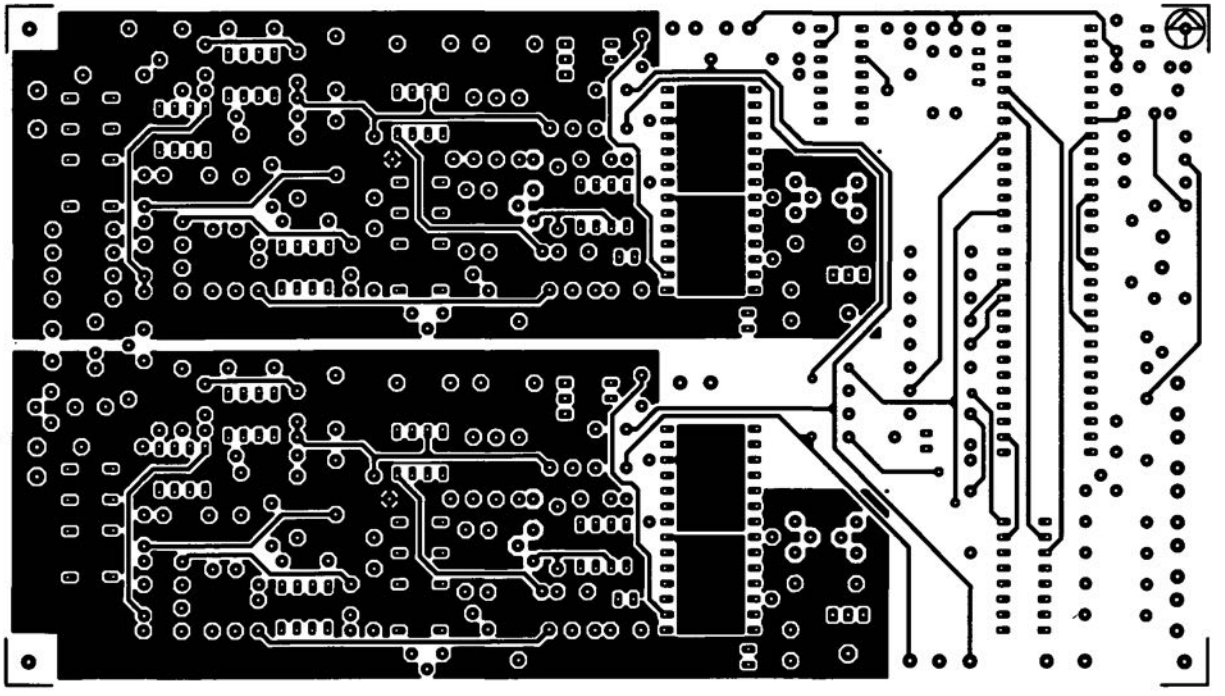


CORRECTIONS AND UPDATES

Digital Audio/visual system (Multi-purpose Z80 card)

May and June 1992
An extensive description of a modification to the memory backup circuit on the Multi-purpose Z80 card is available free of charge through our Technical Queries service.

FM stereo signal generator

May 1993
Capacitors C17 and C19 should have a value of 33nF, not 3nF3 as indicated in the circuit diagram and the parts list of the multiplex generator.

Workbench PSU

May 1993
The polarity of capacitor C15 is incorrectly indicated on the PCB component overlay (Fig. 5a), and should be reversed. The circuit diagram (Fig. 2) is correct.

Transformer TR2 is incorrectly specified in the circuit diagram (Fig. 2) and in the parts list. The correct rating of the secondary is 2 × 12V/5A. Also note that the secondary windings are connected in series to give 24 V.

Audio DAC

September 1992
The polarity of capacitors C25 and C58 is incorrectly indicated on the component overlay of the D-A board (order code 920062-2), and should be reversed.

U2400B NiCd battery charger

February 1993
The value of resistors R17 through R27 should be 2.7kΩ, not 12.7kΩ as stated in the parts list.

VHF/UHF receiver

May 1993
In Fig. 4, the connections to ground of the AF amplifier outputs, pins 5 and 8, should be removed. The amplifier outputs are connected to the loudspeaker only. The relevant printed circuit board is all right.

8051/8032 ASSEMBLER COURSE

PART 6: ANALOGUE SIGNAL PROCESSING AND STACK MANAGEMENT

By Dr. M. Ohsmann

The first subject in this month's instalment is processing analogue signals with the aid of our extension board. Next, we have a short discourse on stack management, which is quite important when it comes to dealing with subroutines. The two subjects form a basis for the next theme: interrupt processing, which is also introduced in this instalment. As usual, the programs discussed are contained on the course diskette, and can be tested straight away using the 80C32 single-board computer and its extension board (see part 3).

D-A conversion

Many microcontroller applications are geared to processing and generating analogue signals. The SBC extension board contains a D-A (digital-to-analogue) converter which is ideal for developing such applications. This course instalment aims at showing you how this D-A converter can be used, in conjunction with the comparators on the extension board, to measure analogue values.

Conversion principle

One way of converting an analogue voltage into a corresponding digital value is based on the 'ramp' principle, which is illustrated in Fig. 28. A ramp-shaped voltage is output via a D-A converter, and increased until a comparator output signals that the instantaneous value of the ramp is greater than the input voltage. The previous DAC output value is then taken to equal the input voltage. The ramp voltage is simply generated by increasing a register value from 0, and sending this value to a DAC. An example of a program that does so is XAMPLE14.A51 on your course diskette. Since that is a relatively simple program, it will not be discussed here.

The main disadvantage of the ramp DAC principle is that it is relatively slow. In the worst case, at a resolution of 8 bits, the ramp value must be increased (and compared to the input voltage) no fewer than 255 times. Similarly, at a resolution of 12 bits, a maximum of 4,096 steps is required. Furthermore, each step should allow for the settling times of the DAC and the comparators. All in all, the ramp principle is too slow for many applications.

A faster DAC principle, which is also used in many DAC ICs, is called successive approximation. As shown below, it is relatively simple to implement in software.

During the successive approximation, the bits of the value to be converted are determined one by one. This means that eight steps are required to achieve 8-bit resolution. A register is used to determine which bit is 'measured'. The individual bits of the analogue value that are already known are also contained in a register. The principle of operation and a corresponding software flow chart are given in Figs. 29 and 30, respectively. Initially, the approximation value is set to 0, and the register that stores the shift bit is set to 1000 0000_2. The approximation starts with bit 7. A conversion cycle consists of the following steps: first, a new DAC output value is determined. This value is the sum (here: logic OR) of the shift bit and the approximation bit set up so far. This value is output to the DAC, and compared to the input value with the aid of the comparator. If the input voltage is greater than the DAC voltage, the new approximation value equals the previously sent comparator value. This approximation value has a '1' at the position of the shift bit. If the input voltage is smaller than the DAC voltage, the old approximation value is retained, which means that it has a '0' at the position of the shift bit. The above sequence determines the new bit in the approximation value. Next, the shift bit

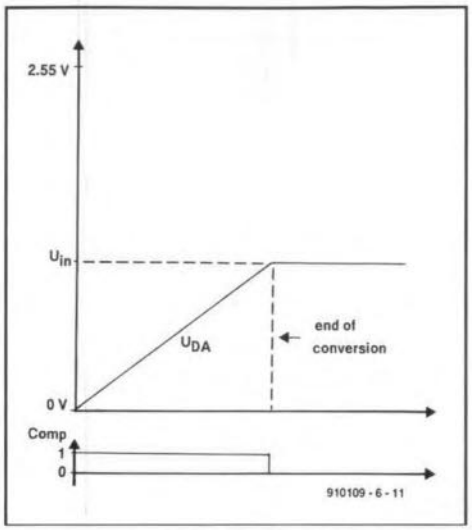


Fig. 28. Ramp A-D conversion principle.

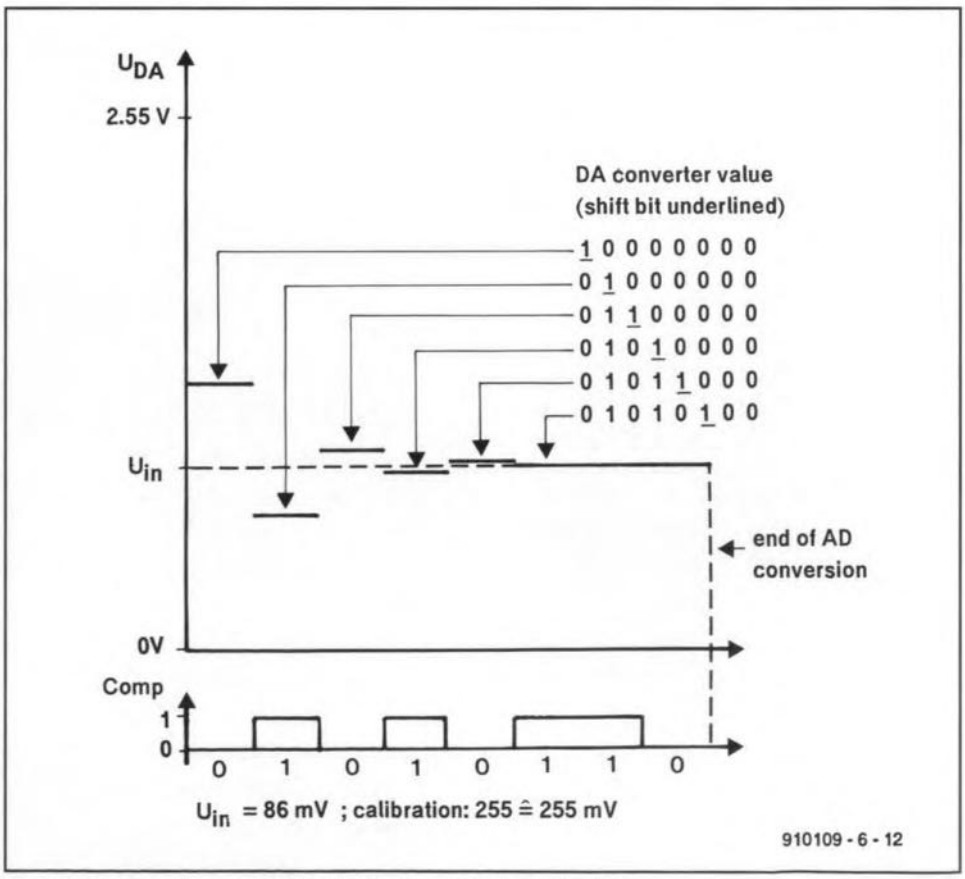


Fig. 29. Successive approximation D-A conversion principle.

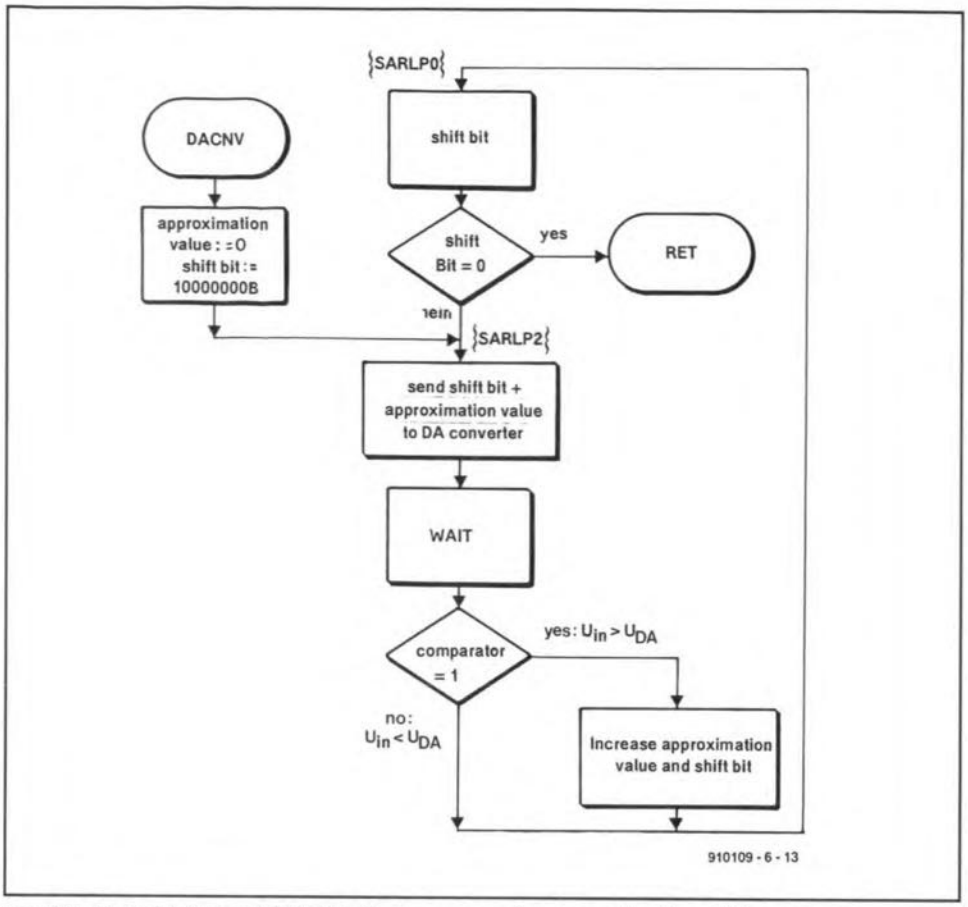
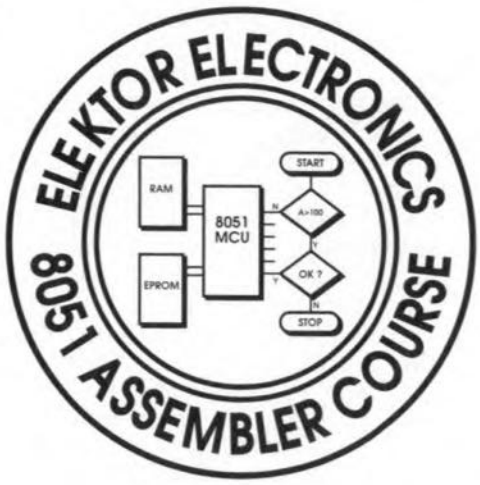


Fig. 30. Flow diagram of XAMPLE15, the successive approximation D-A converter.

```
****** LISTING of EASM51 (XAMPLE15) ******
LINE LOC  OBJ          T       SOURCE
   1 0000                      ; ****** FILE XAMPLE15.A51 ************************************
   2 0000                      ;
   3 0000                      P1      EQU 090H
   4 0000                      ;
   5 0000                              ORG   4100H             ; start address of program
   6 4100 7B 01       [1]  START       MOV   R3,#00000001B     ; mask channel 1
   7 4102 31 20       [2]              ACALL DACNV             ; call DA converter
   8 4104 31 44       [2]              ACALL BYTE              ; send byte and null character
   9 4106 31 4A       [2]              ACALL BLANK
  10 4108 7B 02       [1]              MOV   R3,#00000010B     ; channel 2
  11 410A 31 20       [2]              ACALL DACNV
  12 410C 31 44       [2]              ACALL BYTE
  13 410E 31 4A       [2]              ACALL BLANK
  14 4110 7B 04       [1]              MOV   R3,#00000100B     ; channel 3
  15 4112 31 20       [2]              ACALL DACNV
  16 4114 31 44       [2]              ACALL BYTE
  17 4116 74 0D       [1]              MOV   A,#13             ; line feed
  18 4118 31 4C       [2]              ACALL CHR
  19 411A 74 0A       [1]              MOV   A,#10
  20 411C 31 4C       [2]              ACALL CHR
  21 411E 80 E0       [2]              SJMP  START             ; infinite loop
  22 4120                     ;
  23 4120 D2 91       [1]  DACNV  SETB  P1.1          ; for oscilloscope
  24 4122 7E 00       [1]         MOV   R6,#0         ; approximation value
  25 4124 74 80       [1]         MOV   A,#080H       ; SHIFT-BIT
  26 4126 80 09       [2]         SJMP  SARLP2        ; jump into loop
  27 4128 EF          [1]  SARLP0 MOV   A,R7          ; get SHIFT-BIT
  28 4129 C3          [1]         CLR   C
  29 412A 13          [1]         RRC   A             ; shift right, fill with 0s
  30 412B 70 04       [2]         JNZ   SARLP2        ; continue when SHIFT-BIT<>0
  31 412D EE          [1]         MOV   A,R6          ; get result into A
  32 412E C2 91       [1]         CLR   P1.1          ; show end of conversion on scope
  33 4130 22          [2]         RET
  34 4131 FF          [1]  SARLP2 MOV   R7,A          ; save SHIFT-BIT in R7
  35 4132 4E          [1]         ORL   A,R6          ; add to approximation value
  36 4133 90 C0 00    [2]         MOV   DPTR,#0C000H
  37 4136 F0          [2]         MOVX  @DPTR,A       ; send to DA converter
  38 4137 FC          [1]         MOV   R4,A          ; mark sum for later
  39 4138 7A 64       [1]         MOV   R2,#100       ; settling time
  40 413A DA FE       [2]  SARWT  DJNZ  R2,SARWT      ; wait
  41 413C E0          [2]         MOVX  A,@DPTR       ; fetch comparator output
  42 413D 5B          [1]         ANL   A,R3          ; select desired KOMP.
  43 413E 60 E8       [2]         JZ    SARLP0        ; Bit=0 if Uin<Udac, do not set bit
  44 4140 EC          [1]         MOV   A,R4          ; Bit=1 if Uin>Udac
  45 4141 FE          [1]         MOV   R6,A          ; approximation value: =sum
  46 4142 80 E4       [2]         SJMP  SARLP0
  47 4144                     ;
  48 4144                     ; Monitor interface
  49 4144                     COMMAND EQU  030H
  50 4144                     MON     EQU  0200H
  51 4144                     ccCHR   EQU  001H
  52 4144                     ccBYTE  EQU  003H
  53 4144                     ;
  54 4144 75 30 03 [2] BYTE   MOV   COMMAND,#ccBYTE
  55 4147 02 02 00 [2]        LJMP  MON
  56 414A 74 20       [1] BLANK   MOV   A,#' '
  57 414C 75 30 01 [2] CHR    MOV   COMMAND,#ccCHR
  58 414F 02 02 00 [2]        LJMP   MON
  59 4152                     END
********** SYMBOLTABLE (13 symbols) **********
      P1 :0090      START :4100      DACNV :4120     SARLP0 :4128
  SARLP2 :4131      SARWT :413A    COMMAND :0030       MON :0200
   ccCHR :0001    ccBYTE :0003       BYTE :4144      BLANK :414A
     CHR :414C
```

Fig. 31. Listing of XAMPLE15.A51.



JOIN THE COURSE!

What you need to follow this course:

- **an 8032/8052AH-BASIC single board computer as described in Elektor Electronics May 1991. The preferred CPU is a 8051 or 80C32. Alternatively, any other MCS52-based microcontroller system (but read part 1 of the course);**
- **a course diskette (IBM: order code ESS 1661; Atari: order code ESS 1681) containing programming examples, hex file conversion utilities, and an assembler;**
- **a monitor EPROM (order code ESS 6091);**
- **an IBM PC or compatible operating under MS-DOS, or an Atari ST with a monochrome display.**

Appeared so far:

Part 1: Introduction (February 1992)
Part 2: First 8051 instructions (March 1992)
Part 3: Hardware extensions for 80C32 SBC (April 1992)
Part 4: Flags, bit addressing, PSW, conditional jumps, logic operators (June 1992)
Part 5: Arithmetic instructions (July 1992)

position is shifted to the right, and the next conversion cycle is run, until all bits are determined. In short, the bit to be determined is provisionally set, and compared to the input voltage. If this causes the approximation value to become too high, the bit is reset. If the approximation value is still too low, the bit is left set.

An A-D converter program

The program we are about to describe (Fig. 31) outputs the values of three input

voltages in hexadecimal notation. D-to-A conversion on all three channels is made possible by a subroutine called DACNV, which reads the bit position of the relevant comparator output from register R3. DACNV returns the converted value in the accumulator. The main program begins at label START, and is relatively simple. The bit corresponding to the channel number (1 of 3) is set in register R3. Next, The conversion proper, DACNV, is called. A subroutine called BYTE arranges for the value supplied by DACNV to be output (in hexadecimal form) via the V24 interface. After all three values have been sent to the terminal, the program adds a carriage return/line feed (CR/LF) sequence, and a new conversion cycle is started.

The D-A conversion is a bit more complex. The approximation value is stored in register R6. The shift bit is contained in register R7, and also, occasionally, in the accumulator. The sum of the shift bit and the approximation value is stored in register R4. The conversion proper starts at label SARLP2, where the accumulator contains the shift bit, and R6 the old approximation value. First, the shift bit is saved in register R7 (line 34). The sum of R6 and the accumulator is formed in line 35, and subsequently sent to the D-A converter. This comparison value is contained in R4. A wait loop, SRWT, is inserted to allow for the settling time of the DAC. The comparator output states are copied into the accumulator in line 41. Comparator output selection is achieved by masking the accumulator contents with the bit in R3 (line 42). Depending on whether the selected comparator output supplies a '1' or a '0', the corresponding new approximation value is formed in R6. The jump to label SARLP0 prepares for the next conversion step. The shift bit is loaded into the accumulator, and shifted to the right (lines 28 and 29). If the result is an accumulator content of 0, the conversion is finished. If not, the program continues at label SARLP2.

To enable us to trace the conversion steps with the aid of an oscilloscope (or by listening to the loudspeaker), port bit P1.1 is set during the conversion time. Figure 32 shows the signal reproduced by a digital storage oscilloscope. On completion of the D-A conversion, the value in RT6 is copied into the accumulator.

The advantages of the successive approximation principle are evident: only eight loop iterations are required. A fast DAC, and equally fast comparators, enable an 8051 to achieve 8-bit conversion times of 250 µs fairly easily. The corresponding sampling rate, 4,000 samples s^{-1}, is relatively high.

This program, like others discussed during this course, demonstrates the usefulness of subroutines. To understand how these are managed, it is necessary to have a look at the so-called stack, which is used by the 8051 to store certain data that serves to keep track of subroutine return addresses.

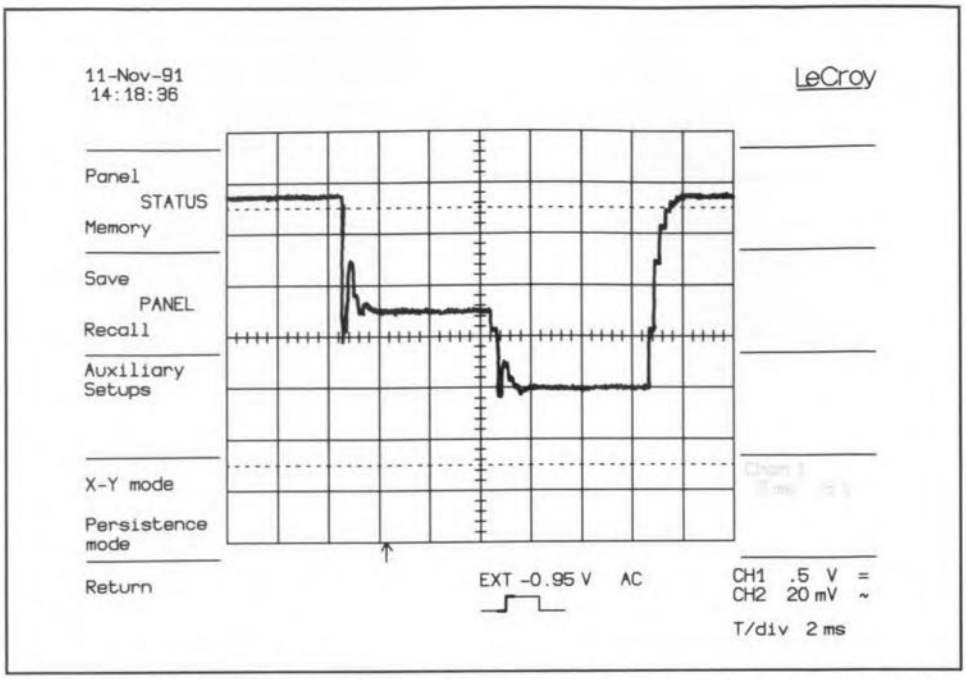


Fig. 32. A-to-D conversion waveform measured with an oscilloscope. Note the signal settling times.

Stacking it up

The stack pointer, SP (at SFR address 081H), points at an address in the stack range where the return addresses of subroutines and interrupt routines are stored. The stack pointer is contained in internal RAM, and is increased by one whenever a subroutine is called. Next, the first byte of the return address is written to the address pointed at by the SP. Next, the SP is increased by one, and the next address byte is stored. This little demonstration program

```
LINE    LOC     OBJ         T       SOURCE

43      4118    12 41 23    [2]     LCALL UPRO1
44      411B    00          [1]     NOP

47      4123    12 4A BC    [2]  UPRO1 LCALL UPRO2
48      4126    00          [1]     NOP

50      4ABC    85 08 44    [2]  UPRO2 MOV 68,8
                .....
```

results in the following stack values:

SP before line 43:	07H
Internal RAM address:	08 09 0A 0B 0C OD
Contents before line 43:	FF FF FF FF FF FF (preloaded)
Contents after line 50:	1B 41 26 41 FF FF (2 addresses on stack)
SP after line 50:	0BH

After a reset , the stack pointer contains the value '7' (refer back to Figs. 5 and 8), so that the stack begins at address '8' in the internal RAM, and grows upwards. This means that the stack overwrites register bank 1, and, possibly, other banks also. Register bank 1 is therefore not available for general programming, unless the SP is loaded with a new value right at the start of the program. When a program contains 'nested' subroutines, each of these requires two bytes of the available stack memory (which is contained in internal RAM).

The situation becomes even more complex when interrupts are programmed. Here, too, each return address calls for two bytes of storage capacity. Additional memory is required to hold saved SFRs, as well as all return addresses for subroutines called up by the interrupt program. The message is clear: make sure that you have sufficient stack room at all times! Users of the 8052, 8032 or 80C32 may avail themselves of the additional 128 bytes of internal RAM contained in these controllers. You may do so by programming

```
MOV  SP,#080H      ;upper RAM as stack
```

This gives a stack space of 128 bytes, which should be enough for most applications.

Saving data on to the stack

It often happens that a certain byte (SFR or accumulator) is to be put away safely, and retrieved a little later. This is achieved by

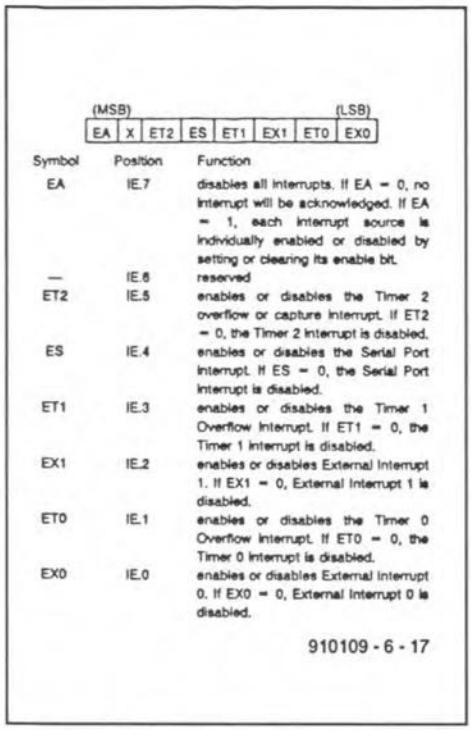


Fig. 34. Functions of individual bits in the interrupt enable register, IE.

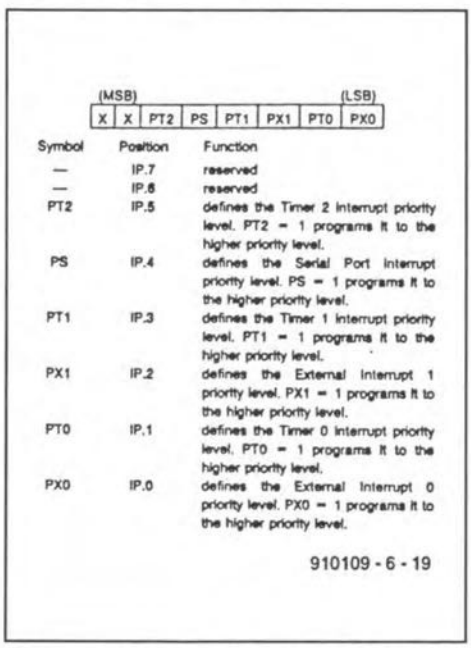


Fig. 36. Bits in the Interrupt Priority register, IP.

the instructions

```
PUSH  ACC        ;save accu on to
                  stack
.....            ;instructions in
                  between
POP   ACC        ;fetch accu from
                  stack
```

The PUSH instruction stores the indicated byte (direct addressing) on to the stack. Subsequently, the SP is automatically increased by one. The POP instruction fetches ('pops') the last PUSHed byte from the stack. Since storing (PUSHing) consumes stack space, the PUSH instruction should be used with care, since only limited space is available. The PUSH and POP instructions are often used within subroutines to rescue SFRs, which are then available again unchanged at the end of a subroutine.

Interrupt	Interrupt address	Link Index	Link Jump
IE0	0003H	1	4003H
TF0	000BH	2	4006H
IE1	0013H	3	4009H
TF1	001BH	4	400CH
RI+TI	0023H	5	400FH
TF2+EXF2	002BH	6	4012H

Fig. 33. Interrupt 'detours' contained in the system monitor program, EMON51.

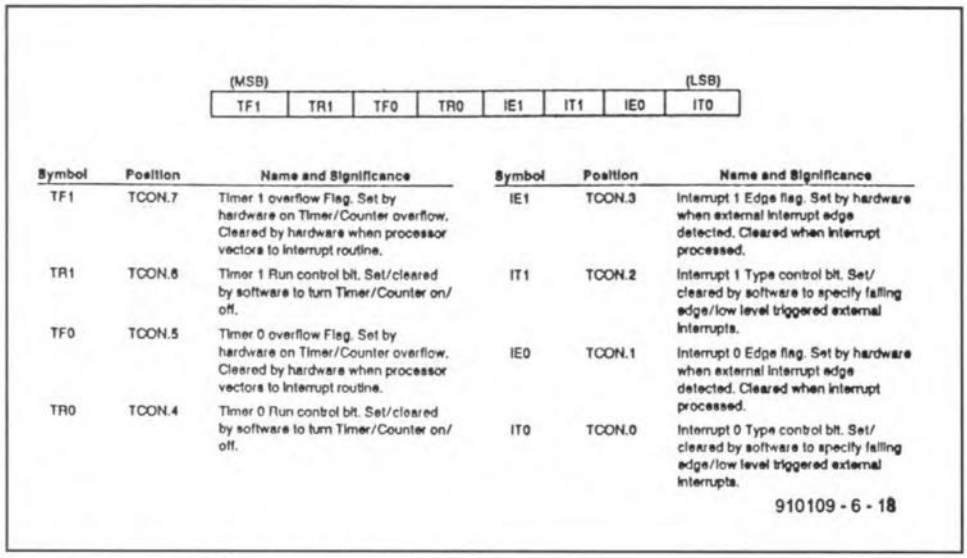


Fig. 35. Bits in the Timer Control register, TCON.

Interrupts

Interrupts are used whenever it is necessary for a program to respond as quickly as possible to external events. Such an event might be the arrival of a measurement value that is to be processed as fast as possible.

Interrupts from various sources can occur at any time during the program execution, which makes their programming and debugging complex, if not problem-

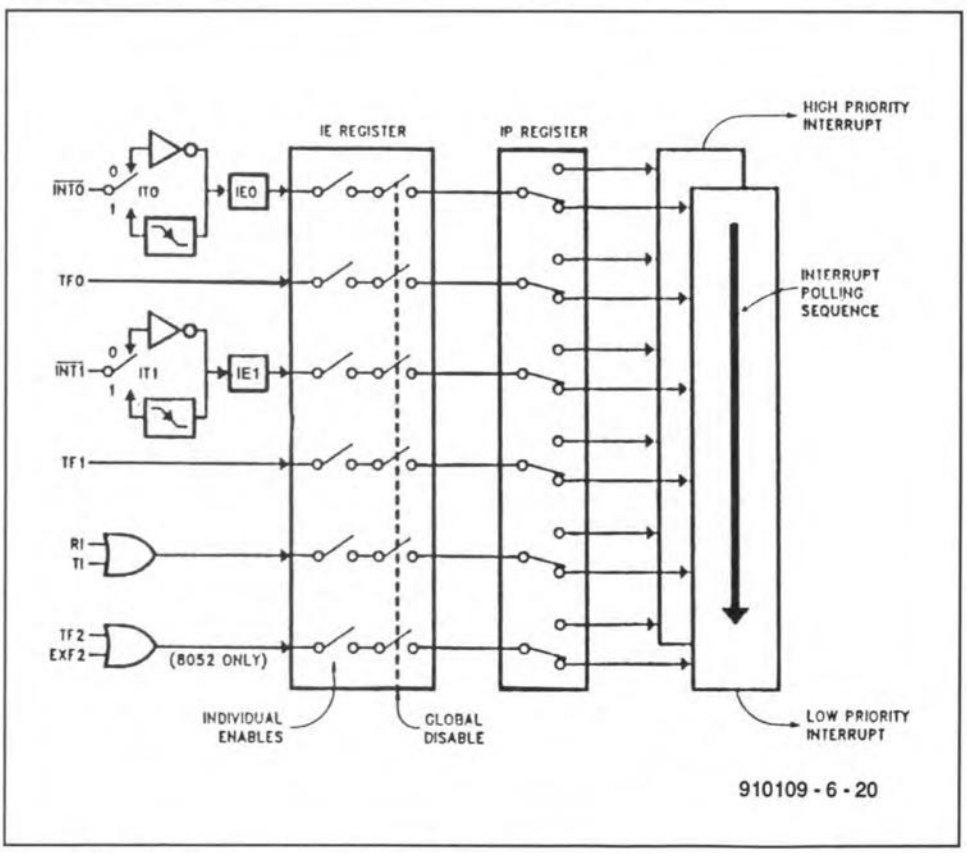


Fig. 37. 8051 interrupt control system structure.

atic. Beginners are, therefore, well warned against the many pitfalls that lurk in interrupt-controlled microcontroller systems.

The interrupt capabilities of the 8051 family are briefly discussed below. External interrupts are applied via IC input pins INT0 and INT1 (pins 12 and 13). On the 80C32 SBC, these two pins receive inverted signals that arrive via connector pins c3 and c5, and IC12. The user can select the interrupt mode beforehand: an interrupt occurs (1) on a signal edge only (positive edge on INT0), or (2) when INT0 = '1' (static logic level).

Further interrupt sources are Timer Flag0 and Timer Flag1 (TF0 and TF1), Receiver Interrupt (RI) and Transmitter Interrupt (TI). The 8052 and 8032 controllers have two more interrupt sources: Timer2 and external interrupt line EXF2. When an interrupt occurs, the processor executes a kind of LCALL instruction, which results in a jump to the address associated with the interrupt. Interrupt sources and associated addresses are listed in Fig. 33.

It will be noted that the interrupt addresses are normally in the memory reserved for EPROMs, and, therefore, not easily changed. Fortunately, the monitor EPROM (EMON51) provides so-called links, which are described in the file EMON51.DOC. The links allow interrupts to be called and relocated as required. For instance, the monitor causes interrupt IE0 to jump to address 4003H of the program memory, which is RAM. After a reset, the monitor loads this address with a jump to an internal interrupt routine. By calling the monitor subroutine LINK, you can change the jump address to point to your own interrupt. All that is required to set up this 'detour' is to have your interrupt address ready in the DPTR, and the index in the accumulator, before calling LINK. It should now be clear why we start our course programs at 4100H instead of 4000H: the lower page, 4000H to 40FFH, is used by the monitor.

The organization of the interrupts is arranged by the SFRs IE (interrupt enable; address 0A8H) and IP (interrupt priority; address 0B8H). Interrupts can be enabled or disabled selectively by setting or resetting the appropriate bits in IE, as shown in Fig. 34. Bits IT0 and IT1 (see Fig. 35) determine whether the external interrupts are level-triggered (bit='0') or edge-triggered (level='1'). Both bits are contained in the timer-control SFR, TCON, at address 088H (IT0 = TCON.0; IT1 = TCON.2). For a quick test, use the following little program (not on your course disk):

```
IE      EQU 08AH        ;new: interrupt
                         enable SFR
;
        ORG 4100H       ;program start
                         address
        MOV IE,#0FFH    ;all interrupts
                         on
FREVR   SJMP FREVR
        END
```

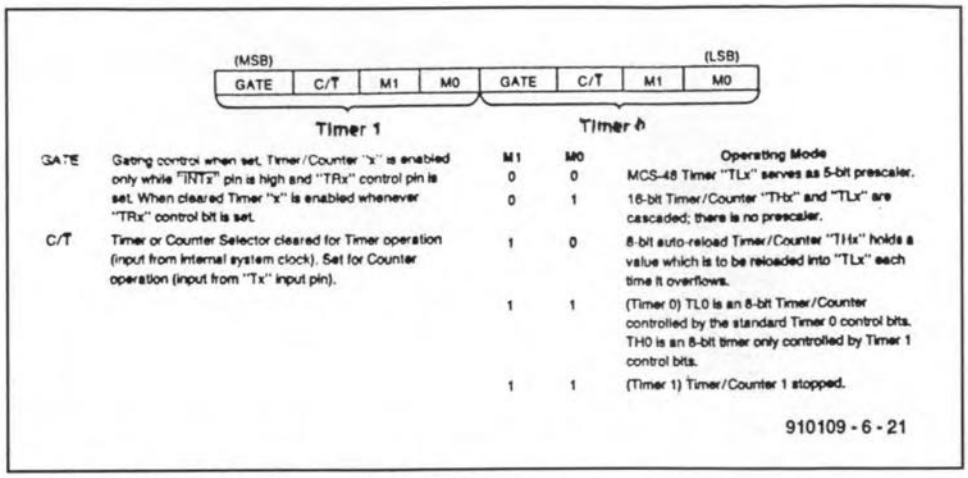


Fig. 38. Bits in the Timer-Mode register, TMOD.

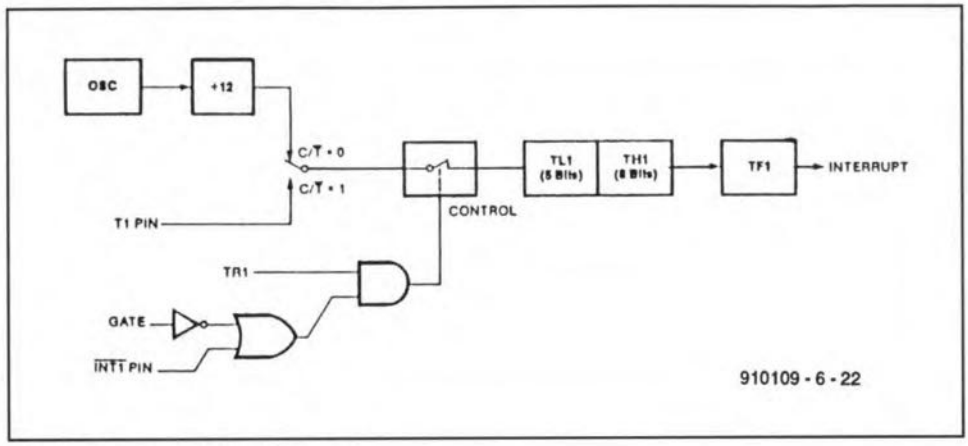


Fig. 39. Timer operation in Mode 0.

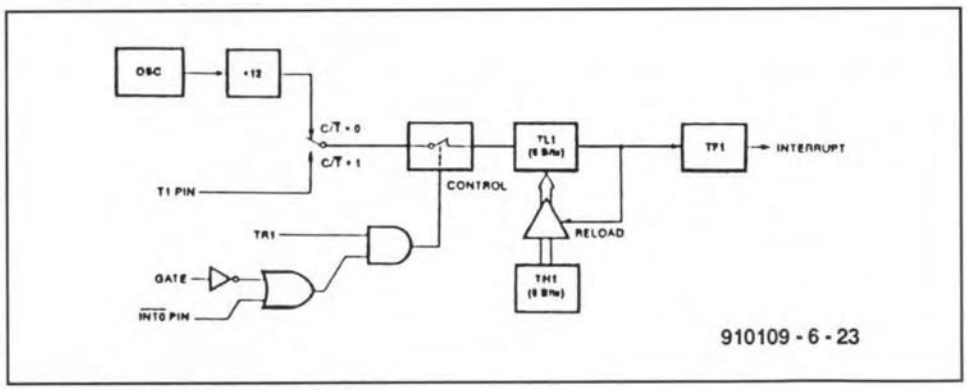


Fig. 40. Timer operation in Mode 2.

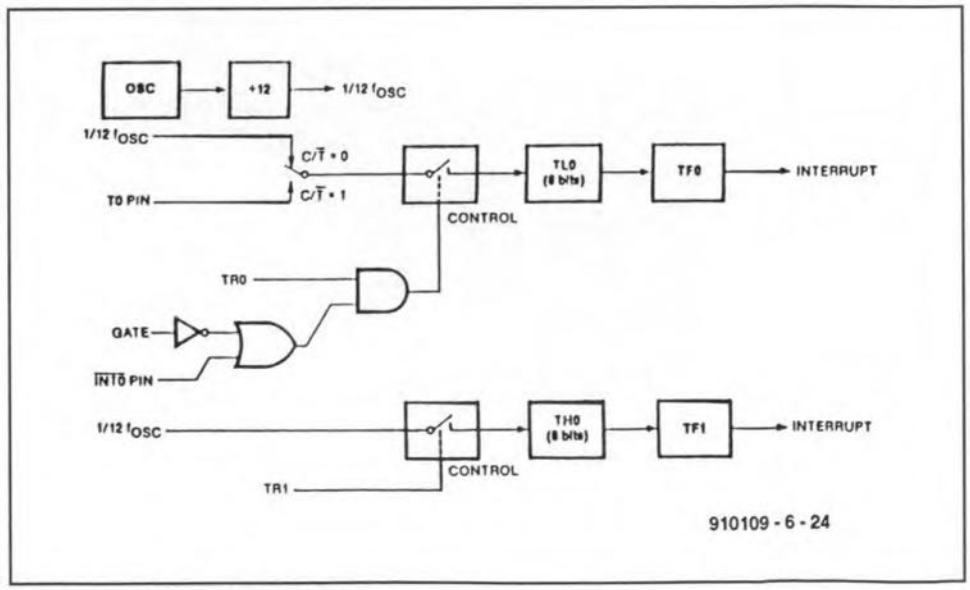


Fig. 41. Timer operation in Mode 3.

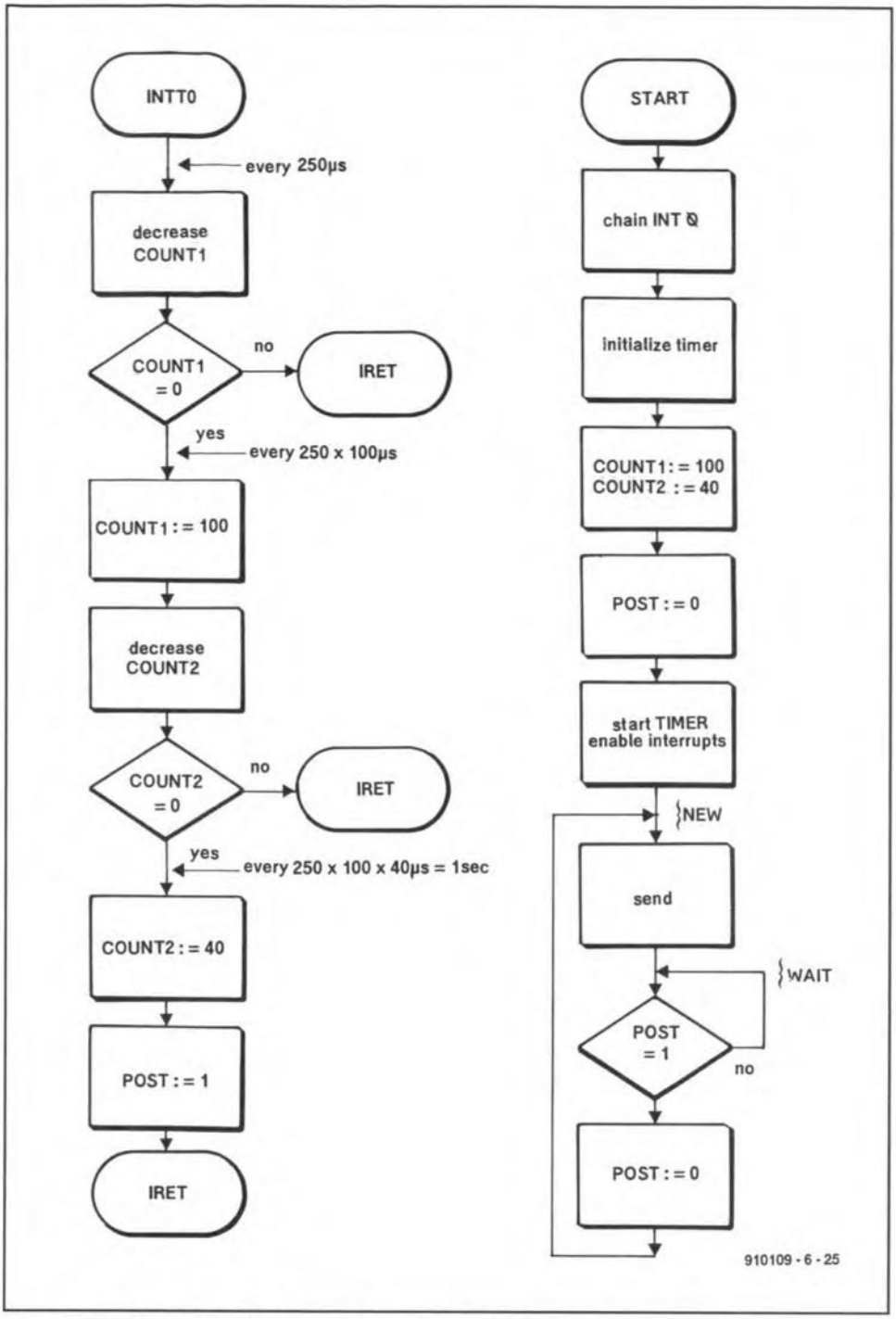


Fig. 42. Flow diagram of the seconds pulse generator program.

Assemble and run this program, and see what happens if you generate an interrupt by applying a +5 V pulse to connector pin c3 or c5. Can you explain what happens?

The 8051 has a low and a high interrupt priority level. An high-priority interrupt can interrupt the routine of a low-priority interrupt. Interrupts can be assigned a priority level by setting the appropriate bits in the interrupt priority SFR — see Fig. 36. Figure 37 shows an overview of the interrupt control system. It also shows the sequence followed to finish interrupt routines, when requests are received simultaneously (polling sequence).

Interrupt routines

When an interrupt occurs, and the 8051 is programmed to respond to it, the program jumps to the routine that belongs with the interrupt. To make sure that the 'interrupted' main program can continue without problems when the interrupt routine is finished, the interrupt routine must not contain instructions that change the registers used by the main program. This is usually ensured by PUSHing the SFRs right at the start of the interrupt service routine, and POPping them back again on return to the main program. To protect registers R0 to R7, the register bank is swapped. This requires a clear-cut subdivision to be defined of the register banks with the associated program levels, at the earliest stage of program development. Add to that the possible complications caused by the register banks and the stack, and it is readily seen that errors may creep in at any stage, and not come to light after a good deal of debugging.

To return from an interrupt to the main program, simply program

```
RETI            ;return from interrupt
```

Contrary to the RET instruction, RETI clears the bits that have triggered the interrupt. A practical example of interrupt programming is discussed together with the function of the timers.

Counters and timers

The 8051 has two counters that can be used to count events. When clocked with an internal signal, these counters may also be used as timers. Each timer is capable of working in different modes. The timer mode is programmed with the aid of an appropriate bit pattern in the associated SFR. Counter contents (states) can be read and preset via SFRs.

The SFR for timer mode control is called TMOD (SFR at 089H; not bit-addressable), while the SFR for timer control is called TCON (SFR at 088H, bit addressable). The function of the individual bits in these SFRs is shown in Figs. 35 and 38.

The lower-order byte of Timer/Counter 1 is addressable under the name TL1 at address 08BH. The higher-order byte is called TH1, and is found at address 08DH. The general mode of operation is determined by mode bits TMOD.4 and TMOD.5. When both are '0', the counter operates as a 13-bit counter. The interaction between the various bits and the external signals is shown in Fig. 39. The C/T bit allows you select between an internal timer clock (C/T = 0) and an external timer clock (C/T = 1).

The logic levels of the bits TR1, GATE, and the level at the INT1 pin, control when the counter ia actually operating. TR1, for instance, allows the counter to be switched on and off (provided GATE = 0). The TF1 flag is set whenever the counter changes from its maximum count to 0; in other words, when an overflow occurs. This flag can be interrogated by software, for instance, to trigger an interrupt. Note, however, that this requires bit 3 (IE3) in the interrupt register to be set.

When C/T = 0, the counter counts the quartz frequency divided by 12, i.e., 1 MHz in our case. In mode 1 (TCON.4 = 1; TCON.5 = 0), the counter counts exactly as in mode 0, but with a width of 16 bits.

In mode 2, the counter works as an 8-bit counter (the count value is contained in SFR TL1), which, on overflow, is reloaded with the value contained in TH1. (8-bit auto reload). This mode is illustrated in Fig. 40. In mode 3, the counter is simply halted.

In the system monitor, EMON51, Timer 1 is used as a baud rate generator. It can not be used for other purposes, unless you have no need for the serial interface.

Timer/Counter 0 operates largely like Timer/Counter 1; only the bits and SFRs

are different. The main difference is, however, that Timer 0 can also be used in mode 3 (TCON.0 = 1; TCON.0 = 1). In this mode it operates as two independent 8-bit counters/timers, as illustrated in Fig. 14. Note that the second 8-bit timer uses a couple of bits that actually belong to Timer 1. This means that these bits can not be used for Timer 1 when Timer 0 is programmed to operate in mode 3. Finally, the 8032 and 8052 processors have a further timer: Timer 2.

After this fairly large chunk of theory, we feel that it is time to turn to practice again. We have in mind a simple clock that operates under interrupt control, and leaves a signal for the main program every second. The main program waits for this signal to transmit an asterisk (*) via the serial interface. The program may be used as a basis to develop a digital clock that controls time-related functions (such as sounding a melody on your birthday).

Interrupt-controlled clock

We will first discuss the interrupt routine proper. The flow chart is given in Fig. 42, and the assembly code listing in Fig. 43 (program XAMPLE11 on your course diskette). The routine starts at label INTT0. Unfortunately, it is not possible to generate a one-second clock signal with a single timer. Even when we divide the internal clock with a 16-bit counter, the maximum time between two overflows is 65,536 µs, or about 0.065 s. We therefore adopt a different approach.

We use an interrupt rate of 4 kHz, which means that 250 µs elapse between two interrupts. This is simple to achieve by setting Timer 0 to auto-reload mode (mode 2), using 256–250 = 6 as the reload value. The flow chart shows that the interrupt routine counts up to 40×100 = 4000 with the aid of two sequentially arranged count bytes (COUNT1 and COUNT2). The variable COUNT1 counts down starting at 100. When it reaches 0, COUNT2 (which starts at 40) starts to count down. When COUNT2 reaches 0, a total of 250×4000 µs has elapsed, and the subroutine leaves 'POST' in the mailbox of the main program. The presence of POST is signalled by a bit.

Main program

The most difficult task of the main program is the correct initialization of the SFRs for the counter and interrupt control. First, the counter mode is loaded, and the mode-2 reload value is set (lines 25, 26 and 27). Note that Timer 1 must be left to operate in mode 2 to enable it to function as the baud rate generator. Next, the counter variables are set up. In lines 31, 32 and 33, the counter is started, and the interrupts are enabled. The rest of the main program is a simple loop. Starting at label NEW, the program first sends an asterisk via the serial interface. Next, it waits for POST in the loop that starts at label WAIT. The presence of the seconds pulse is signalled by the variable POST being unequal to 0. When the POST is fetched, the variable is reset to 0 before looping back to the start of the main program.

```
****** LISTING of EASM51 (XAMPLE11) ******
LINE LOC  OBJ          T       SOURCE
   1 0000                 ; ****** FILE XAMPLE11.A51 ********************************
   2 0000                 ;
   3 0000                 IE      EQU     0A8H
   4 0000                 ACC     EQU     0E0H
   5 0000                 PSW     EQU     0D0H
   6 0000                 TCON    EQU     088H      ; new : Timer/Counter Control
   7 0000                 TMOD    EQU     089H
   8 0000                 TL0     EQU     08AH
   9 0000                 TH0     EQU     08CH
  10 0000                 ;                         ; 250*100*40 microsec = 1 sec
  11 0000                 T0valu  EQU     250       ; 250 microsec for TIMER 0
  12 0000                 TIME1   EQU     100       ; no. of loops for COUNT1
  13 0000                 TIME2   EQU     40        ; no. of loops for COUNT2
  14 0000                 ;
  15 0000                         ORG 050H          ; via MONITOR RAM
  16 0050                 COUNT1    DS  1           ; Software COUNTer 1
  17 0051                 COUNT2    DS  1           ; COUNTer 2
  18 0052                 POST      DS  1           ; 1 means 1 sec has lapsed, else 0
  19 0053                 ;
  20 0053                         ORG   4100H
  21 4100 90 41 34 [2] START    MOV   DPTR,#INTT0     ; chain interrupt routine
  22 4103 74 02    [1]          MOV   A,#2
  23 4105 75 30 40 [2]          MOV   COMMAND,#ccLINK
  24 4108 12 02 00 [2]          LCALL MON
  25 410B 75 8C 06 [2]          MOV   TH0,#256-T0valu ; every 250 microseconds
  26 410E 75 8A 06 [2]          MOV   TL0,#256-T0valu ; one interrupt from TIMER0
  27 4111 75 89 22 [2]          MOV   TMOD,#022H      ; both COUNTers MODE2 2
  28 4114 75 51 28 [2]          MOV   COUNT2,#TIME2   ; preset software COUNTer
  29 4117 75 50 64 [2]          MOV   COUNT1,#TIME1
  30 411A 75 52 00 [2]          MOV   POST,#0         ; no post
  31 411D D2 8C    [1]          SETB  TCON.4          ; start TIMER0
  32 411F D2 A9    [1]          SETB  IE.1            ; switch TIMER0 interrupt on
  33 4121 D2 AF    [1]          SETB  IE.7            ; interrupts on
  34 4123 74 2A    [1] NEW      MOV   A,#'*'          ; send asterisk
  35 4125 75 30 01 [2]          MOV   COMMAND,#ccCHR
  36 4128 12 02 00 [2]          LCALL MON
  37 412B E5 52    [1] WAIT     MOV   A,POST          ; wait
  38 412D 60 FC    [2]          JZ    WAIT            ; for POST
  39 412F 75 52 00 [2]          MOV   POST,#0         ; get POST
  40 4132 80 EF    [2]          SJMP  NEW             ; repeat
  41 4134                 ;
  42 4134 C0 D0    [2] INTT0  PUSH  PSW             ; save
  43 4136 C0 E0    [2]        PUSH  ACC
  44 4138 D5 50 0C [2]        DJNZ  COUNT1,IRET1    ; decrement software counter 1
  45 413B 75 50 64 [2]        MOV   COUNT1,#TIME1   ; reload when 0 is reached
  46 413E D5 51 06 [2]        DJNZ  COUNT2,IRET1    ; and decrement software counter 2
  47 4141 75 51 28 [2]        MOV   COUNT2,#TIME2   ; reload when 0 is reached
  48 4144 75 52 01 [2]        MOV   POST,#1         ; and leave POST
  49 4147 D0 E0    [2] IRET1  POP   ACC             ; after storage
  50 4149 D0 D0    [2]        POP   PSW
  51 414B 32       [2]        RETI                  ; end of interrupt
  52 414C                 ;                       MONITOR INTERFACE
  53 414C                 COMMAND EQU  030H   ; MONITOR command memory location
  54 414C                 MON     EQU  0200H  ; MONITOR jump address
  55 414C                 ccLINK  EQU  040H   ; Interrupt chaining
  56 414C                 ccCHR   EQU  001H   ; send character
  57 414C                         END
********** SYMBOLTABLE (22 symbols) **********
       IE :00A8       ACC :00E0       PSW :00D0      TCON :0088
     TMOD :0089       TL0 :008A       TH0 :008C    T0valu :00FA
    TIME1 :0064     TIME2 :0028    COUNT1 :0050    COUNT2 :0051
     POST :0052     START :4100       NEW :4123      WAIT :412B
    INTT0 :4134     IRET1 :4147   COMMAND :0030       MON :0200
   ccLINK :0040     ccCHR :0001
```

Fig. 43. Listing of the seconds pulse generator program, XAMPLE11.

Assignments

An interesting assignment to work on after studying the material presented here would be to design a program that reads the input voltages at all three analogue inputs of the extension board, and outputs the digitized values via the serial port, say, every minute. If you find that too easy, have a go at outputting decimal values multiplied by certain correction factors.

Another idea is to program a software window comparator that sends an 'OK' message to the terminal when the voltage at analogue input 2 of the extension board is between the voltages at inputs 1 and 3.

Next time

The next course instalment will tackle the serial port of the 8051. The application will be software for a simple MIDI sequencer. In addition, we will show you how to connect an LC display to the 80C32 SBC. ❑

23-CM FM TRANSCEIVER

This transceiver was designed in response to a need for a simple, easy to build, self-contained radio for use through the local 23-cm (1.3-GHz) repeater, as either a mobile or a fixed station. The design draws heavily on circuitry and techniques employed in 900-MHz portable phones, modified to suit amateur needs. It is hoped that this design will prove of interest to others and create more activity on this largely underused band.

By T. Forrester G4WIM

Unit operation

As the design is primarily intended for mobile working, the controls have been kept to a minimum whilst maintaining features required for efficient operation.

The prototype combined the transceiver on/off with the channel select switch in order to save front panel space. The design permits diode programming of up to 5 channels; this number could obviously be increased by using a larger diode matrix or some form of memory. A toggle switch selects either simplex or repeater working. For the latter function a tone burst button is provided which also keys up the transmitter.

There are conventional volume and squelch controls and sockets for external microphone and speaker, as required. The prototype was slightly modified to be compatible with the ICOM HS51 mobile headset. Details of this modification are available on request from the author.

Circuit operation

Figure 1 shows the simplified overall block diagram, high-lighting the most important areas of the design. Figure 2 shows the detail of the receiver circuitry. The incoming signal passes through the aerial change-over relay which is a 960-MHz strip line type having good isolation and an insertion loss of less than 0.5 dB at 1.3 GHz. The RF pre-amplifier (TR9) is a low-noise Avantek GaAs FET, so ensuring excellent sensitivity. The pre-amplifier feeds a ready-made three- stage helical filter (FL3) to heavily attenuate the image response 90 MHz below the receive frequency. Following the helical filter is a low noise MMIC (IC17) providing a further 13 dB of gain and 50-Ω output impedance to drive the SBL1-X diode ring mixer (D8). This mixer is operated slightly above its maximum frequency rating, but experience has shown that the conversion loss increases only slightly and is amply compensated for by the preceding low-noise amplifiers.

The local oscillator signal, which is 45 MHz below the desired receive frequency, is supplied by a synthesizer, see below.

The output of the mixer is passed to the first IF amplifier (TR12). This stage is a low-noise grounded gate FET amplifier whose input impedance is approximately 50 Ω, so providing the diode ring mixer with a reasonable load.

The drain load of TR12 is tuned and loaded to match the following 45-MHz crystal filter. Likewise, the second IF amplifier (TR13) has a tuned and loaded input circuit to match the output of the filter. The 45-MHz IF signal is now at a sufficiently high level to be further processed by IC6.

The 45-MHz signal applied to pin 18 of IC6 is mixed down to an IF frequency of 455 kHz, where it is demodulated and filtered before being passed on to the audio power amplifier (IC5). IC6 also provides the mute function (Fig. 3).

Referring to Fig. 5, on transmit, TR1 is turned on, so that the relevant transmitter sections are powered, and the simplex or repeater transmit offsets are added in to IC1 through to IC3: see the notes on programming below for further details.

The output signal at the collector of TR1 is used to operate the PIN diode switch within the VCO, so routeing the signal from the receive mixer to the RF power amplifier module (PA1). It also powers the microphone stages (TR4 and TR5), activates the varactor diode used for FM transmit (D15) and turns on TR6, so operating RL1 which in turn provides bias for PA1 via TR7. The receiver front end is powered down as TR8 is turned off.

By selecting a jumper between either pins 1 and 2 or pins 2 and 3 on PL6, it is possible to run the final stage of the power amplifier from either 8 V or 13.8 V. The latter supply level generates 2 watts of RF output as opposed to 1 watt.

The heart of the frequency synthesizer uses a Motorola MC145152P2 (Fig. 4) and a 64/65 prescaler combined with some simple logic to provide 25-kHz channel spacing, 6-MHz down shift for repeater access and a 45-MHz offset required for the receiver local oscillator.

The VCO and buffers make extensive use of surface mount parts to create a compact VCO which is very rugged and practically

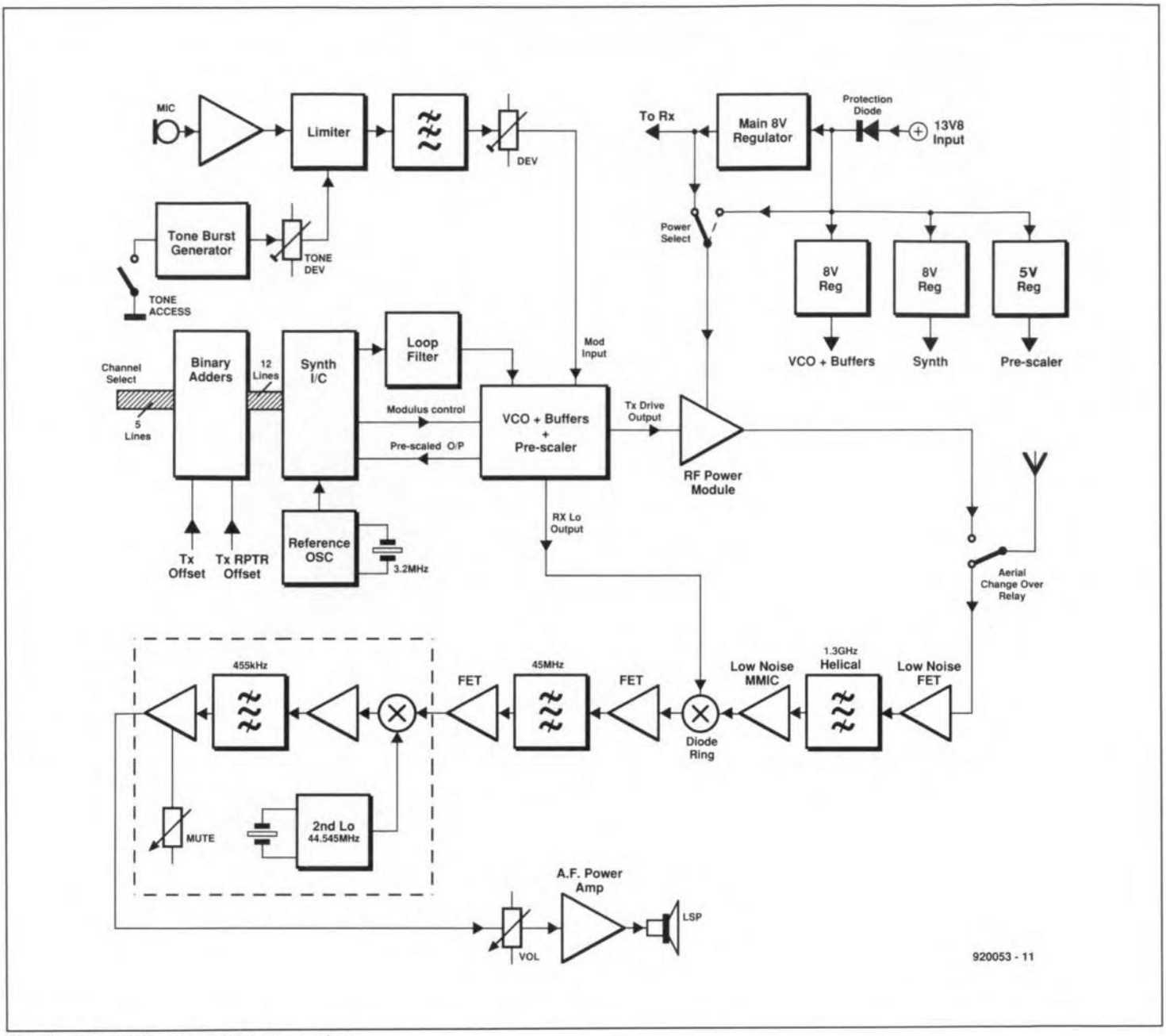


Fig. 1. Block diagram of the transceiver.

immune to vibration.

The pre-scaler (IC13) is a dual-modulus ÷64/÷65 type controlled by the modulus control output of IC11. IC11 is run at 8 V to ensure reliable operation, while IC13 needs to run off 5 V. Level shifting between these two ICs is provided by R83, C45 and D5. This combination also minimizes overall modulus control delay between the two ICs, a critical factor when using dual-modulus prescaling at these very high frequencies.

The loop filter around IC10 needs little comment, and is designed to the Motorola data sheet, attenuating the 25-kHz reference frequency to below –55 dBc. This level of attenuation, while not perfect, is more than adequate for a low-power radio such as this. IC10 is powered from the main 13.8 V supply, filtered by R21 and C53, so providing maximum available output swing.

The reference for the synthesizer is generated by XL1 and TR3. An external reference oscillator was employed as it was possible to design a oscillator with a better frequency stability than using the internal circuits of IC11. At 1.3 GHz, stable frequency generation is a must for reliable communication.

During the transition from receive to transmit, the synthesizer is unlocked for approximately 100 ms until it settles on its new operating frequency. As there is no circuitry to detect synthesizer unlock and disable the RF power amplifier, a carrier momentarily sweeps on to frequency. While this situation is not ideal, it was thought that the extra circuitry involved did not merit being included given the low power output and level of band occupancy.

If any constructor wishes to disable the RF power amplifier while the synthesizer is unlocked, the author can supply the necessary details.

Finally, IC4 provides a simple 1750-Hz tone access for repeater working.

Programming

Since the synthesizer has to generate three possible frequencies for each channel, i.e., receive LO, transmit simplex and transmit repeater, the data presented to IC11 has to be modified according to the mode in use.

Assuming that the unit is receiving on 1297.125 MHz, the LO must be on 1297.125 MHz–45 MHz i.e., 1252.125 MHz. Also, since we are working with a channel spacing 25 kHz, the LO frequency must be scaled down (i.e., divided) by a factor 1252.125 MHz/25 kHz = 50085.

This factor of 50085 needs to be further reduced before it is programmed into the 'A' and 'N' counters of IC11. Since we are using a divide-by-64 prescaler, the 'N' count for IC11 is the integer 50085/64 i.e., 782, the remainder of 37 is used for the 'A' count.

So, to operate on 1297.125 MHz the 'N' count is 782 and the 'A' count is 37. Because we only need to cover the 1297 MHz to 1298 MHz section on the band on receive, it is possible to hard-wire some of the higher-order control lines of IC11. A close check on all the required codes reveals that binary weights 512 and 256 can be permanently held true. This means that from a control aspect 'N' of 782 is reduced by 768 to 14,

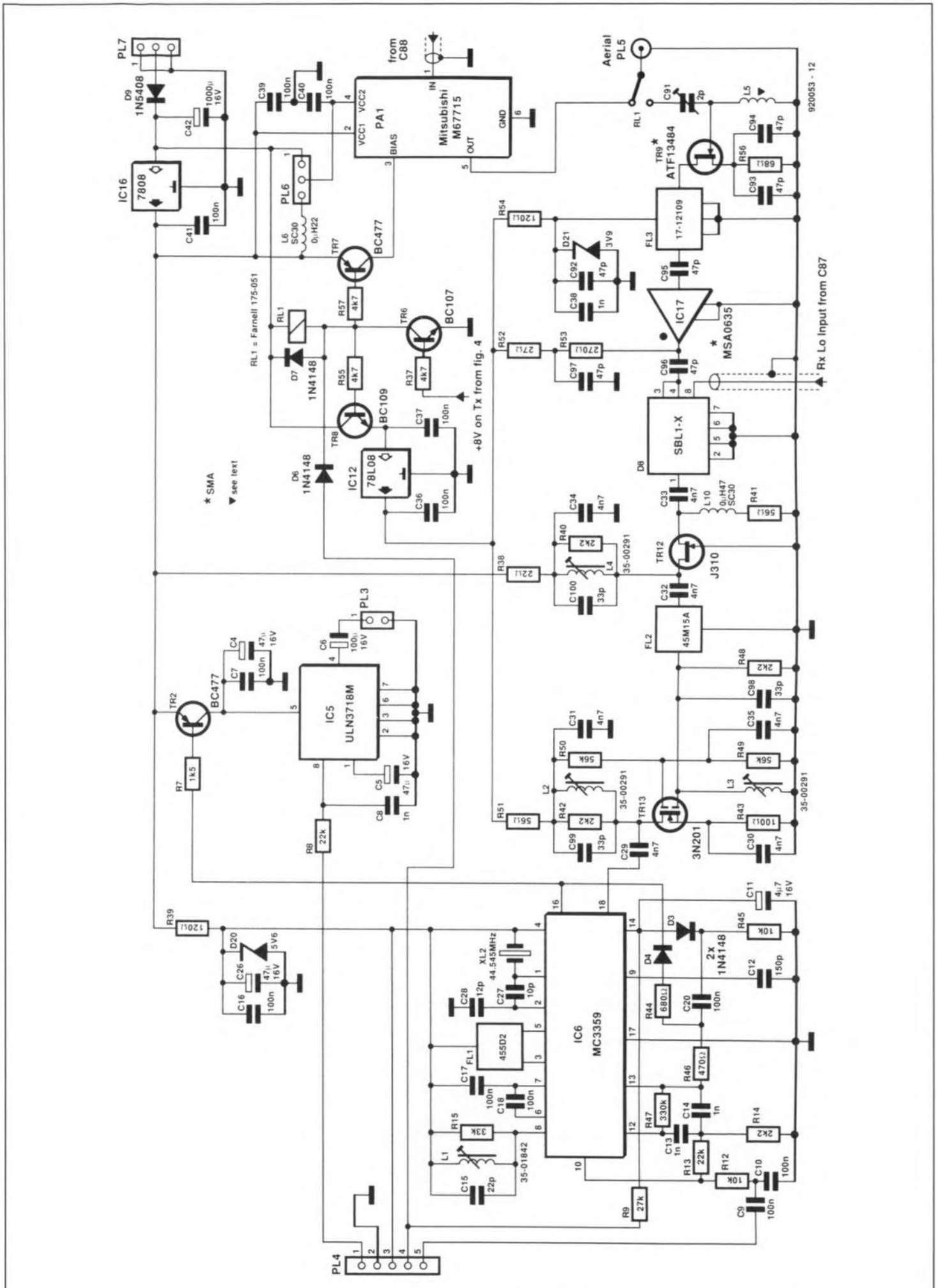


Fig. 2. Circuit diagram of transmit power amplifier, and receiver. Note: SMA = surface mount assembly.

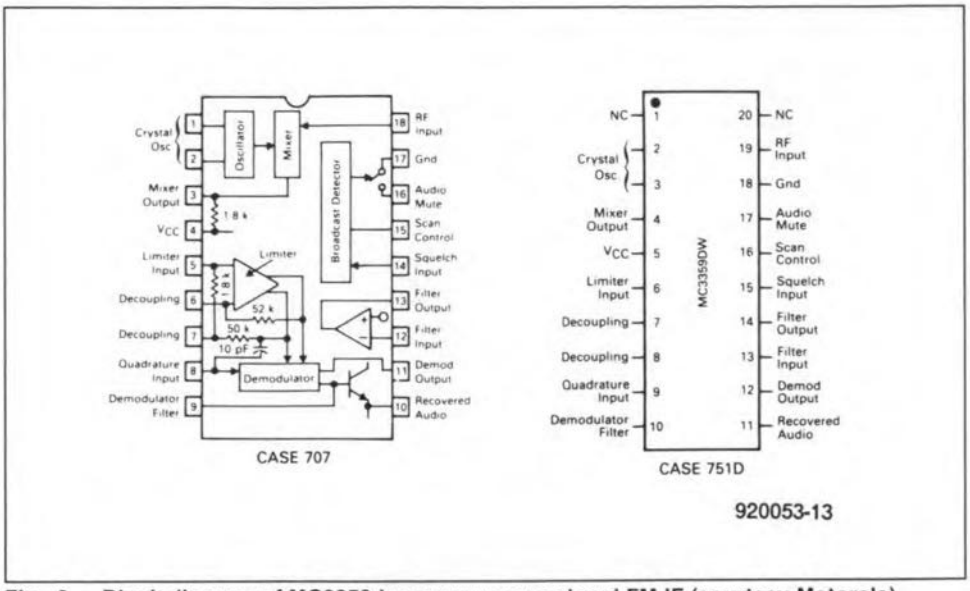


Fig. 3. Block diagram of MC3359 low-power narrowband FM IF (courtesy Motorola).

thereby reducing the number of lines that need to be manipulated. The actual number range becomes 13, 14 or 15 when covering 1296 MHz to 1298 MHz, and is accounted for automatically in the adders (IC2, IC3 and IC4).

To operate at 1291.125 MHz 'transmit' (repeater input for 1297.125 MHz), the synthesizer has to be shifted up by 39 MHz i.e., the count has to increase by 39 MHz/25 kHz=1560. Converting this to 'N' plus 'A' format gives 'N'=24 and 'A'=24.

If, instead, transmit on 1297.125 MHz was required, then 45 MHz would need to be added, i.e., the count has to increase by 45 MHz/25 kHz=1800. Converting this to 'N' plus a format gives 'N'=28 and 'A'=8.

By comparing the above bit patterns required for these two offsets, it becomes apparent that, on transmit, only the '4' weight needs to be changed in the 'N' count, and the '16' weight in the 'A' count, to select either simplex or repeater transmit. All other weights are required regardless of which transmit mode is chosen.

The addition of either of these two offsets to the receive base numbers is easily accomplished by binary adders IC1, IC2 and IC3.

So, to recap, to calculate the numbers — and hence diodes — required for a given channel:

1. Calculate the RX local oscillator (LO) frequency (F_{sig} –45 MHz).
2. Scale down this frequency by a factor (RX LO Freq./25 kHz).
3. Convert to 'N' plus 'A' ('N' overall/64='N'; remainder='A').
4. Subtract 768 from 'N'. This result should be either 13, 14 or 15 when programming receive frequencies between 1296 and 1298 MHz.
5. Convert 'A' (remainder from 3. above) to binary, i.e., 1, 2, 4, 8, 16, 32.
6. Insert diodes from the selected channel number to the binary weights required to program the given 'A' and hence the desired frequency. When fitting the diodes, ensure that they all 'point' towards R3.
The lines on the silk screen around the diode matrix area show where diodes need to be inserted to program the following frequencies to the associated channel.

Channel 1: 1297.125MHz (RM5)
Channel 2: 1297.000MHz (RM0)
Channel 3: 1297.075MHz (RM3)
Channel 4: 1297.150MHz (RM6)
Channel 5: 1297.500MHz (SM20)

Fitting no diodes at all would cause the radio to operate on 1296.200 MHz, and could be useful for monitoring SSB activity.

To make the radio more flexible, a small add-on PCB is being designed which will replace IC1, IC2 and IC3. This circuitry will allow any repeater shift to be programmed, listen on input, and will also permit the use of thumbwheel or similar switches. The programming data will be held in an EPROM mounted on the PCB.

Construction

It is easiest to fit all the surface mount parts first (on the track side of the PCB). A steady hand, a pair of tweezers and some patience are very necessary to make sound joints. Take time to make sure that the VCO section in particular is well put together as eventually it will be covered by a metal box making subsequent repair less easy. A close-up of the VCO area is shown in Fig. 8.

Note that C93 and C94 are mounted through the PCB after their holes have been cleared out with a 1.5-mm drill (to remove the through hole plate). This ensures that the source leads of TR9 are effectively by-passed to the ground plane.

After all the surface mount parts have been fitted, proceed with the remaining resistors and capacitors, followed by the rest of the ICs. Take care not to make any shorts between component leads and the ground plane.

Finally, fit the Molex connectors, relay, crystals and IC16 bolted to a good heatsink. Do not at this stage fit the RF power amplifier.

Before applying power for the first time check that the board has been correctly assembled and that there are no obvious wiring faults.

Testing and alignment

The transceiver is built on one high-quality through-plated, silk screened, solder resisted PCB of about 127 mm × 185 mm,

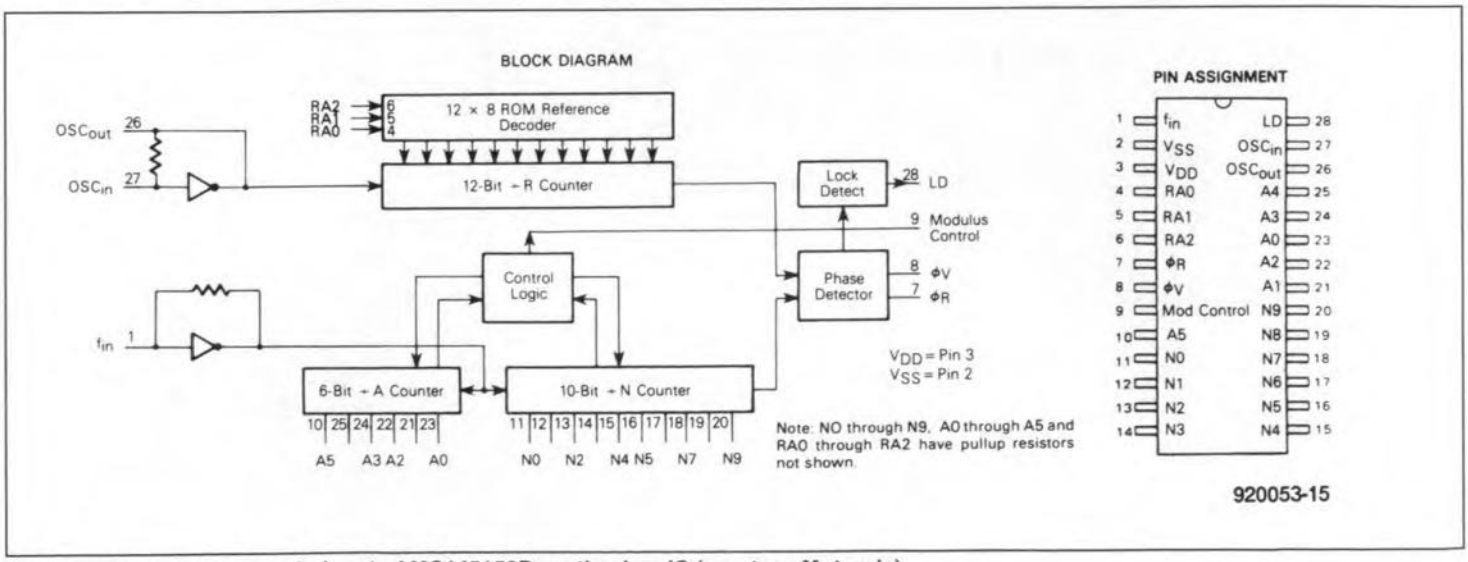


Fig. 4. Block diagram and pinout of MC145152P synthesizer IC (courtesy Motorola).

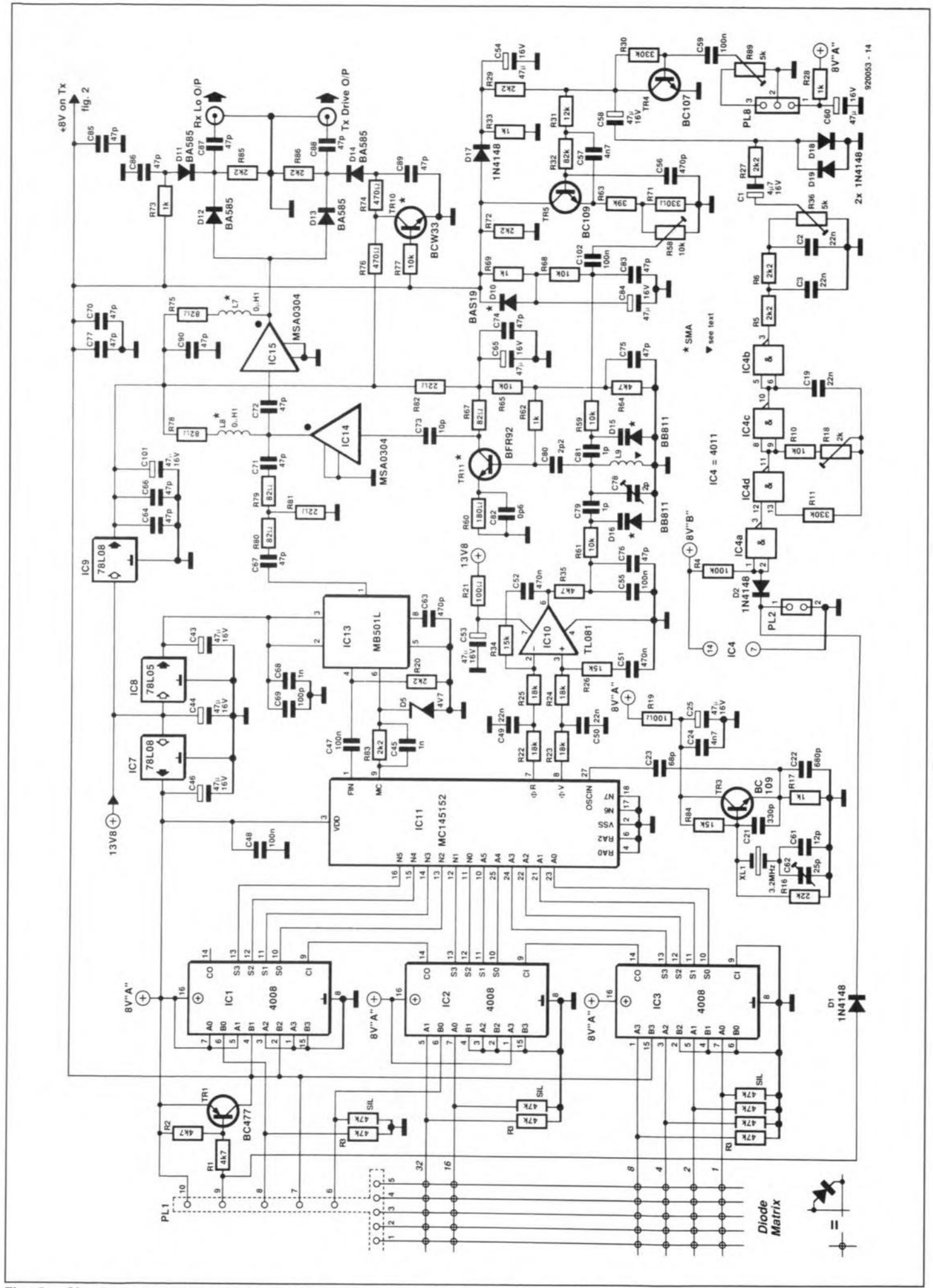


Fig. 5. Circuit diagram of synthesizer and FM modulator. Note: SMA = surface mount assembly.

which is designed to fit inside a standard die cast box or similar case. The PCB and a number of components to build the transceiver are available from the author.

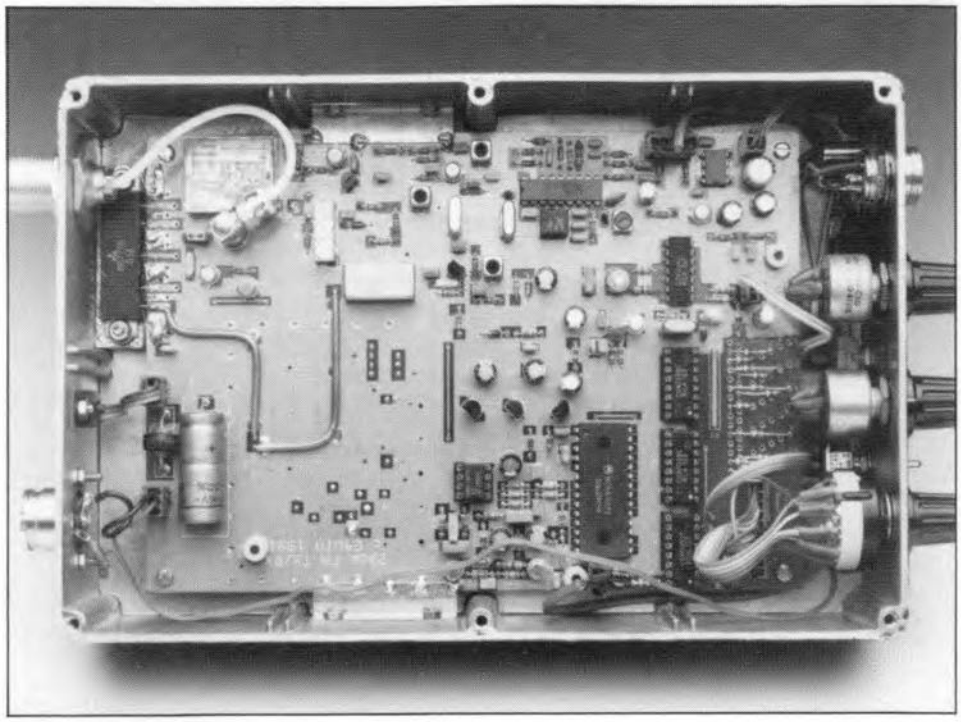
It is possible to align and test most of the PCB without installing it in its case. Only when the RF power amplifier is to be tested does the unit need to be installed in its case.

It is assumed that the unit has been diode programmed to the desired set of frequencies.

Make all the connections as shown in Fig. 6, and turn the unit on. The supply current should be circa 250 mA with the receiver muted. If the current is vastly more or less, there is probably a fault.

Adjust C78 for a voltage of between 4 V and 5 V on pin 6 of IC10. If necessary, slightly adjust the height of L9.

Turn off the power, and place the VCO cover on the PCB. Mark where the signal tracks would short to the cover. File these areas slightly (0.5-mm clearance is plenty). Carefully place the VCO cover box on the PCB and turn on the power. The voltage on



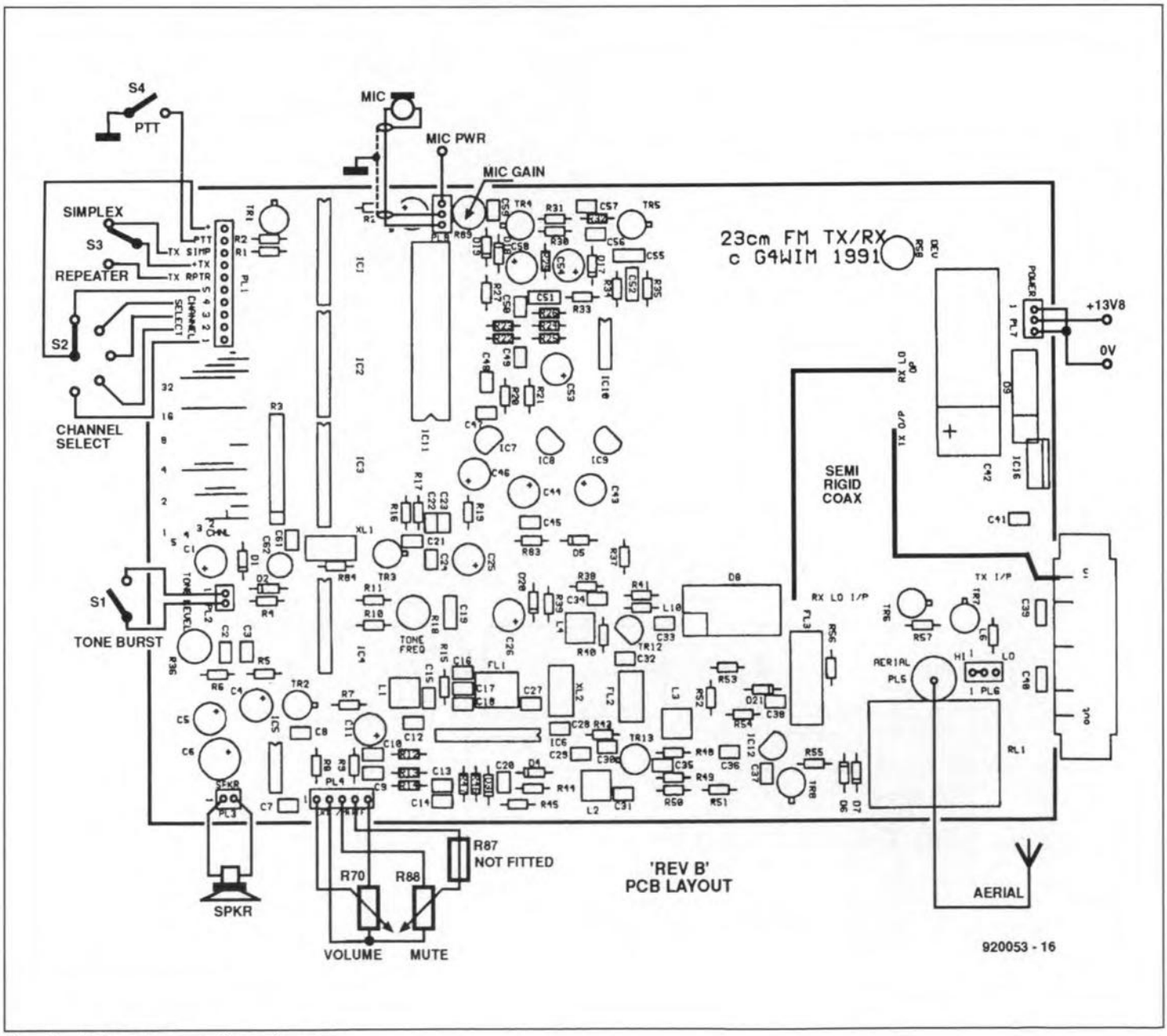


Fig. 6. External connections diagram.

COMPONENTS LIST

* means surface mounted part.
! means Cirkit part number.

Resistors:
5% 0.25-W NK3 Type unless otherwise stated.
* = Chip resistor; 5% RC01 type.

R1;R2;R35;R37= 4kΩ7
R3 = 47kΩ SIL
R4 = 100kΩ
R5;R6;R14;R20;R27;R29;R40;
R48;R83 = 2kΩ2
R7 = 1kΩ5
R8;R13;R16 = 22kΩ
R9 = 27kΩ
R10;R12;R45;R59;R61 = 10kΩ
R11;R30;R47 = 330kΩ
R15 = 33kΩ
R17;R28;R33;R62 = 1kΩ
R18 = 2kΩ preset
R19;R21;R43 = 100Ω
R22;R23;R24;R25 = 18kΩ
R26;R34;R84 = 15kΩ
R31 = 12kΩ
R32 = 82kΩ
R36;R89 = 5kΩ preset
R38 = 22Ω
R39;R54 = 120Ω
R41;R51 = 56Ω
R42;R72;R85;R86 = 2kΩ2 chip *
R44 = 680Ω
R46 = 470Ω
R49;R50 = 56kΩ
R52 = 27Ω
R53 = 270Ω
R55;R57 = 4kΩ7
R56 = 68Ω
R58 = 10kΩ preset
R60 = 180Ω
R63 = 39kΩ chip *
R64 = 4kΩ7 chip *
R65;R68;R77 = 10kΩ chip *
R66 = not fitted
R67;R75;R78;R79;R80 = 82Ω chip *
R69;R73 = 1kΩ chip *
R70 = 10kΩ log. pot
R71 = 330Ω chip *
R74;R76 = 470Ω chip *
R81;R82 = 22Ω chip *
R88 = 10kΩ lin. pot

Capacitors:
pF chip * capacitors are 0805 size,
nF chip * capacitors are 1206 size.
All capacitors are subminiature, 0.1" radial fitting types unless otherwise noted.

C1;C11 = 4.7µF 16 V
C2;C3;C49;C50 = 22nF
C4;C5;C25;C26;C43;C44;C46;C53;C54;C58;
C60;C65;C84;C101 = 47µF 16 V
C6 = 100µF 16 V
C7;C9;C10;C16;C17;C18;C20;C36;C37;C41;
C47;C48;C59 = 100nF
C8;C13;C14;C38;C45 = 1nF
C12 = 150pF
C15 = 22pF
C19 = 22nF 0.2"
C21 = 330pF
C22 = 680pF
C23 = 68pF
C24;C29-C35 = 4.7nF
C27 = 10pF
C28;C61 = 12pF
C39;C40;C102 = 100nF chip *
C42 = 1000µF 16 V axial
C51;C52 = 470nF 0.2"
C55 = 100nF 0.2"
C56 = 470pF
C57 = 4.7nF
C62 = 25pF trimmer
C63 = 470pF chip *
C64;C66;C67;C70;C71;C72;C74-
C77;C83;C85-C90;C92-C97 = 47pF chip *
C68 = 1nF chip *
C69 = 100pF chip *
C73 = 10pF chip *
C78;C91 = 2pF trimmer
C79;C81 = 1pF chip *
C80 = 2.2pF chip *
C82 = 0.6pF chip *
C98,C99;C100 = 33pF chip *

Note: C93 and C94 are fitted through the PCB after the holes have been drilled out by a 1.5-mm drill. Necessary to remove the through hole plating.

Semiconductors:
TR1;TR2;TR7 = BC477
TR3;TR5;TR8 = BC109
TR4;TR6 = BC107
TR9 = ATF13484 *
TR10 = BCW33 *
TR11 = BFR92 *
TR12 = J310
TR13 = 3N201
IC1;IC2;IC3 = CD4008
IC4 = CD4011
IC5 = ULN3718M
IC6 = MC3359
IC7;IC9;IC12 = 78L08
IC8 = 78L05
IC10 = TL081
IC11 = MC145152P2
IC13 = MB501L
IC14;IC15 = MSA0304 *
IC16 = 7808
IC17 = MSA0635 *
PA1 = M67715 (Mitsubishi)
D1-D4;D6;D7;D17;D18;D19 = 1N4148
D5 = 4.7V zener
D8 = SBL1-X
D9 = 1N5408
D10 = BAS19 *
D11-D14 = BA585 PIN *
D15;D16 = BB811 *
D20 = 5.6V zener
D21 = 3.9V zener
Programming diodes 1N4148 types as required.

Inductors:
L1 = 35-01842 !
L2;L3;L4 = 35-00291 !
L5 = see below
L6 = 0.22µH SC30
L7;L8 = 0.1µH *
L9 = see below
L10 = 0.47µH SC30

L5 and L9 are pieces of 22 SWG tinned copper wire soldered 1.5-mm above the PCB on the track side between the relevant pads.

Miscellaneous:
XL1 = quartz crystal 3.2 MHz
XL2 = quartz crystal 44.545 MHz
FL1 = filter 455D2
FL2 = filter 45M15A
FL3 = filter 17-12109 !
PL1 = 10-way Molex
PL2;PL3 = 2-way Molex
PL4 = 5-way Molex
PL5 = SMA coax socket
PL6;PL7;PL8 = 3-way Molex
RL1 = 175-051 (Farnell)
S1 = single pole momentary action
S2 = single pole 5 way
S3 = single pole change over
S4 = PTT (usually part of microphone assembly)
Semi-rigid coax for for RX LO and TX drive connections.

Note: S2 could be 2-pole 6-way, the second pole being used as the power switch, as per prototype.
Sockets as required for external microphone, speaker and power connectors.

Hardware:
4 off Tapped 8mm high pillars.
1 off RF power amplifier mounting block 50×15×6mm aluminium.
1 off Diecast box 220×150×55mm minimum size.
VCO cover 70×53×6mm (internal dimensions) made from 0.5-mm brass or similar.

Cirkit PLC are at Park Lane, Broxbourne, Herts EN10 7NQ, England. Telephone: (0992) 444111. Fax: (0992) 441306.

For PCBs and component sets, contact the author:
Mr. T. Forrester, 12 Lime Close, Hartwell, Northants NN7 2PS, England.

Latest issue PCBs are 'Rev. C'. On these, R62, R60, R61 and R59 become surface-mount assembly (SMA) parts. This PCB also has provision for a PIN diode antenna changeover, and DC FM for 9,600 baud Packet Radio.

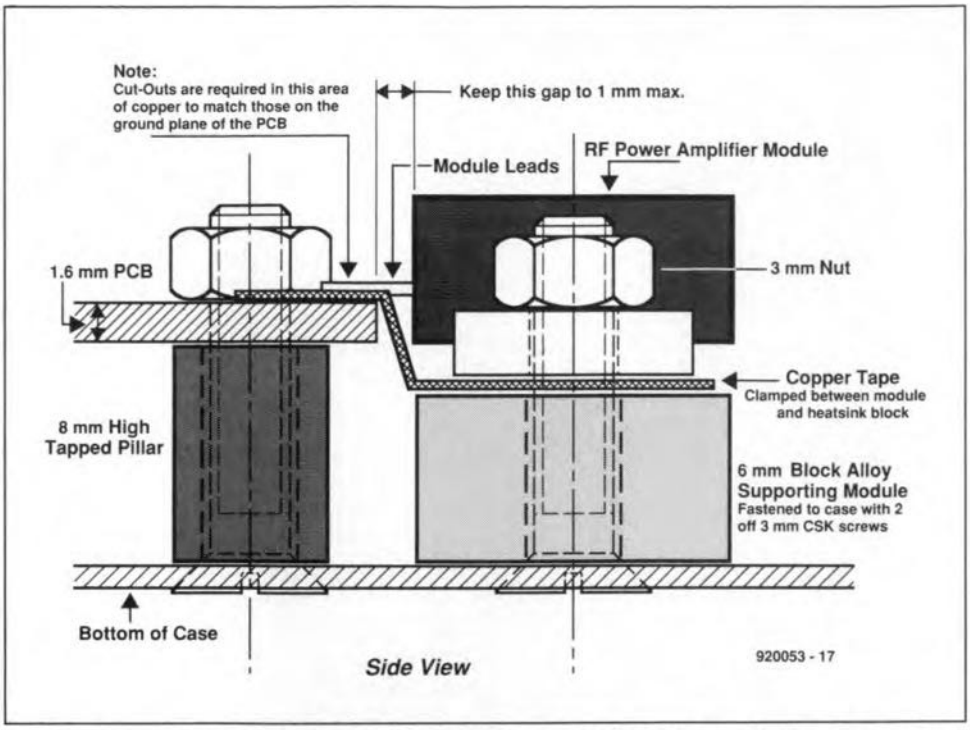


Fig. 7. Suggested mounting of RF power amplifier module. Do not use heat-sink compound on module or copper tape.

pin 6 of IC10 will have increased by about 1 V. This is normal. Turn off the power and tack solder the cover in place every 10 mm or so for the time being.

Turn on the power and set the reference oscillator to 3.2 MHz using C62.

Lift the receiver mute and align the receiver by tuning to a strong local signal. Peak C91 and FL3, followed by L4, L3 and L2. Tune L1 for best recovered audio. Check that the mute action is smooth and positive.

If a signal generator is available, the mute should lift at less than 0.15 µV and have a SINAD of 12 dB or better.

If necessary, adjust the reference oscillator using C62 to ensure that the receive signal is correctly tuned.

If everything is operating all right so far, solder the VCO cover firmly in place, to further reduce any residual microphonic effects.

Referring to Fig. 7, install the PCB in its case on 8-mm pillars. Next, solder the RF power amplifier to the PCB ensuring that copper tape is used to bond the base of the module to the ground plane of the PCB (see drawing in Fig. 7). Make sure that the power module and IC16 are well 'heatsinked' to the case. Insert a link on PL6 to select either high or low power. Connect an RF power meter to PL5, and select transmit. The current should be circa 1.1 A for 2 W output on high power, and about 800 mA for 1 W output on low power.

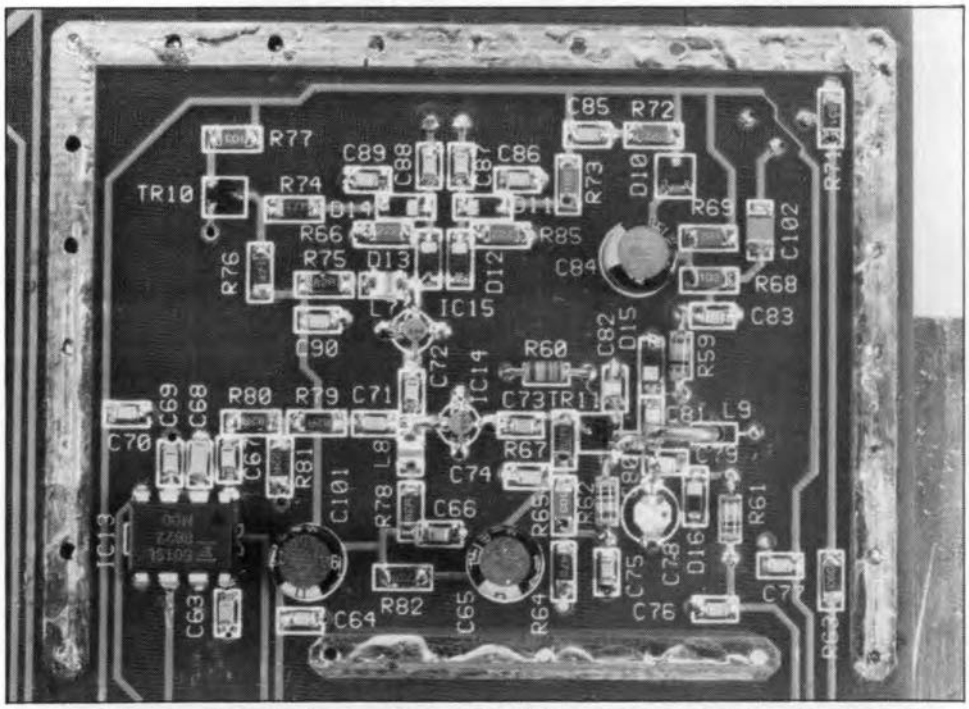


Fig. 8. Close-up of the VCO area of the PCB. This part of the circuit is normally enclosed by a metal cover.

Set the microphone gain (R89) midway. Next, using a deviation meter or off-air signal report, adjust R58 for a peak deviation of about 5-kHz.

Set R36 initially midway, then press the tone button and adjust R18 for 1750 Hz. Readjust R36 for approximately 3-kHz peak tone deviation.

If all is well the radio is now ready for use and should give very good mobile performance when used with a suitable aerial, typically an Alford slot as most repeaters and base stations use horizontal polarisation.

Conclusion

The prototype has been in use by the author for some time now and has proved to be adequate for both base station use and mobile operation. Obviously, owing to the unit's relatively low power and higher propagation losses at 1.3 GHz when compared to, say, 432 MHz, the range attainable is less than that available on lower frequencies. However, as a general guide it seems that when a 23-cm repeater is co-sited with a 70-cm repeater (for instance, GB3NH and GB3CN), the 23-cm repeater is accessible by a mobile from locations where the 70-cm repeater is accessible on a handheld. This assumes that the 23-cm mobile is using a half sized Alford slot aerial providing circa 5-dBi of aerial gain.

Another interesting aspect of 23-cm mobile working is the reduction in mobile 'flutter' when moving even at fairly slow speeds, compared to 'flutter' observed on the lower frequencies.

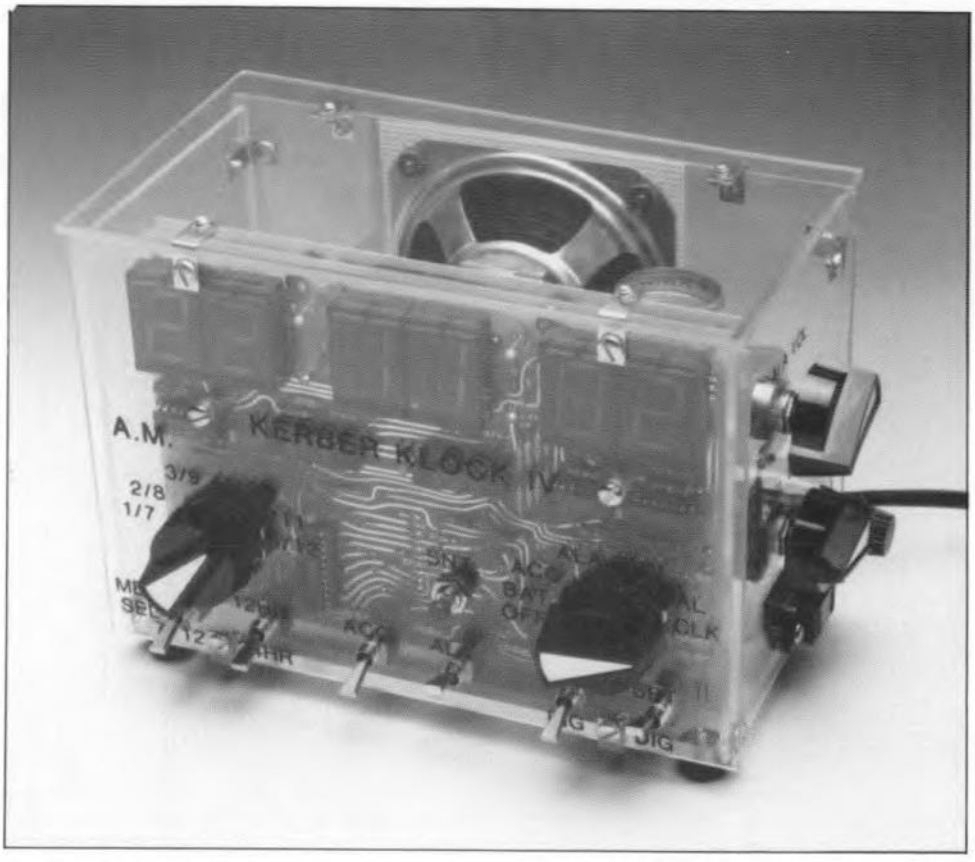
Generally, 23-cm repeaters are always in beacon mode when not actually in use as a repeater. This means that the receiver mute would be permanently lifted when monitoring a repeater/beacon leading to unnecessary idents and noise being received. To overcome this drawback, some repeaters are fitted with a sub-audible tone which is only superimposed on the repeater transmit carrier when the repeater is accessed, and the mute is lifted on its receiver. Typically, the tone would be between 60 Hz and 250 Hz at a deviation of less than 1 kHz. A receiver monitoring the repeater which has a tone mute set to the same frequency (123 Hz for GB3CN) would now only respond to voice traffic passing through the repeater, so ignoring unwanted AFSK idents. If there is enough interest, a compatible tone mute circuit may be developed for this design.

The author can supply high quality PCB's (plated through, solder resist, and silk screened), plus parts or kits of parts as required. (Exact prices yet to be determined and dependent upon demand).

If required it is proposed to supply the VCO and synthesizer sections assembled and tested, leaving only receiver and ancillary parts to the constructor. This approach may be more attractive to those amateurs who feel that surface mount techniques are perhaps beyond them! ■

KERBER KLOCK IV

Musical grandfather clocks are still very popular in many households. This article describes how electronics have been applied to build a microprocessor-based digital clock with twelve different melodies which are selected by the user.



By R. J. 'Bob' Kerber

THE construction of the enclosure can be at the discretion of the user. For those interested in woodworking projects, the electronics could be housed in a mantle clock or carriage clock made of solid walnut, cherry, or whatever. Other materials could be metal, plywood, paneling, or anything else that comes to mind. This article describes the author's enclosure, which uses clear plastic. A clear enclosure is not only an interesting conversation piece but is a unique method of displaying one's handiwork. The enclosure is 7.5 inch wide, 5.5 inch high and 4 inch deep (approx. 191 × 140 × 102 mm).

The Kerber clock plays a melody on the quarter hour, similar to a grandfather clock. There are 12 preprogrammed melodies, which are user selected by a rotary switch on the front panel. At 15 minutes past the hour, a quarter of the melody will be played. At half past the hour, half the melody will be played, and so on, until the entire melody is played on the full hour. Almost any melody can be preprogrammed into the clock at the request of the user — contact the Kerber Klock Ko. for details.

Circuit description

At the heart of the circuit (Fig. 1) is a Motorola 6802 microprocessor. The 6802 has its own internal clock and driver, requiring only an external crystal. It also has 128 bytes of on-chip RAM, which is nice as long as no more RAM is needed because it does not require external RAM with additional address decoding circuitry.

A 51-kΩ resistor and a 4.7-µF capacitor provide a power-on RESET to pin 40 of the CPU. A 4-MHz crystal oscillator is used to provide an external clock frequency to run the processor. The 60 Hz (or 50 Hz) mains frequency is shaped by a 74HC14 inverting Schmitt trigger gate. This frequency is used to run the clock when there is mains power. A 1.2-kΩ resistor monitors the transformer secondary voltage for a power failure. If the mains power fails, the clock switches to another 60 Hz (or 50 Hz) source: the 6840, whose timing signal is gated through to the NMI\ (non-maskable interrupt) pin of the 6802. The NMI\ is used for timing the digital clock and the length of the tones in the melodies.

The IRQ\ (interrupt request) line of the CPU is used for multiplexing the 7-segment LED displays. A 74HC14 gate functions as an oscillator operating at about 2.8 kHz.

A 2532, 2732 or 2764 EPROM stores the machine language program that tells the processor what to do. If a 2532 is used, a jumper wire is required from E1 to E2, and one from E3 to E4. If a 2732 or 2764 is used, a jumper wire is required from E2 to E3, and one from E4 to E5. The jumpers are required owing to these devices having different pins for the same signals. When a 2764 is used, a 28-pin socket is required. The 2532 and 2732 devices can use either a 24 or 28-pin socket. When a 28-pin socket is used, the 24-pin device is inserted in the bottom set of holes (the top is pin 1), as shown on the component location diagram.

Address decoding starts with the 74LS138. Valid memory address (VMA) and the E clock are 'ANDed' through a 74LS00 gate at pin 3 to provide a logic low signal VMA*E\. Address line A15 and VMA*E\ enables the 74LS138 to recognize A14, A13 and A12, which causes the appropriate output to go low when true. For example, when signals A15, A14, A13 and A12 are all high, pin 7 (F000) goes low, enabling the EPROM.

Address E000 from address decoder pin 9 is not used. The letters 'N.C.' in the circuit diagram indicate 'no connection'.

Address D000 from pin 10 enables the 6840 PTM (programmable timer module). The PTM is designed to provide variable time intervals. It has three 16-bit binary counters, three corresponding control registers, and a status register. These counters are under software control, and are used to generate frequencies for the melodies, the alarm, and a 60-Hz frequency used to keep the clock going when on battery backup.

Address C000 (pin 11) is not used.

Address B000 from 74LS138 (pin 12) is used to interrogate the switches inputting to the 74LS244-2, while address A000 from pin 13 interrogates the switches inputting to the 74LS244-1. Switch interrogation occurs 60 times a second (i.e., every 16.67 ms). The 5.6-kΩ resistors pull the inputs of both 74LS244s logic high unless a particular switch pulls that input low. When the processor addresses a switch decoder, it reads the information supplied by the decoder via data lines D7 through D0. The bit combination read back determines what happens. For instance, if switch S_a is in the CAL position, data line D1 instructs the processor to display the date.

Address 9000 from 74LS138 pin 14 is used to determine which of the six display digits, the AM LED or the ACO solid-state relay (SSR) is to be selected. When pin 14 goes low, it causes the data on the data bus (D7 through D0) to be latched into the 74LS374-2 octal D-type flip-flop, and to appear at its output. The ULN2001 is a high-voltage, high-current, Darlington transistor array. An alternative part, the ULN2003,

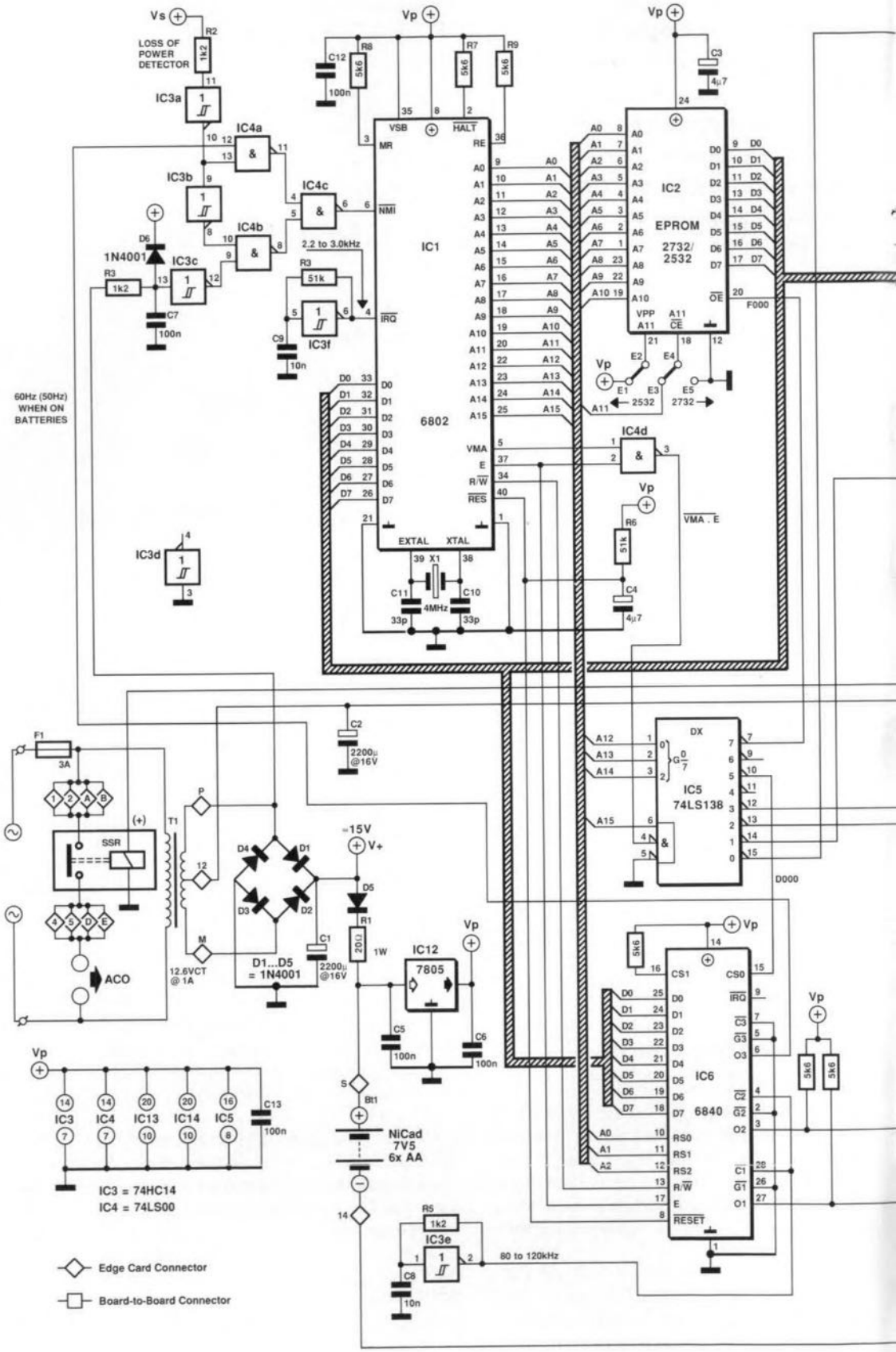
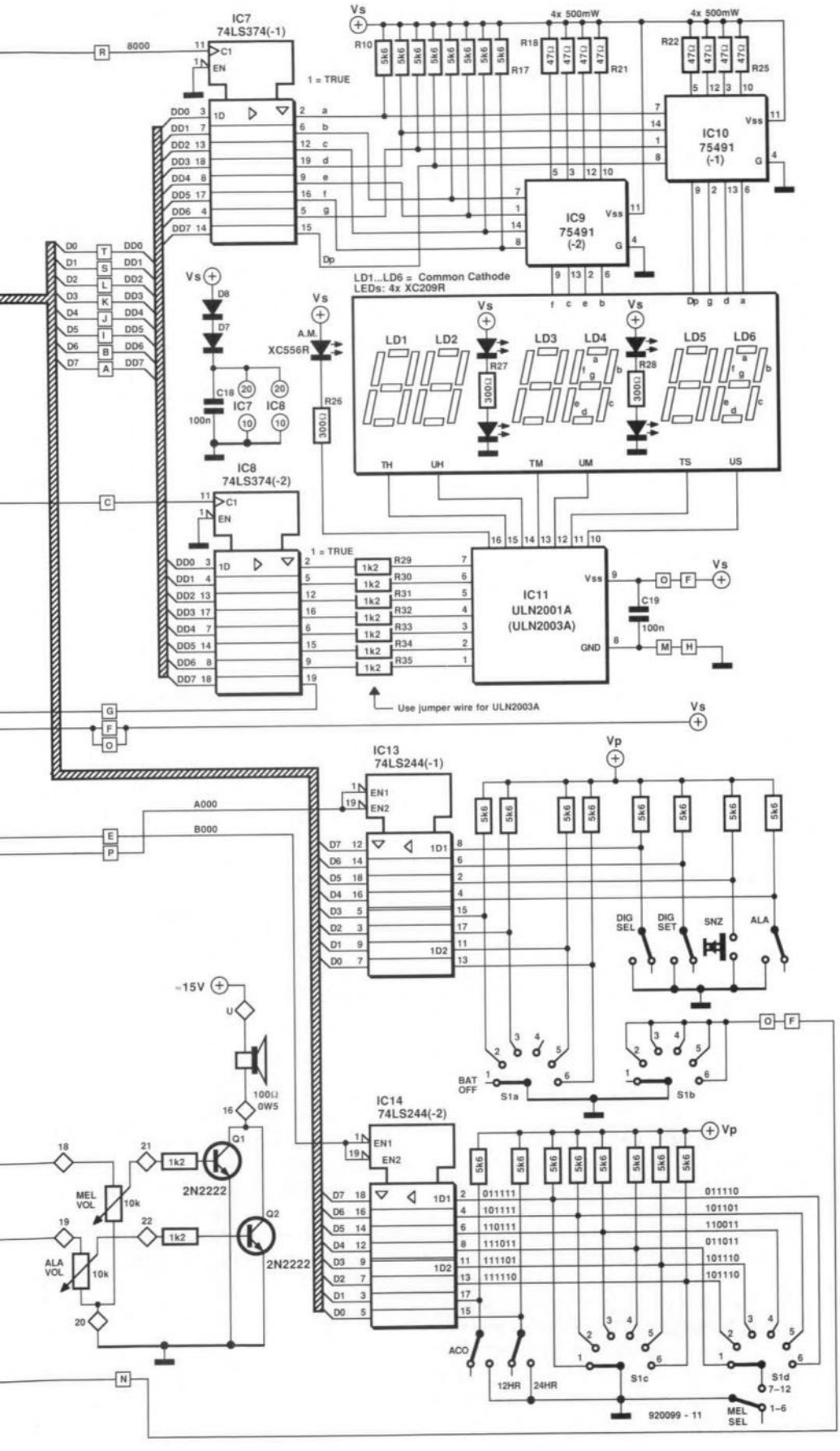


Fig. 1. Circuit diagram of the Kerber Klock.


IC7
74LS374(-1)
IC8
74LS374(-2)
IC9
75491
(-2)
IC10
75491
(-1)
IC11
ULN2001A
(ULN2003A)
IC13
74LS244(-1)
IC14
74LS244(-2)
Vs
Vp
4x 500mW
1 = TRUE
LD1...LD6 = Common Cathode
LEDs: 4x XC209R
A.M.
XC556R
Use jumper wire for ULN2003A
-15V
100Ω 0W5
2N2222
MEL VOL
ALA VOL
DIG SEL
DIG SET
SNZ
ALA
BAT OFF
ACO
12HR
24HR
MEL SEL
920099 - 11

may be used, provided the seven 1.2-kΩ input resistors are replaced with #22 AWG solid wire.

Address 8000 from 74LS138 pin 15 determines which display segments including the decimal point (DP) are to be tuned on. A low level on pin 15 causes data to be latched into the 74LS374-1, and to appear at the outputs. The 75491-1 and 75491-2 are quad LED segment drivers. The eight ½-watt resistors limit the current through the LED segments, thus determining the brightness level. Too large a resistor will make the displays dim, while too small a resistor could burn them out.

Power supply

The rectifier circuit is a full-wave bridge type using four 1N4001 diodes to rectify the 12.6-V a.c. secondary voltage of the mains transformer. A 2200-µF capacitor, C1, is used to smooth the rectified voltage, which is about 15 V d.c. The rectified voltage is fed to the 5-V regulator, the loudspeaker driver, and the NiCd rechargeable batteries. The centre tap of the transformer provides a secondary voltage, which is filtered by a another 2200-µF capacitor, C2.

A 20-Ω, 3-watt resistor is inserted in the 7805 input voltage line to take some of the heat away from the regulator, and provide current limiting to trickle-charge the NiCd batteries. Diode 1N4001 (CR5) prevents battery current from flowing back through the 20-Ω resistor on power failure. The V_p voltage is backed up by NiCd batteries. On battery back-up, the displays will go dark, but the internal circuitry will keep track of the correct time, so that when AC power returns, the correct time will be displayed. The V_s voltage is not required upon loss of power.

Features and functions

The Kerber Klock has two display modes: 12-hour (12:00:00) or 24-hour (00:00:00). Either option is selected by the switch marked 12 HR/24 HR. When in the 12-hour mode, an LED below the tens-of-hours digit will turn on, indicating the time is AM. Switching between 12 HR and 24 HR position changes the display instantly.

The calendar is displayed for two seconds every ten seconds. The date is displayed in the form MM:DD:YY, where MM is the month, DD is the day and YY is the year. The correct number of days is displayed for any particular month. Leap year is calculated by dividing the year by four. If it divides evenly, 29 days are displayed for February, if not, 28 days are displayed.

To disable displaying the date, turn the right-hand rotary switch to the CAL position, and push the SNZ (snooze) button. When the rotary switch is turned back to RUN position, the date will not be displayed. To return to displaying the date, repeat the procedure. A reboot of the system will also cause the date to be displayed.

The alarm is a true 24-hour alarm. When the clock time equals the preset alarm time, and the ALA switch is up, the alarm will sound. The alarm will sound for one minute unless it is terminated by putting the ALA switch down, or by pushing the SNZ button (which will turn the alarm off for 10 minutes). The SNZ button may be pushed as many times as desired, until the alarm is disabled by the ALA switch. The alarm volume can be set by pushing the SNZ button with the ALA switch up.

The AC outlet (ACO) on the right side of the case is an accessories outlet which can control small appliances rated up to 3 A (300 W) maximum. It can be used to turn off a radio and/or a light automatically after you go to sleep, and turn them on in the morning when the alarm comes on. There is a 99-hour and 59-minute counter which can be set in one-minute increments. The ACO is a down counter, and will stay on for the preset time period as long as the ACO switch is up. The ACO will turn on at the alarm time if the ACO and ALA switches are up. Putting the ALA switch down will turn off the alarm but not the ACO.

The melodies are selected by combining the left-hand rotary switch, Sc, with the MEL SEL toggle switch. With MEL SEL in the up position (1-6), melodies one through six are selected by Sc. With MEL SEL in the down position (7-12), melodies seven through twelve are selected by Sc. Any melody can be played on demand by pushing the SNZ button with the ALA switch down. The standard version of the Kerber Klock IV is preprogrammed to play the following melodies:

1. Westminster Chimes
2. London Bridge
3. Somewhere My Love
4. The Way We Were
5. Love Me Tender
6. Strangers In The Night
7. More
8. The High And The Mighty
9. Misty
10. Jingle Bells
11. Oh! Susanna
12. Everybody Loves Somebody

Setting the time (CLK)

Rotate the right-hand rotary switch (Sa) to the CLK position. This will freeze the clock time on the display (HH:MM:SS). Put the SEL DIG (select digit) toggle switch in the up position. A lit decimal point indicates the digit that is ready to be changed. Put the SET DIG (set digit) toggle switch in the up position. The digit with its decimal point lit will start to increment at a 2-Hz rate. Seconds will be reset to 00. Put the SET DIG switch down when the desired number is displayed. Put the SEL DIG switch down and back up to move to the next digit. Set the desired number using SET DIG as done before. Do this for the other digits.

Setting the calendar (CAL)

Rotate switch Sa to the CAL position. This will freeze the date on the display (MM:DD:YY). Put SEL DIG in the up position. A lit decimal point indicates the digit that is ready to be changed. Put the SET DIG (set digit) toggle switch in the up position. The digit with its decimal point lit will start to increase at a 2-Hz rate. Put the SET DIG switch down when the desired number is displayed. Put the SEL DIG switch down and back up to move to the next digit. Set the desired number using SET DIG as done before. Do this for the other digits, and rotate Sa to RUN position. Note that the time of day was not affected while setting the date.

Setting the alarm (ALA)

Rotate Sa to the ALA position. The procedure for setting the alarm time is the same as that for setting the time of day. If in the 12-hour mode, be sure the AM LED is on for AM alarm setting. Rotate Sa to RUN position after the alarm time is set correctly.

To set the alarm, put the ALA switch in the up position. Note that the decimal point of the digit above the ALA switch will come on. This allows the user to tell, in the dark, that the alarm has been set. Set the ALA VOL as desired while pushing the SNZ button. When the time of day is the same as the alarm setting, the alarm tone will sound for one minute unless the ALA switch is put down, or the SNZ button is pushed. The SNZ button turns the alarm tone off for 10 minutes.

Setting the AC outlet (ACO)

Rotate Sa to ACO position. The procedure for setting the counter is the same as that for setting the time of day, except the hours can be set to 99. Putting the ACO switch up will turn on the SSR, which puts mains voltage on the AC outlet on the right side panel of the clock, and start the counter counting downward. When the ACO counter reaches 00:00:00, the AC outlet will turn off. The decimal point above the ACO switch will be lit.

Construction

The construction of the clock is set out in great detail in the manual supplied by the Kerber Klock Ko. The manual also contains the component mounting plans of the two printed circuit boards, a detailed parts list, and a components source list. Prices of a number of items used to build the clock, as well as parts kits, EPROM listings, preprogrammed EPROMs, etc., are indicated on the order form which you can obtain from

Kerber Klock Kompany
R. J. 'Bob' Kerber
36117 Hillcrest Drive
Eastlake, OH 44095
U.S.A.
Telephone (216) 946-3898

Finally, make sure to state 50 Hz mains or 60 Hz mains when ordering or asking for details. ■

ANALOGUE OPAMP INTEGRATOR CIRCUITS

HOW THEY WORK, HOW TO DESIGN THEM AND WHAT MISTAKES ARE MADE

By Joseph J. Carr

INTEGRATION is the mathematical process of finding the area under a curve. While the mathematics of integration are beyond the scope of this article, the underlying concept is not. If you want to find the area under a time varying voltage, then you might apply the mathematics of integral calculus to arrive at a number.

Alternatively, you might use an analogue integrator circuit. The same circuit can also be used to find the time average of a varying voltage.

In Fig. 1 a time-varying voltage signal represents a pressure transducer output. In this particular case, the signal is the output of a human arterial blood pressure transducer used in medical electronics (any other example would also suffice). Notice that the pressure/voltage varies with time from a low non-zero value ('diastolic') to a high peak value ('systolic') between times T1 and T2 (which represents one cardiac cycle). If we want to know the mean arterial pressure (MAP), we would want to find the area under the curve, as shown by the formula in Fig. 1.

Before discussing the circuit, let us first mention the math notation. The $\int$ symbol indicates that the integration process will be applied on the pressure signal, P, over the time interval T1 to T2. The 'd t' indicates that the integration takes place with respect to time. The mean arterial pressure over the T2-T1 interval, also denoted by P-bar, is the integral of the voltage signal representing the pressure. From this illustration we can see that the integrator serves to find the time-average 'mean' value of an analogue voltage waveform — it does not have to be a blood pressure signal.

Passive *R-C* integrator circuits

Perhaps the simplest form of integrator and differentiator circuits are made from simple resistor (R) and capacitor (C) elements, as shown in Fig. 2. You may recognize this circuit as a passive low-pass filter. The *R-C* low-pass filter (integrator) has a −6 dB/octave falling characteristic frequency response.

The operation of the integrator is dependent upon the time constant of the *R-C* network (i.e. $R \times C$). In most cases, we want the integrator time constant to be long (i.e., >10×) compared with the period of the signal being integrated. We can cascade several integrators in order to enhance the effect, and also increase the slope of the frequency response fall-off, although only at the expense of severe signal amplitude loss.

Active op-amp integrator circuits

The operational amplifier makes it a lot easier to build active integrator circuits. Fig. 3 shows the standard operational am-

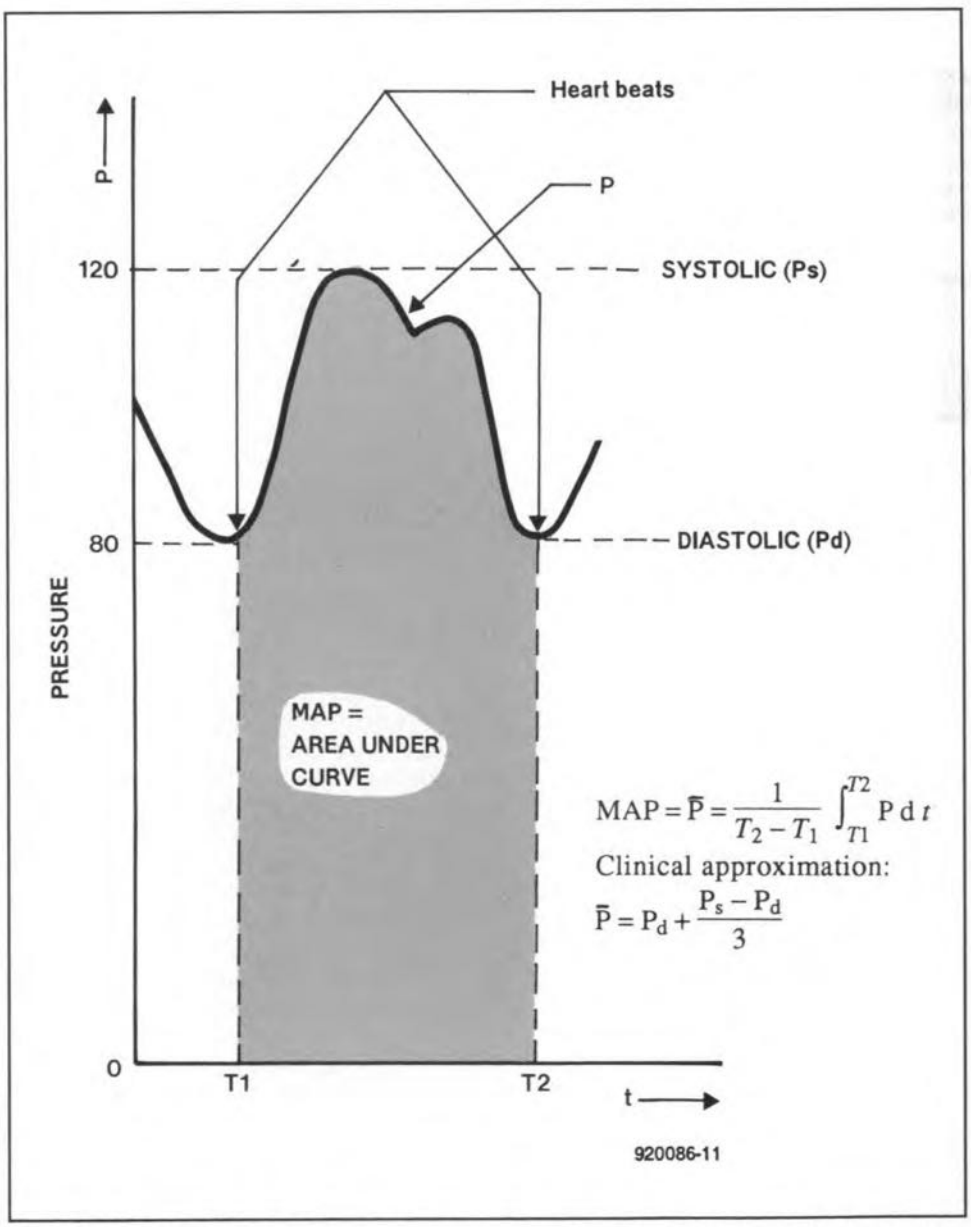


Fig. 1. Blood pressure *vs.* time curve. P is a time varying voltage from a pressure transducer.

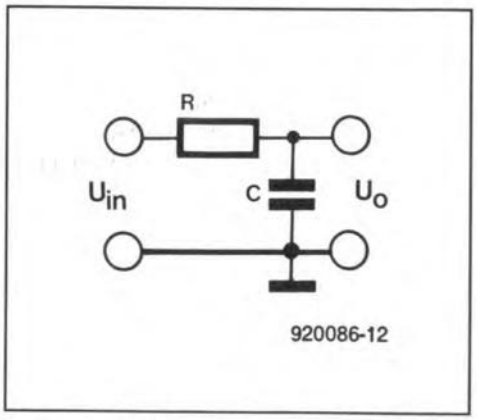


Fig. 2. Passive resistor-capacitor (*R-C*) integrator circuit.

plifier version of the Miller integrator circuit. An IC operational amplifier is the active element; a resistor is in series with the inverting input and a capacitor is in the feedback loop. The output voltage of the integrator circuit is dependent upon the input signal amplitude and the *R-C* time constant. The transfer equation for the Miller integrator is:

$$U_o = \frac{-1}{RC}\int_0^t U_{in}\,dt + K \qquad (1)$$

Where:
U_o and U_{in} are in the same units (volts, millivolts, etc.);
R is in ohms (Ω);
C is in farads (F);
t is in seconds (s);
K is a constant in volts (same units as U_o and U_{in}).

The expression of Eq. [1] is a way of saying that the output voltage is equal to the time-average of the input signal, plus some constant K which is the voltage that may have been stored in the capacitor from some previous operation (often zero). Alternatively, K may represent an offset error voltage in either the input signal or the operational amplifier itself — and therein is found a problem with textbook integrator circuits.

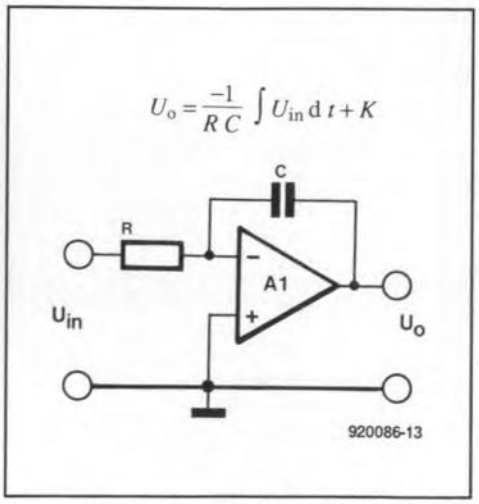


Fig. 3. Miller opamp integrator circuit.

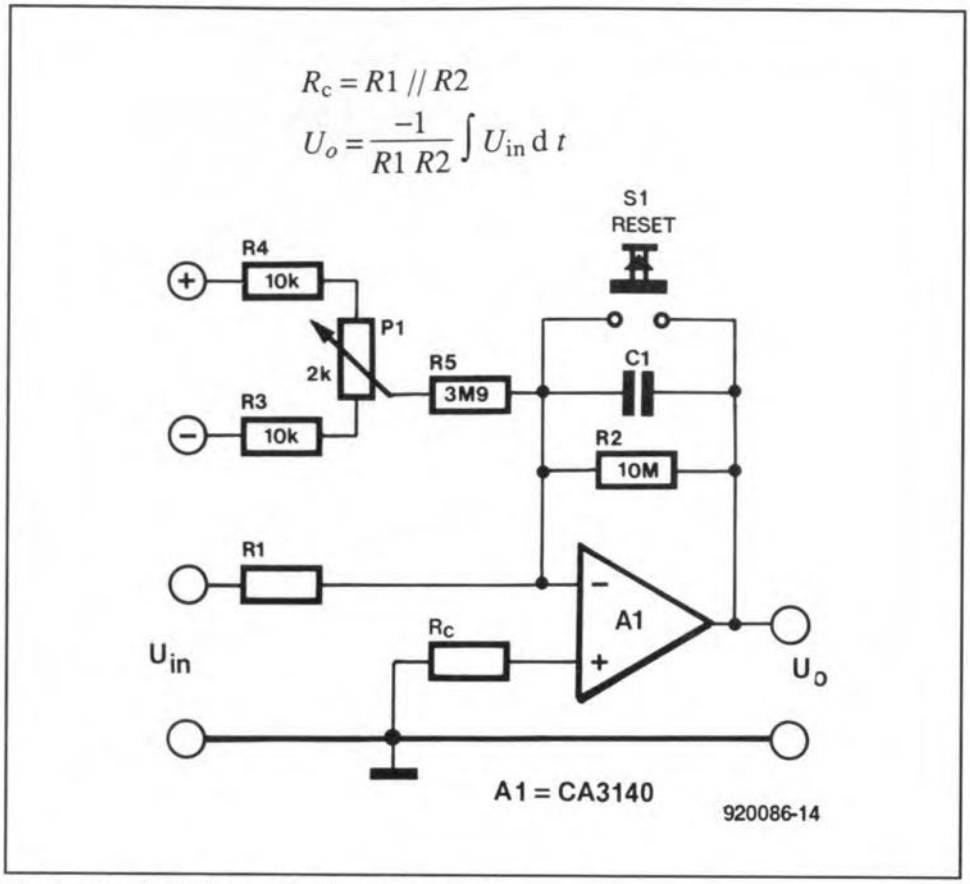


Fig. 4. Practical Miller opamp integrator circuit.

Practical Miller integrator circuits

The circuit shown in Fig. 3 is classic, and appears in textbooks and magazine articles. Unfortunately, it also does not work very well (or at all in some cases) because of the offset voltage problem (a demon *K*!). These circuits are too simplistic because they depend upon ideal input signals that are symmetrical about zero volts, and the properties of 'ideal' operational amplifiers. Unfortunately, the real kind-you-can-go-buy opamps fall far short of the ideal device that was in the mind of the textbook writer. In real circuits we find that integrators saturate very shortly after turn-on.

The problem with the opamp integrators was driven home to me when I worked in a medical school/hospital bioelectronics lab, and had to build an electronic integrator for one of the customers of our electronics laboratory. When I used a Type 741 operational amplifier, the output voltage saturated within milliseconds after turn-on. In fact, saturation came so fast that I initially thought the opamps were bad. The problem was that the input bias currents of the opamp (which are zero in ideal devices) create a high enough output voltage to fully charge the capacitor in the feedback loop very rapidly.

There is another problem with this kind of circuit, and it magnifies the problem of saturation. This circuit has a very high gain with certain values of R and C. Let us pick an example and see what this gain can mean. The voltage gain (A_v) of this circuit is given by the term $-1/RC$ (1) so what is the gain with a 0.01-µF capacitor (certainly not a 'large' capacitor in conventional wisdom) and a 10,000-ohm resistor (note: 0.01-µF is 10^{-8} farads)? The gain is calculated as follows:

$A_v = -1/RC$
$A_v = -1/(10^4 \text{ ohms})(10^{-8} \text{ farads})$
$A_v = -1/10^{-4}$
$A_v = -10^4 = -10{,}000$

With a gain of −10,000, a +1-volt DC signal applied to the input will try to produce a −10,000 volt output. Unfortunately, the operational amplifier's negative output potential is limited to a range of −5 to −20 volts, depending upon the device selected and the applied V– power supply voltage. For this case, the operational amplifier will slew to saturation very rapidly! If we want to keep the output voltage from saturating, then we must either keep the *R-C* time constant under control, or prevent the input signal from rising too high (not good!). If the maximum output voltage allowable is 10 V, then the maximum input signal is 10 V/10,000, or 1 mV. Obviously, the best solution is to keep the *R-C* time constant within bounds.

When I built my first analogue integrator, and found that 741 devices were not suitable, I turned to high-cost premium grade opamp devices. At that time, a premium 725 device cost $15, and it suffered the same problems as the 741. The only difference between the $15 premium

opamp and the $0.50 741 device is that on the $15 opamp the output saturated slowly enough for me to watch it on an oscilloscope or voltmeter — about four seconds — instead of nearly instantaneously. Unfortunately, this was still not acceptable.

Applying a waveform to the input of even the premium op-amp integrator allowed me to see the output waveform rise up the screen of the oscilloscope and disappear off the top of the screen!

How to solve the problem

Fortunately, there are some practical design tactics that will allow us to keep the integration capability, while getting rid of the problems. A practical integrator is shown in Fig. 4. The heart of this circuit is a BiMOS operational amplifier, Type CA3140, or its equivalent BiFET type (the CA3130 or CA3160 will also work; Type CA3240 is a dual CA3140 with the same pin-outs as an LM1458). The reason that this device works so well is that it has a low input bias current (having a MOSFET input circuit with a 1.5×10^{12}-Ω input impedance). When I tested close to a dozen different opamps for the circuit the CA3140, which cost only about two dollars, they out-performed devices costing ten times as much.

Capacitor C1 and resistor R1 in Fig. 4 form the integration elements, and are used in the transfer equation. Resistor R2 is used both to discharge C1 to prevent DC offsets from either the input signal or the opamp itself from saturating the device; its value should be 10 to 20 MΩ. Resistor R2 also limits the gain at low frequencies. The 'RESET' switch is used to set the capacitor voltage back to zero (to prevent a '*K*' factor offset) before the circuit is used. In some measurement applications, the circuit initializes by closing S1 (or a relay equivalent) momentarily.

Because of R2 in the circuit we must place a constraint on the transfer equation: the equation is valid only for frequencies greater than or equal to *F* in Eq. [1]:

$$F = \frac{10^6}{2\pi R_2 C} \qquad (2)$$

Where:
F is the cut-off frequency in hertz (Hz);
R2 is in ohms (Ω);
C is in microfarads (μF).

There is a compensation resistor, Rc, between the non-inverting input of the operational amplifier and ground. This resistor cancels the effects of input bias current and improves thermal drift performance (2). It has a value equal to the parallel combination of R1 and R2:

$$R_c = \frac{R_1 R_2}{R_1 + R_2} \qquad (3)$$

There may still be a minor drift problem, so potentiometer P1 is sometimes added to the circuit to cancel it. This component adds a small countercurrent to the inverting input through resistor R5. To adjust this circuit, set P1 initially to mid-range. The potentiometer is adjusted by shorting the V_{in} input to ground (or setting V_{in} = 0), and then measuring the output voltage. Press S1 to discharge C1, and note the output voltage should go to zero and stay there. If it does not, then turn P1 in the direction that counters the change of V_o after each time S1 is pressed. Keep pressing S1 and then making small changes in P1 until you find that the output voltage stays very nearly zero, and remains constant, after S1 is pressed (there will be some long-term drift normally).
If drift becomes important, and the output voltage range can be limited to less than ±5 V, it is possible to make the CA3140 operate in a low-noise mode. Remember to use the 8-pin metal can package type, rather than the more common 8-pin miniDIP, and place a expandable heatsink (the kind made for TO-5 metal transistor packages) on it. Limit the DC power supplies to ±5 V.

Conclusion

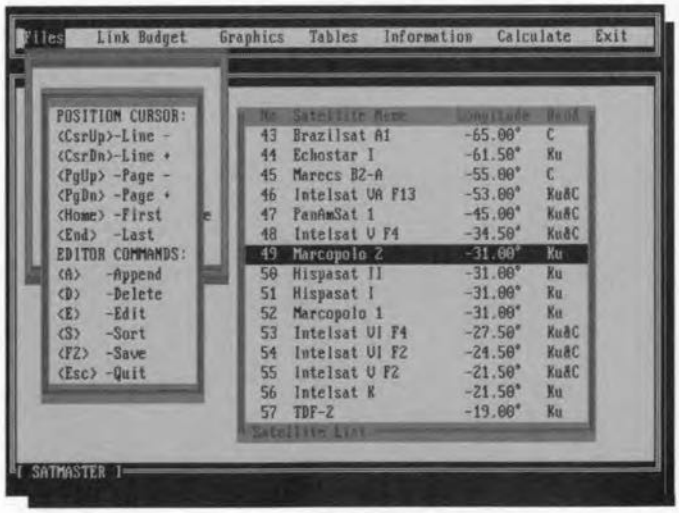
The Miller integrator circuit is based on the operational amplifier. With proper selection of the opamp, and a couple circuit precautions, the Miller integrator will work well in signals processing circuits. ■

Notes (tech. ed.):

1. Strictly speaking, the gain is given by the term $-1/\omega RC$, where $\omega=2\pi f$. However, since we are dealing with near-DC signals here, ω will be very small, which allows the simpler term to be used with impunity.

2. If the signal source is AC-coupled: I_{bias} of the CA3140 is about 50 pA, so that an offset of 0.5 mV is introduced with R_c=10MΩ. This offset, in turn, causes a noise voltage of about 400nV/√Hz.

SATMASTER SOFTWARE AIDS SATELLITE TV RECEPTION



SATMASTER from Swift Television Publications is a software package aimed at all those with an interest in setting up satellite TV reception equipment. Written to run on MSDOS PCs, SATMASTER provides comprehensive information on setting up the dish antenna, as well as on the expected signal quality, which is computed on the basis of the well-known 'downlink budget'. All parameters that go into setting up the downlink budget are entered into the program at very high accuracy via pull-down menus. SATMASTER uses parameters like satellite transmit power, dish diameter, LNB noise temperature, dish type and efficiency, receiver position on earth, receiver bandwidth, and many more, to provide the user with a signal quality indication in the form of a signal-to-noise ratio. Also, dish positioning info is provided.

The program is very simple to set up. The default parameter entries and datafile contents presented by the program are very acceptable in most cases, which should remove some of the fears of beginners confronted with questions they can not answer without a deep knowledge of satellite TV reception technology. As such, SATMASTER is equally suitable for the TV professional and the enthusiast. The program caters for all possible needs, right from installation of motorized systems to a printout of a full downlink budget analysis of any satellite at any location in the world.

The SATMASTER program and accompanying manual are available from Swift Television Publications. The price is £35, which includes postage in the UK, or for Europe, add £2, or add £4 for the rest of the world.
Swift Television Publications, 17 Pittsfield, Cricklade, Swindon, Wilts SN6 6AN. Telephone/fax: (44) 0793 750620.

AUDIO-VIDEO PROCESSOR TYPE AVP300 – PART 4

gig506-IV

An ELV design

THE audio-video processor is constructed on four printed circuit boards: potmeter board, measuring 314.5×159.5 mm (Fig. 9), mother board, measuring 330×198 mm (Fig. 10), intermediate board, 232×198 mm and the switches board, 145×35 mm (both in Fig. 11).

There are no special comments regarding the components, but the following points should be borne in mind.

- All ceramic capacitors, the four SCART connectors, the ten shift potmeters and the four push-button switches must be mounted as close to the board as possible.
- The 15 LEDs must be mounted so that their tops protrude 23 mm through the board.
- Soldering pins ST_{303} and ST_{304} and headers STL A' and STL B' must be soldered at the track side of the intermediate board. If the pins of the headers just do not protrude through the board, there is just enough room to solder them.
- The mains transformer must be fastened with four M4×6 nuts and bolts before its connections are soldered.
- Voltage regulators IC_{501} and IC_{502} must be fitted to a common heat sink, which is then fitted lying down on to the board. Here again, bolt the heat sink down before soldering any connections.
- Resistor R_{626} is normally a wire link. In some cases, however, it may be required to keep the regulating speed of the phase-locked loop (PLL) to which R_{626} belongs down. This is so if, for instance, the processor is used purely as a multi-standard decoder. In that case, R_{626} should be 820 kΩ. If the processor is used in conjunction with a video recorder, it is advisable, however, to use the higher speed of the PLL.
- The terminal wires of all components should be cut as short as feasible.
- In a number of locations, the MKT capacitors are very close together; take care that the non-insulated ends of these components do not touch each other.

The mother board of the audio-video processor built in the Elektor Electronics laboratory was found to have no earth connections for a number of components since it had been forgotten to drill the relevant holes. This deficiency is easily overcome by scratching away the solder mask in these locations and solder the relevant component terminal directly to the earth plane at the component side of the board.

When all components have been mounted and soldered, check carefully that there are no bits of solder across tracks.

> The size of a metric bolt or screw is defined by the letter M followed by a number corresponding to the overall diameter of the thread in mm, the × sign and the length of the bolt or screw, also in mm. For instance, an M4×6 bolt has a thread diameter of 4 mm and a length of 6 mm. The overall diameter of the thread in the BA sizes is: 0 BA = 6.12 mm; 2 BA = 4.78 mm; 4 BA = 3.68 mm; 6 BA = 2.85 mm; 8 BA = 2.25 mm.

Wiring

Wiring is in many instances perhaps the wrong word: often two boards are soldered together without any wires. For instance, the switches board is pushed upright over the SCART connectors into the recesses in the mother board. Corresponding tracks of the two boards are then simply soldered together. It is advisable to start by connecting the outer two tracks first in such a way that the switches board sticks out about 1.5 mm over the mother board.

A cable containing three individually screened wires should be used to connect terminals W, B and G on the mother and switches boards. The three screens should be soldered to sol-

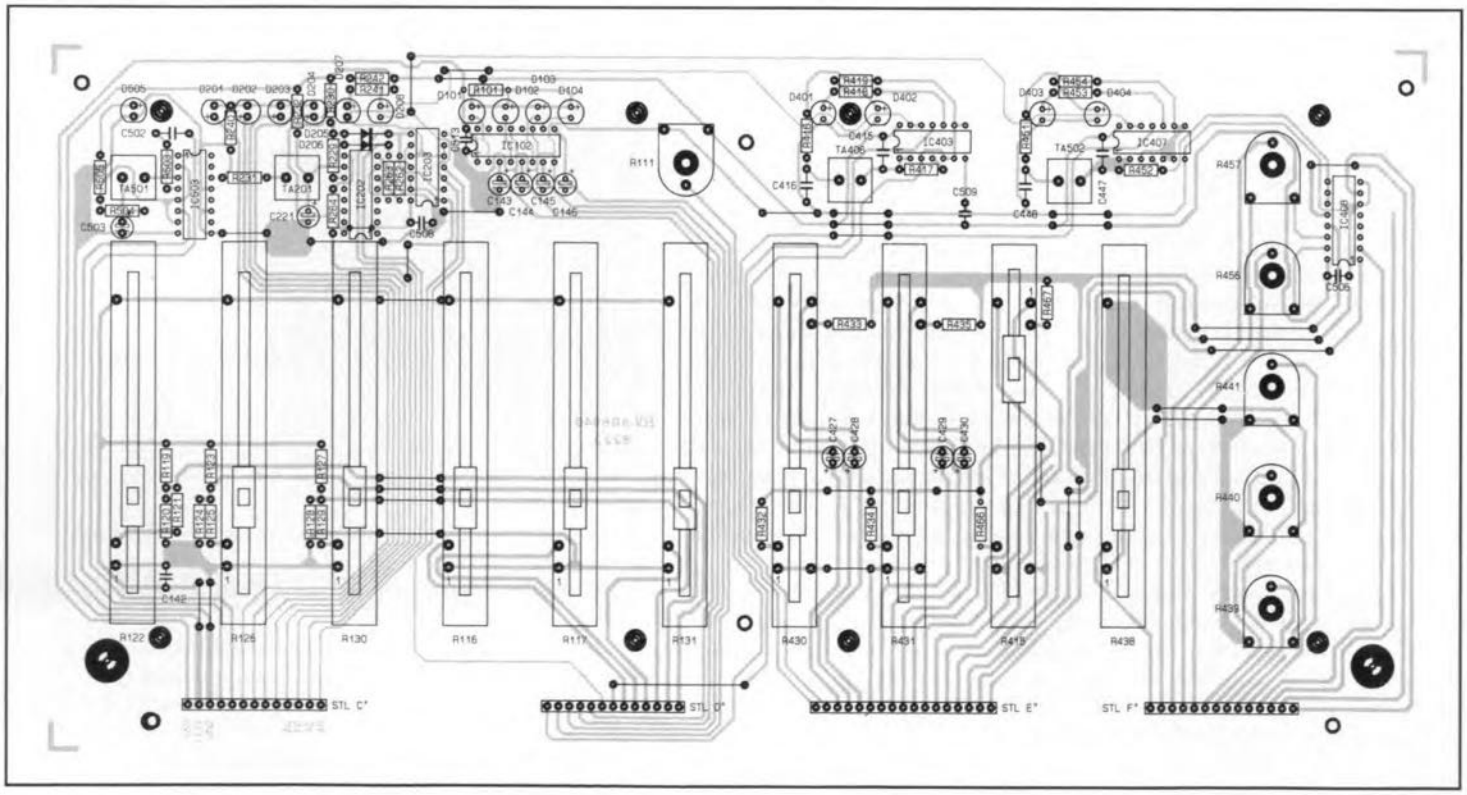


Fig. 9. Component layout of the potmeter board.

der pin A. On the switches board, connect the wires directly to the relevant terminals of switch S_{201}.

The boards are interconnected by lengths of flatcable between terminals points A–F as shown below.

A 5 cm long, 13-way; 2 connectors.
B 5 cm long, 16-way; 2 connectors.
C, D 10 cm long, 13-way; 1 connector.
E 10 cm long, 17-way; 1 connector.
F 10 cm long, 14-way; 1 connector.

The six lengths can be made from a 25 cm long, 32-way piece of flatcable: they are easily separated with a pair of scissors. Four of the 'cables' are terminated into a connector at only one end; their free ends should be soldered to the track side of the potmeter board. The connectors are press-on types that can be fitted to the 'cables' by clamping them on to the cable in a vise.

The connections ST_{203}–ST_{303} and ST_{204}–ST_{304} can be made with lengths of circuit wire about 35 mm long. This is best done when the boards are already interconnected by flatcable and the intermediate board is 'hinged' upwards as shown in Fig. 12.

COMPONENTS LIST

Potmeter board

Resistors:
R101, R240, R505 = 560 Ω
R11 = 10 kΩ preset
R116, R117, R122, R126, R130, R131 = 10 kΩ shift potmeter, mono, linear
R119 = 100 kΩ
R120 = 27 kΩ
R121 = 68 kΩ
R123 = 820 kΩ
R124 = 220 kΩ
R125 = 680 kΩ
R127 = 180 kΩ
R128 = 15 kΩ
R129, R230 = 56 kΩ
R229, R432–R435, R466, R467 = 47 kΩ
R231 = 100 Ω
R232 = 10 kΩ
R241, R242 = 1.2 kΩ
R262–R264, R418, R419, R453, R454 = 1 kΩ
R415, R430, R431 = 47 kΩ, shift pot meter, stereo,linear
R416, R451 = 1 MΩ
R417, R452 = 100 kΩ
R438 = 47 kΩ shift potmeter, mono, linear
R439–R441, R456, R457 = 47 kΩ preset
R503, R504 = 100 kΩ

Capacitors:
C142, C506, C508, C509, C513 = 100 nF, ceramic
C143–C146, C221 = 2.2 µF, 16 V
C415, C447, C502 = 10 nF
C416, C448 = 100 nF
C427–C430, C503 = 1 µF, 16 V

Semiconductors:
D101–D104, D201–D204, D207, D208, D401–D404, D505 = LED, 5 mm, red
D205, D206 = 1N4148
IC102, IC503 = 4049
IC202 = 4040
IC203 = 4011
IC403, IC407 = 4001
IC408 = 4053

Miscellaneous

TA201, TA401, TA402, TA501 = push-button switch

Initial tests

Figure 12 shows the preferred positioning of the boards for the first test and adjustments. Flatcables E and F cannot yet be connected. Make sure that that the 'hinged upwards' intermediate board cannot touch the switches board.

When the power is switched on, the relevant LED should light. With a voltmeter, check the output voltage of the voltage regulator: negative to heat sink and positive to the pin furthest away from the transformer. If the measured voltage differs more than 5% from the specified one, there is a fault somewhere, which must be rectified before further work can be done.

Next, replace the mains fuse by an ammeter set to the 1 A a.c. range. With power on, the meter should read 600–800 mA. If the current is appreciably higher, check the correct operation of T_{501}.

Correct reaction of the LEDs to the electronic switches indicates that the control signals to these switches are all right. The LEDs that indicate the video standard behave like a running light: as long as no standard is recognized, the decoder continues scanning.

Adjustment

Although no special test equipment is required if operation on only one television standard is required (the test card received on a TV receiver or video recorder is then sufficient), a test pattern generator is required for multi-standard operation. This generator should provide PAL, SECAM and NTSC 3.58 MHz signals. NTSC 4.43 MHz requires no adjustment, since that is included in the PAL calibration.

Connect a TV receiver with video input, or, preferably, RGB inputs, to one of the outputs of the audio-video processor and apply the test signal to one of the inputs, but not to an S-VHS one.

Set all potmeters in the video section on the potmeter board to the centre of their travel.

Set the switch at the extreme left of the switches board (RGB out) in accordance with the input of the used TV receiver (left = RGB; right = CVBS). Set the other switches, starting with the one adjacent to the RGB out switch as follows: right, left, right, right, left.

If all is well, the receiver should show some sort of test pattern. Adjust R_{616} (line synchronization) until the picture is stable and then set it to the centre of the range over which stability is obtained. The edges of the picture are determined by the flyback pulse. Adjust the width of this pulse with R_{621} until the picture is centred on the screen. If you have an oscilloscope, this pulse may be measured at pin 6 of IC_{602}: ideally, it should be 12 µs. At the same time, check the shape of the sandcastle pulse at pin 7 of IC_{601}.

If all is well, the screen should now show a good black-and-white picture; if not, there is a fault that must be rectified before further work can be done.

The chroma filter is best calibrated with a SECAM signal (4.286 MHz), because its Q factor is then optimum. Connect pin 27 of IC_{101} to the +12 V line (which sets the decoder to SECAM) and apply a SECAM signal to one of the inputs. Adjust L_{202} for optimum colour reproduction (if a monitor with a composite video input is used, adjust L_{202} for optimum quality). If an oscilloscope is available, adjust L_{202} for minimum amplitude of the signal at pin 15 of IC_{101}. If only a PAL signal is available, connect pin 28 of IC_{101} to the +12 V line and carry out the procedure as described.

Continuing with the SECAM signal, adjust L_{101} until the red and blue in the picture have the same brightness. Then adjust the receiver for a black-and-white picture and set the grey of the picture as desired with R_{102}.

If an oscilloscope is available, adjust L_{101} until the level of the black signal at pin 3 of IC_{101} is the same as that of the sync signal. Lastly, adjust R_{102} until the level of the black signal at pin 1 of IC_{101} is the same as that of the sync signal.

Remove the +12 V line from pin 27 of IC_{101} and connect it to pin 28 of this IC. Also, strap ST_{101} to ST_{102}. Connect an oscilloscope to pin 1 or pin 3 of IC_{101}, apply a PAL signal to one of the inputs (not S-VHS), and adjust C_{116} until the drifting of the colours is a minimum.

Then, replace the PAL signal by an NTSC 3.58 MHz (also called NTSC/M) signal, shift the +12 V line from pin 27 to pin 26 of IC_{101} and adjust C_{117} until the drifting of the colours is a minimum.

If an RGB receiver or monitor is used, the screen should now show a faultless colour picture. If a CVBS signal had to be used, this may not be so, because the encoder has not yet been calibrated.

Remove the link between ST_{101} and ST_{102} and the +12 V line from pin 26 of IC_{101}, and set the RGB out switch to CVBS. Apply a PAL signal to one of the inputs and set C_{316} to the centre of the range over which the picture is in colour. Then, set the 4.43/3.58 MHz switch to 3.58 MHz, apply an NTSC/M signal to one of the inputs and set C_{319} to the centre of the range over which the picture is in colour. Note that the band filters in the encoder have already been calibrated during manufacture.

Finally, adjust L_{203} and L_{204} (band-stop filters) for minimum cross-luminance interference. If an oscilloscope is available, connect it across R_{206} and adjust these inductors until the residue of the colour subcarrier on the luminance signal is a minimum.

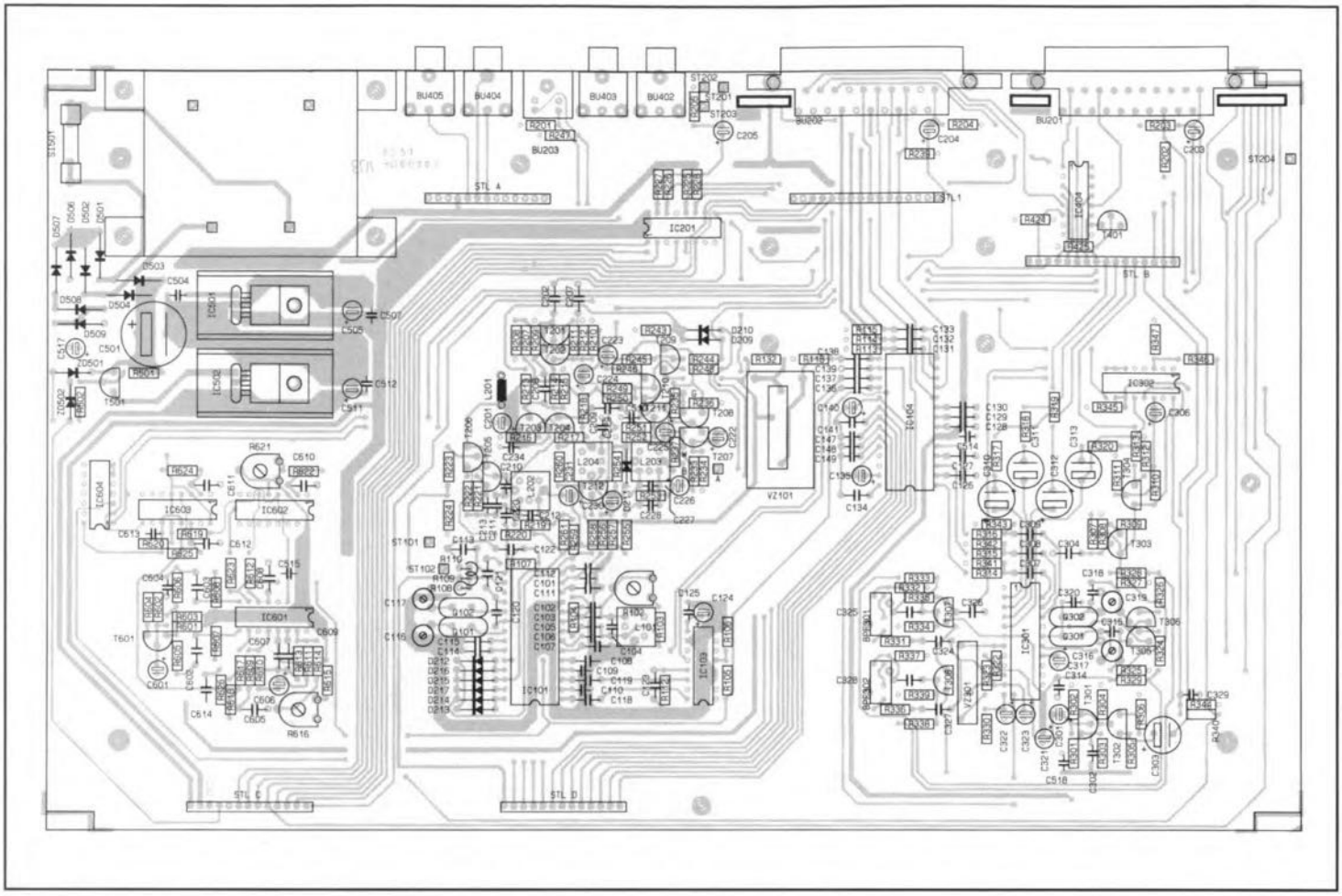


Fig. 10. Component layout of the mother board.

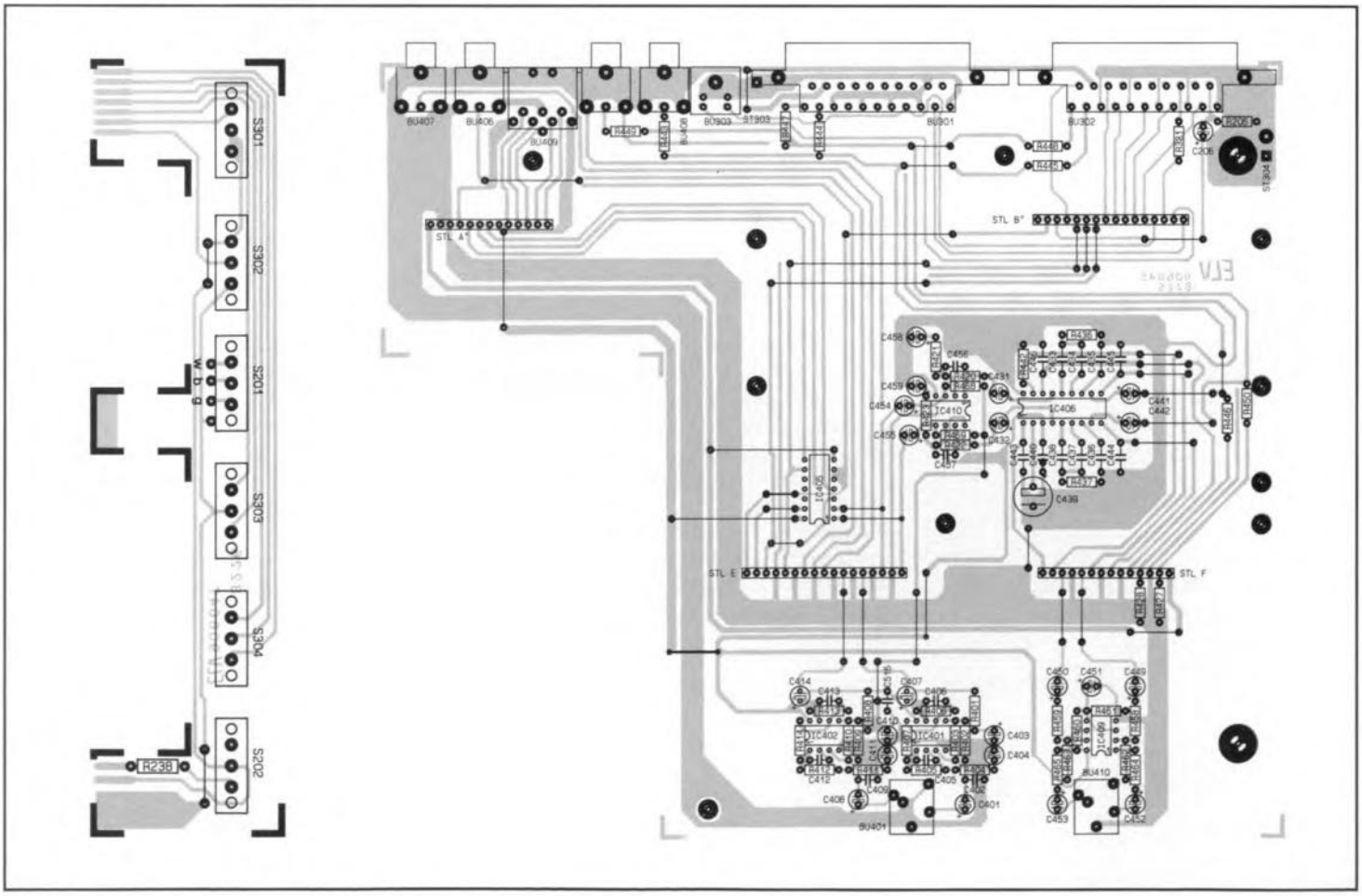


Fig. 11. Component layout of the switches board (left) and intermediate board.

Assembly

Commence with assembling the upper part of the enclosure, the front panel and the potmeter board. Make sure that no parts of the enclosure touch any components on the board. Fasten the board to the upper half of the case with six self-tapping screws. Next, fit two M4 bolts in the appropriate holes in the front of the enclosure; do not tighten these too much. Finally, fasten the front panel to the board with seven insulated screws and one

COMPONENTS LIST

Mother board

Resistors:
R103 = 680 Ω
R104, R220, R223, R259, R501 = 4.7 kΩ
R105, R106, R219, R224, R256, R261, R308, R333, R334, R338–R340, R425, R601, R613, R615, R617–R620, R622 = 10 kΩ
R107, R110 = 3.3 kΩ
R108, R210, R213, R301 = 18 kΩ
R109, R243 = 6.8 kΩ
R112 = 1 MΩ
R113–R115, R201–R205, R239, R247, R305, R313, R317–R320 = 75 Ω
R118, R255, R610 = 1.2 kΩ
R132, R257, R322, R323, R328, R329, R331, R332, R335–R337, R344, R612 = 1 kΩ
R207, R208, R211, R212, R214, R215, R251, R324, R326, R345 = 47 kΩ
R209, R216, R260, R605 = 270 Ω
R217, R218 = 39 kΩ
R221, R222 = 330 Ω
R225–R228, R233, R234, R244, R248, R253 = 22 kΩ
R235, R237, R254, R502 = 270 Ω
R236, R606 = 2.7 kΩ
R245, R246, R249, R250, R302 = 56 kΩ
R252, R330 = 27 kΩ
R258, R307, R311, R325, R327, R346, R347 = 15 kΩ
R303, R304, R309, R312 = 220 Ω
R306 = 47 Ω
R310, R625 = 8.2 kΩ
R314–R316, R341–R343 = 1.8 kΩ
R424, R611 = 100 kΩ
R602 = 1.5 kΩ
R603 = 820 Ω
R604 = 150 Ω
R607 = 2.2 MΩ
R608 =1.5 MΩ
R609, R623 = 3.9 kΩ
R614 = 82 kΩ
R624 = 470 kΩ
R626 = 820 kΩ
R102 = 470 Ω preset
R616, R621 = 25 kΩ preset

Capacitors:
C101, C147–C149, C234, C314, C504, C507, C510, C512, C514, C515, C518, C613 = 100 nF, ceramic
C102, C106 = 15 pF
C103–C105, C212, C213, C227, C302 = 150 pF
C107, C108, C122, C138, C307–C309, C324–C328, C614 = 100 nF
C109, C110, C220 = 220 pF
C111, C112, C123, C607 =10 nF
C113, C121, C126, C127, C134 = 330 nF
C114, C115, C128–C133, C136, C137, C139, C141 = 22 nF
C116, C117, C316, C319 = 2–40 pF trimmer
C118, C119, C202, C207–C209, C304, C610, C612 = 1 nF
C120 = 47 nF
C124, C301, C306, C317, C322, C323, C505, C511 = 10 µF, 16 V
C125 = 22 nF, ceramic
C135, C222–C226, C230 = 22 µF, 16 V
C140, C606 =4.7 µF, 16 V
C201, C203–C205, C601 = 47 µF, 16 V
C210 = 2.2 pF
C211, C320 = 33 pF
C228 = 68 pF
C229 = 120 pF
C231 = 2.2 µF, 16 V
C303, C310–C313 = 470 µF, 16 V
C315, C318 = 10 pF
C321, C517 = 100 µF, 16 V
C329, C604 = 100 pF
C501 = 2200 µF, 40 V
C602 = 470 nF
C603, C608 = 220 nF
C605 = 680 nF
C609 = 3.9 nF
C611 = 8.2 nF

Semiconductors:
D209–D217 = 1N4148
D501–D504, D506–D509 = 1N4001
ZD501 = zener, 5.6 V, 400 mW
ZD502 = zener. 6.8 V, 400 mW
T501 = BC327
T201–T212, T302–T304, T307, T308, T401, T601 = BC548
T301, T305, T306 = BC558
IC101 = TDA4650
IC103 = TDA4660
IC104 = TDA3505
IC201, IC404 = 4052
IC301 = TPE1378A
IC302 = 4053
IC501 = 7812
IC502 = 7805
IC601 = TDA1180P
IC602, IC603 = 4528
IC604 = 4070

Miscellaneous:
L101, L202–L204 = 10 µH
L201 = 51 µH
Q101 = crystal 8.85724 MHz
Q102 = crystal 7.15909 MHz
Q301 = crystal 4.43 MHz
Q302 = crystal 3.58 MHz
BFP301 = 3.58 MHz band-pass filter
BFP302 = 4.43 MHz band-pass filter
VZ101 = 330 ns delay line
VZ301 = 180 ns delay line
BU201, BU202 = SCART socket for PCB mounting
BU203 = S-VHS socket
BU204 = BNC socket
BU402–BU405 = audio socket
SI501 = fuse holder and 800 mA fuse
STL A, STL C, STL D = 13-way header for PCB mounting
STL1, STL B = 16-way header for PCB mounting
Mains transformer 240 V to 15 V, 12 VA, with integral mains cable
Flatcable and connectors (see text)
Heat sinks (2) for IC501 and IC502

Intermediate board

Resistors:
R206 = 75 Ω
R321 = 82 Ω
R401–R403, R408–R410 = 47 kΩ
R404, R411 = 3.3 kΩ
R405, R412 = 100 kΩ
R406, R413 = 12 kΩ
R407, R414, R427, R428, R443–R445, R447–R449 = 10 kΩ
R420–R423. R436, R437, R458, R459 =10 kΩ
R442 = 2.2 kΩ
R446, R450 = 47 kΩ
R460, R461 = 56 kΩ
R462, R463, R468, R469 = 470 kΩ
R464, R465 = 120 Ω

Capacitors:
C206 = 47 µF, 16 V
C401, C404, C407, C408, C411, C414, C454, C455 = 1 µF, 16 V
C402, C406, C409, C413 = 100 pF
C403. C410, C449–C453, C458, C459 =10 µF, 16 V
C405, C412, C456, C457 = 22 pF
C431, C432 = 2.2 µF, 16 V
C433, C434, C437, C438 = 56 nF
C435, C436 = 15 nF
C439 = 100 µF, 16 V
C440, C516 = 100 nF, ceramic
C441, C442 = 4.7 µF, 16 V
C443–C446 = 100 nF

Semiconductors:
BU205 = 8-way DIN socket
BU301, BU302 = SCART socket for PCB mounting
BU303 = S-VHS socket
BU401, BU410 = 3.5 mm stereo jack socket
BU406–BU409 = audio socket
STL A' = 13-way header for PCB mounting
STL B' = 16-way header for PCB mounting
STL E' = 17-way header for PCB mounting
STL F' = 14-way header for PCB mounting

Switches board

Resistors:
R238 = 82 Ω

Miscellaneous:
S201, S202, S301–S304 = slide switch, 1 change-over contact

metal one (for earth connection). If the board bends even slightly, the M4 bolts are too tight.

Fit the intermediate board to the mother board with four bolts and spacers. Fit an M4×30 bolt and a 25 mm spacer to the centre front of the mother board; an M4×35 bolt and 30 mm spacer to the centre right of this board; and two M4×40 bolts and 35 mm spacers right at the back of the board. The remaining holes in the board can be ignored here: they are intended for a possible extension connected to STL_1. Fit the BNC socket to the back panel and connect this to ST_{201} and ST_{202} (earth) via two short lengths of circuit wire.

Invert the enclosure so that its top rests on the workbench and insert a centring rod into each of the four fixing holes at the corners of the underside. Fit the assembled mother board, intermediate board and rear panel to the bottom of the enclosure with M5 bolts, nuts, washers and 60 mm and 15 mm spacers (as appropriate)—see Fig. 13. As soon as the length of the flatcables allows, connect them to the relevant board.

Next, fit the front panel—after removing the ring nuts from the jack sockets. When the front panel is seated firmly, fasten the ring nuts back on to the sockets. Then, fit the knobs to the potentiometers.

Finally, fasten the bottom of the enclosure on to the four M5 bolts with suitable washers and nuts, and fit four anti-slip feet. ■

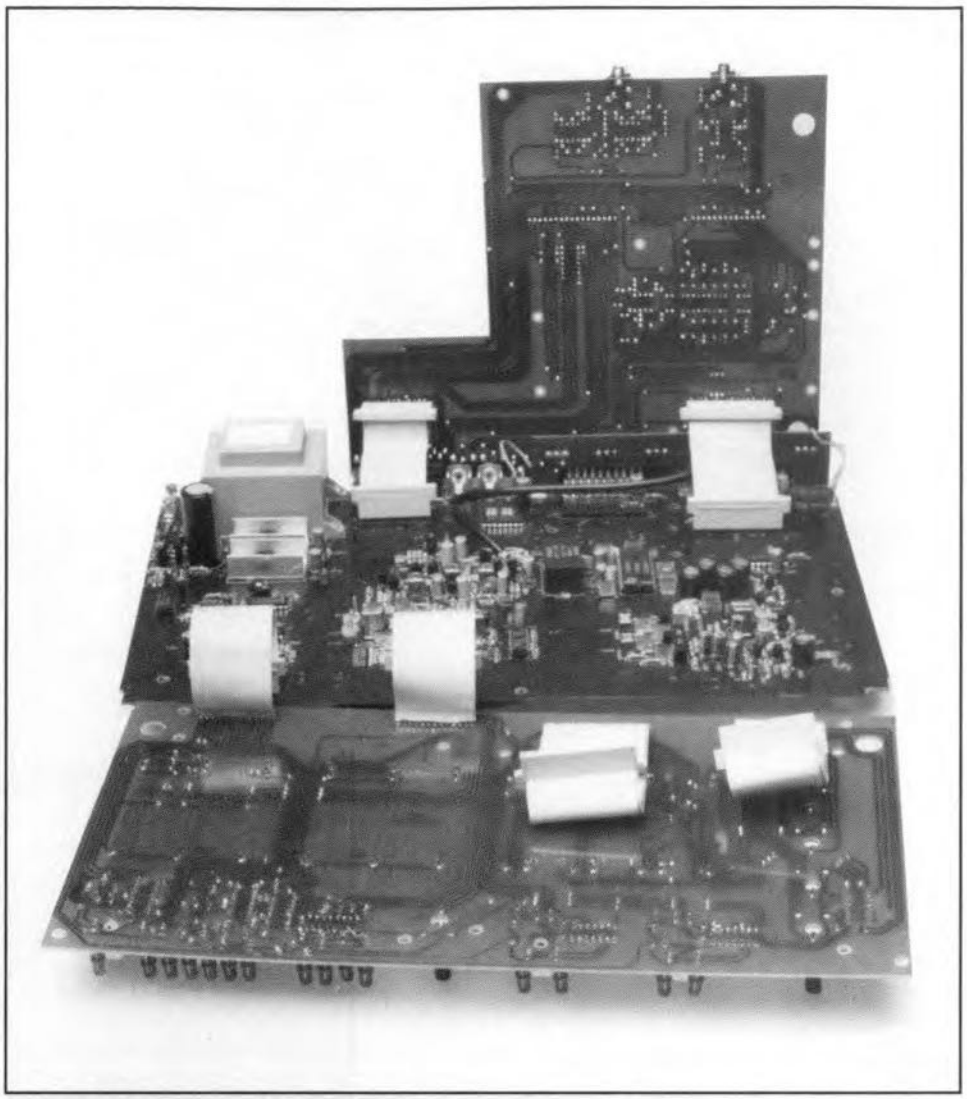


Fig. 12. With the prints hinged away from each other, all calibration points are easily accessible.

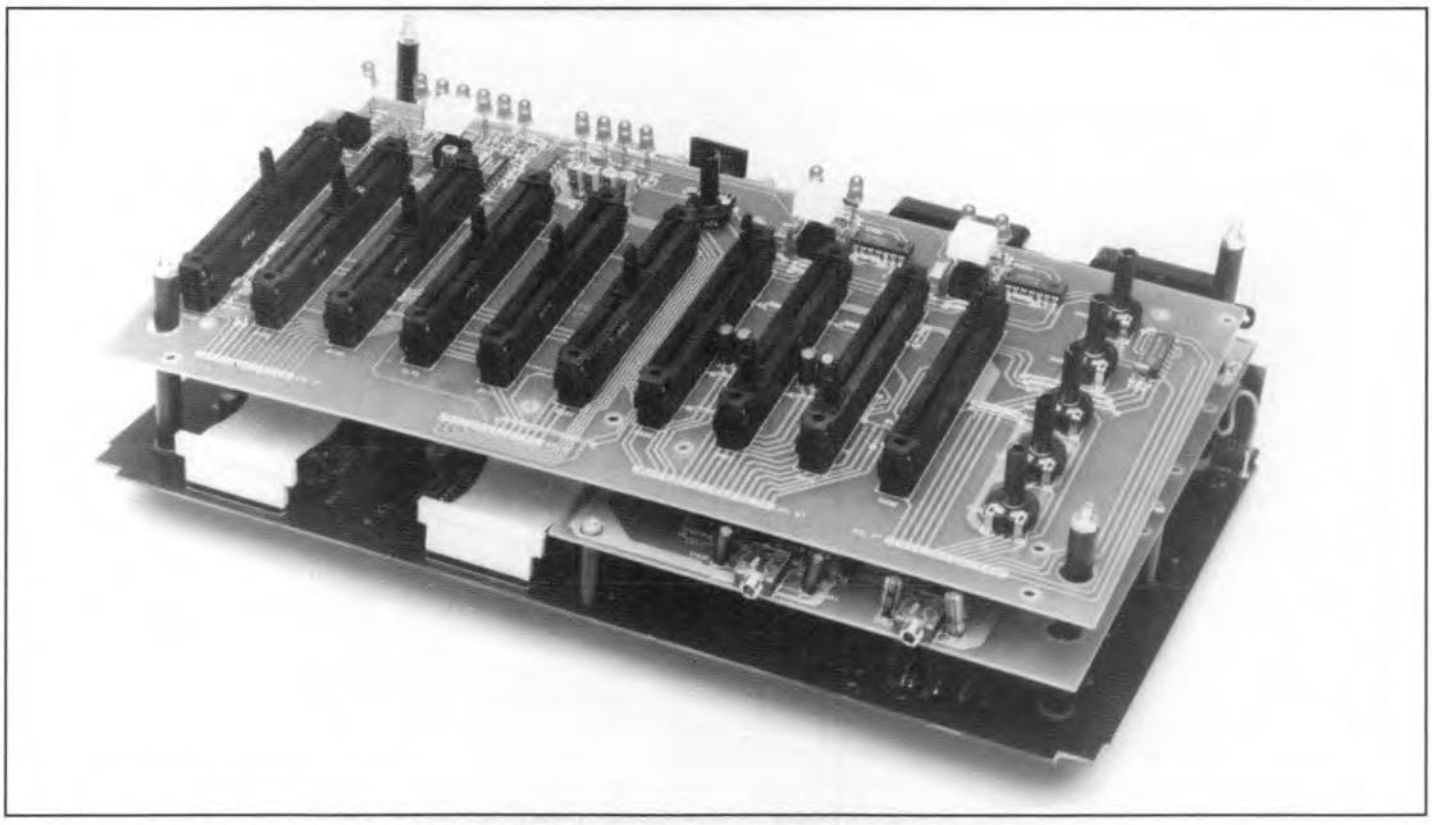


Fig. 13. The completed audio-video processor less front panel and most of the enclosure.

CURRENT-SENSE POWER MOSFETS

by J. Ruiters

Measuring a current without affecting the circuit in which that current is flowing is an ideal test method. Current-sense power MOSFETs are available nowadays that, with the aid of additional internal connections and output pins, enable that ideal to be approached. In these devices, a separate circuit is created in which a small current flows that is directly proportional to the much larger current flowing through the FET proper.

POWER FETs are typified by the drain current flowing more or less vertically through the chip as may be seen in Fig. 1. Strictly speaking, this drawing shows two parallel-connected transistors; but for clarity's sake only the area round the gate is shown. In that area are the actual drain and source connections, which are relatively large to ensure good conduction of the current to and from the transistor.

If the chip is composed of pure, doped silicon, the drain current divides equally to the two transistors. But even when the purity is not quite 100%, the current divides into two reasonably equal parts. This property is used in the construction of power FETs by connecting not two, but hundreds of transistors in parallel. How that is done in HEXFETs is shown in Fig. 4. The entire underside of the resulting chip forms the drain. The borders between the individual transistors form the hexagonal gate, which is insulated by silica (silicon oxide, SiO_2). The top of the chip is covered with aluminium that forms the source. Some power FETs have a square instead of a hexagonal gate.

The structure of the chip in Fig. 2 (whose electrical equivalent is given in Fig. 3) shows that the construction causes several undesired by-products. One of these is capacitance C_{gs}, whose value is fairly large: in current types of the order of 1 nF or more. Another one is a parasitic diode, D_{ds}, between drain and source, which, strictly speaking, is an n-p-n transistor whose base-emitter junction is short-circuited by the aluminium of the source. The diode consists of the same areas as the FET channel, so that $I_{d(max)}$ and $U_{ds(max)}$ apply to it. That is, a power FET has an integral free-wheeling diode, which is advantageous in the switching of inductive loads. In some types, the doping of the silicon is adapted to making the diode a fast recovery type: the resulting transistor is a FREDFET.

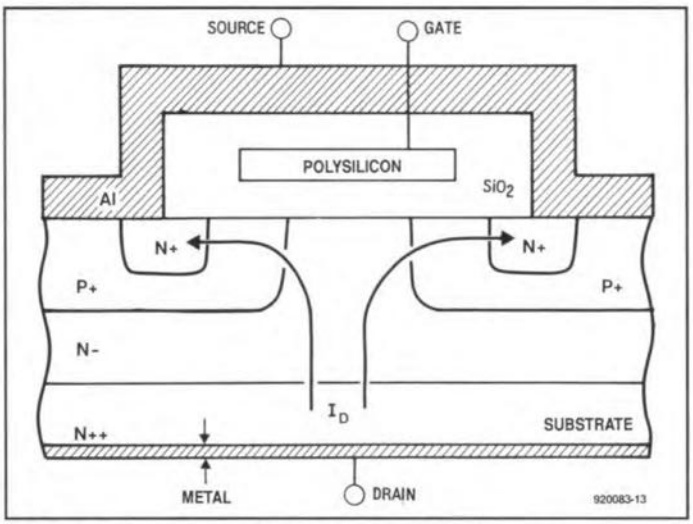


Fig. 1. Basic construction of a power MOSFET.

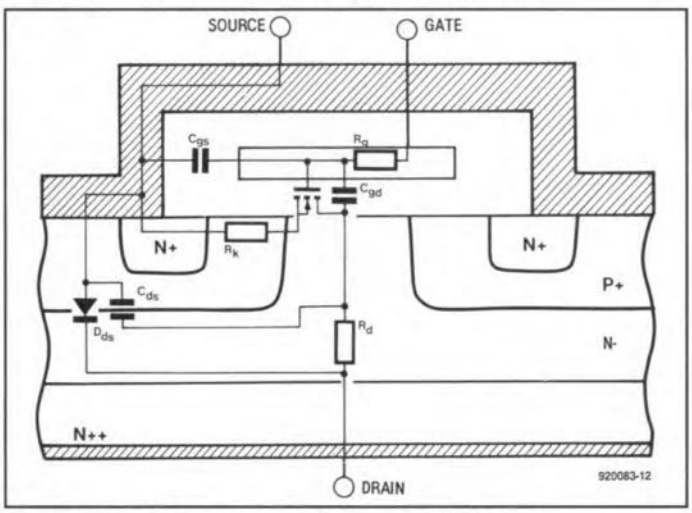


Fig. 2. Electrical structure of a power MOSFET.

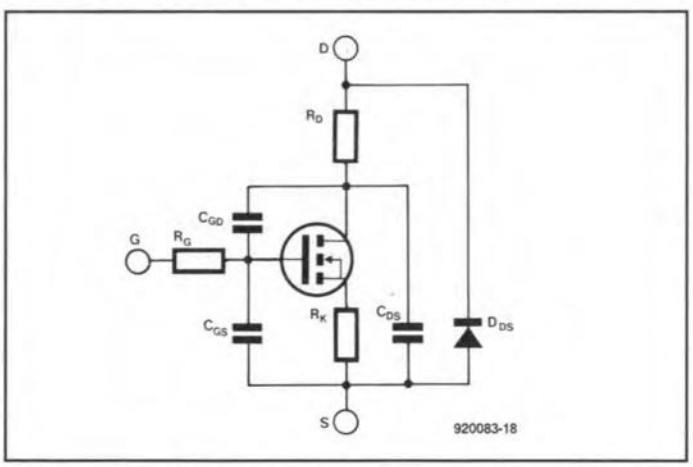


Fig. 3. Equivalent circuit diagram of power MOSFET.

FET with current sensor

Since, as stated earlier, the current through the power FET divides into equal parts through the individual transistors, each of these tiny parts is a measure of the total current. How that property can be used in practice is shown in Fig. 5: a number of the individual transistors are given a separate source connection, which is brought out via current-sense pin C. This is accomplished by isolating a section of the aluminium layer from the rest, resulting in, effectively, two power FETs on one chip—see Fig. 6. The ratio of the drain current current to the sense current is, therefore, determined by the ratio of the number of transistors that provides the sense current and that which provides the source current. Of course, in practice this may not be entirely true owing to (tiny) unevenesses, but, as long as the ratio is large, the resulting error is very small.

To measure the drain current by means of the C-pin, it is important that that pin has the same potential as the source pin. Since that is not so with an external source connection (and certainly not when the current is large), there is an internal link that is brought out via the so-called Kelvin-source pin (K-pin).

A suitable circuit for measuring the current which ensures that the C-pin is held at source potential is shown in Fig. 9. Since the + input of opamp A_1 is connected to the source of the FET via the K pin, the inverting input will be at virtually the same potential. Moreover, A_2 is a current/voltage amplifier, so that the measured current is converted into a voltage (because most applications depend on a voltage that is proportional to the measured current). The circuit also has some drawbacks: it requires two power sources and the output voltage is negative.

It is also possible to sim-

ply convert the measured current into a voltage with the aid of a resistor as shown in Fig. 7. The equivalent circuit of this setup is shown in Fig. 8. There are three possible situations:

$R_t << R_{ds(on)c}$;
$R_t \approx R_{ds(on)c}$;
$R_t >> R_{ds(on)c}$.

The situation when $R_t \approx R_{ds(on)c}$ is disadvantageous, because the effect of the temperature on the division of current between the sense branch and the power branch will then be optimally expressed in voltage U_t.

Best results are achieved when R_t is at least 10 times smaller than $R_{ds(on)c}$. This has the slight drawback that U_t is also smaller, but that can easily be rectified with a small amplifier. If an opamp is used whose output can be driven to earth potential, only one power source will suffice.

When R_t is large, the voltage across the power section, rather than that caused by the sense current across the resistor, is measured. Unfortunately, the temperature dependence of $R_{ds(on)}$ is then reflected in U_t. However, compared with a standard power FET, a current-sense FET has a slight advantage here: its sensor FET serves as a switch (provided, of course, that the power FET is also switched), and this isolates the measuring circuit from the power circuit at the instant the transistor is switched off. In that case, R_t becomes a pull-down resistor. In that way, the input of the measuring circuit is never connected to the, often high, supply voltage of the power section. That is, no special preventive measures are required.

Faster via the K pin

The switching behaviour of current-sense FETs is improved by the Kelvin connection, because the self-inductance of the source connection can then be by-passed via the K pin. In the usual circuit, where the gate voltage is connected between gate and source—see Fig. 10—the counter-e.m.f. (Ldi/dt) of this self-inductance ensures that the effective gate voltage is lowered. This reduces the switching speed. When the K connection is used for the drive circuit—see Fig. 11—the self-inductance of the source (through which a large current flows that causes a large value of di) is by-passed. The gate voltage is then not reduced, so that the transistor can switch faster. ■

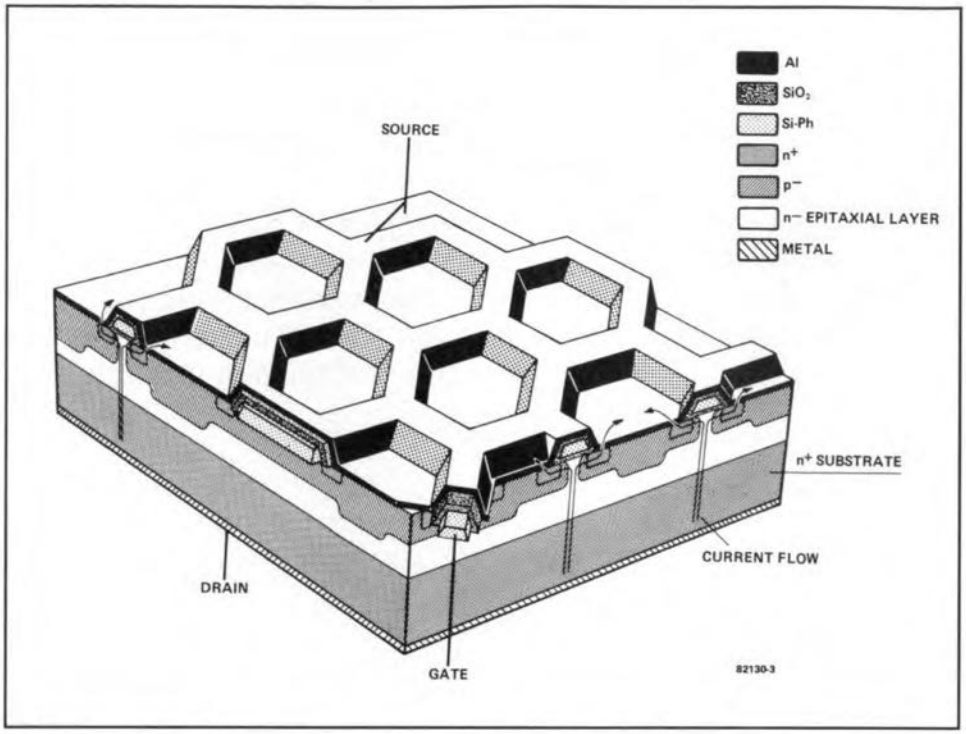
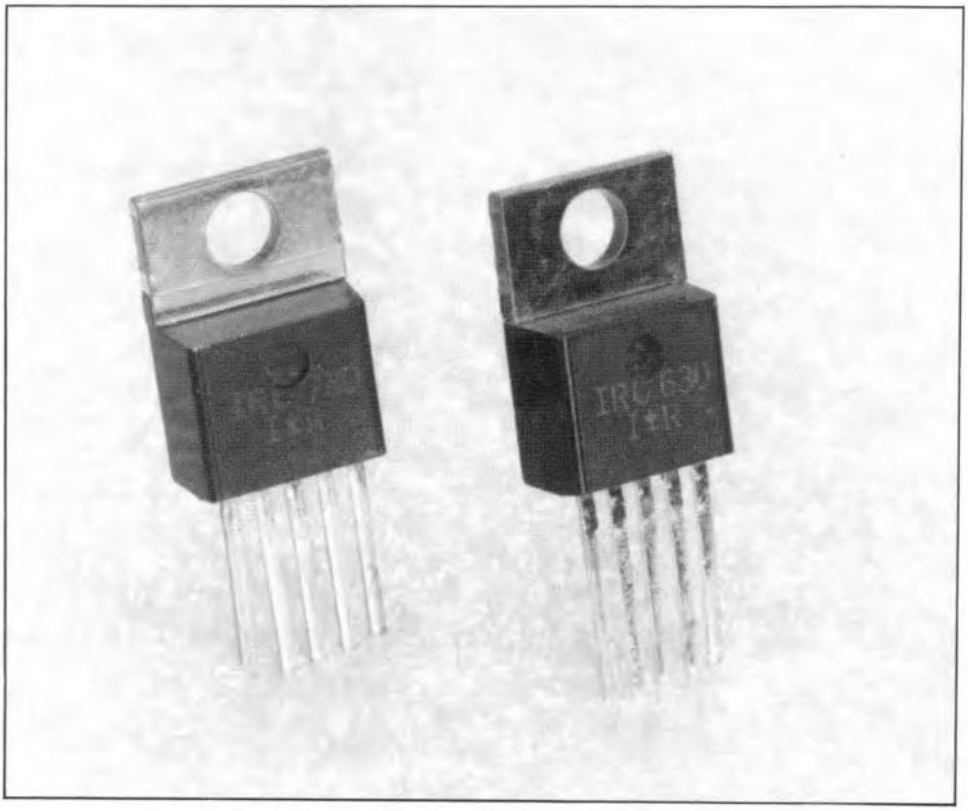


Fig. 4. A power FET consists of a great number of small FETs that are arranged in a honeycomb or, simple, a series of squares.



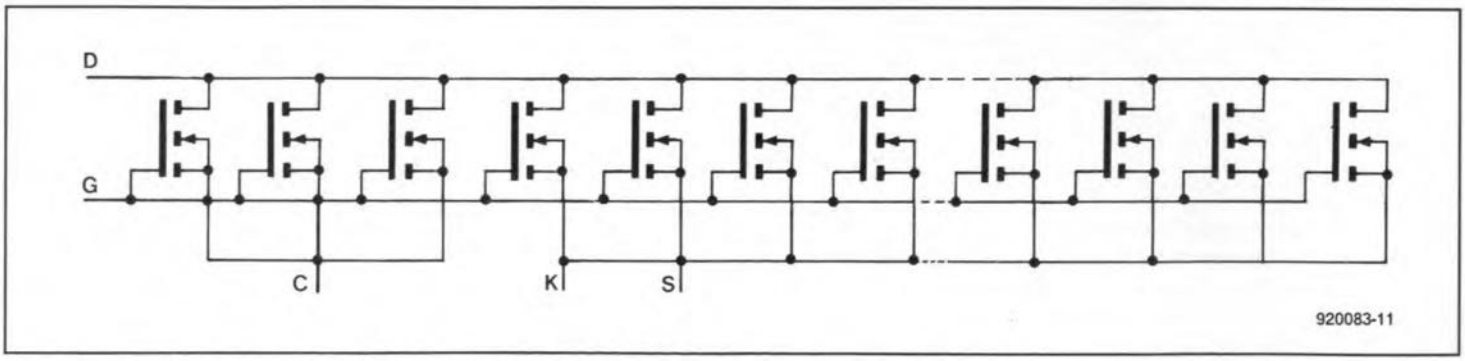


Fig. 5. Connecting a number of the constituent FETs separately creates a virtually loss-free measurement circuit.

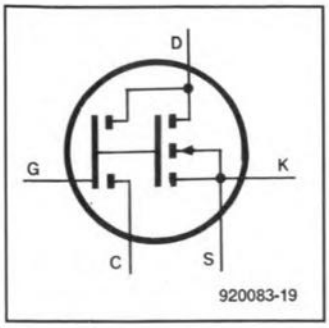


Fig. 6. Circuit symbol of a current-sense power MOSFET constructed as shown in Fig. 5.

Type	Maximum ratings (at 25° C)			Typical ratings		
	U_{ds} U_{dc} (V)	I_d (A)	P_d (W)	$U_{gs(on)}$ (V)	$R_{ds(on)}$ (Ω)	I_d/I_c
IRC530	100	14	79	10	0.12	1465
IRC531	80	14	79	10	0.12	1465
IRC830	500	4.5	74	10	1.4	1520
IRC832	500	4	74	10	1.5	1520
BUK793-60A	60	20	75	10	0.07	1570
BUK795-60A	60	38	125	10	0.035	1645
BUK993-60A	60	18	75	5	0.08	1610
BUK995-60A	60	34	125	5	0.04	1665

Table 1. Brief data of some current-sense FETs.
IRC = International Rectifier
BUK = Philips

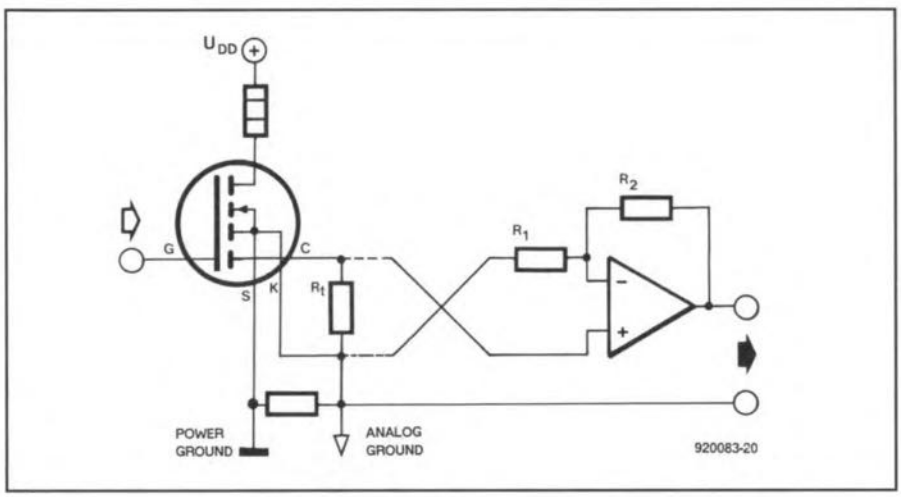


Fig. 7. How to convert the measured current into a voltage with the aid of a resistor. This is a less accurate, but much simpler, method than that shown in Fig. 5.

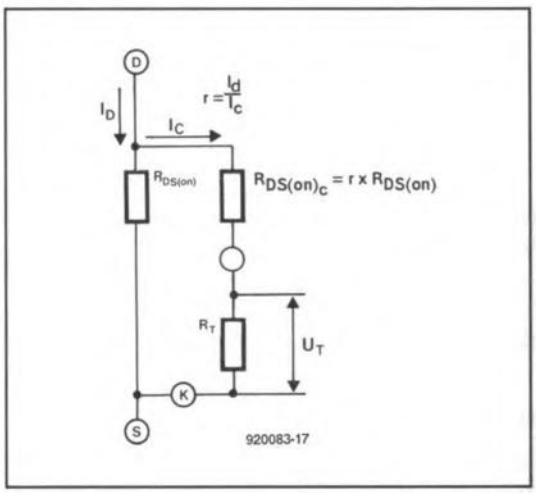


Fig. 8. Equivalent circuit of the setup in Fig. 8.

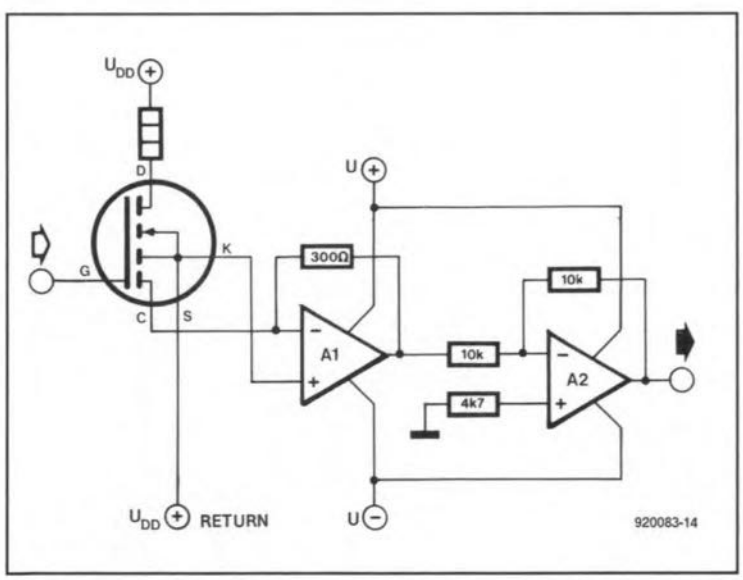
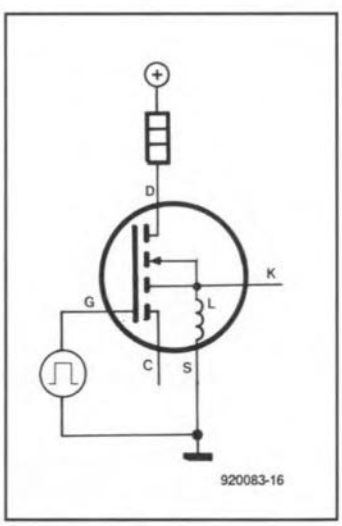


Fig. 9. The current-sense pin is held at (virtually) the source potential with the aid of opamp A_1.



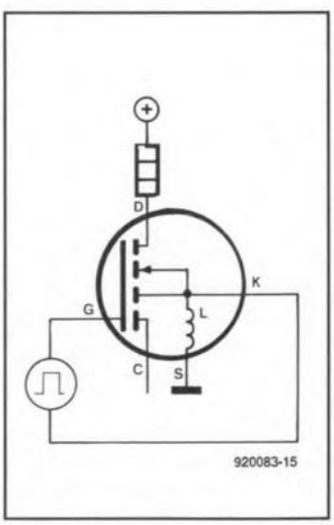
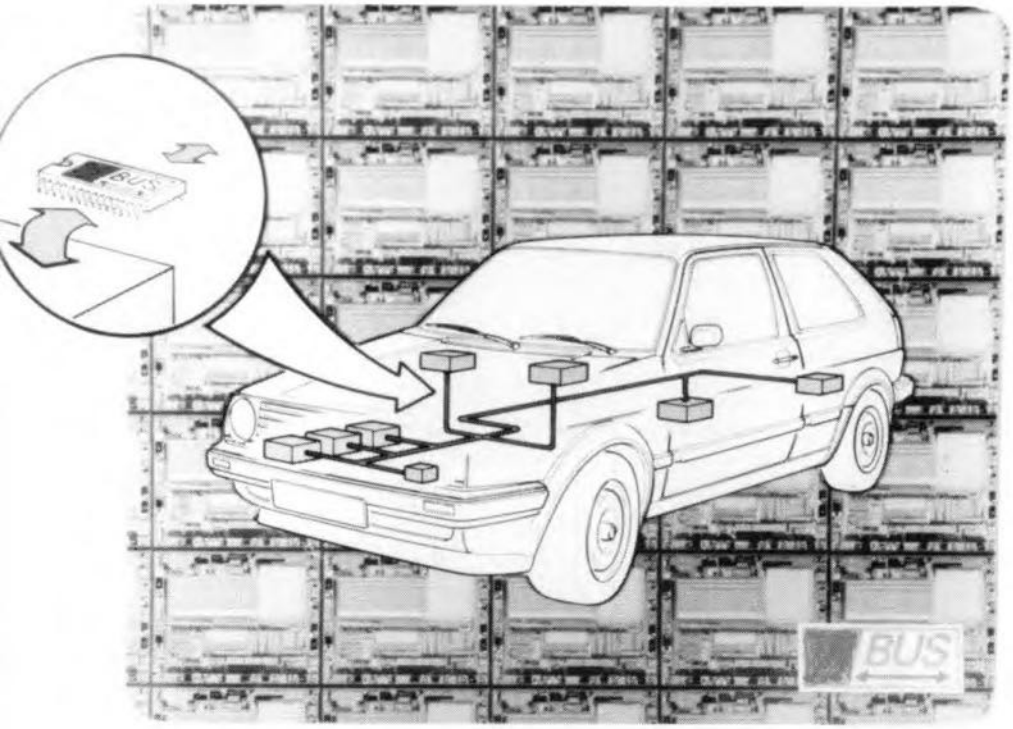


Fig. 10 and Fig. 11. Because in a current-sense FET (Fig. 11) the drive voltage to the gate may be connected in a different manner from that in a conventional power MOSFET (Fig. 10), the current-sense type has a higher switching speed.

CAN — CONTROLLER AREA NETWORK

By Achim Raab



CAN (Controller Area Network) is an advanced serial communication protocol, which supports distributed real-time control with very high noise immunity. CAN allows flexible network configurations based on different types of microprocessor and microcontroller. CANs are typically found in the automotive and industrial environment.

WITH complex mechanical systems, such as those in today's cars, the ultimate in safety can only be ensured by electronic control of all sub-systems. The need for safety and efficiency in motor vehicles has boosted the importance of automotive electronics. As most of you will be aware, there is now electronics to control fuel injection, gas emission, anti-lock braking systems, power steering, and much more.

The CAN bus is designed to meet the requirements of just about every mechanical/electronic control system or sub-system in a motor vehicle. It provides high-speed communication between electronic modules connected to a two-wire bidirectional serial bus, to control each sub-system within the vehicle. CAN provides flexibility in that special-feature modules can be added to a fixed set of basic modules without reconfiguration of any of the basic modules.

Designed to operate in an electrically very noisy environment, a unique property of the CAN protocol is its automatic error-handling capability. Extensive simulations revealed that less than one non-detected communication malfunction would occur in several thousand cars during their lifetime.

A serial bus

The basic idea behind the CAN bus is simple: each electrical load, sensor, actuator, or combination of these, in the vehicle is connected to a small computer module. This represents a total break from the concept of a central, computerized, control connected to modules via a complex wiring system. The CAN protocol is based on simple interconnection of modules via a serial dataline, and thus offers a tremendous reduction of electrical wiring in a car (it is not unusual for a typical luxury class car these days to have something like 2 km of wire 'on board', representing a weight of more than 100 kg).

The simplest CAN implementation is one where all modules are interconnected via the car chassis ('ground') and a single dataline. Each CAN module has, in principle, a single supply wire to the generator or battery, and is controlled locally by a microprocessor or CAN controller (of which several types are already available from leading IC manufacturers such as Intel and Philips Components). These controllers run dedicated software that implements the CAN bus protocol. Originally defined by Bosch in 1987, this protocol has been recognized as extremely reliable in very noisy environments, and is currently also used in many industrial control systems.

CAN features

The CAN bus has provision for a so-called multimaster structure, which may be familiar from office communication network systems such as Ethernet. Each bus user ('node', or simply 'unit') is allowed to start sending messages as soon as the bus is free (CSMA; carrier sense multiple access). In contrast to other bus systems, such as, for instance, Token Ring, bus users need not wait for permission to start transmitting.

A new aspect of CAN is object-oriented message transfer. Many other types of bus system, such as I^2C, are based on user addressing. In these systems, each bus user has its own, unique, address. If unit 'A' wants to convey a message to unit 'B', it transmits an information block that contains the address of 'B', and the actual data. Unit 'B' only accepts data when it recognizes its own address on the bus.

The CAN bus is based on a different principle. The bus units do not receive addresses, but messages are provided with an object identifier (Fig. 1). In a measurement system, for instance, each measured quantity (temperature, voltage, engine speed) may be assigned its own identifier, which is transmitted along with the measured quantity. Each module connected to the bus may receive and process this measured quantity, in as far as it is relevant to its function in the vehicle. The object identifier is an 11-bit word, which allows up to 2,048 different objects to be used. In practice, this number is reduced to 2,032 because some identifiers are reserved for special functions.

A with any multimaster bus system, provision has to be made to prevent bus collisions when two or more units find

that the bus is free, and start to transmit. The CAN protocol offers an efficient priority-oriented bus arbitration system, CA (collision avoidance), to prevent data corruption owing to bus collision.

The CAN protocol defines two different bit levels on the bus: the dominant bit level, and the recessive bit level. A dominant bit level overwrites a recessive bit level. These levels are easiest realized with the aid of open-collector bus drivers as shown in Fig. 2. A recessive bus level is set up when all transistors are off (inputs A, B, C and D at 0 V). If only one transistor is switched on, the recessive bus level is overwritten by a dominant bus level. During the arbitration phase, the 11-bit identifier is placed on the bus, bit-by-bit. At the same time, the transmitter reads back the bit state on the bus, and compares it with the bit just sent. If the two bit levels are different, the transmit operation is immediately halted. In this way, bus collisions are prevented. An example: let us assume that units 'A' and 'B' start to transmit simultaneously. Unit 'A' transmits an object with identifier 01100111001, and unit 'B' an object with identifier 01110111001. Further, let us assume that the dominant bus level is '1' (see Fig. 2). Units 'A' and 'B' each send their first, second and third bit. Since the bit levels are identical, neither unit will detect an error when it reads back the bit level on the bus. However, when the fourth bit is put on the bus, unit 'A' detects an error, because the recessive bit transmitted by it is overwritten by the dominant bit that originates from unit 'B'. The result is that unit 'A' stops transmitting, and unit 'B' is allowed to complete its transmission (note that the transistors invert their drive signals).

The CA system has two advantages. Firstly, the binary value of the identifier allows units to be assigned different priority levels. When two bus units happen to transmit simultaneously, the message from the unit with the lowest identifier value is transmitted first. The second advantage is that the message is not interrupted. With other bus protocols, both bus units stop their transmission when a bus collision occurs, and start random timing generators before attempting to convey the message again. This system is referred to as CD (collision detect).

Given the large number of automotive control functions in a vehicle, it will be clear that real-time communication is a must. Hence, the speed of the CAN must be as high as possible. In principle, the speed of the CAN is limited by the propagation delay in the bus wires, and that in the bus drivers, only. Assuming that a twisted wire pair is used, and the bus drivers have a propagation delay of 100 ns, a bit rate of 1 MBit s^{-1} can be achieved on a bus with an effective length of 40 m. When the bit rate is lowered, the maximum bus length increases accordingly to 10,000 m.

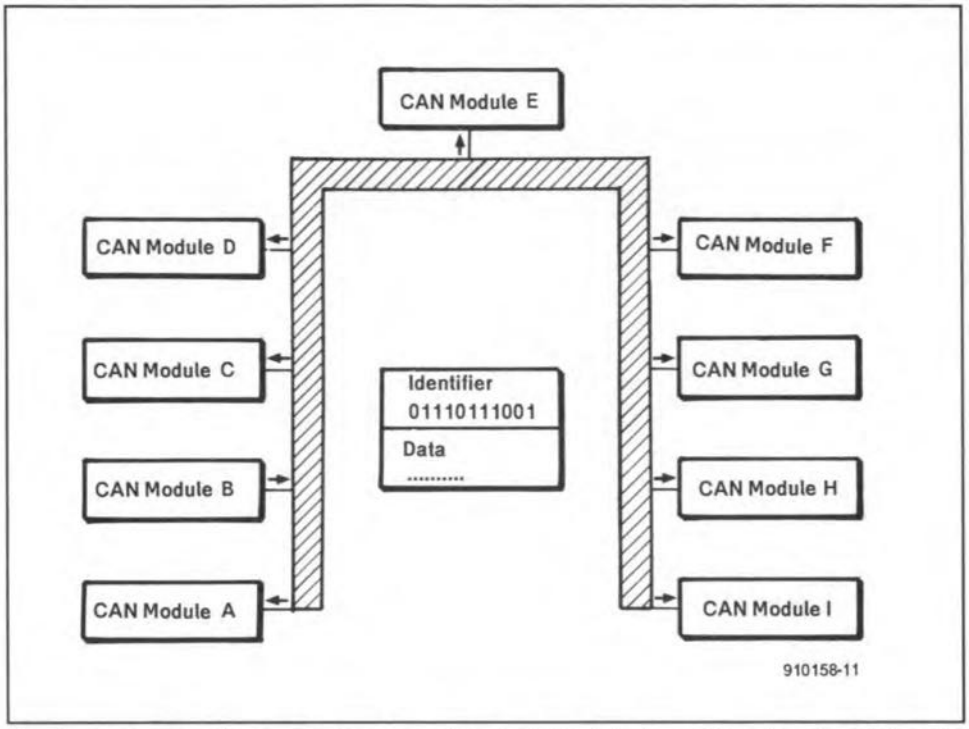


Fig. 1. Contary to other bus systems based on individual device addressing, the CAN protocol makes use of so-called object identifiers to ensure that messages reach the correct destination (i.e., module).

An object has room for data blocks with a maximum of 8 data bytes each. This may appear a relatively small number, but bear in mind that the CAN bus is not intended to convey large quantities of data. Normally, 8 bytes are more than enough to convey measurement values and process states.

The effective data rate is an important characteristic when it comes to judging the 'real' data speed on a bus system. The effective data rate is basically the ratio between the effective data length and the length of the complete message block (whose structure is discussed further on). The ratio works out at a maximum of 57% for the CAN bus. Given the short data length, 57% is a relatively high value.

The CAN protocol does not contain specifications for the bus coupling hardware or the wiring between the modules. Depending on the application, single-wire, two-wire, or fibre-optic links may be used. In most cases, a twisted wire pair is used in combination with bus coupling hardware derived from the RS-485 standard.

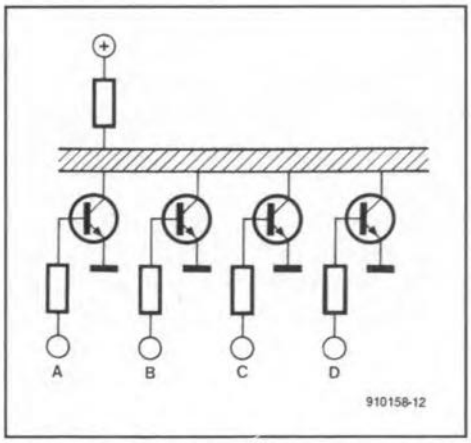


Fig. 2. Open-collector bus drivers enable the required bit levels to be provided in a simple manner.

Data integrity is of the utmost importance in automotive applications. Powerful measures for error detection, signalling and self-checking are implemented in every CAN node. Only think of what would happen if a glitch in the system would switch the gearbox to reverse with the car going at a comfortable 70 mph!

Protective measures like 15-bit CRC (cyclic redundancy check), bit stuffing and MSF (message frame check) are implemented in the CAN protocol, which achieves a total residual error probability smaller than 3×10^{5} for undetected corrupted messages. This means that a maximum of one corrupted bit goes by unnoticed in a total of 33,000 bits. The Hamming distance, HD, achieved by the CAN protocol equals HD=6 (the Hamming distance is a measure of system security). The system is capable of detecting, reliably, up to five corrupted bits in a message. When one of the bus units detects an error in a message, it transmits an error frame, which signals all other bus units to discard the corrupted message. This is done to ensure that all units receive the same, uncorrupted, message. The error frame also serves to prompt the originator of the corrupted message to repeat the message.

Frame types

The CAN protocol specifies two types of message frame for the data exchange be-

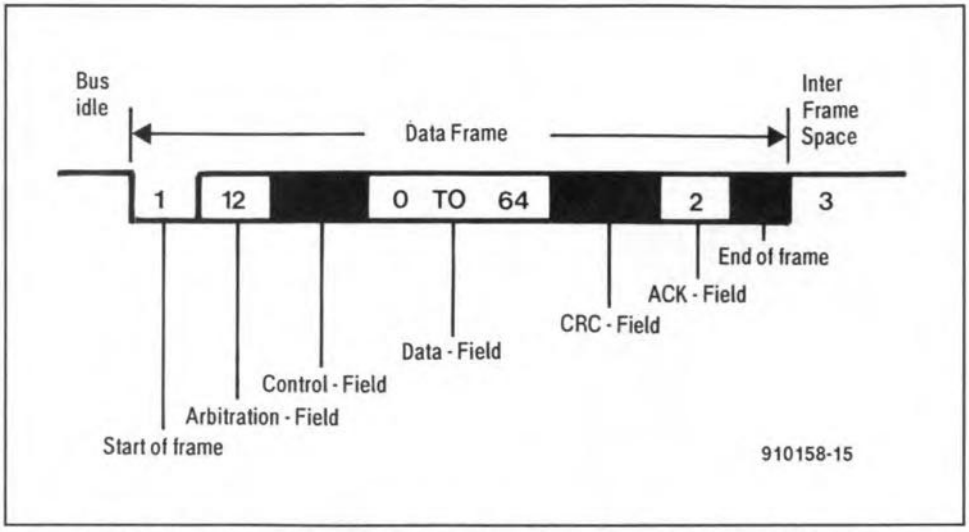


Fig. 3. The CAN protocol defines two types of message frames for the data exchange between modules. The data frame serves to convey the actual data, while the remote frame serves to request data from other modules.

tween CAN nodes. The actual data are conveyed via the 'data frame', while the 'remote frame' serves to interrogate other bus units. A bus unit acting as a receiver for certain data can initiate the transmission of the respective data by its source node by sending a remote frame. The structure of the two frame types is shown in Fig. 3. The start of the frame (type 'data' or 'remote' is marked by the start of frame bit. All bus units are synchronized on the falling (negative) edge of this bit. The subsequent arbitration field contains the previously discussed 11-bit identifier and the RTR bit (remote transmission request). RTR=0 in a data frame, and RTR=1 in a remote frame.

The control field serves to convey the length of the effective data in bytes (data length code, DLC). Only the four lower-order bits are used; the remaining two are reserved for extensions. The control field is ignored in a remote frame, since it does not contain effective data in that case. The actual (effective) data follow the control field (there is no data field in a remote frame), and can be up to eight bytes long.

The CRC field contains the 15-bit CRC checksum and a CRC delimiter, which is a single recessive bit that serves to give the receiver time to process the CRC. The CRC is computed using all previous bits in the message frame. The frame is finished with the acknowledge (ACK) field and the end-of-message field. The ACK field is two bits long, and contains the ACK slot and the ACK delimiter. During the ACK field the transmitting unit sends to recessive bits. All receivers that have received a valid message correctly, report this to the transmitter by sending a dominant bit during the ACK slot. The end of frame field, finally, consists of seven recessive bits.

Data frames and remote frames are separated from preceding frames by a bit field called interframe space, which has a minimum length of three bits.

In addition to the data frame and the remote frame, there are two other frame types, which are not directly related to the transmission of data. A node that requires more processing time can issue an overload frame, which causes other bus units to delay the transmission of the next data frame or remote frame. The function of the fourth frame type, the error frame, was discussed earlier.

CAN on ICs

The availability of inexpensive integrated circuits that implement the full CAN protocol on their own has contributed significantly to the interest in the CAN bus. As this article is written, there are two CAN controllers on the market: the 82526 from Intel, and the PCA82C200 from Philips Components. Both ICs are designed to interface to a microcontroller. Depending on the application, the 82526, which is designated 'full-CAN-controller' is capable of storing and processing between 5 and 18 CAN messages. By contrast, the 82C200 has only two receive buffers and one transmit buffer. The main data of the two ICs are listed in Tables 1 and 2.

The block diagram of the 82C200 is shown in Fig. 4. At the right of the drawing we find the CAN bus connections. RX0 and RX1 are differential inputs for the received data. TX0 and TX1 are transmitter data outputs. Software is used to define TX0 and TX1 either as open-drain, open-source, or complementary (inverting/non-inverting) outputs. The actual interface to the bus, however, requires a further driver circuit — usually some kind of RS-485 circuit.

The microcontroller interface of the 82C200 is shown to the left of the block diagram. Depending on the level applied to the 'mode' input, the controller may be connected directly to an 8051 compatible processor (mode='1'), or a Motorola processor (mode='0'). The XTAL1 and XTAL2 terminals are connected to a quartz crystal or to an external clock source. The typical clock frequency is 16 MHz.

The 82C200 contains a total of 32 registers (status, control and data), which can be accessed by the microcontroller it is linked to. The CAN bit rate (which is not fixed), the mode of the transmitter data outputs, and the interrupt behaviour of the controller are programmed via the status and control registers. To transmit a message, all relevant information in it, i.e., identifier, remote frame bit, data length, and, of course, the effective data, is written into the corresponding registers. When everything is ready to go, the transmission is triggered by setting a certain control bit. Everything else is handled by the controller itself.

By programming the so-called acceptance filter in the 82C200, the controller can be made to respond to messages with certain identifiers only. This allows all other messages, i.e., the ones which are irrelevant for the particular node, to be filtered out.

Only those messages that pass through the acceptance filter are stored in one of the two receive buffers. On reception of a message, a status bit is set, and an interrupt is generated (if so programmed). Next, the microprocessor can read the received data.

Tea leaves

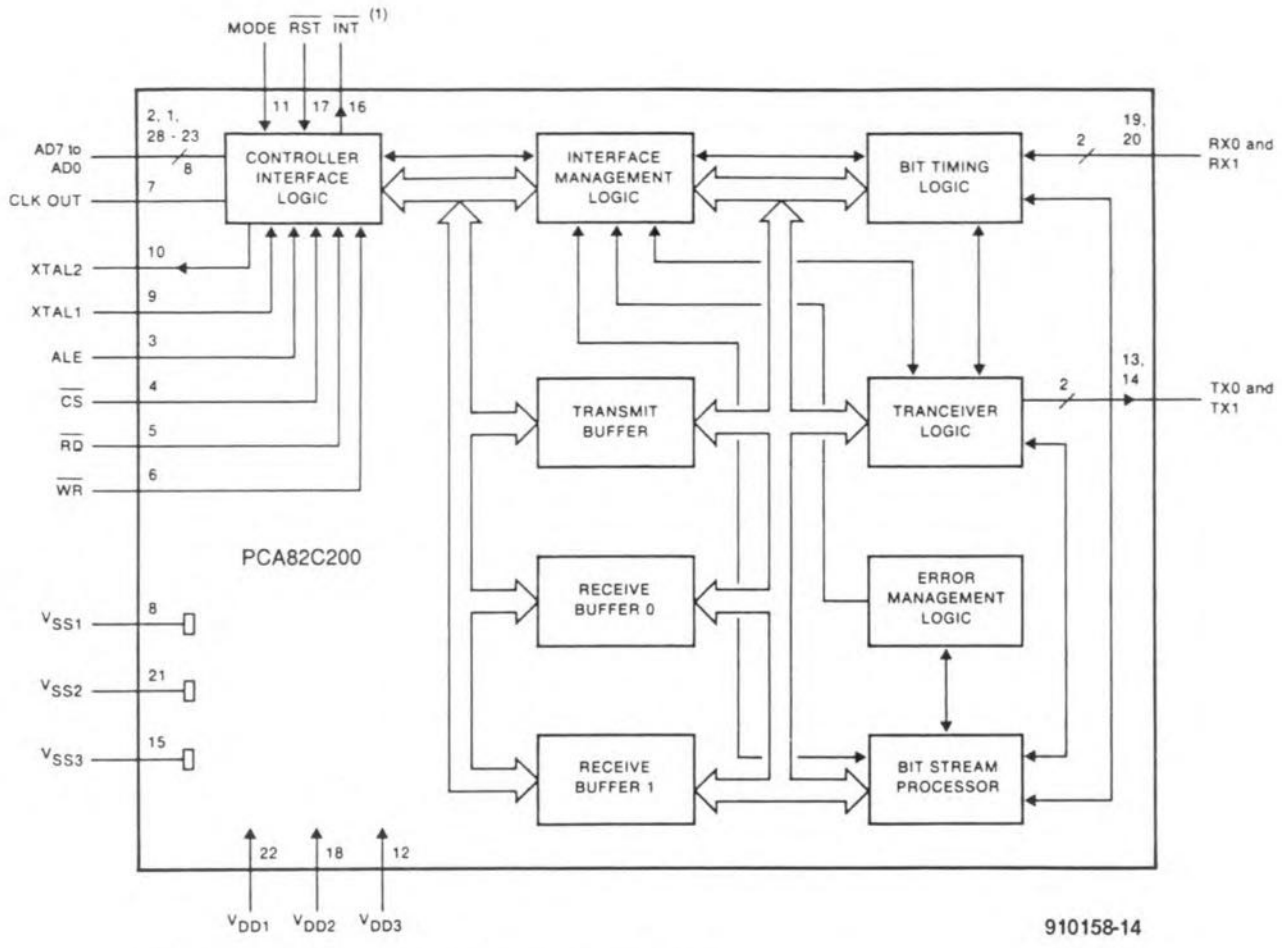
At the present level of CAN technology, each node requires a microcontroller with

Table 1.
Intel 82526 CAN bus controller

- 2,032 different identifiers
- data rate up to 1 Mbit s^{-1}
- Programmable-mode transmit data outputs
- Supply current 22 mA typ.
- Supply voltage 5 V
- Simple interface to 8051-family microcontrollers
- 44-pin PLCC package
- two 8-bit ports

Table 2.
Philips Components 82C200 CAN bus controller

- 2,032 different identifiers
- data rate up to 1 Mbit s^{-1}
- Programmable-mode transmit data outputs
- Supply current 15 mA typ.
- Supply voltage 5 V
- Simple interface to Intel and Motorola processors
- DIL-28 or SO28 package



(1) During 'sleep mode' this pin functions as an input.

Fig. 4. Block diagram of the 82C200 CAN controller (courtesy Philips Components).

a program memory, a CAN controller and a bus driver. An intelligent sensor or actuator, however, in addition requires an A-to-D or D-to-A converter, respectively. Philips have announced a new CAN microcontroller, the 80C592, that should reduce the CAN node hardware layout considerably. Apart from the (application-dependent) bus drivers, this IC contains just about everything required to build an extremely compact CAN node interface. On board the 80C592 are

- an 8-channel 10-bit A-to-D converter;
- a reference voltage source;
- two PWM outputs;
- a complete CAN controller;
- a serial interface (RS232);
- 512 bytes of RAM;
- three 16-bit timers/counters;
- five bidirectional 8-bit ports;
- a watchdog;
- optionally: 16 Kbyte of ROM or EPROM.

This controller allows car manufacturers to realize compact, reliable and inexpensive CAN nodes using a minimum amount of hardware.

Conclusion

The CAN bus is remarkable for its simplicity, reliability and high error immunity. CAN is supported by 'big names' in the car industry, automotive electronics industry and electronics industry: BMW, Daimler Benz, Bosch, Philips Components and Intel. The prospects of widespread use of CAN are very good, not only in the car industry, but also in the measurement and control field. ■

Sources / for further reading:

1 CAN specification Version 1.2, Phillips Components (Division Hamburg, Germany *) September 1990.
2. PCA82C200 Stand-alone CAN controller. Philips Components Doc. no. PS 025.
3. CAN Features and Product Details. Philips Components Doc. no. PS 025.
4. 83C952/80C952/97C952 Target Device Specification 1990 ver. 2.0. Philips Components, August 1990.
5. 82526 Control Area Network Chip Architectural Overview, Intel Corp., January 1988.

* Philips Components, Division of Philips GmbH, Burchhardstrasse 19, 2000 Hamburg 1, Germany. Telephone: +49 40 3296-683.

DESIGN IDEAS

The contents of this article are based solely on information supplied by the author and do not imply practical experience by *Elektor Electronics*

REPLACE YOUR PAGING SYSTEM WITH A HIGH POWERED INTERCOM

By Charles Kitchin (Analog Devices Inc., USA)

A cursory look through an electronics supplier's catalog quickly reveals that, although there are many commercially available paging systems, high power paging systems which also function as intercoms are virtually non existent. Businesses, factories, noisy industrial environments, and summer camps are just a few examples of where just such a system is needed. The ability to page over a wide area, using a large number of remote speakers, while also having the ability to listen to any one (or all) of the areas covered by these speakers, makes this type of system extremely useful.

UNLIKE the common paging system, an intercom provides two-way communications — through its master station it can both 'talk' and 'listen' to individual remote stations or zones of stations. The master can keep in touch with many different work stations widely isolated from one another, thus allowing centralized control and communication over large areas. This can be more than simply a matter of convenience. Since the master station can be readily called in an emergency, lives may be saved.

In the 'talk' mode, an intercom provides the usual paging function. In the 'listen' mode, it can monitor any or all of the stations. With a multi-station intercom system, normal standby mode has the master station (or office) listening to all the stations, any of which can then call the office individually if necessary. Once a remote station has alerted the master station (by yelling at the loudspeaker), the master can switch over and communicate with that one station alone.

With any intercom system, special attention is needed to ensure that the system can adequately monitor the remote stations under conditions of strong electrical noise. In general, the larger the total number of stations in the system and the greater their distance from the master station, the weaker the signal level and the greater the difficulty in discerning a signal out of the background noise. It is usually necessary to use shielded interconnect wiring between stations and to employ an instrumentation amplifier in the listen circuitry of the master station to cancel out as much noise as possible.

Equally important is the type of public address speakers used. The physical size of the speaker horn directly affects the sensitivity of the system: the larger the horn, the greater the speaker output both as a speaker and when used as a microphone. Public address speakers with 12" diameter or larger horns are well suited for intercom work; smaller speakers, such as the common 5" horn variety work well as paging speakers but are generally poor when used as microphones in the listen mode. The 12" speakers, with their larger horns, provide a great deal of acoustical gain when used as microphones. Note that, regardless of type, the metal frames of the speakers need to be grounded to minimize noise pickup.

Circuit operation

Figure 1 is a schematic of the main portion of a practical high powered intercom system. This particular intercom has survived over three years use, controlling the operations of a 200-acre summer camp. It still functions perfectly despite being operated 18 hours a day during periods of blistering heat and occasional thunder and lightning storms. Note that, unlike some intercoms, no power or electronic circuitry is required to operate the remote units, they are simply public address horn loudspeakers which function both as speaker and microphone.

The system has four main subsections: the 'listen' section for monitoring the remote stations; the 'talk' section for public address to page through all the remotes, or to talk to them individually. A third subsection functions to select, via relays and switches, which speakers will be connected to the system at any given time. Finally, the power supply section supplies the correct voltages to power the various active devices.

'Listen' or monitoring section

The 'listen' section consists of only two amplifiers: an AD524 instrumentation amplifier (IA) and a 'bullet-proof' 10-watt power opamp, the LM675. The AD524 IA cancels any signals which are common-mode (i.e., the same on both speaker wires), yet amplifies signals which are differential (i.e., not the same on both speaker wires). Since noise is random, it is mostly common mode and will be cancelled; the signal, however, is applied across the wires (differentially) and will be amplified. Since the common mode rejection of this amplifier is around 80 dB, the noise (theoretically) should be reduced 10,000 times. In reality, though, not all noise is common-mode, yet the improvement in signal to noise is still dramatic. Note that grounding either of the speaker lines (not the shield but the lines) removes all common-mode cancellation. Therefore, care should be taken when adding new speakers and lines that they be connected properly. The AD524 has two resistors between each of its inputs and ground, which provide a DC ground return in the event that all speaker switches are shut off. The two capacitors connected in

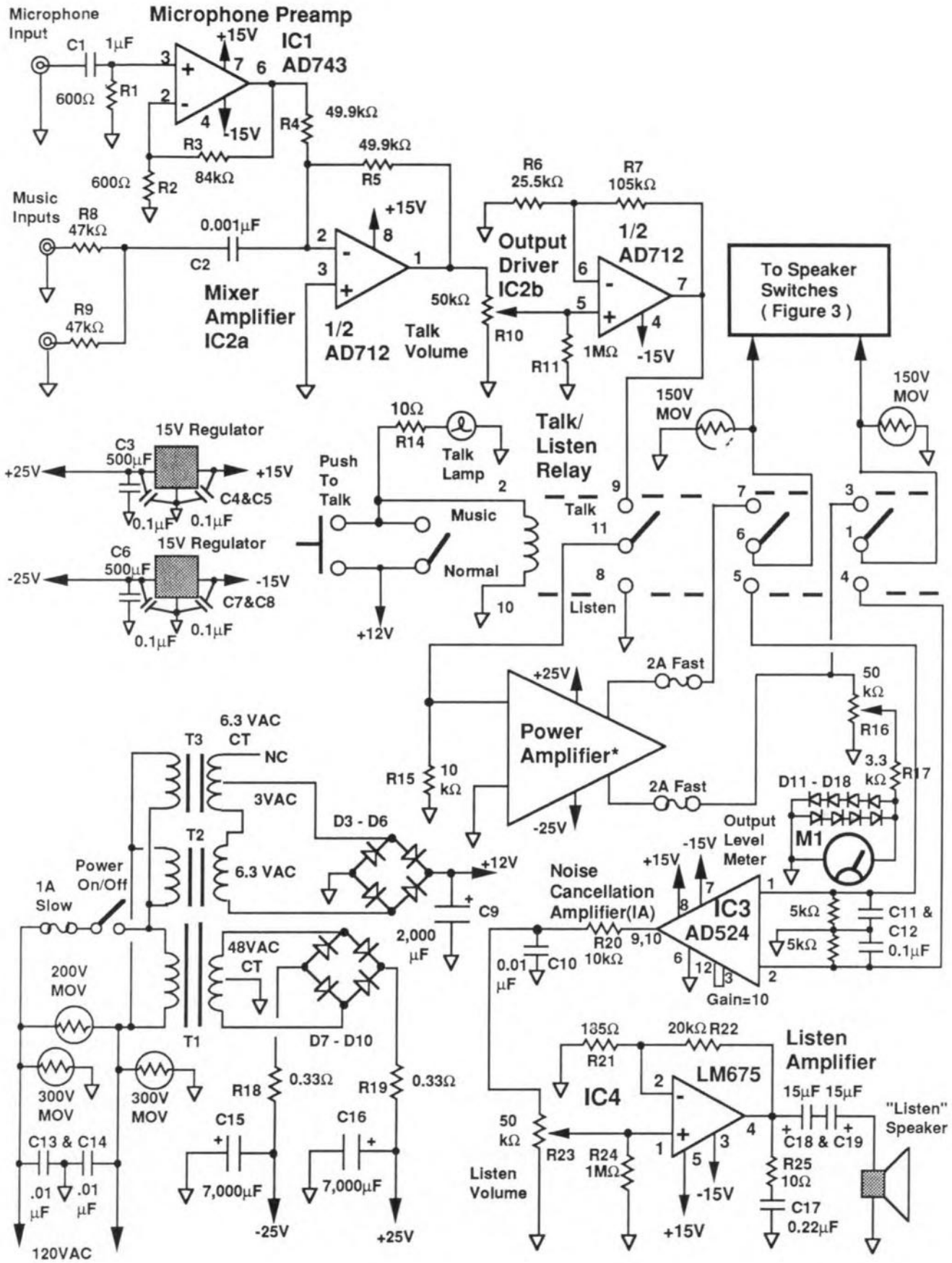


Fig. 1. Intercom main schematic diagram. When using a power amplifier with a single-ended output (such as the simple 20-watt amplifier), ground pin 7 of the listen/talk key.

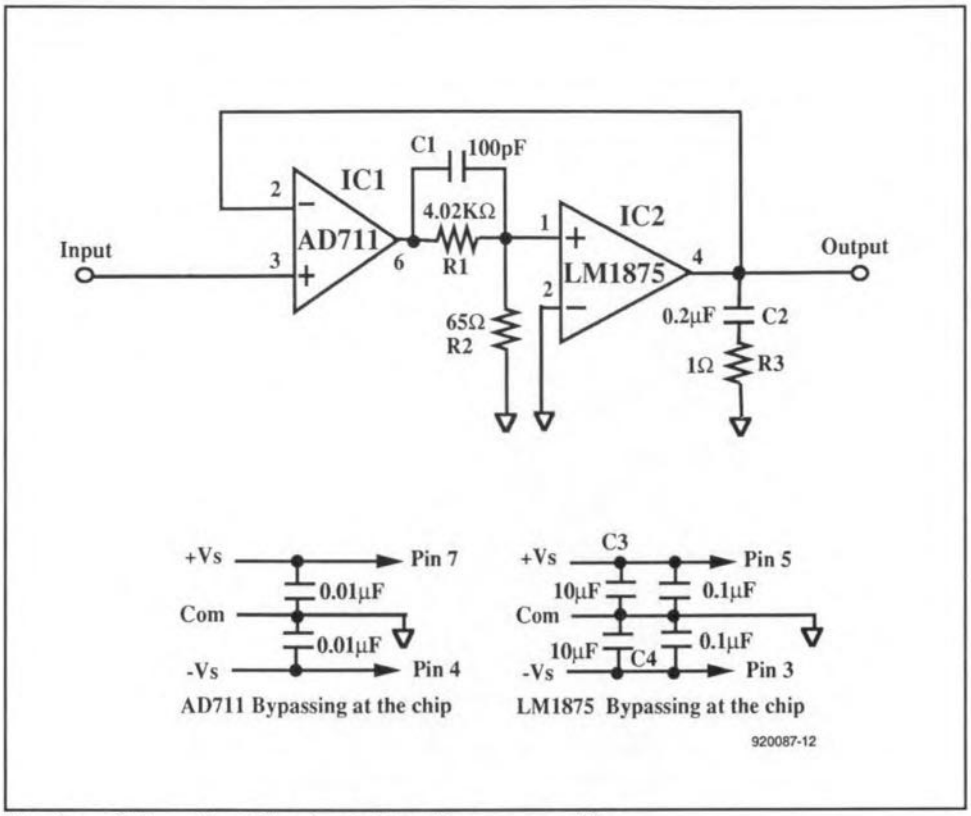


Fig. 2a. Schematic of the simple 20-watt power amplifier.

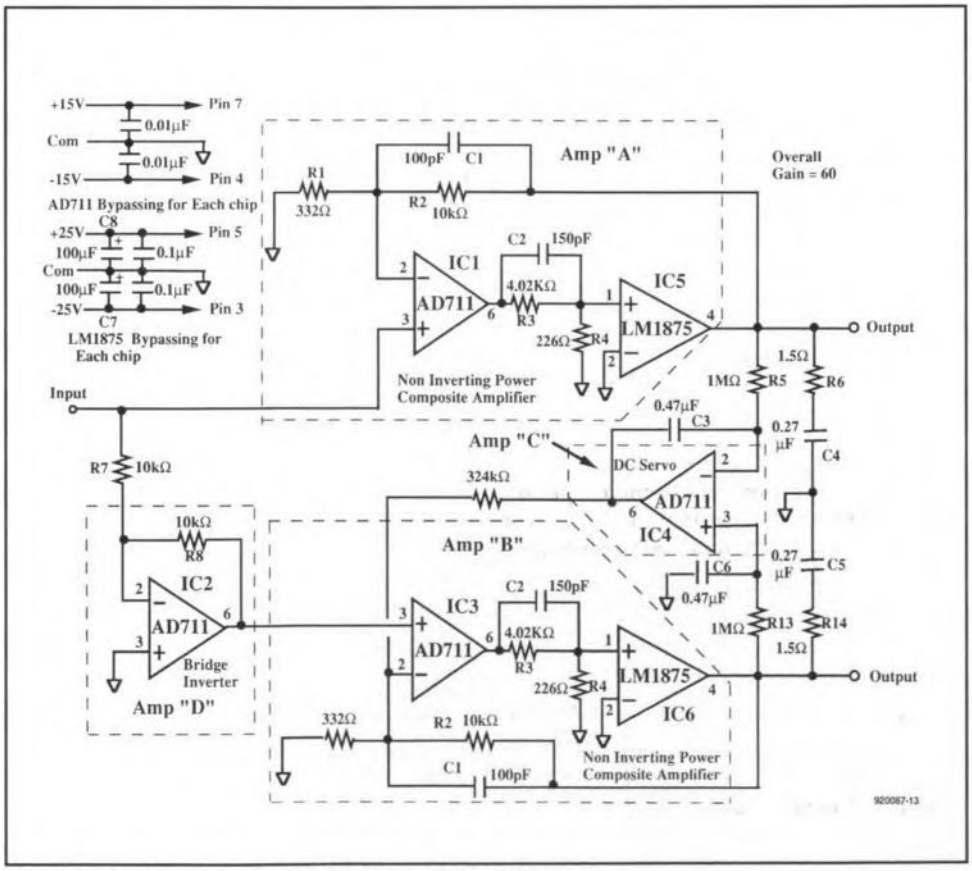


Fig. 2b. Schematic of the 35-watt power amplifier.

parallel with the resistors serve to roll-off some of the high frequency noise and also make the system far less susceptible to radio frequency (RF) interference. The low pass filter at the output of the AD524 serves the same purpose.

The output of the in-amp connects to a 'listen' volume control and from there to an LM675 power opamp. The output of the LM675 connects through a capacitor to a small (4") 'listen' speaker. The LM675 has no extra protection, other than through its supplies, since it is widely considered to be a 'burn-out-proof' amplifier.

The 'talk' or paging section

In the 'talk' section, IC1, an AD743 low noise opamp operating at a gain of 140, serves as the microphone preamplifier. This raises the 5-10 mV microphone output level to approximately 1 V. Mixer amplifier IC2a allows either the amplified microphone output or a high level (0.5 V to 1 V) music input to be broadcast over the system. Output driver amplifier IC2b provides additional gain so that there is ample voltage to drive the power amplifier to its full output level, if desired. Note that all three of these operational amplifiers are used **only** for the paging or 'Talk' function.

The power amplifier

In this design, the power amplifier, which drives the intercom speakers located throughout the system, may be any physically small amplifier capable of delivering 20 watts or more. One alternative to building the power amplifier would be to use a 40-watt VMOS power module. Using the module will greatly simplify construction, but will add about $50.00 to the total circuit cost. Two 'home brew' power amplifiers will be discussed next.

The performance of a monolithic IC power amplifier may be greatly improved by placing it within the feedback loop of an operational amplifier (opamp). This composite amplifier will then have both the low distortion, low offset performance of the precision op-amp and the high current driving capability of the IC power amplifier.

The simple composite amplifier circuit of Fig. 2a delivers 20 watts r.m.s. into an 8-Ω load with a total harmonic distortion (THD) of less than 0.003% and a maximum offset voltage of 1 mV or less. In this circuit, an LM1875 power opamp is connected inside the feedback loop of an AD711 precision BiFET.

Since they are operating within the same loop, a phase lead network, consisting of capacitor C1 and resistors R3 and R4, provides the necessary compensation to stabilize the response of the AD711 and the LM1875.

The 1-Ω, 0.2-µF *R-C* damper network shown between the LM1875's output and ground is necessary if the amplifier is driving an inductive load such as a loudspeaker. For simple resistive loads, the network may be omitted.

Note that if a power amplifier with a single-ended output is used (in this case either the simple 20-watt amp or the commercial VMOS module), pin 7 of the talk/listen relay should be grounded and only one output fuse and fuse holder are needed.

A second circuit, that of Fig. 2b, operates at an overall gain of 60 and provides 35 watts r.m.s.into 8 Ω with less than 0.0035% THD at 1 kHz. The circuit consists of two non-inverting composite amplifiers, 'A' and 'B', in a bridge or differential output connection. Amplifier 'C' is a d.c. servo amplifier that nulls-out any d.c. voltage appearing across the load by making the d.c. offset of the two amplifiers equal.

Amplifier 'D' inverts the input signal 180 times so that the output of amplifier 'B' is non-inverting with respect to the circuit's input. The low input impedance of a high gain inverting composite amplifier makes it

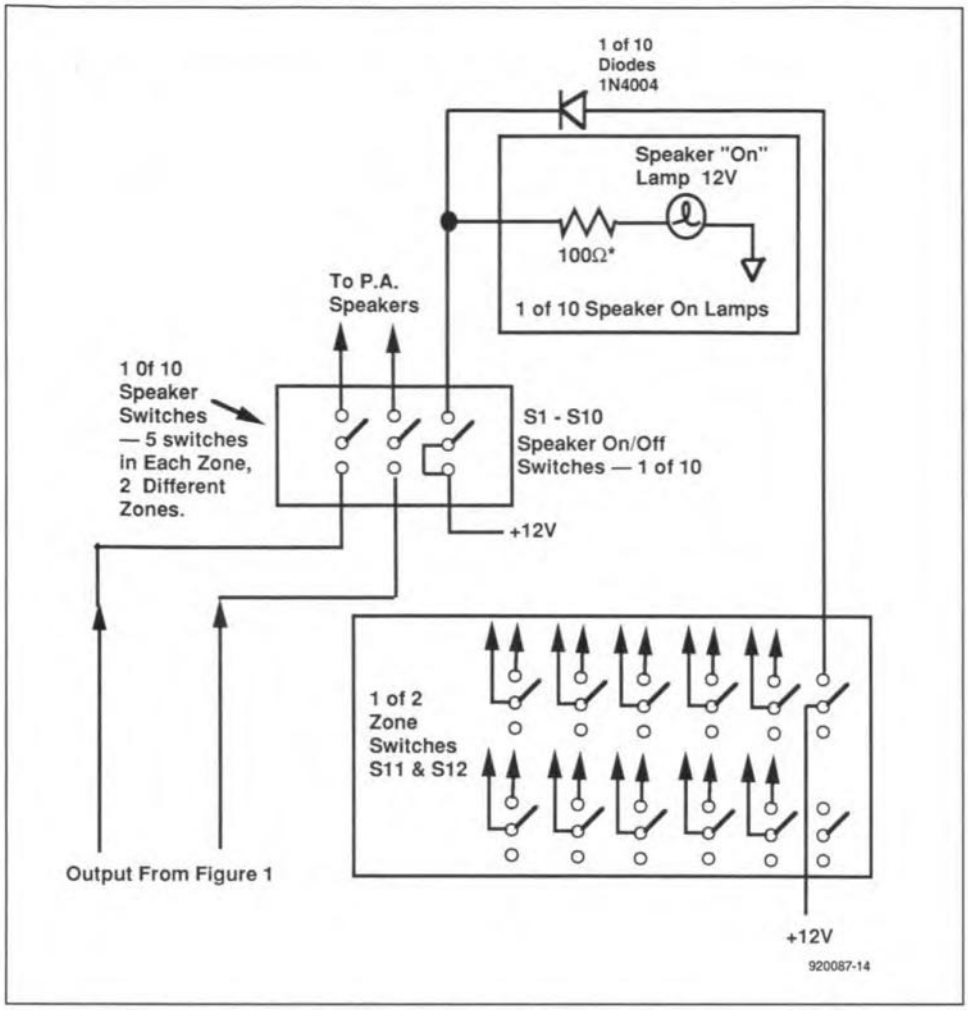


Fig. 3. Speaker and zone switch diagram. The 100-Ω resistor in series with the speaker 'on' lamp reduces the operating voltage to about 6 V, which increases the life span of the lamp 8,000 times. The zone switch contacts are connected in parallel with the speaker switch contacts in each zone. Since there are two speaker switching poles in each speaker switch, switching all five speakers in each zone requires ten poles as shown. One of the two remaining poles is used to switch on all the speaker lamps in each zone.

difficult to drive. This is why two non-inverting composites were used, with one of them driven with a simple op-amp inverter.

An analog VU meter monitors the output level delivered by the power amplifier. A potentiometer located on the back top panel of the intercom sets the meter sensitivity. Eight diodes and one resistor protect the meter from overloads and from the power-down surge of the power amplifier.

'Talk/Listen' function selection

As shown in the schematic of Fig. 1, a 12-V relay switches the intercom from its normal 'listen' function to its 'talk' mode. Note that contacts 8, 11 and 9 select whether or not the input to the power amplifier is to be driven or grounded. Contacts 5, 6, 7, 4, 1 and 3 switch the speakers from the input of the 'listen' section (the IA) to the output of the 'talk' section (the power amplifier). The relay allows two switches to be used: a 'push to talk' and a 'music normal'. Of course, both switches perform exactly the same function but one of them is a momentary contact, while the other is a normal toggle switch. Apart from the convenience of allowing music to be played, having two switches which serve the same function greatly increases system reliability. The switches are extensively protected by MOVs (metal oxide varistors).

Remote station speaker switches

Figure 3 shows how the remote speaker switches are wired. Note that the contacts of the zone switches are wired in parallel with the contacts of the individual speaker switches. The zone switches are highly reliable 12-pole relay switches whose construction is similar to that of a telephone lever switch.

Power supply section

The final section is the power supply. To (help) protect against lightning, the a.c. power line is both fuse (1 Amp slow) and MOV protected. Two power transformers are used: a multi-winding transformer and one with a single winding. A 48-V center-tapped winding on the multi-winding transformer connects to a large (10-A/1000-V) bridge rectifier. The + and – outputs of the bridge, which here is functioning as two full wave rectifiers, are applied to filter capacitors through small series resistors (these resistors limit the initial turn-on current through the capacitors and thus protect the bridge rectifier).

The ±25-V outputs power the power amplifier. Each 25-V power supply also has its own 15-V supply system consisting of a series 15-V regulator. The ±15-V outputs power the opamps, the in-amp, the LM675 listen amplifier, and the opamps in the composite power amplifier.

A second bridge rectifier (this time actually operating as a bridge) is fed by two series-connected 6.3-V filament transformers (only one half of the second transformer is used). Their 9-V a.c. output feeds a second bridge rectifier whose output is filtered by a 2,000 µF capacitor. Because its value is substantially less than that of the main filter capacitors, there is no need for a surge protection resistor. The 12-V output powers all the speaker line lamps and the 12-V talk/listen relay.

Intercom operation

This intercom system has been specifically designed to be as 'fail safe' as possible. The front panel switching uses standard toggle switches rather than the usual (and unreliable) ganged push button switches. The system is divided into two different 'zones'. This was done for two reasons: two zones allow paging half the stations rather than the entire system at one time. Also, the cost and complexity of an 'all speakers' on/off switch was prohibitive. Note that, in all cases, indicator lamps show which speakers are being listened to (or being talked to).

Figure 4 shows the location and function of the intercom's controls. On the top panel there are two knobs, an output meter, and the main power switch. The left control sets the 'listen' volume; this should be set at a comfortable listening level. When different speakers are selected, this control will need to be moved up or down somewhat to maintain the same volume. Note that, unlike the previous system, the listen control does not affect the 'talk' volume in any way.

The knob to the right of the 'listen' control is the 'talk' volume control. This sets the output level applied to the speakers when the push-to-talk button is pushed — the output level meter to the right of the control indicates this level. When 'talking', the talk level control should be set about mid-position, and the operator of the intercom should watch the output level meter when speaking. The operator should adjust his (or her) distance from the microphone (or talk softer or louder) to keep the average output level about mid-scale on the meter. Note that if the level is too high (i.e., the meter reading is mostly in the red zone on the right side of the meter) the speaker volume will be too loud and probably will be distorted as well. Speaking too softly (very little or no indication on the meter) means that your transmission will not be heard. The power on/off switch turns on or shuts off all power to the intercom.

Remote station selection

The next area to explain concerns the switches and lights located on the sloping front panel. As Fig. 3 shows, in this system, there

Fig. 4. Intercom front panel controls.

are 10 speaker switches numbered 1 to 10, two 'zone' switches labeled 'zone A' and 'zone B', a push to talk switch, and a normal/music switch. There are also 10 speaker indicator lights and one large, red "talk" light.

Each speaker switch controls one speaker line which may have one, or several, speakers connected to it. The speaker indicator lights show which speaker lines have been switched on. Note that there are five switches on the top row (switch numbers 1 through 5) and another five on the bottom row (switches 6 through 10). Switching on zone switch 'A' is exactly the same as turning on speaker line switches 1 through 5; likewise, switching on zone switch 'B' is exactly the same as turning on speaker line switches 6 through 10. Switching on both zone switches will turn on all the speaker switches in the system.

A nice feature of this system is that when a zone switch is turned on, all the speaker indicator lights in that zone will go on as well, indicating that it has switched on these speakers. Note that, because they switch on the same speakers, the zone switches may be used if one or more of the speaker line switches fails. Or, if 1 of the zone switches fails to work, the five speaker line switches can be turned on simultaneously to perform the same function.

Through the use of a relay, the push to talk switch 'rewires' or changes the intercom from a listening station to a high power public address (PA) system. The red talk light indicates that you are now paging one or more speakers at a time. Just as with listening, the speaker line switches (and zone switches) select which speakers have been selected. The normal/music switch is electrically identical to the push to talk switch except that it is the type of switch that stays on or off — this allows you to play music over the intercom (you could sit there holding your finger on the push to talk switch, but most people have better things to do with their time).

Again, if the push to talk switch fails, the normal music switch may be used in its place until repairs are made.

Note that each speaker is (and must be) equipped with a '25-volt' line transformer; this increases the speaker's 8-Ω impedance to around 159 Ω (depending on which transformer tap is used). Note, however, that **if even one speaker is connected without a transformer, the whole system will fail to work** (because almost all the power will go into that one 8-Ω speaker).

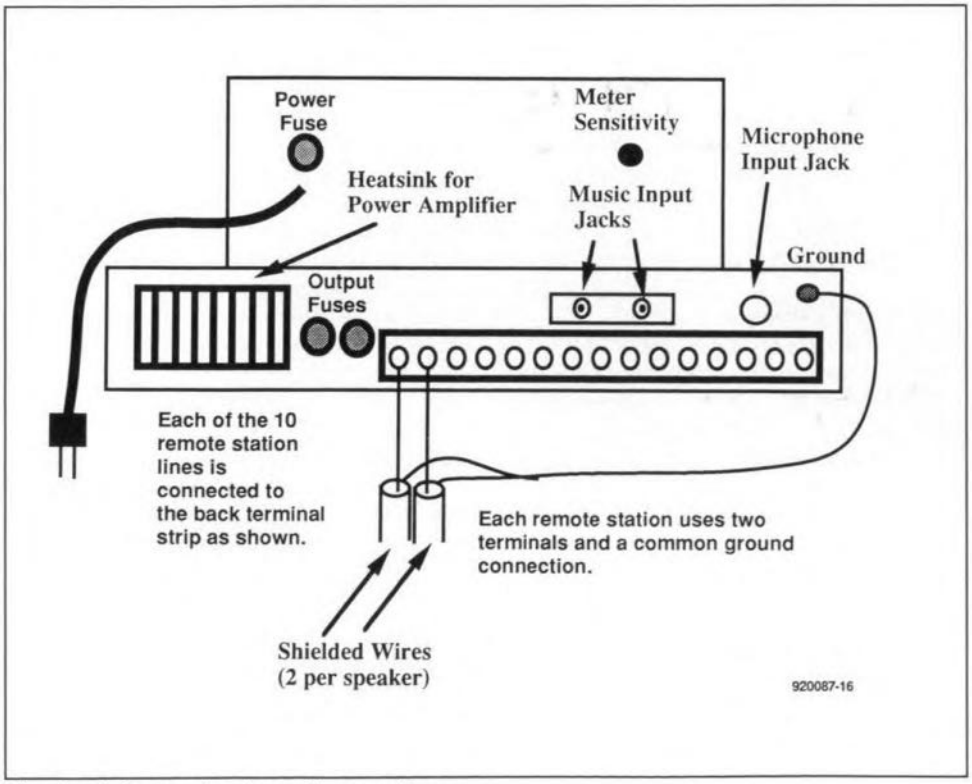


Fig. 5. Intercom back panel connections.

On the back panel

Figure 5 shows the recommended back panel connections to the intercom. Note that shielded wire is recommended for connecting the remote speakers to the master station; the shielding helps to reduce hum and noise when the intercom is used in the 'listen' mode. ■

AN ANTENNA EVALUATION AND SPARE HF TRANSMITTER

This transmitter was designed to provide a frequency-stable, near-fool-proof, RF power source for use in the initial design of new types of comparatively narrow-band compacted resonant antennas, such as small tuned transmitting loops.

By Richard Q. Marris, G2BZQ

A secondary, and important, consideration was that it could be used, as necessary, as a spare transmitter and for holiday use, all of which would automatically follow if the primary design requirements were met.

The target specification

The requirements the transmitter would have to meet are:
(1) Utmost trouble-free reliability, and, in the unlikely event of trouble, this should be correctable in a minute or so.
(2) Absolute frequency stability.
(3) Power capability of up to 15 watts input to the power amplifier stage.
(4) The ability to cope with abuse, in the event of high SWRs often met in the early design stages of small tuned loop antennas, or other experimental designs.
(5) A highly frequency-stable 'on the air' transmitter as a spare, and for possible holiday use.
(6) Construction such that it can be heavily modified for other applications, at a future date.

Design philosophy

Some eyebrows may be raised by the use of valves. However, the very simple reason for their being used here is that they were the best for the job in hand. When the transistor was first introduced, it opened the way to a new era in transmitter circuitry. The author happily went along with this, and has used transistors extensively. However, the valve has not been forgotten, and many hybrid (i.e., transistor-valve) and all-valve circuits have been built depending on the need. After all, valves are still plentiful, relatively inexpensive, and still manufactured. So, why subscribe to the apparent present-day mythology that the use of semiconductors is mandatory? These days, a so-called 'simple' transmitter design with 5 or so watts of output power may well use between 50 and 100 components, excluding power supply. Submit its power amplifier stage to a very high SWR, and the odds are pretty high that it will be damaged, with the tedious job of faultfinding, and extracting and replacing a semiconductor. This kind of work is complicated further by the fact that everything is crammed into a small space on a printed circuit board.

In the present transmitter design, a small number of components is used, and the power amplifier will withstand overloading and other abuse, e.g, a high antenna SWR (standing-wave ratio). A replacement valve can be plugged in in a minute or so, which is absolutely ideal in the early stages of the design of resonant small loop antennas, etc.

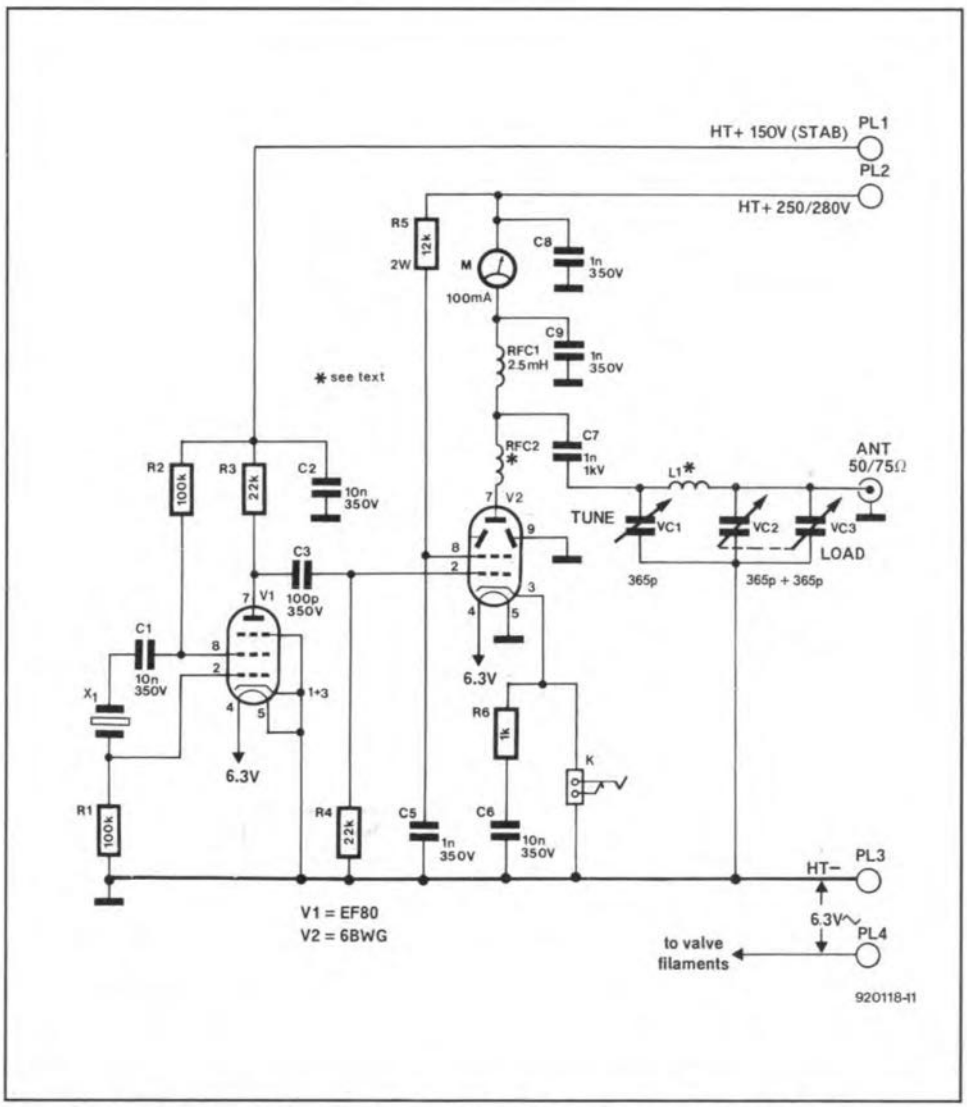


Fig. 1. The test transmitter is a simple two-valve design. A quartz crystal is used to ensure a stable output frequency in the 80-m amateur radio band.

The transmitter circuit

The transmitter circuit consists of a crystal oscillator, a power amplifier and a few associated components — see Fig. 1. The crystal oscillator stage is based on an EF80 high-mu RF pentode, V1, in a simple

Pierce/Colpitts circuit. The 6F19 could be used as an alternative for the EF80. Apart from the well-known quartz frequency stability, an extra refinement is a regulated HT (high tension) of 150 V d.c. applied to the crystal oscillator.

The power amplifier uses a 6BW6 beam pentode, V2. Both valves are well-tried, reliable types. Ceramic or teflon (PTFE) type B9A ('noval') valve bases should be used with V1 and V2. A conventional pi-filter, VC1-VC2-L1, is used to match the PA to 50-75 Ω impedance coaxial feedline to the antenna or ATU (antenna tuning unit). The PA is cathode-keyed with adequate click suppression. The circuit shows a 100-mA milli-ammeter in the anode circuit to facilitate tuning and loading. The meter is also useful for calculating the input power (in watts) by multiplying the anode current with the HT anode voltage.

VC1 and VC2 are good-quality air-spaced receiver type U-frame variable capacitors. VC2 is a 2-gang × 365-pF type, and VC1 a single-gang 365-pF type. All resistors are 0.5-watt rating unless otherwise indicated. All capacitors are 350-V working voltage unless otherwise indicated.

Type FT243 (ex-surplus) plug-in quartz crystals were used in the prototype, with a socket on the front panel for easy frequency change. Other types of crystal could be used, such as HC6/U, HC18/U, HC23/U, etc.

The use of the prototype was restricted to the 3,500 kHz to 3,800 kHz amateur radio section of the 80-m band, using 3.5-MHz band crystals, and L1 is wound for this band. Note that the 80-m band is extended to 4,000 kHz in some countries. However, a simple modification to L1 can make it usable on the 7-MHz (40-m) and 14-MHz (20-m) amateur radio bands. More about this further on.

The voltage requirements of the transmitter are 150 V d.c. (preferably regulated) to V1, and anything between 200 V d.c. and 300 V d.c. for V2. On the prototype, a HT of 270 V is used on V2, which can be loaded to a maximum of 16 watts at this voltage. Normally, however, it is run at a lower power.

Switch S2 (in-built in the AC PSU circuit) is the standby/transmit switch. When S2 is open, the HT to the transmitter is off. When S2 is closed, with the morse key open, the HT is only applied to the crystal oscillator, V1, providing a small non-radiating signal which can be 'frequency-netted' on the receiver. Pressing (closing) the morse key effectively applies HT voltage to V2, thus actuating the power amplifier and transmitter output. The CW (continuous wave or 'morse') signal produced by the transmitter is very clean and frequency stable.

Transmitter construction

The transmitter was built into an existing simple metal box 6½ inch wide, 3¾ inch high and 4 inch deep (approx. 165×95×100 mm). The box size is not at all critical, provided it is not smaller. The box lid is used as the front panel, and fitted with a simple aluminium chassis, as illustrated. The layout of the main components is as shown, and should be adhered to, even if a larger box is used. The top of the box should have ventilation holes drilled into it. The lower rear of the case (just above chassis level) should also have a ventilation slot or holes. This cooling system works like the domestic in-room convector heater. As hot air passes through the top ventilation holes, cold air is sucked into the bottom holes at the bottom rear, thus producing a flow of cold air over the valves.

The resistors and capacitors are readily soldered between the main components' solder tags. Decoupling capacitors should be earthed to the chassis with the shortest leads possible. In practice, this method is more advantageous than a printed circuit board, since the components are well spaced. Clearly, this facilitates quick repairs, as well as drastic modifications, at a later date.

Inductor L1 and choke RFC2 are home constructed. L1 consists of 35 turns of 24SWG (25AWG, approx. 0.6 mm dia.) enamelled copper wire wound on a 1½-inch (38-mm) length of 1-inch (25 mm) diameter plastic tubing, with a spacing of a wire between the turns. The inductor is stood off the chassis, using ¾-inch (approx. 19 mm) long insulated spacers at each end.

RFC2 is a simple anti-parasitic choke, and consists of 7 turns of PVC-covered hook-up wire. It was wound on an old Erie 10-MΩ carbon resistor. A piece of 0.25-inch (6-mm) diameter insulated rod could be used as an alternative. RFC1 is a normal 2.5-mH choke capable of carrying 100 mA.

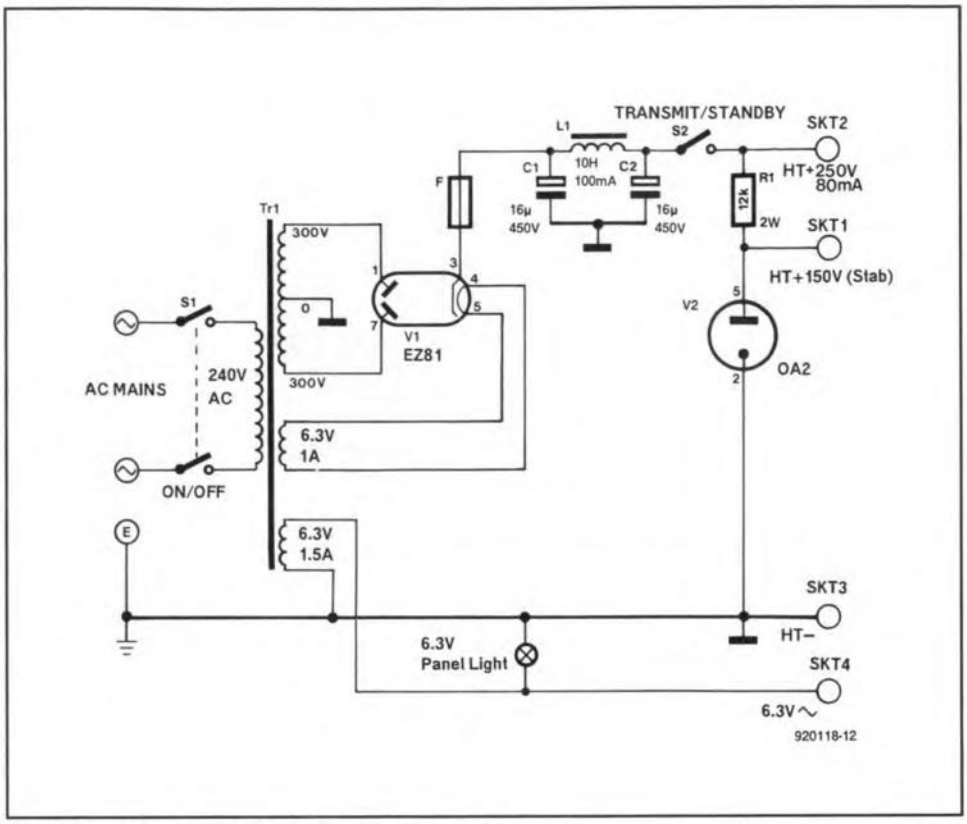


Fig. 2. Circuit diagram of the transmitter power supply.

Although VC1 is specified as a 365-pF single-gang variable capacitor, it was found that this was difficult to find, so one section of a 2-gang × 365 pF was used, with one section not connected.

The jack socket, K, is a 3.5-mm type to match the plug on the author's Junkers morse key. A 6-mm socket could be used to match other types. The coaxial output socket at junction L1-VC2 can be of any style to suit individual needs.

The valve pin numbers shown in the circuit diagram are 'bottom view' numbers, moving clockwise from the gap in the sockets. On most socket types, these numbers are already marked on the base.

The 6.3-V a.c. filament supply is rated at a minimum of 1.5 A.

Power supply unit

The following external voltage supplies are required by the transmitter:

1). HT 150 V at 10 mA, preferably (not essentially) stabilized.
2). HT 270 V at 90 mA minimum.
3). 6.3 V a.c. at 1.5 A minimum.

It is possible that a suitable AC power supply already exists, or can be purchased as a 'surplus' item. The voltage stabilizer, an OA2, and its series resistor, can easily be built into such a unit, as can transmit/standby switch S2.

The circuit diagram of the PSU used by

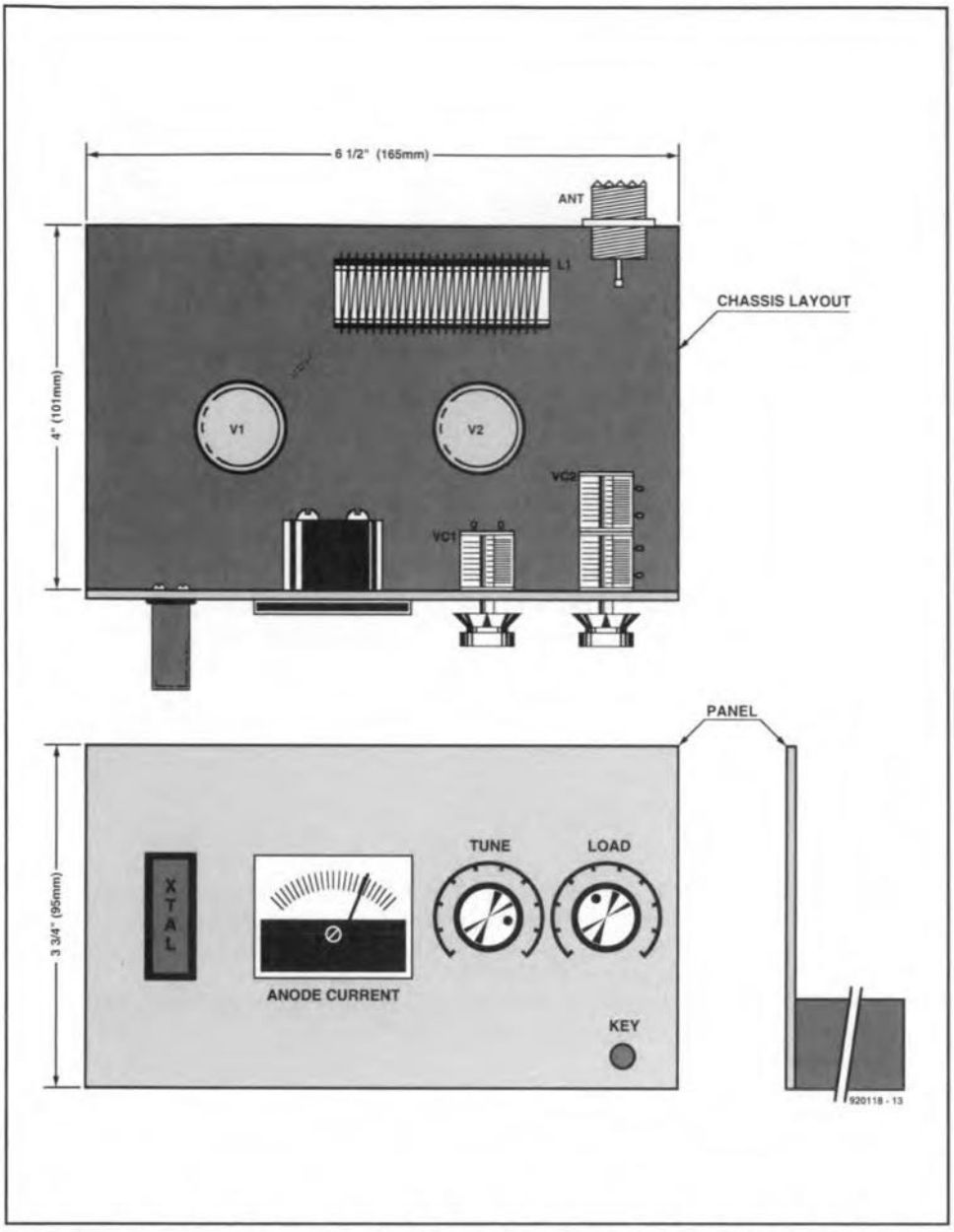


Fig. 3. Suggested component placement on the transmitter chassis and front panel.

the author is given in Fig. 3. It consists essentially of a mains transformer, Tr, a full-wave rectifier (an EZ81 valve), and a smoothing section formed by two 450-V electrolytic capacitors and a 10-H choke. A Type OA2 voltage stabilizer is used to provide the 150 V regulated HT for the crystal oscillator. Stabilization is used here to further improve the frequency stability of the oscillator. Both the EZ81 and the OA2 are fitted in B9A bases. The outputs of the PSU should be terminated with sockets (NOT plugs), that receive plugs terminating a short interconnecting cable from the transmitter. The author's PSU is built into a metal case 8½ inch wide, 4¾ inch high and 6 inch deep (approx. 22×12×15 cm). Again, this size is not mandatory.

Transmitter testing and operation

A 3.5-MHz band crystal is plugged into the front panel crystal socket. A 15-W (minimum) 50-Ω dummy load is connected to the antenna output socket.

Switch S2 is set to the 'standby' position (i.e., 'open'). The mains is switched on, and an initial warm-up period of about 1 minute should be allowed. Check the HT with a suitable voltmeter. With S2 switched on, and the morse key 'open', there will not be an ammeter reading, but is should be possible to receive the crystal oscillator on the receiver.

With both variable capacitors at maximum, close S2 and press the morse key. This will give a meter reading. Very quickly rotate VC1 for a pronounced dip in the anode current. This dip indicates resonance. Rotate VC2 slowly to increase the meter current to about 50 mA, and slightly return VC1, if necessary, to resonance. With a HT of 270 V and an anode current of 50 mA, the input power is about 13.5 W.

The antenna or antenna/ATU combination can now replace the dummy load, and minor adjustments made with VC1/VC2 if necessary. The transmitter is now ready to go on the air. It can be loaded to 60 mA maximum (approx. 15 W). The loading can be reduced as required, e.g., to 40 mA (for approx. 10 W), or 50 mA (for approx. 13.5 W).

Other bands

The transmitter can also be operated on the 7-MHz (40-m) band with either a 3.5-MHz or 7-MHz band crystal, with the size of L1 reduced by removing ⅓ of the turns. Valve V2 then operates as a power amplifier on 7 MHz with a 7-MHz crystal, or as a frequency doubler, with a little lower output, with a 3.5-MHz crystal. In a similar way, by further reduction of the inductance of L1, and using a 7-MHz crystal, the PA will act as a doubler to produce a 14-MHz band signal. Anyone requiring multiband operation could well make L1 a 2-pin plug-in device for easy wavechange.

Conclusion

This two-valve circuit has been designed as a simple, very reliable, near fool-proof, frequency-stable, HF test transmitter. The circuit and component selection (i.e., valves and crystal control) have been dictated solely to meet the target specifications discussed earlier. It performs its job for initial testing of narrowband tuned loop antennas perfectly, and has also proved to be an excellent low-power everyday and spare transmitter.

Finally, as with all AC mains operated equipment, there are high voltages present in the transmitter and PSU circuits. High voltages should always be treated with care and respect, since they may be lethal. ■

SOME SUGGESTED COMPONENT SUPPLIERS

Crystals:
Type FT243 (and others), and holders, from: JAN CRYSTALS, 2341 Crystal Drive, P.O. Box 06017, Fort Myers, FL 33906 - 6017. U.S.A.
All types except FT243 from: Quartz Crystals, P.O. Box 19, Erith, Kent DA8 1LM.

Valves and valve bases:
RST Mail Order Co., Langrex Supplies Ltd., 1 Mayo Road, Croydon, Surrey CR6 2QP.
Colomar (Electronics) Ltd., 170 Goldhawk Road, London W12 8HJ.

Variable capacitors VC1 and VC2:
J. Birkett, 25 The Strait, Lincoln LN2 1JF (can also supply resistors, capacitors and other small components).