ELEKTOR ELECTRONICS

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JULY 1992 UK £2·95

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BUMPER SUMMER ISSUE

With over 50 construction projects

Audio-frequency DAC

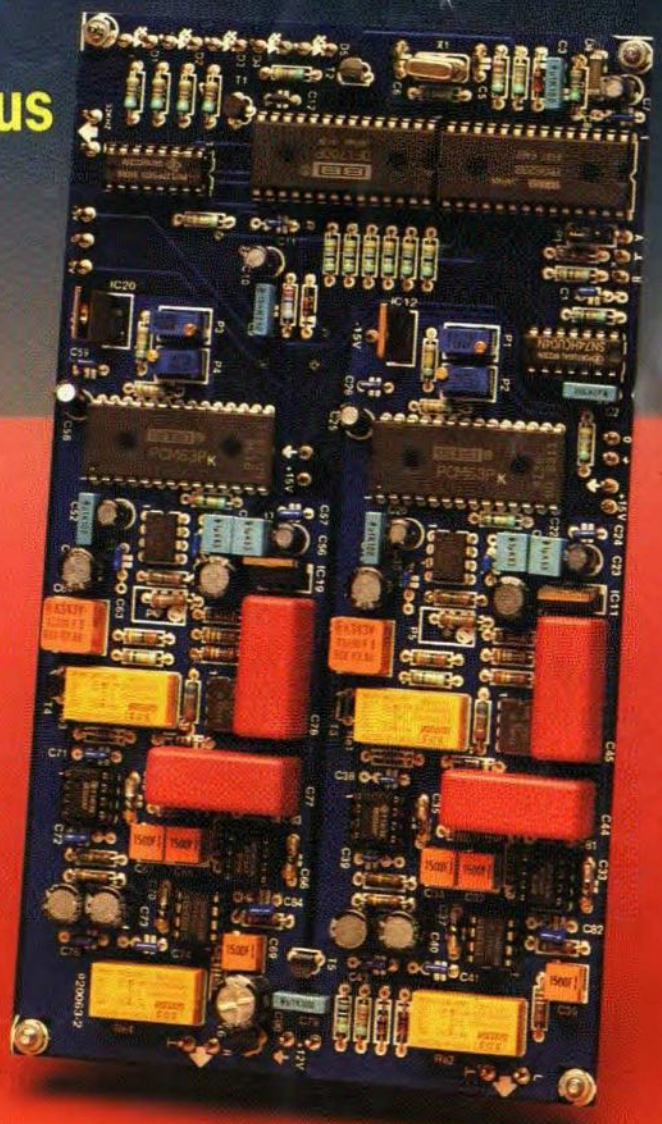
Opto-card for multi-purpose bus

Mark 2 QTC 80+40 loop

Fuzzy logic

Dealing with noise and interference

RS232 tester



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ELEKTOR ELECTRONICS

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July 1992
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- 8051/8032 assembler course Part 6
- The applicable and constructable fictions of electronics
- Flash EPROMs
- CALSOD II: designing loudspeaker boxes by computer
- Current-sense MOSFETs
- EPROM emulator II

Front cover

This month we publish the first part of an a.f. digital-to-analogue converter that can be built into existing equipment or be used as a stand-alone unit. It is eminently suitable for use with the CD player we published earlier this year. Twenty-bit converter ICs, ×8 over-sampling and high-quality analogue stages are used to translate accurately the digital output of CDs, DAT recorders or radio broadcasts into the desired analogue information.

ABC
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OPTO CARD FOR UNIVERSAL PC I/O INTERFACE

Whenever an interface is connected to a circuit with a supply voltage higher than 5 V, there is the risk that an error during experimenting, or a faulty component, will cause serious damage to the computer system. The opto card described here has been designed to afford complete electrical isolation between the computer and the (cruel) outside world, which is the only way to prevent system down time and expensive repairs caused by incompatible signal levels.

Design by J. Ruiters

IN this article we present the second extension card for the Universal I/O Interface For IBM PCs, described in Ref. 1. While the relay card for this bus (Ref. 2) offers electrically isolated outputs, the present opto card is designed to process input signals in the safest possible way. By the way, the multi-purpose Z80 card described elsewhere in this issue may also be used as a controller for the universal bus.

Eight optocouplers

The circuit diagram of the opto card is given in Fig. 1. If you compare it with the circuit diagram of the relay card, you will find quite a few similarities. That is not surprising, because the functions of the two cards are closely related, one being a parallel output device (relay card), the other a parallel input device (opto card). The address decoding logic, for instance, is identical, consisting of a number of gates and a bidirectional buffer. With reference to Fig. 1, we are talking of IC9, IC10 and IC12. How the card is addressed, that is, how it complies with the rules of extension card addressing that apply in the universal bus system, will be reverted to below.

The opto card is actuated when bus signals A0, A1, $\overline{RD}$ and $\overline{ENABLE}$ go logic low. Consequently, bus buffer IC10 is enabled, and data is conveyed towards connector K1, i.e., towards the PC. At the same time, the $\overline{OC}$ input of data latch IC11 is pulled low, which enables the latch outputs. The data on the databus is clocked into the latches on the negative (falling) edge of the $\overline{OC}$ signal. This means that data applied to the optocoupler inputs is captured right at the start of a read cycle of the computer system, which ensures that data is stable on the bus during the actual read operation.

The eightfold optocoupler input circuit is all plain sailing. The only parameters to keep in mind are a couple of maximum specifications. To begin with, the input voltage is limited to 'low voltage' (in most countries, this is defined as 42 V a.c., or 60 V d.c.). This limitation is not caused by the optocouplers, but rather by the printed circuit board and a few other components. When designed to handle the 240 V (110 V) mains voltage at the input, the PCB would have become much larger to meet the relevant safety requirements. A further point to note is the specification of the series resistors with the optocouplers (R2, R4, R6, R8, R10, R12, R14 and R16). The indicated resistors (1 kΩ, 0.25 W) may be used when the input voltage is between 2 V and 15 V d.c. Each optocoupler is protected against reverse voltages by a diode connected in anti-parallel. If voltages greater than 15 V d.c. are applied to the inputs, the

series resistors have to be increased accordingly, or resistors with a higher permissible dissipation must be used. The latter solution is not very elegant because of the larger size and the heat developed. The resistor values are calculated such that the LED current is a few milli-ampères at the given input voltage.

The construction of the opto card is entirely straightforward, and therefore not discussed further.

The bus system

As shown in Fig. 2, the address of any extension card connected to the universal bus system is determined by its position in the chain of extension cards. Unconventionally, DIP switches, jumpers and the like are not used. Apart from the beautifully simple and inexpensive hardware, the advantage of this system is mainly that you can not make address setting errors because there is nothing to set: the card address is determined by its physical position in the system. Note, however, that you must not confuse the bus-IN and bus-OUT connectors. Remember, the incoming A0 signal is inverted on every extension card, and swapped with A1 on the bus-OUT connector. This is done to enable any extension card to be selected when both A0 and A1 are logic low, although the actual address to be supplied by the PC to select a particular card is determined by the number of cards connected ahead of that card.

Those of you who have recalled from the earlier articles that the bus system has only four addresses may be surprised to see eight extension cards in Fig. 2. This is simple to explain. Any bus address can be read from, or written to. In other words, there are four 'read' addresses, and four 'write' addresses, which makes a total of eight. This difference is of no consequence as long as you do not wish to use more than four cards, which can then be chained via linking cables without problems. The difference between reading and writing is not in order until you use more than four cards. Let us assume that you wish to hook up four relay cards and four opto cards. This requires the positions with the same card number, e.g., 1 and 1', to be occupied by one relay card (write only) and one opto card (read only). You can not fit two

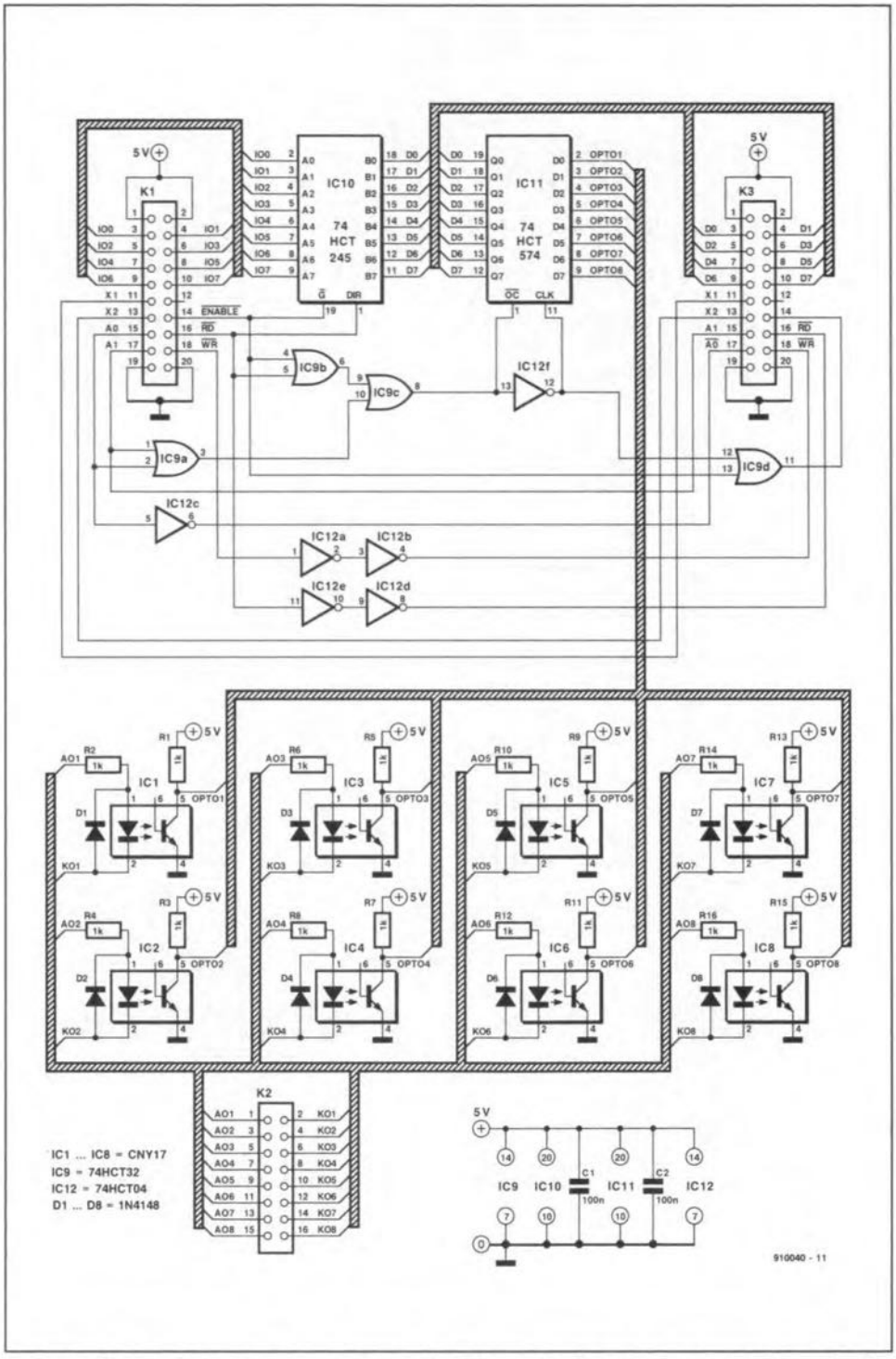


Fig. 1. Eight optocoupler inputs ensure that input signals can not cause damage to the computer.

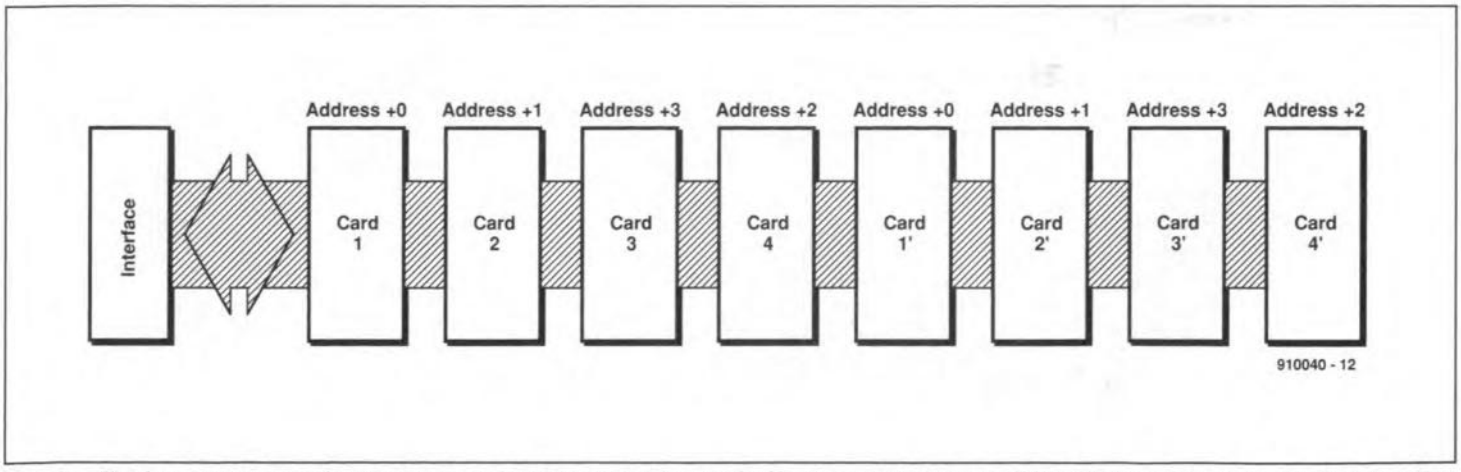


Fig. 2. The bus system can always accommodate four extension cards. However, it is also possible to fit up to four more cards, depending on their type (read or write function).

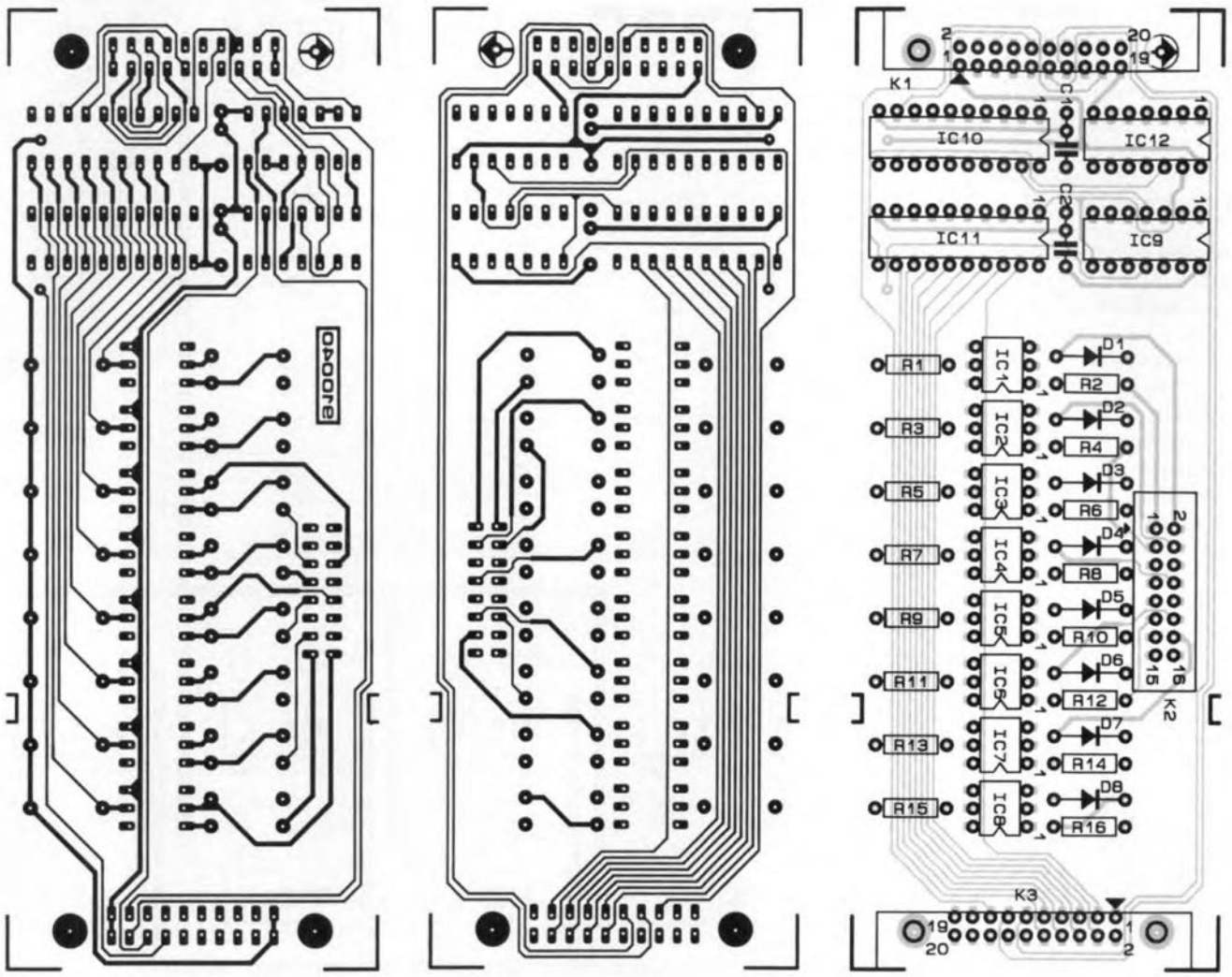


Fig. 3. Track layouts (mirror images of the component side and the solder side) and component mounting plan of the double-sided PCB for the opto interface.

cards with 'write' functions, or two cards with 'read' functions, in a position with the same card number. If you still do so, the computer will forever be unable to 'see' the card with the accented (') number. Fortunately such an 'impossible' connection will not damage the hardware, because the first card addressed in the chain keeps the $\overline{\text{ENABLE}}$ signal for the rest of the chain logic high, whereby all other extension cards are disabled.

A different kettle of fish are extension cards with read *and* write functions (we have not published any of these, but you may have ideas ...). Such cards must always be fitted in one of the first four positions, but as far as possible towards the end of the chain. If a 'read/write' card is fitted in position '1', and three relay cards in positions '2', '3' and '4', it would appear that you can not fit an opto card up to position 2'. That will not work, however, since there is first card 1', but that position is blocked by card 1. The upshot is that first four positions must always be occupied by cards that can only be read from or written to. This leaves the next positions available for cards with the double 'read/write' function.

Summarizing the above:

- the address occupied by the card is determined by its physical position in the chain;
- at every address, a distinction is made between reading and writing;
- if an address is used for writing or reading only, the corresponding accented position may be occupied by a card with the complementary function only.

■

References:

1. "Universal I/O interface for IBM PCs". *Elektor Electronics* May 1991.

2. "Relay card for universal bus". *Elektor Electronics* November 1991.

COMPONENTS LIST

Resistors:

16	1kΩ	R1-R16

Capacitors:

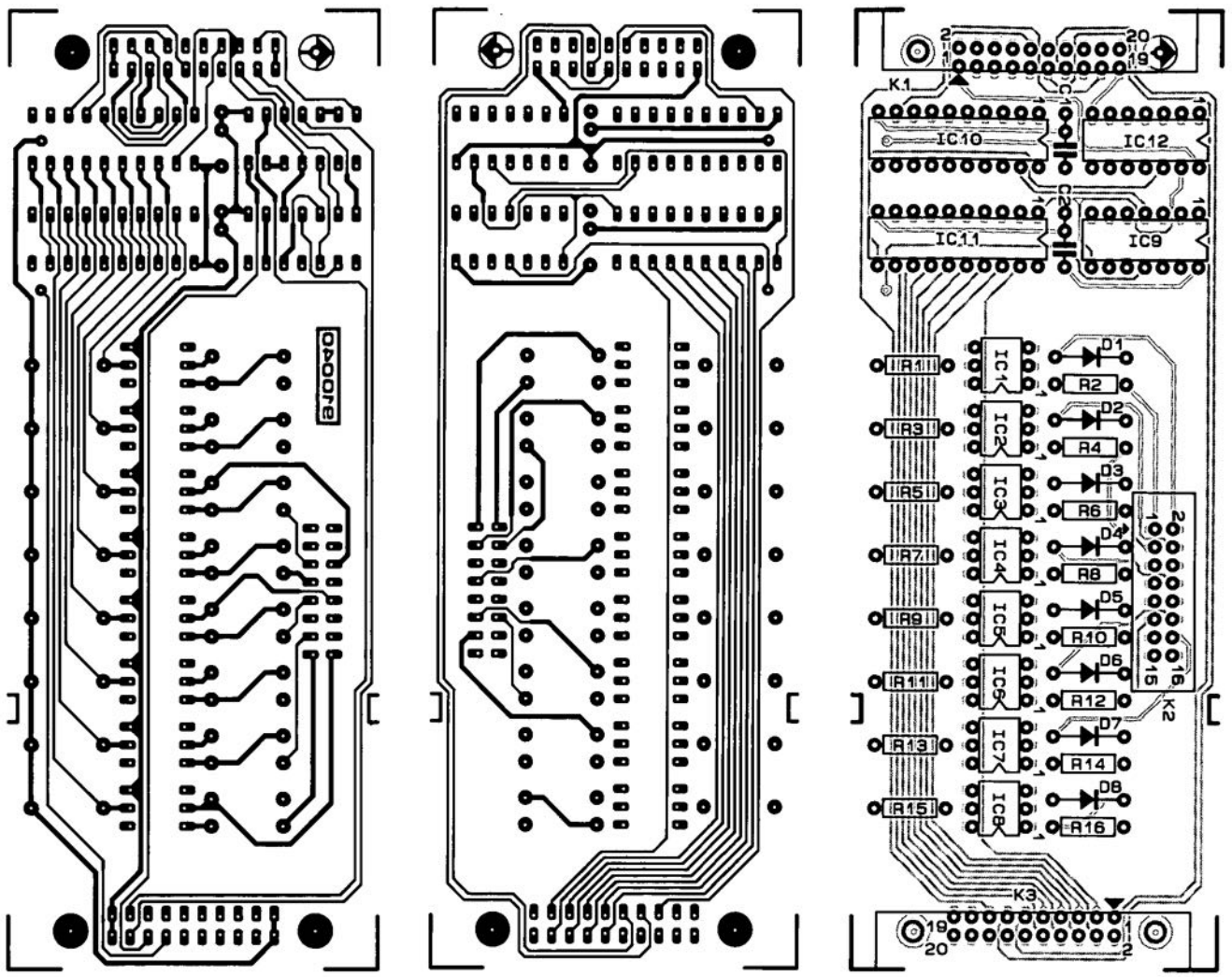
2	100nF	C1;C2

Semiconductors:

8	1N4148	D1-D8
8	CNY17	IC1-IC8
1	74HCT32	IC9
1	74HCT245	IC10
1	74HCT574	IC11
1	74HCT04	IC12

Miscellaneous:

2	20-way header with side latches, angled PCB connections	K1;K3
1	16-way box header	K2
1	Transparent plastic enclosure Type 222 (Heddic)	
1	Printed circuit board	910040



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AUDIO-VIDEO PROCESSOR TYPE AVP300 – PART 3

An ELV design

Synchronization circuit

THE signals in a number of circuits of the processor must be matched to the input signal to prevent a wandering or distorted picture. The circuit responsible for this is the sync(hronization) circuit, whose diagram is shown in Fig. 6.

The sync circuit is based on sync separator IC_{601}. This circuit is fed with the VBS signal via T_{601} and provides three output signals: a sandcastle pulse at pin 7; a square wave at pin 3, whose first transition (leading edge) determines the onset of the horizontal sync pulse; and the vertical sync pulse at pin 10.

The signals at pin 3 and pin 7 are not yet suitable for further use. The sandcastle pulse contains as yet no information on the vertical blanking that is essential for colour demodulator IC_{101} (Fig. 4). Also, a signal that merely determines the onset of the horizontal sync pulse is not enough for further processing of the video signal. To make it into a true sync signal, a fly-back pulse is required. In fact, three pulses are needed: a horizontal and a vertical blanking pulse (12 µs and 1.9 ms respectively) and a horizontal sync pulse of 4.7 µs. These pulses are generated by monostables IC_{602}, IC_{603a} and IC_{603b} respectively.

The horizontal blanking pulse generated by IC_{603a} (pin 6) is superimposed on to the sandcastle pulse via R_{623}. The modified sandcastle pulse has exactly the right shape to ensure correct functioning of IC_{101}.

The reason for IC_{602} being fed directly by the sync separator, whereas both IC_{603a} and IC_{603b} are fed via potential dividers, is that IC_{602} operates from the 12 V supply line and the other two from the 5 V line.

Gate IC_{604b} combines the horizontal and vertical blanking pulses into a composite sync signal. Note that the vertical blanking pulse is applied to the gate via XOR gate IC_{604a}, because this signal is difficult to load owing to the impedance R_{617}-R_{618}.

Audio frequency circuits

To enable background music or a commentary to be added to the audio signal, the processor is equipped with a mixer and tone control.

The input of the audio circuits shown in Fig. 7 enables up to three signals to be mixed: the audio signal associated with the selected video source (master), a randomly selected audio signal (line) and a signal from a stereo microphone.

Selection of the master signal is facilitated by an input selector switch, consisting of analogue multiplexer IC_{404}, and two electronic switches, IC_{405b} and IC_{405c}. The multiplexer selects four of the five possible audio signals, while the electronic switches take care of the fifth. Three audio signals are available from the SCART connectors in Fig. 3 and connector BU_{301} in Fig. 5. The other two arrive from the S-VHS connector and the BNC socket.

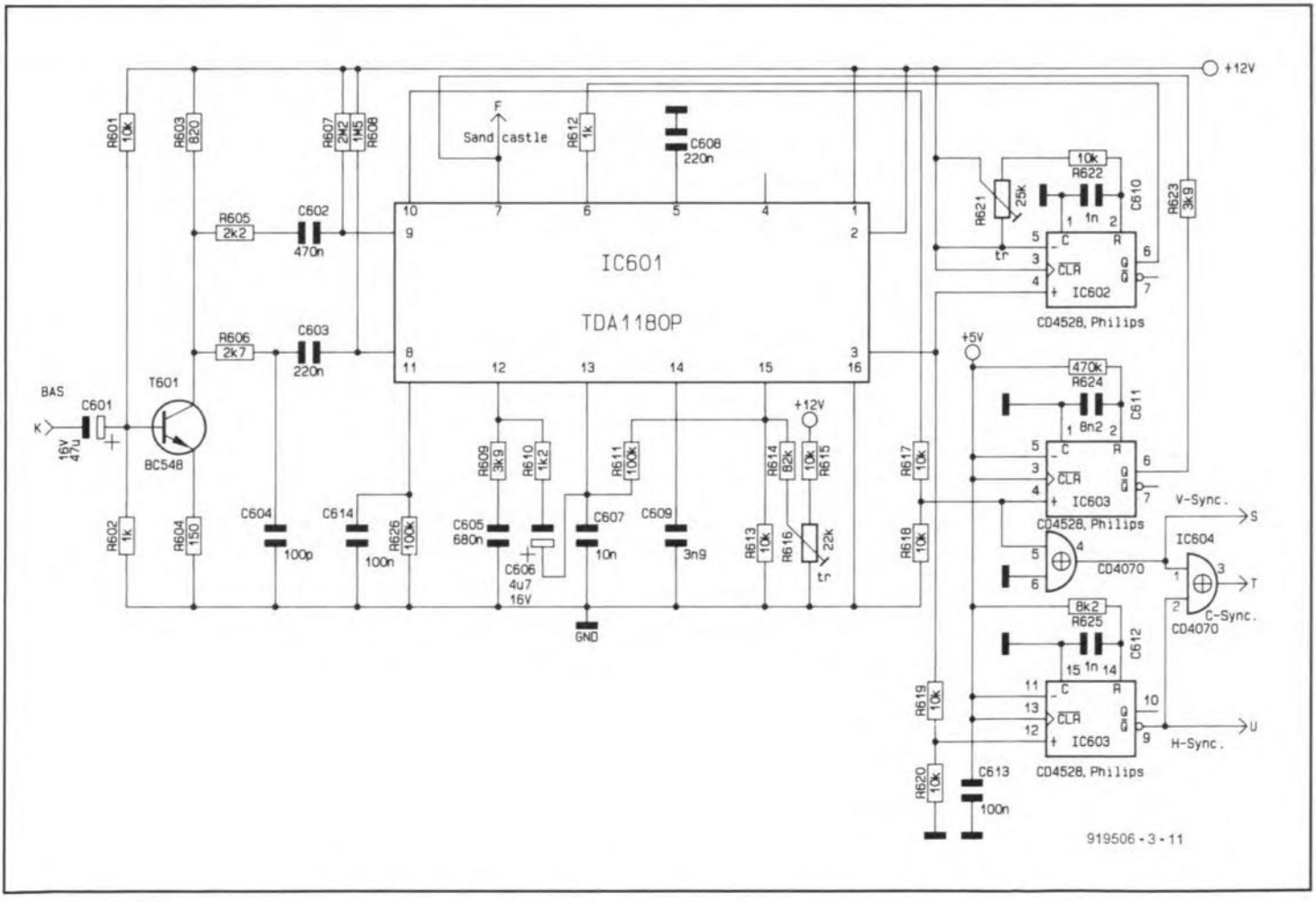


Fig. 6. Diagram of the synchronization circuit.

The line signal at sockets BU_{406} and BU_{407} is connected directly to the line control potentiometers on the mixer.

The level of the microphone signal is well below that of the line and master signals and is, therefore, amplified in IC_{401} (left-hand) and IC_{402} (right-hand).

The mixer consists of three linear stereo slide potentiometers, whose wipers are connected to the relevant left-hand or right-hand line via a summing resistor. The use of linear potentiometers may not seem right, but their wipers are loaded by the summing resistors in a manner that results in traditional logarithmic volume control.

Since not many video signals carry stereo sound, the audio circuit can be switched to mono by closing electronic switch IC_{405a},

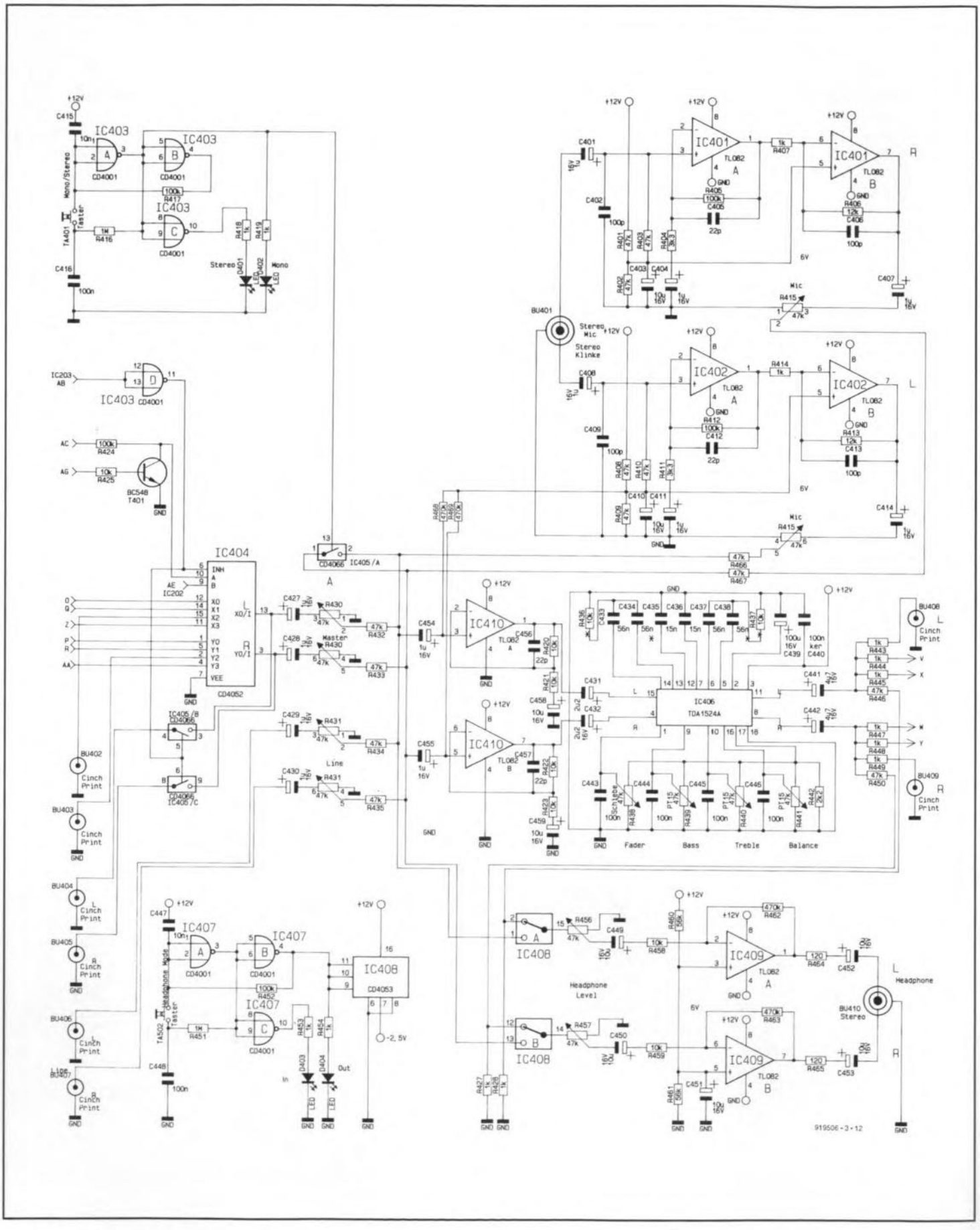


Fig. 7. Diagram of the audio circuits.

which is controlled with switch TA_{401} and a bistable, IC_{403}. The left-hand and right-hand signals from the mixer are then interconnected; their sum is seen by the remainder of the circuit as a mono signal.

The signal is then applied to two non-inverting opamps, IC_{410a} and IC_{410b} and from these to control amplifier IC_{406}. The control amplifier enables the volume, bass and treble , and the balance to be adjusted. The control range of the bass frequencies can be enlarged by using R_{436}, R_{437}, C_{434} and C_{438} (marked with an asterisk). Without these components, the bass range is the traditional ±20 dB. The output of IC_{406} is available at output sockets BU_{408} and BU_{409}.

The headphone amplifier enables the signal before and after the control amplifier to be listened to, depending on the position of electronic switches IC_{408a} and IC_{408b}. These switches are controlled by push button TA_{502} and the circuit based on IC_{407}. The signals from the two sections of IC_{408} are applied to potentiometers R_{456} and R_{457}, with which the volume and balance of the signal to the headphones can be adjusted. The signal to the headphone is amplified in dual opamp IC_{409}.

Power supply

The circuit of the mains-operated power supply is shown in Fig. 8. The rectifier may look unfamiliar, but it is a straightforward bridge, whose negative connection is not directly to earth, but via three diodes. The drop across these diodes is used as an auxiliary negative supply (–2.5 V) for electronic switches IC_{405} and IC_{408}.

Transistor T_{501} serves as the on/off control; it is operated by push button TA_{501} and the circuit based on IC_{503}. That IC is fed by the potential across C_{501} to ensure that it can always be powered. That voltage is too high, however, and it is, therefore, lowered by zener diode ZD_{501}. The output of IC_{503c} is additionally protected against too high voltages by zener diode ZD_{502}.

The circuit following switching transistor T_{501} is traditional: two three-terminal regulators ensure stable output voltages of 5 V and 12 V. The capacitors following the regulators are decoupling devices used at miscellaneous positions in the circuits.

The next and final instalment, dealing with the construction and calibration, will appear in our September issue (there is no August issue).

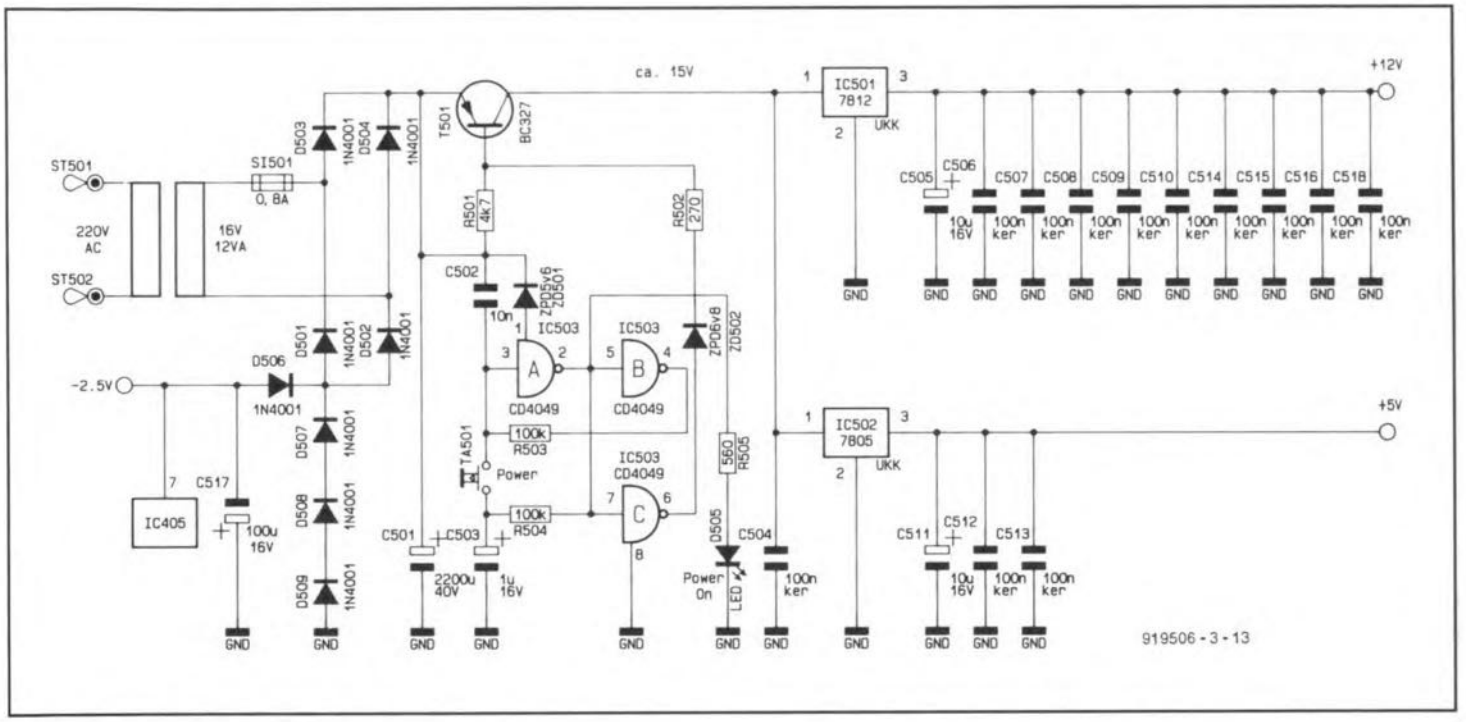
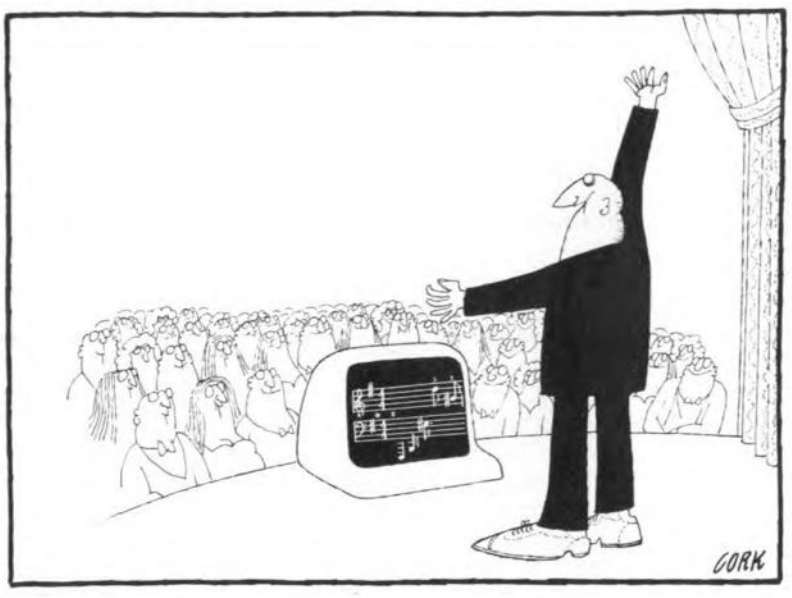


Fig. 8. Circuit diagram of the power supply.



DEALING WITH NOISE AND INTERFERENCE IN ELECTRONIC INSTRUMENTATION CIRCUITS

SHIELDING, FILTERING AND USING LOW NOISE AMPLIFIERS

Many electronic instrumentation and data acquisition circuits must deal with low-level signals in the presence of strong interfering signals. If the signal level is small enough, even the noise produced by amplifiers and passive components can obscure the desired signal. In this article we will look at several strategies for solving problems with low signal level amplifier systems. These techniques include use of a low noise amplifier (LNA), filtering, circuit shielding, input leads shielding (including professional guard shielding techniques) and isolation of the circuit from the power mains.

By Joseph J. Carr

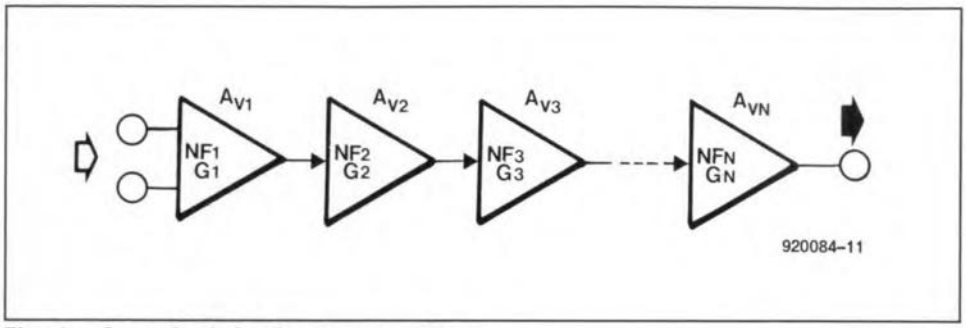


Fig. 1. Cascade chain of voltage amplifiers.

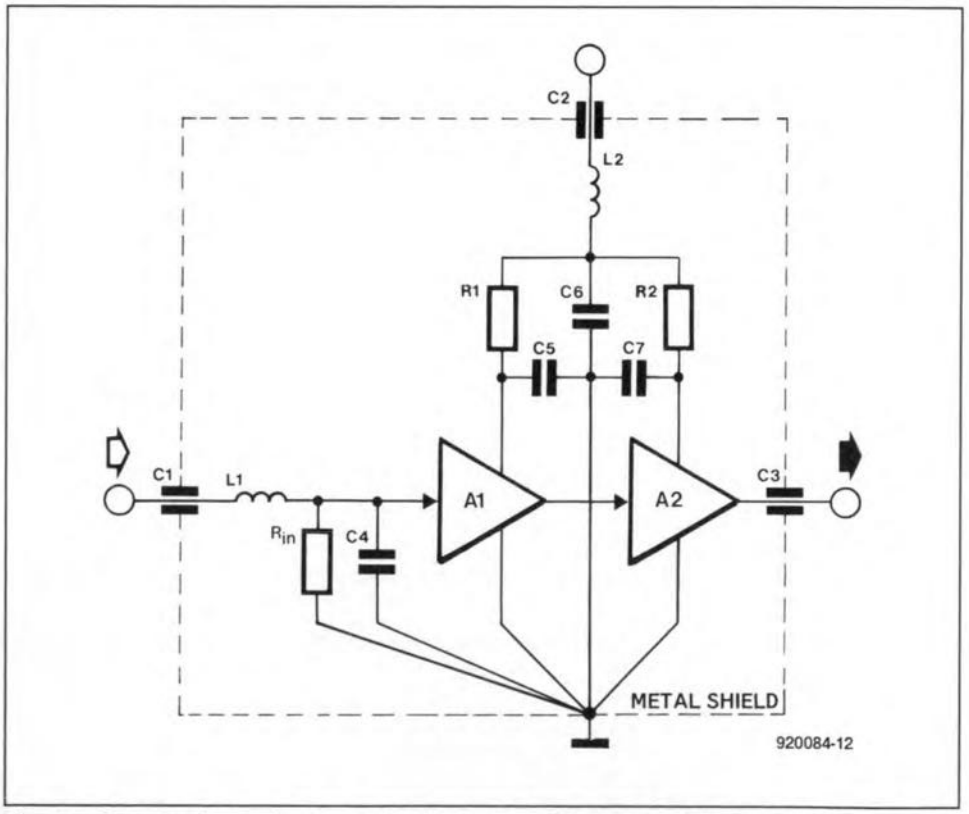


Fig. 2. Generic electronic circuit showing use of shielding and filtering to eliminate noise interference.

Noise, etc.

Noise can be defined as any unwanted signal, even though a somewhat narrower definition is sometimes sought in textbook treatments of the subject. But in the context of this article, *noise* can mean the internal 'hiss-like' noise generated in any amplifier, the atmospheric noise in radio receivers, 50 or 60 Hz hum picked up from the power mains, and interference from nearby sources of electromagnetic radiation (e.g., radio stations or other RF devices). Noise signals mix with, and either distorts or obscures the desired signals.

Several different forms of noise signal can be recognized: *white noise*, *impulse noise* and *interference noise*.

White noise supposedly contains all possible frequencies, so gets its name from analogy to white light, which contains all colours. Such noise is also called *gaussian noise*, although in reality it is neither 'white' nor 'gaussian' unless there are no bandwidth limits placed on the system. True white noise has a bandwidth from d.c. to daylight, and beyond. In practical electronic circuits, however, there are bandwidth limitations, so the noise is actually pseudo-gaussian 'pink' or even 'orange' noise. True gaussian noise can be eliminated absolutely by low-pass filtering, because it by nature integrates to zero, given sufficient time. Bandwidth-limited noise, however, does not integrate to zero, but to a low value. The effect of low-pass filtering on pink noise is therefore not total reduction.

An analogy to pseudo-gaussian or pink

noise is the 'hiss' heard between stations on an FM broadcast band receiver. Much of the noise in instrumentation systems is due to thermal sources, and has an RMS value of:

$$U_n = \sqrt{4\,K\,T\,B\,R} \qquad (1)$$

Where:
U_n is the noise signal in volts (V);
K is Boltzmann's constant (1.38×10^{-23} joules per Kelvin);
T is the temperature in Kelvin (K);
B is the bandwidth in hertz (Hz);
R is the circuit resistance in ohms (Ω).

Noise can be generated in a passive component such as a resistor by virtue of its resistance. According to Eq. (1), in a circuit with a 1,000 Hz bandwidth and a resistance of 100 kΩ, there is 0.6 microvolts (μV) of noise created by molecular motion due to temperature. Although this signal may appear to have a very low amplitude, keep in mind that many signals found in practical systems have the same order of magnitude. For example, in medical electronics, the electroencephalograph (EEG) machine records minute scalp potentials generated by the human brain's electrical activity, and may have components as low as 1 to 2 μV, with peak amplitudes in the 10 to 100 μV range. In that application, 0.6 μV represents a significant artifact, especially when amplified 5,000 to 10,000 times, as is common practice in EEG machines.

Part of the solution to this type of problem is to keep circuit impedances in the early stages — i.e., those stages that most of the gain follows — very low so that the resistance term in Eq. (1) is reduced to a minimum practical value. Additionally,

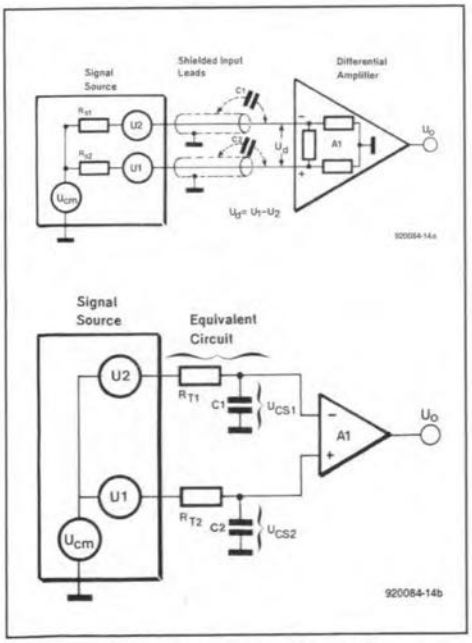


Fig. 4. a) Typical circuit for a differential input amplifier circuit showing sources of resistance and capacitance in the circuit; b) equivalent circuit.

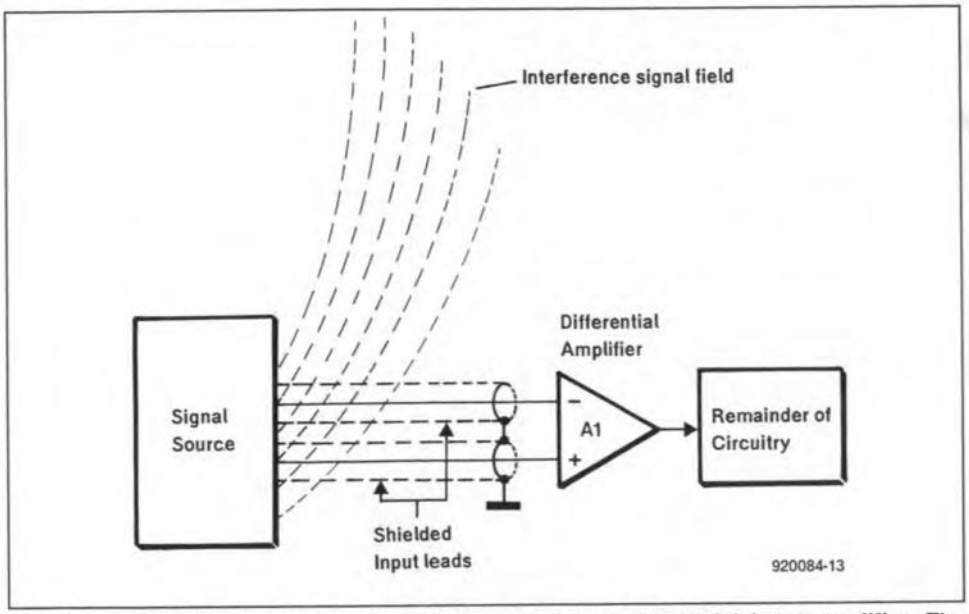


Fig. 3. Generic instrument using a signal source and differential input amplifier. The shielding prevents external interference signal fields from invading the circuit — or does it?

low-pass filtering, bandpass filtering or other methods might be employed to keep the bandwidth term low.

There are several sources of noise that are peculiar to solid-state amplifiers: *shot noise*, *Johnson noise*, and *flicker noise*. In some amplifiers these noise sources can add up to a significant amplitude. Although low-pass filtering offers relief, it is better to specify a low-noise amplifier for the earliest stages in the system.

Friis' equation uses the noise factors (i.e. ratio of input to output signal-to-noise ratio) to show us that low noise amplifiers in the input stages provide most of the noise relief for the entire system. It is for this reason that satellite communications or TV earth stations use Low Noise Amplifiers (LNA) as preamplifiers on the dish antenna. Similarly, analogue instrumentation and data acquisition amplifiers use a single LNA in the front-end, and then ordinary amplifiers throughout the rest of the circuit. The Friis equation for a cascade chain of amplifiers such as Fig. 1 is:

$$NF_{total} = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1}\,G_1 + \frac{NF_n - 1}{G_1\,G_2\,G_3 + G\,(N-1)} \qquad (2)$$

Where:

NF_{total} is the noise factor of the entire cascade chain;
NF_1, NF_2, etc. are the noise factors of the individual stages;
G_1, G_2, etc. are the gains of the individual stages.

Thus, we can use a single, usually premium low noise amplifier device for the first stage, and regular amplifiers for all others.

Low noise operational amplifiers are a good choice, but are sometimes rather expensive. A low cost alternative for many uses is the CA3130, CA3140 or CA3160 device in the 8-pin metal can package (not the mini-DIP!). Use a flexible heatsink of the type used for TO-5 metal transistor packages on the op-amp package, and operate the device from ±5 V dual polarity d.c. power supplies. This treatment (heatsinks and low power supply voltages) will mimic low-noise operation.

Other noise problems

Impulse noise is due to local electrical disturbances such as arcs, lightning bolts, electrical motors and so forth. Part of this same general type is general electromagnetic interference (EMI) problems. Such interference is usually caused by nearby radio transmitters, or other RF sources. It is not usually possible to force the transmitter off the air, even when it is an amateur operator, because they are licensed by the Government to be there … while you are not.

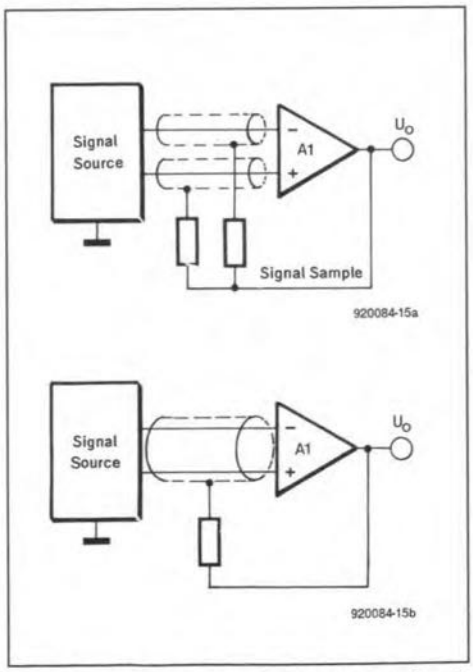


Fig. 5. a) Simple guard shield drive circuit for twin shields; b) same circuit for single shield circuits.

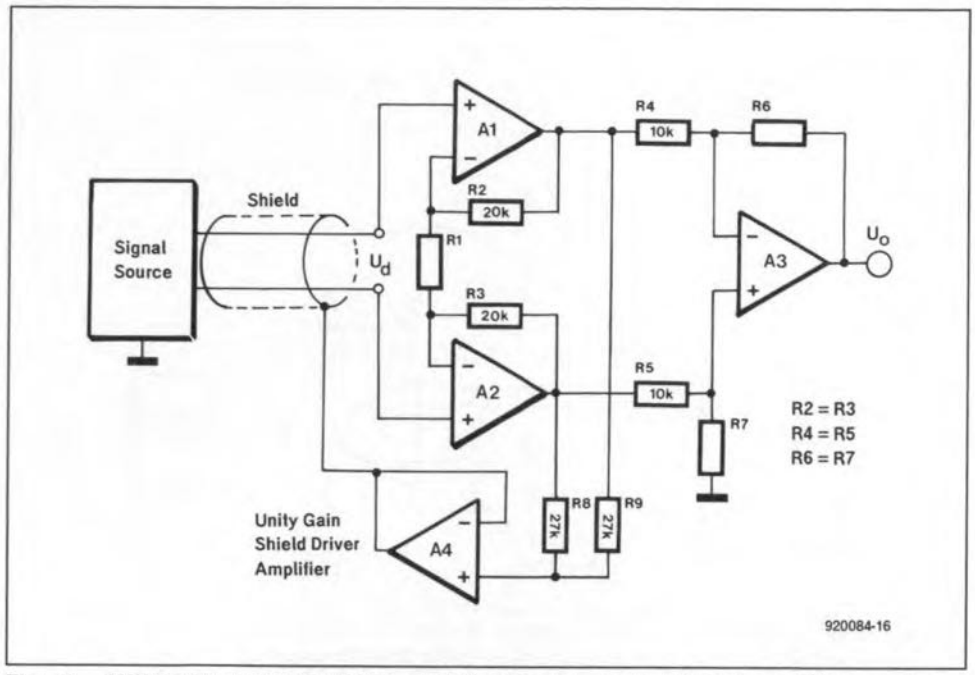


Fig. 6. Differential instrumentation amplifier, based on operational amplifiers, using an active guard shield driver (amplifier A4).

From an engineering point of view, your equipment might be very expensive and quite good, and still be very poor from an EMI point of view. The purpose of any electronic equipment is twofold: a) *it must respond to proper signals*, and b) *it must reject improper signals*. It is point 'b)' where most improperly designed equipment fails most significantly.

Shielding and filtering of signal lines is the key to EMI problems. Figure 2 shows a generic circuit with several of the possible correction types used. First, note that the entire instrument is built inside of a shielded metal box, and the box is grounded. Points of entry and exit are passed through feedthrough 'EMI filter' capacitors. Feedthrough capacitors C_1 through C_3 have values of 50 pF to 2 nF (0.002 µF), depending on the circuit impedance and which capacitor is specified. For example, the signal line capacitors C_1 and C_3 will have smaller values, while power supply capacitor C_2 should be larger than 1 nF (0.001 µF).

Each stage in Fig. 2 is isolated from other stages by a resistor, and has its own decoupling capacitor (C_5 and C_7). The main power bus is decoupled (C_6), and has a series radio frequency choke (L_2) to prevent RF that gets past C_2 from interfering with the operation of the circuit. The input leads are similarly filtered with L_1 and C_4. The input resistance (R_{in}) of the amplifier and capacitor C_4 also form a low-pass filter with a frequency response that rolls off at a −3 dB/octave rate from the −3 dB point defined by:

$$F = \frac{1}{2\pi R_{in} C_4} \qquad (3)$$

Where:
F is the frequency in hertz (Hz)
C_4 is in farads (F)
R_{in} is in ohms (Ω)

Not all of the techniques of Fig. 2 are needed, or even appropriate, in all circuits. Their inclusion was meant to show the possibilities, rather than form a recommendation for all applications. Select those that are appropriate, or practical, for your particular application.

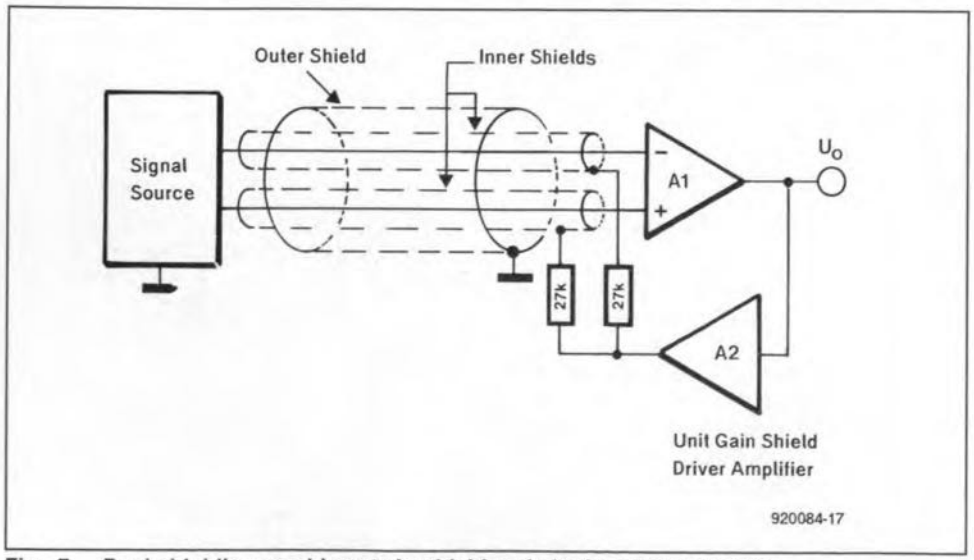


Fig. 7. Dual shielding combines twin-shield and single shield concepts.

Suppressing local interfering signals

Local interfering signals are created by other electrical devices close to the circuit being operated, and by the 50/60 Hz electrical power mains in the building. Consider Fig. 3, where a low-level signal source is connected to an amplifier at the input of a larger circuit. The signal source might be a sensor such as a Wheatstone bridge strain gauge, an electro-optical detector. Alternatively, it may be a biopotential such as the EEG brain wave signal or electrocardiograph (EEG) heart signal. The common factor shared by these signals is that they produce low level signals, and often must operate in a high interference environment.

A common solution to these problems is to use a *differential amplifier* at the input of the circuit. One of the properties of the differential amplifier is that its *common mode rejection ratio* (CMRR) tends to suppress interfering signals from the environment. It does this job because the inverting (−) and non-inverting (+) inputs offer equal gain, but are of opposite polarity. If identical signals are applied to the two inputs simultaneously, the net output voltage will be zero.

When a differential amplifier is used in a situation where it is connected to an external signal source through wires, those wires are subjected to strong local signals such as the 50/60 Hz a.c. fields from nearby power line wiring. Fortunately, in the case of the differential amplifier the field affects both signal equally, so the induced interfering signal is canceled out by the common mode rejection property of the amplifier.

Guard shielding

Unfortunately, the cancellation of interfering signals by the input amplifier CMRR is not total. There may be, for example, imbalances in the circuit that tend to deteriorate the CMRR of the amplifier. These imbalances may be either internal or external to the amplifier circuit. Figure 4a shows a common sensor interface scenario, similar to Fig. 3: a differential amplifier connected to shielded leads from the signal source, U_{in}. Shielded lead wires offer some protection from local fields, but there is a problem with the standard wisdom regarding shields: *it is possible for shielded cables to manufacture a valid differential, but erroneous, signal voltage from a common mode signal*!

Figure 4b shows an equivalent circuit that demonstrates how a shielded cable pair can create a differential signal from a common mode signal. The cable has capa-

citance between the centre conductor and the shield conductor surrounding it. In addition, input connectors and the amplifier equipment internal wiring also exhibits capacitance. These capacitances are lumped together in the model of Fig. 4b as C_1 and C_2.

There are also resistances in the circuit. The signal source resistances R_{S1} and R_{S2} are generally low, but in some cases (e.g., EEG, ECG, pH electrodes, optoelectronic sensors, etc.) they may be quite high. In addition, there are also input impedances, both differential and unbalanced to ground (see Fig. 4a).

As long as the sum circuit resistances are equal, and the two capacitances are equal, there is no problem with circuit balance. But inequalities in any of these factors (which are commonplace) creates an unbalanced circuit in which common mode signal U_{cm} can charge one capacitance more than the other. As a result, the difference between the capacitance voltages, U_{CS1} and U_{CS2}, is seen as a valid differential signal by the amplifier.

A low-cost solution to the problem of shield-induced artifact signals is shown in Fig. 5a. In this circuit, a sample of the two input signals are fed back to the shield, which in this situation is not grounded. This type of shield is called a *guard shield* circuit. Either double shields (one on each input line) as shown in Fig. 5a or a common shield for the two inputs as in Fig. 5b, can be used.

An example of guard shielding for the standard three op-amp instrumentation amplifier, a very common differential front-end for electronic instrument circuits, is shown in Fig. 6. The instrumentation amplifier consists of A1, A2 and A3, with associated resistors. If R2=R3, R4=R5 and R6=R7, the voltage gain of the circuit is given by:

$$A_V = \left(\frac{40k\Omega}{R1} + 1\right)\left(\frac{R6}{10k\Omega}\right) \qquad (4)$$

(All resistance in kilo-ohms)

In Fig. 6, the gain can be set by selecting values for R1 and R6, which implies also a value for R7 (which is equal to R6). Variable gain control is provided by making R1 variable. Keep R1 away from zero ohms, however, or the gain will get very high very quickly.

In the circuit of Fig. 6, a single shield covers both input signal lines, but it is possible to use separate shields. In this circuit a sample of the two input signals is taken from the junction of resistors R8 and R9, and fed to the input of a unity gain buffer/driver 'guard amplifier' (A4). The output of A4 is used to drive the guard shield.

Perhaps the most common approach to guard shielding is the arrangement shown in Fig. 7. Here we see two shields used: the input cabling is double-shielded insulated wire. The guard amplifier drives the inner shield, which serves as the guard shield for the system. The outer shield is grounded at the input end in the normal manner, and serves as an electromagnetic interference suppression shield.

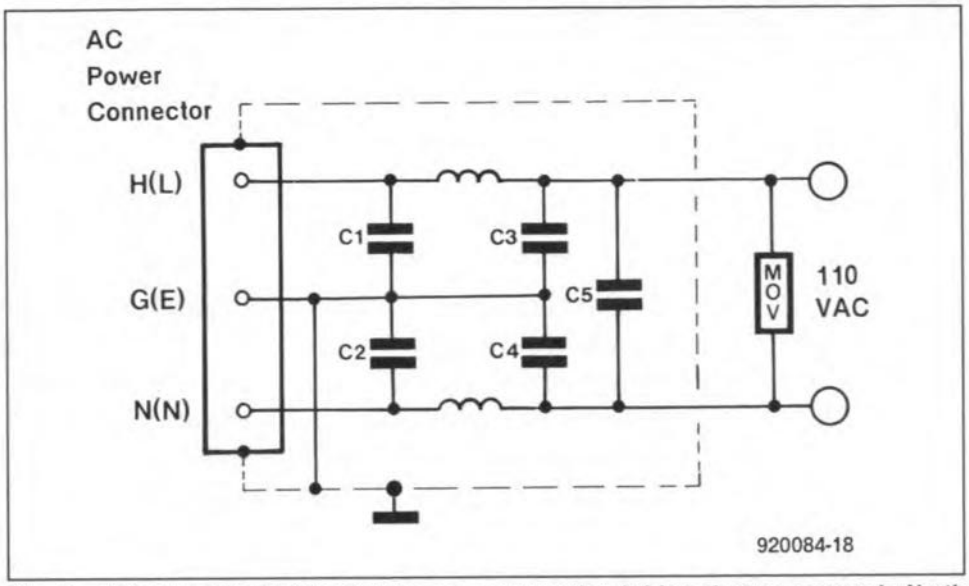


Fig. 8. Shielded LC EMI filter for the a.c. power mains (wiring shown common in North America).

Power line noise

Another potential source of interference is noise and EMI signals arriving on the a.c. power mains. I can recall digital instrumentation and computers in a medical school building that acted in a schizophrenic manner until it was identified that the a.c. power mains were the source of the problem.

A humorous event while this problem existed came about when the medical (M.D.) and medical sciences (Ph.D and D.Sc) students took the standard multiple choice national examination in human physiology. They used a 'mark-sense' answer sheet on which they use a pencil to darken the letter corresponding to the printed candidate answer they believe is correct. These papers were then taken to an optical scanner that input the answers to a computer. While the scanning was going on one year, some ac power line switching equipment started operating, sending high voltage transients over the mains. The result was that the entire freshman class of medical and sciences students flunked the national exam!

Where sensitive scientific instruments are used, one might want to consider designing the ac electrical power mains system to be either isolated from the building system, or having a separate system that keeps a separated neutral and ground conductor all the way back to the service entrance of the building.

Figures 8 and 9 show methods for dealing with severe power mains noise. In Fig. 8 we see an *L-C* power line filter wired in the North American standard manner. These filters are shielded low-pass filters, and are mounted inside of equipment as close as possible to the point where a.c. enters the cabinet. Some filters are available molded into the a.c. chassis connector. Exterior to the filter is a *Metal Oxide Varistor* (MOV) device used to suppress a.c. line transients above the normal peak a.c. voltage (some high voltage transients can reach 2000 V for 30 µs).

The transformer in Fig. 9 performs two functions. First, it isolates the equipment electrical system from the mains electrical system. Second, it frequency limits the system to prevent high frequency transients and pulses from passing into the equipment. It is my opinion, shared by many other engineers, that no computerized or other digital equipment — and many types of analogue equipment — should be operated in a noisy environment without one of these transformers. If the equipment is life-support, or life-saving, as it often is in medical applications, then it is probably engineering malpractice to design a piece of equipment without the transformer. ■

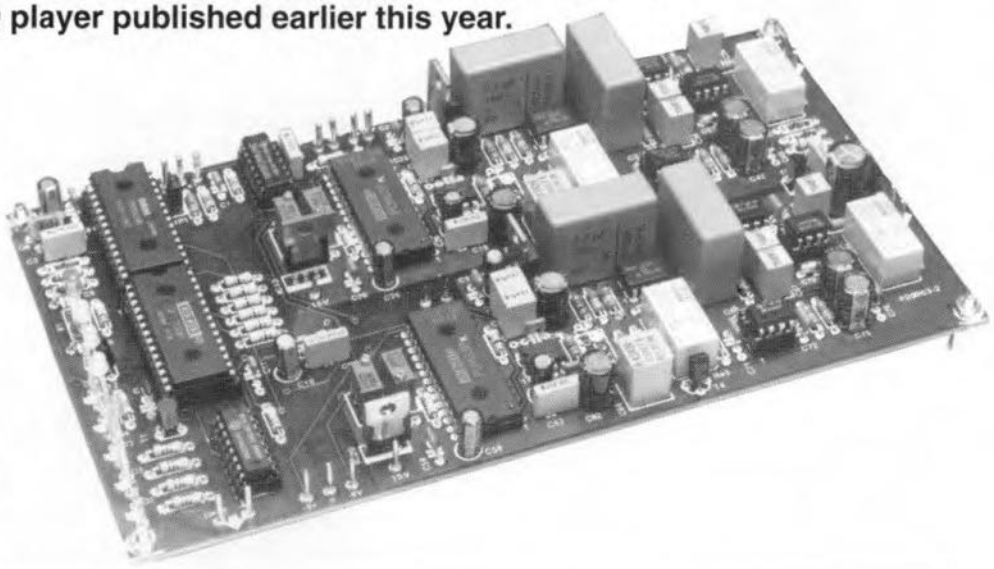
Fig. 9. Line isolation transformer used with digital instruments, analogue instruments and computers to eliminate high voltage transients, mains voltage fluctuations and other problems. This transformer is manufactured by Topaz in the USA.

A.F. DIGITAL-TO-ANALOGUE CONVERTER

PART 1

Design by T. Giesberts

Twenty-bit converters, ×8 oversampling and high-quality analogue stages are used to translate the digital output of CDs, DAT recorders or radio broadcasts into the desired analogue information as accurately as possible. The converter is a stand-alone unit that is eminently suitable for use with the CD player published earlier this year.



DURING the past decade, digital techniques have assumed an increasingly important role in audio engineering. Hailed, somewhat exaggeratedly, as 'perfect' and 'ideal', quite a few improvements have been found necessary since those early years in appliances using these techniques. No doubt, others will be found indispensable over the next few years. There is also a growing band of audio pundits who foresee the end of both the CD and DAT before the year 2000.

Be that as it may, at present, the CD player is the second most important unit in the audio chain (world-wide, the compact cassette is still way ahead as the most popular music medium). It is well known that the output sections of that unit play a vital role in producing a near-perfect reproduction of the original sound. Unfortunately, a CD player cannot be upgraded as easily as a record player in the past. Then, a better quality tone arm or styles could be added without any trouble. In a CD player, the only improvements possible are in the digital or analogue sections and they are not so easily implemented. There are, of course, two other possibilities: buy a new CD player or an add-on digital-to-analogue converter—DAC. Neither of these is a simple solution, although in the case of the add-on unit, it should be borne in mind that it can be used with a number of different appliances.

Furthermore, there are not that many commercially available stand-alone DACs on the market, probably owing to their high price: at present this can vary from a few hundred to a few thousand pounds. A build-yourself design was until now not really feasible owing to the non-availability of certain parts and components. The design presented costs about one third of a commercially available unit with near-identical specifications: £250–£400.

The design

The digital-input selection in the block schematic in Fig. 1 accepts four digital signal sources, which may be connected by fibre-optic or coaxial cable. The tape select stage enables any one of the four signals to be applied to the digital tape output.

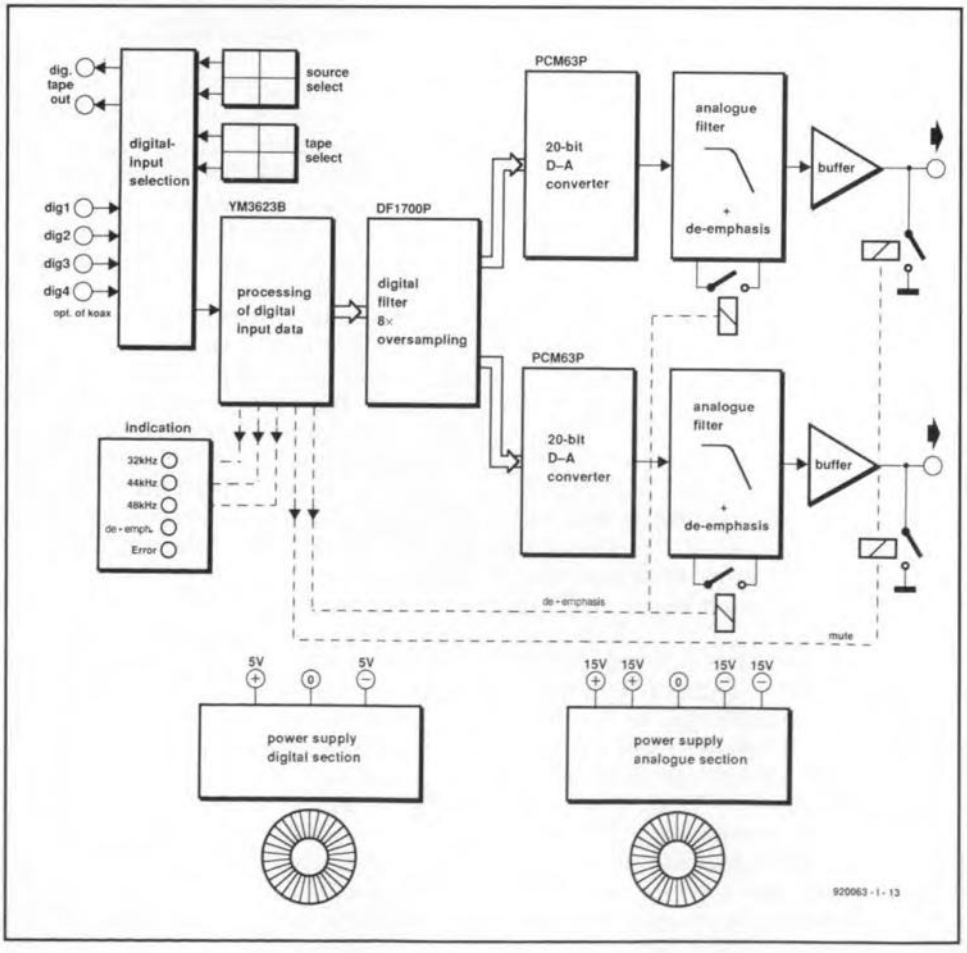


Fig. 1. Block diagram of the digital-to-analogue converter.

The selected input signal is applied to a special Yamaha IC Type YM3623. The circuit of this chip is shown in Fig. 2. Its PLL (phase-locked loop) produces a clock from the input signal for the subsequent stages. The range of the PLL is wide enough to enable the processing of all current sampling frequencies. In the absence of an input signal, the IC's crystal oscillator generates a stable frequency for the digital filter and the actual DAC stages.

The most important task of this chip is, however, the analysis of, and error detection (Philips-Sony format) in, the audio data of the incoming signal before this is applied to the digital filter.

Basically, the data provided by the IC could be processed directly by the DAC, but that would create problems in the analogue section, because the sampling frequency must be sufficiently suppressed there without introducing amplitude and phase errors in the audio range. That introduction is combated by oversampling, which involves the computation by a digital filter of intermediate steps that cause the sampling frequency to be shifted upwards artificially. The more intermediate steps, the higher the sampling frequency, and the easier the design of the analogue filters.

The digital filter, a Burr-Brown Type DF1700 dual channel type, provides ×8 oversampling, which means that each sample is converted into eight discrete levels. These levels make possible smaller steps than the various original levels. The ×8 oversampling converts the input data frequency of 44.1 kHz (with CD reproduction) to 352.8 kHz. This means that a third-order filter can be used in the analogue section, which reduces filter phase non-linearities.

The interposition of additional steps and the computation of the intermediate values increase the resolving power at the output of the digital filter compared with that of the 16-bit input. If a converter with an accuracy of more than 16 bits is used, the increased resolving power is retained in the conversion, so that in the present design, the converter processes 20 bits. This is, by the way, the maximum resolution the DF1700 can provide at its output. The pass-band ripple of the DF1700 is <0.00005 dB.

Although one-bit converters are currently in fashion, they do not really give satisfactory results for top-of-the-range equipment. In the present design, a 20-bit monolithic IC Type PCM63P from Burr-Brown was chosen. Burr-Brown supplies many manufacturers of CD players and currently this chip is their top multibit converter.

The PCM63P—see Fig. 4—contains two 19-bit converters: one each for the positive and negative halves of the signal. This design has the advantage that it prevents bipolar zero distortion (traditional DACs usually switch the most significant bit around the bipolar zero, which may give rise to glitches and non-linear distortion). To ensure exact synchronization of the two converters, they use the same *R-2R* ladder network and the same reference voltage. Because of the 20-bit conversion, the harmonic distortion is low:

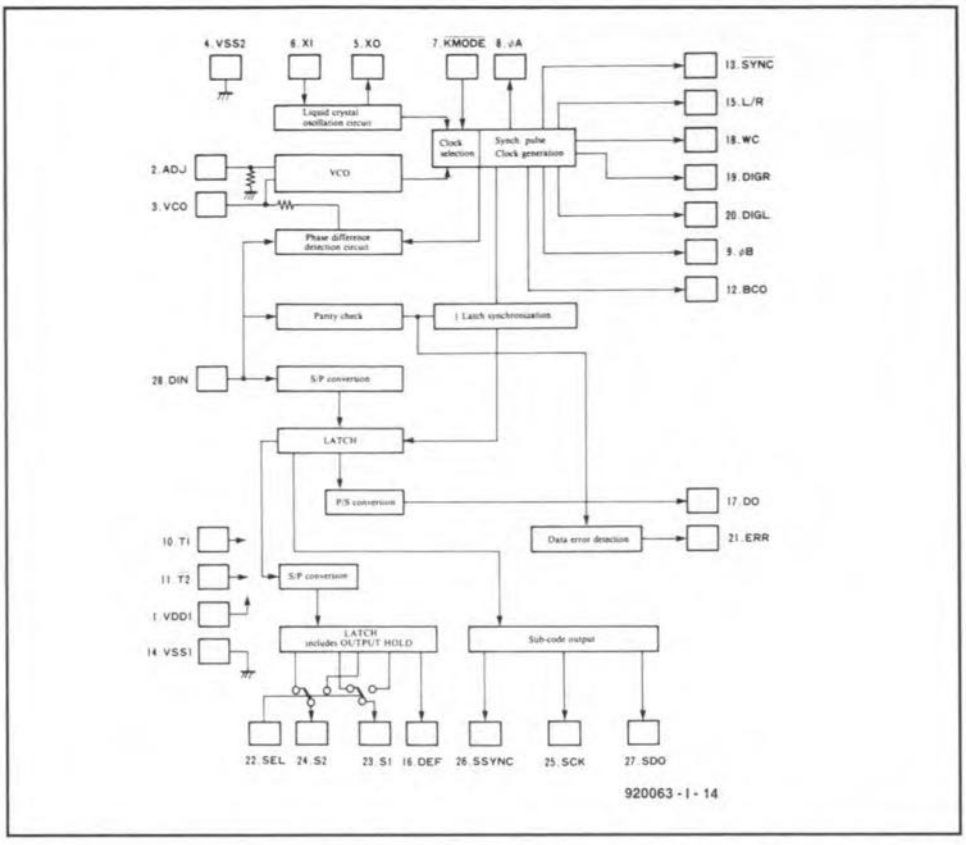


Fig. 2. Block schematic of Yamaha's digital audio interface receiver Type YM3623.

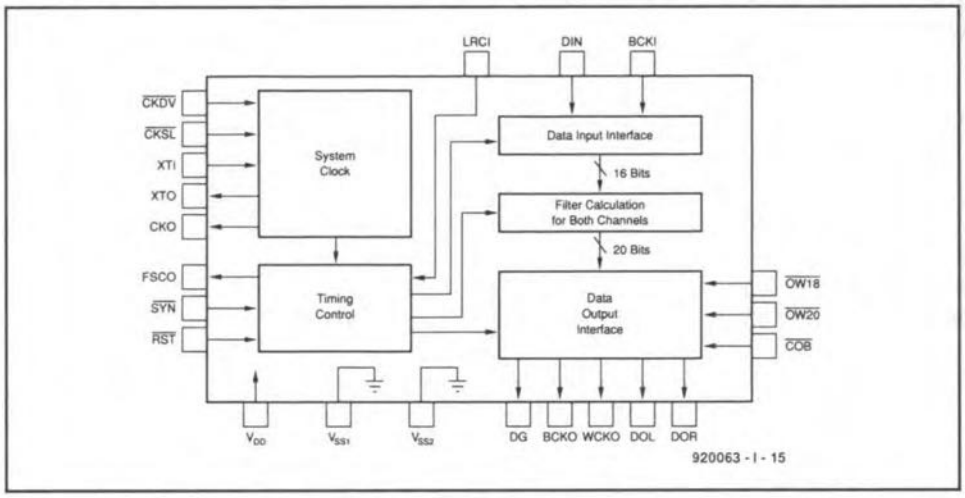


Fig. 3. Block schematic of Burr-Brown's Type DF1700 dual-channel digital filter.

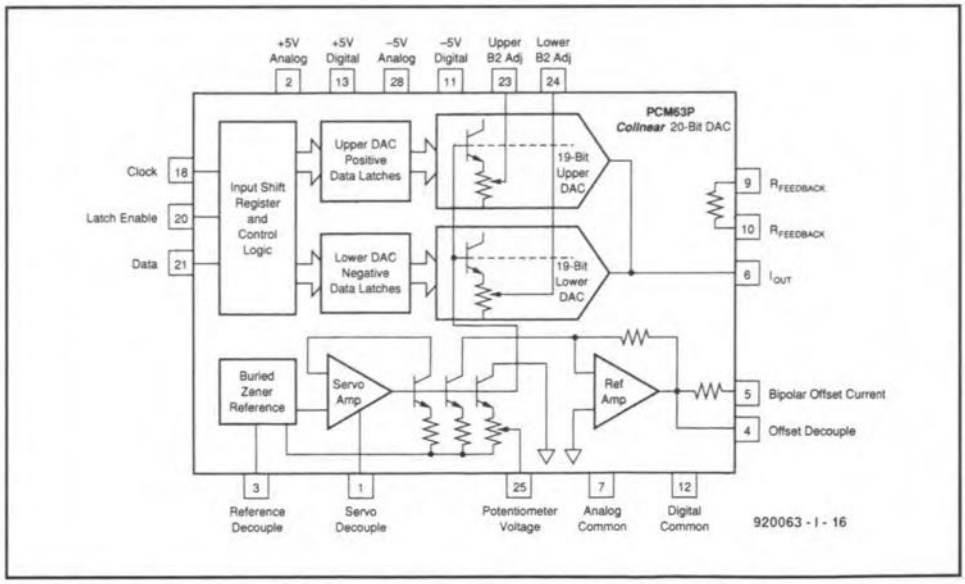


Fig. 4. Block schematic of Burr-Brown's 20-bit monolithic audio DAC.

–96 dB at full drive (K version).

The analogue output section consists of a very fast current-to-voltage converter following the DAC and a third-order low-pass filter in which no opamps are used. Its design is known as a Generalized Impedance Converter—GIC. In this, an opamp configuration to ground acts as a second-order frequency-dependent passive element. This has the advantage that the audio signal does not have to pass through an opamp.

The analogue signal is fed to the output via a buffer stage. Relays short-circuit the output when a high level of noise is present or when the de-emphasis circuit is switched in, if the input signal makes that necessary.

The design of the power supply ensures complete separation of the digital and analogue sections, and it, therefore, used two transformers. No fewer than ten regulator ICs ensure optimum supply quality.

The circuit

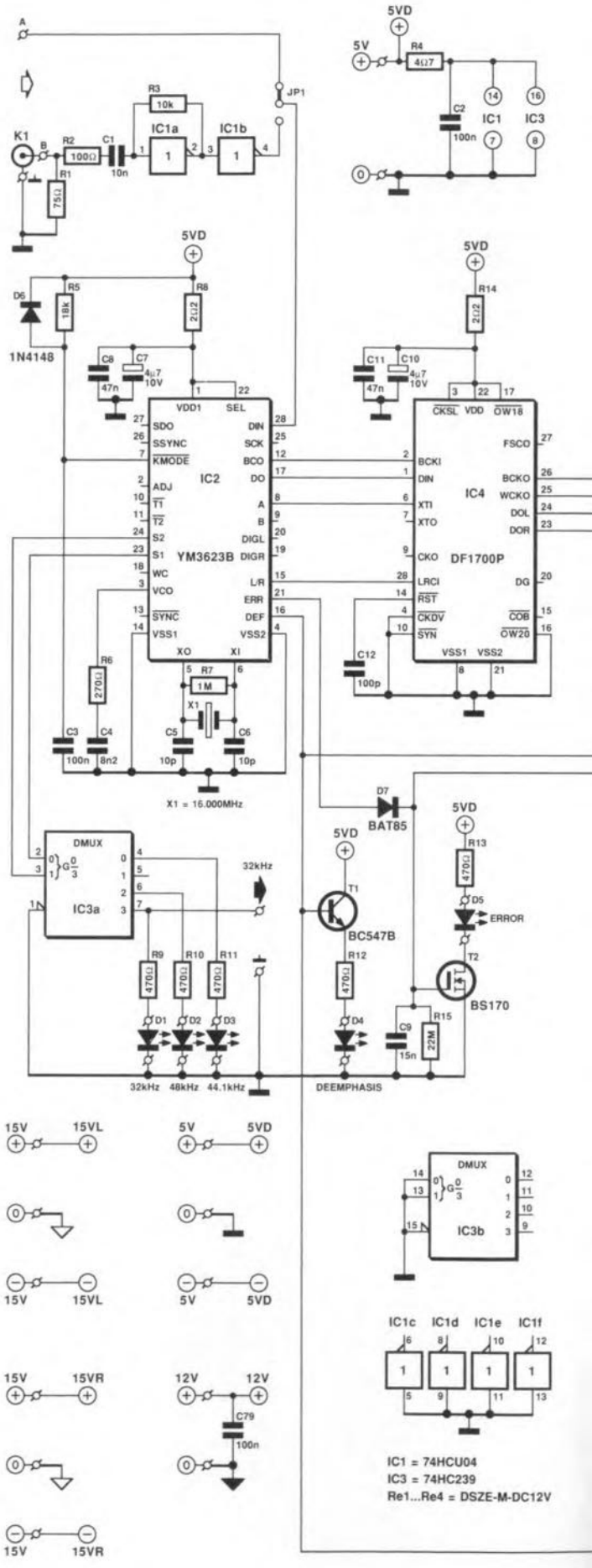
The digital signal from the CD player, DAT recorder, or DCC (digital compact cassette) player enters the circuit in Fig. 5 via K_1. Resistor R_1 ensures correct termination of the coaxial input cable to obviate possible reflections. The bi-phase signal is enhanced by two inverters, IC_{1a} and IC_{1b}. With the aid of R_2 and R_3, the former is arranged as an analogue amplifier that raises the 500 mV signal six-fold. Inverter IC_{1b} produces a pure TTL signal with improved transitions (edges). The signal is then applied to the Digital Audio Interface Receiver—DIR—IC_2.

When the digital input selector (to be published shortly) is used, the input signal is applied from that selector to A—resistors R_1, R_2, and R_3, capacitor C_1 and IC_1 can then be omitted.

The YM3623B requires only few external components. Crystal X_1 provides a stable output frequency in the absence of input data; the internal PLL is then switched off. Capacitor C_4 and resistor R_6 form, the integrator network for the VCO—voltage-controlled oscillator—of the internal PLL. The values of these components have been chosen to ensure that the 32–48 kHz frequency range is scanned with the minimum of phase jitter. Network R_5-C_3-D_6 resets the clock switchover circuit in the IC at power-on. The supply line is decoupled by R_8-C_7-C_8.

Note that the crystal frequency is usually chosen to give an oscillator frequency of exactly 44.1 kHz (after scaling). In practice, it transpired that that created a lot of interference in the PLL, since both operate at about the same frequency. Therefore, a crystal frequency that is not a multiple of the sampling frequency was chosen. This does not detract from the operation of the circuit, because the oscillator is in any case used only as an emergency frequency source for the internal logic of the IC and subsequent circuits in the absence of in put data. The crystal frequency may be 16–20 MHz.

The YM3623B provides, apart from the audio data, also additional information contained in the bi-phase signal. For instance,



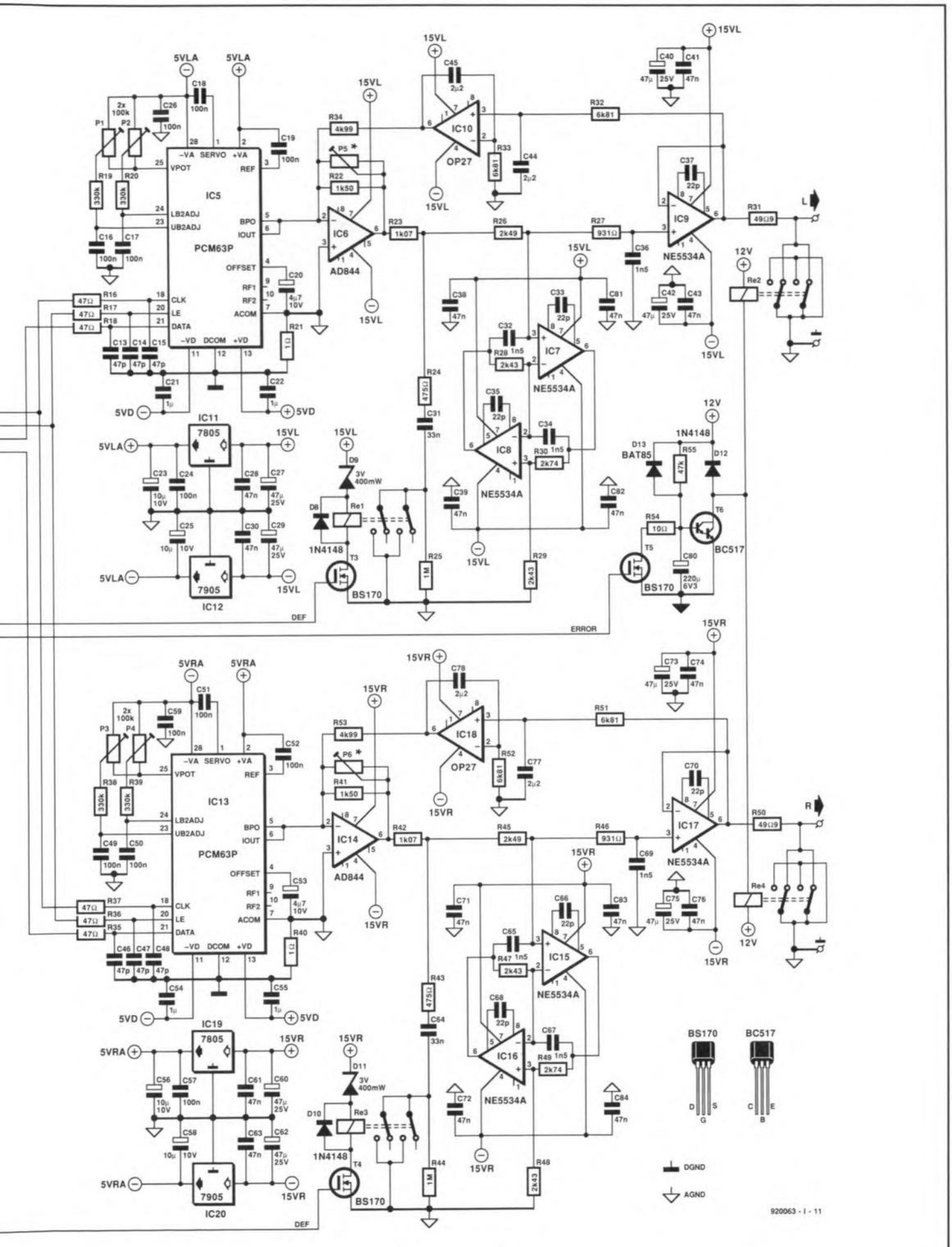


Fig. 5. Circuit diagram of the audio-frequency digital-to-analogue converter.

outputs S_1 and S_2 carry the current sampling frequency. That information is made visible with the aid of IC_{3a} on one of three LEDs: 32 kHz; 44.1 kHz; 48 kHz.

The copy bit contained in the information is not made visible, because it is not used by any manufacturer.

The ERR(or) output indicates when an error has been detected in the data input. The signal available at this pin is lengthened sufficiently by pulse stretcher R_{15}-C_9-D_7 to switch on T_2 switching, so that D_5 lights. The ERR signal is also used to energize relays Re_2 and Re_4 via T_5, whereupon the analogue outputs are switched off. Transistors T_2 and T_5 are MOSFET types to keep the switching currents on the printed-circuit board low.

The DEF output signals the presence of pre-emphasis on the input, whereupon the de-emphasis network and T_1 are switched on via Re_1 and Re_3. As soon as T_1 conducts, D_4 lights.

Subsequently, the audio signal is fed from pin 17 of IC_2 to digital filter IC_4. This IC needs clocks to function correctly: one is derived from the bi-phase signal and is available at pin 8 of IC_2, while the other is the timing signal for writing serial data and is available at pin 12 of IC_2. It also needs a multiplex signal that indicates whether the current data are for the left-hand or right-hand channel; this signal is fed from pin 15 of IC_2 to pin 28 of IC_4.

The supply lines to the filter are decoupled by R_{14}-C_{10}-C_{11}.

After the filter has translated each data word into eight new values, the DACs can be driven by these data (DOR=Data Out Right; DOL=Data Out Left). Again, some control signals are needed: bit clock (BCKO) and word clock (WCKO).

The *RC* networks inserted into the lines from the filter to the DACs filter out any RF interference and noise signals.

As an aside, assuming that a CD signal is input, the system clock from IC_2 to IC_4 is 16.9344 MHz—the L/R clock is, of course, 44.1 kHz. The clock (BCO) for writing serial data is 2.8224 MHz. The BCKO clock and WCKO clock between the digital filter and the DACs are 8.4672 MHz and 352.8 kHz respectively. It is clear that these are all RF signals, and it is imperative to keep them—and their harmonics—away from the analogue section.

Presets P_1 and P_2 (P_3 and P_4) enable the setting of the MSB—most significant bit—of each 19-bit converter in IC_5 and IC_{13}. Precision test equipment is required for this, however; if that is not available, the presets can be omitted. The ICs are available in three versions indicated by (a) no letter after the type number (least expensive); (b) a J after the type number; (c) a K after the type number (most expensive).

Since the divorce of the analogue and digital sections comes about in the DACs, attention must be paid to the power supply. As already stated, the supplies for the two sections are completely separate. All supply connections are decoupled independently. Moreover, on the relevant printed-circuit board, the earth connections for the two

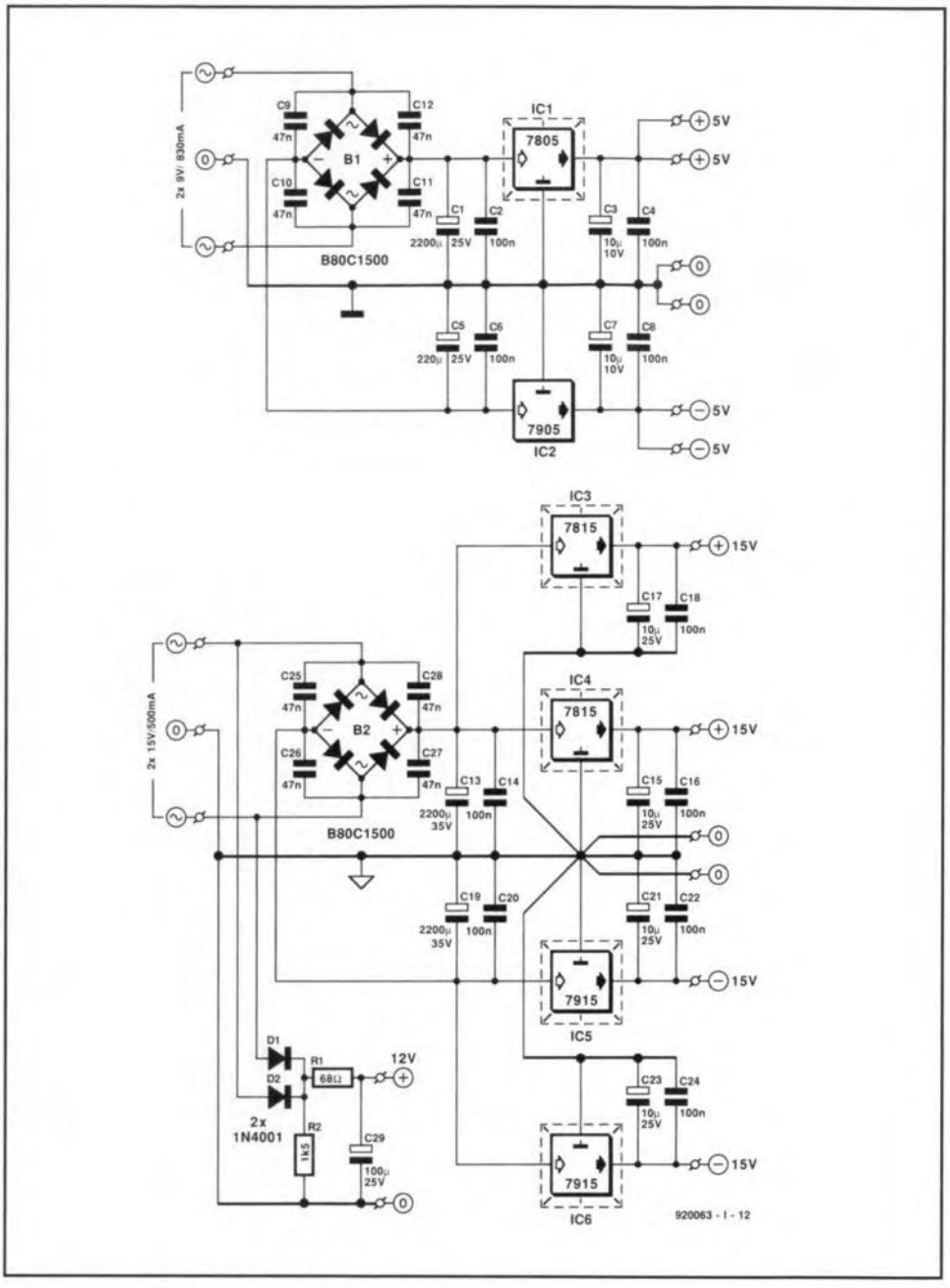


Fig. 6. Circuit diagram of the power supply for the DAC.

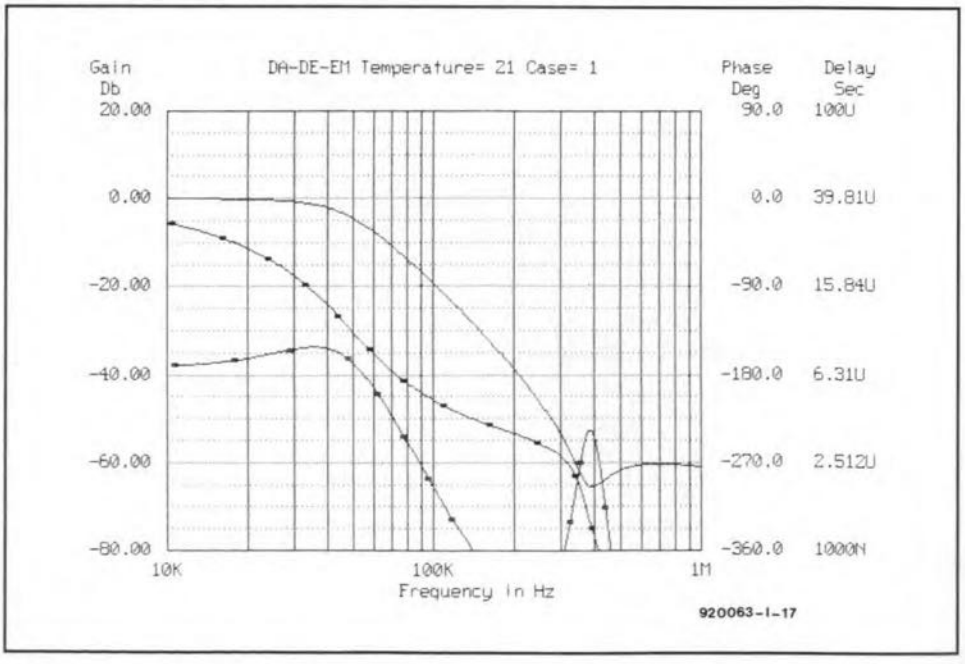


Fig. 7. Theoretical response of the analogue output filter.

sections have been kept separate.

The output of the converters is applied to a current-to-voltage converter, IC_6 and IC_{14}, for the left-hand and right-hand channel respectively. These are needed, because virtually all converters provide an analogue output current rather than a voltage. Undistorted conversion of the voltage waveform (analogue signal with superimposed steps of the sampling frequency) requires an IC with a very high slew rate. That requirement is met by Analog Devices' Type AD844, an opamp with a bandwidth of 60 MHz and a slew rate of no less than 2000 V/µs.

The output filter is a third-order pseudo passive design, that is, there are no active components in the signal path. It consists of R_{23}+R_{26} followed by the GIC configuration of IC_7 and IC_8, which is followed in turn by passive section R_{27}-C_{36}.

The de-emphasis network is entirely passive and consists of R_{23}-R_{24}-C_{31}. It is switched into circuit by relay Re_1 as soon as this is energized, whereupon R_{25} is short-circuited (left-hand channel).

Finally, buffers IC_9 (left-hand) and IC_{17} (right-hand) provide a high load for the low-pass filter on the one hand, and sufficient current for driving a (pre)amplifier at the output of the converter.

The impedance of the analogue outputs is 50 Ω (R_{31} and R_{50}). Resistors R_{31} and R_{50} also make it possible for the mute relays, Re_2 and Re_4, to short-circuit the outputs to earth without detriment. Energizing of these relays is delayed by the circuit based on T_6. This gives the entire circuit time to settle in after power-on before any relays are energized. In the case of error indications, the mute relays are de-actuated off via T_5.

There is a wide choice of opamps for the low-pass filter and buffer stages. Ten different models were tried in the prototypes, but their performance was more or less uniform. The parts list (next instalment) gives an NE5534A, which was the least expensive of the ten. Note also, that there are commercial CD players costing over £1000 that also use the NE5534A.

It will have been observed that the entire analogue section is DC coupled and also that there is no output capacitor. To ensure that the direct voltage at the output is always exactly zero, a servo control, IC_{10} and IC_{16} respectively, has been added between the output of the buffer opamp and the non-inverting input of the current-to-voltage converter opamp. Although the off-set current of the DACs is virtually zero, this arrangement ensures that very-low-frequency signals, as well as the off-sets of the various opamps, are nullified.

The servo control is an integrator that monitors the output voltage of the buffer, on the basis of which it adjusts the direct voltage of the *I-U* converter so that the output voltage remains zero. The control has absolutely no effect on signals in the analogue circuits above 10 Hz. To ensure purity of the signal in the servo control, which is after all a sort of high-pass filter with low cut-off frequency, all capacitors are MKP (metal-plated polypropylene) types.

The power supply—see Fig. 6—is clearly in two parts. That for the digital section delivers ±5 V (B_1, IC_1, and IC_2). In that for the analogue section, rather more components are used, because it was thought important to give the left-hand and right-hand channel its own regulation. Bridge rectifier B_2 is followed, therefore, by two positive and two negative regulators. A 'star' earthing point obviates any problems with earth currents.

There is a separate 12 V supply, provided by D_1 and D_2, for the mute relays. The value of capacitor C_{29} has been kept small to ensure that the mute relays are de-energized the instant the power is switched off.

Each of the supplies uses its transformer. It is, of course, possible to use one with split secondaries, but that will have to be wound to order. In the prototypes, toroidal transformers were used, which keep the stray field to an absolute minimum. ■

The second and final part of this article, describing the construction of the converter, will be published in our September issue (there is no August issue).

PULSE GENERATOR

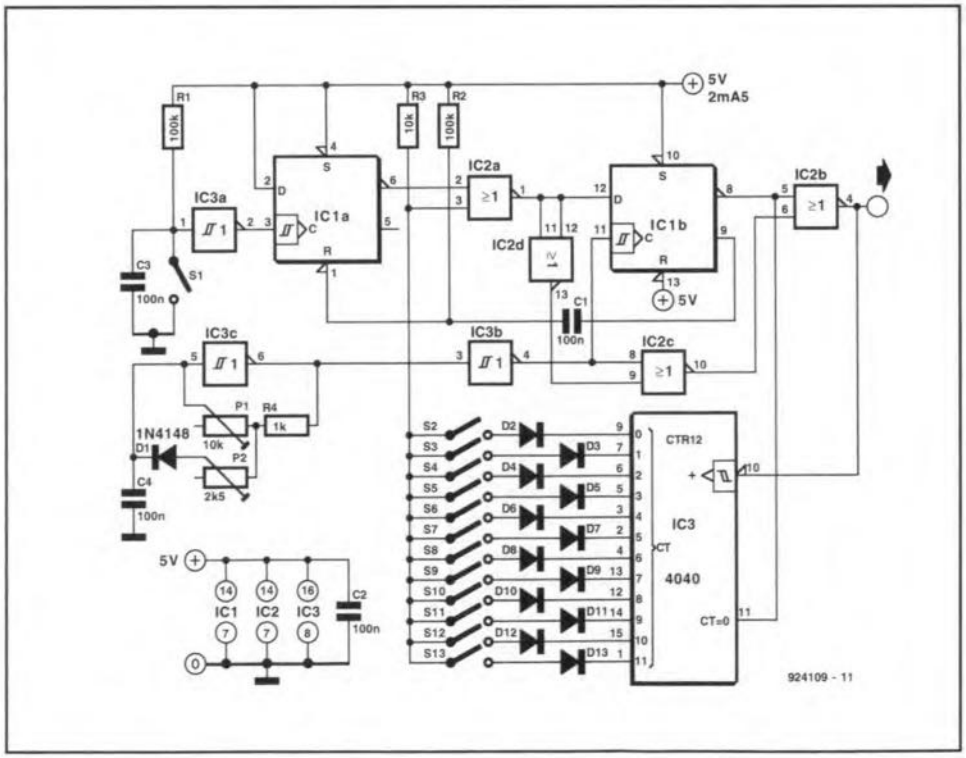
THIS pulse generator can provide up to to 12 pulses at its output, depending on the setting of hexadecimal switches S_2–S_{13}.

The (rectangular) pulses are generated by IC_{3c}; with circuit values as shown, their p.r.f. (pulse repetition frequency) is a few kHz.

The output of the generator is taken to one input of NOR gate IC_{2c} via buffer/inverter IC_{3b}.

When switch S_1 is operated, bistable IC_{1a} receives a clock pulse, whereupon a logic 1 is passed to the D input (pin 12) of IC_{1b} via IC_{2a}. The other input of IC_{2a} is low because counter IC_3 is disabled via its reset input. At the next leading clock transition (edge), the bistable is set, so that IC_3 and, via IC_{2b}, the pulse output are enabled.

When the relevant number of pulses has been output, junction R_3-S_2 goes high, whereupon the output of IC_{2a} goes low and IC_{1b} passes a logic 0 from its D input to pin 9 ($\overline{Q}$ output). IC_{1a} is reset via C_1, so that S_1 can be operated again, and the counter is reset via pin 8 of IC_{1b} ($\overline{Q}$ output). Also, pin 8 disables gate IC_{2b}, so that no more pulses can appear at the output.



The generator draws a current of only 2.5 mA.

(A.N. Other – 924109)

ELEMENTS OF PASSIVE ELECTRONIC COMPONENTS

PART 3: THE CAPACITOR

by Steve Knight, B.Sc.

THE history of the modern capacitor goes back to antiquity when the Greeks made a study of electrification of amber by friction. After that, very little more about the subject of electrostatics emerged until the middle of the eighteenth century when, in 1746, the Dutch physicist Pieter van Musschenbroek (1692–1761) discovered, by accident, the principle of the capacitor in the form of the celebrated Leyden jar. Having received a powerful electric shock from his experiments, arising from an attempt to electrify water in a bottle, van Musschenbroek confessed that he would not take such another shock 'for the kingdom of France'. Many modern experimenters have, no doubt, uttered words to the same effect when carelessly handling circuits boards containing charged capacitors.

We have seen in the previous parts of this article that inductance and inductive effects depend upon the magnetic field; here we shall see that capacitance and capacitive effects depend upon the electric field. The existence of an electric field depends itself on the presence of electric charges. When the charges are removed, the field vanishes. The nature of the field and the direction taken by the electric flux is a function of the magnitude of the charges and their distribution.

The fundamental electric charge, e, resides in the electron, which carries a charge of -1.6×10^{-19} coulomb (C). Electrons may be added to a body so as to give that body an excess of electronics; the body then exhibits a negative electrostatic charge. In the same way, electronics may be removed from a body, giving it a deficit of negative charges; the body is then positively charged. In normal circumstances, bodies have neither an excess nor a deficit of electrons and are uncharged, neutral, or at 'earth' potential. So the general mass of the earth is a permanently neutral body and materials may carry charges in the form of an excess or a deficit of electronics with respect to earth. There should be no confusion here with the 'excess' or 'deficit' of charge carriers in semiconductor materials, where the crystal remains electrically neutral.

As the Greeks established, without being aware of what they were handling, the removal from, or the addition to, a body of electrons may be accomplished by purely mechanical means, as when a piece of amber is rubbed with silk, or, more practically for our purposes today, by applying a potential difference between conducting materials.

A field of electric force, like a magnetic field, may be represented in magnitude and direction by drawing lines of force in the region surrounding the charged body or between charged bodies, the line densities being an indication of the field strength. The relationship between these convenient though imaginary lines and the field strength $\boldsymbol{E}$ (a vector) is that the tangent to a line at any point gives the direction of $\boldsymbol{E}$ at that point and the number of lines per unit cross-sectional area (that is, the flux density, D, in C m^{-2}) is proportional to the magnitude of $\boldsymbol{E}$. A number of typical and idealized fields for isolated and adjacent charges is shown in Fig. 1. Unlike the magnetic field, electric lines of force do not form closed loops. but are taken to emanate from positive charges and terminate on equal and opposite negative charge. When, therefore, a charged body is brought into proximity of an uncharged body, an induced charge of opposite sign appears on the near surface of the body, resulting from the line termination points. Hence, a net attraction is set up between the bodies because unbalanced forces act on the induced surface charges as illustrated in Fig. 2: a phenomenon known to the Greeks when their charged pieces of amber attracted wisps of straw.

It was believed at one time that a metallic body could not be given a charge by frictional means as could bodies of non-conducting or insulating materials; however, provided that the metal is supported or held by an insulating substance, such conductors can be charged just as well as anything else. In metals, only the negative charge is free to move; the positive charge is as immobile as it is in glass or any other insulator.

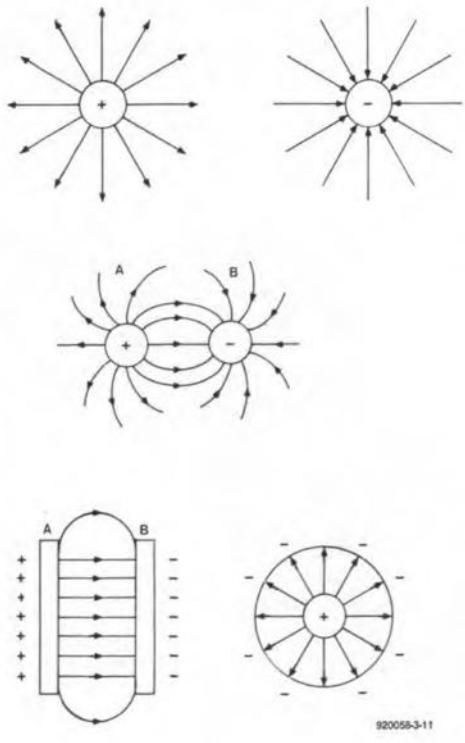


Fig. 1. Some typical electrostatic field configurations using the concept of lines of force.

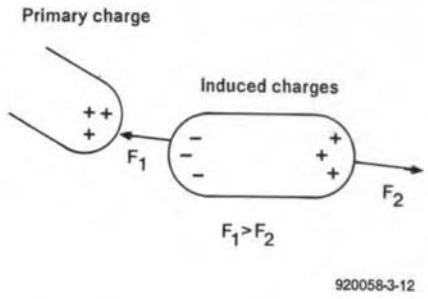


Fig. 2. A charged body attracts an uncharged body because unbalanced forces act on the induced charges disposition.

The electric field

To get a proper understanding of the phenomenon of capacitance, we need a proper appreciation of the field concept. In both magnetic and electric systems, energy is stored in the field, *not* in the component parts producing the field. Before Faraday's time, the force acting between charged particles was thought of as a direct and instantaneous interaction between the particles, and Faraday himself always thought of the field in terms of lines of force. This concept still provides us with a convenient way of visualizing field patterns as we have seen, but it is really necessary to think in terms of charge acting on a field or of a field acting on a charge, and *not* as charge acting upon charge as the action-at-a-distance concept would have us suppose. Look at Fig. 1c for a moment; suppose particle A carrying the positive charge suddenly moved to the left; how soon after this would the charge on particle B learn that A has moved and that the force of attraction it has so far experienced decreases? If action-at-a-distance were true, the information would be transmitted instantaneously to particle B, but this does not accord with commonplace experience. Moving charges in the aerial system of a radio transmitter, for example, establish an electromagnetic field and so influence electrons in a distant receiving aerial system, but only after a *finite* time, determined by the distance travelled and the speed of light.

When the flux density, $\boldsymbol{D}$, changes, the electric force $\boldsymbol{E}$ changes proportionally and there is a constant relationship for a field established in air: the ratio $\boldsymbol{D}/\boldsymbol{E}$ is designated ε_o. This is the *permittivity* of free space or the free space constant. Its value is found ex-

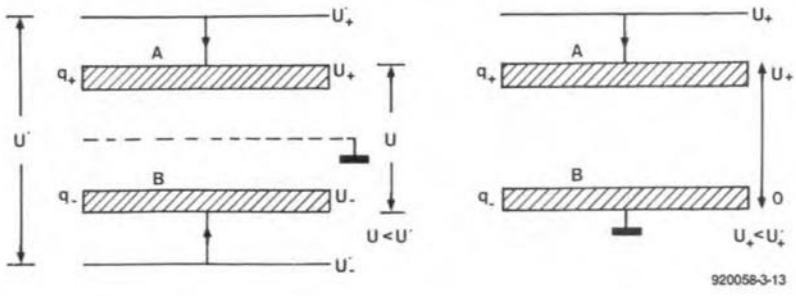


Fig. 3. The potential between conductors carrying equal charges falls as the conductors approach one another.

perimentally to be 8.85×10^{-12} F(arads) m^{-1}.

Capacity

There is a limit to the charge that may be placed upon a conductor. If an attempt is made to exceed this limit, a discharge will take place from the surface of the conductor to some nearby earthed or neutral point, sometimes as a spark or a fine corona or brush discharge into the surrounding air. Any conductor, therefore, has a certain ability or 'capacity' for holding a charge. Can we now obtain a practical definition of capacity and is it possible to increase the capacity of a given conductor so that more charge may be added before an 'overflow' occurs?

When a positive charge is added to a conductor, the potential of the conductor is raised relative to a neutral plane. This 'rise' in potential is measured in a negative sense for a negatively charged conductor; in both cases, the potential U is found to be proportional to the charge q coulombs; hence, $q=CU$, where C is a constant of proportionality. This constant, that is, the capacity of the conductor, is called the *capacitance*. The m.k.s. unit of capacitance is the coulomb/volt, more commonly called the *farad* (F), named in honour of Michael Faraday. Thus, one farad = one coulomb/volt; that is, 1 coulomb of charge raises the potential of unit capacitance by one volt. The farad is a very large unit, and in practice the microfarad, μF (10^{-6} F), the nanofarad, nF (10^{-9} F), and the picofarad, pF (10^{-12} F) are used, although memory back-up values of several farads are now commonplace.

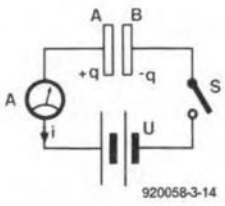


Fig. 4. Charging the basic capacitor.

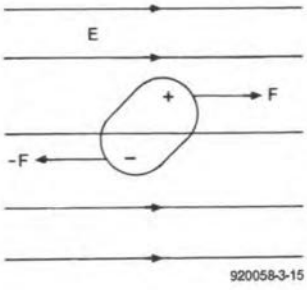


Fig. 5. Forces act on a molecular dipole and tend to align it with the electric field.

How might the capacity of an inductor be increased? What follows is true for conductors of any shape, but to make the explanation easier, it is assumed that a conductor in the form of an isolated metal plate, A, carries a positive charge, q_+ coulomb, giving it a positive potential. In Fig. 3a, this potential is represented by the line U'_+. The line marked U represents a neutral plane or earth line. Suppose a second metal plate, B, carrying a negative charge, q_- coulomb, also isolated, has a corresponding potential, U'_-, represented by the line U'_-. The potential difference between the plates is clearly $U'=U'_+-U'_-$ and this is proportional to the charge on *either* plate.

Let the two plates now approach each other; the charge on the plates will be unaffected, but what happens to their potentials? If a positive charge is brought near to an isolated conductor, the potential of that conductor will be lowered, since a negative charge will be induced on it; in the same way, the proximity of a negative charge will raise the potential. This, the potential of the positively charged plate A, will be lowered by the nearby presence of the negatively charged plate B from U'_+ to some lower value U_+. Similarly, the potential of plate B will be raised from $-U'_-$ to some higher value $-U_-$. These new potentials are shown in the figure: the changes are indicated by the vertical arrows.

The same effect can be produced if a single plate, carrying, say, a positive charge Q_+, is approached by an isolated neutral plate as shown in Fig. 3b. Lines of force from the charge on A will terminate on the inner surface of plate B and an induced negative charge will be established there. The inner plate surfaces now carry equal but opposite charges. The induced charge on B produces its own field and, in the same way as described above, the potential of A consequently falls. Hence, the 'capacity' of A has been effectively increased by the presence of plate B. We conclude that the potential difference between two conductors that carry constant, equal charges of opposite sign is reduced as the conductors are brought closer together.

Devices that operate on these principles are capacitors; perhaps their old name of 'condenser' was not so inappropriate when it is considered that the electric field is concentrated by such means and so made capable of storing additional electrostatic energy.

The parallel plate capacitor

The parallel plate is the most basic of all capacitor designs: all other varieties are simply adaptations of it. Suppose two parallel plates are connected into a circuit as shown in Fig. 4. Starting with plates A and B uncharged, let a voltage be applied by the closing of switch S. A positive charge $+q$ then appears on the left-hand plate and a negative charge $-q$ on the right-hand one, so that finally the potential difference between the plates is equal to the applied voltage, U. The plates are then charged.

For these charges to be established, there must have been a movement of electrons around the circuit; that is, a current must have flowed in the direction A to B for the time during which the equalization of the voltages was attained. This *displacement* current can be detected on an ammeter wired in series with the circuit. If the battery is switched off, the charge on the plates persists, as does the potential U across the plates. Thus, the capacitor stores electrical energy. It should be noticed particularly that q coulombs is the quantity of charge on *either* plate; it must not be taken as the net charge on the capacitor, which is *zero*.

If the plates are now connected together by a piece of wire, the capacitor will discharge; a momentary displacement current follows from plate B to plate A to restore the neutral condition of the plates and reduce the terminal voltage to zero. No current passes *through* the capacitor; there is simply a movement of electrons away from the positive plate and towards the negative plate; and these return in the opposite direction when the device is discharged.

Effect of a dielectric

When a slab of insulating material is placed in the space between the plates of a capacitor, it is found that the capacitance is increased. This comes about because the molecules of the dielectric, as the insulator is called, have what are known as electric *dipole moments* which may be permanent in some material and tend to align themselves with an applied electric field, as illustrated in Fig. 5. The dipoles have random orientations in the absence of an external field, but experience a torque tending to align them with the field when this is applied. Complete alignment does not occur, because of ther-

mal agitation of the molecules, but the alignment increases as the field is increased or the temperature falls. Molecules that do not have permanent dipole moments will, nevertheless, acquire them when subjected to an electric force. The field tends to separate the negative and positive charges on the molecule, so creating an induced dipole that will tend to alignment only when the field is present.

When a slab of dielectric is introduced between the plates of a capacitor, assumed to carry a fixed charge q, the effect of dipole alignment is to separate the *centre* of positive charge of the slab slightly from the *centre* of negative charge. The dielectric, although remaining electrically neutral, becomes polarized. The overall effect is the appearance of positive charges on one surface of the slab and of negative charges on the other. These charges must be equal in magnitude; within the slab itself, there is no displacement of electrons and no transfer of charge over large distances. As Fig. 6 shows, the induced surface charges will always be established in such a way that the electric field they themselves set up, $\boldsymbol{E}_1$, will oppose the applied field. The resultant field in the dielectric, $\boldsymbol{E}_2$, is then the (vector) sum of $\boldsymbol{E}$ (the applied field) and $\boldsymbol{E}_1$, and this is always smaller than $\boldsymbol{E}$. We conclude that, owing to the presence of a dielectric in a field, induced surface charges tend to weaken the original field. This weakening shows itself as a fall in the potential between the plates; hence, the capacitance, for a constant q, must be increased.

Faraday first investigated the effect of a dielectric on the capacitance of a conductor. In an experiment similar to that shown in Fig. 7, two capacitors were charged to the same potential, U, by the battery. Unlike the argument made earlier, in this system U does not change, so the charge q on the capacitor with the dielectric must increase above that on the air-spaced capacitor, which Faraday found was so. Thus, since q is greater for the same potential and $C=q/U$, the capacitance must increase through the introduction of a dielectric. If we give the capacitance with dielectric the symbol C_d and that without a dielectric C_a, the ratio C_d/C_a is called the dielectric constant or, more generally, the *relative permittivity*, ε_r. The dielectric constant is unity for air spacing (strictly, for a vacuum), which, as we have noted, has a free space permittivity ε_o. The *absolute permittivity* when a dielectric is used is $\varepsilon_o\varepsilon_r$. Hence, the capacitance of any capacitor can be expressed as $C=\varepsilon_o\varepsilon_r L$, where L depends on the form of construction and has the dimensions of length. For a parallel plate capacitor, L is A/d, where A is the plate area and d the plate separation.

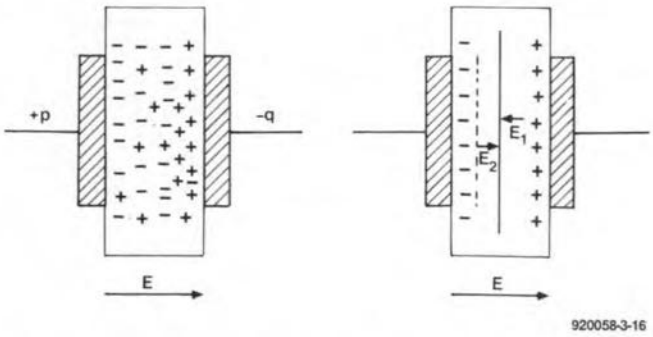


Fig. 6. (a) The applied field *E* separates the centre of +ve charge from that of –ve charge. (b) The surface charges set up a field E_1 which opposes the applied field *E*. The resultant field $E_2=E-E_1$ is thus weaker than *E*.

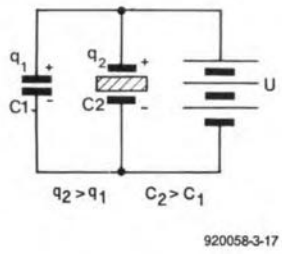


Fig.7. The principle of Faraday's experiment to show that a dielectric increases the capacitance.

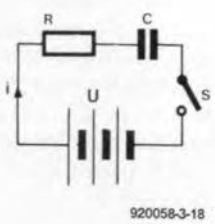
Energy and losses

When a capacitor is charged to potential U, energy is stored in the electric field established between the plates. When the capacitor is discharged, the field energy is returned to the external circuit in some way, often as a spark that generates heat and light. For a perfectly efficient capacitor, there would be no energy loss and all the charge put into the system would be returned by it. In a dielectric, work is done in turning the molecular dipoles, and if the capacitor is charged and discharged periodically, this process causes heat to be generated in the dielectric which represents energy loss; this loss can be represented as a small resistance in series (or a large resistance in parallel) with a loss-free component. It is usual to express such a loss in terms of the angle by which the lead of the current on the voltage falls short of 90°.

The energy stored in a capacitor is potential energy, which is dependent on the potential difference set up across the plates; in an inductor, it is comparable with kinetic energy associated with the movement of electrons in a wire. It is easily shown that the energy stored in a capacitance C is given by $CU^2/2$ joules.

Time constant

Since current is the rate of change of charge, $i=dq/dt$, the charge on a capacitor cannot change instantaneously, because that would require an infinite current and hence an infinite rate of change of voltage. This does not accord with experience. In effect, since the capacitance is constant, the voltage across a capacitor must momentarily remain the *same* before *and* after any abrupt change in the



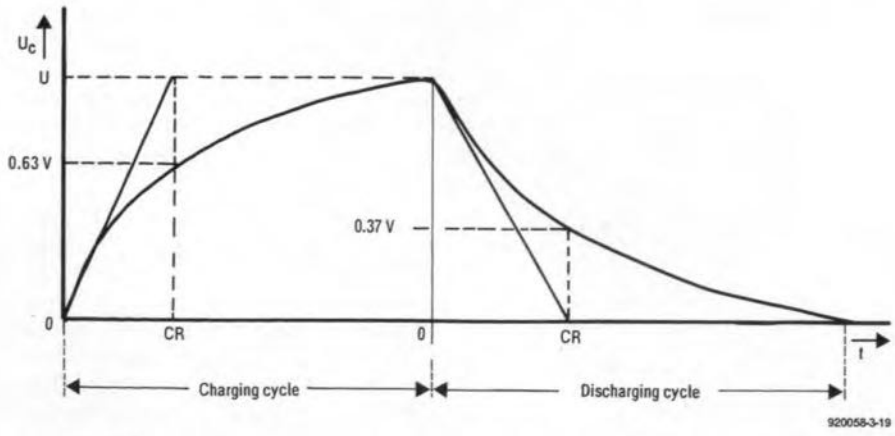


Fig. 8. The meaning of time constant for the charging and discharging of a capacitor through a resistor.

circuit conditions. This concept is of great value in predicting the behaviour of a circuit at some particular instant of time, such as the closing or opening of a switch. We can use it here in a very brief study of the capacitor as a timing element, where the charging cycle is restricted by the use of a series resistance—see Fig. 8.

The voltage across C cannot rise immediately to the level of the applied voltage, U, when switch S gets closed: in fact, it remains at zero. So, the capacitor behaves as an instantaneous short-circuit and the applied voltage appears across R. This situation cannot remain, however; C begins to charge with a consequent rise in its terminal voltage and the potential across R falls correspondingly. The charging current will, therefore, be reduced from its initial value of $i=U/R$ to $i=(U-U_c)/R$. That is, as the voltage across C rises, the current and the rate of charging falls. Since $dq=idt=CdU$, $i=CdU/dt$. At the onset of charging, the initial current, $i=U/R$; hence, $U/R=CdU/dt$, and the *initial* rate of rise of voltage is U/CR V s^{-1}. If this rate could continue unopposed, the voltage on C would reach its final value U in a time given by $t=U/(U/CR)=CR$ seconds as shown in Fig. 8. One important point arises here: if the charging current is kept constant, the charging curve will be linear. This fact is used in circuits where a voltage with a linear sawtooth waveform is required.

With the existing situation, of course, the voltage across C continually rises and opposes the supply voltage, thus making the charging cycle non-linear. At *any* particular instant, the capacitor still has to be charged $(U-U_c)$ volts, and if this in turn were to continue at a constant rate, the time for the completion of the charge would be $U-U_c/(U-U_c/CR)=CR$ seconds as before. Hence, at *any* point on the charging curve, the time remaining to complete the charge at a *linear* rate is CR seconds. In theory, then, the capacitor can never be charged completely.

Figure 8 shows the actual form of the charging curve which is exponential in form, just as the rise of current in an inductor was seen to be in the first part of this article.

The product CR has the dimensions of time, and it is not too difficult to show that in a time equal to CR seconds, the charge will have reached a level given by $U_c=0.63U$.

The curve also shows the discharge condition, assuming that the charged capacitor discharges through the same resistance. Again, if the initial rate of fall in the capacitor voltage were to continue at a constant rate, the cycle would be completed in CR seconds, and this would be true for any point on the curve. Notice that the level actually reached in CR seconds is 0.37 V.

The product CR is known as the *time constant* of the circuit and is a very important and fundamental aspect of capacitance principles. Note that the time constant is normally given the symbol τ, thus $\tau=CR$.

To summarize: the electronic age could not exists without capacitors and inductors. Both of these passi ve components are used in conjunction with each other and with other devices to produce tuned circuits, oscillatory systems, smoothing circuits, the transmission of signals and to provide time delays, to name but a few. Perhaps these brief studies will afford the 'passives' a little more respect than they usually get. ■

ACOUSTIC CRYSTAL TESTER

A CRYSTAL cannot be tested acoustically, unless, that is, its output is scaled down to the audio frequency range by a circuit as shown in the diagram.

A divider that is particularly suitable for this purpose is the Type 4060 CMOS IC. This circuit contains not only a 14-stage binary scaler, but also a complete oscillator.

The crystal to be tested is connected across the input terminals and S_2 set as indicated in the table. The crystal frequency is scaled down in IC_1 and, depending on the setting of S_2, one of the outputs of the 4060 drives transistor T_1 via R_2. The transitor, in turn, drives a small loudspeaker, LS_1. The power delivered to the speaker is limited by R_5 to prevent damaged eardrums.

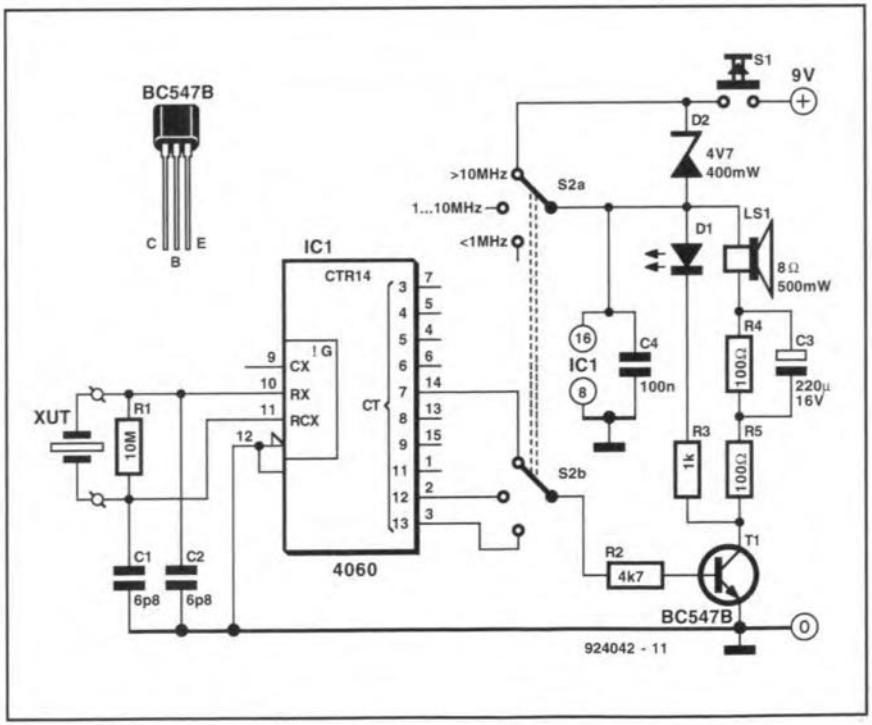
It is, of course, not possible to use one scale factor for all sorts of crystal, and that is why switch S_2 enables selection of one of three different factors. For crystals <1 Mhz, the scale factor is 128; for crystals in the range 1–10 MHz, the scale factor is 4096; and for crystals >10 Mhz, the scale factor is 8192.

Also, crystals operating above 10 MHz oscillate readily at somewhat higher voltages than low-frequency ones. That is why S_{2a} and D_2 lower the supply voltage to 4.7 V when crystals below 10 MHz are tested.

If a mains-operated power supply is preferred over a 9-V battery, a 12 V/50 mA one is recommended. Inn that case, D_2 must be a 6.8 V type.

[K.H. Lorenz – 924042]

Position of S_2	Crystal Frequency	Oscillator Frequency	Tone Frequency
<1 MHz	32.768 kHz 100 kHz	32.768 kHz 100 kHz	256 Hz 781 Hz
1–10 MHz	1 MHz 4 MHz 10 MHz	1 MHz 4 MHz 10 MHz	244 Hz 977 Hz 2 441 Hz
>10 MHz	27.145 MHz 48 MHz 100 MHz	9.048 MHz 16 MHz 20 MHz	1 105 Hz 1 953 Hz 2 441 Hz



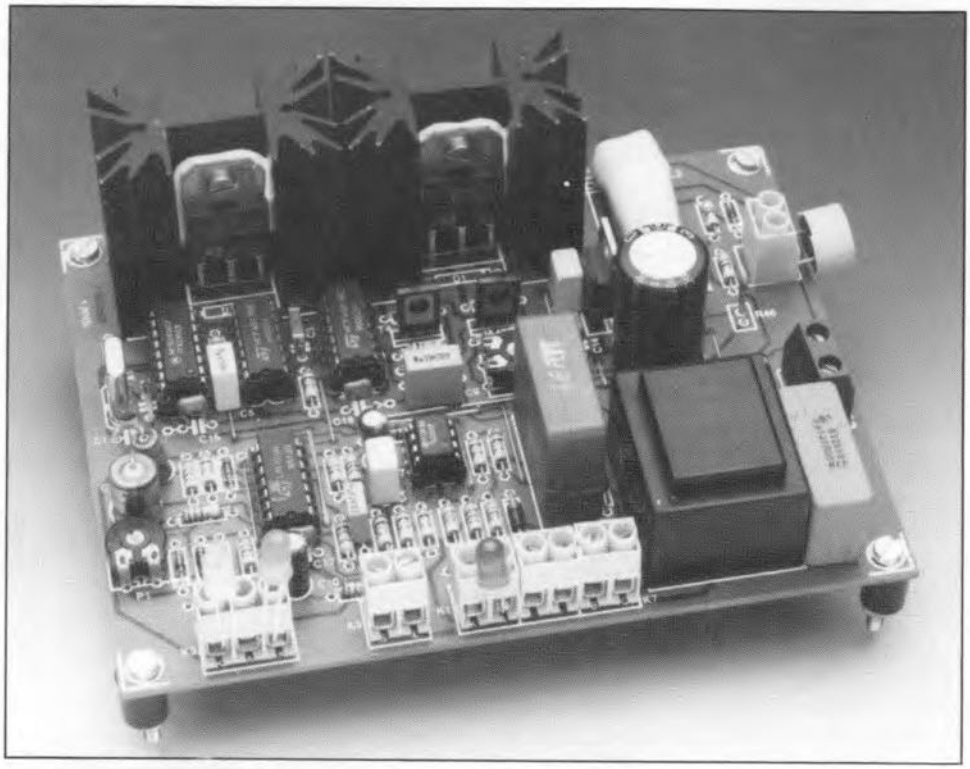
12 VDC-TO-240 VAC INVERTER

Design by N. Grimm

Many people intending to go on a camping or caravanning holiday will appreciate this 600 VA converter that provides a standard 240 V 50 Hz a.c. supply from a 12 V vehicle battery.

A perennial problem in the design of an inverter is the waveform of the output voltage. A sine wave is, of course, the ideal, but unfortunately the losses in the inverter are then unacceptably high. It is far better to design a rectangular waveform output for which the losses are much smaller. That in turn allows a compact design that can deliver a fairly high power. This has, however, the serious disadvantage that virtually all appliances that are to be powered by the inverter require a more or less sinusoidal supply.

In the present design, a compromise between these opposites has been reached: the output voltage has a trapezoidal waveform. This is near enough to a sine wave to enable standard domestic appliances to operate from the inverter and, moreover, it does not appreciably add to the cost or size of the unit. Repeatability and reliability were two important aspects of the design. Efficiency and control action from no-load to full-load conditions in the prototypes are excellent.



Design

The block diagram of the inverter is shown in Fig. 1. A power stage, connected to the battery via a polarity protection circuit, converts the battery voltage into a low-level alternating voltage, which is applied to the secondary winding of a mains transformer. The turns ratio of the transformer is such that across the primary winding an alternating voltage at a level of 240 V is generated.

A controller stage provides the necessary correcting voltage to the power stage. The controller receives information from a temperature monitor, an input-current limiting stage, and a quartz oscillator (clock).

The oscillator provides a stable 100 Hz signal to which the frequency of the output voltage is locked.

An optoisolator supplies part of the output voltage to a voltage regulator. If the optoisolator should fail, a small piezo buzzer warns that the voltage regulator is inoperative. The output of the regulator is applied to the controller.

The circuit

In the circuit diagram in Fig. 2, four modules, each containing four power transistors, make up the push-pull power stage of the inverter. The power transistors in each of the modules are connected in parallel via R_5–R_8 and R_{52}–R_{55}. The low-value resistors in the emitter circuits provide current feedback, which ensures near-equal currents through the transistors. Modules 1 and 2 form one branch of the push-pull power stage, and modules 3 and 4 the other. The four secondary windings of Tr_2 are connected to the collector circuits of the power transistors and to the positive terminal of the battery via relay contact Re_2. The power transistors alternately connect and disconnect the secondary windings to and from earth.

The control voltage for the power stages is derived from crystal oscillator IC_1. The

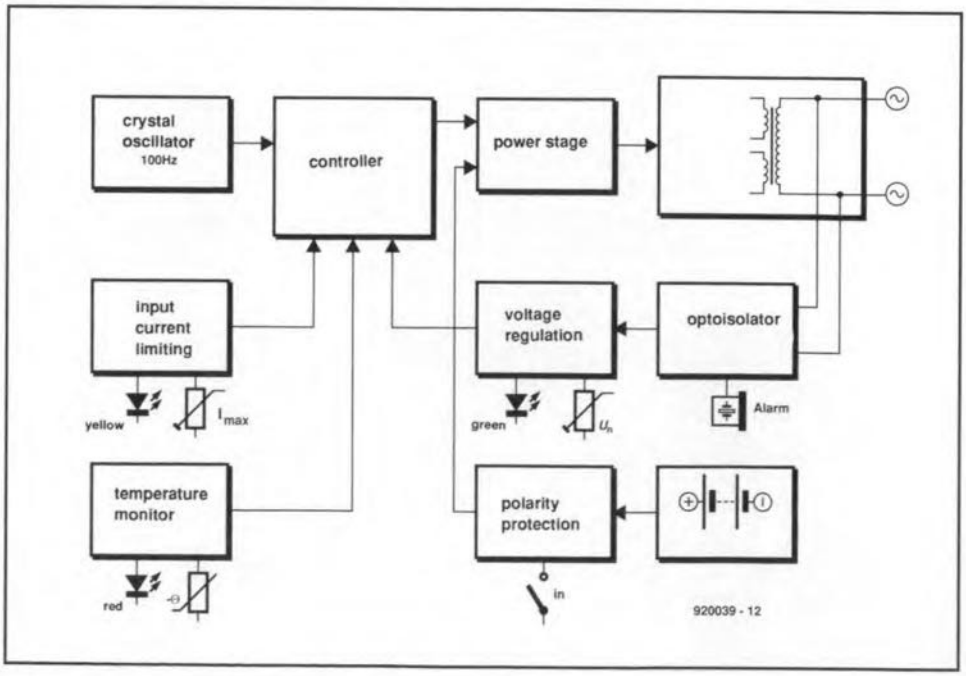


Fig. 1. Block diagram of the inverter.

crystal has a frequency of 3 2678 MHz, which is scaled down by the chip itself to a rectangular 200 Hz signal. Bistable IC_{2a} scales this down further to 100 Hz. The resulting 100 Hz signal is supplied to bistable IC_{2b}, which delivers two out-of-phase 50 Hz signals to its two complementary outputs.

The clock signals are applied to the bases of Type BD679 darlington transistors, T_2 and T_4, via AND gates IC_{3a}–IC_{3b} and IC_{3c}–IC_{3d} respectively. These transistors provide sufficient base current for drivers T_3 and T_5, each of which forms a darlington configuration with the power transistors in modules 1–2 and 3–4 respectively.

In this kind of configuration, it is essential that the drive signals for the two push-pull branches do not overlap. If that were to happen, all power transistors would conduct simultaneously, albeit for a very short time. This would, however, cause an unnec-

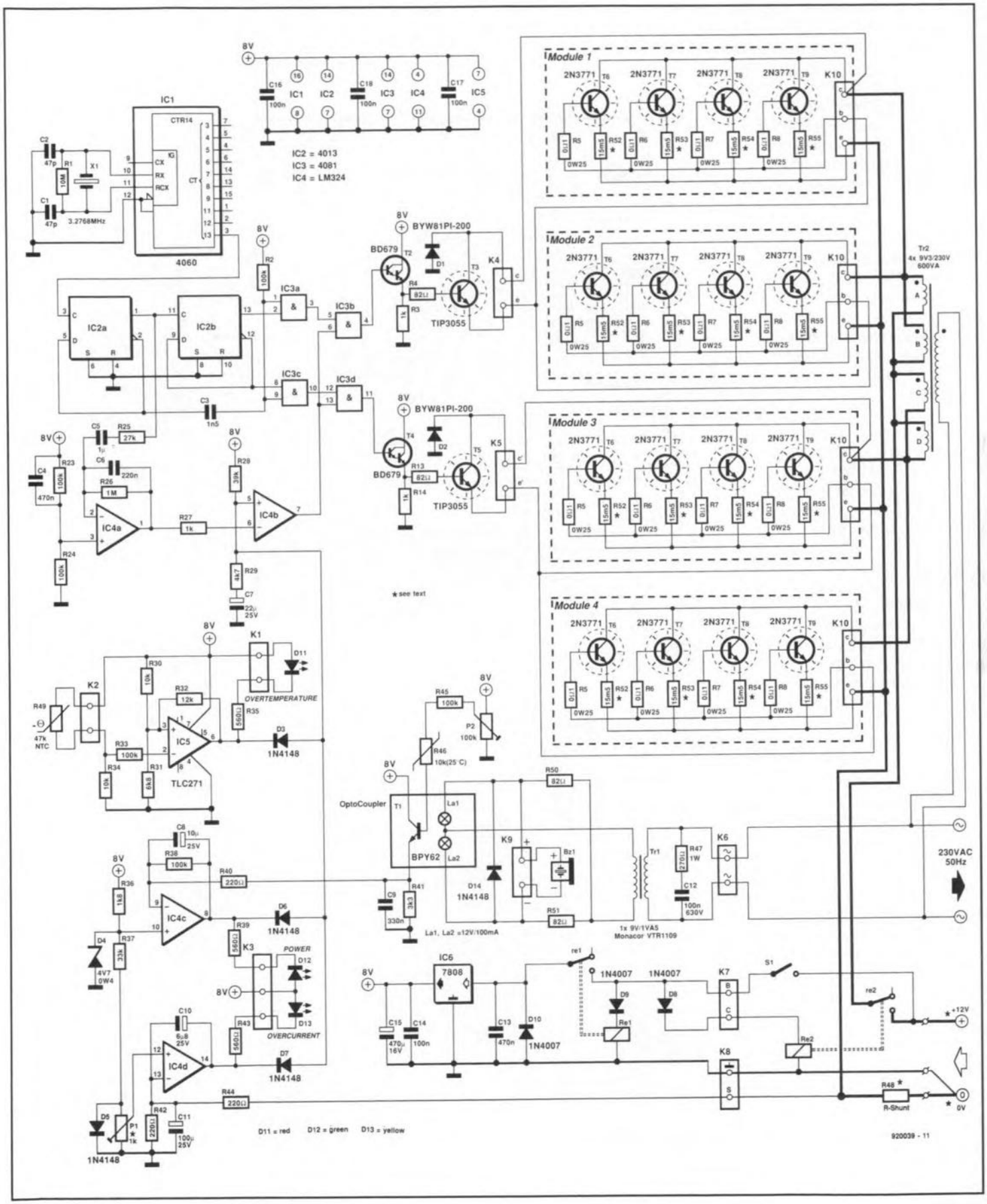


Fig. 2. Circuit diagram of the inverter.

essary drain on the battery, and also be a potential risk to the power transistors. This situation is obviated by shortening the clock pulses to about 0.1 ms by network R_2-C_3.

The control and protection functions are provided by opamps IC_4 and IC_5.

The 100 Hz output signal of IC_{2a} is applied to the inverting input (pin 2) of integrator IC_{4a}. The output of this opamp is a triangular waveform (pin 1).

The triangular waveform is compared by IC_{4b} with the signal at its non-inverting input (pin 5). That signal consists of three components that are OR-linked via D_3, D_6 and D_7.

The output (pin 7) of the comparator is a rectangular waveform, whose duty factor depends on the level of the voltage across R_{29}-C_7.

The clock provided by bistable IC_{2b} is combined with the output of the comparator by IC_{3b} and IC_{3d}.

If the width of the pulses provided by IC_{4b} is small, the push-pull output is switched on only relatively briefly, which results in a low inverter output. The greater the width of the pulses, the higher the inverter output will be.

The components of the signal at pin 5 of IC_{4b} are provided by temperature monitor IC_5, voltage regulator IC_{4c} and current limiter IC_{4d}.

The inverting input of IC_5 is fed with the voltage across an NTC (negative temperature coefficient) resistor R_{49}, which is mounted on one of the heat sinks for the power transistors. The non-inverting input is at a fixed potential provided by R_{30}-R_{31}. When, owing to a rising temperature, the value of R_{49} becomes low, the output (pin 6) of IC_5 toggles to near-earth potential, which is indicated by the lighting of D_{11}. Feedback resistor R_{32} provides a hysteresis of about 10 °C, so that IC_5 switches off at about 60 °C and switches on again at around 50 °C.

Because of its low output level, IC_5 pulls the non-inverting input of IC_{4b} to ground via D_3. This results in a lowering of the duty factor of the output signal of IC_{4b}, and this in turn reduces the mean current through the power transistors and, therefore, the output voltage of the inverter.

Voltage regulator IC_{4c} compares the reference voltage at pin 10, which is held steady by R_{36}-D_4, with the potential at its inverting input (pin 9). That potential is derived from the inverter output by optoisolator T_1-La_1-La_2. The light bulbs operate from a 9 V supply provided by Tr_1.

The base of phototransistor T_1 is at a temperature-dependent potential derived from the 8 V supply via P_2-R_{45}-R_{46}. When it receives a large light flux, the potential across R_{41} rises above the reference voltage at pin 10 of IC_{4c}, the output of that opamp drops and D_{12} lights. At the same time, the voltage at pin 6 of IC_{4b} drops, resulting in a lower duty factor and, consequently, a reduced output voltage. When the inverter output has dropped to a value that causes pin 9 of IC_{4c} to become more negative than pin 10, the inverter output rises again. The regulation is set with P_2 to obtain a stable 240 V output.

Piezo buzzer monitors the two light bulbs. In normal operation, there is no drop across it, but when one of the bulbs burns out, it is connected to the 9 V secondary of T_1 via R_{50} or R_{51} and sounds an alarm.

The control board is connected to the battery via a separate earth line. The current in that line is so small that for all practical purposes the earth potential of the board is the same as that of the battery. The output stages and Tr_2 are connected to the (earthed) battery terminal via R_{48}. This is, however, not a

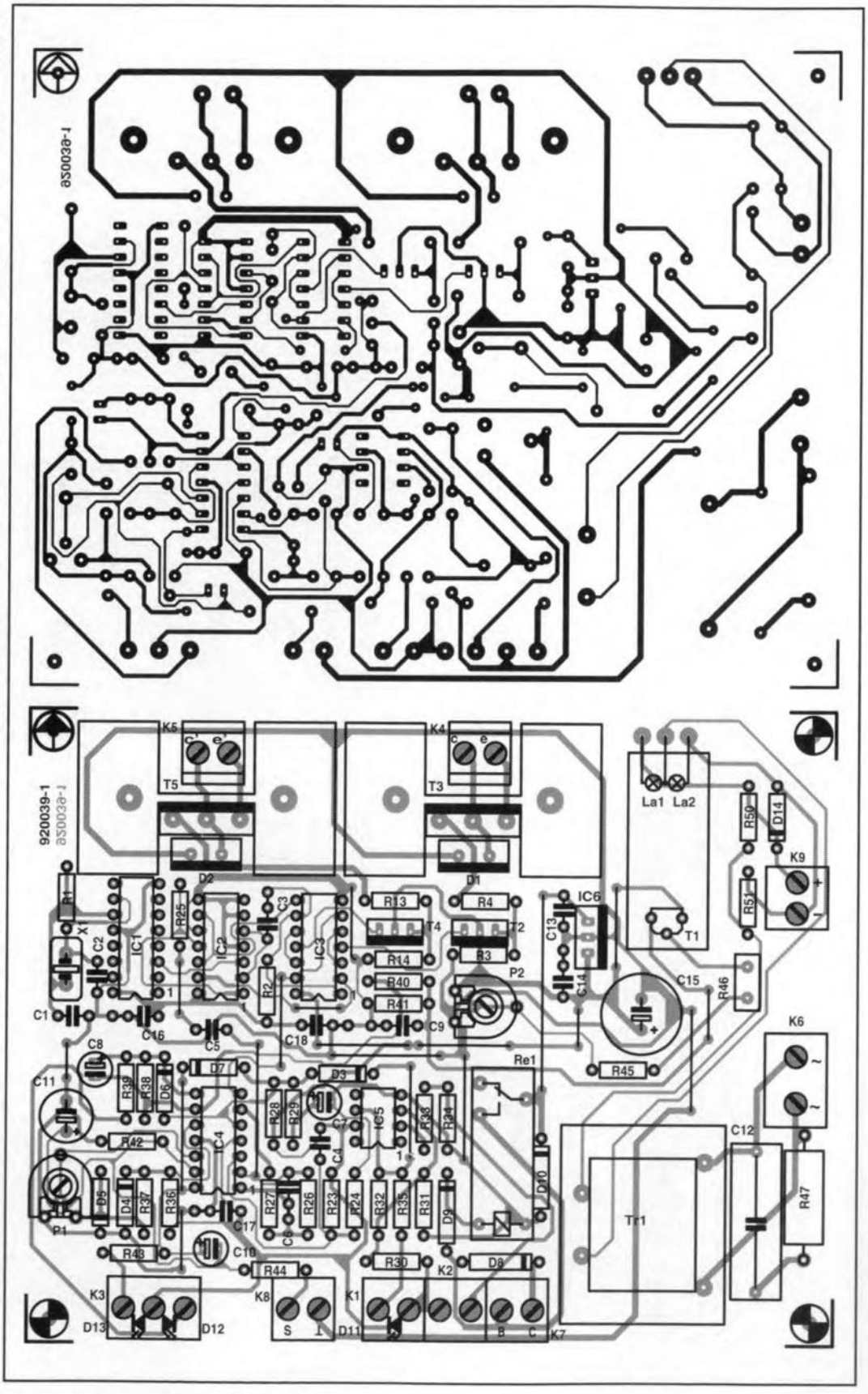


Fig. 3. The printed control circuit board.

PARTS LIST

Control circuit

Resistors:
R1 = 10 MΩ
R2, R23, R24, R33, R38, R45 = 100 kΩ
R3, R14, R27 = 1 kΩ
R4, R13, R50, R51 = 82 Ω
R25 = 27 kΩ
R26 = 1 MΩ
R28 = 39 kΩ
R29 = 4.7 kΩ
R30, R34 = 10 kΩ
R31 = 6.8 kΩ
R32 = 12 kΩ
R35, R39, R43 = 560 Ω
R36 = 1.8 kΩ
R37 = 33 kΩ
R40, R42, R44 = 220 Ω
R41 = 3.3 kΩ
R46 = 10 kΩ (at 25 °C) NTC
R47 = 270 Ω, 1 W
R48 = see text
R49 = 47 kΩ NTC
P1 = 1 kΩ multiturn preset
P2 = 100 kΩ multiturn preset

Capacitors:
C1, C2 = 47 pF
C3 = 1.5 nF
C4, C13 = 470 nF
C5 = 1 µF
C6 = 220 nF
C7 = 22 µF, 25 V, upright
C8 = 10 µF, 25 V, upright
C9 = 330 nF
C10 = 6.8 µF, 25 V, upright
C11 = 100 µF, 25 V, upright
C12 = 100 nF, 630 V
C14, C16, C17, C18 = 100 nF
C15 = 470 µF, 16 V, upright

Semiconductors:
D1, D2 = BYW81P1-200 (SGS Thomson)
D3, D5–D7, D14 = 1N4148
D4 = 4.7 V, 400 mW, zener
D8–D10 = 1N4007
D11 = 5 mm LED, red
D12 = 5 mm Led, green
D13 = 5mm LED, yellow
T1 = BPY62/2
T2, T4 = BD679
T3, T5 = TIP3055
IC1 = 4060
IC2 = 4013
IC3 = 4081
IC4 = LM324
IC5 = TLC271
IC6 = 7808

Miscellaneous:
La1, La2 = telephone bulb, 12 V, 100 mA
K1, K2, K3, K4, K5, K7, K8, K9 = 2-way spring-loaded PCB terminal board, 5 mm grid
K3 = 3-way spring-loaded PCB terminal board, 5 mm grid
K6 = 2-way spring-loaded PCB terminal board, 7.5 mm grid
S1 = on/off switch, 2 A
X1 = crystal, 3.2768 MHz
Re1 = 12 V relay, contact rating 8 A
Re2 = 12 V relay, contact rating 70 A
Bz1 = 5 V d.c. buzzer
Tr1 = secondary 9 V, 1.5 A (Monacor)
Tr2 = primary 4×9.3 V, 50–60 Hz; secondary 240 V*
2× heat sink Type 129/37.5 SA†
Enclosure 165×440×350 mm
PCB Type 920039-1
Front panel foil Type 920038F

Power circuit (for one module)

Resistors:
R52–R55 = made from 0.433 Ω/m resistance wire (see text)
R5–R8 = 0.1 Ω, 3 W

Semiconductors:
T6–T9 = 2N3771

Miscellaneous:
K10 = 3-way flat-cable connector for PCB mounting
Heat sink Type SK85/75/SA†
Heat sink Type WP40/30/SA†, 1000 mm long (see text)
PCB Type 920038-2

† Available from Dau Ltd, 70–75, Barnham Road, Barnham PO22 0ES; Phone (0234) 553031

*Available from Amplimo BV, Vossenbrinkweg 1; 7491 DA Delden, The Netherlands; Phone 05407 62024; Fax 05407 63132

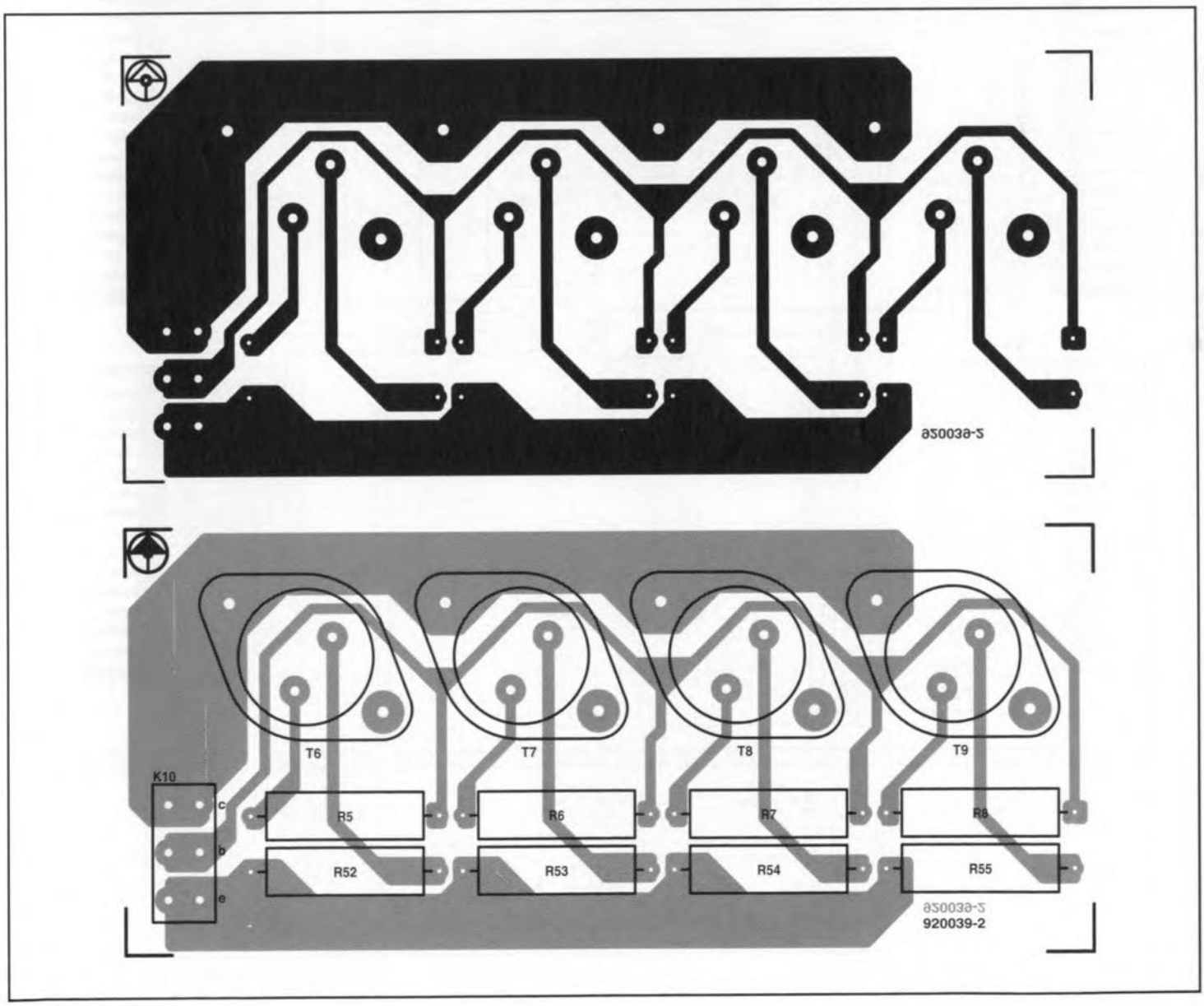


Fig. 4. The printed power circuit board.

resistor, but represents the resistance of the connecting cables. The (load-dependent) drop across this resistance ensures that the potential at the inverting input (pin 13) of IC_{4d} is positive with respect to earth. The voltage level at the non-inverting input (pin 12) is preset with P_1. When the drop across R_{48} exceeds the level at pin 12, IC_{4d} changes state, whereupon its output (pin 14) pulls pin 5 of IC_{4b} to ground via D_7. That results in a lowering of the duty factor and, consequently, a drop in the inverter output. This situation is indicated by the lighting of D_{13}.

Polarity protection is provided by relays Re_1 and Re_2 and diodes D_8 and D_9. The inverter can be switched on by S_1 only if the battery is connected with correct polarity.

Finally, IC_6 and C_{13}–C_{15} provide traditional regulation of the power supply for the control board.

Construction

The inverter is built on five PCBs: one for the control, monitor and regulation stages—see Fig. 3, and four for the power stages: one for each module—see Fig. 4.

Populating the control board is straightforward. Driver transistors T_3 and T_5 must be fitted on a suitable heat sink as shown in the parts list, but IC_6 does not need one. Sockets should be used for all ICs.

The optoisolator is constructed from a length of pipe of suitable, but not too large, diameter, into which the phototransistor and the two 12 V (telephone) light bulbs are fit-

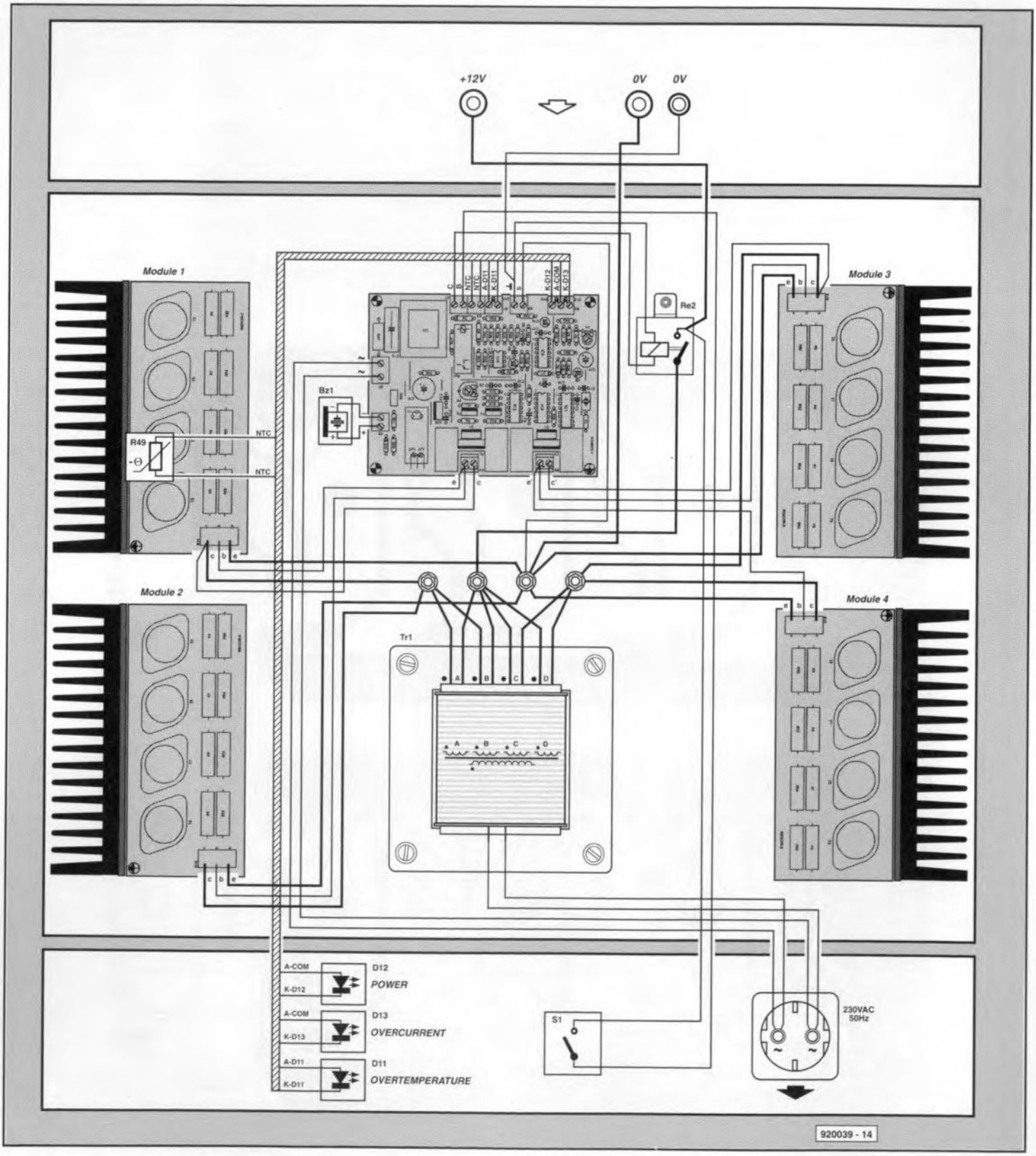


Fig. 5. Wiring diagram of the inverter.

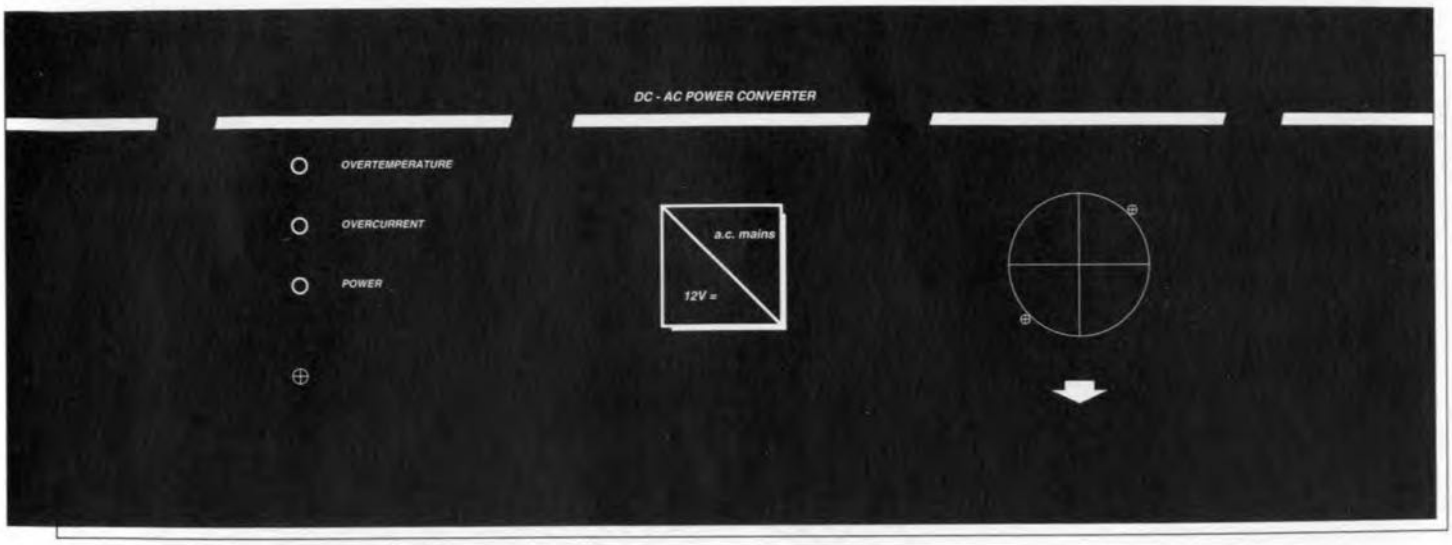


Fig. 6. A self-adhesive foil for the front panel is available through our Readers' services.

ted at either side. When the connecting wires of these components have been taken outside, the pipe must be sealed light-tight.

Transformer Tr_2 is a special type that may have to be made to order, although it is available from certain retailers. It is not cheap: of the order of £75–£80.

Each of the four power boards is designed for use with an angle-profiled heat sink, for instance, that shown in the parts list, that must be sawn to the required length of 16 cm. The necessary holes are best drilled in it by using the a photocopy of the board as a template. The power transistors are mounted on it with insulating washers, non-metallic screws, nuts and washers, and a good helping of heat conducting paste, before the board and heat sink sink are fastened together.

Power resistors R_{52}–R_{55} consist of a 50 mm (2 in) length of resistance wire, whose ends must be cleaned with wire wool and bent at right angles. Solder them on to the board so that they are a few millimetres above the surface.

Boards and power stages are best interconnected with the use of bullet plugs and sockets as used in vehicle wiring.

Wiring to the power transistors should be flexible and have a cross-sectional area of not less than 2.5 mm². The sixteen wires to the emitters and those to the collectors should preferable have the same length.

The inverter should be connected to the battery with starter cable of cross-sectional area not less than 10 mm², but preferably 16 mm².

Testing

The control board is best tested before it is assembled with the remainder of the inverter with the use of a 12 V battery or laboratory power supply. Connect the +ve line to K_7B and the –ve line to K_8. With an oscilloscope or voltmeter, check the voltages at the output of drivers T_3 and T_5 (K_4 and K_5 respectively). After power-on, the duty factor of this waveform should change slowly to 1:1.

Next, apply a variable direct voltage across the secondary of Tr_1. When the level of that voltage is raised to about 6–8 V, the effect of the voltage regulation on the duty factor should be quite clear.

For the remainder of the tests, it is better not to use a power supply, but a car battery. Also, take care with using a multimeter: its 20 A d.c. range may be overloaded at even low loading of the inverter.

Connect a 100 W light bulb to the output socket of the inverter. A few seconds after power-on, this should attain maximum brightness. Adjust P_2 until it has the same brightness as when it is connected to the mains. It is, of course, also possible to carry out this adjustment with the use of a moving-iron voltmeter. Note that moving-coil and digital voltmeters are not suitable. Recheck the output voltage after the inverter has been on for about 10 minutes. If it has risen by more than 3–5 V, replace R_{46} by a 5 k (25 °C) type.

The current limiting must be set after the inverter has been loaded with six 100 W light bulbs in parallel. Adjust P_1 such that current limiting just begins. If the inverter is to be used at high loads regularly, P_2 should be re-adjusted accordingly. The inverter can deliver up to 800–1000 W for short periods, provided the battery is capable of this. If the inverter is to be used in high ambient temperatures, a cooling fan should be added.

Under no-load conditions and operating from a well-charged 12-V battery, the inverter draws a current of about 1 A; with a 100 W load, the drain is around 10 A; with a 300 W load, the current is some 30 A; and at full load, the drain is around 80 A—a current that most car batteries cannot deliver for long periods. Apart from the fact that the battery gets hot, its efficiency drops sharply. For instance, an 80 Ah battery delivering 40 A has an effective capacity of only 60% of its rated capacity.

It is, of course, possible to operate from a 24-V power source (battery or solar cells, for instance), when all currents mentioned will be halved. The changes necessary to do this are: (a) the primary of Tr_2 should be rated at 21 V; (b) the power transistors should be Type 2N3772; and (c) the relays should be 24-V types. Furthermore, it would then be prudent to fit IC_6 on a small heat sink.

Efficiency

A variety of tests, carried out on the author's prototype operating from a 12-V battery, showed that the efficiency varied from 68% to nearly 75% when the battery voltage and load ranged from 11.3 V and 970 W to 12.5 V and 25 W.

pared by IC_{4b} with the signal at its non-inverting input (pin 5). That signal consists of three components that are OR-linked via D_3, D_6 and D_7.

The output (pin 7) of the comparator is a rectangular waveform, whose duty factor depends on the level of the voltage across R_{29}-C_7.

The clock provided by bistable IC_{2b} is combined with the output of the comparator by IC_{3b} and IC_{3d}.

If the width of the pulses provided by IC_{4b} is small, the push-pull output is switched on only relatively briefly, which results in a low inverter output. The greater the width of the pulses, the higher the inverter output will be.

The components of the signal at pin 5 of IC_{4b} are provided by temperature monitor IC_5, voltage regulator IC_{4c} and current limiter IC_{4d}.

The inverting input of IC_5 is fed with the voltage across an NTC (negative temperature coefficient) resistor R_{49}, which is mounted on one of the heat sinks for the power transistors. The non-inverting input is at a fixed potential provided by R_{30}-R_{31}. When, owing to a rising temperature, the value of R_{49} becomes low, the output (pin 6) of IC_5 toggles to near-earth potential, which is indicated by the lighting of D_{11}. Feedback resistor R_{32} provides a hysteresis of about 10 °C, so that IC_5 switches off at about 60 °C and switches on again at around 50 °C.

Because of its low output level, IC_5 pulls the non-inverting input of IC_{4b} to ground via D_3. This results in a lowering of the duty factor of the output signal of IC_{4b}, and this in turn reduces the mean current through the power transistors and, therefore, the output voltage of the inverter.

Voltage regulator IC_{4c} compares the reference voltage at pin 10, which is held steady by R_{36}-D_4, with the potential at its inverting input (pin 9). That potential is derived from the inverter output by optoisolator T_1-La_1-La_2. The light bulbs operate from a 9 V supply provided by Tr_1.

The base of phototransistor T_1 is at a temperature-dependent potential derived from the 8 V supply via P_2-R_{45}-R_{46}. When it receives a large light flux, the potential across R_{41} rises above the reference voltage at pin 10 of IC_{4c}, the output of that opamp drops and D_{12} lights. At the same

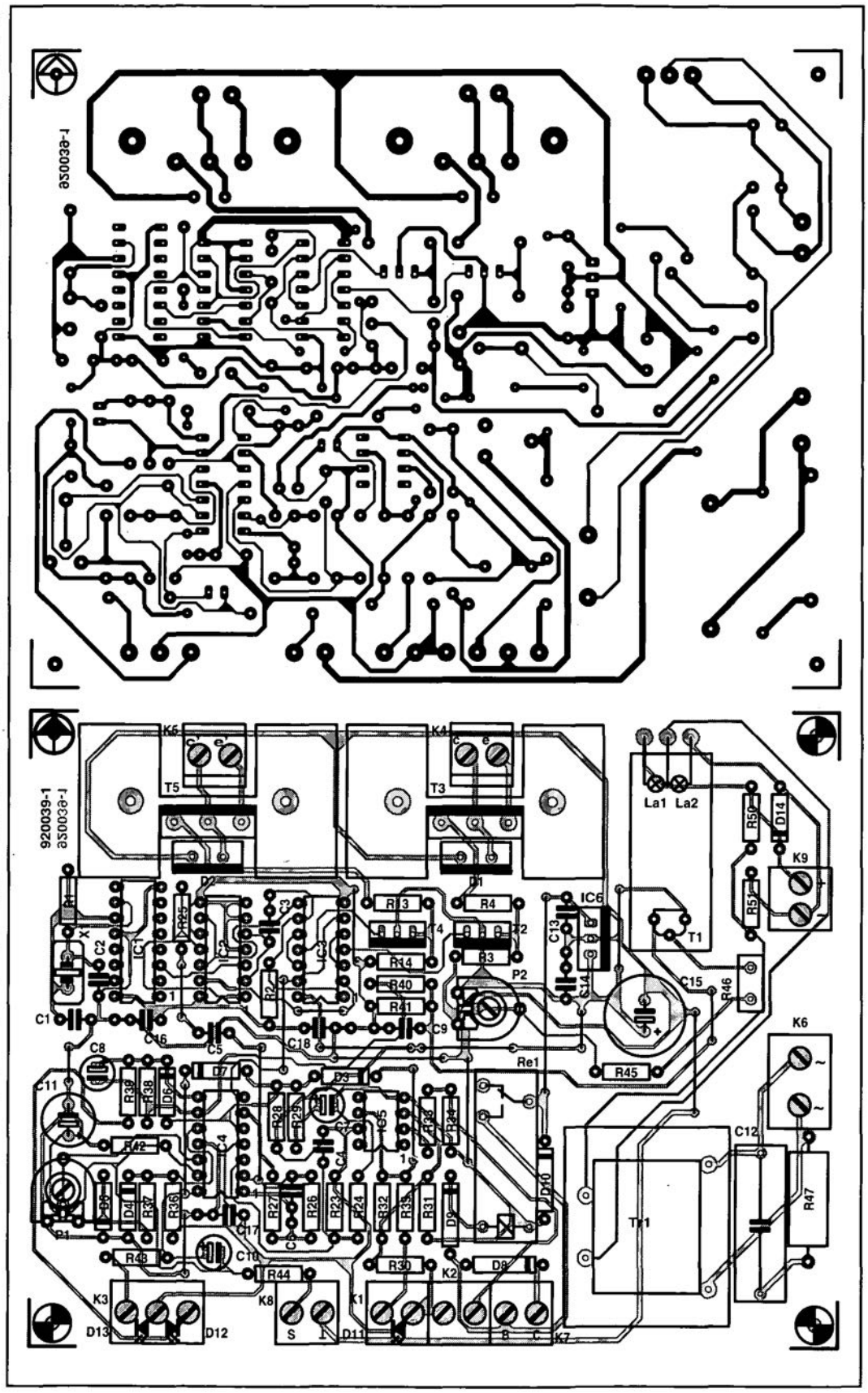


Fig. 3. The printed control circuit board.

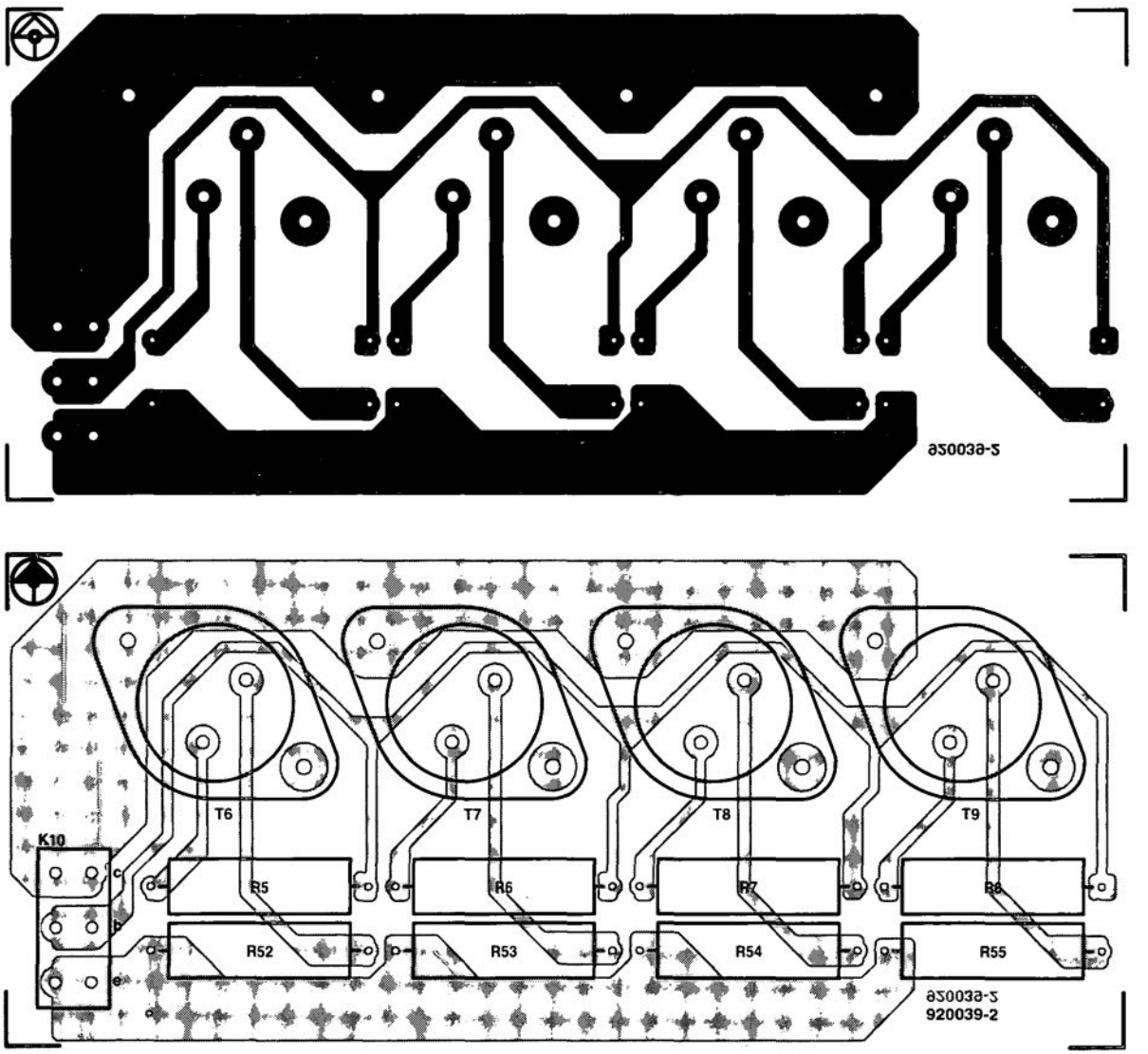


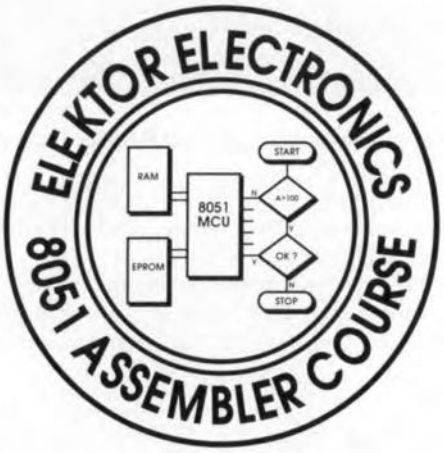
Fig. 4. The printed power circuit board.

8051/8032 ASSEMBLER COURSE

PART 5: ARITHMETIC INSTRUCTIONS

By Dr. M. Ohsmann

This instalment of the course is devoted to arithmetic operations, which are used in nearly every program, however small. In addition, some programming techniques will be discussed to show how simple calculations can be performed on the basis of the arithmetic instructions. Finally, two example programs are given that take the theory into practice: a capacitance meter and a noise generator.



Addition

The 8051 family of microcontrollers has the following instruction to add two 8-bit values (bytes):

```
ADD A,BYTE-OPERAND    ;add BYTE-OPERAND to accu contents
```

The result of the above instruction is left in the accumulator. The carry bit (CY, sometimes also referred to as C) is set if there is a carry out from bit 7, and cleared otherwise. When adding unsigned integers in the range 0 to 255, a set carry flag indicates that an overflow occurred.

The auxiliary carry (AC) flag, used for BCD number adding, is set if there is a carry out from bit 3, and cleared otherwise. The AC flag is used by the DA A instruction discussed further on.

The overflow (OV) flag is set if there is a carry out of bit 6, but not out of bit 7, or a carry out of bit 7, but not bit 6; otherwise OV is cleared. This flag allows an overflow to be detected when adding two signed integers in the range −128 to +127.

The meaning of the flags depends on whether the bytes involved are unsigned integers, signed integers, or BCD numbers. The difference between these three requires a short discussion, given below.

Number notation

1. Unsigned numbers

These are all numbers that can be written with the aid of a sequence of weighted binary values 2^n, where n is 1, 2, 4, 8, 16, etc.:

128×bit7 + 64×bit6 + … +4×bit2 + 2×bit1 + 1×bit0

In this way, a byte (eight bit positions) can be used to represent all unsigned values between 0 and 255.

2. BCD numbers

The BCD (binary coded decimal) number notation is based on indicating the left and right 4-bit groups (nibbles) contained in a byte as binary coded decimal numbers. The advantage of this notation is that it is simple to output. However, it also has a disadvantage: binary addition and subtraction can not be used just like that on BCD numbers, since additional corrections ('decimal adjustments') are required. The DA A instruction is capable of performing these corrections, for which it uses the AC flag.

3. Signed numbers

The world is, unfortunately, not completely positive. Many computer applications require the use of negative values, which forces us to think of ways to add the minus sign to a number. In computer number notation, this is usually done as follows for the range −128 to +127: if the number to be represented, x, is positive or nought, it is simply written as a byte without a sign. If x is negative (and has an absolute value smaller than or equal to 128), it is represented as (256+x), i.e., the value lies between 128 and 255. This means that bit 7 is set to indicate that the number is negative. To be able to output a negative number, the value has to be formed first, so that the new (then positive) number can be output with a minus sign in front of it. Negative numbers are also treated separately with multiplications and divisions.

Table 1 shows some examples of bit patterns that represent different numbers.

4. Large numbers

It often happens that the eight bit positions of a byte are not sufficient to represent all numerical values needed to achieve a certain accuracy. 16-bit values, for instance, are represented by two bytes; 32-bit values by four bytes, and so on. The bytes that form a 16-bit or 32-bit number are kept together as a group stored in successive memory locations. In this course, the lowest order byte is always stored at the lowest address. The bytes stored in the next higher locations are either signed, unsigned or BCD numbers. When two bytes are used to represent numbers, the following 16-bit ranges are available:

Table 1

Binary	Hex	non-signed	signed	BCD number
00000000	00	0	0	0
00000001	01	1	1	1
00000010	02	2	2	2
00010001	11	17	17	11
00100101	25	37	37	25
11111111	FF	255	−1	not defined
10000000	80	128	−128	80
01111111	7F	127	127	not defined

Unsigned: 0 to 65535
Signed: −32768 to +32767
BCD: 0 to 9999

Table 2 shows a few examples.

Adding with carry

If 16-bit or 32-bit numbers are to be added, it is required that a carry resulting from a byte position be taken into account when the next byte is added. This is achieved with the instruction

```
ADDC A,BYTE-OPERAND   ;add operand+CY to A
```

The result of this instruction is left in the accumulator. The following program example adds a number NMBR2 to a 16-bit number NMBR1, which is contained in RAM:

```
MOV   A,NMBR1      ;fetch LS byte of
                    NMBR1
ADD   A,NMBR2      ;add LS byte of
                    NMBR2
MOV   NMBR1,A      ;store result
MOV   A,NMBR1+1    ;fetch next byte of
                    NMBR1
ADDC  A,NMBR2+1    ;add byte, incl.
                    previous carry
MOV   NMBR1+1,A    ;store result
```

BCD correction

To obtain a BCD number as the result of adding two BCD numbers, the instruction

```
DA    A            ;decimal adjust
```

where DA A stands for decimal adjust accumulator for addition. DA A is executed immediately after the addition. Six is added to the accumulator if the value of the low-order nibble of A is greater than 9, or if the AC flag is set. This produces the proper BCD digit in the low-order nibble. The CY flag is set if this adjustment produces a carry out, which propagates through all higher-order bit positions. Next, we can check if the CY flag is set, or if the value of the higher-order nibble is greater than 9. If either of these conditions is met, six is added to the higher-order nibble. If, again, a carry out is produced, the CY flag is set, signalling that the result of the previous ADD or ADDC instruction is greater than 99 after the DA instruction. An example:

```
                    ;Addition of 99 and 11
MOV A,#11H          ;BCD value 11 to accu      00010001B   11
ADD A,#99H          ;+ BCD value 99 gives     +10011001B   99
                    ;not a BCD value =         10101010B   AA
DA  A               ;gives                    000010000B + carry
                    ;equals BCD               1 00010000   110
```

After the DA A instruction, the CY flag again signals a carry, which means that the BCD value is 100.

Subtraction

The MCS-51 instruction set has only one instruction for subtraction:

```
SUBB A,BYTE-OPERAND   ;subtract OPERAND+CY from A
```

If the status of the carry (borrow) bit is not known before starting a subtraction, it should be cleared by a CLR C instruction.

Comparison

The subtraction instruction has a further, important, application in the comparison of two values. This involves use of the CY (borrow) flag, which is set when a value y is subtracted from a value x, where y is greater than x. So, to check if a number y is greater than x, program $x<y$, and subsequently test the carry flag:

```
MOV   A,x          ;fetch x from
                    internal RAM
CLR   C            ;clear carry
SUBB  A,y          ;form x−y
JC    GREATER      ;jump if y>x
```

In this example, both x and y are taken to be unsigned integers. A comparison between two signed integers is a little more complex.

Table 2

Byte at address (hexadecimal)		hex	non-signed	signed	BCD
m+1	m				
00	00	0000	0	0	0
12	34	1234	4660	4660	1234
0A	BC	0ABC	2748	2748	not defined
80	00	8000	32768	−2768	8000
FF	FF	FFFF	65535	−1	not defined

Multiplication and division

The 8051 features an auxiliary accumulator, referred to as register B, and located at SFR address 0F0H. It is used for multiplication and division of unsigned 8-bit numbers. The relevant instructions are

```
MUL   AB           ;multiply A and B
DIV   AB           ;divide A by B
```

where A is contents of the accumulator contents, and B that of register B.

The result of the MUL instruction is that the low-order byte of the 16-bit product is left in the accumulator, and the high-order byte in register B. If the product is greater than 255, the overflow (OV) flag is set; otherwise it is cleared.

The result of the DIV instruction is that the accumulator receives the integer part of the quotient, while the integer part of the remainder is stored in register B. Both the carry and the overflow flags are cleared. Only if B contained 00, the overflow flag is set to indicate a division by zero.

The power of the MUL and DIV instructions offered by MCS-51 devices is limited by the fact that they do not allow direct 16×16-bit multiplication, nor division of a 16-bit number by an 8-bit number. Later, enhanced, versions of the 8051, like Siemens' 80537, have much more powerful multiplication and division instructions.

To compensate the 'lack of arithmetic power' of the 8051, the course monitor program, EMON51, offers a number of subroutines that may be used to perform 16×16-bit multiplications with 32-bit results. Simply study the relevant sections of EMON51.LST to see how this is done. The monitor is also capable of doing 32-bit/16-bit divisions.

Capacitance measurement using the V24 port

The practical use of the above arithmetic instructions will be illustrated by an example. We have in mind a capacitance meter that transmits the value of an unknown capacitor to the terminal (display) via the V24 serial interface on the 80C32 SBC. Interestingly, the measurement prin-

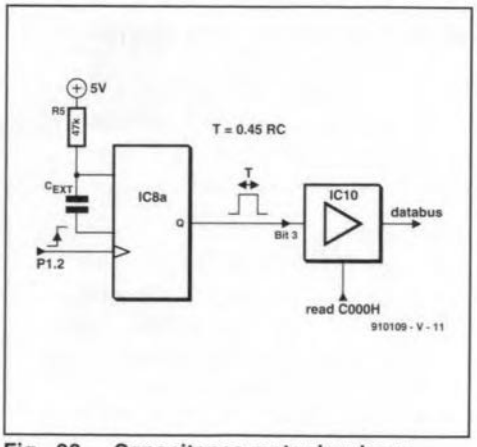


Fig. 22. Capacitance meter hardware.

ciple adopted allows resistance and time measurement also.

The hardware (contained on the SBC extension board) is shown in Fig. 22. The operation of the capacitance meter is both classic and simple: first, monostable IC_{8a} is triggered by the program. Next, the program measures the monostable period, i.e., the time that elapses between the triggering instant and the instant the Q output of IC_{8a} toggles. The measured time is converted into an equivalent capacitance value, and subsequently sent to the display. What sort of program is required to realize such an instrument?

1. Time measurement

The monostable time is measured by a 16-bit number, MTIME. With reference to the listing in Fig. 24, each measurement starts with resetting MTIME to 0 (label lp1; lines 20 and 21). Next, the monostable trigger pulse (positive edge) is output via port line P1.2. The loop that starts at label lpp lengthens the start pulse a little, to allow some recovery time for the monostable before a new trigger action.

After sending the trigger pulse, the program enters the time measurement loop, marked by the label MLP. The program checks if the monostable is still triggered by monitoring bit 3 of RAM address 0C00H. If so, the variable MTIME is increased by one. If not, the measurement is finished, and the program jumps to the label ENDMEAS. Lines 29 to 34 show how MTIME is increased, and thus, more generally, how 16-bit and 32-bit variables are treated when it comes to using them in calculations. Starting with the lowest-order byte, the calculations are performed in a step-by-step manner, taking carry-overs into account at all times. After increasing MTIME, the program returns to the start of the loop.

2. Overflow detection

It may happen that the measured capacit-

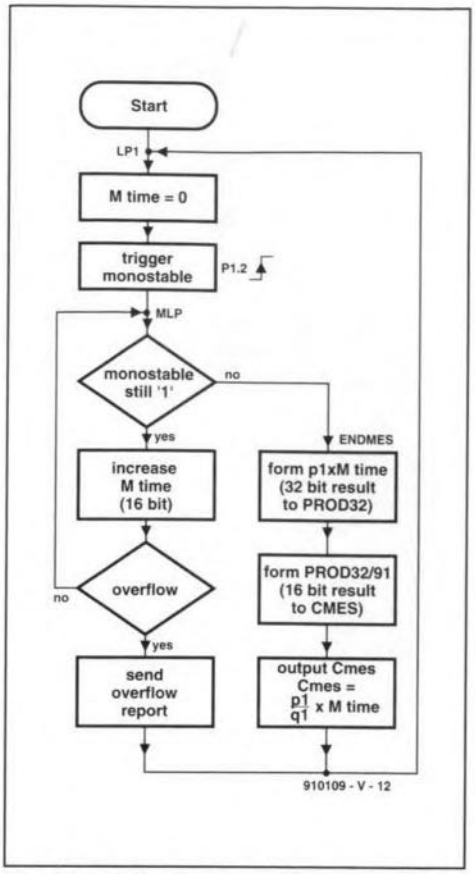


Fig. 23. Flow diagram of the capacitance meter program.

```
****** LISTING of EASM51 (XAMPLE08) ******
LINE LOC  OBJ           T       SOURCE
   1 0000                       ; ****** FILE XAMPLE08.A51 ********************************
   2 0000                       ;
   3 0000                       P1      EQU 090H        ; SFR addresses as usual
   4 0000                       ACC     EQU 0E0H
   5 0000                       DPL     EQU 082H
   6 0000                       DPH     EQU 083H
   7 0000                       ;                       ; calibration constants
   8 0000                       p1      EQU     1000    ; counter
   9 0000                       q1      EQU     1522    ; denominator of cal. factor
  10 0000                       ;
  11 0000                       MONTOP  EQU     050H    ; use assembler for RAM management
  12 0000                               ORG     MONTOP  ; above MONITOR RAM
  13 0050                       MTIME   DS      2       ; 16 bit measured TIME
  14 0052                       p       DS      2       ; p=p1 : multiplier ( 16 bit value )
  15 0054                       q       DS      2       ; q=q1 : divisor ( 16 bit value )
  16 0056                       PROD32  DS      4       ; product MTIME*p ( 32 bit value )
  17 005A                       Cval    DS      2       ; result given in nF ( 16 bit value )
  18 005C                       ;
  19 005C                               ORG     4100H           ; start address of program
  20 4100 75 50 00 [2] lp1      MOV     MTIME+0,#0      ; reset 16 bit value MTIME
  21 4103 75 51 00 [2]          MOV     MTIME+1,#0
  22 4106 C2 92    [1]          CLR     P1.2            ; Trigger:=0
  23 4108 E4       [1]          CLR     A
  24 4109 D5 E0 FD [2] lpp      DJNZ    ACC,lpp         ; wait loop for trigger pulse
  25 410C D2 92    [1]          SETB    P1.2            ; trigger monostable
  26 410E 90 C0 00 [2]          MOV     DPTR,#0C000H    ; address for monostable output
  27 4111 E0       [2] MLP      MOVX    A,@DPTR         ; read monostable output
  28 4112 30 E3 15 [2]          JNB     ACC.3,ENDMEAS   ; BIT 3 = 0 means END
  29 4115 E5 50    [1]          MOV     A,MTIME         ; else increment 16 bit value
  30 4117 24 01    [1]          ADD     A,#1            ; i.e. add 1
  31 4119 F5 50    [1]          MOV     MTIME,A         ; store (LSB)
  32 411B E5 51    [1]          MOV     A,MTIME+1       ; fetch MSB
  33 411D 34 00    [1]          ADDC    A,#0            ; add 0 + carry
  34 411F F5 51    [1]          MOV     MTIME+1,A       ; store MSB
  35 4121 50 EE    [2]          JNC     MLP             ; carry -> overflow, else continue
  36 4123 90 41 74 [2]          MOV     DPTR,#OVTXT     ; send overflow message
  37 4126 31 88    [2]          ACALL   STXT
  38 4128 80 D6    [2]          SJMP    lp1
  39 412A 90 03 E8 [2] ENDMEAS  MOV     DPTR,#p1        ; end of time measurement
  40 412D 85 82 52 [2]          MOV     p+0,DPL         ; p:=p1 ( 16 bit value )
  41 4130 85 83 53 [2]          MOV     p+1,DPH
  42 4133 78 52    [1]          MOV     R0,#p
  43 4135 79 50    [1]          MOV     R1,#MTIME
  44 4137 75 30 52 [2]          MOV     COMMAND,#ccMUL ; calculate MTIME*p
  45 413A 12 02 00 [2]          LCALL   MON
  46 413D 86 56    [2]          MOV     PROD32+0,@R0  ; store to PROD32 (32 bit value )
  47 413F 08       [1]          INC     R0
  48 4140 86 57    [2]          MOV     PROD32+1,@R0
  49 4142 08       [1]          INC     R0
  50 4143 86 58    [2]          MOV     PROD32+2,@R0
  51 4145 08       [1]          INC     R0
  52 4146 86 59    [2]          MOV     PROD32+3,@R0
  53 4148 90 05 F2 [2]          MOV     DPTR,#q1        ; q:=q1
  54 414B 85 82 54 [2]          MOV     q+0,DPL
  55 414E 85 83 55 [2]          MOV     q+1,DPH
  56 4151 78 56    [1]          MOV     R0,#PROD32
  57 4153 79 54    [1]          MOV     R1,#q
  58 4155 75 30 53 [2]          MOV     COMMAND,#ccDIV ; compute (MTIME*p)/q  (16 bit value
  59 4158 12 02 00 [2]          LCALL   MON
  60 415B 86 5A    [2]          MOV     Cval+0,@R0    ; store to Cval
  61 415D 08       [1]          INC     R0
  62 415E 86 5B    [2]          MOV     Cval+1,@R0
  63 4160 90 41 7F [2]          MOV     DPTR,#TXT1    ; send first text
  64 4163 31 88    [2]          ACALL   STXT
  65 4165 78 5A    [1]          MOV     R0,#Cval
  66 4167 75 30 05 [2]          MOV     COMMAND,#ccdRO16 ; send Cval in decimal
  67 416A 12 02 00 [2]          LCALL   MON
  68 416D 90 41 82 [2]          MOV     DPTR,#TXT2    ; send second text
  69 4170 31 88    [2]          ACALL   STXT
  70 4172 21 00    [2]          AJMP    lp1
  71 4174                       ;
  72 4174 0D 0A 4F              OVTXT   DB      13,10,'Overflow',0
          76 65 72
          66 6C 6F
          77 00
  73 417F 43 3D 00              TXT1    DB      'C=',0
  74 4182 20 6E 46              TXT2    DB      ' nF',13,10,0
          0D 0A 00
  75 4188                       ;
  76 4188                       ccSTXT  EQU  002H  ; monitor commands and addresses
  77 4188                       ccdRO16 EQU  005H
  78 4188                       ccMUL   EQU  052H
  79 4188                       ccDIV   EQU  053H
  80 4188                       COMMAND EQU  030H
  81 4188                       MON     EQU 0200H
  82 4188                       ;
  83 4188 75 30 02 [2] STXT     MOV COMMAND,#ccSTXT
  84 418B 02 02 00 [2]          LJMP MON
  85 418E                       END
********** SYMBOLTABLE (26 symbols) **********
      P1 :0090        ACC :00E0        DPL :0082        DPH :0083
      p1 :03E8         q1 :05F2     MONTOP :0050     MTIME :0050
       p :0052        PROD32 :0056       Cval :005A
     lp1 :4100        lpp :4109        MLP :4111    ENDMEAS :412A
   OVTXT :4174       TXT1 :417F       TXT2 :4182     ccSTXT :0002
  ccdRO16 :0005      ccMUL :0052      ccDIV :0053    COMMAND :0030
     MON :0200       STXT :4188
```

Fig. 24. List file produced by assembling the capacitance meter program, XAMPLE08, on your course diskette.

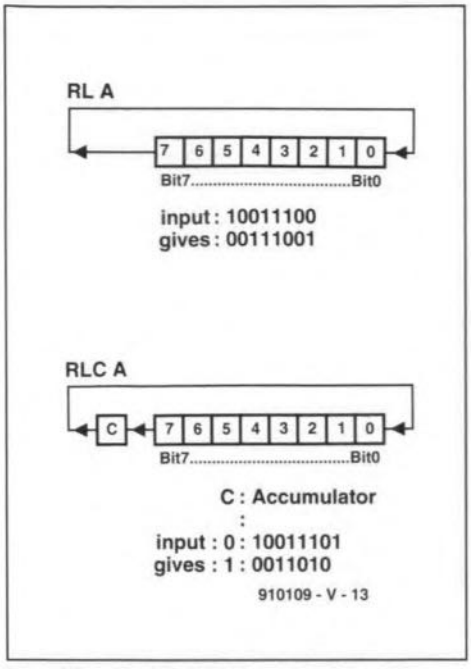


Fig. 25. Illustrating the operation of the rotate instructions.

ance (i.e., the value of MTIME) exceeds the range of a 16-bit number. When this happens, a MTIME produces an 'overflow', which is detected in line 35. The overflow condition is reported on the display with the aid of the serial output routine called up in lines 36 and 37.

3. Number conversion

It, is, of course, required that the capacitor value be indicated in a usual unit of measure, say, nanofarads. To obtain such values, the number of iterations of the measurement loop is first converted into an equivalent time, which represents the length of the monostable period. Since each loop iteration takes 12 µs, the pulse length, T, at the end of the loop equals T=12×MTIME microseconds. Note, however, this is not quite correct since 6 microseconds elapse before the loop is entered. Fortunately, the resulting error is so small that we need not bother about it.

According to the data sheets of the 74HC123, the monostable period, T, is calculated from

$$T = 0.45\ R_{ext}\ C_{ext}$$

when C_{ext} is greater than 10 nF. The units are ohm, second and farad. Since R_{ext}=47 kΩ (resistor on the SBC extension board), we get

$$C_{ext} = 0.5673\ \text{MTIME}$$

where C_{ext} is in microfarads (µF). Since the 8051 lacks a floating-point arithmetic module, we have to resort to equivalent fractions, a procedure familiar from Forth programming. First, therefore, we write 0.5673 as 5673/1,000. This allows both the denominator and the numerator to be fitted into 16-bit numbers. In the program, these appear as variables p1 and q1. To multiply MTIME with 0.5673, we first multiply it with the denominator (lines 39 to 52), and subsequently divide the resulting 32-bit number (stored as 4 bytes under PROD32) by the numerator (lines 53 to 63). The result is a 16-bit number stored under the variable Cval, which is converted into decimal and output to the display by calling a routine in the EMON51 system monitor (line 66).

Theory and practice

Unfortunately, the results of the above calculations must be taken with a pinch of salt, mainly because of tolerances on the 47-kΩ resistor and on the 74HC123. The latter tolerance is particularly troublesome as it is fairly large and temperature-dependent. The program therefore includes variables to calibrate the capacitance meter, not by adjusting the resistor, but by a more clever approach. First, p1 and q1 are turned into constants set to 1,000. Next, the program is started, so that the value of MTIME is output rather than the capacitor value, although a close-tolerance 1.5-µF capacitor is connected. The resulting value of MTIME, say, 1,540, is noted, and assigned to q1 in the final program. The other variable, p1, remains at 1,000, so that MTIME=1,540 when a 1-µF capacitor is connected. Multiplied by p1 (1,000), and divided by q1 (1,540), this gives the correct readout: 1,000 nF. Since the monostable period is virtually proportional to the connected capacitance, the meter can be calibrated in this way without problems.

The capacitance measurement program, simple as it may be, already goes to show that converting measurement values into a meaningful indication requires a thorough

JOIN THE COURSE!

What you need to follow this course:

- **a 8032/8052AH-BASIC single board computer as described in Elektor Electronics May 1991. The preferred CPU is a 8051 or 80C32. Alternatively, any other MCS52-based microcontroller system (but read part 1 of the course);**
- **a course diskette (IBM: order code ESS 1661; Atari: order code ESS 1681) containing programming examples, hex file conversion utilities, and an assembler;**
- **a monitor EPROM (order code ESS 6091);**
- **an IBM PC or compatible operating under MS-DOS, or an Atari ST with a monochrome display.**

Appeared so far:

Part 1: Introduction (February 1992)
Part 2: First 8051 instructions (March 1992)
Part 3: Hardware extensions for 80C32 SBC (April 1992)
Part 4: Flags, bit addressing, PSW, conditional jumps, logic operators (June 1992)

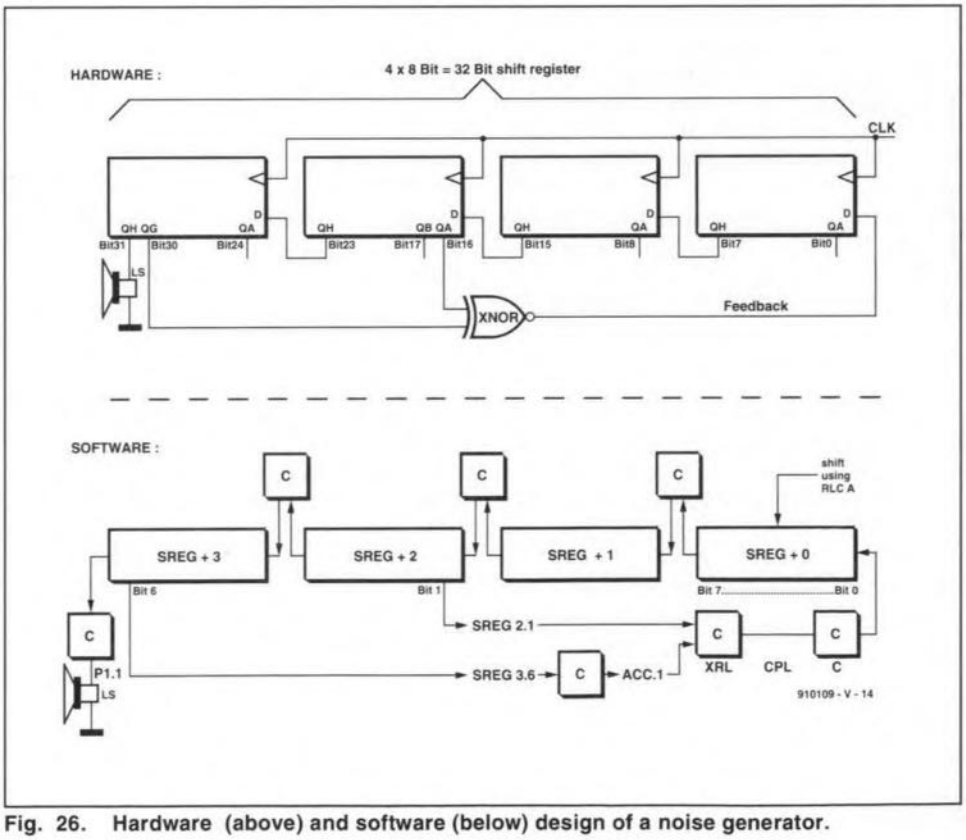


Fig. 26. Hardware (above) and software (below) design of a noise generator.

understanding of various programming steps involving arithmetic instruction sequences. Those of you who wish to practise with these may do so by writing small programs that make use of the arithmetic routines built into the system monitor program, EMON51.

Shift and rotate

The following instructions are available to shift (or rotate) a bit pattern in the accumulator to the left or to the right:

```
RL    A      ;rotate accu left
RLC   A      ;rotate accu left
               through carry flag
RR    A      ;rotate accu right
RRR   A      ;rotate accu right
               through carry flag
```

The operation of the rotate instructions is illustrated in Fig. 25. By clearing the C flag before an RRC or an RLC, a 0 is shifted into the extreme left hand or extreme right-hand accu bit position, respectively. The rotate instructions can be used in shift register simulations (see below), or in arithmetic operations (see, for example, the realization of the DIV routine in EMON51).

```
****** LISTING of EASM51 (XAMPLE09) ******
LINE LOC  OBJ          T        SOURCE
   1 0000                ; ****** FILE XAMPLE09.A51 **********************************
   2 0000                ;
   3 0000                P1      EQU 090H        ; SFR addresses as usual
   4 0000                ACC     EQU 0E0H
   5 0000                ;
   6 0000                MONTOP  EQU     050H    ; use assembler for RAM management
   7 0000                        ORG     MONTOP  ; above MONITOR RAM
   8 0050                SREG    DS      4       ; 32 bit shift register
   9 0054                ;
  10 0054                        ORG     4100H           ; start address of program
  11 4100 75 50 00 [2]          MOV     SREG+0,#0       ; clear shift register (32 bit)
  12 4103 75 51 00 [2]          MOV     SREG+1,#0
  13 4106 75 52 00 [2]          MOV     SREG+2,#0
  14 4109 75 53 00 [2]          MOV     SREG+3,#0
  15 410C E5 53     [1] NEW     MOV     A,SREG+3        ; form XNOR logic combination
  16 410E A2 E6     [1]         MOV     C,ACC.6         ; bit 6 of SREG byte 3
  17 4110 92 E1     [2]         MOV     ACC.1,C         ; to bit 1 in accu
  18 4112 65 52     [1]         XRL     A,SREG+2        ; XOR with pos. 1 of SREG+2
  19 4114 A2 E1     [1]         MOV     C,ACC.1         ; = XOR of bits 17 and 30
  20 4116 B3        [1]         CPL     C               ; C = NOT-XOR of bits 17 and 30
  21 4117                       ;
  22 4117 E5 50     [1] SHIFT   MOV     A,SREG+0        ; 32 bit shift register
  23 4119 33        [1]         RLC     A               ; shift rightmost byte
  24 411A F5 50     [1]         MOV     SREG+0,A        ; and save
  25 411C E5 51     [1]         MOV     A,SREG+1        ; fetch next byte
  26 411E 33        [1]         RLC     A               ; bit stored temporarily in C
  27 411F F5 51     [1]         MOV     SREG+1,A
  28 4121 E5 52     [1]         MOV     A,SREG+2        ; etc.
  29 4123 33        [1]         RLC     A
  30 4124 F5 52     [1]         MOV     SREG+2,A
  31 4126 E5 53     [1]         MOV     A,SREG+3
  32 4128 33        [1]         RLC     A
  33 4129 F5 53     [1]         MOV     SREG+3,A        ; C now contains new output
  34 412B 92 91     [2]         MOV     P1.1,C          ; send to loudspeaker
  35 412D 80 DD     [2]         SJMP    NEW             ; and start again
  36 412F                       END
********** SYMBOLTABLE (6 symbols) **********
      P1 :0090      ACC :00E0    MONTOP :0050     SREG :0050
     NEW :410C    SHIFT :4117
```

Fig. 27. Listing of the noise generator assembler program.

A noise generator

Reference 3 describes a noise generator of which the central part is formed by a shift register with feedback as shown in Fig. 26. As a programming example, we will implement this circuit on the 80C32 SBC and its extension board. The result is a programmable noise generator. The noise will be output via the loudspeaker, which is driven via port line P1.1.

The function of the program we are about to discuss is based on the noise generator hardware shown in the top drawing in Fig. 26. The shift register is stored at four consecutive locations in the internal RAM; the extreme right-hand bit is contained in the byte at the lowest address. This storage arrangement corresponds to the structure of a 32-bit number. This number is shifted to the left, where the XOR gate determines which bit is fed back into the sequence, at the far right end. The highest-order bit (bit 31) drives the loudspeaker.

The program listing of the noise generator is shown in Fig. 27. It is a straightforward implementation of Fig. 26, only the realization of the XOR gate (lines 15 to 20) is based on a 'trick'. Essentially, the function of the XOR gate is translated into software by combining bits in the sequence into a new bit that is added to the rightmost end of the 32-bit word. This creates feedback in the shift register, so that the output is a pseudo-random bit sequence with a long repeat time. To be precise: one loop iteration takes 23 µs, and the shift register goes through about 2 million states before a bit pattern is repeated. The pseudo-random signal thus has a sample rate of about 43 kHz, and the first 'duplicate' occurs after about 13 hours, so pretty random it is!

When used as a noise generator for audio measurements, the system requires a low-pass filter to shape the output spectrum. However, even without such a filter, the loudspeaker will produce quite a bit of real noise (a practically 'white' spectrum is produced with components up to about 20 kHz).

Assignments

Based on what has been discussed so far, consider the following assignments. Add ranges to the capacitance meter that allow it to measure smaller as well as larger capacitors. You may also try your hand at implementing an autoranging function. Another interesting subject could be the realization of a 'tolerance window' that tells the user of the capacitance meter instantly whether or not the value of a ceratin capacitor is within the required range. Producing a program to realize this will enable you to get a thorough grip on the possibilities of the arithmetic instructions.

Finally, how about turning the noise generator into a rhythm generator?

What's in store

This month's instalment nearly completes the discussion of the 8051 instruction set, which has been elucidated, where necessary, with examples. This allows us to concentrate on more hardware-oriented aspects of the 8051 in the following instalments. The subjects to be discussed will be: timers, LCD connection, serial interface and D-A/A-D conversion. ❑

Reference:

3. *The art of electronics*, by P. Horowitz and W. Hill (Cambridge University Press, 1989).

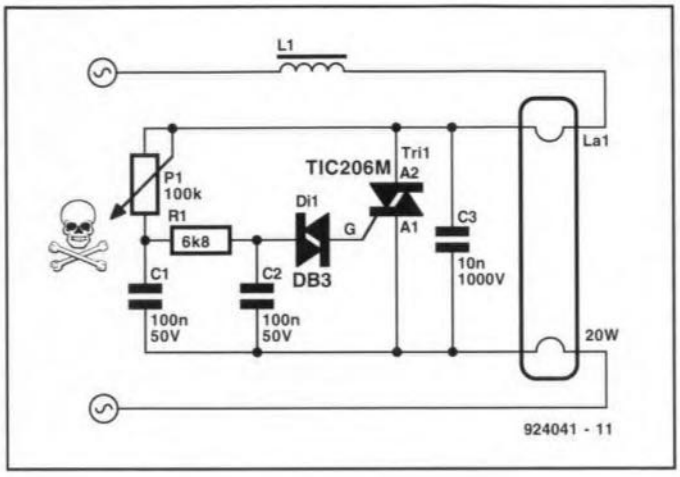
DIMMER FOR NEON TUBES

A NEON tube cannot be dimmed as easily as an incandescent lamp because the tube can start only at a voltage much higher than the mains, after which it will remain lit at the mains voltage. The level of both the starting voltage and the working voltage depends on the temperature of the tube.

Normally, the high starting voltage is obtained by interrupting the current through a choke. This is usually done by the starter, which also ensures that a fairly large current flows through the filaments of the tube. This heats the ends of the tube, which makes starting easier.

These tasks of the starter are taken over by the circuit show in the diagram, which also enables the tube to be dimmed.

During the zero voltage crossings of the applied mains voltage, the triac will instantaneously switch off. At those instants, capacitor C_3 will be charged rapidly, which results in the instantaneous voltage, whose phase has shifted relative to that of the current, being applied across the tube. Capacitor C_3 and the choke form a resonant circuit that raises the sudden voltage across the tube to a very high value, whereupon the tube starts.



The larger the angle of the mains voltage during which the triac conducts, the larger the current through the tube filaments, which results in a lower starting voltage. At the same time, since a larger part of the current flows through the triac, that through the tube will be reduced, so that the tube will light more faintly.

When the tube is first switched on, the dimmer control, P_1, should be set for maximum brightness of the tube to facilitate starting.

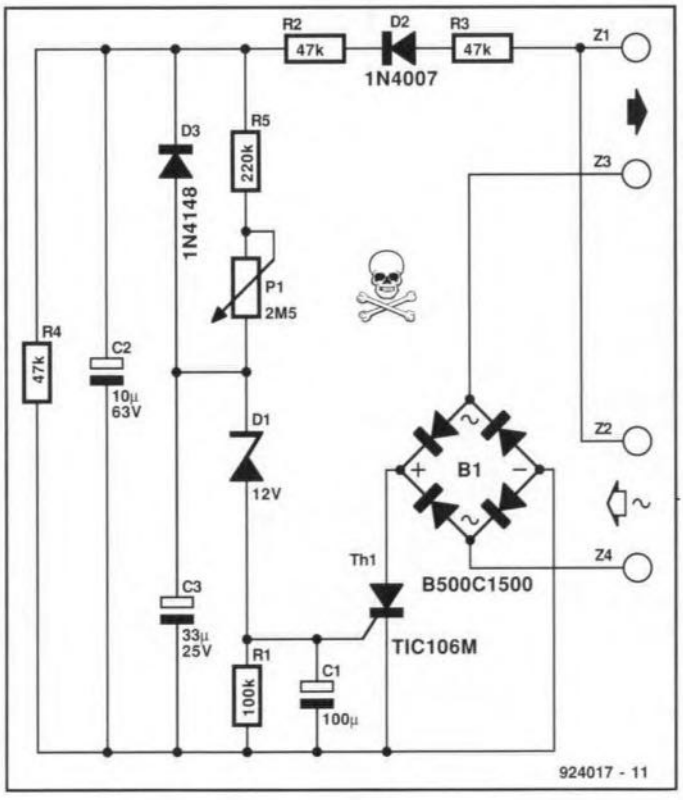
The triac used should have a high du/dt value, otherwise the steep voltage transitions occurring across the tube, and thus across the triac, during the zero voltage crossings would cause the triac to remain on.

[SGS Thomson – 924041]

POWER-ON DELAY FOR ATARI ST

WHEN the Atari ST is provided with an external hard-disk drive, it has to be reset after about 15 seconds, as otherwise the drive is not enabled. The delay circuit presented here obviates that inconvenience by ensuring that the computer is not switched on until a (presettable) period of time has elapsed. The circuit may also be used with the combination of MS-DOS computer and HP DeskJet printer, since the latter can be switched on only after the MS-DOS machine is powered. If that type of printer is used with an Atari ST, the printer must be switched on before the computer is. No doubt, there are other situations where this delay may prove useful.

Operation of the circuit is fairly simple. After the mains has been switched on, capacitor C_3 is charged via R_5 and P_1. When, after a period of time set with P_1, the potential across C_3 has reached 12 V, zener diode D_1 conducts and switches on thyristor Th_1. That device ensures that bridge B_1 provides an a.c. connection between the mains input and the mains output. At the instant the thyristor is switched on, owing to the anode-cathode current, its gate voltage rises slightly. This results in C_3 being charged a little more and thus serves as gate-current buffer to ensure that the thyristor remains on during the mains zero voltage crossings. Therefore, once the thyristor has been switched on, it stays on.



The delay is best built into a small man-made fibre box with integral mains connectors.

The circuit is best built on a small piece of veroboard or other prototyping board, bearing in mind that it will carry the full mains voltage. This means that tracks carrying the mains must be separated by at least 3 mm and preferably 5 mm. This probably entails the removal of tracks between the mains-carrying ones.

[R. Lucassen – 924017]

WIDEBAND ACTIVE TELESCOPIC ANTENNA

MOST VHF/UHF amplifiers for use with a symmetrical antenna (such as an open or closed dipole) have a balun at the input. A balun (short for 'balanced to unbalanced') is an inductive device that converts the symmetrical (balanced) RF signal into an asymmetrical (unbalanced) signal that can be applied to the base of a transistor. Unfortunately, baluns have an inherent loss of 2–3 dB, while most input transistors (typically a BFR91 or similar) have noise figures not better than about 2 dB. This explains the rather poor overall noise figure of 4–5 dB of this type of input stage.

A much lower noise figure is achieved by the circuit shown here, which does not incorporate a balun, and uses the BFG65 low-noise transistor as the amplifying device. The combination of a telescopic rod and a low-noise wideband RF amplifier is referred to as an 'active antenna'. The design shown here has two options: (1) if used with an existing antenna, it ensures a much better S/N (signal-to-noise) ratio in the receiver, or (2) the same S/N ratio can be achieved using a much simpler antenna.

The antenna proper is an open dipole with a total length of 1.6 m, which works as a 0.5 lambda dipole from 60 MHz to about 187 MHz, or as a multi-lambda V-dipole up to about 900 MHz. Unusually, the balanced-to-unbalanced conversion is done at the output of the amplifier, with the aid of a length of coax cable that functions as a kind of choke. The construction of the amplifier on the PCB shown, and its electrical behaviour, enables the antenna to 'see' a balanced load.

The two telescopic rods are connected directly to the solder pads marked 'ANT.1' and 'ANT.2'. Usually, telescopic rods have a kind of 'knee' construction at the base that enables them to be rotated as well as bent up and down. With some dexterity, this mechanism may be retained for use with the present amplifier.

The output inductor, L_1, consists of 10 turns of 2.5 mm dia. 60 Ω coax cable wound on a 10 cm long ferrite rod with a diameter of 10 mm.
The phantom supply for the amplifier is not contained on the printed circuit board, but is simple to install at the input of the receiver, since it consist of a resistor and a capacitor only. If the receiver is located further than about 2 m away from the active antenna, it may be connected to K_1 via a length of ordinary coax cable like RG58.

Provided the antenna is used in an area with relatively low local field strengths, you may lower the noise figure of the BFG65 by increasing R_3 a little. This should not be done, however, if there are strong signals around, in which case the result is an increased risk of cross-modulation.

With R_3=560 Ω, the current consumption is about 20 mA. The gain of the dipole signal amounts to about 12 dB, while a noise figure of about 1 dB is achieved. This will ensure results comparable to those of a much larger antenna (yagi), provided signal reflections and multipath reception are not a problem.

(J. Barendrecht – 924102)

PARTS LIST

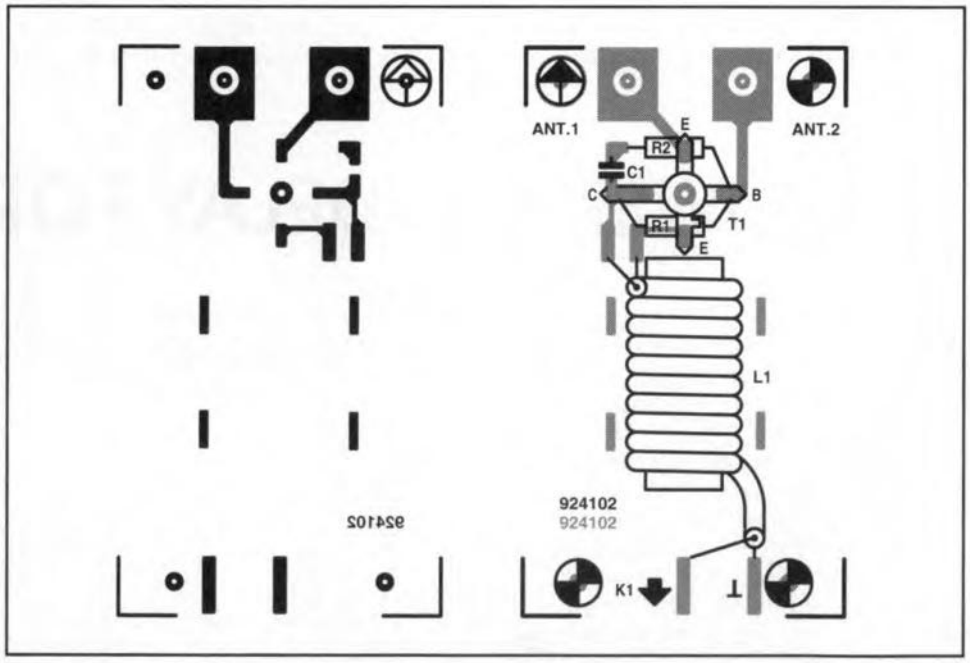
Resistors:
R1 = 10kΩ
R2 = 390Ω
R3 = 560Ω (see text)

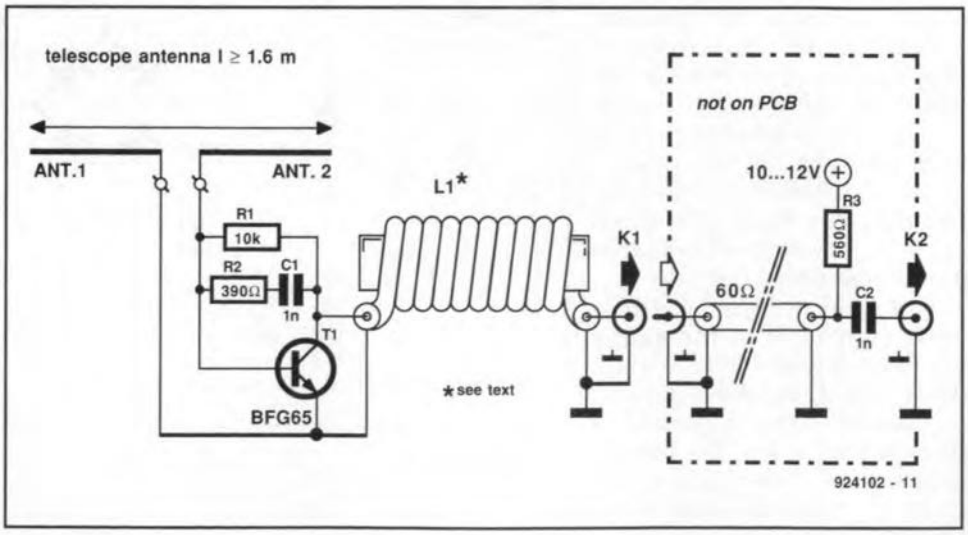
Capacitors:
C1 = 1nF ceramic
C2 = 1nF ceramic

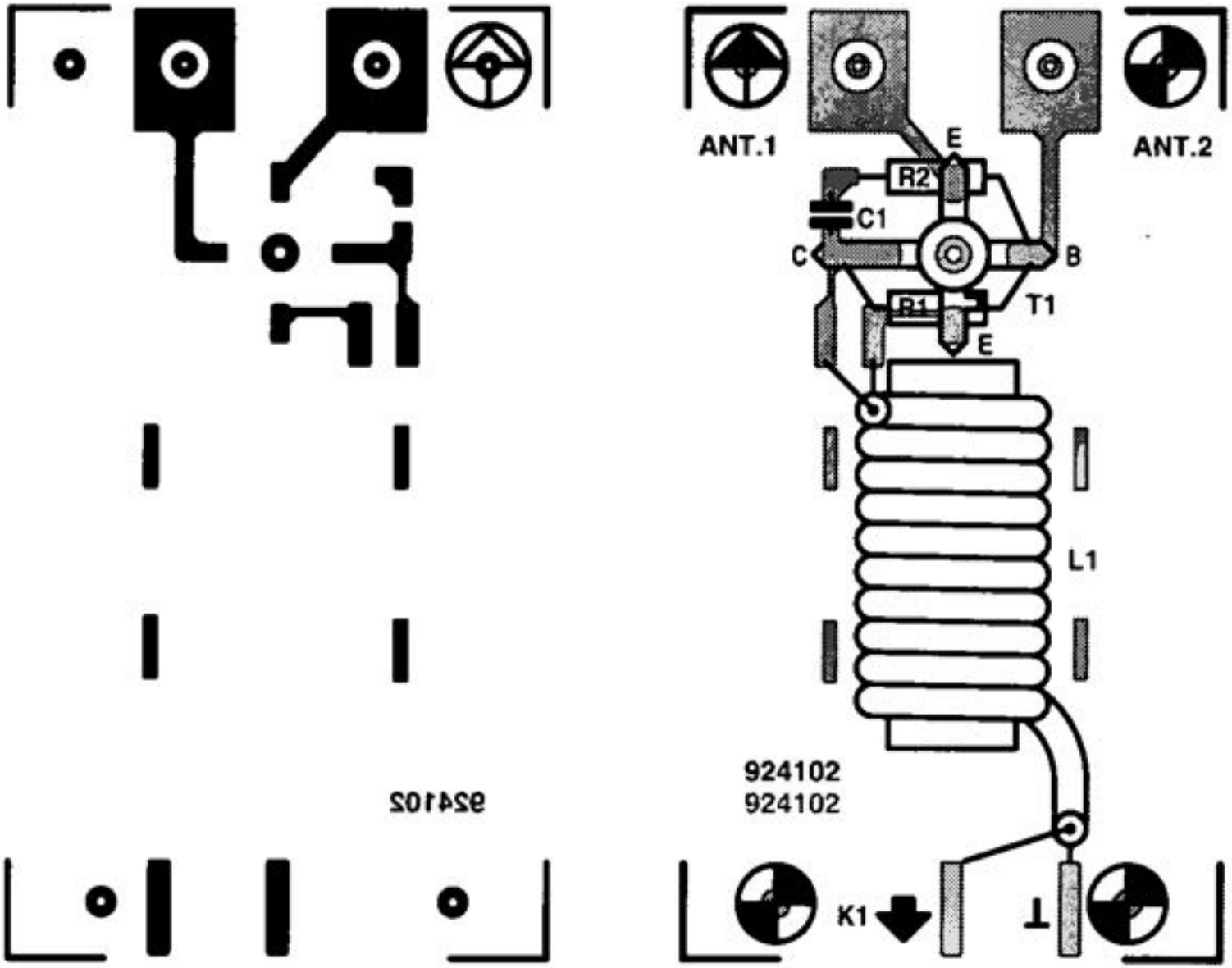
Semiconductors:
T1 = BFG65

Inductor:
L1 = see text. Materials: 2.5-mm dia. 60-Ω coax cable; 10-mm dia. ferrite rod.

Miscellaneous:
ANT.1;ANT.2 = telescopic rod antenna for PCB connection. Min. length = 80cm.
K1 = BNC socket.
Printed circuit board 924102.






ANT.1
ANT.2
E
R2
C1
C
B
T1
R1
E
L1
924102
924102
924102
K1

READERS' CORNER

CORRECTIONS

Wide-band active telescopic antenna
(page 46)
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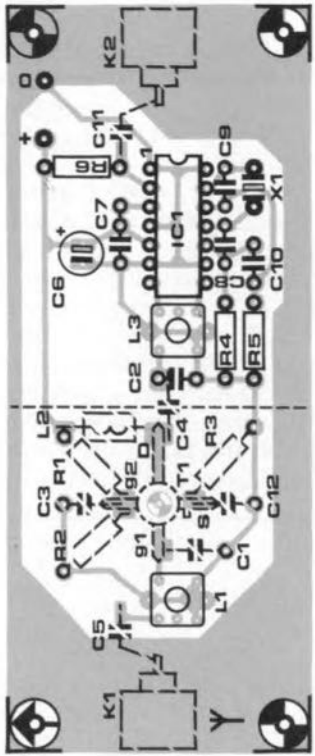

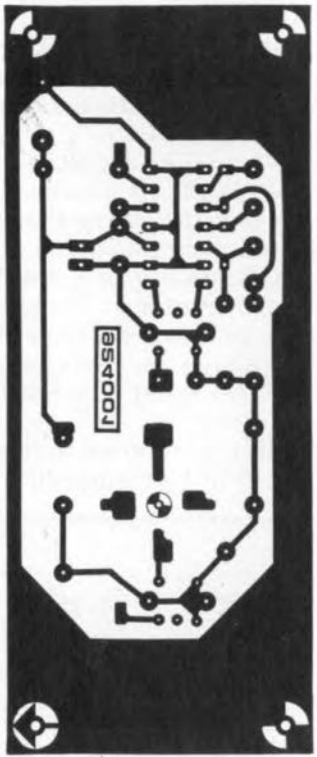

LETTERS

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L.J. Burns
New Zealand

Unfortunately, the designer could not obtain the repeatability of his prototype that is absolutely vital for our readers. Furthermore, the designer has since moved away. Sorry!
[Editor]

asdoor

INFRA-RED HEADPHONE TRANSMITTER

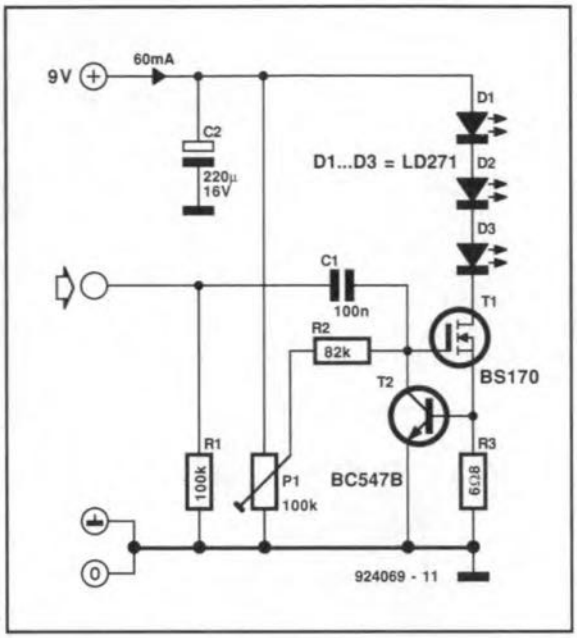
THE proposed transmitter provides an optical (infra-red), that is, wireless, connection to a headphone. The receiver is described in the next article.

Three infra-red (IR) LEDs are provided with a quiescent current by T_1. The level of that current is set with P_1. When an audio signal is applied to the gate of T_1, the current through the LEDs is modulated. Consequently, the light emitted by the diodes is also (amplitude) modulated.

To prevent overdriving of the gate causing too high a current through the LEDs, a current limiter, consisting of T_2 and R_3, holds the current below 100 mA.

The maximum dissipation of a BS170 is 830 mW at an ambient temperature of 25 °C, while the maximum drain current is 500 mA. Therefore, even when the FET is overdriven, those limits are not exceeded.

The optimum quiescent current through the LEDs must be determined in conjunction with the receiver (which must be adjusted for minimum distortion).



The prototype transmitter drew a current of about 60 mA at a supply voltage of 9 V. It is, therefore, advisable to use a mains adaptor, because that current is just a little too high for a PP3 battery. Keep the earths of the mains adaptor and the audio signal separated as shown in the diagram to prevent feedback of the LED current to the input.

The gate-source voltage of a BS170 may be up to 15 V. If you use a signal source that delivers a higher level, it is advisable to incorporate a simple protection circuit (for instance, a 10-V zener diode in parallel, or a resistor in series, with the input).

The optical connection is fairly directional, but this can be improved by placing the LEDs at varying angles. Also, the distance of operation can be extended appreciably by fitting reflectors behind the LEDs.

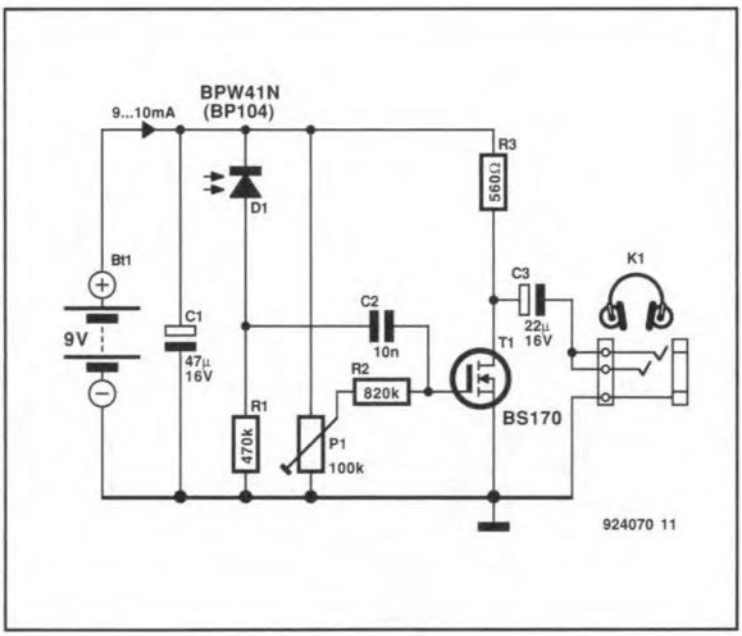
The optimum input level for an operating distance of some metres (4–8 ft) is 100–200 mV.

(Amrit Bir Tiwana – 924069)

INFRA-RED HEADPHONE RECEIVER

THIS receiver is meant to complement the transmitter described in the previous article. It's design is based on just one FET. This has the advantage that construction is simplicity itself, and the disadvantage that for a sufficiently low output im-pedance the value of drain resistor R_3 has to be fairly low. That results with correct operation of T_1 to a fairly large (certainly for a battery) current. The value of R_3 was chosen, as a compromise, at 560 Ω, which makes driving 600 Ω headphones possible. The load seen by T_1 is then 300 Ω.

Both usable types of receive diode shown in the diagram have a daylight filter and are tuned to the wavelength of the LEDs in the transmitter (950 nm at 25 °C). At a couple of metres (5–8 ft) distance, a (no-load) output voltage of 200–300 mV is obtained, which is quite sufficient for most headphones. The circuit then draws a current of 9–10 mA.



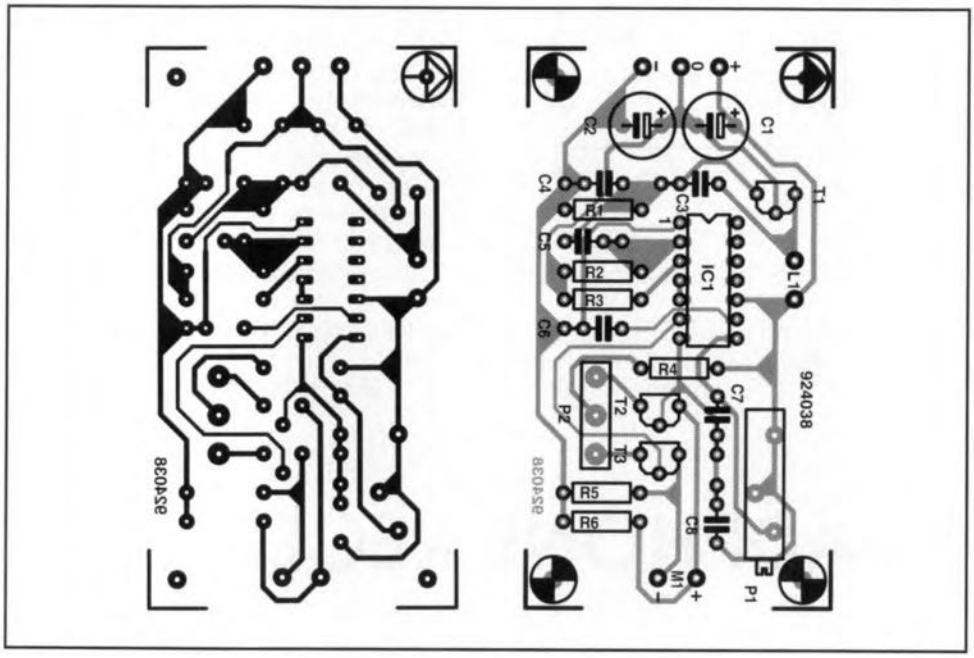
The setting of P_1 is fairly critical, but its control range may be reduced by adding a small resistor at either side of the preset. The preset should be adjusted for minimum distortion. This is best done by applying a 1 kHz audio signal at a level of 150 mV to the transmitter and adjusting both circuits for minimum (audible) distortion. This should be done without electric light, because the transmitter does not modulate the audio signal on to a carrier, so that light bulbs, and particularly neon tubes (which emit an appreciable amount of IR light at 950 nm, modulated with 100 Hz) can cause quite a hum. Even normal ambient light causes a deterioration of the signal-to-noise ratio. However, with a little ambient light and a distance between transmitter and receiver of 3–4 m (10–13 ft), the distortion was 1–2%, which is not bad for such a sparse design.

(Amrit Bir Tiwana – 924070)

METAL DETECTOR

THIS detector will help you find fairly large objects that consist of materials with a relatively high permeability. Also, it indicates whether the magnetic object inside the detection coil has good or bad conductive properties. Examples of materials that couple good magnetic properties to a fairly high electrical isolation are ferrites pressed from metal oxides. The detector is not suitable for 'coin digging', for which it is not sensitive enough. The more fanciful stuff like bombs and treasures left by pirates, is, however, reliably located.

The metal detector is powered symmetrically by two 9-V batteries, each of which is loaded with about 15 mA. The detection coil, L_1, forms part of a sine wave oscillator built around transistor T_1. Normally, the central frequency of the VCO (voltage-controlled oscillator) in the PLL (phase-locked loop) contained in IC_1 equals the oscillator frequency of T_1. That



PARTS LIST

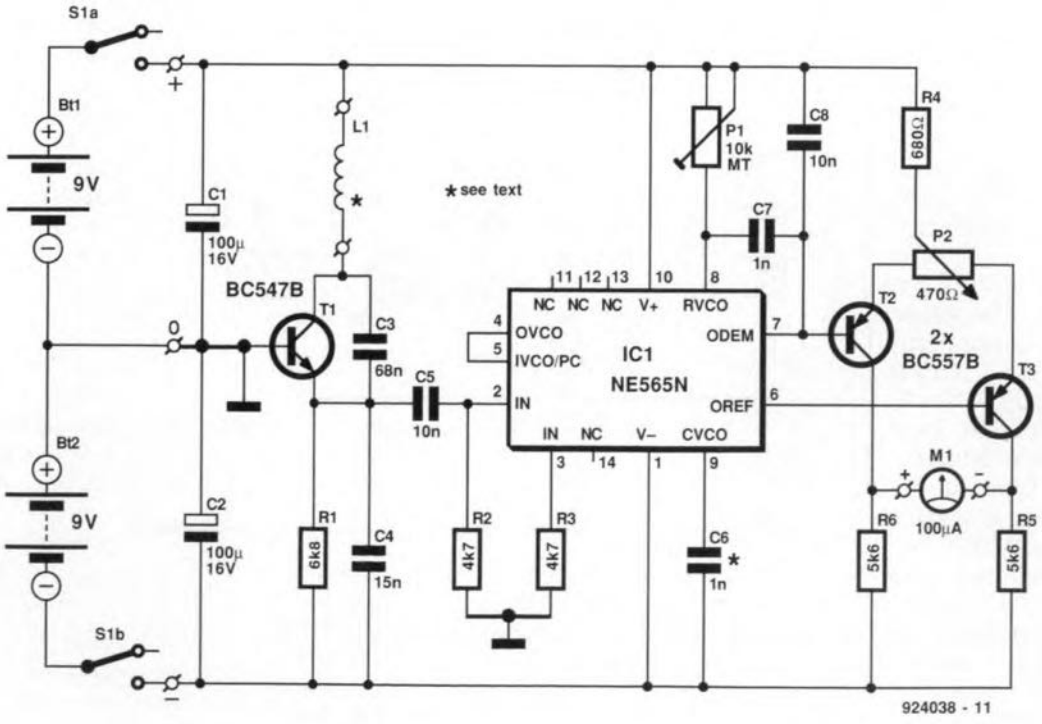
Resistors:
R1 = 6kΩ8
R2;R3 = 4kΩ7
R4 = 680Ω
R5;R6 = 5kΩ6
P1 = 10kΩ multiturn preset
P2 = 470Ω linear potentiometer

Capacitors:
C1;C2 = 100µF 16V radial
C3 = 68nF
C4 = 15nF
C5;C8 = 10nF
C6;C7 = 1nF

Inductor:
L1 = details in text

Semiconductors:
T1 = BC547B
T2;T3 = BC557B
IC1 = NE565N

Miscellaneous:
S1 = miniature double-pole change-over switch.
Bt1;Bt2 = 9-V battery with connecting clip.
M1 = centre-zero ±50µA moving coil meter.

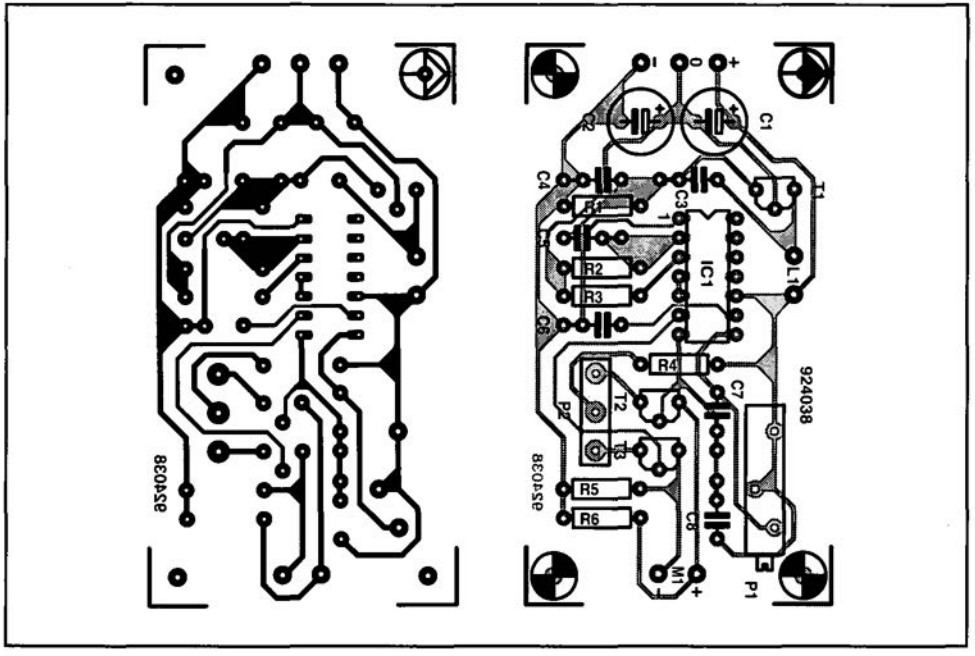


changes when a metal object (ferrometallic or non-ferrometallic) enters the field induced by L_1. When that happens, the sine-wave oscillator is detuned, and the voltage difference between pins 6 and 7 of IC_1 indicates the difference between the sine oscillator frequency and the VCO frequency. This difference causes moving-coil meter M_1 to deflect. The needle deflection itself is a measure of the frequency change, while the direction of the needle depends on the type of material detected by the coil. The meter used here is a centre-zero ±50 µA type.

The coil consists of 40 turns of enamelled coper wire on a plastic former with a diameter of about 10 cm (4 in). The inductance so obtained ensures that the sine-wave oscillator works at a frequency which is roughly equal to that of the VCO in the PLL.

Use an oscilloscope to check that pin 2 of IC_1 supplies a sine-wave signal with a frequency of about 75 kHz. Next, adjust P_1 such that the edges of the rectangular signal at pin 4 coincide with the positive peaks of the sine wave at pin 2. Next, null the meter by turning potentiometer P_2. Since the null adjustment will drift a little as the battery volatge drops, it will be necessary to redo the balance adjustment every now and then during use.

(K. Kraus – 924038)



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C4 = 15nF
C5;C8 = 10nF
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Semiconductors:
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IC1 = NE565N

Miscellaneous:
S1 = miniature double-pole change-over switch.
Bt1;Bt2 = 9-V battery with connecting clip.
M1 = centre-zero ±50µA moving coil meter.

CB-TO-SW DOWN CONVERTER

THIS converter enables long-distance (DX) reception of AM or SSB stations in the 27-MHz citizens' band (CB) on a short-wave or medium-wave radio (note, though, that AM or SSB modulation in the 27-MHz CB band is no longer allowed in a number of countries).

The converter consists of a prestage, T_1, and a mixer/oscillator, IC_1. The antenna signal is coupled inductively to the gate of dual-gate MOSFET T1 via tuned circuit L_1-C_1, which acts as a 27 MHz input filter. The operating point of the MOSFET is determined by resistors R_1-R_2 connected to the gate-2 terminal. The amplified signal is fed to the mixer amplifier via a coupling capacitor and a second tuned circuit, L_3-C_2. The oscillator on board the S042P IC (manufacturer: Siemens) works with a quartz crystal, X_1. The quartz frequency is selected such that the difference frequency produced by the mixer (also on board the S042P) falls within the tuning range of the radio connected to the output of the converter. For instance, if an inexpensive 26.800 MHz crystal is used, the frequency of the received 27-MHz station, f_{in}, is

$$f_{in} = 26{,}800 \pm f_{dial}$$

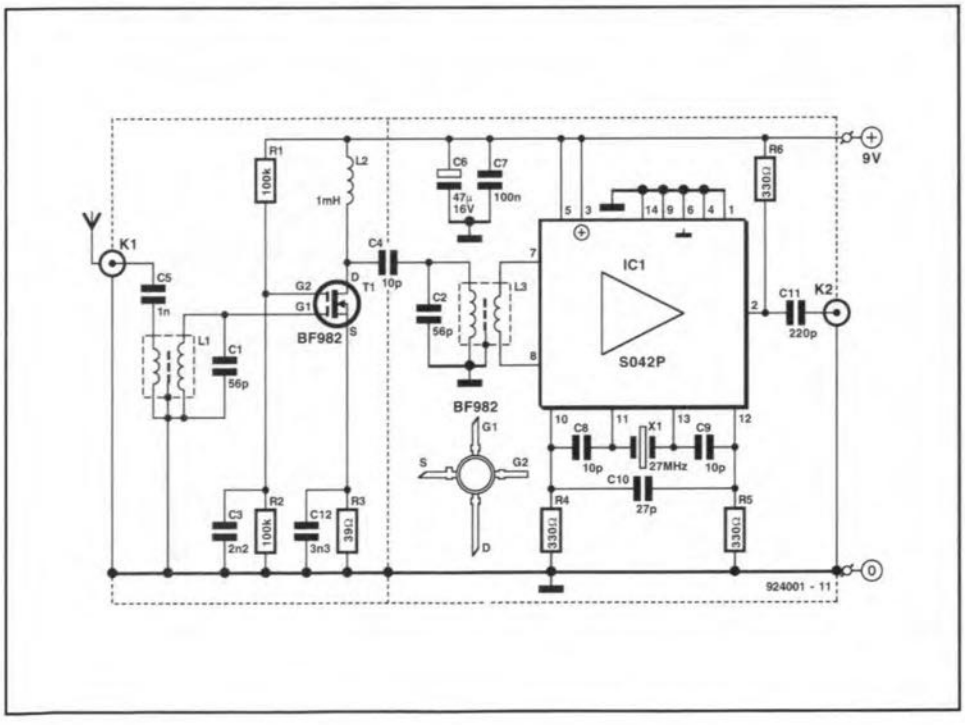
where f_{dial} is the frequency read on the radio's tuning scale (in this case, the received stations will appear in the medium-wave band). Other crystal frequencies may be used, e.g., 10 MHz, to move the CB band into the SW range (17 MHz).

Construction of the converter is fairly easy on the printed circuit board shown here. Parts shown with a dashed outline are fitted at the solder side of the board. The converter is shielded all around to prevent spurious radiation. The antenna and the IF output are best connected via coax sockets (SO239 or BNC). The two inductors in the converter are simply adjusted for best reception.

The converter is powered either by a regulated 9-V adaptor, or by the radio is is connected to, if this is capable of furnishing 9 V at a few tens of mA.

(924001 — Dr. U. Kunz)

For drawings of the PCB, see p. 99



PARTS LIST

Resistors:
R1;R2 = 100kΩ
R3 = 39Ω
R4;R5;R6 = 330Ω

Capacitors:
C1;C2 = 56pF ceramic
C3 = 2nF2 ceramic
C4 = 10pF ceramic
C5 = 1nF ceramic
C6 = 47µF 16V radial
C7 = 100nF ceramic
C8;C9 = 10pF ceramic
C10 = 27pF ceramic
C11 = 220pF ceramic
C12 = 3nF3 ceramic

Semiconductors:
T1 = BF982
IC1 = S042P

Inductors:
L1;L3 = 113CN2K50989189ADZ (Toko)
L2 = 1mH choke

Miscellaneous:
K1;K2 = BNC socket
X1 = see text

READERS' CORNER

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(page 46)
In contrast to what is stated in the article and in the Readers' Services (page 102), a printed-circuit board for the antenna *is* available at £2.75 plus 48p VAT (No. 924102).

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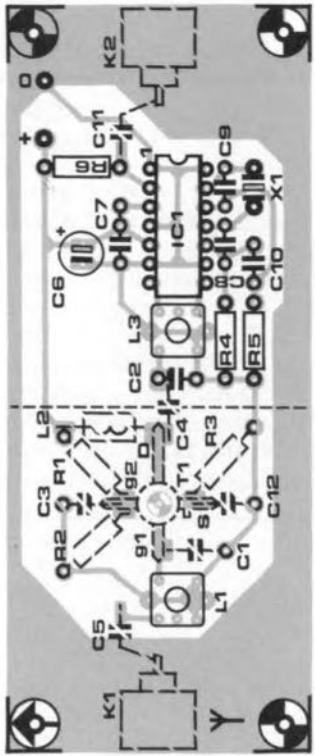

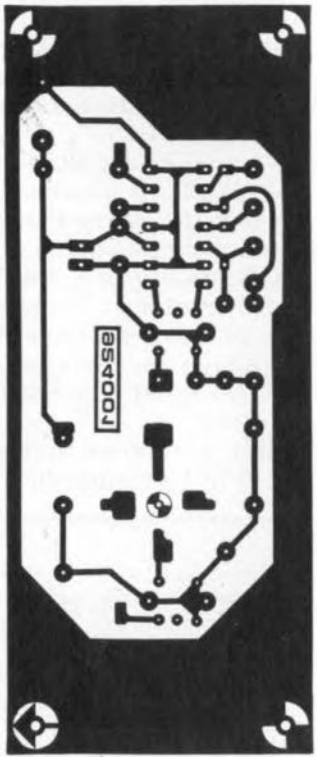

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[Editor]

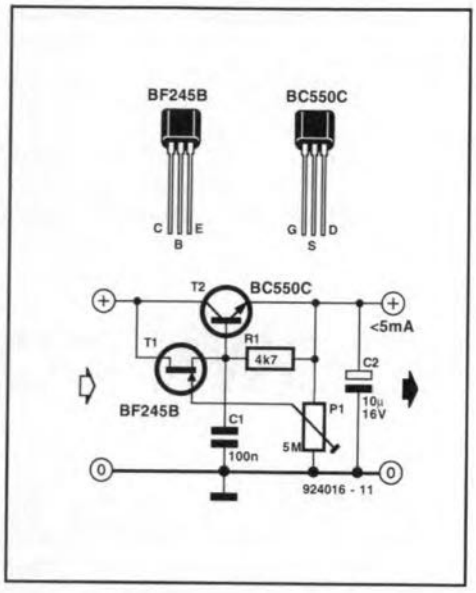
asdoor

LOW-DROP REGULATOR I

NOWADAYS the only reasons for not using a voltage regulator in a power supply are: I have not got one; I need an 'odd' voltage; I want to keep the current drain very low.

The regulator shown in the diagram is suitable for currents of 5–10 mA. The two transistors draw only a tiny current. The drop across the regulator depends on the load current and lies between 0.5 V and 1.4 V. The output voltage may be preset between 1.8 V and 8 V.

On power-up, there is no voltage at the source of T_1, so that the FET conducts. Current amplifier T_2 then draws base current and is switched on. This arrangement means that the reference (gate) voltage may be taken from a high-resistance potentiometer. The quiescent current depends on the level of the preset output voltage: at 5 V, it is a mere 1 µA.



When T_2 is switched on, the output voltage will rise to its preset level. The base potential of T_2, and thus the source potential of T_1, remains about 0.6 V higher than the output voltage, so that it rises in step with the output voltage. The gate of T_1 is, however, connected to the wiper of P_1, whose voltage rises more slowly than the output voltage, because the preset is a potential divider. Consequently, the gate of T_1 becomes more and more negative with respect to its source. An equilibrium is soon reached, whereby the FET reduces the base current of T_2 to a degree that ensures stability of the output voltage.

In normal circumstances, the output voltage vs load current ratio is of the order of 9 mV/mA.

[B.C. Zschocke – 924016]

TELEPHONE MONITOR

MODERN telephones can easily be connected in parallel, enabling a household to have one in the bedroom, kitchen and hall or study. It is, however, not always easy to see (or hear) at one position whether the phone at one of the other positions is in use or has taken up the call.

The d.c. level on most telephone lines drops from 48 V to about 8 V when one appliance is in use and to around 5 V when two telephones are in use. Also, its polarity changes over when a telephone is in use.

Since the polarity changes over, the circuit is of necessity a bridge type as shown in Fig. 1. To keep the current drain small and relatively constant at varying voltage levels, a current source is needed for the high-efficiency indicator LEDs. At 50 V across *a* and *b*, the circuit is inactive; when that potential drops to about 8 V, the current source is on; when the level has dropped to about 5 V, the 'switch' across the upper LED opens so that both diodes light.

The diagram of the practical circuit is shown in Fig. 2. The bridge rectifier is formed by diodes D_1–D_4, while T_3 serves as the LED switch.

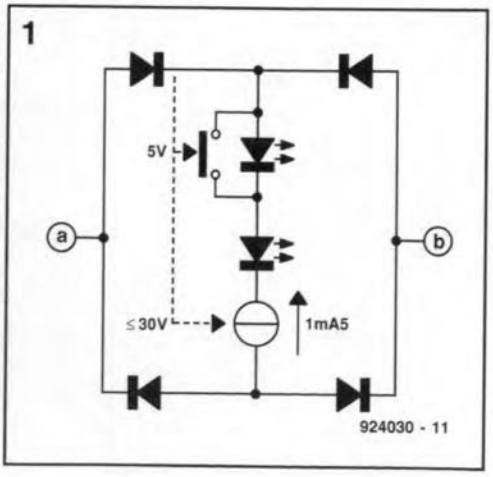
When the applied voltage is greater than 30 V, T_1 is on and switches off current source T_2. In this situation, the circuit draws not more than 0.5 mA. When the applied voltage drops to 8 V, T_1 is off and T_2 is on. The current source is completed by D_5, D_6, R_3 and R_5: with values as shown, the current supply is about 1.5 mA.

In this situation, because of the values of R_1 and R_2, T_3 is on, and D_7 is short-circuited. As soon as a second receiver is lifted, the line voltage drops to some 5 V, resulting in T_3 being switched off, so that D_7 lights.

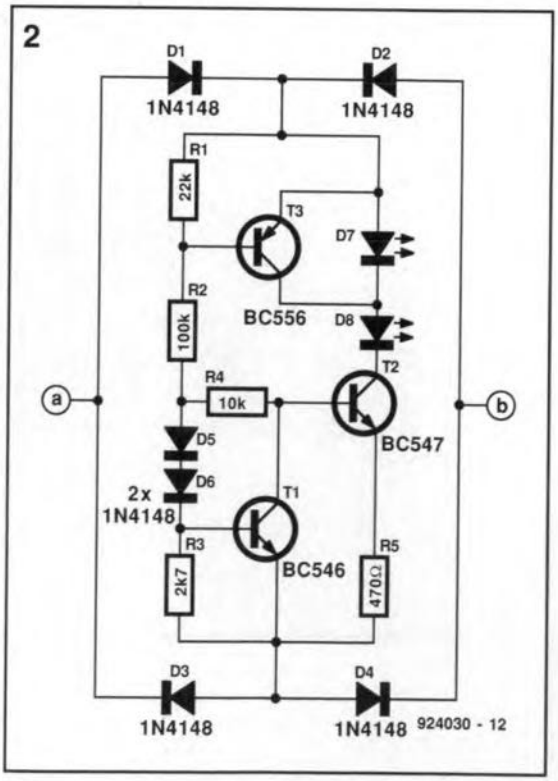
The current through the LEDs is necessarily small and should in any circumstances not rise above 5 mA. With two telephones that means that R_5 must be 270–330 Ω, and for three telephones, 390–470 Ω. As already stated, this means that high-efficiency LEDs are essential.

(P. Holmes – 924030)

1

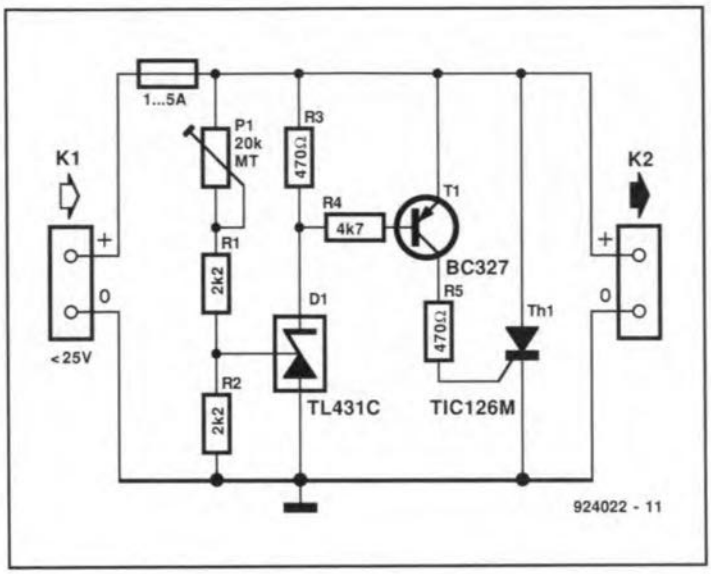


2



CROWBAR PROTECTION

QUITE a few electronic components, particularly active ones, cannot withstand too high voltages. Preventing costly circuits dying a premature death because the supply voltage has risen too high, an overvoltage protector is no luxury. Such a protector must, of course, act swiftly, otherwise the deed has been done before it has a chance to act. Therefore, (slow-acting) relays are not suitable for this purpose.



The circuit shown here, a so-called crowbar, contains several fast-acting components. It is intended to be connected between the mains and the appliance to be protected.

The circuit depends, as it were, on brute force: when the supply voltage rises too high, a thyristor short-circuits the output. This means that the too high voltage is immediately removed from the connected appliance and also that fuse F_1 blows. Brute force, indeed!

The voltage at which the crowbar comes into action is set between 5 V and 25 V with P_1. This is done as follows:

1. Set P_1 to its maximum value.
2. Replace the fuse temporarily by a wire bridge and connect the crowbar to a variable power supply. Set the current limit of that supply to 1 A and the output voltage to the value at which the crowbar is desired to act.
3. Turn P_1 back slowly until the thyristor comes on, that is, when the current limiter of the power supply comes into action.

The crowbar is now set. Replace the wire bridge by the fuse (max. rating 5 A). In quiescent operation, the crowbar circuit draws a current of only about 1 mA.

[J. Ruiters – 924022]

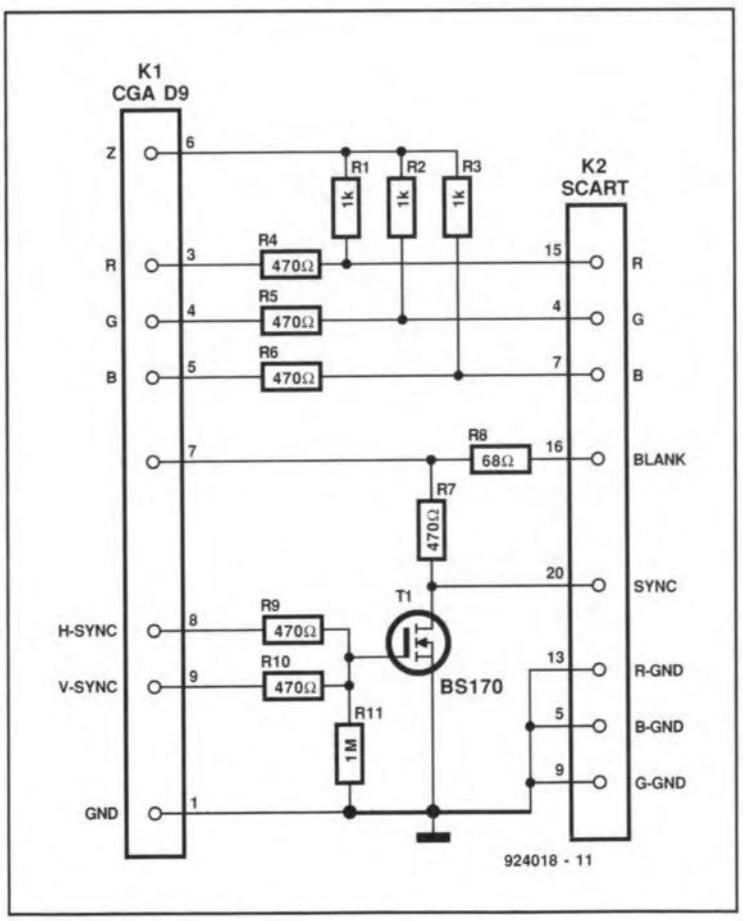
CGA-TO-SCART ADAPTOR

THE adaptor has the great advantages of not needing a separate power supply and requiring so few external components that these can easily be accommodated in the SCART connector.

The signals on the R, G, and B pins of the CGA card are converted from TTL level to SCART level with the aid of transistors R_4, R_5 and R_6 and the input impedance (75 Ω) of the SCART inputs. The output impedance of the so created voltage dividers is not exactly 75 Ω as specified for SCART video inputs, but in practice this does not appear to make much difference.

Resistors R_1–R_3 between pin 6 of the CGA card and the R, G, B pins of the SCART connector ensure that the brightness is brought down to 50% when pin 6 is active.

A composite sync(hronization) signal and a blanking signal for the TV are derived from the horizontal and vertical sync pulses of the CGA card with the aid of R_7–R_{11} and T_1.



The 5-V supply for T_1 is obtained from the CGA card via pin 7. Since that pin is not normally used, it must be linked to the 5-V line by a short length of wire.

(S. Pluis – 924018)

LOW-BATTERY INDICATOR

THE reliability of readings of battery-operated measuring instruments depends, of course, on the state of the battery. Even simple instruments are, therefore, provided with a facility (normally a push button) to check the battery voltage. If, however, the state of the battery must be monitored constantly, that type of check is not very reliable. And then there are instruments that have no battery check facility whatsoever.

The indicator shown in Fig. 1 solves all these problems. With jump links JP_1 and JP_2 in the positions shown, D_2 serves primarily as on/off indicator. This low-current LED lights constantly as long as the battery voltage is sufficiently high and the optional alarm input (a) is not actuated. When the battery voltage drops below a value set by P_1, oscillator IC_{1b} is switched on, whereupon D_2 begins to flash at a frequency of about 0.5 Hz. A second oscillator, IC_{1a}, is actuated when a high voltage level is applied to terminal a. The LED will then flash at a frequency of 10 Hz. This additional indication is often useful to alert the user to an operational error.

When JP_1 and JP_2 are in their other position, there is no on/off indication; the quiescent current then drops from about 4 mA to a few µA. If this condition is selected, the connections of D_2 must be changed over (as shown in dashed lines).

The circuit uses the NAND gates of a Type 74HC132 IC, which is suitable for supply voltages, U_i, of 2–6 V. Since the change-over point of the indicator depends on the supply voltage, connected to U_i, this must be regulated. It is, of course, possible, even preferred, to connect U_i to the regulated supply of the relevant measuring instrument. Here, an independent supply of 5 V is assumed. Since the regulator, IC_2, is a low-drop type, the battery voltage may drop to about 5.5 V before the stability of the output voltage (at U_i) becomes questionable.

The design may be adapted for use with higher supply voltages: if IC_1 is replaced by a Type 4093, the circuit becomes suitable for an input voltage, U_i, of up to 18 V. The series resistor of D_2 must, of course, also be adapted: for instance, D_5 should be 3.9 kΩ when U_i = 15 V.

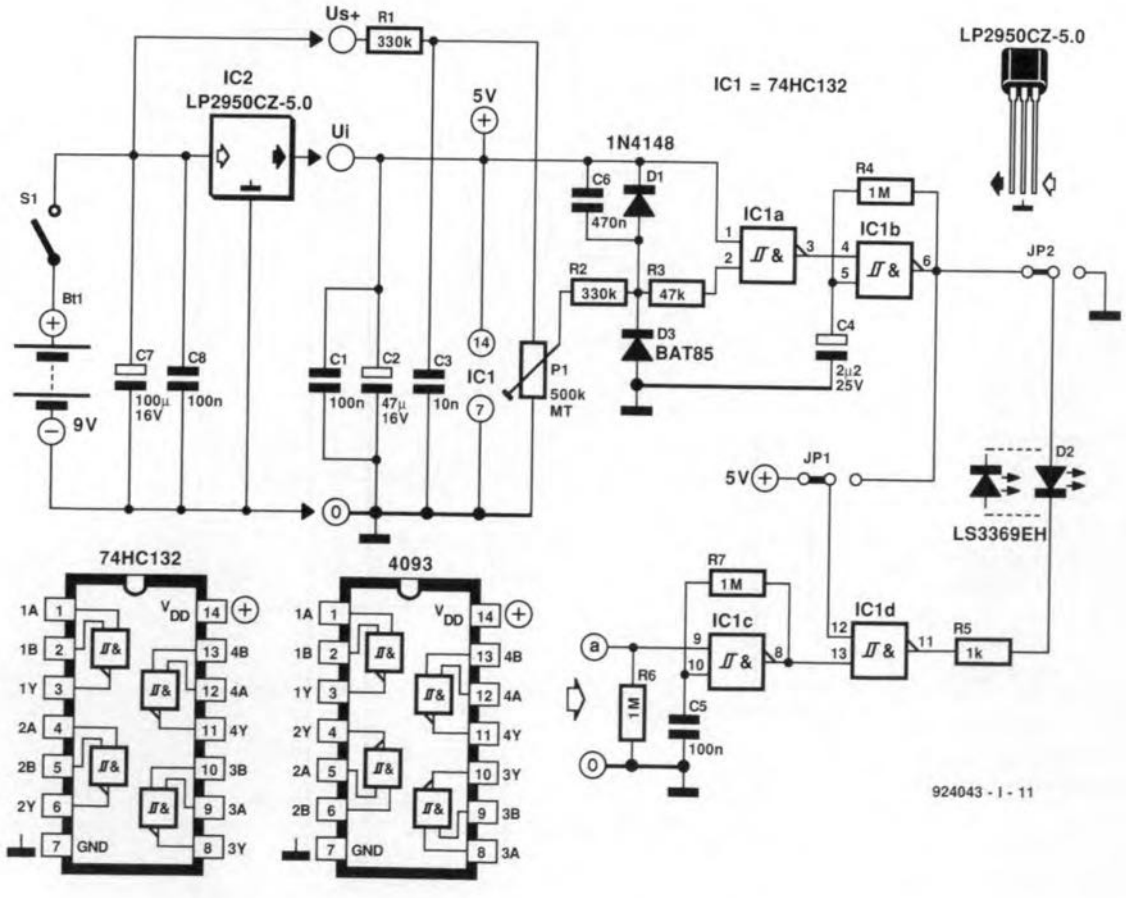
The battery voltage is applied to the input of IC_{1a} via potential divider R_1-P_1. Diode D_1 protects the gate against too high a voltage from a fresh battery.

Although the function of C_6 may not be immediately evident, it is a vital one: the capacitor ensures that the upper switching threshold (about 2.5 V) of IC_{1a} is exceeded briefly on power-on. Oscillator IC_{1b} is then reset. After about one second, the potential at junction R_2-R_3 is a measure of the state of the battery. If that potential lies below about 1.5 V (the lower switching threshold), the oscillator is actuated. If C_6 were not in circuit, the oscillator would not be reset at low battery voltages, resulting in an erroneous low-battery indication.

Preset P_1 (maximum resistance) is adjusted when a variable power supply is connected to U_s+ and set to an output level at which the indicator is to become operational, say, 6 V. Turn P_1 slowly until D_2 begins to flash.

The alarm input, *a*, may be adapted for use with *negative* battery voltages by the circuit shown in Fig. 2.

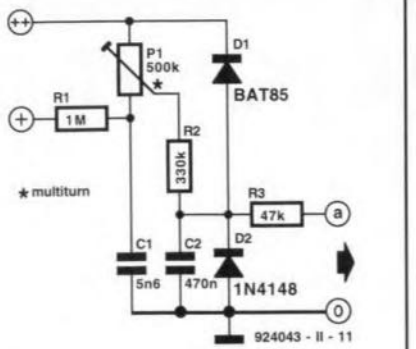
1



In fact, the two circuits together monitor a symmetrical battery supply: the positive line via U_s+ and the negative line via the circuit in Fig. 2, connected to terminal *a* in Fig. 1. When one of the batteries becomes low, D_2 begins to flash: at a frequency of 0.5 Hz in case of the + battery, and at about 10 Hz in case of the – battery. When both batteries become low simultaneously, D_2 flashes with interruptions.

The circuit in Fig. 2 raises the negative battery voltage to above earth level. Note that, because of the loading of its output, R_6 in Fig. 1 must be removed. Connect the ++ line to U_i in Fig. 1, the + line to the negative terminal of the symmetrical battery supply, and 0 to 0 in Fig. 1.

2



Provided all connections are correct, the total current drain rises by only about 10 µA over that of Fig. 1 (assuming two 9-V batteries in series).

Preset P_1 is adjusted in a manner similar to that described above for P_1 in Fig. 1. When the upper switching threshold of IC_{1c} is exceeded, the gate oscillates and D_2 begins to flash. The power-on reset (terminal *a* becomes logic 0) is provided by capacitor C_2. That capacitor is discharged via D_1 and the supply lines.

Diode D_2 protects IC_{1c} against negative input potentials, while capacitor C_1 prevents the circuit being triggered by possible brief noise peaks on the battery voltage.

[J. Ruiters – 924043]

VOLTAGE CONVERTER I

THE limiter is capable of converting a 70–260 V r.m.s. alternating voltage into a 180–350 V direct voltage. For that, a full-wave rectifier, contained in an MC34161, is used as a voltage doubler at low input voltages and as a standard rectifier at high input voltages. In this way, an input voltage variation of ×4 is reflected in an output voltage change of not greater than ×2.

The MC34161 has an integral voltage reference source that provides a voltage of 2.54 V at pin 1. The level of a signal applied to pin 2 is compared internally with a potential of 1.27 V.

Voltage divider R_2-R_3 ensures that the internal comparator changes state when the input voltage rises above 135 V: pin 5 then becomes logic high. The potential at pin 2 is then lower than 1.27 V. The triac is switched off, and this removes the centre link between the output capacitors, C_2 and C_3, so that voltage doubling cannot take place. Diodes D_1–D_4 then operate as a normal bridge rectifier.

Table 1
Input voltage vs output voltage

$U_{a.c.}$	$U_{d.c.}$
70	180
85	218
100	260
125	325
160	212
175	233
200	270

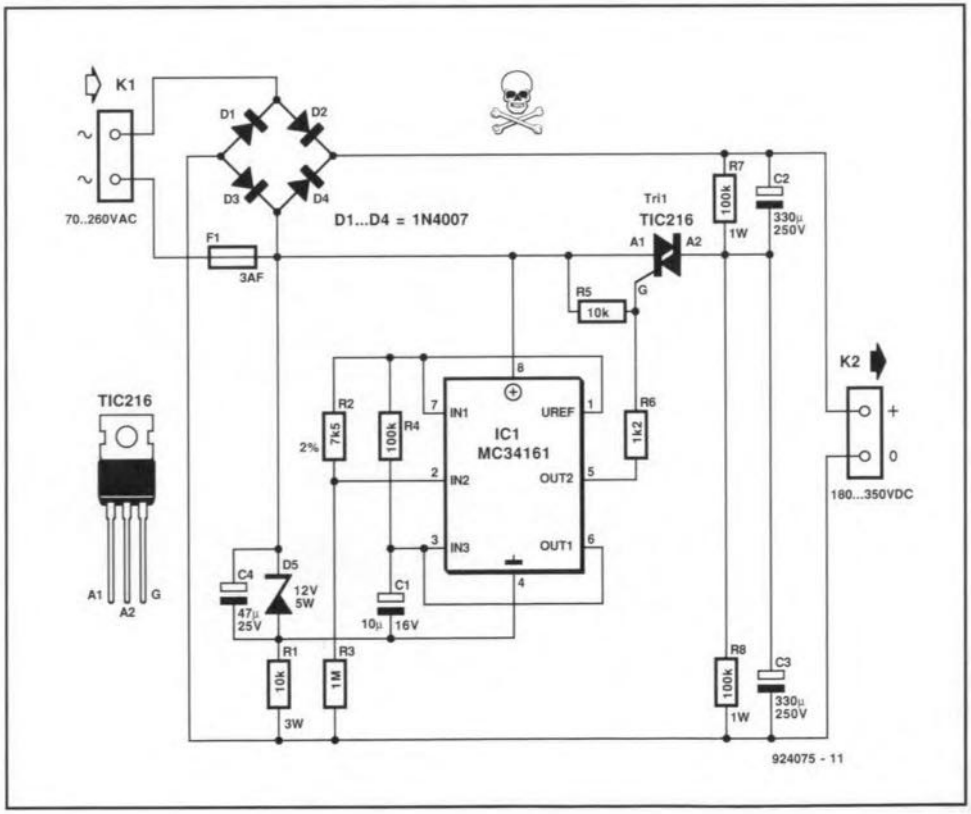
When the input voltage is lower than 135 V, the potential at pin 2 remains higher than 1.27 V: the internal transistor at pin 6 is then off. Because of R_4, pin 3 then carries the reference voltage of 2.54 V. That in turn results in the internal transistor at pin 5 being switched on, so that triac Tri_1 switches from the blocking state to the conducting state. Diodes D_2 and D_3, and capacitors C_2 and C_3, then function as voltage doubler.

Zener diode D_5, in conjunction with R_1 and C_4, ensures that the IC is supplied from a stable 12 V source. The time taken by the circuit to switch from standard rectifier to voltage doubler is determined by R_4-C_1.

The working voltage of capacitors C_2 and C_3 must be ≥250 V.

WARNING: the circuit carries high voltages and must therefore be treated with the greatest care.

(Motorola Application – 924075)



BATTERY REGULATOR FOR SOLAR POWER SYSTEM

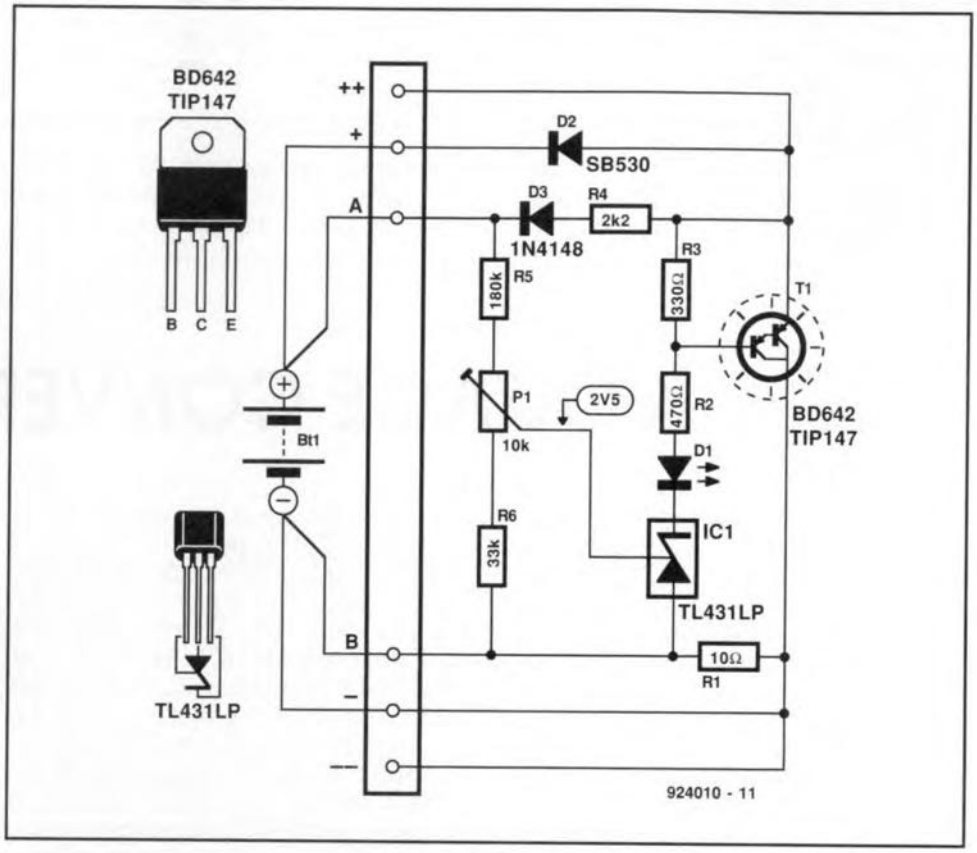
Although newer types of solar cell have come to the fore recently, amorphous cells are bound to be with us for some time to come, mainly because of their low cost. Most solar cells based on amorphous technology have a relatively high internal resistance, which results in large differences between the loaded and 'open-circuit' output voltages. Where a rechargeable battery is used as an energy storage device, a voltage regulator circuit is in order that charges the battery when the cell output voltage is high, and forms a minimum load on the battery when the cell output voltage is low.

For relatively small solar power systems, the parallel (or 'shunt') regulator is a viable alternative. Apart from a single (Schottky) diode, nothing is inserted between the solar cell and the battery. Since the supply voltage is furnished by the solar panel, the regulator works always, even if the battery is fully discharged or not connected. This ensures the best possible protection against overvoltage of all circuits powered by the solar cell (or array of cells).

The heart of the shunt regulator presented here is formed by a Type TL431LP precision voltage regulator from National Semiconductor. When the solar cell output voltage rises above the level set with preset P_1, a current starts to flow through R_3-R_2-D_1. When the current has risen to about 5 mA, transistor T_1 starts to conduct. The transistor used here, a BD642, may be replaced by almost any other, similar, power darlington, for example, the TIP147. The collector of the BD642 is conveniently connected to ground, which means that the device can be bolted direct on to a heat sink.

Since the regulator is capable of shunting quite high currents, it has separate sense inputs, 'A' and 'B', to monitor the battery voltage. The solar cell is connected to terminals '++' and '– –'. Resistor R_4 limits the current through D_3 in the event of the high-power series diode, D_2, breaking down. Not shown in the circuit diagram, but required in the interest of safety, are fuses in series with the battery and the load(s). Also, do not forget to connect a surge arrester in parallel with the solar cell.

The Schottky diode used here, an SB530 from Conrad, is capable of passing up to 5 A. For panel output currents up to 3 A, it may be replaced by the more familiar 1N5401 (which, unfortunately, has a slightly higher forward drop voltage). Talking of ratings: the heat sink on to which the power transistor is bolted must

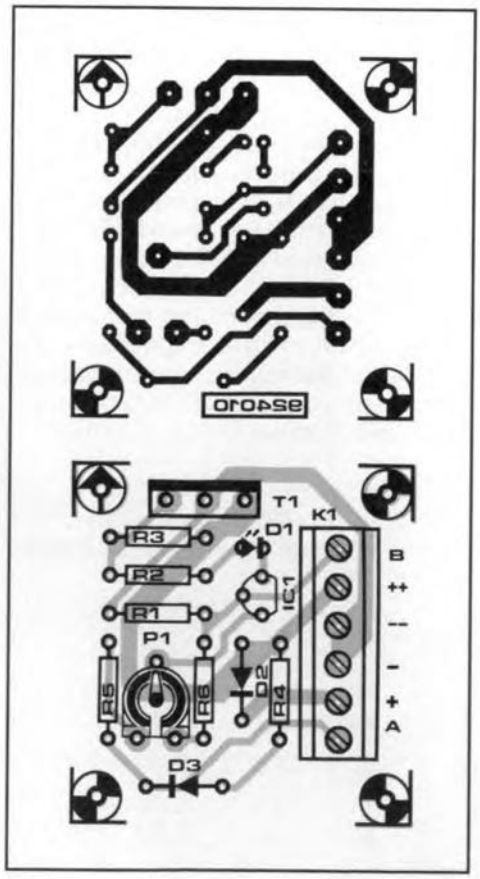


PARTS LIST

Resistors:
R1 = 10Ω
R2 = 470Ω
R3 = 330Ω
R4 = 2kΩ2
R5 = 180kΩ
R6 = 33kΩ
P1 = 10kΩ preset H

Semiconductors:
T1 = TIP147 or BD642
D1 = LED
D2 = SB530
D3 = 1N4148
IC1 = TL431LP

Miscellaneous:
K1 = 6-way PCB terminal block; pitch = 5mm



have a thermal resistance of 1.5 KW^{-1} or smaller, in which case power dissipation levels up to 40 W can be handled without problems. For very high power applications, connect a number of power darlingtons is parallel, and connect their emitters via 0.22-Ω current distribution resistors. Obviously, to cope with the increased power dissipation, the size of the heat sink must be increased accordingly.

The component values shown result in a battery voltage adjustment range of 13.4–17.6 V. This is on the high side for most (lead-acid and gel-type) batteries, which do not fare very well at charge voltages greater than 13.8 V. The circuit can be modified for an output voltage range of about 11–16 V by fitting: R_5=220 kΩ; R_6=47 kΩ; P_1=25 kΩ. ■

(K. Schönhoff – 924010)

from National Semiconductor. When the solar cell output voltage rises above the level set with preset P_1, a current starts to flow through R_3-R_2-D_1. When the current has risen to about 5 mA, transistor T_1 starts to conduct. The transistor used here, a BD642, may be replaced by almost any other, similar, power darlington, for example, the TIP147. The collector of the BD642 is conveniently connected to ground, which means that the device can be bolted direct on to a heat sink.

Since the regulator is capable of shunting quite high currents, it has separate sense inputs, 'A' and 'B', to monitor the battery voltage. The solar cell is connected to terminals '++' and '– –'. Resistor R_4 limits the current through D_3 in the event of the high-power series diode, D_2, breaking down. Not shown in the circuit diagram, but required in the interest of safety, are fuses in series with the battery and the load(s). Also, do not forget to connect a surge arrester in parallel with the solar cell.

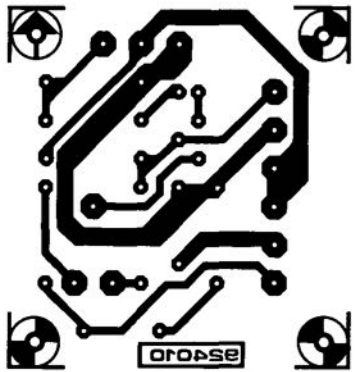
The Schottky diode used here, an SB530 from Conrad, is capable of passing up to 5 A. For panel output

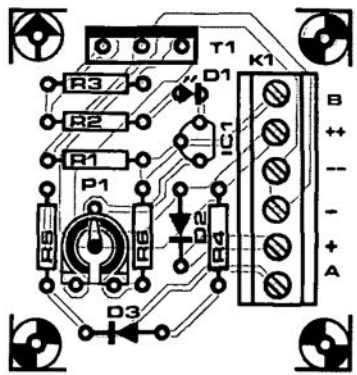
PARTS LIST

Resistors:
R1 = 10Ω
R2 = 470Ω
R3 = 330Ω
R4 = 2kΩ2
R5 = 180kΩ
R6 = 33kΩ
P1 = 10kΩ preset H

Semiconductors:
T1 = TIP147 or BD642
D1 = LED
D2 = SB530
D3 = 1N4148
IC1 = TL431LP

Miscellaneous:
K1 = 6-way PCB terminal block; pitch = 5mm





LOW-DROP REGULATOR II

IF a stable 5-V direct voltage is to be derived from an already low supply voltage, the 4805 from SGS Thomson is probably the most suitable regulator IC available at present. The popular 7805 does not work so well with supplies lower than about 8 V. The 4805, on the other hand, needs an input voltage that is only about 0.5 V higher than its output voltage. Its data sheets state that its output voltage remains stable so lang as the input voltage does not drop below 5.7 V. That voltage, by the way, is the worst-case voltage when the output current is 400 mA. In practice, therefore, the regulator normally works fine with input voltage as low as 5.4 V.

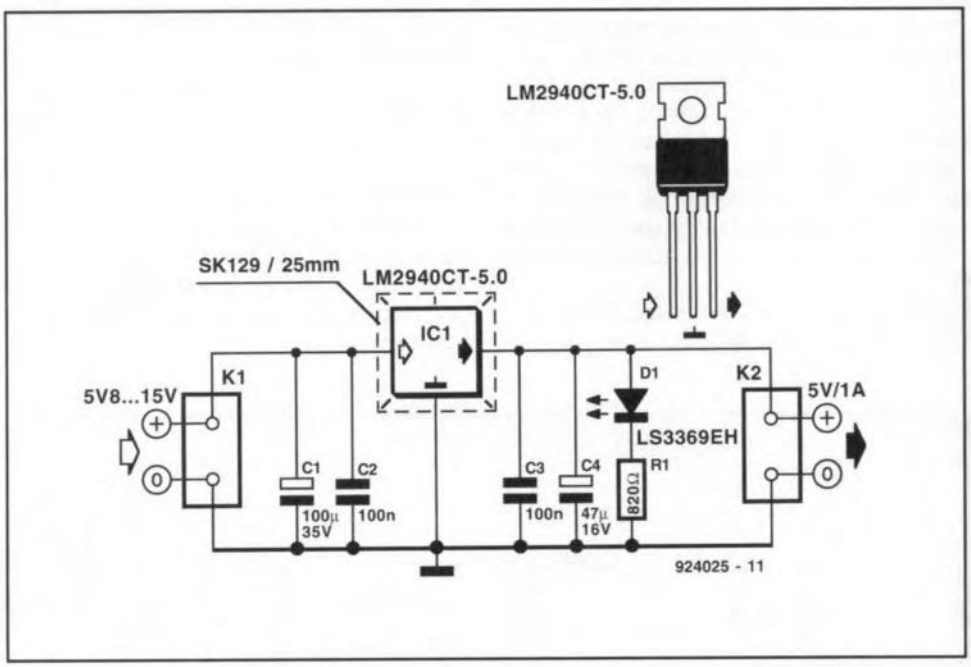
What to do if the output current is more than 400 mA? Well, in that case, and for output currents up to 1 A, the LM2940T appears to be just about the best available. This IC from National Semiconductor is available in three variations: 5 V, 8 V, and 10 V. The 5-V version, in which we are principally interested here, is type-coded LM2940T-5. These ICs are pin-compatible with the 7805 and 4805, which makes it possible for an existing low-drop supply based on one these devices to be upgraded fairly simply.

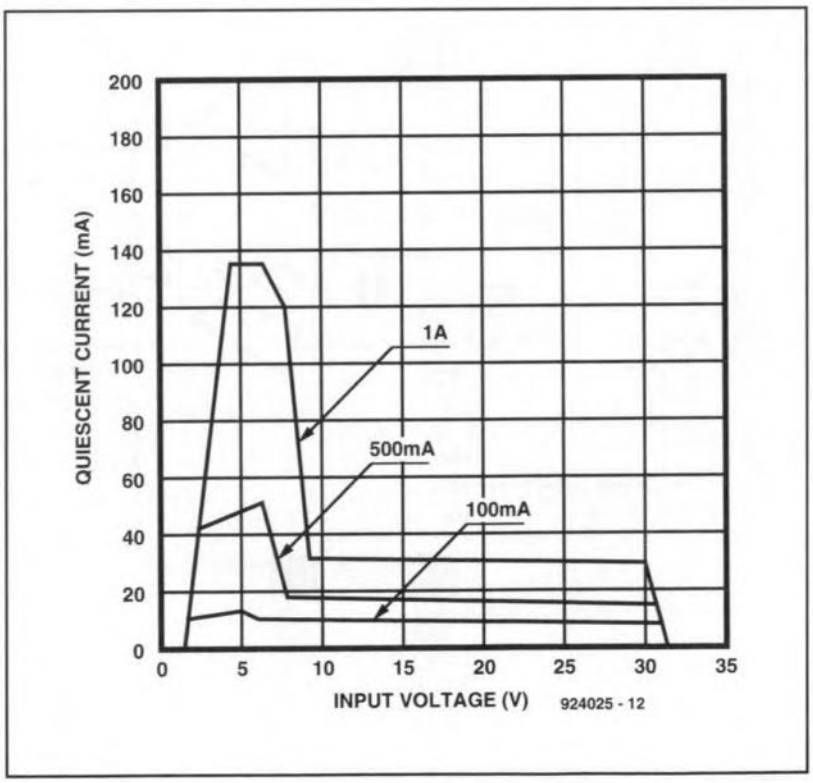
For completeness' sake, the circuit diagram shows a simple 5-V design. The only really important parameter here is the capacitance of decoupling capacitor C_4. According to the relevant data sheets, its value should be not less than 22 µF to ensure correct stability.

If the input voltage does not go above about 7.5 V, a heat sink is not necessary. If the regulator is required to operate at a higher output voltage and the full output current, a suitable heat sink is imperative. A heat sink rated at 6.5 °C W^{-1} makes the low-drop circuit suitable for input voltages up to 15 V at full output current or up to 25 V at 500 mA. The worst case input voltage is 5.8 V..

The LM2940T, like the 7805, is short-circuit-proof, but it does draw a rather high quiescent current as shown in the characteristic curves.

[J. Ruiters – 924025]





WATER PUMP CONTROL FOR SOLAR POWER SYSTEM

IN most small solar power systems using a boiler it is required that the water circulation pump is not switched on until the temperature of the collector (the solar panel) exceeds that of the water in the vessel. Here, a two-sensor monitor is presented that enables this condition to be met. One sensor is fitted on the collector, the other on the water vessel. The control shown here has two adjustments: one for the temmperature difference at which the pump starts to operate, and one for the temperature difference at which it is switched off. Although these settings are independent, the switch-off level must be lower than the switch-on level. Calibration in degrees Celcius is simple because the gradient of the voltage at the wiper of the potentiometers (or presets) that set the on/off temperatures is exactly 0.1 V $°C^{-1}$.

The two temperature sensors Type LM334 are adjusted to supply a temperature gradient of 1µA $°C^{-1}$. Unequal sensor temperatures therefore produce a current flow at their junction. The voltage across R_1 is directly proportional to the temperature difference measured. This enables the switching thresholds of the on/off control to be set with the aid of two presets: the 'on' preset (P_4) is adjusted to, say, 3 °C, and the 'off' preset (P_3) to 1 °C. The range of the two presets is about 5 °C.

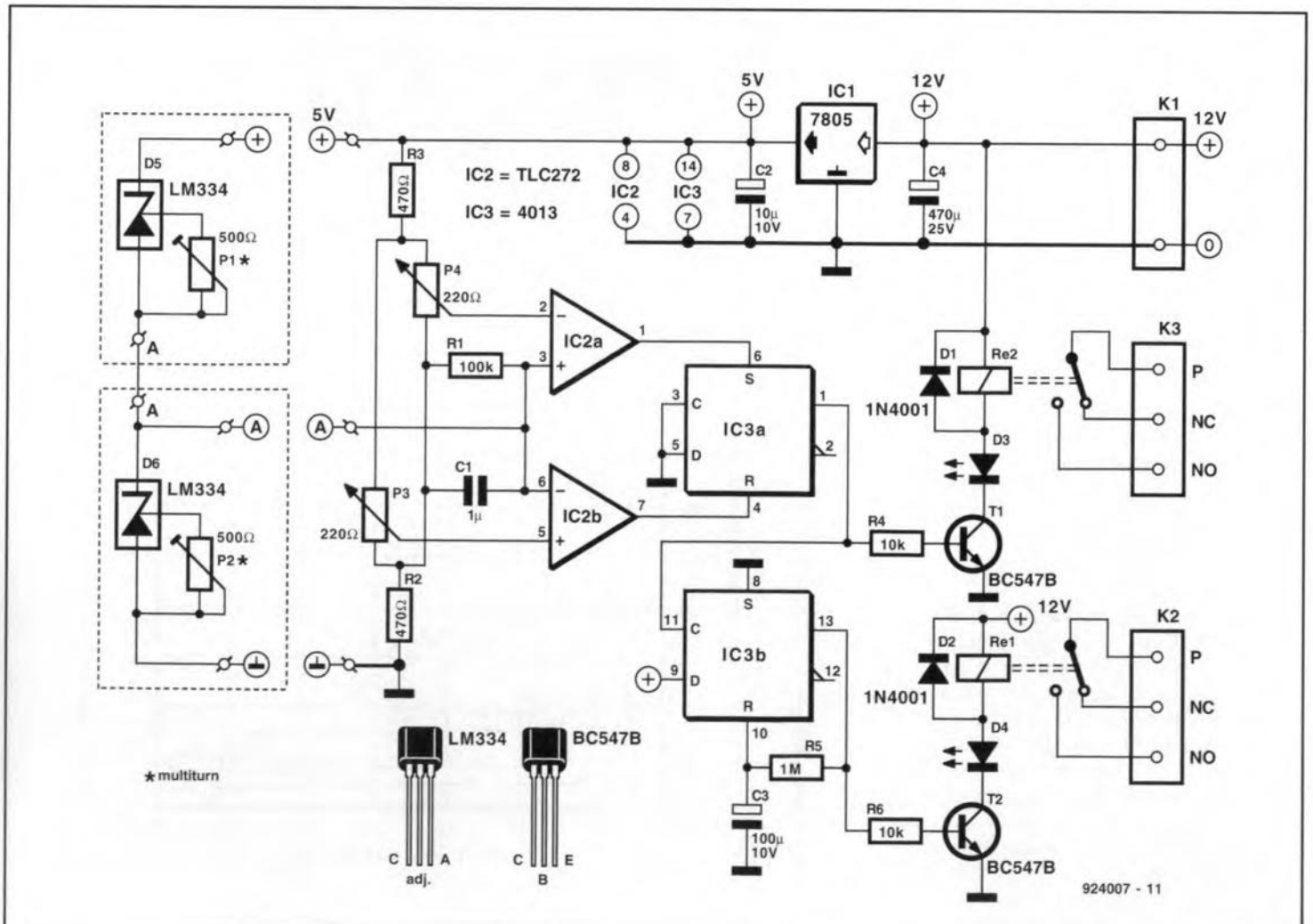
The sensors used here supply a current rather than a voltage. This eliminates thermocouple effects caused by temperature changes on the connecting cables between the sensors and the circuit. If voltage-type sensors such as PTCs or NTCs were used, the circuit would have become more complex because of the required compensation. The AD590 may be used instead of the LM334. Note, however, that the AD590 does not require an adjustment preset or resistor.

Relay Re_2 switches the pump on and off. A second relay, Re_1, comes on after Re_2. It is optional, and may be used to switch the pump briefly to a higher speed, which is required in some solar heating systems to increase the intial water flow, or to fill the system.

The circuit is calibrated by setting equal sensor currents at equal sensor temperatures. The sensor current equals

$$[273 + T_a)]\ \mu A,$$

where T_a is the ambient temperature in degrees Celsius. Thus, at a room temperature of 20 °C, presets P_1 and P_2 are adjusted until the current flow through each sensor is 293 µA. A few microamps more or less will not make much difference, as long as the sensor currents are equal. It is best to first adjust one sensor only. Start by connecting a microammeter between 'A' and ground, and



PARTS LIST

Resistors:
R1 = 100kΩ
R2;R3 = 470Ω
P3;P4 = 220Ω linear potentiometer
R4;R6 = 10kΩ
R5 = 1MΩ
P1;P2 = 500Ω mutiturn preset

Capacitors:
C1 = 1µF MKT
C2 = 10µF 10V radial
C3 = 100µF 10V radial
C4 = 470µF 25V radial

Semiconductors:
D1;D2 = 1N4001
D3;D4 = LED
D5;D6 = LM334
IC1 = 7805
IC2 = TLC272
IC3 = 4013
T1;T2 = BC547B

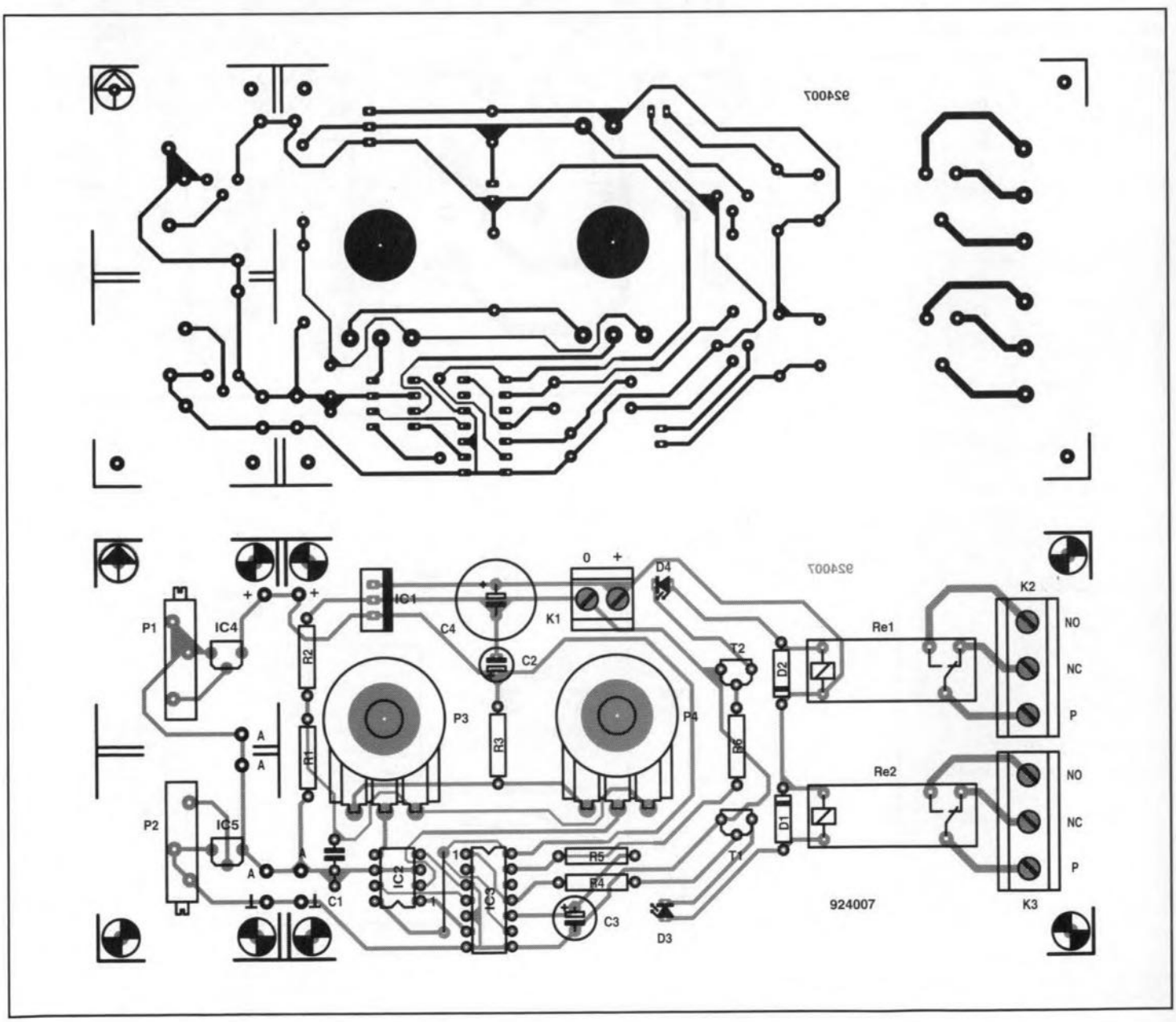
Miscellaneous:
K1 = 2-way PCB terminal block, pitch 5mm.
K2;K3 = 3-way PCB terminal block, pitch 7.5mm.
Re1;Re2 = GBR 10.2-11.12 (12V coil, contact 250V @8A).
Enclosure: about155x61x90 mm; e.g., Retex Gibox Type RG3.
PCB Type 924007.

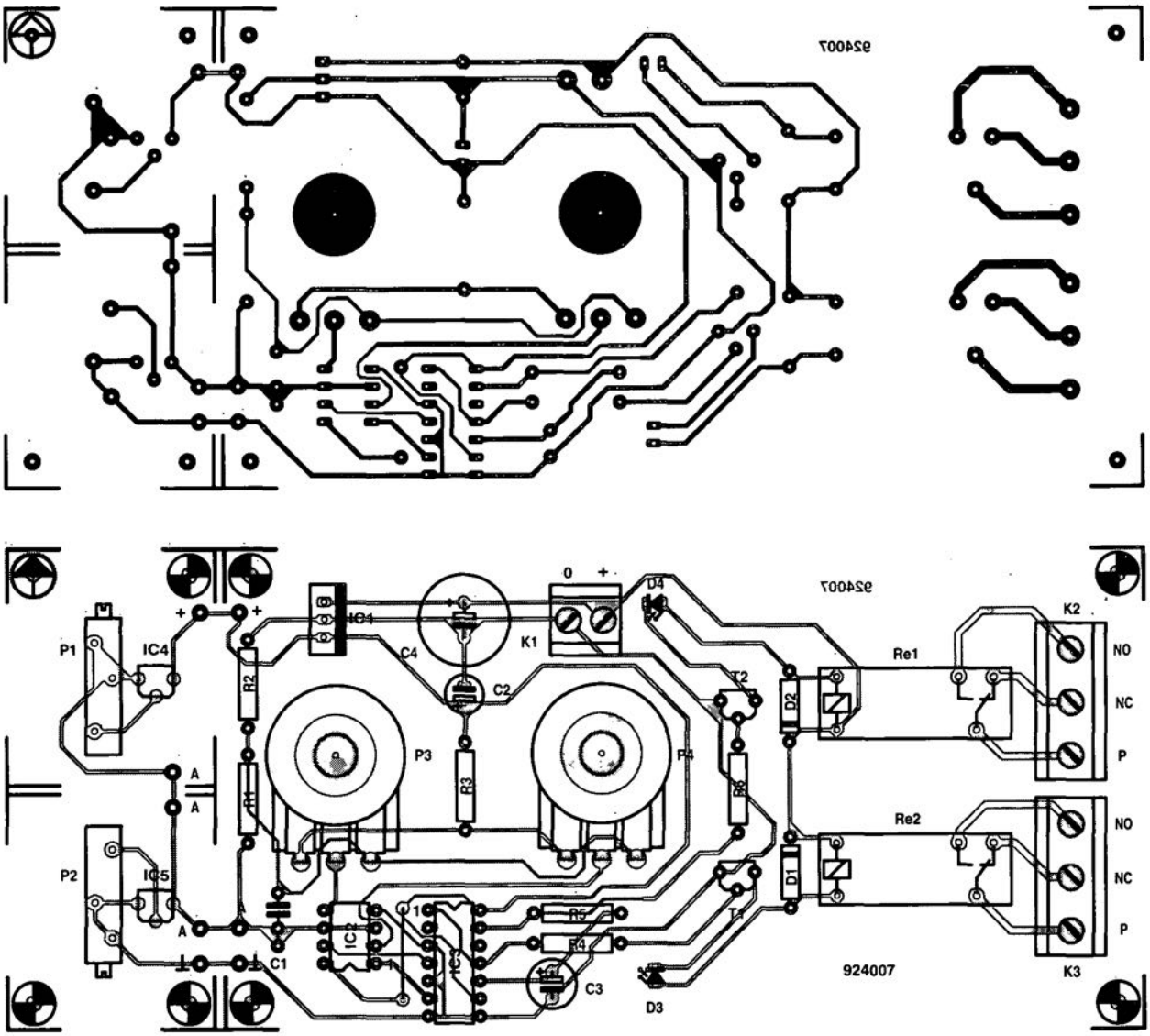
adjust P_1 . Next, adjust the other preset until the voltage across R_1 is nought. It will be clear that these initial adjustments require that the two LM334 are at the same temperature.

Current consumption of the on/off control is about 11 mA plus about 35 mA for each relay.

The dimensions of the printed circuit board are geared to the size of the box mentioned in the parts list. The potentiometers are fitted with the spindles at the track side of the board.

(K. Walraven – 924007)




924007
924007
P1
IC4
R2
C4
K1
D4
K2
Re1
NO
NC
P
T2
D2
C2
P3
P4
R3
R6
A
A
P2
IC5
R1
IC1
IC2
R5
R4
T1
D1
Re2
NO
NC
P
C1
C3
D3
924007
K3

POWER SUPPLY TESTER

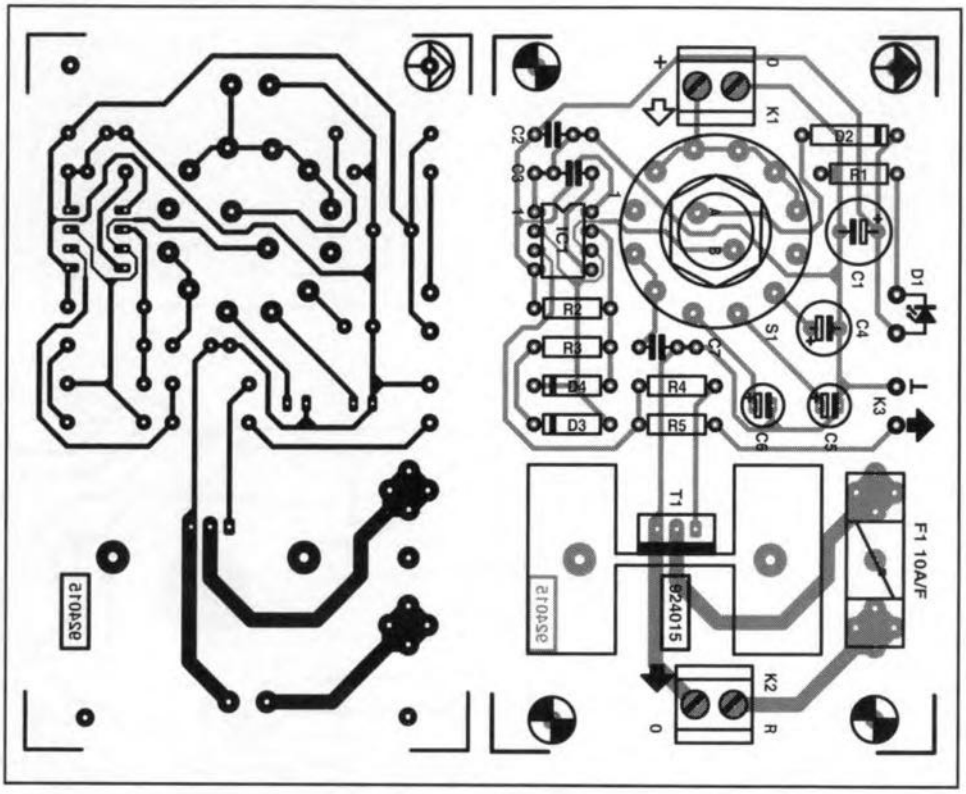
THIS little circuit enables you to measure the so-called dynamic response of a d.c. power supply. A power MOSFET, T_1, is used to switch the supply load on and off at a user selectable rate. The response of the supply to these fast load variations is displayed on an oscilloscope.

The switching rate is selected with the aid of a rotary switch, S_1, which also serves as the on/off switch. The available switching frequencies are: 10 Hz, 100 Hz, 1 kHz and 10 kHz. The well-known 555 timer IC is used to supply the switching signal. Diodes D_3 and D_4 cause the astable multivibrator to supply an output signal with a duty factor of about 0.5. The switching transistor, T_1, is protected against too high currents by a fast 10-A fuse inserted in the drain line. The tester may be powered by any regulated d.c. supply with an output voltage between 6 V and 15 V. However, this must not be the supply under test! Given the low current consumption of the tester (40 mA max.), a 9-V battery is an excellent power source.

The tester is extremely simple to use. First, select the load resistance of the supply you wish to test; say, 12 Ω/15 W for a 12-V, 1-A PSU. This resistor is connected between output 'R' of the tester, and the '+' output of the PSU. The '0' output of the tester goes to the '-' (or '0') terminal of the PSU. Next, connect the scope input to the PSU outputs, and the trigger input to K_3 of the tester. Switch on the scope, the PSU and the tester. The scope will now display the dynamic regulation characteristic of the PSU at the given output current (1 A) and the selected switching rate (initially, 10 Hz).

Construction of the tester is straightforward on the small printed circuit board shown here. The power MOSFET is bolted on to a small PCB-mount heat sink, and will not run very hot even when the maximum permissible drain current (about 10 A) is approached.

(J. Ruiters – 924015)



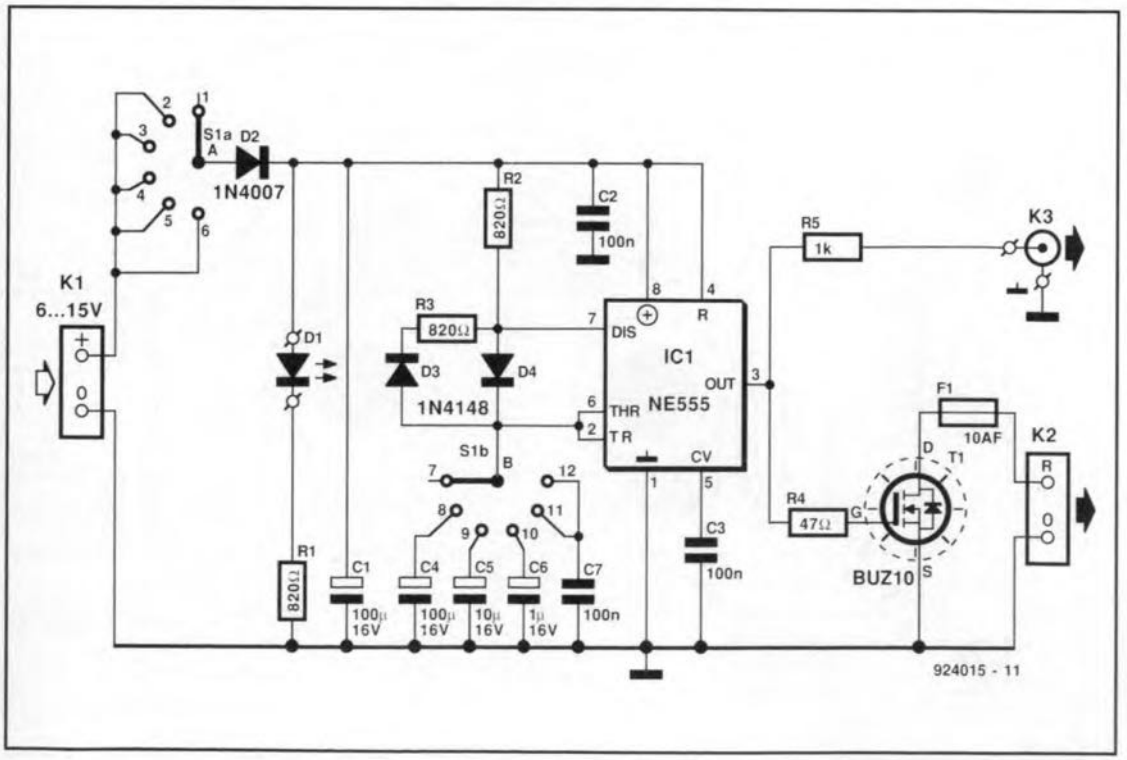
PARTS LIST

Resistors:
R1;R2;R3 = 820Ω
R4 = 47Ω
R5 = 1kΩ

Capacitors:
C1 = 100µF 16V radial
C2;C3;C7 = 100nF
C4 = 100µF 16V radial
C5 = 10µF 16V radial
C6 = 1µF 16V radial

Semiconductors:
D1 = LED, red, 5mm
D2 = 1N4007
D3;D4 = 1N4148
T1 = BUZ10
IC1= NE555

Miscellaneous:
K1;K2 = 2-way PCB terminal block; pitch 5mm.
K3 = panel mount BNC socket.
S1 = 2-pole 6-way PCB mount rotary switch.
F1 = 10A fast fuse plus PCB mount holder and cap.
Heat sink 5K/W, e.g. SK129/38.1mm.

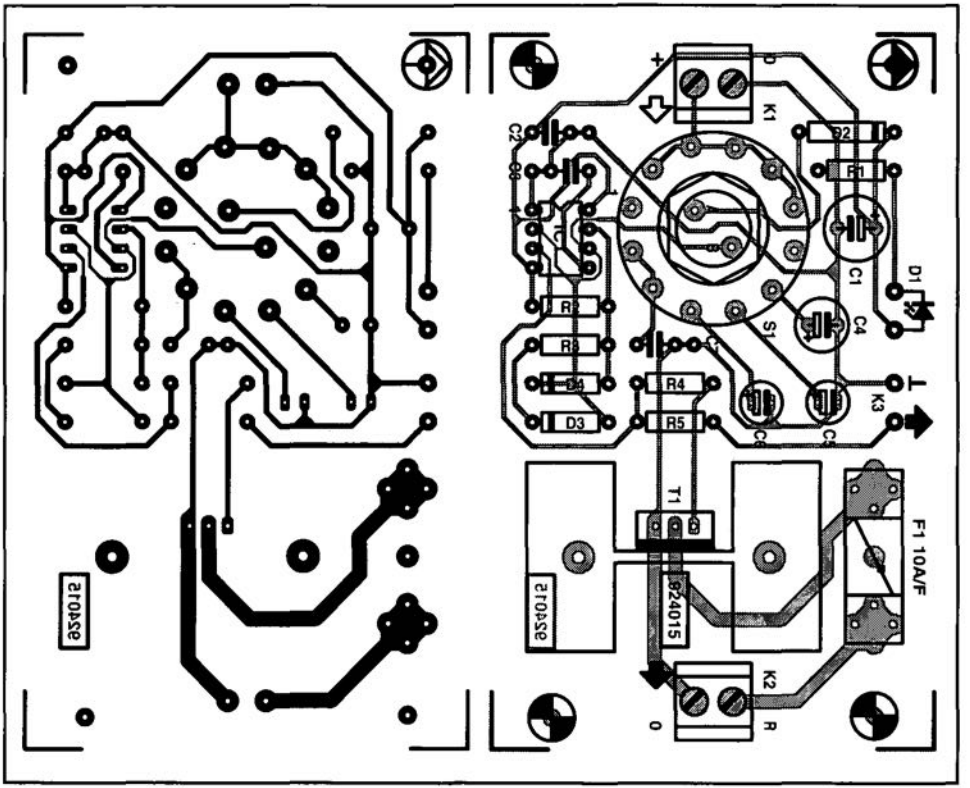


10 Hz, 100 Hz, 1 kHz and 10 kHz. The well-known 555 timer IC is used to supply the switching signal. Diodes D_3 and D_4 cause the astable multivibrator to supply an output signal with a duty factor of about 0.5. The switching transistor, T_1, is protected against too high currents by a fast 10-A fuse inserted in the drain line. The tester may be powered by any regulated d.c. supply with an output voltage between 6 V and 15 V. However, this must not be the supply under test! Given the low current consumption of the tester (40 mA max.), a 9-V battery is an excellent power source.

The tester is extremely simple to use. First, select the load resistance of the supply you wish to test; say,

PARTS LIST

Resistors:
R1;R2;R3 = 820Ω
R4 = 47Ω
R5 = 1kΩ



PC FAN CONTROL

IT is an unfortunate and well-known fact that most PCs of the 'IBM and compatible' type make a lot of noise, which is both undesirable (as regards noise in the working environment) and unnecessary (as regards the actual power consumption, which is often quite low). Many fans in PC power supplies are over-rated, noisy, and run at a constant, high, speed. Fortunately, the authors found that such fans can do their protective job just as well at far lower speeds.

The speed controller presented here consists of (1) a temperature monitor based on a LED as the sensor device, and (2) an idle speed regulator. The combination of the temperature monitor and the idle speed regulator results in a linear relation between temperature and fan speed. In other words: the fan will never run faster than strictly necessary. By virtue of the two separate regulator circuits, there is no interaction between idle speed and temperature regulation, as with many other (less sophisticated) fan controllers. The result is low fan speed (low noise) at low temperatures, as well as good cooling and a safe start-up at all times.

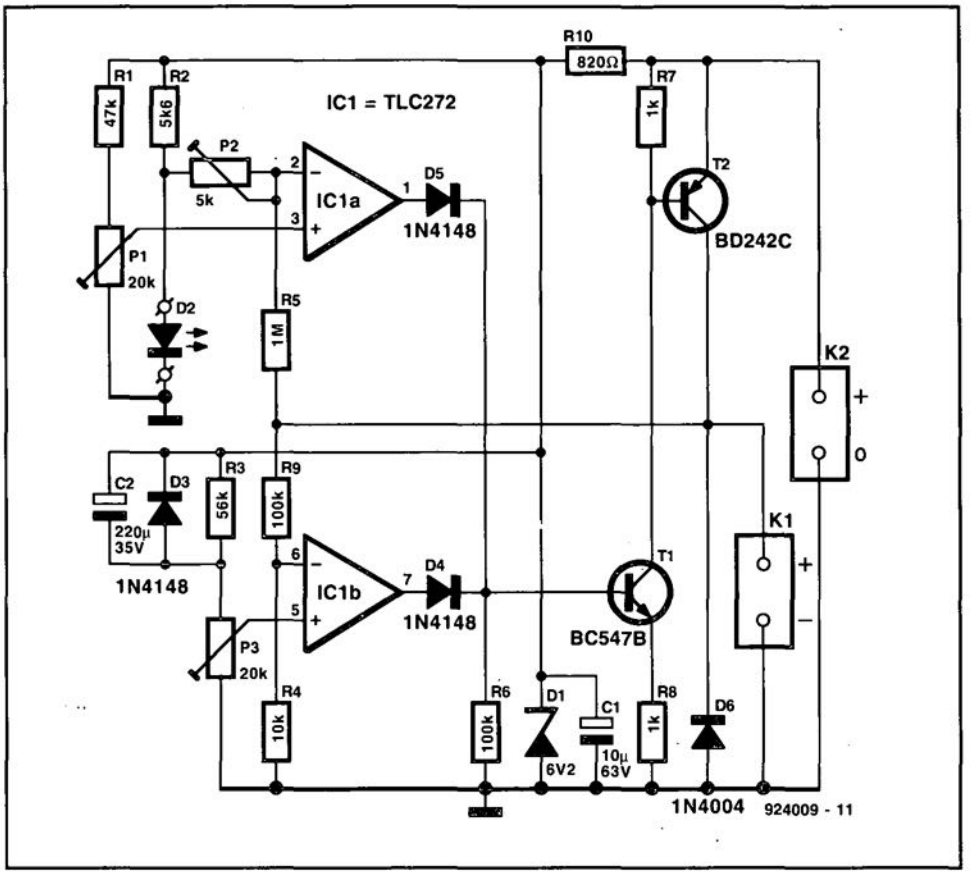
When the temperature inside the PC rises, the voltage drop across the red LED, D_2, decreases by approximately -2 mV K^{-1}. This results in a higher output voltage of opamp IC_{1A}. Preset P_1 is used to set the start level, while P_2 determines the slope of the regulator characteristic. The adjustment range of the idle-to-full speed regulation is about 2 °C to 30 °C.

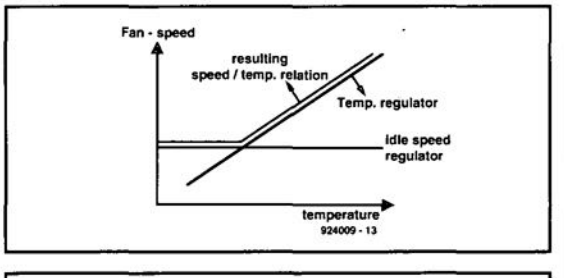
The idle speed is set to the desired value by adjusting P_3. Capacitor C_2 ensures a 4-second full-speed start up period, while diode D_3 restarts the fan after a short interruption on the mains.

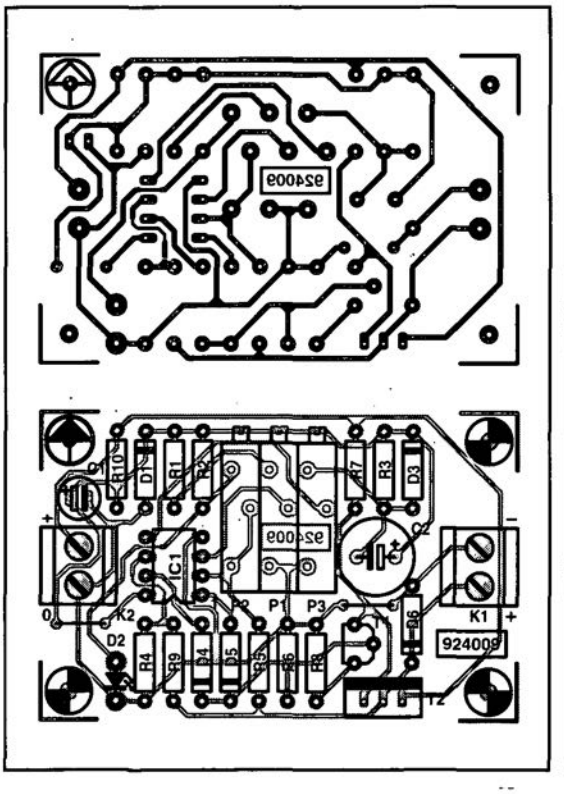
The outputs of the temperature monitor and the idle speed regulator are 'joined' by two diodes, D_4 and D_5, at the base of T_1. The regulator is stabilized by feeding a small portion of the fan voltage back to the - inputs of the opamps.

The circuit is built on a small printed circuit board that can be fitted into the PC's power supply. The LED may have to be moved off the board, and connected with wires, to enable it to be fitted in a position where temperature changes are best noticed.

(L. Svenkerud and A. Kristiansen – 924009)







PARTS LIST

Resistors:
R1 = 47kΩ
R2 = 5kΩ6
R3 = 56kΩ
R4 = 10kΩ
R5 = 1MΩ
R6;R9 = 100kΩ
R7;R8 = 1kΩ
R10 = 820Ω
P1;P3 = 20kΩ multiturn preset
P2 = 5kΩ multiturn preset

Capacitors:
C1 = 10µF 63V radial
C2 = 220µF 25V radial

Semiconductors:
D1 = 6V2 0.4W zener diode
D2 = LED, red, 5mm
D3;D4;D5 = 1N4148
D6 = 1N4004
T1 = BC547B
T2 = BD242C
IC1 = TLC272

Miscellaneous:
K1;K2 = 2-way PCB terminal block, pitch 5mm.

HALOGEN LAMP PROTECTOR

HALOGEN lamps, particularly high-wattage ones, tend to draw very high currents when they are cold, because they then have a very low resistance: of the order of 0.1 Ω or lower. If such a light is operated from a 24 V battery, a switch-on peak current of over 200 A may flow. This is highly detrimental to the life span of the light, which after only a few switch-ons may give up the ghost. That costly situation may be prevented by gradually building up the power supplied to the lamp. Since operation is from a d.c. source, the only practical way of so doing is by pulse-width modulation. With that technique, the voltage to the lamp is switched from zero with increasing pulse width, while the current is smoothed by a coil, so that its average level increases gradually. Switching is carried out with two MOSFETs Type BUZ11. This type is characterized by an extremely low channel resistance, which is typically 0.03 Ω for a gate-source voltage of 15 V; moreover, the can handle continuous currents of up to 30 A and pulsed ones of up to 120 A. By connecting the two in parallel, the current is split two ways: not exactly 50/50, of course, but near enough to ensure that on switch-on the devices remain within their limits.

The control circuit for the MOSFETs, T_2 and T_3, provides nothing new. A regulator, IC_1, ensures that the supply to the circuit cannot rise too high: it is set for about 18.5 V. The battery voltage cannot be used directly, because, among others, the gate-source voltage of the MOSFETs must not be higher than 20 V.

A sort of triangular waveform is generated by Schmitt trigger IC_{2a}; R_2 and R_4 ensure that the operating point of the opamp is half the supply voltage. Because of the feedback via R_6-C_5, the output waveform is rectangular. However, the voltage across C_5 is an exponential waveform, that is more or less triangular. That voltage is compared by IC_{2b} with the terminal potential of C_6, which, after switch-on, rises gradually.

As long as the voltage across C_5 is lower that at the non-inverting input of IC_{2b}, the output of that opamp will be high. As soon as the inverting input reaches a potential higher than that at the +ve input, the output changes state, which is accelerated by the positive feedback via R_{10}.

The higher the terminal voltage of C_6, the longer the output of IC_{2b} will remain high. Eventually, it will reach a value higher than the maximum voltage across C_5: pin 7 of IC_{2b} is then permanently high. The lamp is then no longer switched on and off, but remains on.

The Type CA3240 dual opamp in the IC_2 position has the advantage that its output can become almost zero, but the disadvantage that it cannot sink relatively large currents. Because of that, T_1 ensures that the gate capacitances of T_2 and T_3, together 2–10 nF, are discharged rapidly. Those gate capacitances are charged again (that is, T_2 and T_3 are driven into conduction) by IC_{2b} via D_2. An additional driver is not needed, because the CA3240 can source enough current at high levels. When the FETs are on, their gate potential is about 16 V.

When the lamp is switched off, C_6 is discharged immediately, so that the circuit is ready at once to switch it on again. To ensure that on switch-off the induced potential across L_1 does not rise above the maximum level of the drain-source voltage (50 V), the coil is shunted by D_3. This needs to be a fast type (25 ns or better) that can handle currents of up to 30 A.

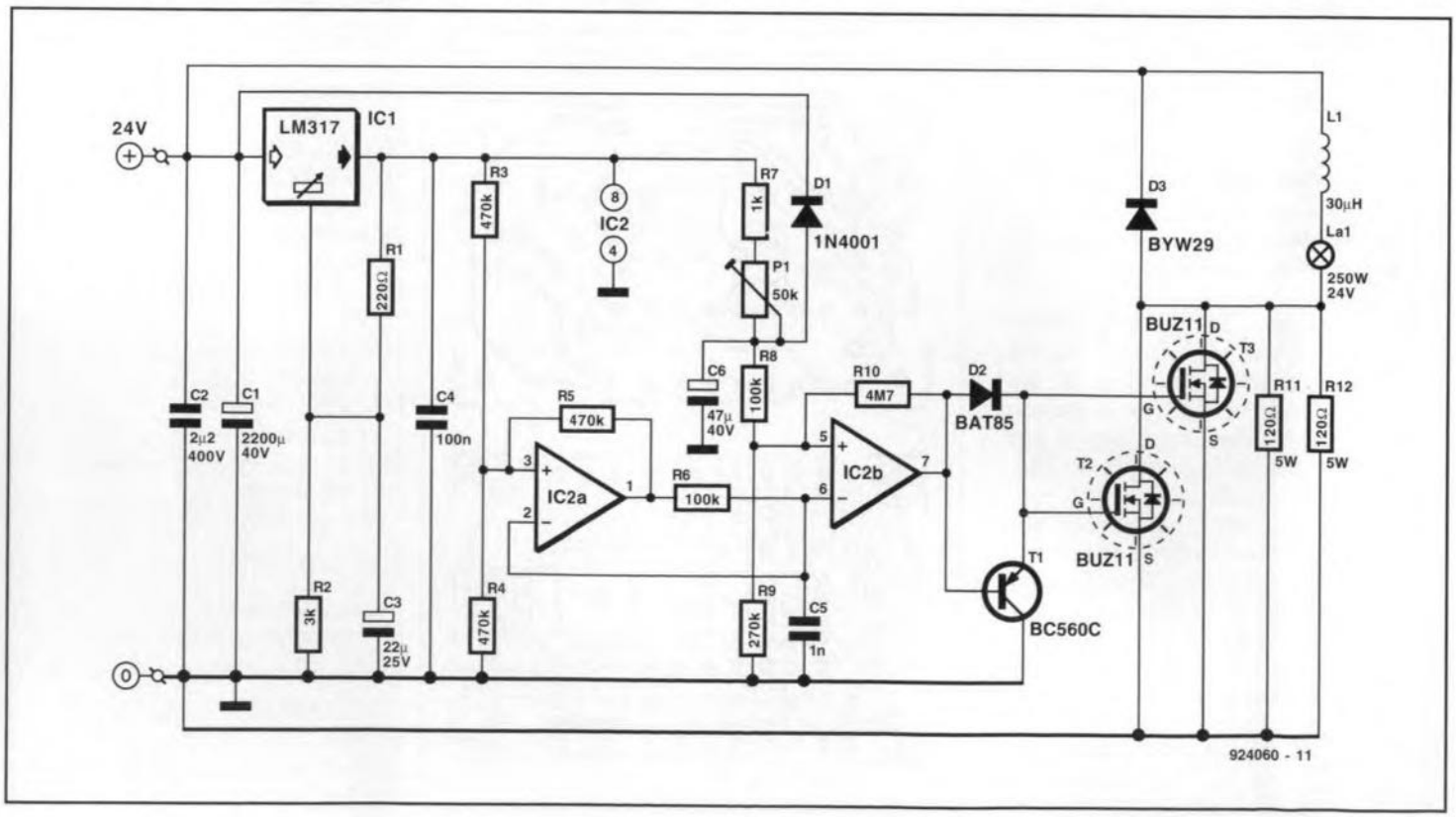
Resistors R_{11} and R_{12} provide the lamp with some voltage before the MOSFETs switch on.

The speed at which the circuit switches the lamp on is preset with P_1; normally, it will be sufficient to set this to the centre of its travel.

It is advisable to mount the FETs on a heat sink, although their dissipation is of the order of 1.6 W only.

Capacitors C_1 and C_2 must be able to handle high-frequency pulse currents of up to 30 A.

Inductor L_1 must ensure that the lamp current does not exceed a predetermined value: the larger the in-



ductance, the lower the maximum level of the current. However, the physical dimensions of the coil must be acceptable. In the prototype, the maximum lamp current was set at 30 A. At a switching frequency of 7 kHz, an inductance of 30 µH is sufficient. Moreover, to avoid saturation problems, the coil is an air-cored one.

It is made by winding 45 turns of 1.5 mm ($^1/_{16}$ in) dia. enamelled copper wire in three layers on a 24 mm ($^{15}/_{16}$ in) dia. round former. During the winding, apply some glue from time to time to the turns.

The current drawn by the circuit is primarily that through the lamp: with a 250 W lamp and a 24 V battery, the current is some 10 A.

(J.J. Paauwe – 924060)

EXTRA BRAKE LIGHT

THERE are many cars on the road that could do with an extra brake light, particularly one high up that can be seen by the third, fourth or fifth car behind it. That proposed here consists of a running-light bar of LEDs that starts again and again when all LEDs light. In some countries, this may not be allowed—check with your local highway or police department, but it can be used, anyway, in model cars.

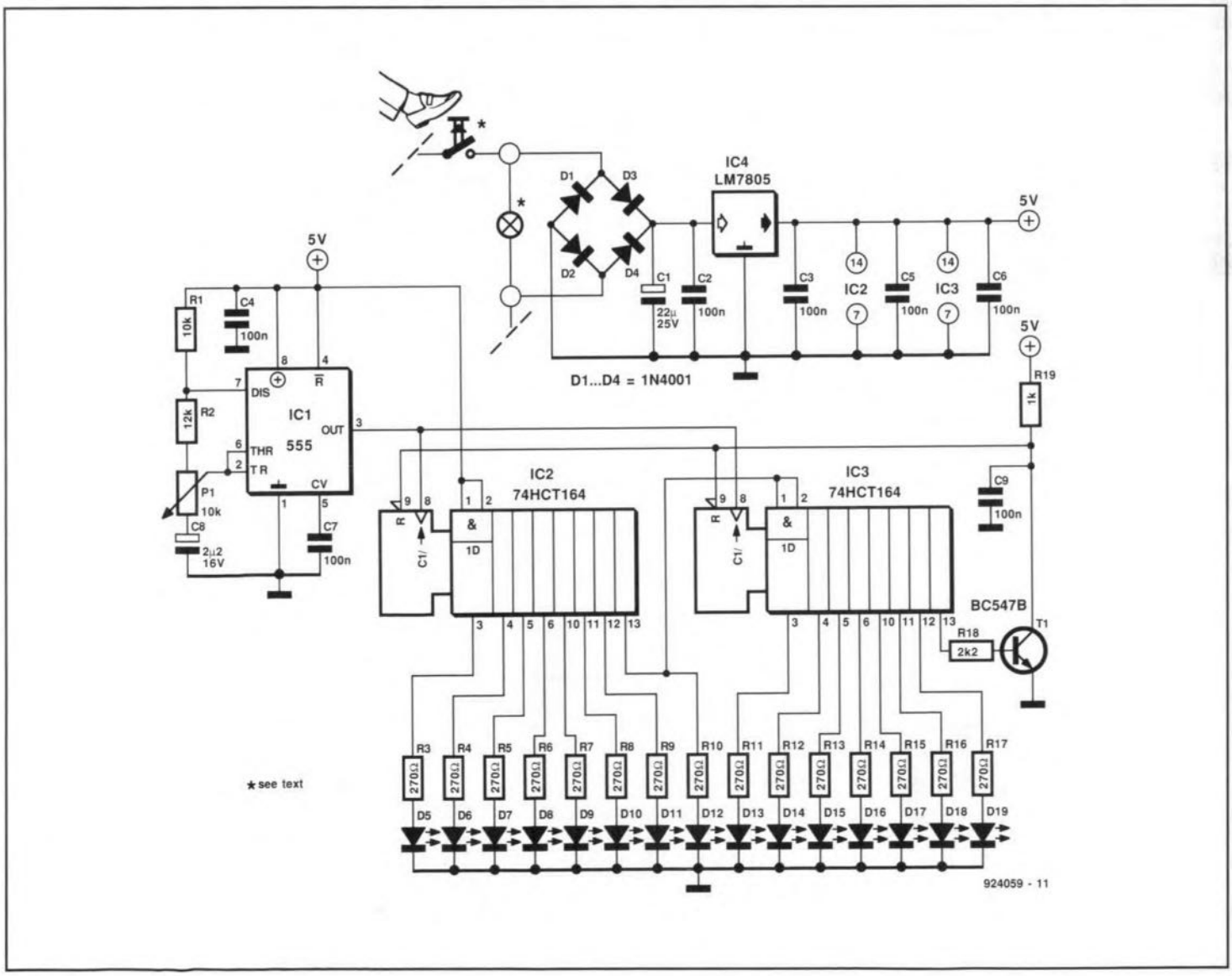
Power is taken from terminals of the present brake lights. Because of bridge rectifier D_1–D_4, the polarity of that voltage is immaterial. The voltage is kept steady at 5 V by IC4.

An oscillator, based on IC_1, provides clock pulses to shift registers IC_2 and IC_3 as long as the brake pedal is pressed. The p.p.r. (pulse repetition rate) is set with P_1.

LEDs are connected to the outputs of the shift registers via series resistors. Because input pins 1 and 2 of IC_2 are connected to the positive supply line, each clock pulse generates a logic high at successive output pins, so that more and more LEDs will light. Since the last output of IC_2 is linked to input pins 1 and 2 of IC_3, the outputs of that register will also be supplied successively with logic 1s when all LEDs connected to IC_2 light. When, finally, the last output of IC_3 goes high, T_1 is switched on, which results in a reset of the shift registers and all LEDs going out. If the brake pedal is still pressed, the LEDs will light one by one again.

Network R_{19}-C_9 ensures that the shift registers are reset and thus the LEDs go out the instant T_1 is switched on.

(Soumya Mitra – 924059)



DIGITAL VOLUME CONTROL

TWO ladder networks and a buffer each form a volume control with a range of 63 dB. Network R_3–R_{17} provides fine control in steps of 1 dB, whereas network R_{20}–R_{34} provides coarse control in steps of 8 dB. The desired attenuation is set with the aid of multiplexers IC_1 and IC_3, each of which is controlled via three digital inputs. The design is such that the binary code on the six-bit wide overall control input accords with the set attenuation.

Resistor R_1 ensures that C_1 can discharge, even if K_1 is open-circuited. This resistor and network R_3–R_{17} form an input impedance of 46.3 kΩ. The resistor also determines the maximum permissible input voltage. That voltage depends, in the first instance, on the supply voltage to IC_1 and IC_3 (±8.2 V). Resistor R_1 plus R_3–R_{17} attenuate the input signal×2.4 (7.6 dB). This means that the maximum input level must not exceed 20 V_{peak}, that is, 14 V r.m.s. That means also that IC_{2a} must not amplify to prevent too high an input to the second ladder network and buffer.

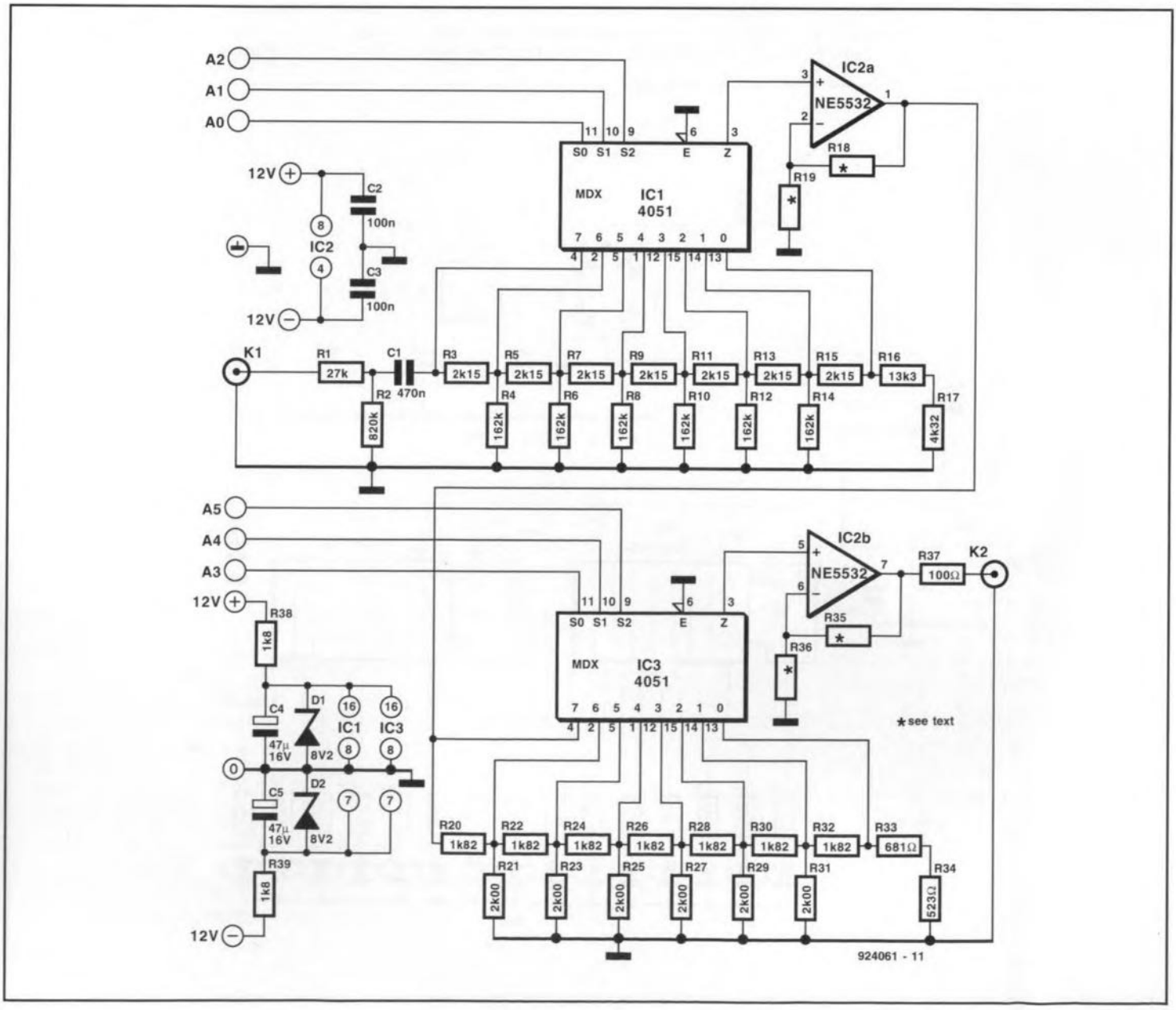
The amplification of the two opamps is determined by R_{18}-R_{19} and R_{35}-R_{36} respectively. As stated before, that of IC_{1a} should be unity, in which case R_{18}=0 Ω and R_{19} is omitted. If the amplification of IC_{2b} is also unity, the overall control range is –7.6 dB to –70.6 dB. To obtain a control range of 0–63 dB (when the binary code on the control inputs accords with the actual attenuation), IC_{2b} should provide an amplification of ×2.4.

The current drawn by the circuit is determined primarily by the dual opamp and amounts to about 10 mA.

The overall distortion is <0.003% over the range 20 Hz to 20 kHz and an input signal of 1 V.

The control has one, small, drawback: when the volume is set, weak clicks occur (which are typical of all normal CMOS switches). That makes it less suitable for super-de-luxe applications, although many listeners will not even notice the clicks. And, in any case, the volume is not varied constantly.

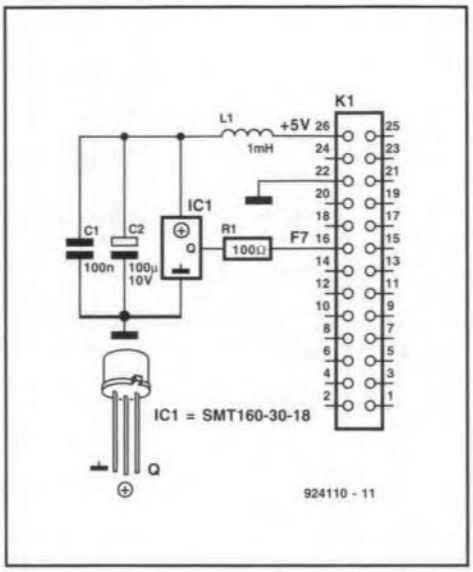
(P.C. Hogenkamp – 924061)



AUDIBLE FLUID LEVEL INDICATOR

A 600 Hz signal at a level of 2.4 V_{pp}, generated by the oscillator on board an LM1830 (National Semiconductor) is applied to a probe via C_2. The probe is immersed in the liquid whose level is to be monitored. Because of C_2, there is no direct voltage at the probe, so that there are no electrolysis problems.

As long as the probe makes no contact with the (conductive) liquid, the signal level at the input of the detector is equal to the level of the oscillator signal. When the liquid touches the probe, the detector input is connected to ground (or nearly so). This causes the level at pin 10 to drop. When it becomes more than 0.6 V lower than the oscillator signal, the detector switches on the internal output transistor in the rhythm of the oscillator frequency, since that is not suppressed by the detector.



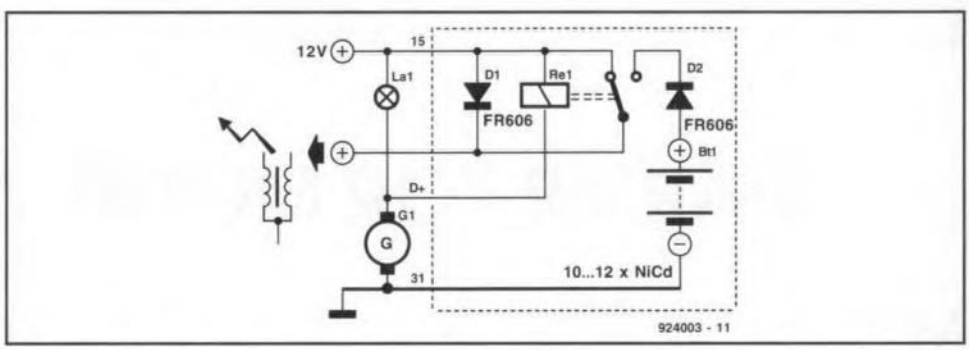
The consequent signal at pin 12 is used to drive a simple output stage, T_1, which drives a small loudspeaker, LS_1.

The supply for the circuit is best taken from a 9-V PP3 battery. In quiescent operation, the current drain is 3 mA; when the alarm sounds, the current rises to about 80 mA.

[L. Lemmens – 914110]

SUPER STARTER FOR CARS

THE super starter makes it possible to start cars with ageing batteries and obsolescent (coil-based) ignition systems, particularly during cold or damp weather. During starting, the voltage of an ageing (and possibly cold) battery will be insufficient for the coil to generate a tension high enough to create a strong spark across the spark plugs. The circuit presented ensures that the coil is powered by a battery of NiCd cells; even in these arduous conditions, such cells will last up to ten minutes. After the engine has started and the dynamo voltage has risen, the coil is powered by the car battery again.



The circuit uses the D+ terminal of the charging current indicator lamp (La_1) to check whether the engine is running, since that terminal is connected directly to the dynamo. As log as the engine does not run, and the dynamo, therefore, does not generate a voltage, relay Re_1 is energized via the ignition key (+ connection) and the low-resistance dynamo (connection to earth). The NiCd battery then provides plenty of power to the coil, irrespective of the state of the car battery. Once the engine has started, a voltage will be generated by the dynamo. There is then no potential difference across the relay coil and its contact changes over, whereupon the coil is supplied by the car battery (or the dynamo).

Diode D_1 prevents two possible troubles. First, it prevents the relay interrupting the current to the coil when its contact changes over, which would result in a spark at a moment that the engine does not need one. Therefore, the coil is powered via the diode during the change-over period. This reduces the voltage across the coil by about 2 V, but that does not matter. Secondly, it ensures that the car can be started when the car battery is fully charged and the NiCd cells are flat, or have been removed for charging.

The relay must have a contact rated at not less than 8 A. Car relays with change-over contacts are not easily obtainable as a spare part, but can be often be found in car scrap yards (particularly in Citroen CX models).

The Type FR606 diode may be replaced by a Type BYW29-100; both can handle currents up to 6 A and their reverse voltage is high enough to withstand the inductive peaks generated by the coil.

The circuit is best built in behind the dashboard, although it is advisable to place the NiCd cells in a removable holder to enable them to be charged externally. It is, of course, possible to charge them from the car battery via a suitable resistor. The D+ connection at the charging indicator lamp is that which is at earth potential when the engine is not running, but the ignition is switched on. At the ignition switch is a cable that goes to the coil: that cable must be connected to the output, 15, of the circuit. The ⊕ terminal of the circuit must be connected to the freed contact at the ignition switch. The –ve line of the circuit must be connected to the car chassis.

(J.Vaessen – 924003)

Mains (power line) voltages are not listed in the articles. It is assumed that our readers know what voltage is standard in their part of the world.

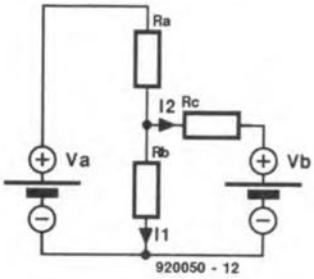
Readers in countries that use 60 Hz supplies, should note that our circuits are usually designed for 50 Hz. This will not normally cause problems, although if the mains frequency is used for synchronization, some modification may be required.

The international letter symbol '*U*' is used for voltage instead of the ambiguous '*V*'. The letter V is reserved for 'volts'.

CORRECTIONS

Plant warmer (June 1992)

Resistor R_c was omitted from Fig. 2. The correct diagram is shown below.



Inductance-capacitance meter (March 1992)

The value of R_{16} and R_{17} should be 39 Ω, not 30 Ω as shown in the parts list.

8751 Emulator (March 1992)

The features list in the first column on page 53 should read:

- download, modify, and upload 8751 programs without having to erase and program an 8751.
- put breakpoints in programs.
- display register and memory contents.
- ...

  etc.

FM tuner – Part 3 (May 1992)

In the PSU parts list on page 54, R_{301} should be 150 Ω, 1%, not 150 kΩ, 1%.

Video enhancer (July 1992)

Preset P_2 is best adjusted for a signal level of 2 V_{pp} at the collector of T_2. Output transistor T_3 may run fairly hot: this is normal.

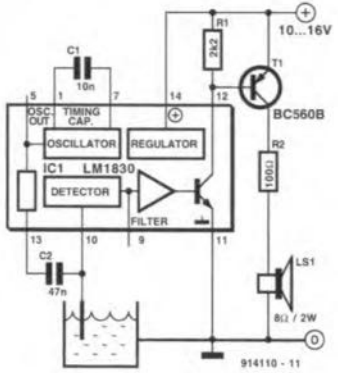
The third paragraph of the text on page 73 should read: The frequency characteristic of the signal at the base of T_3 is shaped by P_1, R_6 and C_8, and is, therefore, to a certain extent under the control of the user (with P_1).

Mark 2 QTC 80/40 loop antenna (July 1992)

The frequency '3800 kHz' mentioned twice under **2. 40-metre band** (page 90) should have read '7300 kHz'.

Audible fluid level indicator (July 1992)

Owing to a printing error, the diagram in this article is incorrect. The right diagram is shown below.



SIMPLE SIGNAL GENERATOR

THIS signal generator provides a 440 Hz sine wave output at two levels. The power supply may lie between 1.5 V and 16 V, so that even a single 1.5 V battery can do.

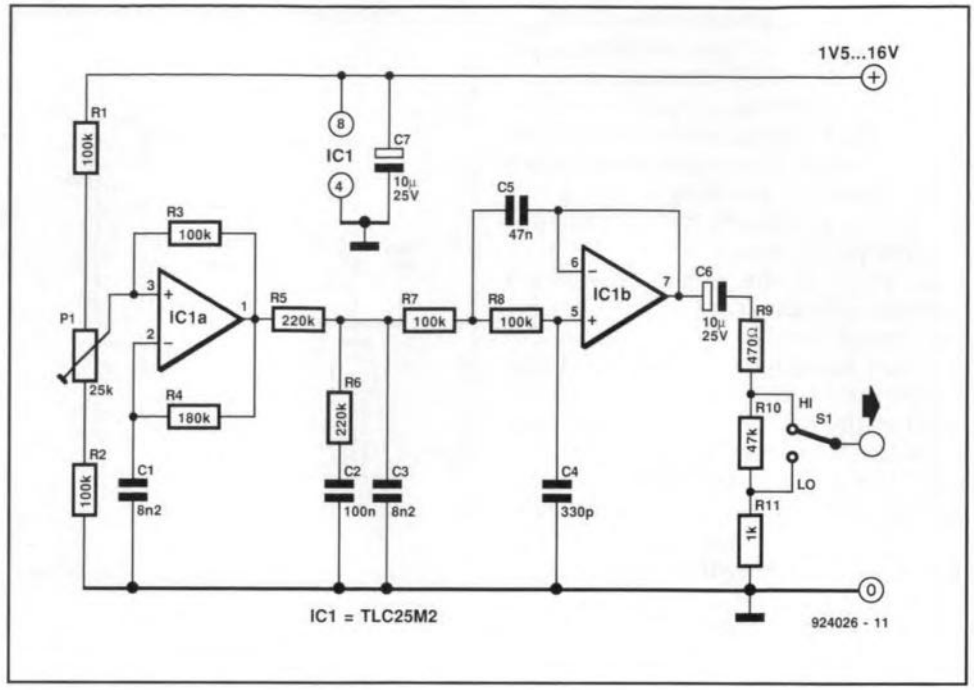
Opamp IC_{1a} operates as a rectangular-wave generator; the values of R_4 and C_1 determine the frequency at which the output of the device toggles. Preset P_1 enables the output to be set as a square wave (it may be adjusted by listening for minimum distortion).

Network R_5-R_6-C_2 reduces the output of IC_{1a} by 3 dB (50%), after which the signal is superimposed on half the supply voltage (derived from the average level of the rectangular signal by C_2). That voltage is needed for setting the d.c. operating point of IC_{1b}.

Opamp IC_{1b} forms a third-order Chebishev filter with a cut-off frequency of 400 Hz. This filter removes the majority of harmonics from the rectangular signal, so that the output is a reasonably clean sine wave.

The level of the output signal is selected with S_1 from potential divider R_9-R_{10}-R_{11}, depending on the requirements of the circuit on test. With a power supply of 16 V, the output level is 1.5 V r.m.s. or 30 mV r.m.s.; with a 1.5 V supply, the output levels are 150 mV and 3 mV. The output frequency is somewhat dependent on the supply voltage and varies from about 440 Hz at 1.5 V to around 370 Hz at 1.5 V.

The circuit draws a current of 300 µA at 16 V and 80 µA at 1.5 V.



(C. Sanjay – 924026)

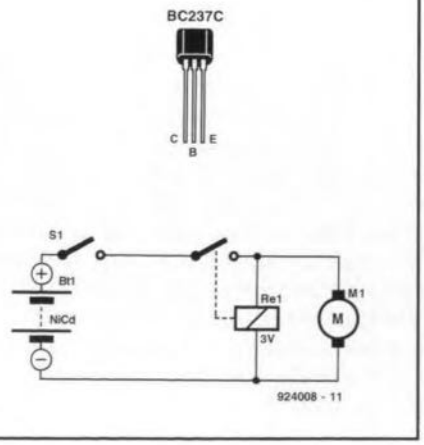
STARTER FOR MODEL AIRCRAFT

MODEL aircraft tend to be realistic reproductions of the real thing. That means, among others, that starting the petrol engine must be done by hand or with an external, electric starter. Manual starting may be realized in two ways: with the circuit in Fig. 1 or with that in Fig. 2.

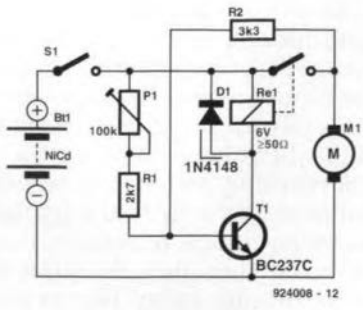
The circuit in Fig. 1 places a 3-V relay between the starter and the motor. When the starter switch is closed, nothing happens. But if then the propeller is turned by hand, the motor acts as a generator and, once it is turned fast enough, the generated voltage is high enough to energize the relay, whereupon the motor starts. An advantage of this is that it is a pure mechanical operation, which is readily incorporated. A disadvantage is that once the relay is energized, it is operated by a 6-V supply: a slight waste of energy.

The circuit in Fig. 2 is rather more economical, since it uses a 6-V relay. Again, the motor is used as a generator operated by turning the propeller. The generated voltage is applied to the base of T_1 via R_2. When the base is supplied with sufficient current, the transistor is switched on, the relay is energized and the motor starts. The starting point can be preset with P_1.

1



2



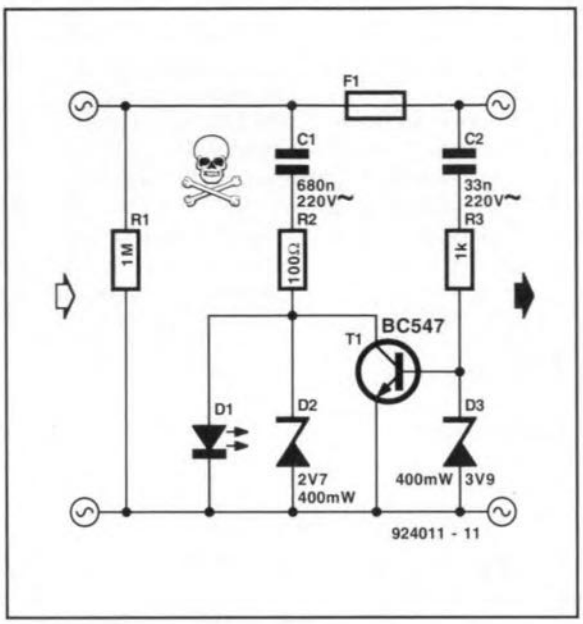
[G. Bartelt – 924008]

FUSE MONITOR

WHEN an appliance ceases to operate, there may be various causes for this, one of which is the blowing of the mains fuse. The monitor proposed here contains an LED that lights when that is the case. It is suitable for use with fuses rated from milliamperes to amperes.

As long as the fuse is intact, the full mains voltage exists across C_2-R_3-D_3. Capacitor $_2$ and resistor R_2 serve to limit the base current of T_1. Diode D_3 prevents C_2 from being charged, which would cause the base current to quickly drop to zero.

Capacitor C_1 and resistor R_2 limit the current through D_1, while D_2 ensures that the voltage across the LED does not exceed 2.7 V. At the same time, D_2 prevents C_1 from being charged.



As long as the mains voltage exists at junction F_1-C_2, transistor T_1 conducts and short-circuits D_1 and D_2. When F_1 blows, T_1 is switched off, whereupon current flows through D_1 and D_2: the LED then lights.

Resistor R_1 must conform to relevant safety regulations. Furthermore, capacitors that still carry the mains voltage after the appliance is switched off, must become discharged (via R_1) within a stipulated time.

When the monitor is in use, remember at all times that certain of its parts are at, potentially lethal, mains voltage.

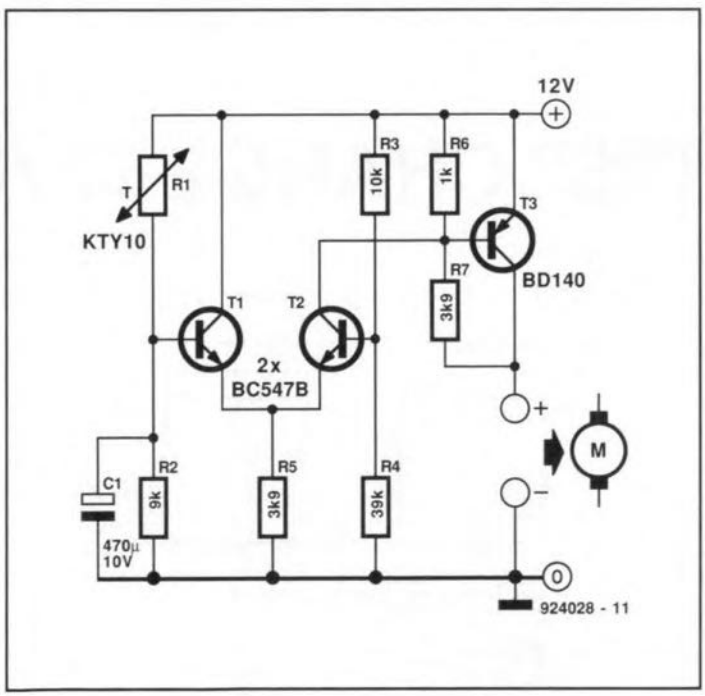
[I. Fietz – 924011]

PC COOLING FAN CONTROL

MOST PCs are provided with a cooling fan to ensure that the internal temperature does not rise unduly. Unfortunately, in many PCs the fan noise soon becomes an irritant. Since for a large part of the time the fan cools the PC more than is necessary, it seems sensible to make the speed of the fan dependent on the ambient temperature. That is the purpose of the circuit shown.

The circuit, designed with discrete component, is intended for the control of 12-V fans that do not draw a current exceeding 200 mA.

To ensure that the fan operates satisfactorily in all circumstances, the supply to it must not drop below its starting voltage. That voltage is equal to the 12-V supply less the 'zener' voltage of T_3-R_6-R_7. With values shown in the diagram, the supply to the fan will be at least 7 V. If the fan does not start at 25 °C, replace temperature sensor temporarily by a 1.8 kΩ resistor and lower the value of R_7. If the fan runs too fast, raise the value of R_7.



Transistors T_1 and T_2 compare the fixed potential at junction R_3-R_4 with the temperature-dependent one at junction R_1-R_2. It may be found convenient initially to place 25 kΩ potentiometer meter in the R_2 position, adjust this till the fan runs correctly, measure the resistance and then replace it by a fixed resistor of that value.

Place the temperature sensor in the warm air flow of the fan. When the computer is switched on, the speed of the fan, owing to C_1, will be fairly high, but will soon drop to a minimum. With a thermometer, measure the temperature of the outflowing air close to the sensor. When the temperature has reached a value of about 35 °C, the control circuit should come into action, indicated by an increase in the speed of the fan or its supply voltage. If that does not happen, change the value of R_2, or adjust the potentiometer in its place. When the temperature rises, the speed of the fan will increase. The maximum speed will be only slightly lower than that without the control circuit. This is thanks to the fact that T_3 can be driven into hard conduction, so that the drop across it is only some tenths of a volt.

[K Walraven – 924028]

TELEPHONE GONG

THOSE of you who like the telephone bell louder may find this circuit of interest. It uses the telephone bell signal to actuate an oscillator, which in turn drives a relay that operates a standard door-gong.

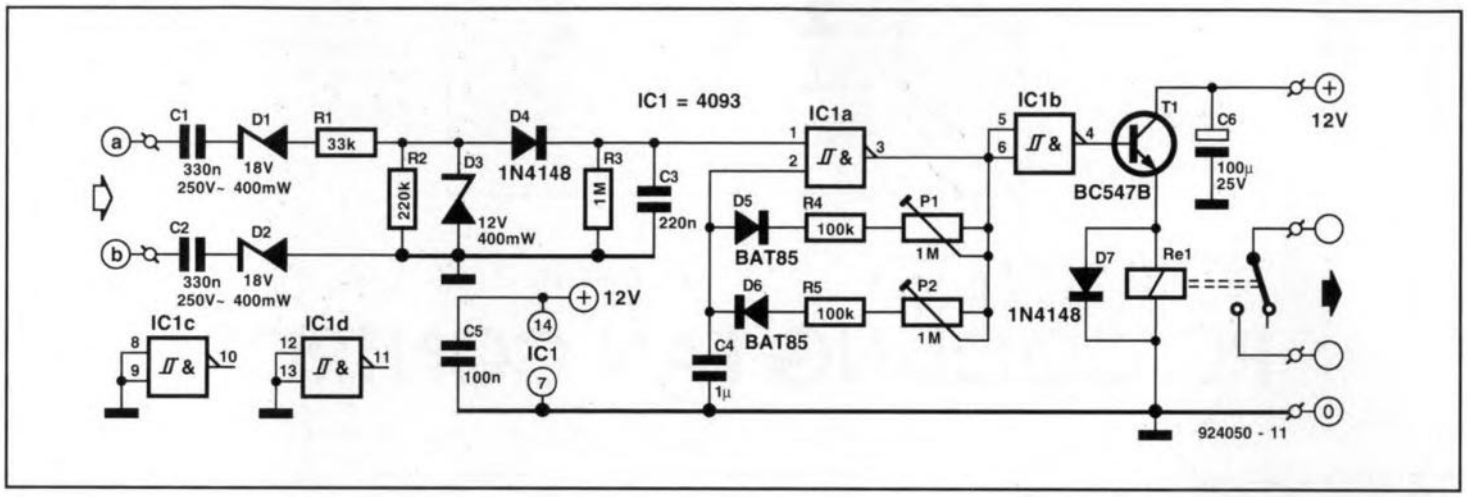
The oscillator is an *RC* type based on a 4093 Schmitt trigger. Both the charging and discharge times of C_4 are set with presets. The oscillator is followed by a kind of buffer that energizes the relay via T_1.

The telephone bell signal is applied to terminals *a* and *b*. Capacitors C_1 and C_2 in the two lines isolate the circuit from the telephone network, at least as far as d.c. is concerned. To prevent the circuit responding to speech signals, level thresholds are provided by zener diodes D_1 and D_2. Network R_1-D_3 limits the 120–150 V_{pp} bell signal to about 12 V. That signal is rectified by D_4 and smoothed by C_3, after which it is used to switch IC_{1a}. Capacitor C_3 is discharged rapidly via R_3 when the bell signal ceases. Resistor R_2 prevents too high a drive voltage when there is speech on the input lines.

The relay contact is connected across the terminals via which the gong is operated. The circuit may be fed by the same transformer used for the gong. When the relay is energized, the total current drawn is only 35 mA.

The setting of presets P_1 and P_2 depends on individual taste how long the on and off periods of the gong are desired to be.

(T. Giesberts – 924050)

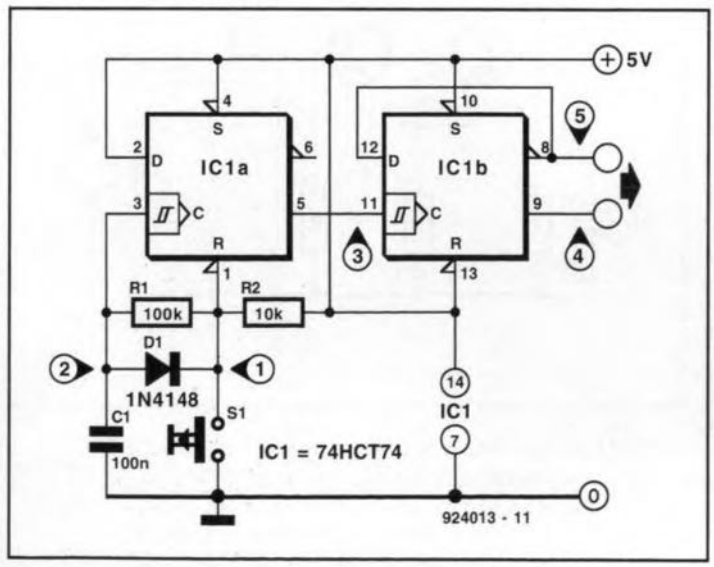


BOUNCE-FREE CHANGE-OVER SWITCH

ANY push-button switch can be used as a bounce-free, change-over switch with the aid of two D-type bistables contained in a 74HCT74 and some external components.

In the circuit diagram, IC_{1b} provides the change-over function. The $\overline{Q}$ output (pin 8) of this bistable is interconnected with its D input (pin 12), which results in the logic levels at the Q and $\overline{Q}$ outputs alternately changing state when a leading transition (edge) appears at its clock input (pin 11).

Circuit IC_{1a} serves as pulse generator and debouncing element. The push-button switch, S_1, is connected between its reset input (pin 1) and earth. Normally, because of R_2, there is a high level at pin 1. When the push-button is pressed, IC_{1a} is reset.



The clock input (pin 3) is also connected to the switch via R_1-C_1. When the switch is operated, C_1 discharges rapidly via D_1; when the switch is released, it takes a little while before C_1 is recharged to a logic high level.

When S_1 is open, pin 9 (IC_{1b}) is low, while pin 8 and pin 5 (IC_{1a}) are high. When the switch is closed, IC_{1a} is reset immediately, resulting in pin 5 and pin 3 going low. When S_1 is released, the reset is removed, but it takes a little while before C_1 is charged to a logic high level. Only when that level is reached, and a leading transition appears at pin 3, does pin 5 go high again. This results in IC_{1b} being clocked, whereupon its Q outputs change state.

(A. Rietjens – 924013)

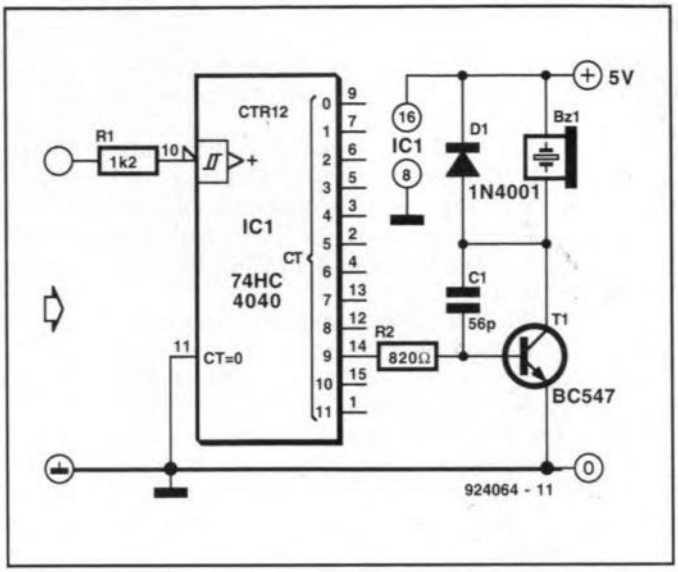
FREQUENCY PROBE

THE frequency probe enables you to 'listen in' to the speed of your computer. It is, however, also suitable for use with other digital circuits, because it makes high frequencies audible, so that signals can be conveniently monitored.

A 12-bit counter serves as 'frequency detector'. The signal measured in a computer or digital circuit is divided by 1024 and is output at pin 14. It is then used to control a transistor, T_1, which in turn drives piezo buzzer Bz_1.

The scale factor has been chosen to convert MHz into kHz, so that the clock frequency of, say, an XT computer will be heard as a shrill 8 kHz tone. If higher frequencies need to be monitored, scale factors of 2048 and 4096 can be obtained by connecting R_2 to pin 15 or pin 1 respectively. If an HCT circuit is used, the measuring limit is some tens of MHz. For frequencies <4 MHz, a standard Type 4040 may be used: that has the advantage that the supply voltage need not be exactly 5 V.

The supply connections and the probe are best made from flexible wire terminated into crocodile clips.



(Amrit BirTiwana – 924064)

SCANNER FOR PREAMPLIFIER

THE scanner is an extension for the 'All-solid-state preamplifier' published in the December 1989/January 1990 issues of this magazine. As its name implies, it scans all inputs of the preamplifier to ascertain where there is an audio signal present. That input remains selected. After there has been no signal for some time, scanning is resumed.

The scanning action is provided by rectangular-wave generator IC_{2c}. The output of this oscillator is applied to one of the input selector keys via buffer/inverter IC_{2d} and diode D_3. The diode prevents the key being disabled when the oscillator is off. The oscillator is switched on and off by IC_{2b}, which in turn is controlled by IC_{1b}. That opamp is configured as a comparator whose voltage threshold is preset with P_1.

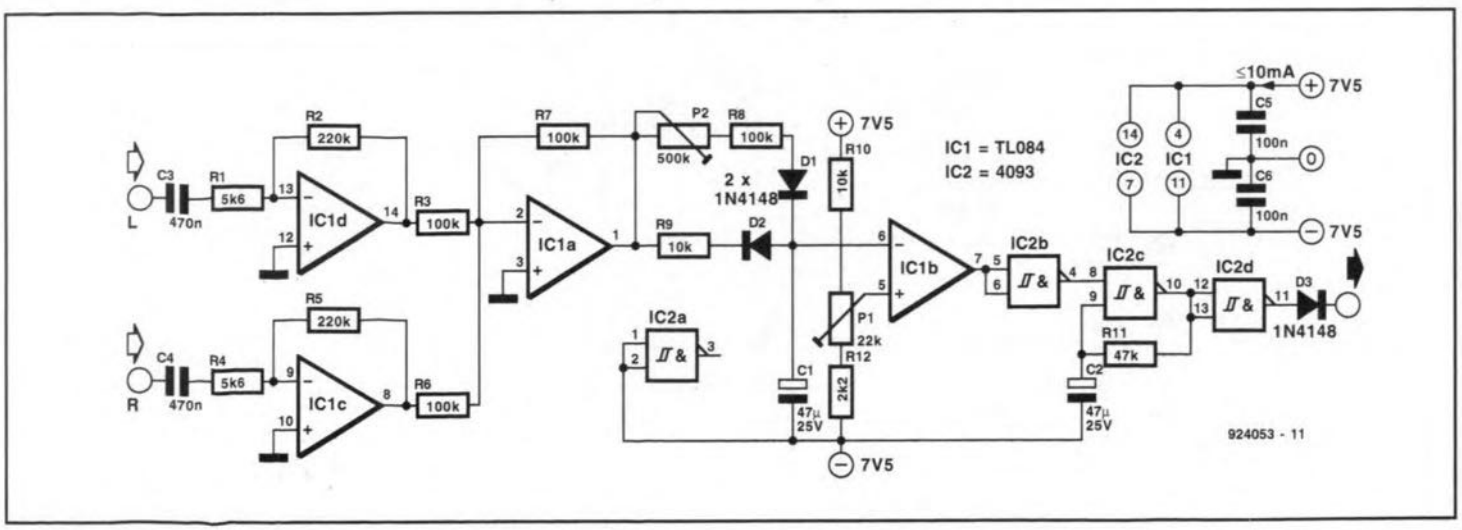
The inputs of the scanner are linked to the audio inputs on the volume control board of the preamplifier. The relevant signal is amplified ×40 by IC_{1c} and IC_{1d}, after which summing amplifier IC_{1a} combines the left-hand and right-hand signals. As soon as there is music or speech on the input lines, C_1 will partly discharge rapidly. When the voltage across the capacitor drops below the level set by P_1, IC_{1b} disables the oscillator via IC_{2b} and the input selected at that instant remains actuated. As long as there is a signal coming in, part of the charge on C_1 will ebb away via IC_{1a}. If there is no signal for some time (presettable with P_2 between 3 s and 25 s), the capacitor will be charged almost completely via P_{23}, R_8 and D_1. Once the terminal voltage of C_1 rises above the comparator threshold, the oscillator is enabled again and the scanning action resumes.

A total scan of all inputs is completed in 3 s (determined by R_{11}-C_2).

The input sensitivity can be set between 10 mV and 4 V with P_1.

The current drawn by the scanner is not greater than 10 mA.

(L. Soete – 924053)



STEREO PROTECTOR AGAINST D.C.

IF a d.c. coupled output amplifier breaks down during operation, the loudspeakers, particularly the bass units, are at risk. The bass particularly so because it is not decoupled for d.c. by the capacitors in the crossover network. If, for instance, the output transistor has given up the ghost, the bass units will get the full d.c. supply voltage at their terminals.

A suitable circuit to protect the loudspeakers in such an eventuality, and at the same time to obviate the annoying 'plops' on switch-on is shown in the diagram. Interestingly, it operates from an unregulated, nonsymmetrical power supply. Normally, it may be powered directly from the power supply of the output amplifier.

The a.c. component of the signals in the output stage is bypassed by R_1 and the two anti-series connected capacitors, C_2 and C_3. The signal at the junction R_1-R_2 is, therefore, the d.c. component of the loudspeaker signal. From there it is applied to potential divider R_2-R_3 and then to window comparator IC_{1a} and IC_{1b}. Since the supply voltage is fixed at 10 V by R_{13}-D_7, the window height is fixed at 2 V by R_5. In other words, $u_2 = 6$ V and $u_3 = 4$ V. In the absence of d.c. at the output of the power amplifier, $u_1 = 5$ V. In this situation, the outputs of 'OR gates' D_1 and D_2 is logic high.

When the d.c. component at the output of the power amplifier is greater than ±2 V, u_1 is greater or smaller than either u_2 or u_3. The output of one of the opamps will then be logic low.

When the power amplifier is switched on in step with the present circuit and u_1 lies within the window, C_4 is charged via R_8. After about 1.5 s, 'Schmitt trigger' IC_{1d} changes state and its output becomes logic high. The relay is then energized and connects the loudspeaker to the power amplifier: no 'plop'.

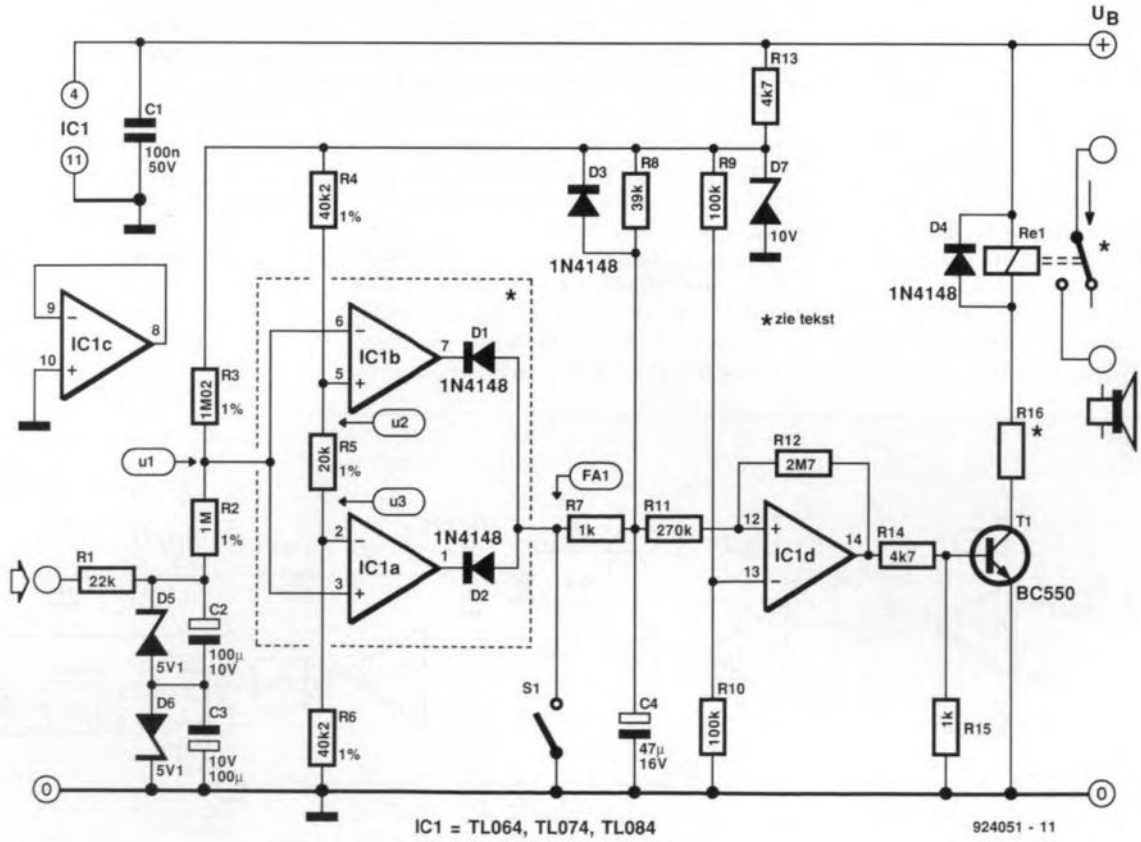
If a defect occurs, or if the direct voltage at the output of the power amplifier rises, C_4 is discharged via R_7 within 50 ms. The output of IC_{1d} then goes low, the relay is deenergized and the loudspeaker is disconnected from the output amplifier.

Resistor R_{13} and the operating voltage of the relay must be suitable for the supply voltage. If that voltage is 20–40 V, a good value and rating for R_{13} is 4.7 kΩ, 1 W; while for 12–20 V, 1 kΩ, $^1/_4$ W is right. If the supply voltage is, say, 36 V, the operating voltage of the relay should be 24 V. The difference of 12 V should be dropped across a suitable resistor. If, for instance, the relay draws 15 mA, R_{16} should have a value and rating of 820 Ω, $^1/_4$ W.

If there is likely to be a requirement for switching off the circuit, S_1 should be incorporated. When that switch is closed, the relay is energized.

For a circuit suitable for a stereo power amplifier, only components R_1–R_3, C_2, C_3, D_1, D_2, D_5, D_6, IC_{1a} and IC_{1b} need to be duplicated. The additional circuit is connected in parallel with S_1. Note that the relay should then have two working contacts or two relays with their contacts in series should be used.

[T. Schaerer – 924051]



SIMPLE POWER SUPPLY CONCEPT

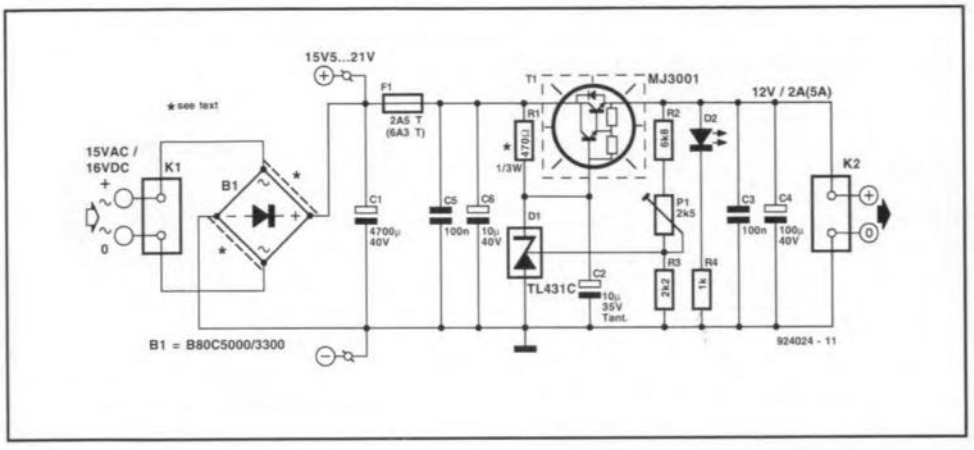
THE best known alternatives to a 'quick and dirty' power supply are the three-pin fixed voltage regulator and the zener-plus-transistor combination. While these basic circuits will suit a good many applications, they do have their limitations, which can be frustrating at times. For example, most types of fixed voltage regulators are limited to an output current of about 1 A only. Where more power is required, a 'current bypass' transistor is often added. However, while this boosts the maximum output current, the regulation of the supply suffers. Fixed voltage regulators with higher output currents (say, 5 A) are no alternative because they are notoriously expensive.

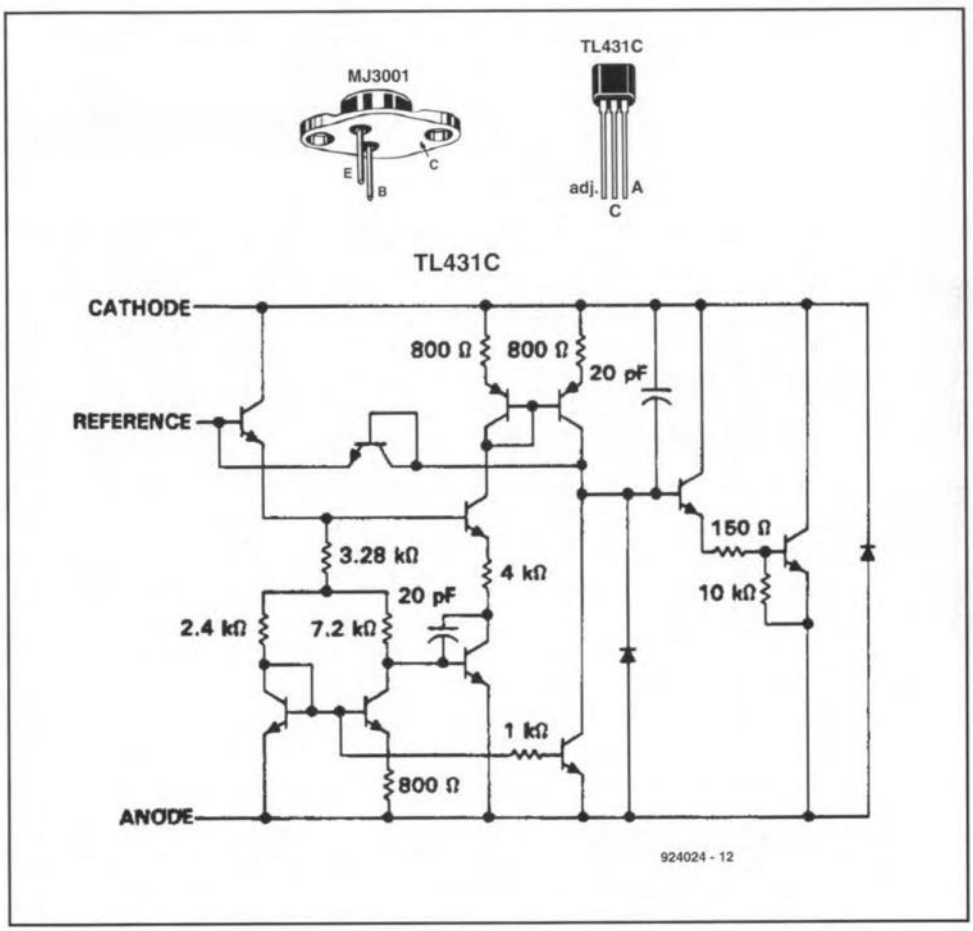
The second alternative, the zener-plus-transistor circuit, has limited use also because of its relatively poor ripple rejection and insufficient stability at output load variations.

The PSU presented here suffers none of the disadvantages mentioned above, and is simple to memorize as a multi-purpose concept. It is the perfect low-cost supply for a host of applications. At first glance, the circuit looks very much like the familiar zener-transistor combination. However, an essential difference is that feedback is implemented, which results in a 100-Hz ripple suppression of up to 55 dB—far more than can be achieved with the simple zener-transistor stabilizer.

The voltage reference used here is D_1, a TL431C from Texas Instruments. The internal structure of the TL431C is shown in the diagram. Here, D_1 supplies a base current to T_1 that results in 2.5 V across resistor R_3. This allows you to calculate the supply output voltage, U_o, from

$$U_o = 2.5\ [1+(P_1+R_2)/R_3] \text{ volts.}$$





The indicated component values result in an output voltage of 12 V. For other output voltages, simply adapt the output voltage divider, making sure that the current through P_1, R_2 and R_3 is at least 1 mA. This is required to ensure that the current flowing into the reference input of the TL431 is negligible (approx. 2 µA). The power transistor is a darlington with a guaranteed current gain of 1 000 or greater at an emitter current of 5 A. This means that only 5 mA of base current is required. Although this is not much, it has to be taken into account when R_1 needs to be given a different value. Also, D_1 requires a minimum cathode-anode current of 0.5 mA, which results in a total, minimum, current of 5.5 mA through R_1. This design infomation, together with the lowest possible input voltage, U_{in} (measured across C_6), and the base-emitter drop of T_1 (approx. 2 V), results in a theoretical value of the current limiting resistor:

$$R_1 = (U_{in}-U_{be}-U_o)/I_{R1} \quad [\Omega].$$

Because the current gain of the darlington may be up to two or three times the guaranteed value mentioned above, it is often possible to give R_1 a higher value than calculated. Since a higher resistor value results in lower dissipation of R_1 and D_1, some experimenting is certainly worth while.

The PCB designed for the supply accommodates the complete rectifier section, that is, a bridge rectifier, a buffer capacitor and a fuse. The buffer capacitor, C_1, and the on-board heat sink for T1 are large enough for output currents up to 2 A.

As already mentioned, this PSU is a concept. Those of you who do not need the rectifier section may omit it, and connect a d.c. voltage of 16 V to K_1. Note, however, that this requires wire links to be fitted in the positions indicated with dashed lines near the bridge rectifier.

If you require more output cur-

rent (say, up to 5 A), simply move the power transistor off the board, and fit it on a larger heat sink (see parts list). Also, increase the buffer capacitor to 10000 µF. Since such a capacitor (or array of capacitors) will not fit on the board, it is connected as an external part via heavy-duty wires and two spade terminals (marked '+' and '–' on the component overlay). A continuous output current of 5 A also requires the bridge rectifier to be cooled a little. This is best achieved by leaving it on the PCB, and clamping it on to a side panel of the metal enclosure used to house the supply.

(J. Ruiters – 924024)

PARTS LIST

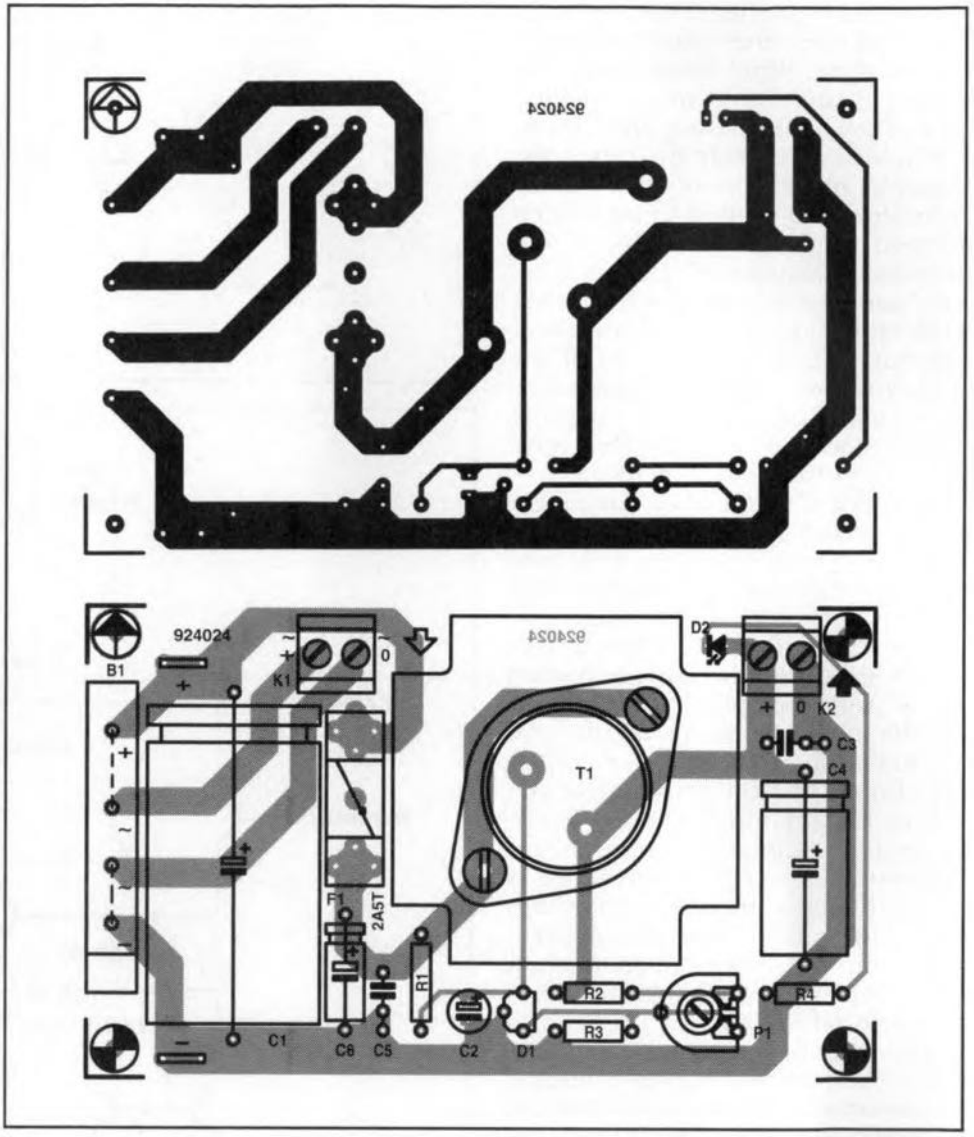
Resistors:
R1 = 470Ω 0.33W (see text)
R2 = 6kΩ8
R3 = 2kΩ2
R4 = 1kΩ
P1 = 2kΩ5 preset H

Capacitors:
C1 = 4700µF 40V
C2 = 10µF 35V tantalum
C3;C5 = 100nF
C4 = 100µF 40V
C6 = 10µF 40V

Semiconductors:
D1 = TL431C
D2 = LED, green, 3mm
T1 = MJ3001
B1 = B80C5000/3300

Miscellaneous:
K1;K2 = 2-way PCB terminal block, pitch 5mm.
F1 = 2.5A fast fuse (6.3A)* and PCB mount holder.
Heat sink: SK201 (6K/W) or SK71/75mm* (1.25K/W).
Two 'fast-on' spade terminals for PCB mounting *.
Printed circuit board 924024.

* for 5 A version only.



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Two 'fast-on' spade terminals for PCB mounting *.
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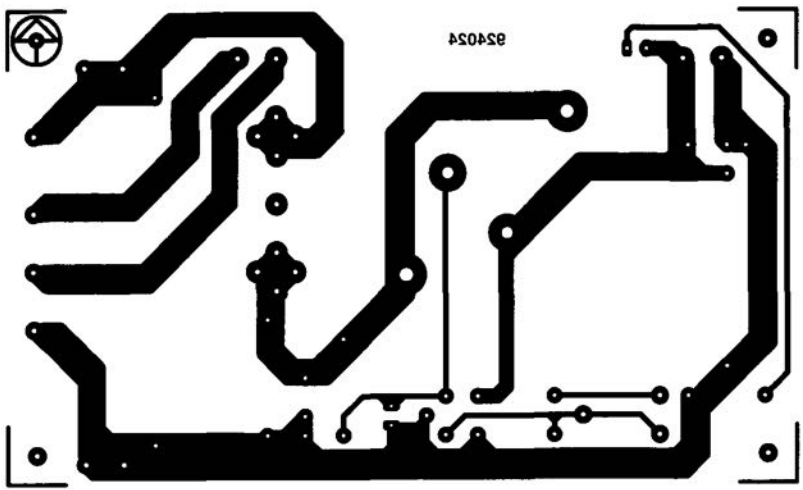
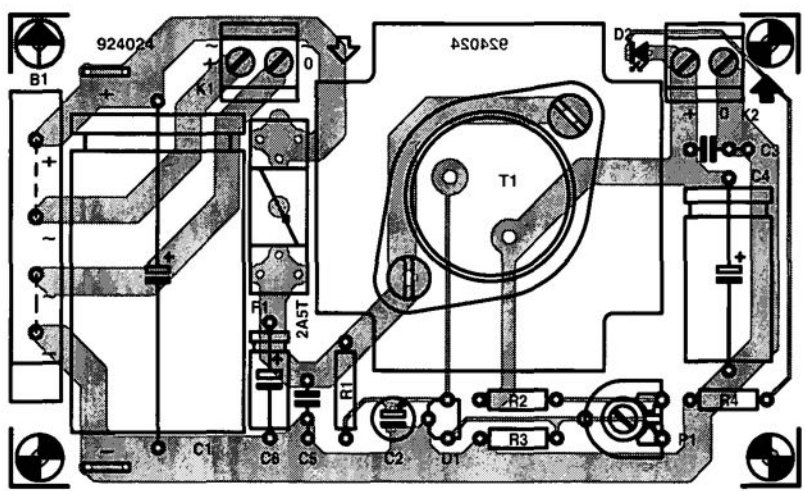




EXPERIMENTAL FAST NICD CHARGER

THE perpetual difficulty in designing fast NiCd chargers is determining when the battery is charged, that is, when to stop charging.

The charger presented here is based on the latest developments as reported by several manufacturers. It is not at all certain whether, and under what conditions, the circuit will consistently give satisfactory results.

The battery is charged with a current (in mA) that is ten times its nominal capacity (in mAh). That means that, for instance, an HP7 (AA; RG) type battery is charged at 5 A, a current 100 times larger than used in standard charging.

The charging is controlled by Type 555 timer IC, here connected as an astable. If the IC's output is high, charging takes place. There is, however, a fixed period of time ($=R_6C_3$) during which there is no charging. As soon as charging stops, C_1 is connected across the battery by electronic switch IC_{3a}. Its terminal voltage is then compared by IC_{1a} with the maximum battery voltage set by P_1. The output of the comparator is integrated by R_3 and C_2 and then used to determine the period of the astable. If the maximum battery voltage has not been reached, charging takes place for about 90% of that time. If the maximum battery voltage has been reached, charging takes place for 1% of the time (trickle charging). Do not leave the battery connected to the charger unnecessarily: when the LED lights, the battery is fully charged.

During charging, owing to a variety of resistances, primarily in the supply leads and connections, the battery e.m.f. is an unreliable yardstick for determining the state of charge of the battery.

Therefore, the e.m.f. is taken immediately after a burst charge, because then the voltage can be measured exactly. The important question is, of course, to what e.m.f. P_1

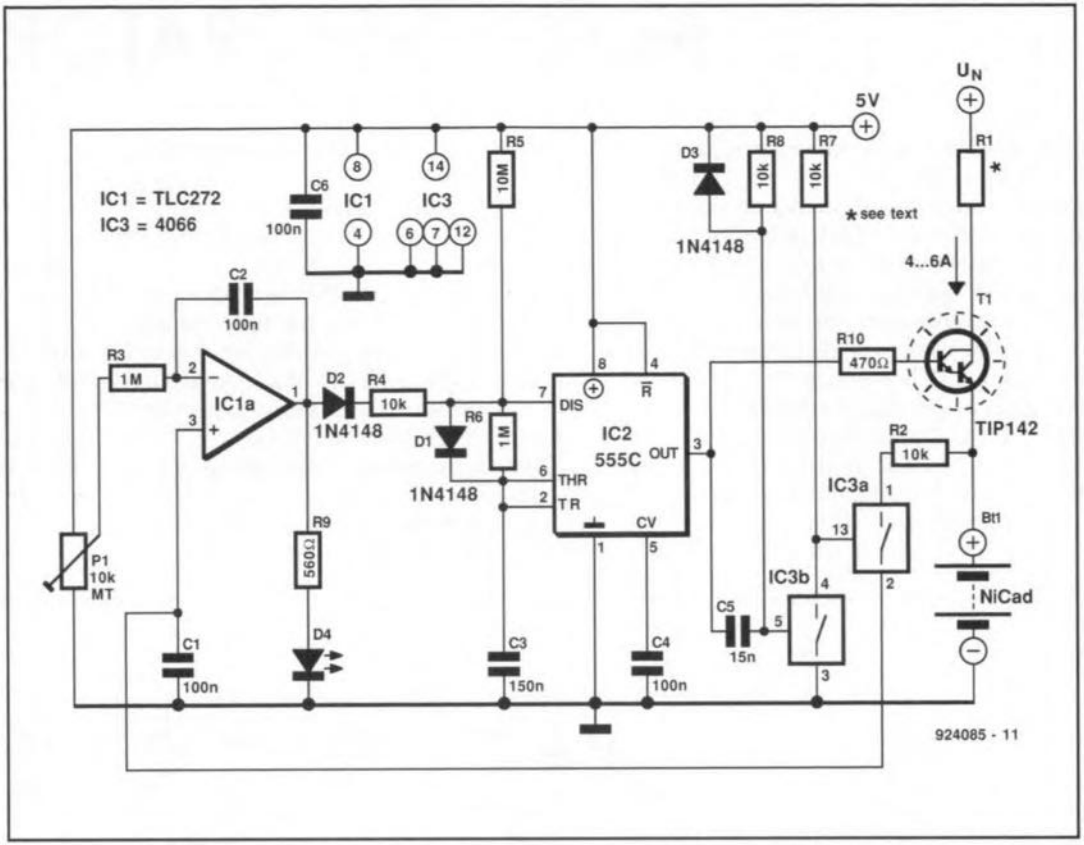
should be set; in other words, what is the correct battery e.m.f.? Opinions vary, but with our prototype we had good results with a value of 1.42 V at room temperature(21 °C).

The circuit draws a current of only 10–15 mA, which may be obtained with a 7805 regulator.

The proposed charger is intended for charging one 1.5 V NiCd battery in 8–10 minutes. The charging current for a 500 mAh battery is about 5 A, which need not be regulated, since it will be limited by R_1.

The value of R_1 is given by Ohm's law. If, for instance, the charging current is drawn from an 8-V source, and assuming that the drop across the battery and T_1 is 2 V, the voltage across the resistor is 6 V. Its value should thus be 6/5=1.2 Ω. Bear in mind that the power dissipated in it is 6×5=30 W: you will, therefore, have to connect a number of resistors in parallel.

If you want to charge a number of batteries in series, raise the level set by P_1 accordingly (at 1.42 V per battery). Note, however, that you should use only batteries that have already been sorted for equal capacity by the manufacturer. Also, the supply voltage to the charger circuit must always be 2 V higher than the level set with P_1.



Finally, after every five fast charges, give the battery a 'normal' ($^1/_{10}$ mAh over 14 hours) charge.

(K. Walraven - 924085)

CONTINUITY TESTER

A continuity tester is very useful for checking printed-circuit boards. It indicates a sound connection by a squeak from a buzzer; there is, therefore, no need to continually watch a meter.

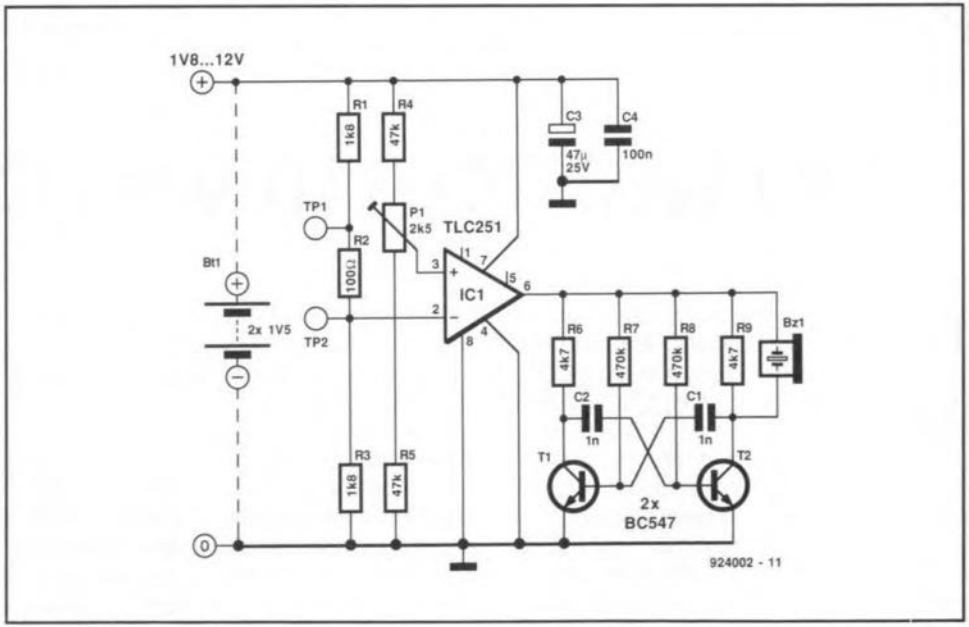
The voltage across test terminals TP_1 and TP_2 is only 80 mV. That is not sufficient to test diodes, but it obviates the risk of damage to electronic components.

The design consists of a comparator, IC_1, and an astable consisting of T_1 and T_2, whose frequency is around 1250 Hz for a supply voltage of 3 V. The astable is actuated the moment the output of IC_1 (pin 6) goes logic high. This happens when the resistance between TP_1 and TP_2 is low, so that the voltage at pin 2 of the comparator is lower than that at pin 3, which depends on the setting of P_1.

The circuit is powered by a 3-V battery (two 1.5 V cells in series), but may be maximum 12 V. At such a high supply voltage, it may be that the tone of the buzzer is too high; in that case, the values of C_1 and C_2 should be increased.

If a Type TLC271C is used instead of a TLC251 for IC_1, the supply voltage must be not lower than 3 V. At 3 V, the circuit draws a current of about 1.4 mA.

(C. Sanjay – 924002)



NOISE GENERATOR

NOISE generators are used for measuring the self-noise of amplifiers and receivers and for some acoustic measurements. The noise of traditional low-frequency noise generators is based on the stochastic properties of an ion current resulting from a gas discharge. A simple noise generator can, however, be designed without a special gas discharge tube: the reverse-biased base-emitter junction of a bipolar transistors a compact and inexpensive alternative.

In the circuit diagram, the noise voltage is taken from the emitter of T_1. The base-emitter junction of this p-n-p transistor begins to behave like a break-down diode at a reverse bias of about 9 V, but it really starts to generate noise at 10 V.

To ensure that the circuit works satisfactorily with a battery supply of 9 V, a step-up generator, based on IC_1, is used. This stage provides a rectangular output voltage at a frequency of around 2750 Hz.

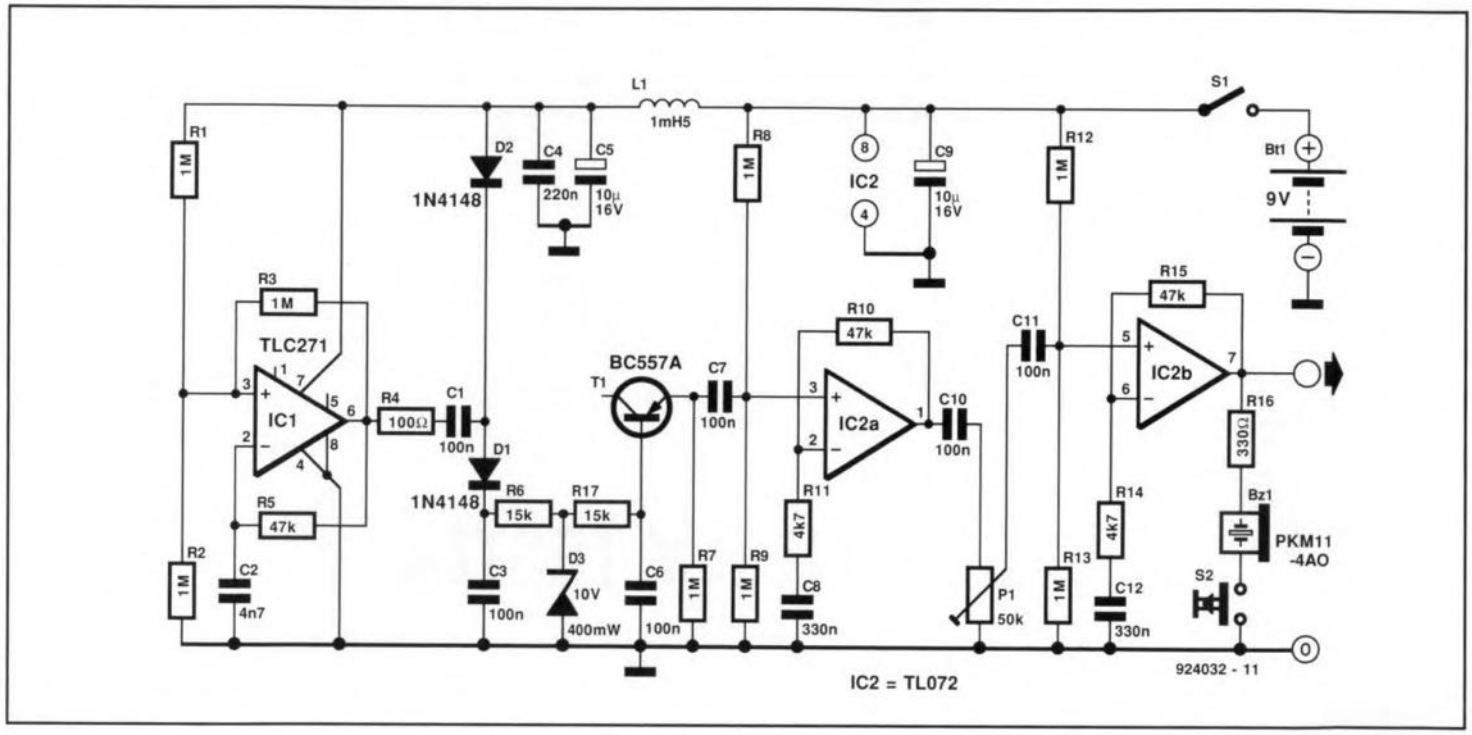
The diode pump, consisting of C_1, C_3, D_1, and D_2, doubles the battery voltage, which results in a stable direct voltage of 10 V across D_3.

Low-pass filter R_{17}–C_6 prevents frequency components of the rectangular-waveform generator appearing in the noise spectrum.

Each of the opamps in IC_2 raises the noise voltage in the frequency range from 01 Hz to 300 kHz tenfold. The amplitude of the output voltage can be preset with P_1. The noise signal can be tested with the a.c. buzzer by closing S_2.

With a fresh 9-V battery, the circuit draws a current of 5–6 mA.

[J. Ruiters – 924032]



240 VAC-TO-110 VAC CONVERTER

FROM time to time one comes across appliances in second-hand goods stores that were designed for operation from a 110 V a.c. (50/60 Hz) supply. If such an appliance is a pure resistive load, such as a radiant fire, a soldering iron, or a melting furnace, the circuit shown may be found useful. Strictly speaking, it is a dimmer set so that the output voltage has an r.m.s. value of 110 V. It is, of course, possible to set it to a different output voltage if so desired.

To obtain an r.m.s. voltage of 110 V across the load, the phase angle at which the triac is switched on must be about 110°. There is no guarantee that this will be met exactly by the present design: owing to tolerances of the various parts, the phase angle may be quite different so that the r.m.s. voltage will be higher or lower than 110 V. It is, therefore, essential, to check the actual voltage across the load. *Bear in mind that the circuit carries mains voltage and is thus potentially lethal.* Checking the phase angle with an oscilloscope cannot be carried out safely without special precautions. The safest and most accurate way of measuring the voltage across the load is with the use of a true-r.m.s. voltmeter (which shows the r.m.s. value also of non-sinusoidal voltages). If the voltage across the load is not correct, the value of R_2 must be altered.

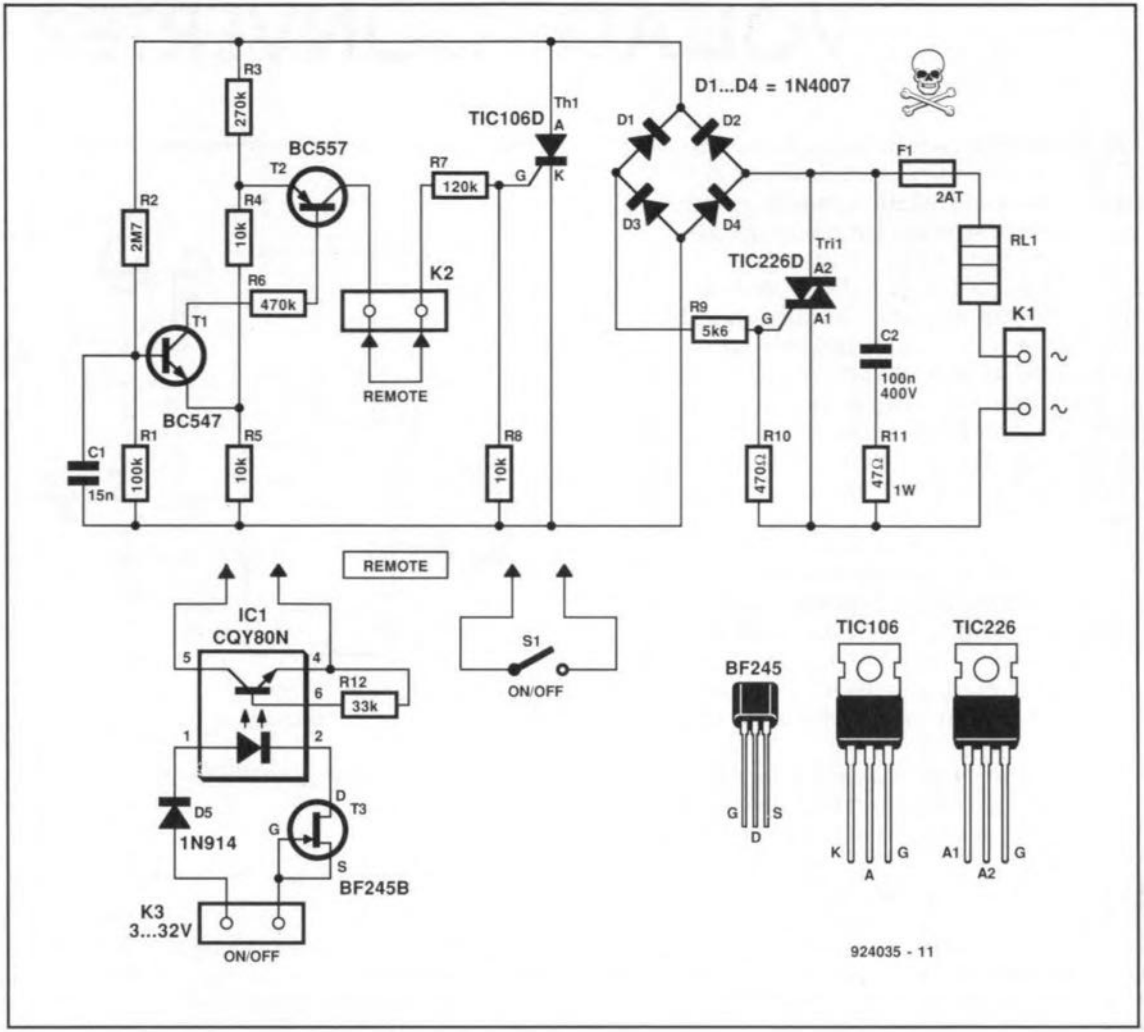
If you have no true-r.m.s. meter to hand, checking may be done in a slightly more primitive way. Use an incandescent 5 W, 240 V bulb as the load and place a thermometer close to it. Switch on the converter, wait till the thermometer gives a stable reading and note that reading (if the thermometer goes off its scale, place it a little further away from the bulb). Do not change the distance between the bulb and the thermometer, and connect a second 5 W, 240 V bulb in series with the first. Once the first bulb has cooled down sufficiently, connect the two in series across the 240 V mains supply (when the bulbs

will each drop 110 V). If the thermometer after a while has the same reading as before, you can be pretty certain that the converter provides an r.m.s. voltage of 110 V.

The converter may be remotely switched on and off via a direct connection between a suitable 240 V switch to the REMOTE terminals. The wire link should then, of course, be removed. It may also be switched on and off by a voltage of 3–32 V as shown. This optoisolator circuit has the great advantage of isolating the circuit from the mains.

If a triac Type TIC226 is used, the converter can handle currents of up to 2 A. If the triac is mounted on a heat sink, the current may go up to 4 A.

[J. Vanden Berghe – 924035]



VIDEO ENHANCER

THE enhancer amplifies the high frequencies of a video signal, resulting in a sharper picture. It may be inserted between, say, the video recorder output and the SCART input of a television receiver.

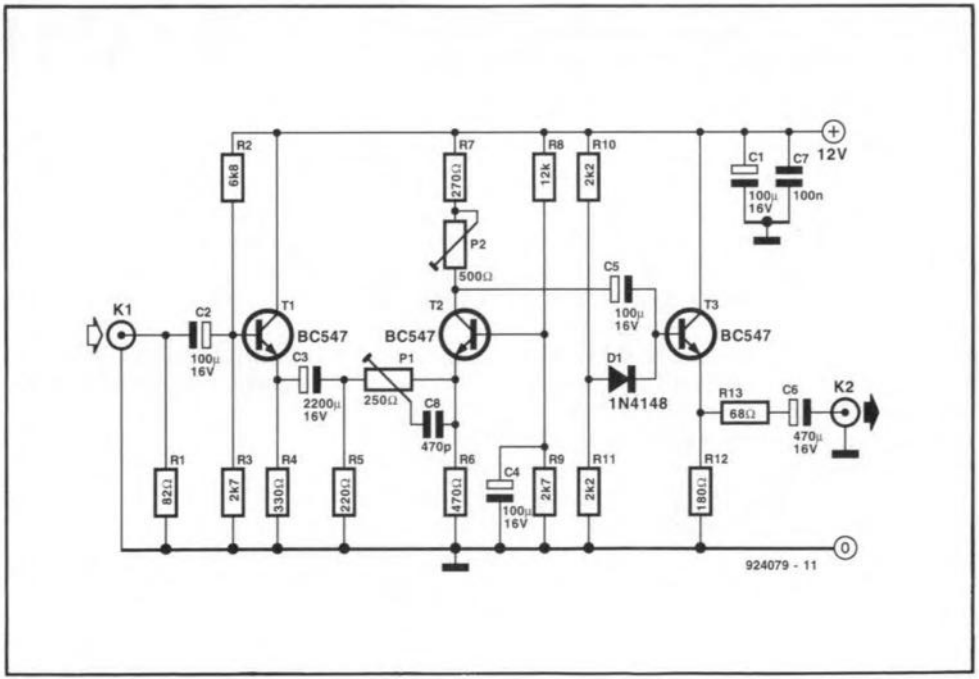
The simple design is based on only three transistors. The first, T_1, is a buffer. Resistor R_1 ensures that the input impedance is of the order of 75 Ω. The signal is then applied to amplifier T_2, whose gain is determined by the setting of P_2.

The frequency characteristic of the signal at the base of T_2 is shaped by P_1, R_6, and C_8, and is, therefore, to a certain extent under the control of the user (by P_1).

Buffer T_3 provides sufficient current for correctly driving most 75 Ω loads.

Preset P_2 must be set to give an output voltage of 1 V_{pp} (terminated output; for an open-circuit output, the level should be 2 V_{pp}).

The enhancer draws a current of about 50 mA. Note that the 12 V supply should be regulated.



(J. Bodewes – 924079)

Mains (power line) voltages are not listed in the articles. It is assumed that our readers know what voltage is standard in their part of the world.

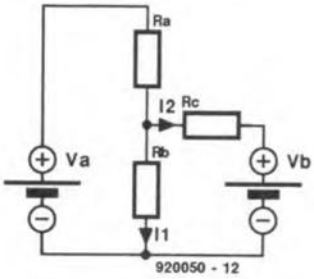
Readers in countries that use 60 Hz supplies, should note that our circuits are usually designed for 50 Hz. This will not normally cause problems, although if the mains frequency is used for synchronization, some modification may be required.

The international letter symbol '*U*' is used for voltage instead of the ambiguous '*V*'. The letter V is reserved for 'volts'.

CORRECTIONS

Plant warmer (June 1992)

Resistor R_c was omitted from Fig. 2. The correct diagram is shown below.



Inductance-capacitance meter (March 1992)

The value of R_{16} and R_{17} should be 39 Ω, not 30 Ω as shown in the parts list.

8751 Emulator (March 1992)

The features list in the first column on page 53 should read:

- download, modify, and upload 8751 programs without having to erase and program an 8751.
- put breakpoints in programs.
- display register and memory contents.
- ...

  etc.

FM tuner – Part 3 (May 1992)

In the PSU parts list on page 54, R_{301} should be 150 Ω, 1%, not 150 kΩ, 1%.

Video enhancer (July 1992)

Preset P_2 is best adjusted for a signal level of 2 V_{pp} at the collector of T_2. Output transistor T_3 may run fairly hot: this is normal.

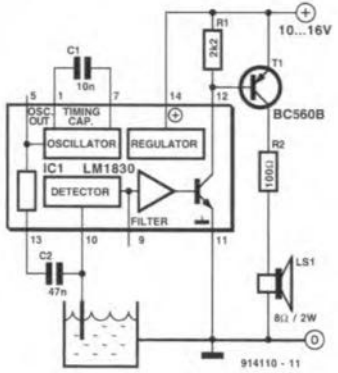
The third paragraph of the text on page 73 should read: The frequency characteristic of the signal at the base of T_3 is shaped by P_1, R_6 and C_8, and is, therefore, to a certain extent under the control of the user (with P_1).

Mark 2 QTC 80/40 loop antenna (July 1992)

The frequency '3800 kHz' mentioned twice under **2. 40-metre band** (page 90) should have read '7300 kHz'.

Audible fluid level indicator (July 1992)

Owing to a printing error, the diagram in this article is incorrect. The right diagram is shown below.



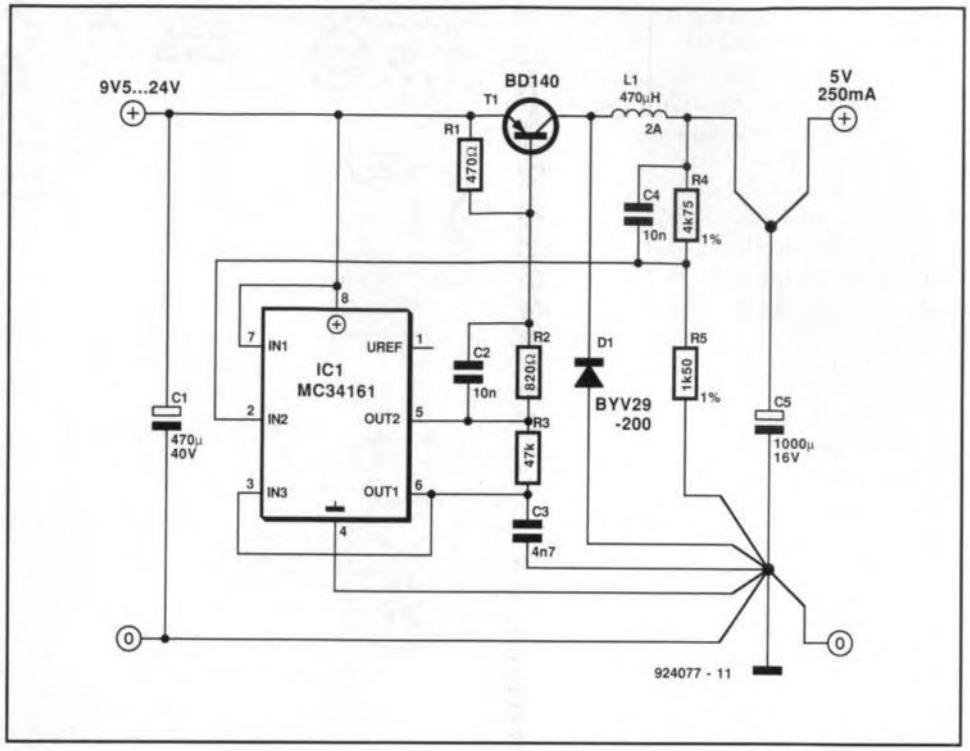
VOLTAGE CONVERTER II

ALTHOUGH a 9.5–24 V direct voltage can be brought down to 5 V easily by a standard regulator, the converter described here has the advantage that, since it is a switch-mode type, it hardly dissipates any heat. Its maximum, steady output current at 5 V is 250 mA, although it can cope with peaks of up to 750 mA.

The converter is based on a Motorola Type MC34161 circuit, to which a power stage, T_1 has been added. Inductor L_1, C_5 and D_1 remove any ripple from the output.

The internal comparator at pin 2 of IC_1 is connected to the output of the converter via potential divider R_4-R_5 to monitor the output voltage. The second comparator (pin 3) is used in the oscillator circuit and connected to pin 6 direct and to pin 5 via R_3-C_3.

When the supply is switched on, the output of the converter, and thus the voltage at pin 2, is 0; the oscillator operates normally. Transistor T_1 charges C_5 via L_1. When T_1 is off, L_1 ensures a supply of energy to C_5 via D_1. As soon as the terminal voltage of C_5 has risen to a sufficiently high level, the internal comparator at pin 2 changes state. The oscillator is then switched off via pin 6, so that T_1 is also off. After C_5 has discharged to an extent that its terminal voltage drops below the preset level, the oscillator is re-enabled, and C_5 is charged again via T_1.



The values of L_1 and C_5 determine the switching frequency; with values as shown, an input voltage of 12 V and a load current of 250 mA, the frequency is 18 kHz. At higher inductances and input voltages, the frequency drops.

It is essential that *all* earth connections are taken to the negative terminal of C_5 as shown in the diagram.

The inductor is a standard triac choke, to which a number of turns have to be added. If the inductance of the choke is $L\,\mu H$ and its number of turns is n, the number of turns, n' required for the present inductor is given by $n'=n\sqrt{(470/L)}$.

(Motorola Application – 924077)

CURRENT LIMITING FOR LM317 REGULATOR

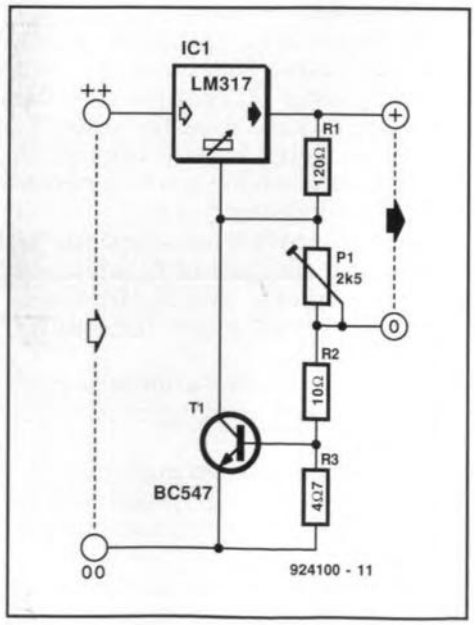
ALTHOUGH the well-known Type LM317 voltage regulator is already short-circuit-proof, there are cases where a limit of the heavy short-circuit current can be desirable. As the diagram shows, such a current limiting facility can be provided in a simple manner. Use is made of the fact that the output voltage, U_o, is dependent on the feedback to the control input. As long as the current limiting does not operate, resistors R_2 and R_3, as well as T_1, may be ignored, The output voltage is then:

$$U_o=1.25(1+P_1/R_1)+I_{adj}P_1 \text{ (volts)}.$$

Since the maximum level of I_{adj} is 0.1 mA, P_1 can set U_o to 1.25–27 V.

When the current through the regulator causes a drop of about 600 mV across R_3, T_1 will come on. This will cause a drop in the level at the control input of the regulator, and thus in the output voltage. With a value of R_3 as shown, the current limiting will come into operation at a current of 0.6/4.7=120 mA.

(National Semiconductor Application – 924100)



FRONT-TO-REAR WIPER COUPLING

ON some cars, it is convenient to couple the rear window wiper to the windscreen wiper. However, since the rear window does not get nearly as wet as the windscreen, particularly when the car is moving, the rear wiper should operate only once for every umpteen wipes of the windscreen. Note that your car may be one of the fortunate ones of which the rear window, when the car is moving in the wet, does not get wet at all because of the car's design.

The coupling shown in Fig. 2 ensures that the rear wiper operates once for every four or 16 wipes of the windscreen, depending on the setting of switch S_1 (as shown, once every four).

The clock for the circuit is taken from the return (terminal 53e – green/black wire on most cars) of the windscreen wiper motor—see Fig. 1. This signal, which is a square-wave, is applied to IC_1 via K_1. Its level is lowered to not more than 5 V by potential divider R_1-R_2 to prevent any damage to IC_1. Any noise from the car's electrical system is bypassed by C_1.

The Q_2 output (pin 1) of IC_1 goes high every fourth clock input, and the Q_4 output (pin 3) once every eighth clock input.

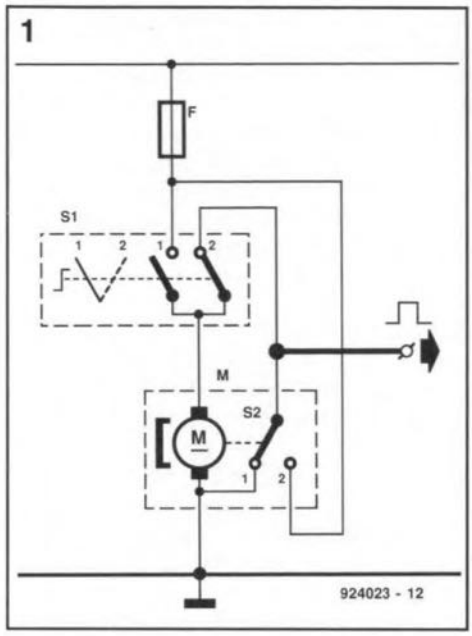
The trailing edge of the signal at S_1 is transformed into a trigger pulse by R_5-C_3. This pulse, whose length is determined by R_7-P_1-C_6, is applied to monostable IC_2. The length of the pulse should be set to about one second to give the rear wiper time to get going.

The monostable drives transistor T_1, which in turn controls relay Re_1 This relay is a motorcar type that can handle the large switch-on current of a wiper motor: it may be rated at 25 A or 35 A.

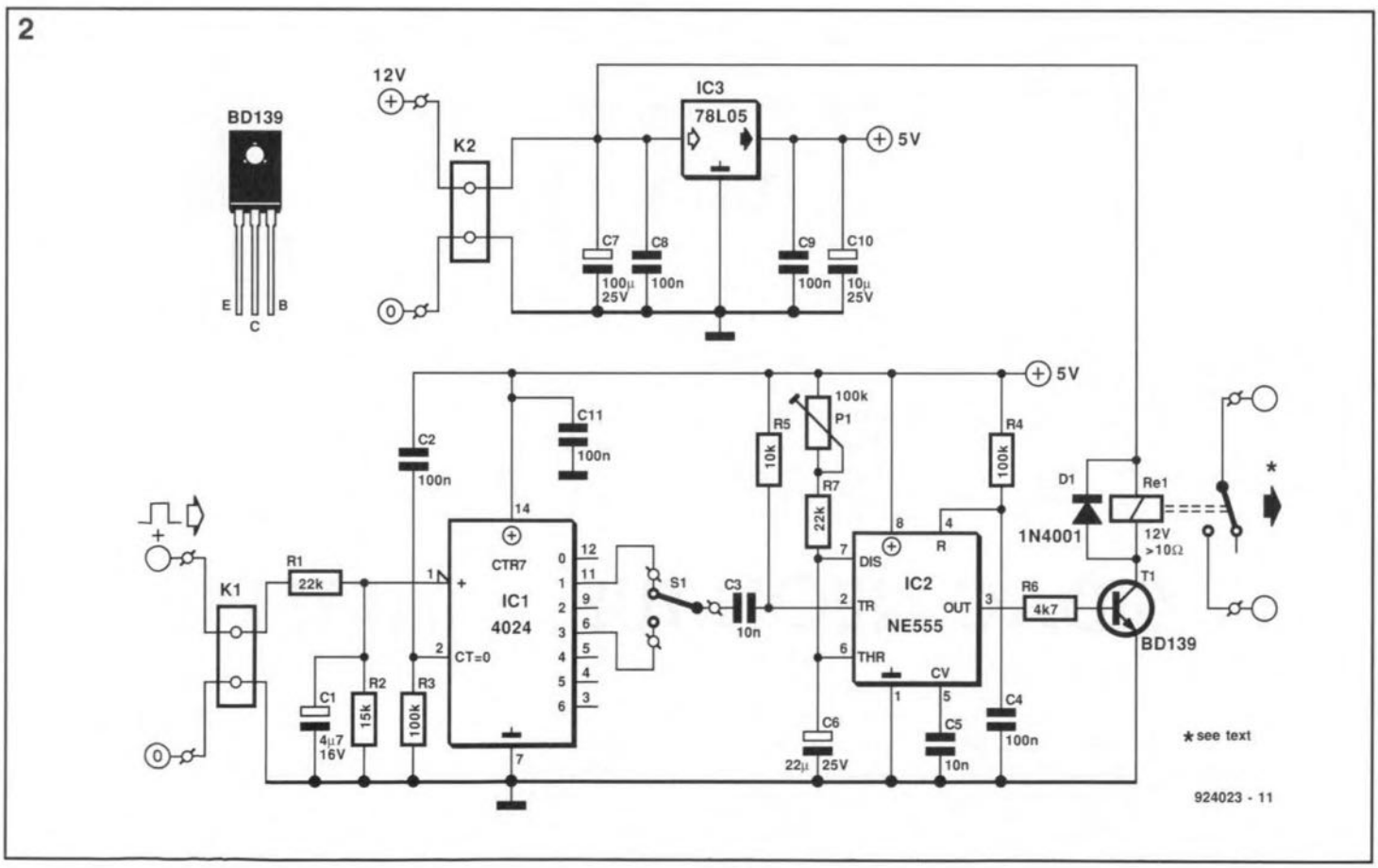
The supply for the circuit is provided by IC_3, which brings down the car voltage of 12 V to 5 V. This IC also prevents large peaks on the battery voltage from reaching the circuit.

[I. Fietz – 924023]

1



2



THREE-PHASE SIMULATOR

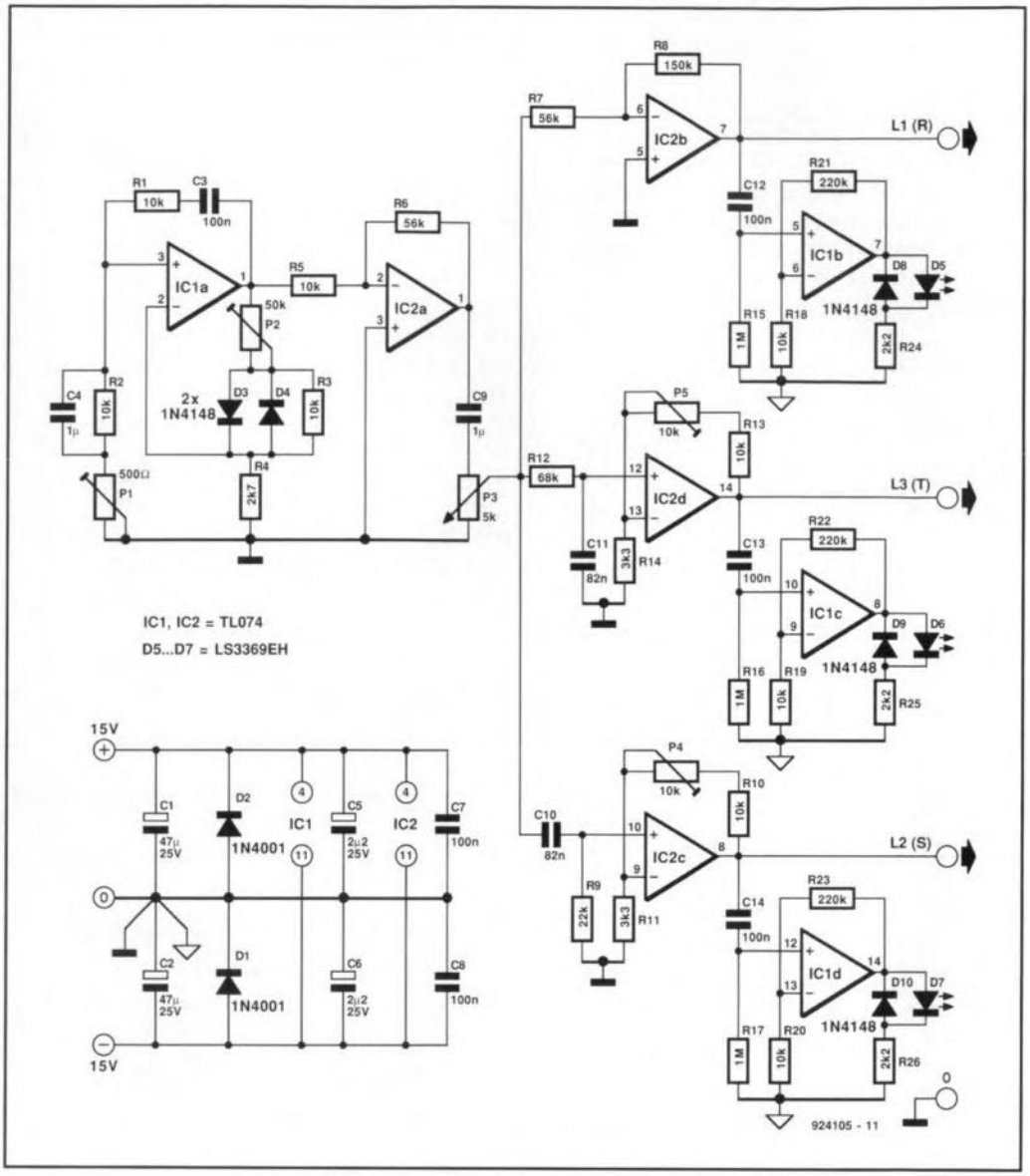
MOST domestic consumers (in the UK) are provided with a single-phase supply, unless exceptionally heavy loading is foreseen. It may, however, occur that a low-voltage three-phase supply is required for experimental purposes and in such cases, the simulator can prove useful.

The source signal for the phases, R, S and T is generated with a standard Wien bridge. The sine-wave generator is formed by IC_{1a}. Preset P_1 enables the frequency to be set accurately to 50 Hz; the output level (pin 1) is set with P_2 to 1 V (peak).

Circuit IC_{2a} provides a constant load impedance for IC_{1a}, which is important for the stability of the generated frequency. It also raises the signal level to 5.6 V (peak). The peak value of the phases is set to 0–12 V with P_3. Series capacitor C_9 prevents the offset voltage of IC_{1a} and IC_{2a} adding direct voltage to the outputs of IC_{2b} and IC_{2d}.

The R phase results from inverting the signal at the wiper of P_3, that is, shifting it by 180°. Owing to low-pass filter R_{12}–C_{11}, the T output lags the signal at the wiper by 60°, while R_9–C_{10} provide a 60° lead at the S output. There is, therefore, a 120° phase difference between any pair of phases.

Presets P_4 and P_5 need to be set only once and that in such a manner that the peak values of the three phases are identical.



Low-current LEDs D_5–D_7 light only if there is an alternating voltage present at the associated output. An accidentally short-circuited phase is, therefore, detected immediately.

The opamps are short-circuit proof and can provide a current of about 10 mA. When a symmetrical ±15 V supply is used, the quiescent current is ±20 mA.

(J. Ruiters – 924105)

SIDAC NEON TUBE STARTER

THE sidac from Motorola is best compared with a triac of which the gate connection is missing. It switches on whenever the voltage across it exceeds a certain level. The polarity of that potential is immaterial: likle a triac, the sidac works equally well with direct and alternating voltages. Furthermore, when the sidac is on, it resembles a short-circuit and remains in that state until the level of the current drops below a certain value (the holding current), whereupon it switches off.

A series network of a sidac and a load connected to the mains results in a kind of dimmer whose, non-variable, phase angle depends on the starting voltage of the sidac. Sidacs are available for starting voltages between 104 V and 280 V.

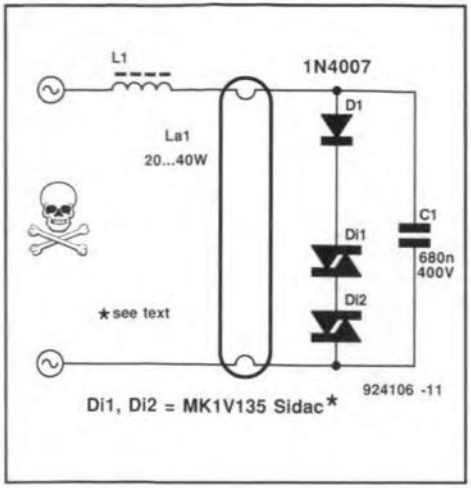
A neon tube does not switch on as easily as an incandescent lamp because the tube can start only at a voltage much higher than the mains, after which it will remain lit at the mains voltage. The level of both the starting voltage and the working voltage depends on the temperature of the tube.

Normally, the high starting voltage is obtained by interrupting the current through a choke. This is usually done by the starter, which also ensures that a fairly large current flows through the filaments of the tube. This heats the ends of the tube, which makes starting easier.

These tasks of the starter are taken over by two 135 V sidacs (or a single 270 V one). The starting voltage is

thus 270 V, which is below the peak value of the mains (about 340 V), but higher than the working voltage of a 20–40 W neaon tube.

As long as the tube has not started,



almost the whope of the mains voltage is dropped across the starter. Assume for a moment that the polarity of the mains causes D_1 to be forward biased. When the instantaneous value of the mains voltage reaches the level of the starting voltage of the sidacs, these will short-circuit the starter, whereupon a fairly heavy current will flow through the filaments and the coil. This gives rise to a magnetic field around L_1. When the polarity of the mains voltage reverses, the positive current through L_1 will decrease gradually. When the level of the current approaches zero, the sidacs switch off, whereupon the instantaneous negative mains voltage is applied across the tube immediately, because of C_1 being charged rapidly. This capacitor and the starter form a series resonant circuit that magnifies the sudden drop across the tube to way above the level of the mains voltage.

During the next positive period of the mains voltage, the sidacs switch on again, and the sequence repeats itself until after a few cycles the tube has warmed up enough to remain lit. The drop across the lit tube does not exceed the starting voltage of the sidacs, so that the electronic starter is switched off.

Capacitor C_1 not only suppresses any r.f. interference generated by the tube, but also makes the load on the mains supply less inductive (so-called cosϕ improvement).

The capacitor and diodes can probably be fitted into the man-made fibre enclosure of the original starter.

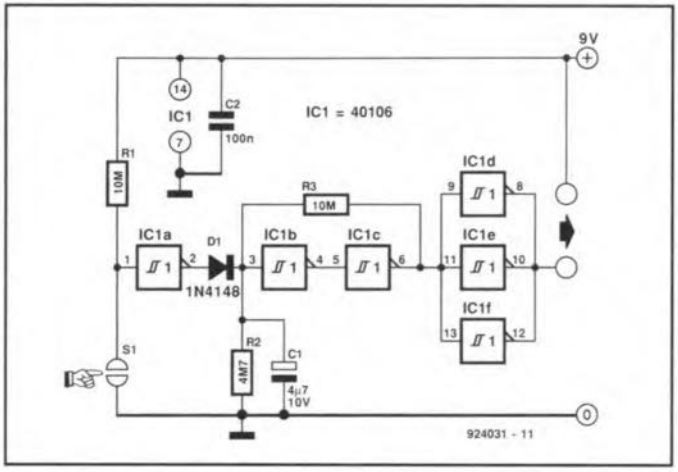
(Motorola Application – 924106)

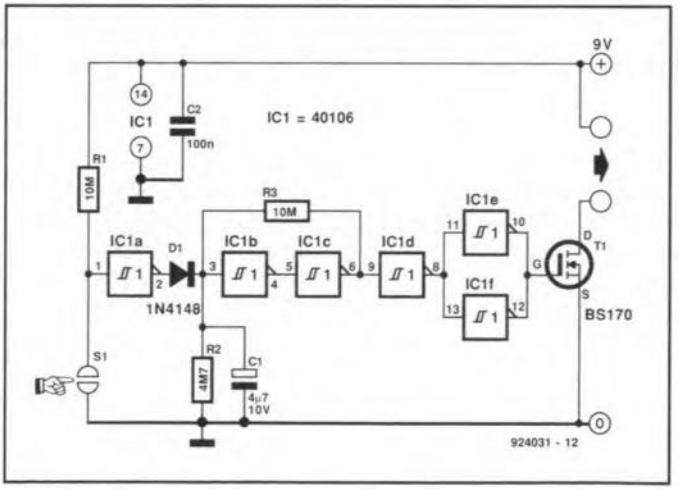
TOUCH 'ON', AUTO 'OFF' CONTROLLER FOR BATTERY-OPERATED EQUIPMENT

THIS handy circuit is intended for battery-operated appliances. It functions as a touch-operated supply on switch and delayed supply off switch. Figure 1 shows the design for applications that require only a few milliamperes. Figure 2 is identical but for the added FET at the output, which enables up to 300 mA to be switched.

The active electronics is formed by six Schmitt triggers contained in a Type 40106. The touch key consists of two small conducting plates that can be interconnected by our skin resistance. When the key is not touched, R_1 causes a high level at the input of IC_{1a}. That gate is followed by a diode, D_1, which ensures that C_1 can be charged only if the output of IC_{1a} is high. When the key is touched, C_1 is charged rapidly. The capacitor discharges slowly via R_2: the state of its charge is monitored by N_2-N_3-R_3.

The shunting of gates IC_{1b} and IC_{1c} by resistor R_3 greatly increases the hysteresis at the input of IC_{1b}. That means that the output of IC_{1c} goes high only when C_1 is almost fully charged, and changes state again only when C_1 is nearly discharged.





Gates IC_{1d-f} serve as output buffers.

The appliance connected to the output terminals will be provided with power as soon as the touch key is operated, because C_1 will then be charged rapidly. The discharge time of this capacitor (and thus the time that the appliance is powered) is fairly long and depends on the value of R_2 and the leakage resistance, and may, therefore, be extended by giving R_2 a higher value. Note that it is not advisable to increase the value of C_1 by much, because that increases the charging time and, worse, simply touching the key may not be sufficient any more. When C_1 is nearly discharged, the supply to the connected appliance is switched off.

(R. Evans – 924031)

REV COUNTER FOR DIESEL ENGINES

ALTHOUGH most petrol-engined cars and lorries have a rev counter as standard, that is by no means the case in diesel-engined motor vehicles. The reason for this is that, since a diesel engine has no contact breaker, it is not so easy to derive pulses to drive a rev counter. There are, none the less, several possibilities of adding a rev counter if so desired.

Firstly, it would be possible to take the pulses from terminal W of the alternator. Unfortunately, that machine does not run at the same speed as the engine, so that some arithmetic unit would have to be added. Moreover, and more seriously, terminal W of modern alternators is no longer accessible externally.

A second way might be to attach a small magnet to each of the cranks on the crankshaft and so induce magnetic pulses in a fixed coil. The problem here is to attach these magnets securely.

A third method is an optical one proposed in this article. In this, the cranks are divided into sectors that are painted alternately white and black. A home-made light barrier is then used to evaluate the speed with which the sectors are rotating. If the cranks are divided into four sectors, pulses are generated that are suitable for driving commercially available rev counters, irrespective of whether the diesel engine has four, six or eight cylinders.

The circuit in Fig. 1 may, therefore, be considered as an adaptor for the rev counter.

A small 12-V bulb lights the crankshaft, whereupon the light reflected by the white sectors falls on to phototransistor T_1. This transistor is connected in a darlington configuration with T_2. The type of phototransistor is not important: it is thus not necessary to use the BP103 shown in the diagram. The output of T_2 is applied via C_2 to IC_1, where it is chopped and amplified by about ×50 to give a a rectangular output signal of about 10 V_{pp}. That signal is perfect for driving a rev counter.

The circuit is best built on a small piece of prototyping (vero) board and then fitted in a tube, whose front is closed watertight by a circular piece of perspex. It may be necessary to separate the lamp and the phototransistor by a dark screen.

The circuit is connected to the rev counter by a three-core cable. The cable connections (+12 V, earth and pulse signal) to the circuit must be waterproof.

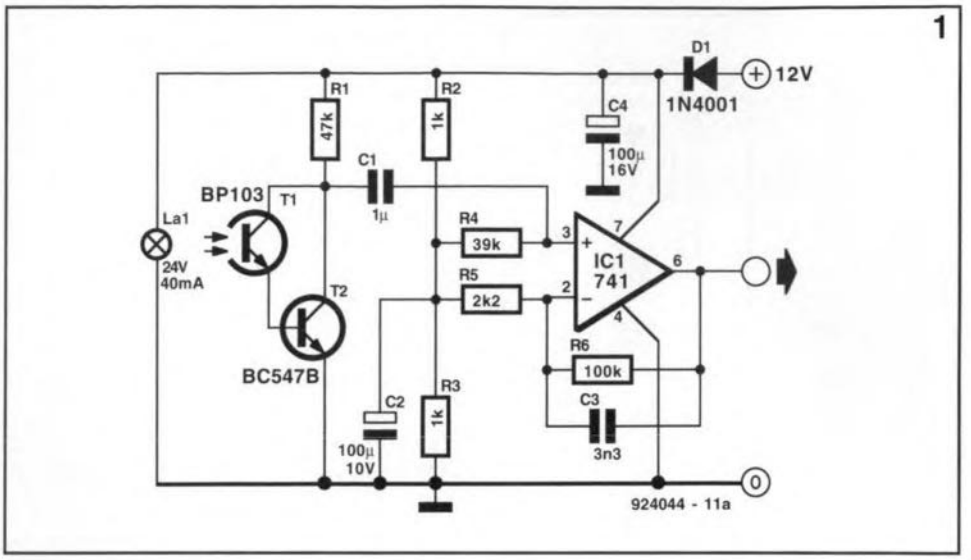
If the lamp is found to be too bright, it may be connected in series with a small resistor.

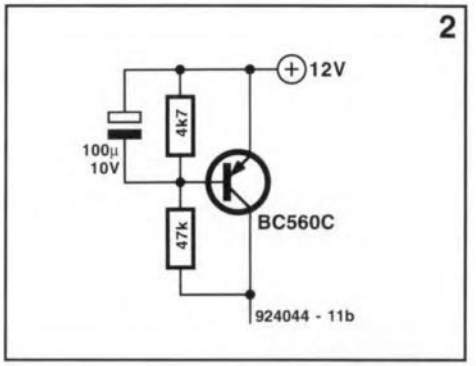
The circuit can be tested by measuring the voltage at the collector of T_2, which should be 1–5 V when a white sector is being illuminated.

If the sensitivity is too high, replace R_1 by the circuit in Fig. 2, which keeps the voltage at the collector of T_2 at around 5 V.

The circuit draws a current of about 10 mA plus the current through the lamp.

[N. Sauer – 924044]





SMARTEC TEMPERATURE SENSOR

THE Smartec Type SMT160-30-18 is a temperature sensor with a digital output, and housed in a TO-18 case. Pins 1 and 3 are are the supply input pins. With a nominal 5 V supply, the current drain is not more than 200 µA. At pin 2, a short-circuit-proof and TTL compatible output, a rectangular voltage with a pulse repetition frequency (p.r.f.) of 3 kHz is available. The value of the frequency is not all that important, because the actual temperature data are stored in the duty factor (that is, the ratio of the pulse width to the pulse spacing). There is a linear relation between the temperature, T and the duty factor:

$$\text{duty factor} = 0.32 + 0.0047 \times T.$$

Thus, at a temperature of –45 °C, the lowest at which the sensor can be used, the duty factor is 0.109. The maximum temperature at which the sensor can be used is 130 °C. The sensors are calibrated to an accuracy of ±0.25 °C during production.

In principle, it would be feasible to apply the rectangular signal to a moving coil meter. This would indicate a value that is directly proportional to the average voltage level of the rectangular signal and thus with the duty factor and the temperature.

```
program SMARTEC;
(**************)

{ SMARTEC: V1.0/JR.    }
{ Turbo Pascal 5.5.    }

{$R-,S-,I-,F-,O-,A-,V+,B-,N-,E+,D-,L-}

uses
  crt,dos,PMEASURE;
const
  ErrStr1='Error: load sequence ADCF.CFG aborted!';
  ErrStr2='Error: multifunction PC card not found!';
  SmartChan=7;

procedure Measure;
(****************)
var
  PulseLevel:HighOrLow;
  DutyCycle:real;
  Time:record
    High,Low:Second;
  end;
  Dummy:Char;

function Temperature(DutyCycle:real):real;
(**************************************)
const
  a=0.32;
  b=0.0047;
begin (* Temperature *)
  Temperature:=(DutyCycle-a)/b;
end;  (* Temperature *)

begin (* Measure *)
  with Time do
    begin
      High:=0;
      Low:=0;
    end;
  PulseLevel:=Low;
  SelectFreqChannel(SmartChan);
  StartPulseTimeConversion(PulseLevel);
  repeat
    if PulseTime.Updated
      then
        begin
          if PulseLevel=High
            then
              begin
                Time.High:=PulseTime.Value[SmartChan];
                PulseLevel:=Low;
              end
            else
              begin
                Time.Low:=PulseTime.Value[SmartChan];
                PulseLevel:=High;
              end;
          with Time do
            begin
              if (Low>0.1E-6) and (High>0.1E-6)
                then
                  begin
                    DutyCycle:=High/(High+Low);
                    write('Temperature: ',Temperature(DutyCycle):5:1,' °C ');
                    writeln('(',DutyCycle*100:4:1,' %)');
                    gotoxy(1,1);
                  end;
            end;
          delay(500);
          StartPulseTimeConversion(PulseLevel);
        end;
  until keypressed;
  Dummy:=readkey;
end;  (* Measure *)

begin (* SMARTEC *)
  clrscr;
  if ConfigFileErrorCode<>0
    then
      begin
        writeln(ErrStr1);
        Beeps(2);
      end
    else
      if not HardwareFound
        then
          begin
            writeln(ErrStr2);
            Beeps(3);
          end
        else
          begin
            InstallTimeIntHandler;
            InstallHardwareInthandler;
            Measure;
            UnInstallHardwareIntHandler;
            UnInstallTimeIntHandler;
          end;
end.  (* SMARTEC *)                                    924110 - 12
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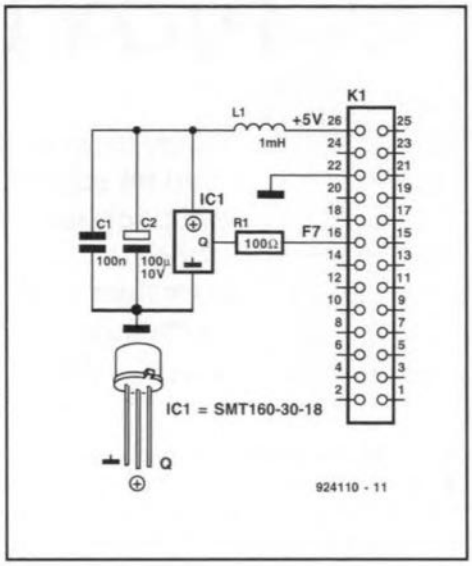


In practice, it is, however, much more sensible to connect the sensor to a digital input port of a peripheral interface or a microcontroller. Sampling the rectangular signal enables the computer system to carry out temperature measurements with a minimum of external components as shown in the diagram. A suitable PC measurement card was published early last year (see Ref. 1). Connector K_1 is a 26-way box header that is linked to connector K_6 of the measurement card via a short length of flatcable. The 5 V supply is taken directly from the computer. On the the prototype, L_1-C_1-C_2 proved essential to prevent jitter of the signal, which caused the first digit after the decimal point to move to and fro.

The program for controlling shown here is also available, with other basic routines for the measurement card through our Readers' services (ESS 1753)

(J. Ruiters – 924110)

Reference

'Multifunction measurement card for PCs', *Elektor Electronics*, February 1992, p. 14.

FUZZY LOGIC: AN INTRODUCTION

Fuzzy logic is a kind of statistical reasoning, whose foundations can be said to have been laid in the 18th century by the British philosopher Thomas Bayes. With this technique, large amounts of data can be condensed into a much smaller set of variable rules than with rigid logic. The result is an expert system that can process information faster, and provide a more flexible, more human-like response than conventional logic.

THE great German polymath, Gottfried Leibniz (1646–1716), dreamed about devising a way whereby a couple of philosophers could discuss and settle any human argument once and for all by pure logic. But he and many other thinkers after him have discovered that there are many problems that cannot be solved by just logic. This realization gave rise to another way of attempting to solve problems: the use of statistics. In statistical reasoning, probabilities express the idea of 'perhaps'. One method of statistical reasoning, whose foundations can be said to have been laid in the 18th century by the British philosopher Thomas Bayes, is called fuzzy logic. In fuzzy logic, there is not just 'true' and 'false', 1s and 0s, 'black' and 'white', but also all the various grades of grey in between. Fuzzy logic can condense large amounts of data into a much smaller set of variable rules than rigid logic. The result is an expert system that can process information faster, and provide a more flexible, more human-like response than conventional logic. For example, a washing machine controlled by fuzzy logic will wash very dirty clothes very hard; not-so-dirty clothes get a milder wash, and so on. Fuzzy logic is already being used in many domestic appliances, cameras and passenger trains.

Traditional control technology is based on a mathematical model that describes the control process. Although this is perfectly satisfactory for simple processes, it gets more difficult as the process becomes more complex. In such cases, the solution is derived from a simplified model or from a set of values that was determined empirically.

An example from everyday life would be when you are driving along in your car and you want to turn left (or right): without conscious calculation you determine the moment when you have to start turning the steering wheel. Without precise information of the width of the roads, the position of your car, the way the front wheels of your car react to the turning of the steering wheel, the wheel base of your car, and so on, you will normally act so that you do not get on the wrong side of the road or on the pavement. In the same easy manner, you can steer your car, or that of your neighbours, through completely different bends. What you are doing is reacting in a 'fuzzy-logical' way to the effect of an action. You turn the steering wheel a little, your eyes register the effect of this and your brain corrects, if necessary and without complex analyses and calculations, the action. If we were to have this, to us simple, operation carried out by a digital control system, we would have to design a surprisingly compiex system that would, moreover, require a fairly large computer power. However, for a control system based on fuzzy logic, the rules would be based on human practical experience. For instance, at home:

if the room temperature is much *too low*, turn up the thermostat *to maximum;*

if the room temperature drops *slowly*, turn up the thermostat *a little*.

But how do we define *too low*, *slowly*, and *a little*? Fortunately, fuzzy logic can cope with these terms, as we will see later on.

Collecting data

An important principle of fuzzy logic is *set theory* (in mathematics, a set is a collection of elements chosen for membership of the set because it possesses some required property). This may be illustrated by, say, our desire to go out and buy fragrant red roses. We may go to a market and find a stall that sells flowers. We make our wishes known to the stall-holder, who subconsciously may reason: '*if* the flower is a rose, *and* if it is red, and *if* it is fragrant, *then* the customer will buy a bunch'. In other words, if the flower is an *element* of all three collections (rose, red, fragrant), it is the desired one. This is illus-

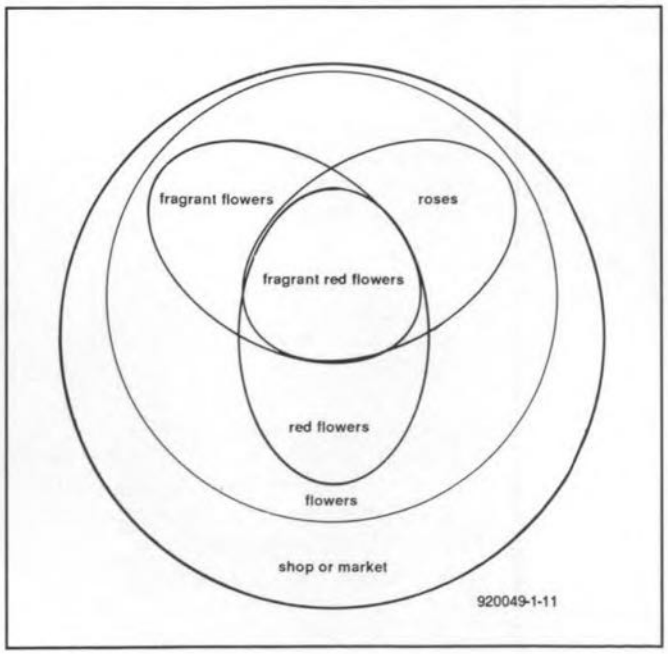


Fig. 1. Venn diagram of choices in a flower shop.

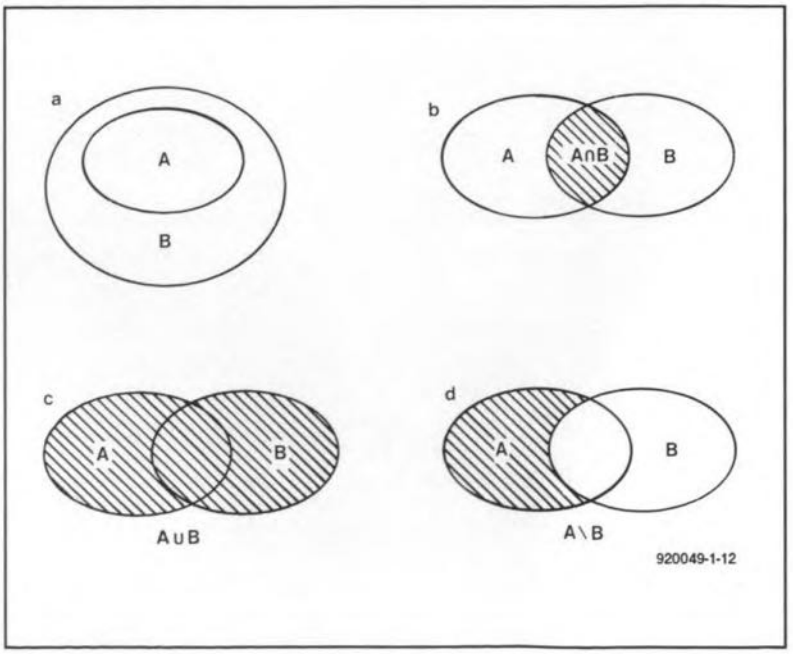


Fig. 2. Various basic operations in Set Theory.

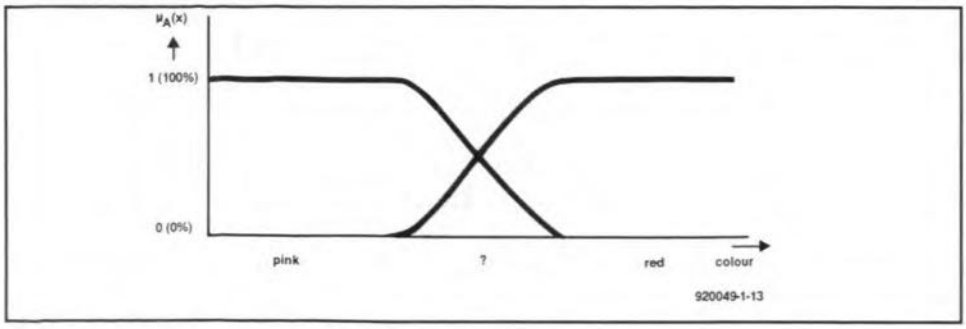


Fig. 3. Typical 'degree of association' cruve.

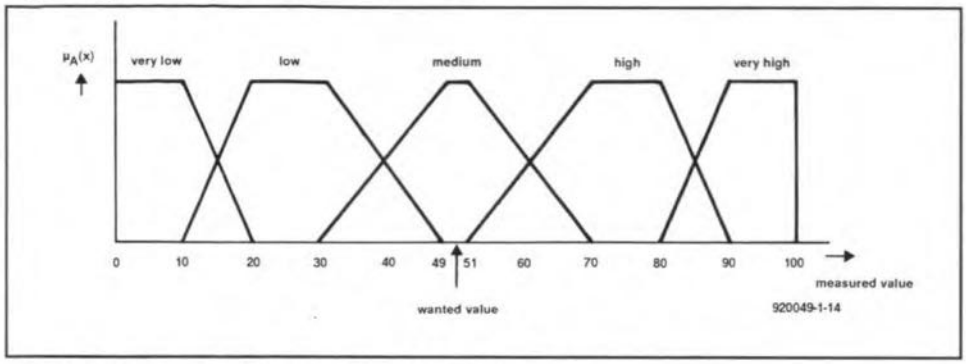


Fig. 4. Example of a fuzzy division of a measured value.

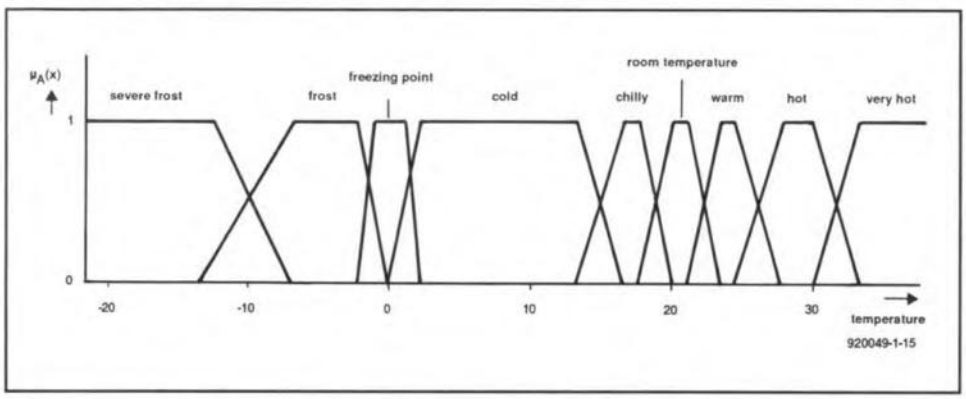


Fig. 5. Allocating likely values of temperature to fuzzy sets.

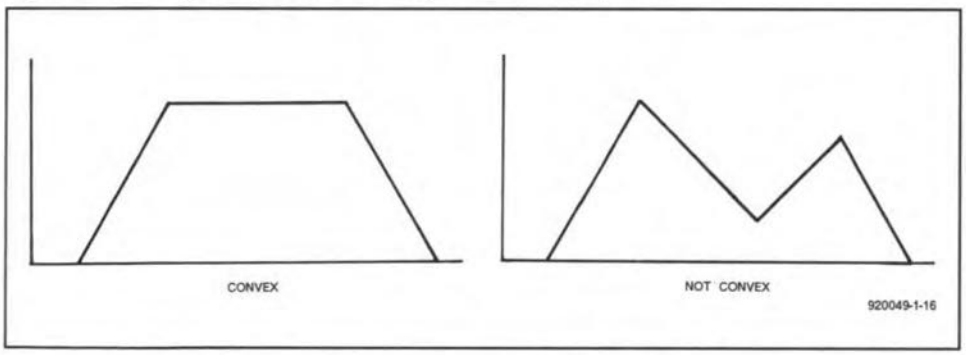


Fig. 6. The 'degree of association' curve should be as at the left, not as on the right.

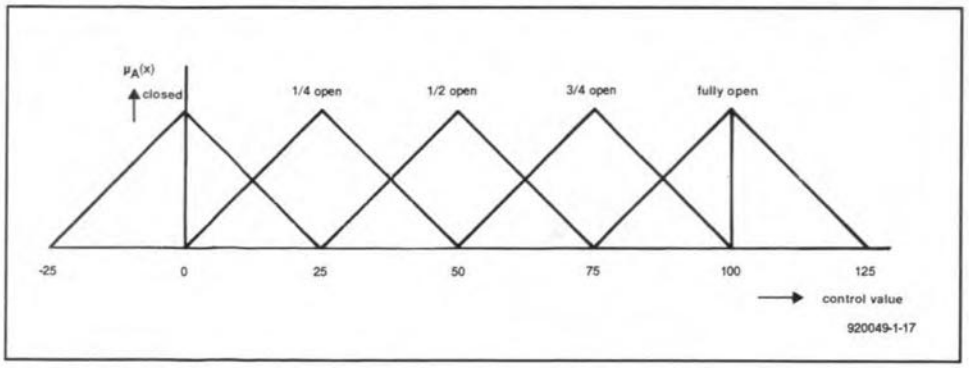


Fig. 7. Fuzzy sub-division of output signals.

trated in the Venn diagram in Fig. 1.

In the logic rule we use to arrive at a final conclusion, we make use of a number of basic operations that are illustrated in Fig. 2, another Venn diagram. Figure 2a shows the simplest situation that can occur: from a set B, a new set A is formed, such that all elements of A are also elements of B. Such a set A is called a *subset* of B. Mathematically, this is expressed as $B \supset A$, read as 'A is a subset of B'. A more general situation arises when two sets A and B are involved, each of which possesses elements that are not common to to the other, so that neither $A \supset B$ nor $B \supset A$ is true. The set of elements C that is common to the two sets is called the *intersection* of sets A and B and is written $C = A \cap B$; this is illustrated in Fig. 2b. Another important set related to sets A and B is the set C containing all the elements belonging to A, to B or to both A and B. This is called the *union* of sets A and B and is written $C = A \cup B$, read as 'A cup B'; it is illustrated in Fig. 2c. Finally, in connection with sets A and B, there is the *complement* of B relative to A, which is written as $A \backslash B$ and read as 'A minus B'; this is illustrated in Fig. 2d.

All this is still clearly defined, but in the earlier instance of the red roses, we could ask: 'What is red; where does pink begin?'. In general, the colours red and pink will be recognized as such by most people, but in between them there is a range of hues that is not clearly red or pink. That sort of problem is solved by the use of fuzzy sets, in which a clearly red flower is entirely common to the red set and not at all to the pink set. A flower with a colour in between red and pink is common to both sets, for instance, 70% red and 30% pink. This is called the *degree of association*, μ. For example, the degree of association of an element x to a set A is written as $\mu_A(x)$. The degree of association is shown by the curves in Fig. 3.

The type of characteristic shown in Fig. 3 is an important aid in the application of fuzzy logic in control engineering, because it enables measured values to be arranged in sets. The measured values (input signals) are entered on the x-axis, while the degree of association curves for a number of sets are plotted on the y-axis—see Fig. 4. In the design of control systems, it is usual to take an odd number of sets and to place the centre one in a position where it coincides with the desired value: here, 50.

Another instance of allocating likely values of ambient temperatures to fuzzy sets is shown in Fig. 5. The boundaries between areas are not always clearly defined; in fact, in this way it may be determined how 'fuzzy' the boundary between two sets is. It is customary, but not obligatory, to allow the boundaries to overlap to such an extent that the combined border areas have a degree of association of 100%, that is, μ=1.

It will have been noticed in these examples that the curves of μ are trapezoidal. This is the most customary shape, since it allows straightforward arithmetic. Other shapes are possible, as long as they are convex, that is,

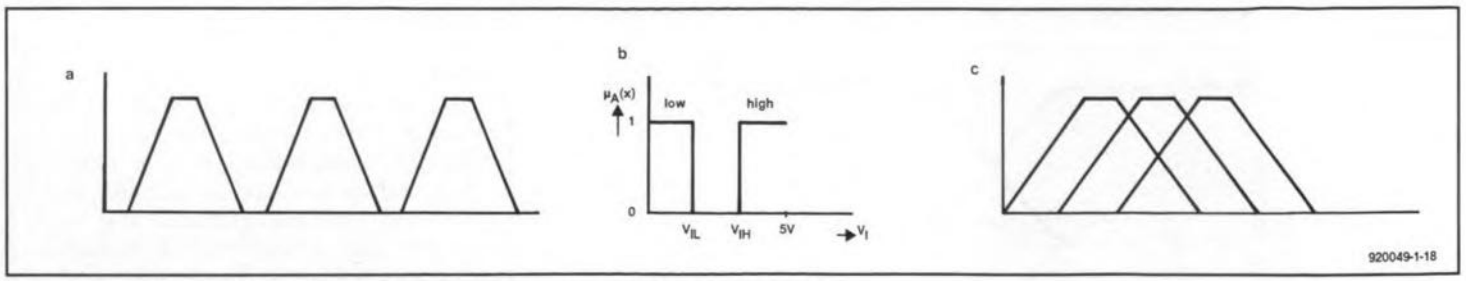


Fig. 8. Examples of how not to sub-divide fuzzy input and output signals.

their edges should not have transitions as shown in Fig. 6. It is, however, possible to omit the horizontal top of the trapezium so that the curves attain a triangular shape. This is done, for instance, in the case of a set that represents the desired value of a control system to obtain a very accurate setting. It is always done when the subdivision of output signals is fuzzy—see Fig. 7, which shows the positions of a boiler valve in a heating system. It may look strange that the µ-characteristic for 'closed' extends to –25% and that for 'open' to +125%, but that is how these sets are weighted to the same scale as the other three positions. Once the output signals have been brought back to concrete values, the valve can be set exactly between 0% and 100%, no more, no less.

Examples of how not to subdivide input and output signals are shown in Fig. 8. The curves in Fig. 8a do not overlap, which means that there is no defined µ for a number of values. A well-known example of this is the inputs of TTL-gates—see Fig. 8b. In these, a certain range of values belongs to the set 'low' and another range to the set 'high'. Values between these ranges will lead to unpredictable behaviour. This is, by the way, a special fuzzy set: a so-called crisp-set. In Fig. 8c, the edges of the various curves spill over into various other sets: this will lead to instability.

Logic combining of fuzzy sets

We have seen how input and output signals can be divided into fuzzy sets. To use these to make a practical control system, certain rules are required to indicate the logic connections between input and output sets. These rules, which describe and determine the behaviour of the system, can be arrived at through practical experience of the system or by trial and error.

As an example of how to go about setting the rules, we will use a system that has a switch-on behaviour as shown in Fig. 9b. This is quite a common behaviour: for a little while after switch-on, the measured value will swing around the wanted value. It is the task of the control system to bring the measured value to the wanted value quickly and to keep it there in spite of possible interference. To design the system, we set out the error, that is, the difference between measured and wanted values (Fig. 9c) and also the variations in the measured value (Fig. 9d). The *x*-axes of these figures show no concrete values, only a 0. In practice, the allocating of concrete values together with the selecting of sensible sets (and the rules mentioned earlier) will be the key to a successful design.

The fuzzy division of the control signal is approached in two ways. First, we divide the magnitude of the signal into seven sets—see Fig. 9e. These sets enable us to give the system a proportional-control behaviour. To ensure that the system responds timely to the reactions of the process (integrating and differentiating), we need a number of sets that indicate by how much the control signal must be corrected to prevent overshoot, or to limit it to a wanted minimum value—see Fig. 9f.

Next, we have to formulate the rules necessary to keep the measured value equal to the wanted value. They are summarized in Table 1. Rules 1–7 must ensure that through proportional control the measured and wanted values are kept equal, or nearly so. Rules 8–14 ensure through integrating control that the value of the control signal is corrected as relevant to obtain the wanted value. Overshoot of the control signal after the wanted value has been reached is prevented by rules 15–21, which, when the error becomes smaller, slow down the altering of the measured value. All the rules together ensure that the system reacts rapidly without overshoot.

In fuzzy logic, all these considerations can be evaluated by simple arithmetic and a computer or analogue electronics. There are processors and controllers designed specifically to carry out fuzzy-logic computations. It is interesting to note that an algorithm to carry out these computations would need a 32-bit microprocessor, whereas in fuzzy logic an 8-bit microcontroller is sufficient.

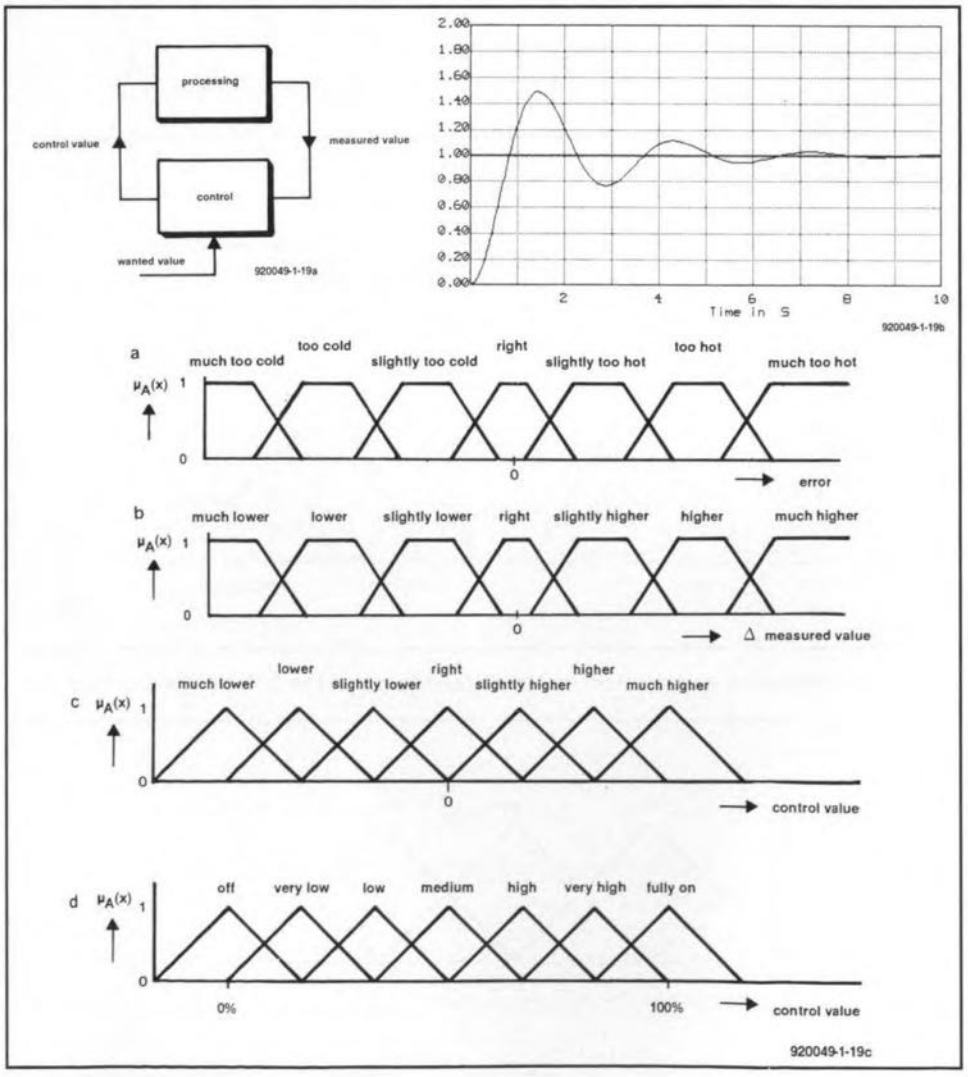


Fig. 9. Example of how to compute a control system.

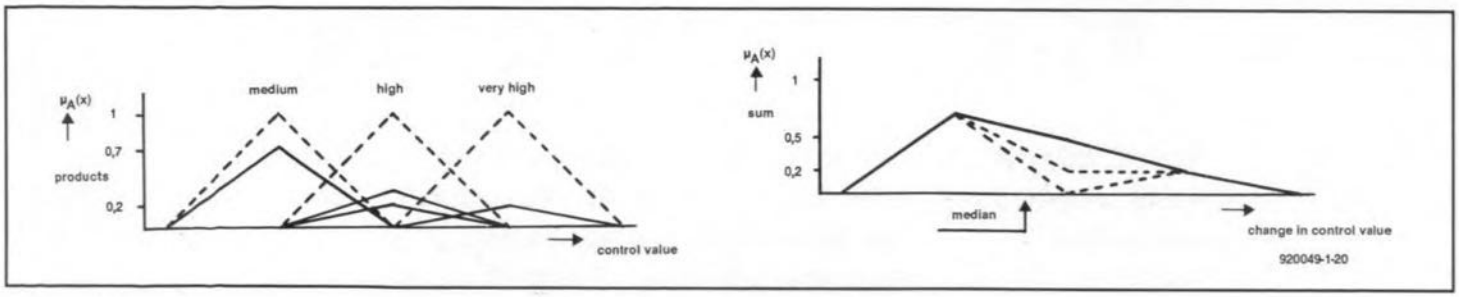


Fig. 10. Computation of the control signal for the system illustrated in Fig. 9.

Fuzzy logic arithmetic

The function $\mu_A(x)$ enables us to calculate to what degree an element x is common to set A. If we use a microcontroller and an analogue-to-digital (A-D) converter, the calculation becomes very simple, because the converter provides concrete values. For each of these values, the associated μ can be found in relevant tables.

Evaluating the logic rules is normally simplicity itself. There are three basic operations: AND, OR and NOT. In an AND-operation, the smallest μ-value of the relevant sets is allocated to the output set. If, for instance, two inputs, x and y, have values of $\mu_A(x)=0.8$ and $\mu_B(y)=0.3$, it follows from the logic rule 'A AND B gives C' ($A.B=C$) that the smallest μ, that is, 0.3, must be allocated to C. This is done by adding an element of value 0.3 to set C. This operation is called minimum-operator (MIN{A,B}) and is one of the special instructions in fuzzy logic.

The OR-operation allocates the largest μ-value to the output set. This operation is called maximum-operator (MAX{A,B}). With the values from the previous example, the logic rule 'A OR B gives C' ($A+B=C$) gives an element with a μ-value of 0.8.

The NOT operation is just as simple: deduct the μ-value from 1: NOT $A=1-\mu_A(x)$.

Compensating operations yield results that lie somewhere between AND and OR; they add a sort of 'but' to the logic rule. For instance, you want to buy a house. It must be sound, in a good position, and not too expensive, *but*, if it is very nice and well situated, it may cost a little more. In pure logic terms, such a consideration is difficult to realize, but compensating operators make it possible. The most important of these is the gamma-operator. If the value of y lies between 0 and 1, this operator can be set between AND and OR. The simplified form of the gamma-operator (for three sets) is

$$\mu_r(x)=[\mu_A(x)\mu_B(x)\mu_C(x)]^{(1-y)} \times \times\{1-[1-\mu_A(x)][1-\mu_B(x)][1-\mu_C(x)]\}^y,$$

where $\mu_r=\mu_{result}$ and $0\leq y<1$.

Fuzzy becomes distinct

After working through the logic rules, we have a number of indications (21 in Table 1) of what has to happen next. All the results in Table 1 refer to a signal that controls the relevant process. In complex processes, more control signals may be used. For the calculation of concrete values for these signals, a method is needed that somehow combines the results relevant to the signals. There are two usual methods: min-max-median and product-sum-median. The former is simple, but not suitable for the example in Table 1, because several logic rules apply to the same output set. In that case, the product-sum-median method must be used.

Assume that on evaluation of the logic rules the following results have been obtained: 0.7 median; 0.2 and 0.3 high; and 0.2 very high. How the product-sum-median method works is shown in Fig. 10. For each element, we multiply the height of the triangle indicating the μ of a set with the value of the elements and use the results to draw four new (smaller) triangles. We then add the areas of the triangles together and determine the median position of the resulting figure: the value on the x-axis underneath that position is the value we seek.

All this may sound pretty complicated, but the arithmetic is not too difficult. If we assume that the functions of μ for the control signals are isosceles triangles, the calculation becomes:

$$S_c = \frac{\sum_{x=1}^{q}[\alpha(x)\times S_a \times A]}{\sum_{x=1}^{q}[\alpha(x)\times A]}$$

where:

S_c is the value of the control signal;
q is the number of logic rules whose value is relevant to the magnitude of the control signal;
$\alpha[x]$ is the result of logic rule number x;
S_a is the value of the control signal immediately underneath the apex of the triangle (set) to which logic rule x refers;
A is the area of the relevant triangle (set) ($A=^1/_2 \times$ base $\times$ height).

This formula is worked out in a computer in seconds: S_a and A are fixed data for all sets, which, therefore, can be stored in memory and need not be computed. If all triangles have identical areas, as in the example, the calculation becomes even simpler, because A can then be ignored both in the numerator and the denominator. ■

Table 1.

	error	Δ measured value	control value
1.	much too cold		full on
2.	too cold		very high
3.	slightly too cold		high
4.	right		medium
5.	slightly too hot		low
6.	too hot		very low
7.	much too hot		off
8.	much too cold		much higher
9.	too cold		higher
10.	slightly too cold		slightly higher
11.	right		right
12.	slightly too hot		slightly lower
13.	too hot		lower
14.	much too hot		much lower
15.	slightly too cold	much higher	off
16.	slightly too cold	higher	very low
17.	slightly too cold	slightly lower	high
18.	slightly too cold	lower	high
19.	slightly too hot	higher	off
20.	slightly too hot	much higher	off
21.	slightly too hot	much lower	high

Reference

Fuzzy sets, theory and its applications, by H.J.Zimmermann, ISBN 0 7923 9075 X Kluwer Academic Publishers

RS-232 QUICK TESTER

No PC interface has attracted more attention in the electronics press, and caused hotter debates, than the RS-232 interface. It is unfortunate but true that both hardware and software appear to be open to different interpretations when it comes to connecting RS-232 devices like printers, plotters, mice and modems. The tester described here is a handy tool to help you locate possible hardware errors, when hooking up a new RS-232 peripheral is not going as smoothly as you would have hoped.

Design by A. Rietjens

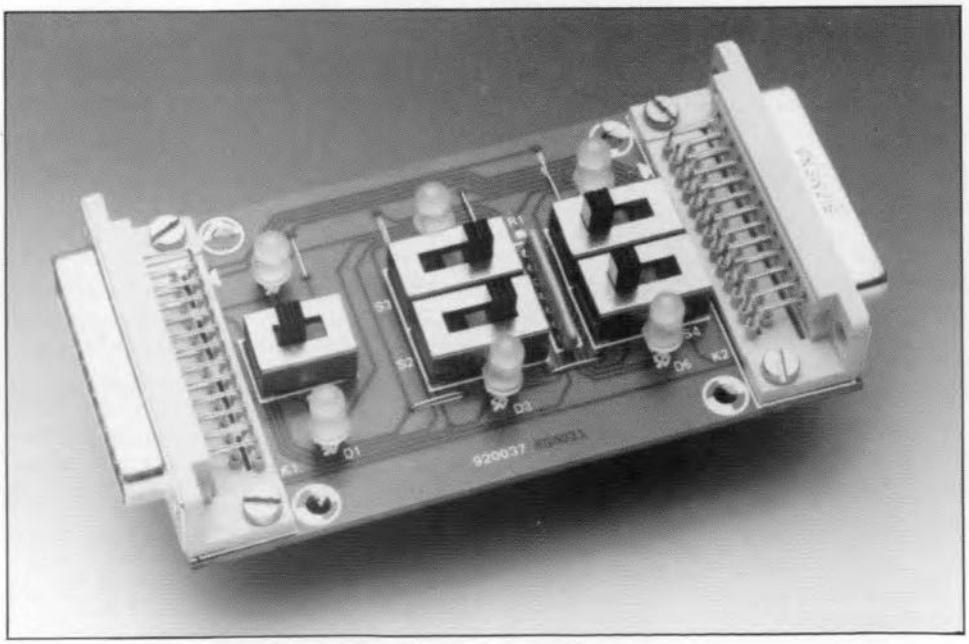
THE RS-232 interface is an old faithful in the telecommunications industry, its protocol and hardware being geared to conveying data over long distances. In its most rudimentary form, the interface could be reduced to only two lines: ground and data, which are used alternately by the transmitter and the receiver. First, data is sent from location A to location B. Next, the control software changes the direction, and location B starts to transmit to location A. This type of half-duplex communication is nearly extinct these days, when a three-wire connection appears to be the minimum. Provided software is used to deal with the handshaking function, such a three-wire link could be used, theoretically, to implement full-duplex communication. In most cases, the handshaking software is realized on the basis of the Xon/Xoff protocol. In this system, the receiver sends the Xoff code as soon as it has received the maximum amount of data it is able to handle. Transmission of the Xoff code causes the communication to be interrupted until the receiver transmits the Xon code. Communication is resumed on receipt of this code at the transmitter side of the link.

The main advantage of the Xon/Xoff protocol is that only three wires are required to set up a bidirectional data link. Also, the simple electrical connection is a boon because it prevents hardware problems. However, true full-duplex communication is not possible using the Xon/Xoff protocol.

Faster!

The fastest and most versatile version of the RS-232 interface is its complete implementation on the basis of hardware handshaking. In addition to the two data lines, the 'full' version has a number of handshaking lines (usually five) to control the data exchange between connected devices. Unfortunately, in particular the connection between transmitter and receiver has given rise to much confusion. This is mainly caused by poor understanding of the terms DTE (data terminal equipment) and DCE (data communication equipment) used in handbooks and system documentation.

A DTE is, for instance, a PC or a terminal, while a modem or a line printer is usually a DCE. By virtue of the RS-232 protocol, it is possible to interconnect not only a DTE and a DCE (the original aim), but also two DTE devices, without the need of inserting a modem. A DTE-DTE connection, however, requires some cross-links to be made in the connecting cable. Figure 1 shows the most frequently used connection options.



The RS-232 connector

Most of you will recognize the 25-way RS-232 sub-D connector found on virtually all PCs these days. The 9-way (AT-style) version, which omits some of the less important handshaking lines, is also used increasingly. The lines discussed below are available on both the 25-way and the 9-way sub-D connector — see the overview in Table 1.

As already mentioned, eight pins on the RS-232 connector are essential for a reliable data link. Pin 2 carries the TxD (transmit data) signal. This line is used by a DTE device to send data to a DCE device. Pin 3 is used for the complementary function, RxD (receive data), which carries data from the DCE device to the DTE device. Pin 4 carries the RTS (request to send) signal, which is sent by the DTE to the DCE to indicate that it is about to send a dataword. The DCE responds via pin 5, the CTS (clear to send) line. In addition, there is the DSR line (pin 6). Via this line, the DCE informs the DTE that it is 'on line' and ready for use. The DCD (data carrier detect) pin carries a signal that is used by the DCE to set up a stable data connection with another DCE. The last line is DTR (data terminal ready), via which the DTE tells the DCE that it is on, and ready to use the DCE to set up a data link. Figure 1 shows how a DTE is connected to a DCE: a pretty straightforward connection.

In practice, a communication sequence via an RS-232 link would look something like this. Initially, a PC (DTE) and a modem (DCE) are switched on. The PC actuates the DTR line, and the modem actuates the DSR line shortly afterwards. Next, the modem

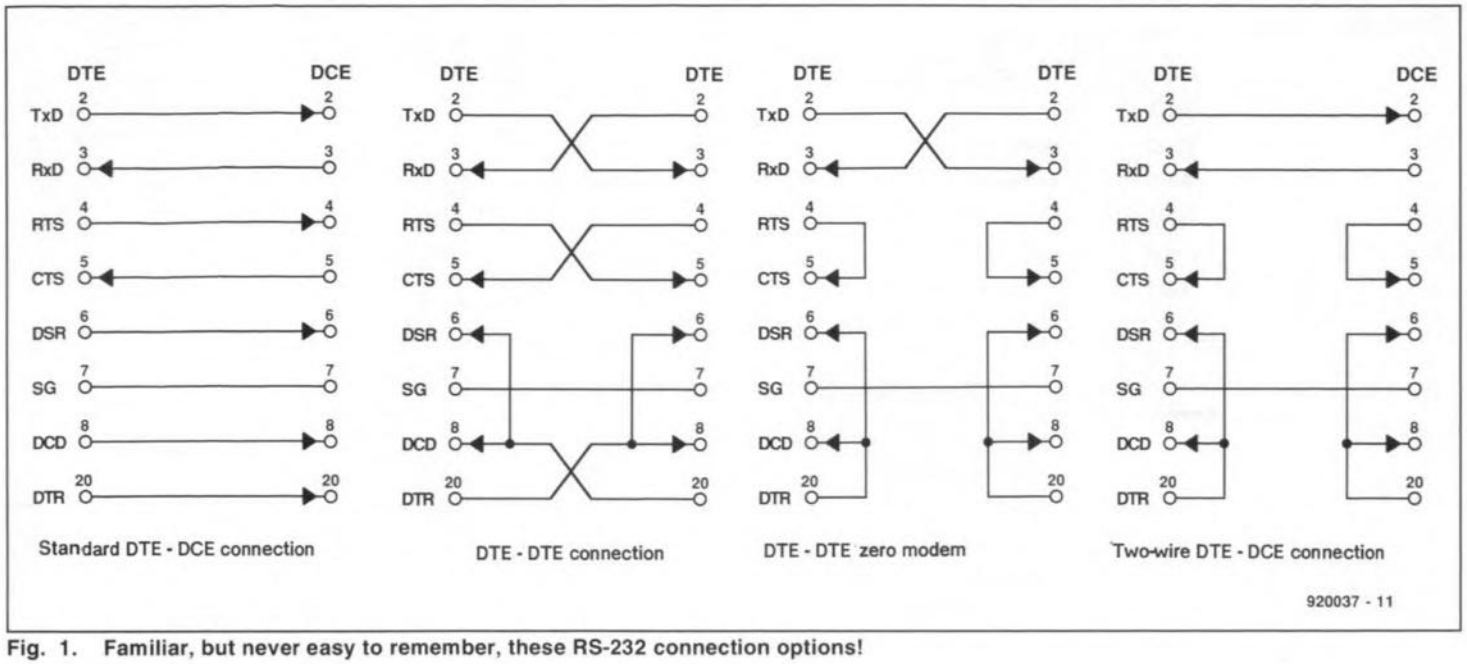


Fig. 1. Familiar, but never easy to remember, these RS-232 connection options!

sets up the link to another modem, and subsequently actuates the DCD line. This is detected by the PC, which decides that communication can be started, and actuates the RTS line in order to do so. If the modem is capable of processing the transmit command, it actuates the CTS line, whereupon the communication, i.e., data exchange, can commence. One wonders what could possibly go wrong if everything appears to be as simple as that. Well, a lot! Let us look as some possible problems.

First, there is quite some confusion about the signal levels on the RS-232 interface. According to the RS-232 standard, the control signal levels may lie between +3 V and +27 V for a logic '1', and between –3 V and –27 V for a logic '0'. This applies to control lines DTR, DSR, DCD, RTS and CTS.

The opposite applies to the data lines, RxD and TxD, which use active-low levels, i.e., a logic '0' corresponds to a level between +3 V and +27 V, while a logic '1' corresponds to a level of –3 V to –27 V. Evidently, manufacturers of equipment that uses only +5 V and ground for an RS-232 interface violate the standard by not meeting the required voltage swing (and polarity).

A second source of trouble is the connection of two DTE devices. Although there should be no problems with such a connection, cross links are required in practice on all lines except DCD.

A third problem arises when the RS-232 interface is not complete at the DTE or DCE side. In the worst case, this requires some hard thinking before a link can be set up successfully. The best known 'trick' to fool the handshaking circuits at either side of the link is the zero-modem, which simulates signals normally supplied by the 'other party' (see Fig. 1). This is also referred to as 'local echo'.

RS-232 quick tester

We all hope that there will be no problems when serial equipment is properly connected. After all, a good quality cable has been used, connectors have been secured, and matching data transfer parameters (number of data bits, stop bits, and parity) have been set at both sides after wading one's way through hefty manuals, and some cajoling with DIP switches. Alas, problems are still likely to occur. Time to get out your RS-232 tester!

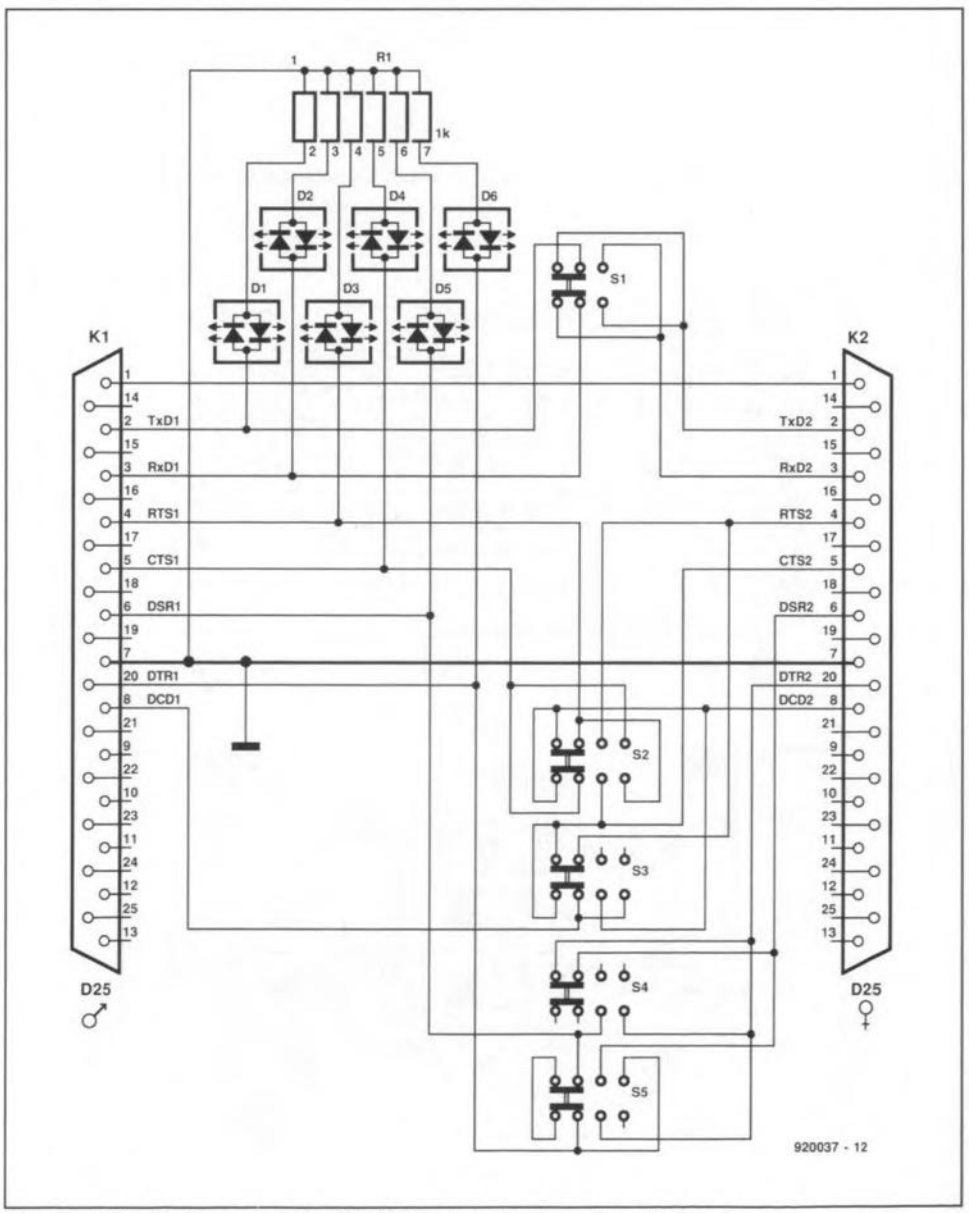


Fig. 2. Circuit diagram of the RS-232 tester: simple and uncluttered.

D-25 pin	D-9 pin	Signal	Function	DTE	DCE
1		CG	chassis ground		
2	**3**	**TxD**	**transmitted data**	**out**	**in**
3	**2**	**RxD**	**received data**	**in**	**out**
4	**7**	**RTS**	**request to send**	**out**	**in**
5	**8**	**CTS**	**clear to send**	**in**	**out**
6	**6**	**DSR**	**data set ready**	**in**	**out**
7	**5**	**SG**	**signal ground**		
8	**1**	**DCD**	**data carrier detect**	**in**	**out**
9			positive test voltage		
10			negative test voltage		
11			not assigned		
12		SDCD	secondary DCD	in	out
13		SCTS	secondary CTS	in	out
14		STxD	secondary TxD	out	in
15		TxC	transmit check (DCE)	in	out
16		SrxD	secondary RxD	in	out
17		RxC	receive clock	in	out
18			not assigned		
19		SRTS	secondary RTS	out	in
20	**4**	**DTR**	**data terminal ready**	**out**	**in**
21		SQ	signal quality detect	in	out
22	9	RI	ring indicator	in	out
23		SEL	speed selector DTE	in	out
24		TCK	speed selector DCE	out	in
25		BSY	data line busy	in	out

Table 1. RS-232 connector pinning overview. Essential signals are in bold print.

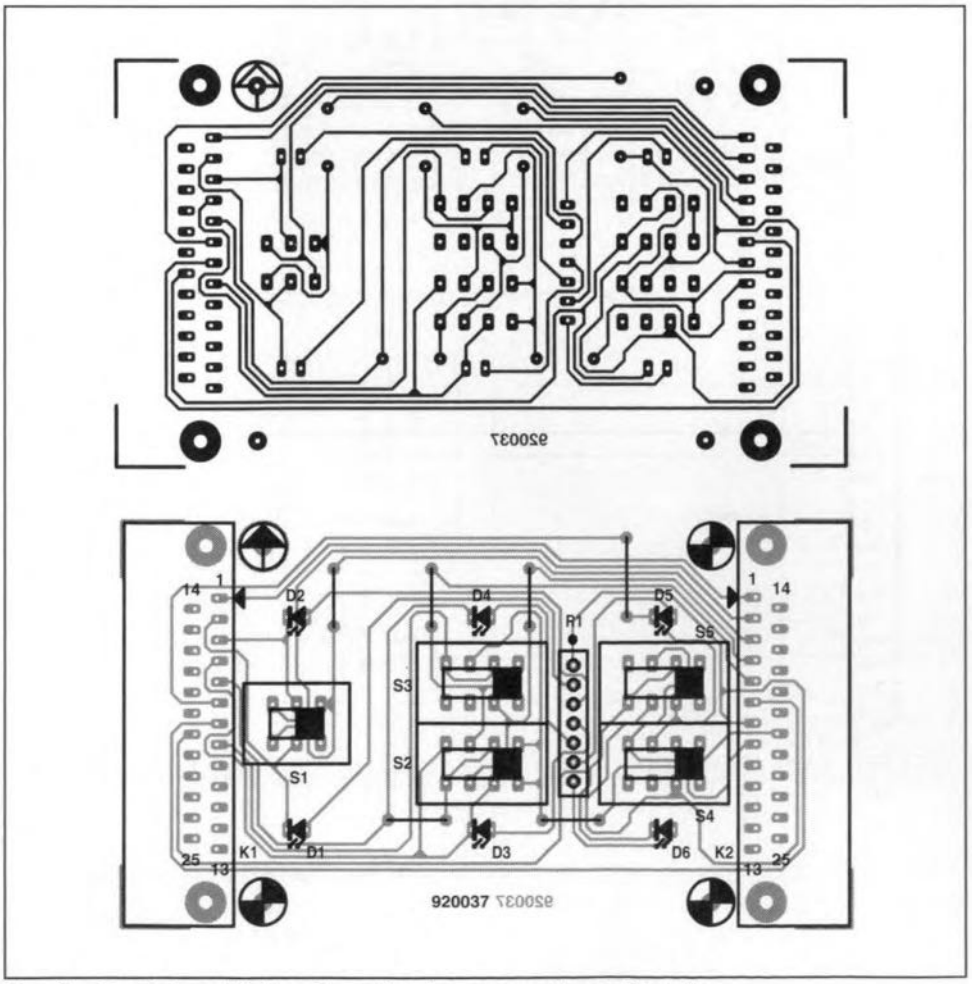


Fig. 3. Track layout (mirror image) and component mounting plan.

As shown in Fig. 2, the circuit consists merely of a number of connections, a set of switches, and six LEDs. The tester is inserted between the DTE output and the cable to the DCE, or another DTE. It should be noted that switches S_2 and S_3, and S_4 and S_5, form pairs, and must always be operated simultaneously. Two separate switches are used rather than a fourfold slide switch because the latter proved difficult to find at a reasonable price.

LED D_1 indicates the level on the TxD line, D_2 that on the RxD line, D_3 that on the RTS line, D_4 that on the CTS line, D_5 that on the DSR line, and, finally, D_6 that on the DTR line for the DCE. The LEDs are bicolour (red/green) types, which enables high and low signal levels to be easily seen. Red means a positive line voltage; green a negative line voltage.

Figure 4 shows the connections that are established when the switches are operated. If all switches are set to position 'A', all cross-links required to connect two DTEs via a standard RS-232 cable are made. So, if you want to set up an RS-232 link between two PCs, insert the tester between one of these and the cable. The LEDs will indicate how the communication is getting on.

Normally, A DTE is connected to a DCE via a standard RS-232 cable. If the switches are set to position 'B', the tester may simply be inserted in the link. Here, too, the LEDs show what is happening (or not).

Switches S_2, S_3, S_4 and S_5 also have a position 'C', which serves to set up a null-modem connection. A null-modem causes local feedback at the peripheral and the terminal. This disallows hardware control over the data exchange, and may be required either when the Xon/Xoff protocol is used, or a peripheral device is connected to a PC, or any other computer system, that does not have hardware handshaking. Examples of equipment that lacks hardware handshaking on the serial port include the 80C32 single-board computer (Ref. 1), and many types of serial A-to-D converter.

COMPONENTS LIST

Resistors:

1	6-way array 1kΩ	R1

Semiconductors:

6	bicolour LED	D1-D6

Miscellaneous:

1	2-pole 2-way slide switch (e.g., Spoerle MFP220)	S1
4	2-pole 3-way slide switch (e.g., Spoerle MFP230)	S2
1	25-way PCB-mount male sub-D connector; angled	K1
1	25-way PCB-mount female sub-D connector; angled	K2
1	Printed circuit board	920037

Construction

The design of the printed circuit board for the RS-232 quick tester is shown in Fig. 3. Start the construction by fitting the six wire links on the board, followed by the resistor array (note the orientation!) and the five switches. As already mentioned, switches S2-S5 are formed by two double-pole, 3-way slide switches, because a 4-pole switch with 3 positions proved difficult to get. The equivalent switch pair will be fine as long as you remember always to operate them together. With some dexterity, the switches may also be coupled by a small piece of plastic glued in between the levers.

Continue the construction by fitting the two connectors K1 (male) and K2 (female), followed by the LEDs, D1-D6. Note that all LEDs should be fitted with the same orientation. The flat side of a bicolour LED should be at the side of the cathode of the diode symbol printed on the overlay. Take care to ensure the correct LED orientations, or you will not be able to tell the RS-232 signal level for sure. To make it sturdy and easy to handle, the tester may be fitted into a small plastic enclosure.

The circuit is now ready for use. Set all switches to position 'A' for a DTE-DTE link, or to position 'B' for a DTE-DCE link. If you need a null-modem link, set S4 and S5 to position 'C'. A null-modem may be called for in a DTE-DTE link as well as in a DTE-DCE link. Well, at this stage proper communication via the RS-232 ports can only be disrupted by software faults, in which case Murphy's laws apply. ■

Reference:

1. 80C32/8052AH-BASIC single-board computer. *Elektor Electronics* May 1991.

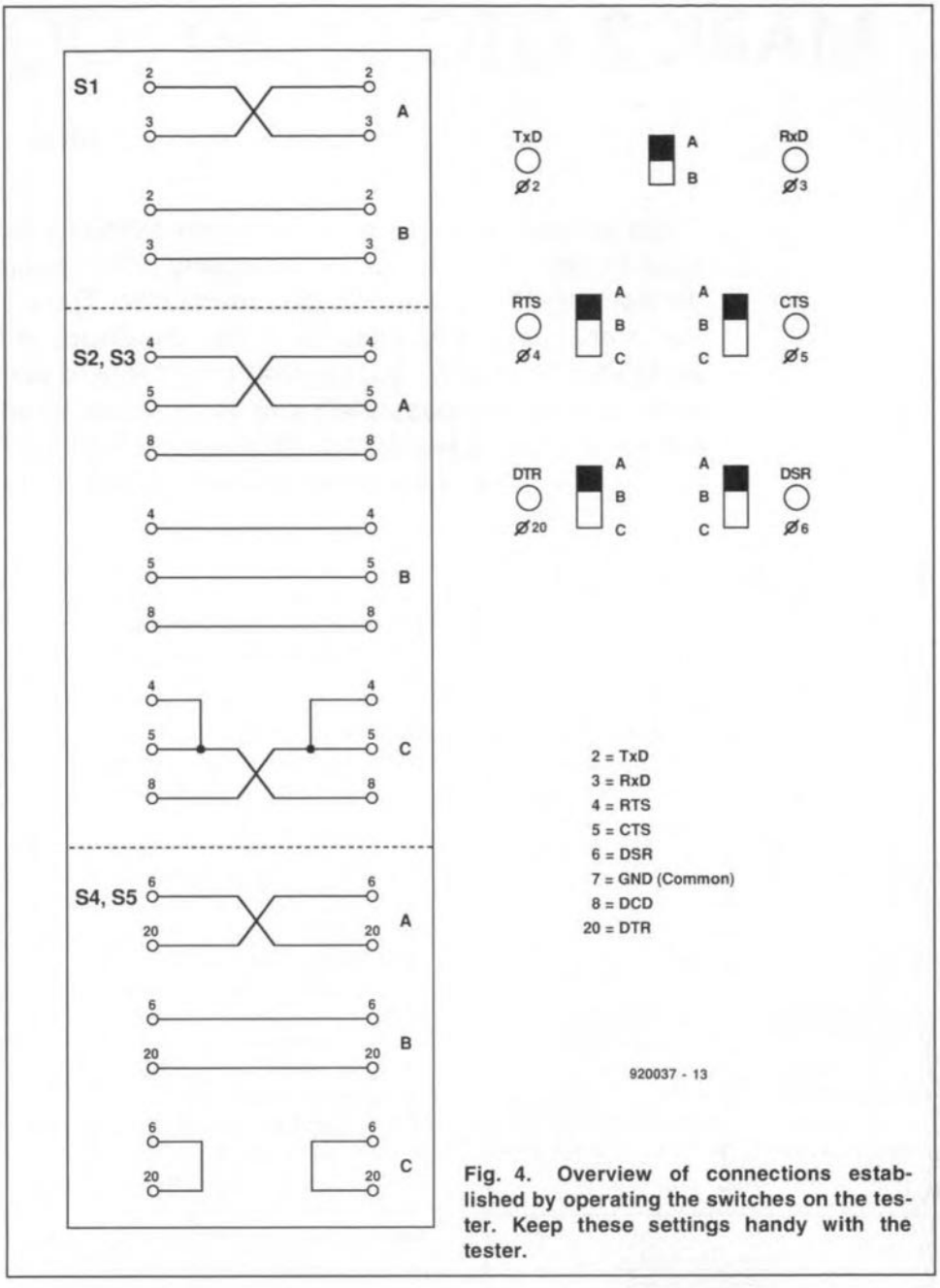
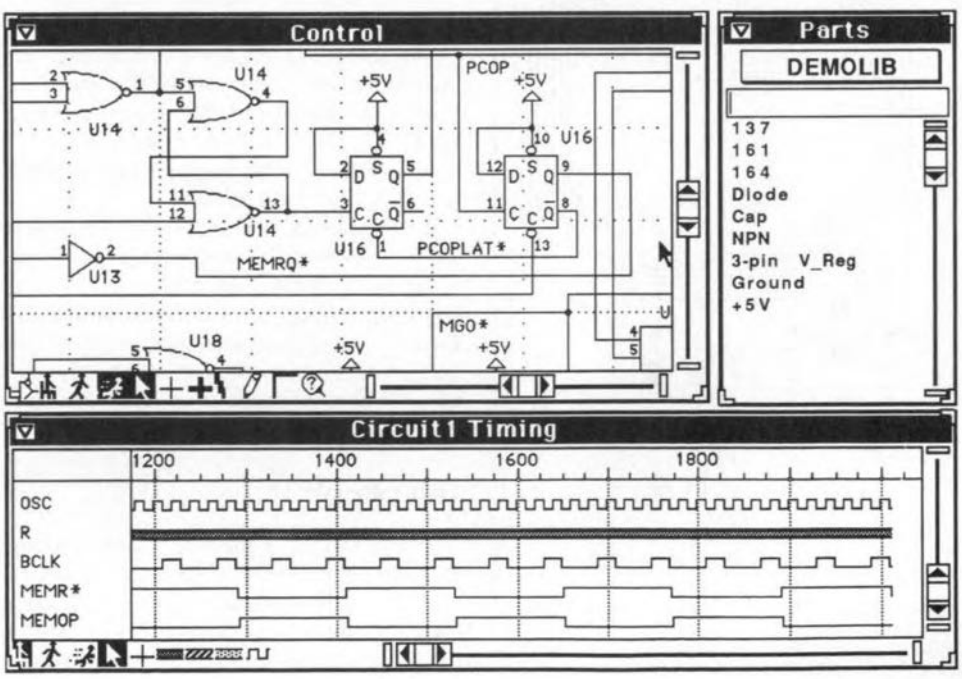


Fig. 4. Overview of connections established by operating the switches on the tester. Keep these settings handy with the tester.

NEW PRODUCTS

LogicWorks logic simulator now available for DOS.

LogicWorks has been the number-1 package for teaching digital circuit design on the Macintosh since 1985, and is now available to the wider DOS audience. LogicWorks brings circuit ideas to life on the screen with fully interactive digital simulation. Probes, displays and switches can be placed right on the circuit diagram, and operated just like a real circuit breadboard. Device delays, clock rates and signal connections can be changed with a few mouse clicks, allowing circuit ideas to be tested out in seconds. More info from **Capillano Computing Systems Ltd., Canada. Tel. (604) 522-6200, Fax (604) 522-3972.**



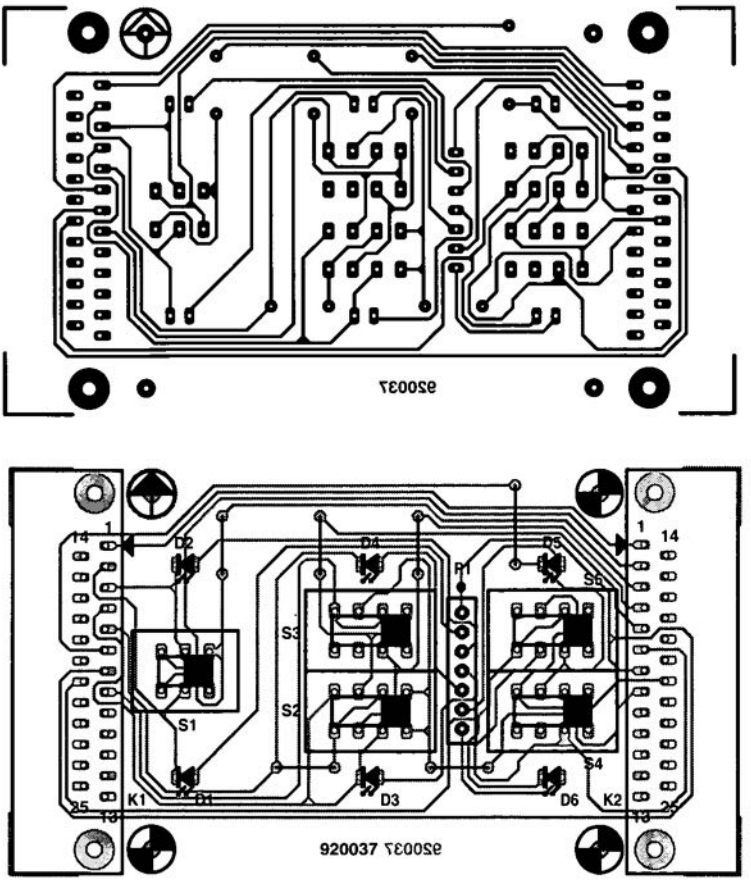


Fig. 3. Track layout (mirror image) and component mounting plan.

MARK 2 QTC 80/40 LOOP ANTENNA

by Richard Q. Marris, G2BZQ

The original experimental QTC transmitting loop antenna was built in late 1990, tested immediately, and details were published in the June 1991 issue of this magazine. The design raised a lot of interest and a number of fellow amateurs in both the UK and the USA advised the author that they were apartment dwellers (no outdoor antenna possible!) and were going to construct it. Others asked whether a two-band 80/40 metre (3.5–7.0 MHz) version was feasible. That request is answered in this article.

IN response to the comments and questions of a number of readers, particularly in the UK and the USA, a Mark 2 QTC loop antenna was constructed to cover the 80 m and the 40 m bands. A similar octagonal configuration as for the original was used, but the tuning/coupling impedance matching circuits were redesigned for two-band operation after a number of experiments and tests. The result is even simpler than the original.

The original QTC loop was a 30 in. (75 cm) diameter octagonal spiral loop, of novel design, whose general circuit and configuration is shown again in Fig. 1. The loop was designed for indoor use, set up on a table alongside an 80-m low-power CW transmitter. It was intended as a possible answer for those amateur transmitting enthusiasts who, for one reason or another, cannot erect an outdoor antenna.

Theoretically, a small, indoor loop using a maximum of 10 W RF power cannot be expected to produce a signal comparable with the conventional 100 W transmitter/outdoor dipole set-up. However, in practice, it occasionally does; we think for the following reasons.

1. The QTC loop being directional, and comparatively narrow-band, reduces incoming interference (and outgoing, such as TVI!).
2. Being 'on hand' alongside the operator, the QTC loop can be peak resonated for absolute maximum performance and directivity on the spot frequency being used.
3. Some outdoor dipoles (and other types) are erected to textbook dimensions, with little or no regard being paid to the height and surrounding objects, resulting in an off-tune compromise, which, when fed with, say, 100 watts, produces results that are accepted without the realization that these could be greatly improved if the antennas were tuned to optimum frequency at optimum height. To which should be added the antenna compass alignment, and the type, length and condition of the coaxial feedline, and so on. The overall result is that the original 100 W signal is largely dissipated or attenuated in the system.

Reason 3. became apparent during various contacts with continental European stations when using the QTC Loop, and later the Mk. 2 QTC Loop, and discreet questions were asked about the height, length and surrounds of their antennas.

Nevertheless, it must be stressed that in most cases the QTC loop signal was somewhat down on the outdoor dipole/transmitter set-up. It was, however, quite adequate for 2-way communication, which must be considered satisfactory when an enthusiast is lumbered with a 'no outdoor antenna' situation, for whatever reason.

The circuit

The original QTC Loop was intended for operation on the 80-m (3.5 MHz) amateur band. The circuit and general layout are given in Fig. 1. A spiral $5\ ^1/_8$ turns loop, L_1, and inductance L_2 were resonated to frequency by bandset and bandspread variable capacitors C_1–C_2. There was also an optional tuning meter.

The Mark Two QTC 80/40 Loop uses an identical spoke framework—see Fig. 2. The total number of turns of L_1 is five for 80 metres and an optional tap for 40 metres. It is resonated by C_1–C_2, which is a good-quality receiving type two-gang variable capacitor (2×125 pf) with the built-in padders removed. Coupling to the transmitter (and receiver) is by C_3 (300 pF ceramic variable) to 48 in (120 cm) of RG58 coaxial feedline. The original tuning meter—see Fig. 1—can be used with advantage.

Construction

The construction is shown in Fig. 3. It consists of an eight-spoke octagonal frame, a vertical member, and a heavy base to prevent it tipping over. On to this is fixed the sim-

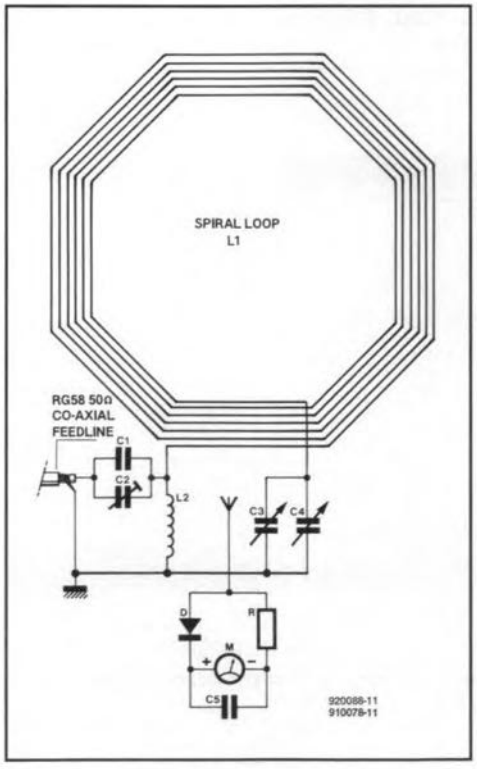


Fig. 1. The original QTC Loop.

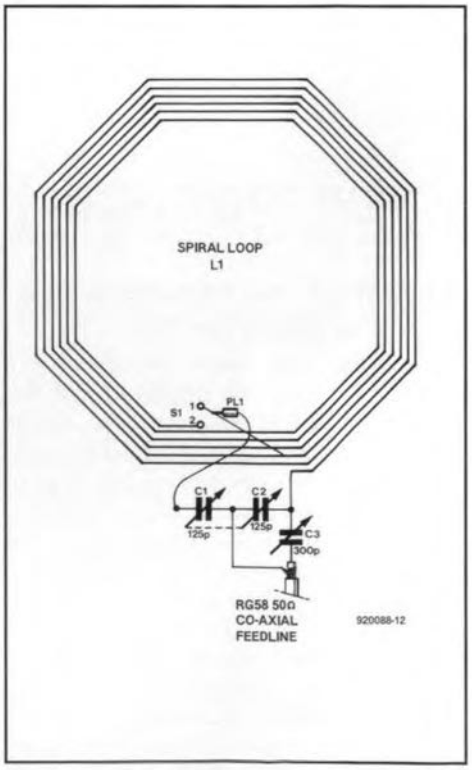


Fig. 2. The QTC Mark 2 circuit.

ple resonating/loading unit, which is constructed on a standard 9"×4" (23×10 cm) fibre-glass board, copper-clad on one side. Ideally, this should be replaced by a suitable box. However, as it was anticipated that the loop would be used as a test bed for future experiments, a board was used as this can be re-used, or quickly replaced, at little cost—see Fig. 3 and Fig. 4.

The loop frame consists of eight spokes made from four lengths of moulded hardwood, each 30 in. long, $^5/_8$ in. wide and $^1/_4$ in. thick (760×16×6 mm). A 2BA (5 mm dia) clearance hole is drilled in the centre of each spoke. The spokes are then glued and clamped together with a long 2BA (5 mm dia) bolt, nut and washers. The spokes must overlap in the order shown in Fig. 3 and evenly spaced apart. The assembly should then be allowed to dry out thoroughly, after which it is given a coat of polyurethane varnish. A six-way, 2 A polythene terminal block (cut from a standard 12-way block) is screwed to the end of each spoke to provide the necessary securing, spacing and insulation of the wire turns.

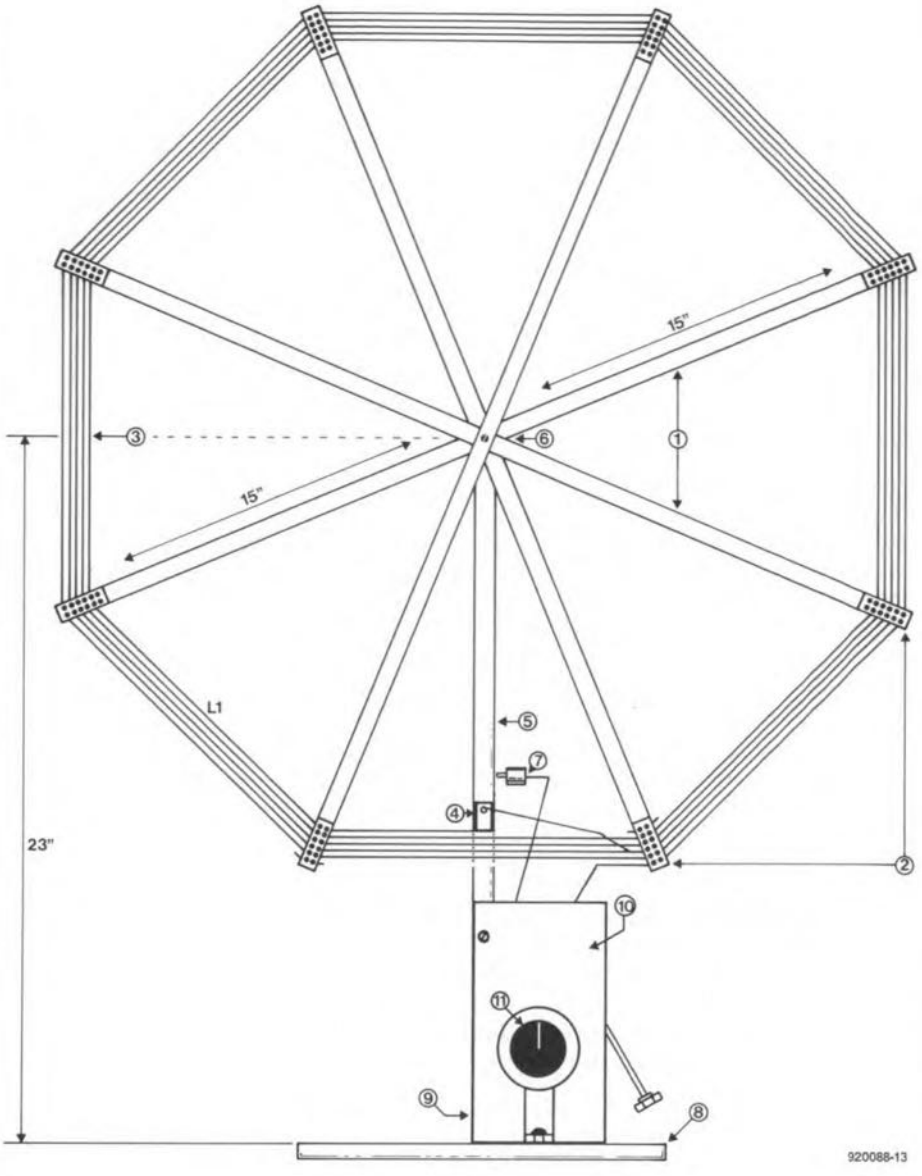
A 23×0.8×0.8 in (585×20×20 mm)vertical wooden support is glued, screwed and bracketed to a suitable 12×8×0.5 in (300×200×12 mm) wooden base, the whole being teak-wood stained. The loop frame is then glued and bolted to the top of the vertical support as shown.

The loop winding, L_1, uses PVC covered 7/0.2 mm wire with an outside diameter of 1.2 mm and rated at 1 kV, 1.5 A. After loosening the grub screws in the terminal blocks, thread the wire through, turn by turn, for five turns, starting at the outer hole of the bottom right-hand spoke, threading through all the blocks in an anti-clockwise direction, and terminating at the inner hole of the bottom left-hand spoke. Tighten the grub screws while going along just enough to hold the wire in place, and firmly when all the wire is threaded through and pulled tight. Leave long wire tails at both ends: these can be cut back and soldered later—see Fig. 3.

Next, secure the fibre-glass board to the wooden upright—see Fig. 3 and Fig. 4. Positioning the capacitors depends on their actual size and shape, but should be more or less as shown in Fig. 4. Capacitor C_1–C_2 must be fastened to the panel as shown and fitted with an extension shaft, with front support bracket and panel bush as shown in Fig. 4, with a wooden support platform, cut to size, to support the bracket.

Capacitor C_3 is mounted at an angle and fitted with an *insulated* extension shaft as shown in Fig. 3 and Fig. 4. *It must be completely insulated from the copper-clad fibre-glass panel.* Also, it should be fitted such that the knob is well away from the loop winding. This capacitor requires setting in only one position for 80 m (3.5 MHz) and 40 m (7.0 MHz) and may, therefore, be considered preset.

A two-way polythene terminal block is screwed to the vertical support just inboard of the bottom inner end of L_1—see Fig. 3. This is to give the 40 m (7.0 MHz) facility later.



1. 4 lengths of moulded hardwood 30×$^5/_8$×$^1/_4$ in. (760×16×6 mm). Varnished. 2BA (5 mm dia.) holes drilled in the centre of each length. Then glued and bolted together, spaced evenly, as shown.
2. 8 off 6-way, 2-amp polythene terminal blocks used as insulated wire spacers.
3. 5 turns PVC stranded 7/.02 mm wire; o/d = 1.2 mm; rating 1 kV, 1.5 A.
4. 2-way, 2-amp polythene terminal block
5. Vertical wood support 23×0.8×0.8 in. (585×20×20 mm). Wood stain.
6. 2 in×2BA (50 mm × 5 mm dia) bolt.
7. Fly lead (for 7 MHz tap) fitted 2 mm plug.
8. Wooden base 12×8×$^1/_2$ in. (300×200×12 mm). Wood stain.
9. $2^1/_2$ in (6 cm) bracket behind vertical wood support.
10. 9×4 in. (23×10 cm) single-side copper-clad fibre glass board.
11. Knob for C_1+C_2.
12. Knob, shaft coupler and shaft (insulated) for remote control of C_3.

Fig. 3. Construction of the Mark 2 QTC Loop.

The outer end of L_1 must be cut back and soldered to the junction of C_2 and C_3 as shown in Fig. 3. The inner end of L_1 is cut back and inserted into the bottom connection on the terminal block—see Fig. 2 and Fig. 3. Solder a flexible plug lead, cut to length, to the stator of C_1. A 2 mm plug is a snug fit in the block terminal insert.

Selecting of the 40 m (7 MHz) tap is discussed in 'Testing and operation' later.

All other behind-the-panel wiring must be in 16 SWG tinned copper wire, with the copper cladding of the board used for the 'earth' connections—see Fig. 4.

Fit a large 3 in. dia (75 mm) control knob to C_1–C_2.

Secure a 48 in (1.20 m) length of RG58 coaxial feedline with cleats to the wooden base.

Testing and operation

1. **80-metre (3.5 MHz) band**
   Initial tests must be made with a receiver. Rotate the resonating control, C_1–C_2, to ensure that it covers the 3500–3800 kHz (3500–4000 kHz in the USA) band. Then rotate C_3 for maximum signal in the centre of the band.
   Feed a small amount of RF to the loop and re-adjust C_1–C_2 to resonate at the exact transmit frequency. Capacitor C_3 may also require a small re-adjustment for maximum loading (or lowest SWR if a SWR meter is available). Check the loop radiation with a nearby field strength meter (the tuning meter used on the original QTC Loop is ideal). It should now be possible to fully load the loop. Capacitor C_3 should not require any further adjustment over the band.
   Check the directional properties by tuning the receiver to a signal and rotating the loop for maximum signal—this is also the position for maximum radiation to the desired station.

2. **40-metre (7 MHz) band**
   The approximate position of the 40-m 'tap' on L_1 is shown in Fig. 2 and Fig. 3. The exact position must be selected carefully so that C_1–C_2 are enmeshed about 15% at 3800 kHz. The tap is made with a flexible lead.
   To avoid mutilating the PVC wire covering on L_1 when seeking the correct 'tap' position, take a lead from the top insert on the two-way terminal block. Solder a thin sewing needle at the other end.
   With the receiver tuned to about the centre of the 40-m band, insert the 2 mm plug into the two-way terminal block at the top and push the needle through the PVC wire cover in the position shown in Fig. 2 and Fig. 3. Resonance should be obtained at 3800 kHz with C_1–C_2 enmeshed about 15% and C_3 peaked for maximum signal. If necessary, move the 'needle' tap slightly to the left or right as required. The tapping point will vary between loop models, depending on the construction. Once the tap point has been found, the PVC can be removed, and the lead end soldered on in place of the needle. It will be found that any tiny needle holes will not show if the wire is squeezed between finger and thumb.
   The transmitter can now be resonated/loaded to the loop as in the 80-m band.

3. **Other bands**
   There seems to be no obvious reason why a further tap cannot be added for another band, such as the 20 m (14 MHz) band using a similar technique to the one described. A slow motion drive could be added between the knob and C_1–C_2. The loop would probably be less directional on the higher frequencies.

Safety

The QTC 80/40 Loop is designed for use with *low* transmitter power. The prototype has been operated with up to 10 watts CW. It has been tested up to 20 watts, but any higher powers would necessitate higher voltage variable capacitors and thicker wire for L_1.

In the interest of domestic household safety, *10 watts should not be exceeded*. There will be no prizes for the operator for setting fire to the curtains or giving the kids a nasty RF shock, or scaring the living daylights out of the cat.

Reference

'The QTC loop antenna', *Elektor Electronics*, June 1991, p. 40.

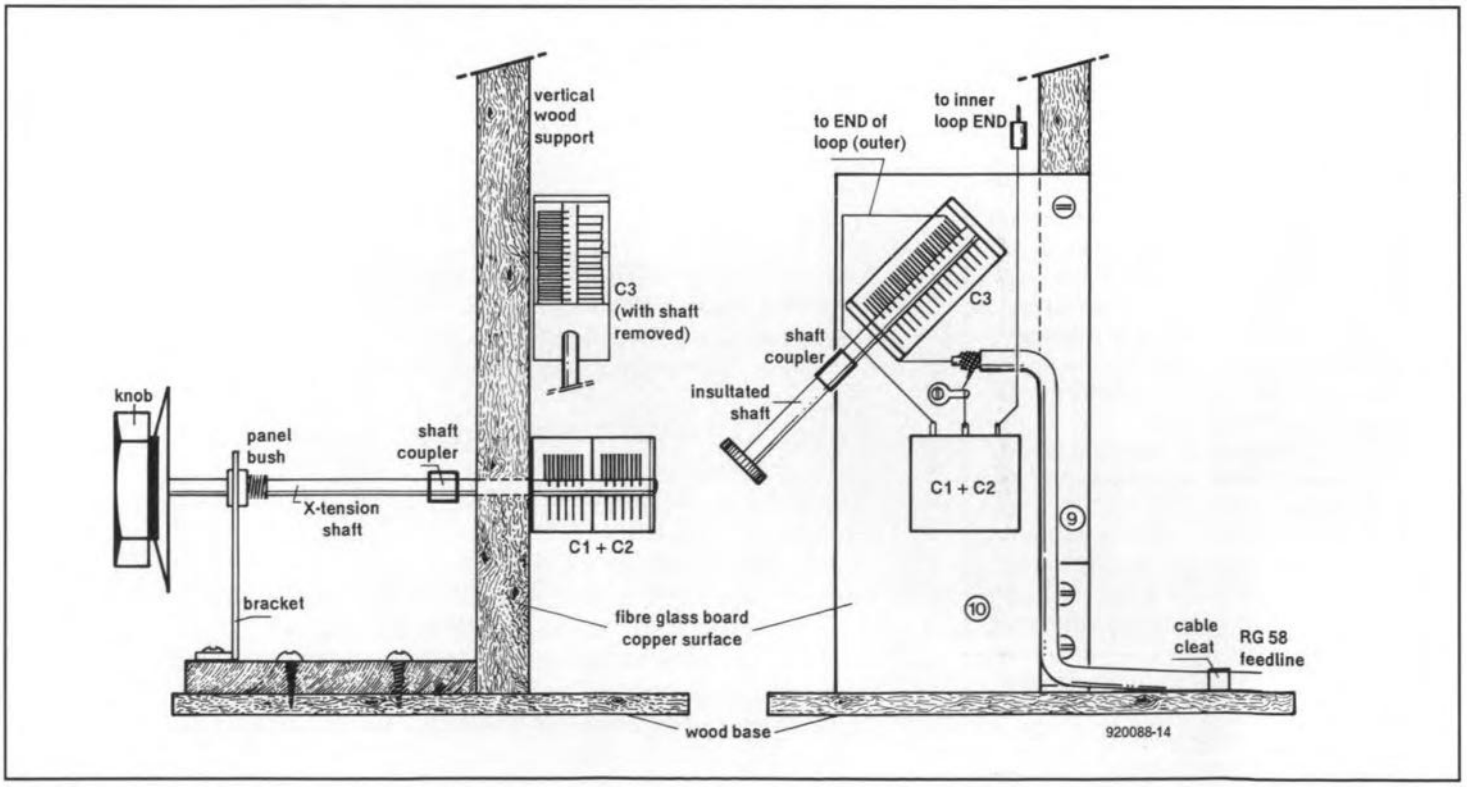


Fig. 4. Panel details.

Mains (power line) voltages are not listed in the articles. It is assumed that our readers know what voltage is standard in their part of the world.

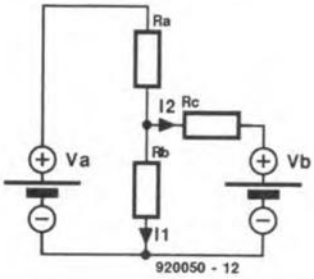
Readers in countries that use 60 Hz supplies, should note that our circuits are usually designed for 50 Hz. This will not normally cause problems, although if the mains frequency is used for synchronization, some modification may be required.

The international letter symbol '*U*' is used for voltage instead of the ambiguous '*V*'. The letter V is reserved for 'volts'.

CORRECTIONS

Plant warmer (June 1992)

Resistor R_c was omitted from Fig. 2. The correct diagram is shown below.



Inductance-capacitance meter (March 1992)

The value of R_{16} and R_{17} should be 39 Ω, not 30 Ω as shown in the parts list.

8751 Emulator (March 1992)

The features list in the first column on page 53 should read:

- download, modify, and upload 8751 programs without having to erase and program an 8751.
- put breakpoints in programs.
- display register and memory contents.
- ...

  etc.

FM tuner – Part 3 (May 1992)

In the PSU parts list on page 54, R_{301} should be 150 Ω, 1%, not 150 kΩ, 1%.

Video enhancer (July 1992)

Preset P_2 is best adjusted for a signal level of 2 V_{pp} at the collector of T_2. Output transistor T_3 may run fairly hot: this is normal.

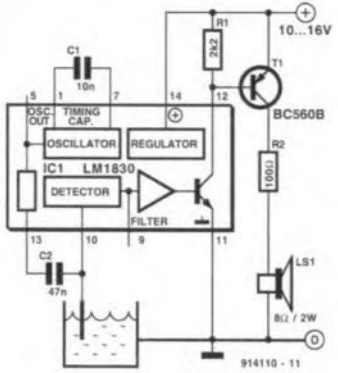
The third paragraph of the text on page 73 should read: The frequency characteristic of the signal at the base of T_3 is shaped by P_1, R_6 and C_8, and is, therefore, to a certain extent under the control of the user (with P_1).

Mark 2 QTC 80/40 loop antenna (July 1992)

The frequency '3800 kHz' mentioned twice under **2. 40-metre band** (page 90) should have read '7300 kHz'.

Audible fluid level indicator (July 1992)

Owing to a printing error, the diagram in this article is incorrect. The right diagram is shown below.



FM TUNER

PART 5 (FINAL PART): S-METER, WIRING, CONSTRUCTION, COMPONENT SUPPLIER INFORMATION

By H. Reelsen

The last printed circuit board to be discussed is the LED-based S-meter (signal strength) unit, which is fitted on to the front panel of the tuner enclosure.

The S-meter is a simple circuit (Fig. 16) based on the familiar LM3914 LED bar driver IC from National Semiconductor. This IC allows LEDs to be connected direct, i.e., without the usual external current limiting resistors. Here, the LM3914 is used in 'bar' mode, which allows rectangular face LEDs to be used to mimic a continuous horizontal scale. The driver is powered from the 5-V supply line in the tuner. The bar indication is a good alternative to a moving-coil meter because the input voltage range starts at 0 V (in spite of the single power supply), and the circuit is simple to adapt to the required full-scale voltage level. The full-scale indication is determined by a voltage reference source that outputs 1.25 V between pins 7 (REFOUT) and 8 (REFADJ). The resistor connected between these two pins has two functions. Firstly, it determines the current through the LEDs driven, according to

$$I_{LED} = 12.5\ V/R1.$$

The indicated value of 1.2 kΩ results in a LED current of about 10 mA.

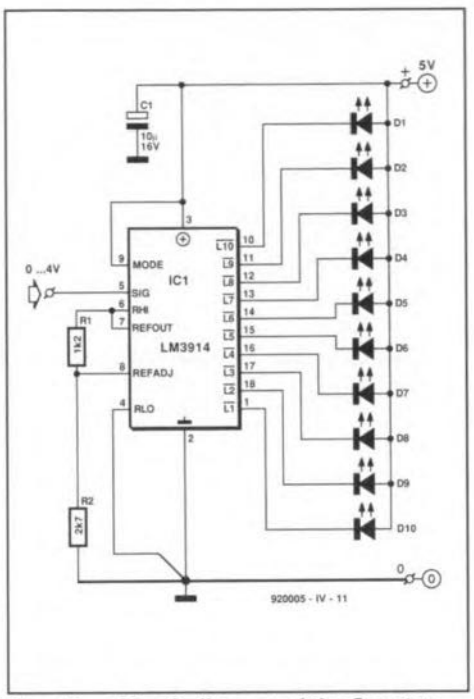


Fig. 16. Circuit diagram of the S-meter.

Secondly, the combination of R1 and R2 determines the full-scale input voltage level, U_{max}:

$$U_{max} = 1.25\ V \times (R1/R2 + 1) = U_{RHI}$$

The voltage at RHI (pin 6) determines the end-of-scale value, while that at RLO determines the start of the scale. The resistor values used here result in a scale range of 0 to 4 V.

The supply voltage of the LED driver is not limited to 5 V only. In fact, you may use any supply voltage between 3 V and 12 V, as

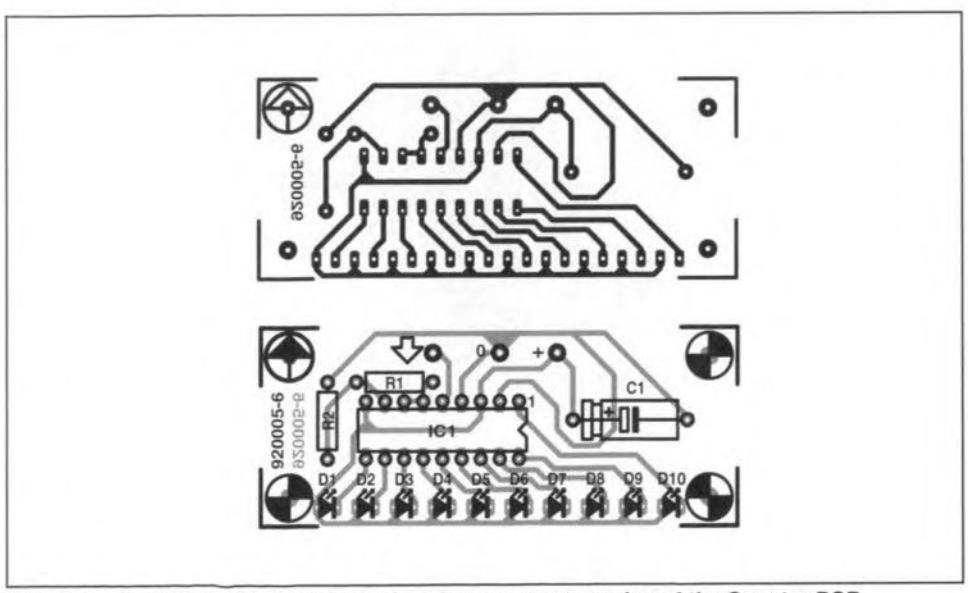


Fig. 17. Track layout (mirror image) and component overlay of the S-meter PCB.

COMPONENTS LIST

Resistors:

1	1kΩ2	R1
1	2kΩ7	R2

Capacitors:

1	10µF 16V	C1

Semiconductors:

10	LED, green, rectangular	D1-D10
1	LM3914	IC1

Miscellaneous:

1	Printed circuit board	920005-6

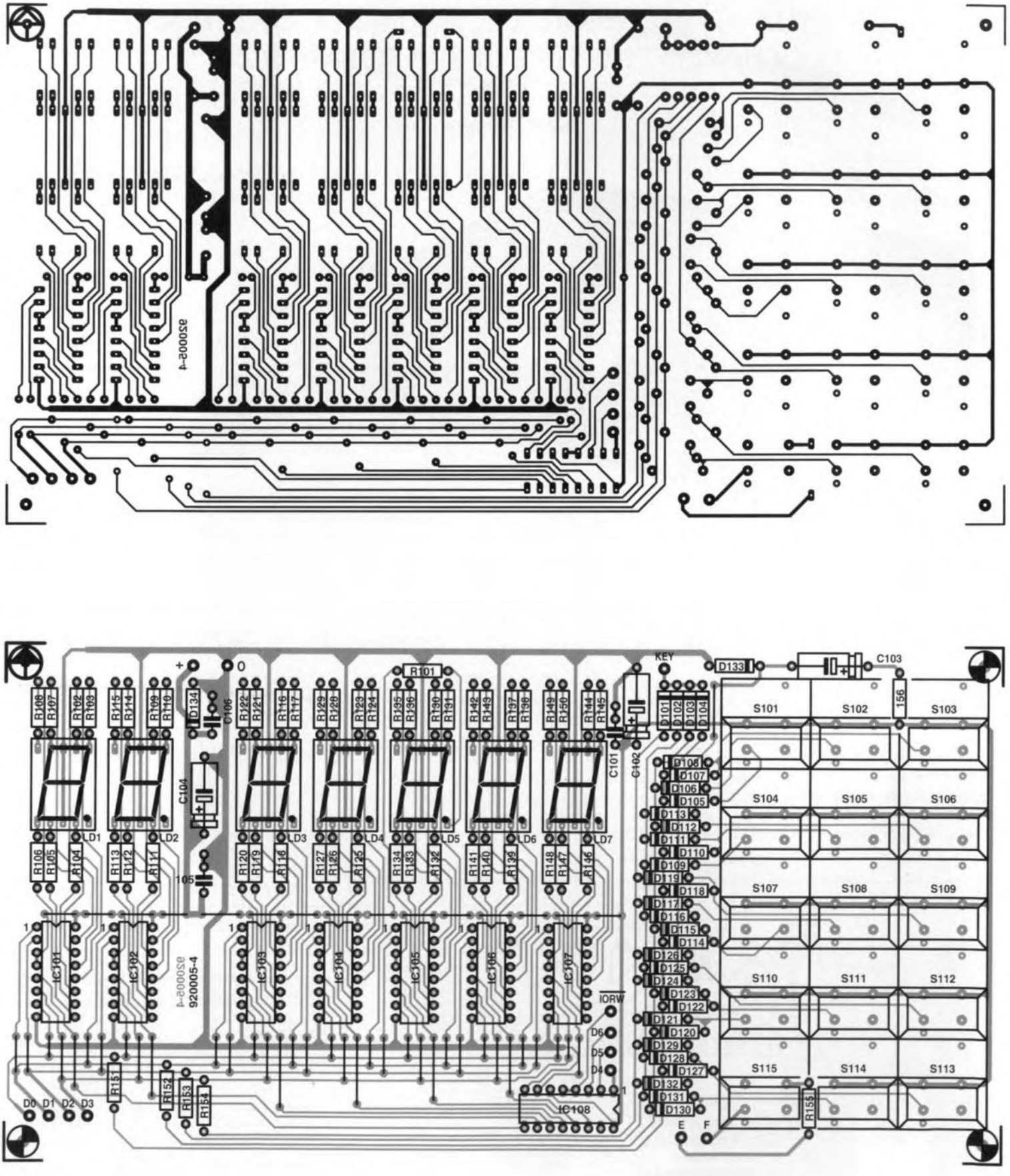


Fig. 18. Track layout (mirror image) and component mounting plan of the keyboard/display PCB.

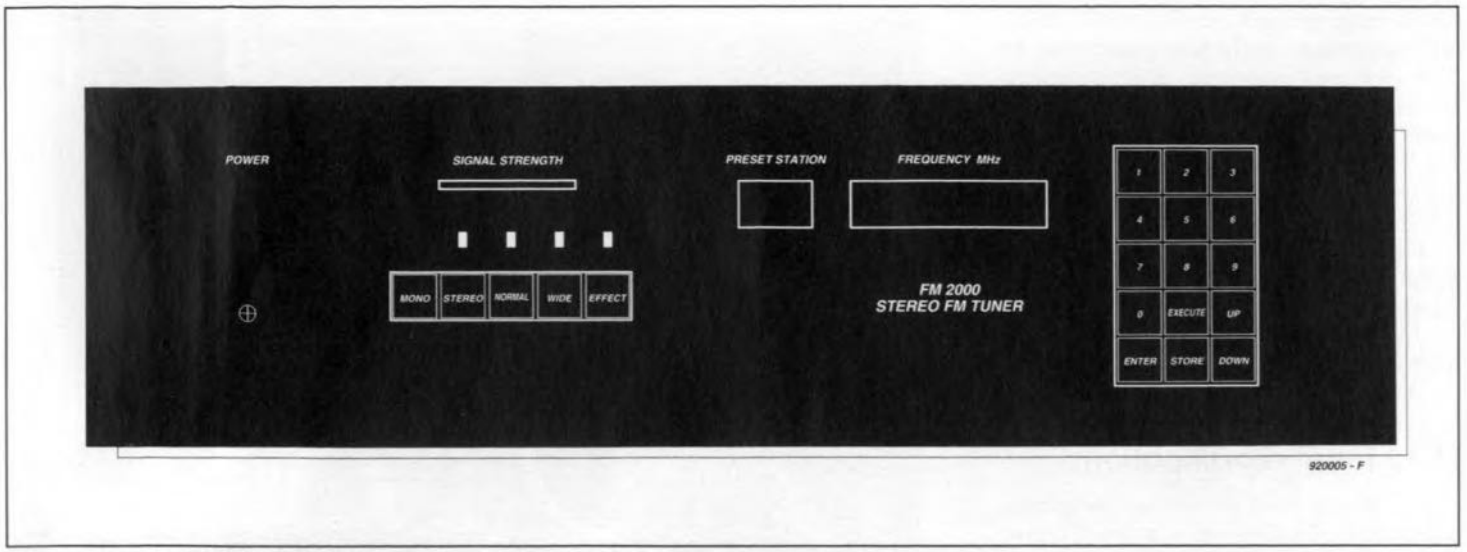


Fig. 19. Front panel layout (shown at approx. 36% of true size).

COMPONENTS LIST

Resistors:

1	680Ω	R101
49	330Ω	R102-R150
5	1kΩ	R151-R155
1	390Ω	R156

Capacitors:

1	220nF	C101
1	22µF 16V	C102
1	100µF 16V	C103
1	22µF 25V	C104
2	100nF	C105;C106

Semiconductors:

33	1N4148	D101-D133
1	1N4001	D134
7	74HC4511	IC101-IC107
1	74HC138	IC108
7	DP352PK (red, common cathode) (Telefunken Electronic)	LD1-LD7

Miscellaneous:

15	Digitast key with wide (17mm) cap	S101-S115
1	Printed circuit board	920005-4
1	Front panel foil	920005-F

long as the input voltage does not exceed the supply voltage.

The signal strength indicator is built on the small printed circuit board shown in Fig. 17. It effectively replaces the moving-coil S-meter shown in the circuit diagram of the main tuner board.

Keyboard PCB

Figure 18 shows the printed circuit board for the keyboard/display unit of which the circuit description was given in last month's article. On this PCB is a 100-nF decoupling capacitor, C106, not indicated in the circuit diagram (Fig. 14). It is connected in parallel with D134.

The functions of the keys are apparent from the front panel foil layout given in Fig. 19. This self-adhesive foil is available

COMPONENT SUPPLIER INFORMATION

FD12 tuner module:
Restek Electronic Products GmbH
Industriegebiet
Richard-Roosen-Strasse 15
3500 Kassel-Waldau
GERMANY.
Telephone: +49 561 585001.
Fax: +49 561 581664.

TQF-2599 quartz filter:
Toyocom
(Toyo Communications Equipment)
Onarimon-Daiichi Bldg.
20-4 Nishi-Shimbashi 3-chome
Minato-ku
Tokyo 105
JAPAN.
Telephone: +81 334 361 431.
Fax: +81 334 338 526.

Toyocom Europe GmbH
Bollenhöhe 5
D-4020 Mettmann
GERMANY.
Telephone: +49 2104 12099
Fax: +49 2104 15546

Viertron b.v.
Zuideinde 2
2991 LK Barendrecht
HOLLAND.
Telephone: +31 1806 18355.
Fax: +31 1806 19967.

F-G Electronics GmbH
Dipl. Ing. F. Grigelat
Mühlweg 32-33
D-8501 Rückersdorf (nh. v. Nürnberg)
GERMANY.
Telephone: +49 911 570101.
Fax: +49 911 570100 or 576000.
Contact: Mr. Borgers.

FM tuner kits:
Elektronikladen
Giessler und Danne Bauteile Vertriebs GmbH
Hammerstrasse 157
4400 Münster
GERMANY.
Telephone: +49 251 795125.
Fax: +49 251 74301.

214KCS-10115X inductor:
Contact your national Toko distributor (equivalent types may be supplied).

Componex
Vogelsanger Weg 80
4000 Düsseldorf 30
GERMANY.
Telephone: +49 211 626291.
Fax: +49 211 626295.

Cirkit Distribution Ltd.
Park Lane
Broxbourne
Herts EN10 7NQ.
ENGLAND.
Telephone: (0992) 441306.
Fax: (0992) 464457.

Bonex
12 Elder Way
Langley Business Park
Slough
Berkshire SL3 6EP.
ENGLAND.
Telephone: (0753) 49502.
Fax: (0753) 43812.

Integrated circuits TDA series:
C-I Electronics
P.O. Box 22089
6360 AB Nuth
HOLLAND.
Fax: +31 45 241877.

ready-made through our Readers Services, and fits perfectly on the front panel of the 19-inch rack enclosure used to house the receiver. It should be noted, however, that the order of the function keys as indicated in Fig. 19 should be corrected to (left to right):

NORMAL WIDE EFFECT STEREO MONO

Enure this order by cutting out the rectangular, lettered, pieces from the foil, and sticking them on to the right keycaps.

The LEDs indicate the following functions (left to right):

WIDE EFFECT MUTE STEREO

FD12 tuner modifications

Those of you keen on taking the performance of the FM receiver to an even higher level may be interested to know how the noise figure of the FD12 tuner module can be lowered. Well, this may be achieved by replacing the BF900 dual-gate MOSFET in the RF input amplifier by a later, improved, type, the BF982.

To gain access to the BF900, remove both covers of the tuner module. Locate the transistor (Figs. 20 and 21), and remove it from the board, noting its orientation. The BF982 is pin compatible, and can take the place of the BF900 without any modification to the circuit. Make sure to treat the BF982 with care: like the BF900, it is a static sensitive device, which requires the soldering iron tip to be grounded. That completes the low-noise modification. Fit the covers again.

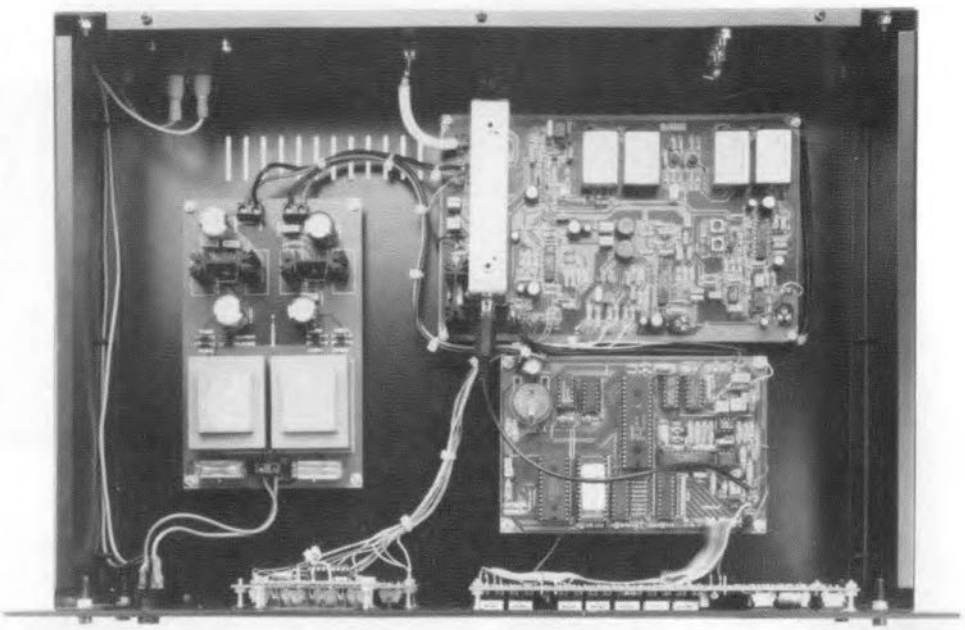
Conversely, it may happen that the tuner has to cope with very high signal levels, for instance, from a radio/TV cable network in which amplifiers are used to boost certain FM band signals. High signal levels may cause intermodulation, and require a separate, attenuated, receiver input, which has to be provided on the rear panel of the enclosure. Use any suitable RF input socket, and solder a 82-Ω resistor between the centre pin and ground. Next, connect a 1-kΩ resistor between the centre pin of the coax socket and the signal wire in the coax cable to the terminal marked 'Ant.' on the main tuner board.

Case and front panel

The photographs in last month's instalment give a good impression of the internal construction of the FM tuner. The rear panel of the 19-inch case contains the two audio output sockets (RCA or 'phono' style), the **isolated** RF input socket, and the mains appliance socket. The latter may, of course, be substituted by a fixed mains cord with a feed-through grommet and a strain relief clamp at the inside of the enclosure. In any case, the metal enclosure must be connected to the protective earth terminal (E) on the mains socket.

The main tuner board, the synthesizer board and the power supply board are mounted on 10 to 15 mm high PCB pillars secured to the bottom plate of the enclosure.

The other three boards (mode control; S-meter; keyboard/display) are fitted at the in-



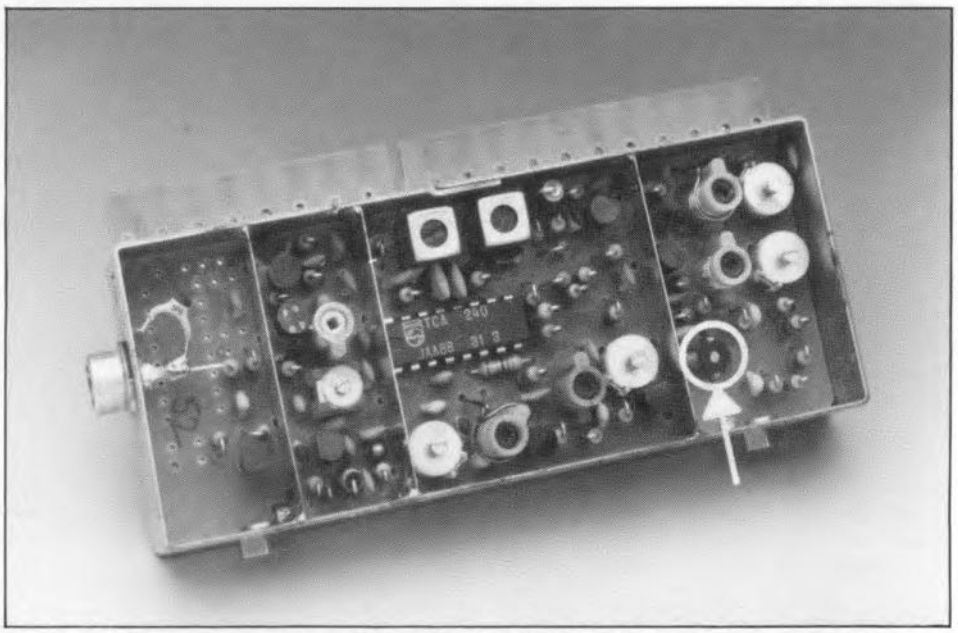


Fig. 20. Showing the position of the BF900 DG MOSFET in the FD-12 tuner module.

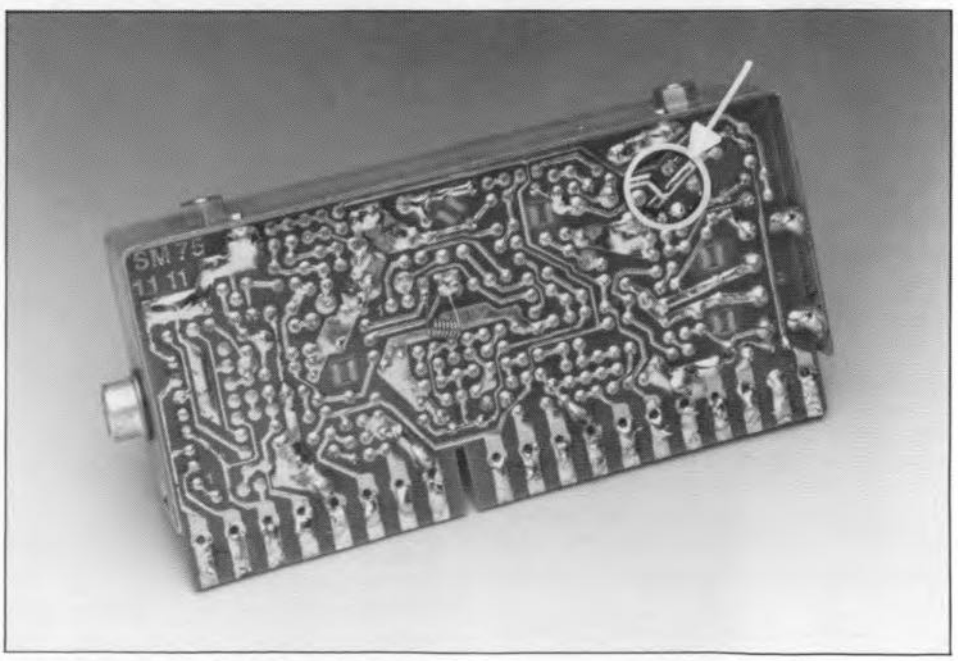


Fig. 21. Solder side view of the FD-12 tuner PCB.

Table 1. Wiring overview

Power supply board		
0 (K3)	↔	Main tuner board GND
+32V (K3)	↔	Main tuner board +33V
0 (K2)	↔	Synthesizer board 0 (near C414)
+5V (K2)	↔	Synthesizer board + (near C414)
+5V (K2)	↔	Mode control board +5V
+5V (K2)	↔	Display board +5V
Main tuner board		
+33V	↔	main tuner board + (near D2)
+33V	↔	Synthesizer board ++ (near R415)
UABST	↔	Synthesizer board TUNE (near R406)*
M1 –	↔	Display board 0
M1 +	↔	Display board INPUT (arrow 'in')
GND	↔	Mode control board 0
+15V (+C67)	↔	Mode control board +15V
BASIS B LED	↔	Mode control board A
P-STEREO	↔	Mode control board B
MUTE LED	↔	Mode control board C
STEREO-LED	↔	Mode control board D
MODESELECT A	↔	Mode control board E
MODESELECT B	↔	Mode control board F
MONO	↔	Mode control board G
MUTE (at R45)	↔	Mode control board H
Synthesizer board		
$\overline{\text{UNLOCKED}}$	↔	Mode control board I
Keyboard/display board		
D0	↔	Synthesizer board D0
D1	↔	Synthesizer board D1
D2	↔	Synthesizer board D2
D3	↔	Synthesizer board D3
D4	↔	Synthesizer board D4
D5	↔	Synthesizer board D5
D6	↔	Synthesizer board D6
$\overline{\text{IORW}}$	↔	Synthesizer board $\overline{\text{IORW}}$
+ (near D134)	↔	Synthesizer board + (near C414)
0 (near C106)	↔	Synthesizer board – (near C414)
E (near S115)	↔	Synthesizer board – (near C414)
F (near S115)	↔	Synthesizer board RESET

* Use screened cable.

side of the front panel. Their locations are governed by the layout of the front panel foil, which has a size of 483×132 mm (W×H). Before sticking it on to the front panel, the foil (or a photo copy of it) is conveniently used to mark out the holes that have to be cut and drilled. Next, use photocopies of the overlays to mark the locations of the corner fixing holes for each PCB. The distance between the inside of the front panel and the PCBs is made such that the keytops are flush with the outside of the front panel. This may require some filing and cutting of PCB spacers, but it is certainly worth your while. On the prototype, we glued the heads of standard cylinder head screws to the inside of the front panel, at the locations marked out with the aid of the respective overlays. Plastic PCB spacers and nuts were used to achieve the correct mounting distances behind the front panel. Alternatively, you may want to use screws with countersunk heads, and drill holes in the front panel such that the surface remains flat for the foil to be stuck on smoothly. This, however, is not easy, and bumps and holes easily occur in the front panel (if not immediately, then after some time), which spoils the look of the receiver. We therefore recommend fitting the PCBs with the aid of screws glued to the inside of the front panel.

The front panel foil has transparent windows (bezels) for the displays and the LED bar. The clearance for the keys must be cut out very carefully using a sharp hobby knife. Take care not to damage the foil parts cut out, since these are used to stick on the keycaps later. Once again observe the key order (left to right):

NORMAL WIDE EFFECT STEREO MONO.

Wiring

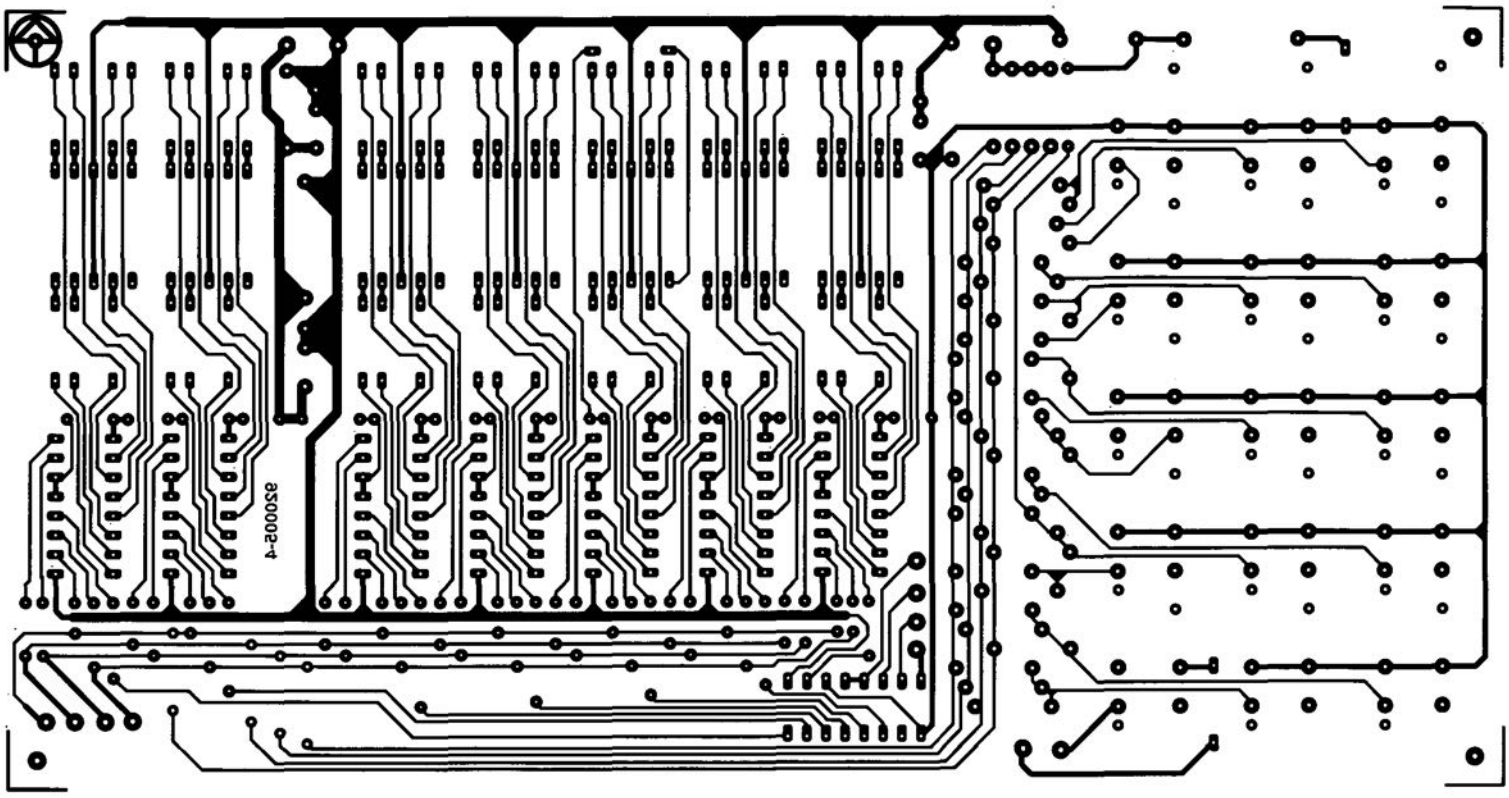
To keep synthesizer noise to a minimum, the ends of the signal wire in the coax cable must be kept as short as possible. This means that the signal wire must be screened over the maximum possible length between RF input socket (on the rear panel of the enclosure), and the 'Ant.' and 'GND' terminals on the main tuner board. The shielding braid of the coax cable must be connected at both ends: to the 'GND' terminal next to the 'Ant.' terminal, and to the shaft of the RF input socket, which is fitted **isolated from the rear panel**.

The audio output signals are taken from the R-OUT and L-OUT terminals on the main tuner board to the output sockets on the rear panel. The cable screening is connected to the respective ground (GND) terminals on the main tuner board. The output sockets are also the best location to make the **only** connection between the **circuit ground** (GND carried via the screening of the audio cable) and **earth** (carried via the metal enclosure).

The connection of the components connected to the mains must be carried out with great attention paid to proper isolation, and using appropriate wire. All mains wiring must be secured to the enclosure, and kept away as far as possible from signal wiring.

The connections between the printed circuit boards are listed in Table 1. Needless to say that a carefully done wiring job may prevent precious time spent on fault finding. Note that the tuning voltage (UABST) is carried via a single-core screened audio cable.

Provided the main tuner board has been adjusted as outlined earlier, the FM tuner is ready for use when the wiring is finished. Simply connect the antenna, an audio amplifier, and power up. Program your favourite stations, and ... happy listening! ■



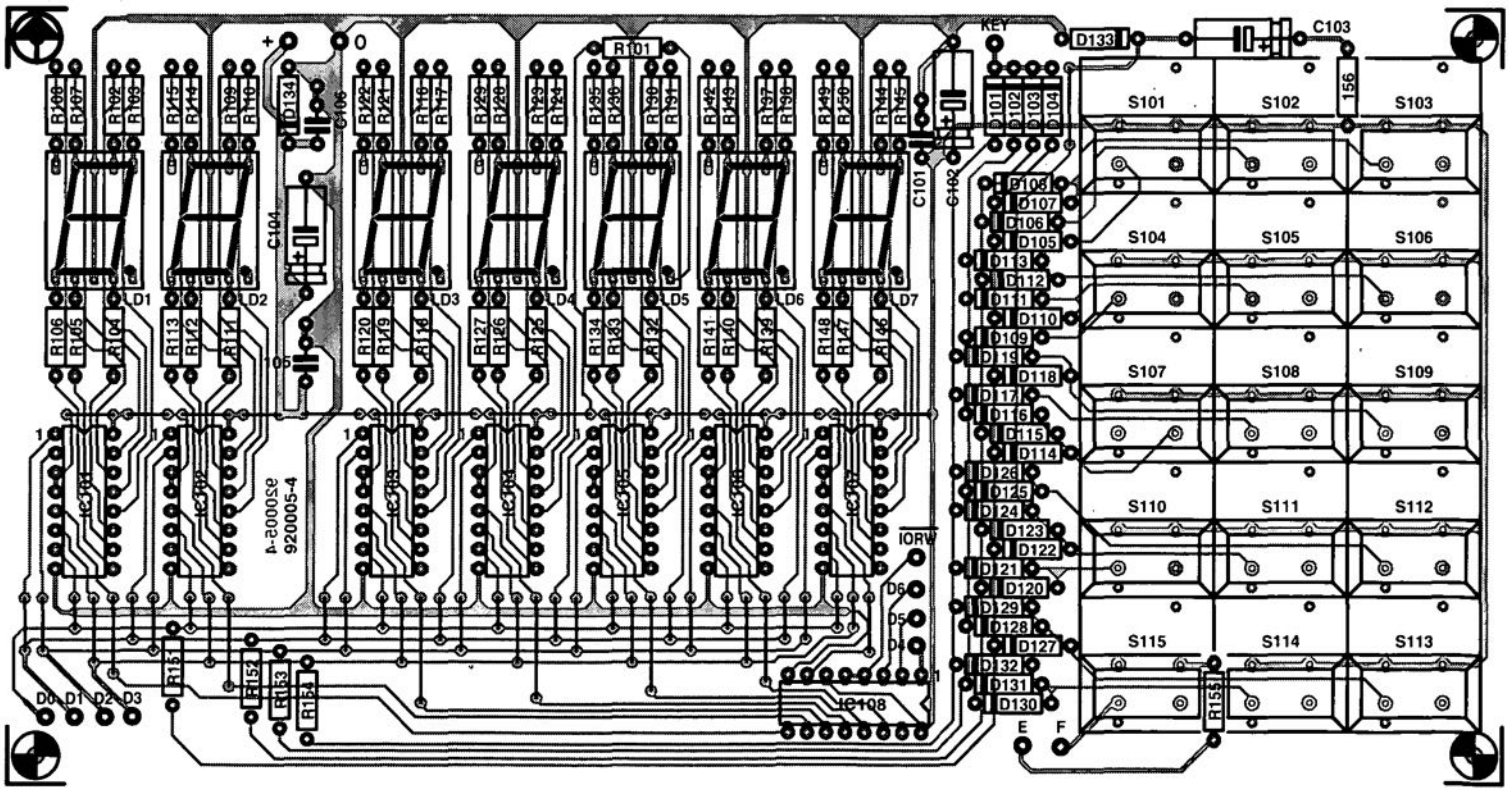


Fig. 18. Track layout (mirror image) and component mounting plan of the keyboard/display PCB.

SCIENCE & TECHNOLOGY

A VIRTUAL COMPONENT: HALF-CAPACITANCE FROM HEAVISIDE

by M.C. Soper, MA

A capacitor can be defined by the fact that

$$i=C(dV/dt)$$

is the formula relating voltage, V, current, i, and time, t, when the voltage across the capacitor, C, changes.

Similarly, although rarely used now except in r.f. work,

$$V=L(di/dt)$$

is the formula used to define an inductor, L.

Oliver Heaviside used his transform to define the 'fractional integral' in the following terms:

if $F(t)$ has Laplace transform $f(s)$, then

$$\int_0^t F(u)du$$

has Laplace transform $f(s)/s$ and dF/dt has Laplace transform $sf(s)-F(0)$.

Now, the half-integral

$$\int_0^t F(u)du$$

has the Laplace transform $f(s)t^2(s)$. When defined, the half-derivative is the inverse of the half-integral. Call this operator $D^{1/2}$, then

$$D^{1/2}(x)=2t^2(x/\pi)$$

and

$$D^{1/2}(x^m)=x^{m-1/2}(m-1)!/(m-{}^1/_2)!$$

Since these are all calculated from the first derivative half-integrated (by using the inverse Laplace transform), they are all properly defined functions. In general, let $f(x)$ be expressible as a power series in x, then $D^{1/2}(yf(y))$ is properly defined, where $y^2=x$ (if x real, take positive value).

Static to dynamic

Definition: let $D^{1/2}$ denote half-differentiation with respect to time. Then, a half-capacitor obeys the law

$$i=CD^{1/2}(V)$$

and a half-inductor obeys the law

$$V=LD^{1/2}(i).$$

To show how a half-derivative is calculated, consider the half-derivative of $\exp(at)$. This can be done as the half-integral of the derivative:

if $y=\exp(at)$, then $dy/dt=a\exp(at)$.

If $F(t)=a\exp(at)$,

then $f(s)=a/(s-a)(f(s)/t^2(s)=$

$=az/(s-a)$ (where $1/z$ is t^2/s),

for which $F(t)=t^2(a)\exp(at)\text{erf}(t^2[at])$ is the inverse Laplace transform. For the ability to calculate this, we are much indebted to Oliver Heaviside.

Thus, the admittance of the half-capacitor at angular frequency ω is given by:

$$Ct^2(j\omega)\text{erf}(t^2[j\omega t])$$

and the impedance of the half-inductor is given by

$$Lt^2(j\omega)\text{erf}(t^2[j\omega t]).$$

Erf (x) is the integral from 0 to x of $\exp(-x^2)\times 2/\sqrt{\pi}$.

The product of the two impedances is L/C, and t is the time since turn-on. Note that after the circuits have settled down (t is large), $\text{erf}(t^2[j\omega t])$ is very close to one. Thus, the formulas are much simplified and become:

$$Lt^2(j\omega)$$

and

$$1/Ct^2(j\omega).$$

Therefore, some time after turn-on, a half-inductor becomes:

$$(L/t^2[2/\omega])(1+j)$$

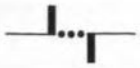
and a half-capacitor:

$$\{1/(Ct^2[2\omega])\}(1-j).$$

Half-reactance for sale

Evidently, a half-inductor can be viewed as a frequency-dependent resistor in series with a frequency-dependent inductor, and similarly for a half-capacitor.

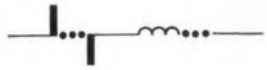
We need symbols at this point and choose



for the half-capacitor and

for the half-inductor.

Choose $L\omega L=1/C\omega C$ and consider:



This becomes:

$$L(1+j)t^2(\omega/2)+L(1-j)t^2(\omega/2)=Lt^2(2\omega),$$

which is a real, frequency-dependent resistance; note, however, that $LC=1/\omega$ compared with the usual formula $LC=1/\omega^2$ for a tuned circuit at resonance.

The parallel connection produces exactly the same result: let $z=Lt^2(\omega/2)$, then

$$z(1+j)//z(1-j)=2z=Lt^2(2\omega).$$

Note that with normal tuned circuit, the parallel impedance at resonance is infinite, and the series impedance is zero.

Is Z maximum or minimum when $LC\omega=1$?

Let $kLC\omega=1$, then the series connection is

$$L(1+j)t^2(\omega/2)+kL(1-j)t^2(\omega/2)=$$

$$=Lt^2(\omega/2)[1+k+j(1-k)],$$

which, with magnitude squared, becomes

$$\omega L^2(1+k^2).$$

This is a minimum when $k=0$, unlike the case for a usual tuned circuit.

Let $z=Lt^2(\omega/2)$, then for the parallel case:

$$(1-j)/2z+(1+j)/2kz=[(k+1)+j(1-k)]/2kz.$$

The parallel impedance is then:

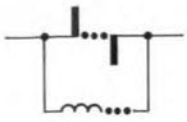
$$2kz/[(k+1)+j(1-k)].$$

Let k be positive, then the minimum impedance occurs when $k=0$, and the maximum when k is very large.

Zero resistance

The condition $L\omega=-1/C$, which can be brought about by the use of negative impedance converters—NICs—leads to zero resistance in both the parallel and series connection. Then,

has zero impedance and, similarly, for the parallel case



gives an impedance $jz=jLt^2(\omega/2)$.

For a half-capacitor in series with a 1-Ω resistor, a law like this is obeyed:

$$V-v=CD^{1/2}(v),$$

where V is the supply voltage. Therefore, the solution of half-differential equations like this is specifically interesting to see what kind of evolution of voltage across the half-capacitor occurs in practice.

Duration of the initial transient

So far in this analysis, we have adopted a simplified expression for the half-reactances, ignoring the error function (erf); this is justified, since the time-dependent feature vanishes very quickly at all but the very lowest frequencies, and this we will establish now.

As time increases, the function erf(t) rises to close to 1, and then stays near 1 indefinitely for increasing time. Erf constantly increases to this level. When $t=0.75$, erf(t) is close to $1/1.414=0.7071$, and thereafter is greater. Thus, we must consider:

$$\text{erf}(t^2[\omega t])>0.7071.$$

This occurs when $(\omega t)>0.55$; since $\omega=2\pi f$, we have:

$$ft>0.0872.$$

This implies that for frequencies above 10 Hz, this feature can be ignored after 0.2 s.

The effect of j within the square root has been ignored here, but analysis in terms of functions like Fresnel sine and Fresnel cosine shows that the same general behaviour is displayed, although the complex number introduces some small wobbles in the tendency to unity.

Since the use of $\exp(j\omega t)$ in circuit analysis implicitly applies only to the steady state when d.c. levels are quiescent, the use of the simplified formulae is justified. The fact that, just after initial transients, $dy/dt=y$ has other solutions is important, even for physics, since the half-derivative may have a direct bearing on the thinking behind Dirac's equation of the electron. If time is never measured directly, how can we assert confidently that the first derivative, and not the half-derivative, is appropriate for measuring change?

Laws obeyed by half-reactance

Laws obeyed by half-reactance will apply in the steady state after the levels within the circuit have become quiescent. There are two kinds of element, say, cZ and ℓZ, where the small letters denote 'half'.

1) $1/cZ=Ct^2(j\omega)$

$\ell Z=Lt^2(j\omega)$

$(cZ)\times(cZ)$ is a capacitance;

$(\ell Z)\times(\ell Z)$ is an inductance.

2) $(cZ)\times(\ell Z)$ is 'has no reactance'.

3. $c1Z//c2Z$ is a half-capacitance;

$\ell 1Z//\ell 2Z$ is a half-inductance.

4. $c1Z+c2Z$ is a half-capacitance;

$\ell 1Z+\ell 2Z$ is a half-inductance.

5. $1/cZ$ is a half-inductance;

$1/\ell Z$ is a half-capacitance.

There are other relations that can be related to the original defining relations:

$$i=CD^{1/2}(V)$$

and

$$V=LD^{1/2}(i).$$

Evidently, when a half-capacitance is in series with a 1-Ω resistance, there is a relation between the voltage on the resistance and that on the half-capacitance. Let V be the applied constant voltage across the series pair; then:

$$i=V-v=CD^{1/2}(v).$$

Half-differentiating this yields

$$VC/t^2(\pi t)-i=C^2D(v),$$

that is, after the circuit has settled down, i and v are related by the law of a negative capacitance. The same applies to the half-inductance in parallel with a 1-Ω resistance: this becomes a negative inductance. This does apply not only to a constant voltage, but also to a sinusoidally varying one.

But does following the law of a negative capacitance necessarily entail that we have a negative capacitance? Say, $i=-CD(v)$ and let $v=V\exp(j\omega t)$, then

$$i=-CV j\omega\exp(j\omega t);$$

let $i=I\exp(j\omega t)$, then

$$V/I=v/i=-1/j\omega C,$$

which is the formula for the impdance of a negative capacitance; so, the answer is yes.

Practical use of half-reactance

Can these circuit elements be built? The essential requirement is the square-rooting of some impedance. Now, suppose we had a device to square any impedance presented to the input terminals, so that the square of the impedance appeared at the output terminals. We could then compare the output with, say, an inductance and feed back any error signal to the input of the squaring device appropriately transformed, and thus have the appearance of a half-inductance at the input.

Thus, fabrication is possible, because impedance squaring devices are known to exist. The case of a capacitor is not so easy, because some active devices do not work well with a pure capacitive load; but certainly a half-capacitor in parallel with a very high impedance could be made. The effect of 1-Ω in series can then be checked empirically. (A circuit element that produces a negative capacitance or a negative inductance when combined with standard components cannot fail to have many uses if practically produced, but until this is checked empirically there is uncertainty about whether this can be done practically: a'practical' implementation may just oscillate).

More significantly, a circuit that has an impedance magnitude that is not simply proportional or inversely proportional to frequency, but to the square root of frequency, or the reciprocal of this, is a device that has many immediate uses in the design of different types of filter: new types of filter with a more gentle roll-off than usual.

In particular, the ends of the frequency band would have responses less dependent on component tolerances, so that the frequency response of, say, audio filters at high and low frequencies would be more predictable, and the spread in manufacture would be less.

Also, the half-capacitance and half-inductance, apart from theoretical interest, open the door to devices whose impedance magnitude depends on half-integral powers of the frequency domain.

We must restate here that these devices are defined in practice by the half-derivative operation (or half-integral) and not by the simple square-root form, which is approximate.

Quiescence

We have already determined how long the quiescent phase lasts at different frequencies, that is, before the approximations used in the laws of the last section become accurate. This is a consideration that relates to the use of the device itself, but, on a more general note, this is serious, because we never directly measure time (think about how time is determined). We cannot say whether changing parameters should be differentiated or half-differentiated to represent the rate of change. Consider that there is another way of considering the time variable, that is, change in a parameter u is represented by $D^{1/2}(u)$, where the half-derivative is with respect to a variable f and:

$$D^{1/2}(u)=du/dt=(df/dt)(du/df)$$

by the chain rule. We may then consider that t and f are related by some non-trivial func-

tion like $t=\text{erf}(t^2[f])+g(f)$, and thus that our physics and our picture of the world is changed, unobservably. (Dirac argued that d/dt had to feature in the equation of the electron, but did not consider fractional derivatives, invented by Heaviside, which can feature, because t is not measured directly).

This does not matter at all if our Universe is now quiescent, because of the properties of the erf function, but at some very, very low frequencies there is a difference which would seem to our measurements as 'physics' changing with time. The red shift, for instance, may be a feature resulting from this; nor has a changing value of G, the gravitational constant, been ruled out as yet.

Why should this be relevant to electronics? Because all circuits are turned on. This means in practice, that assumptions made for quiescent conditions may not apply in some case for a very long time after switch-on; mathematically, this means that for some time

$$a\exp(at)\text{erf}(at^2[t]),$$

where $a=t^2(j\omega)$, is just as relevant as $\exp(j\omega t)$, although it is both time-dependent and a function of frequency.

The prime example of this is the 'American East Coast Blackout' after which it was found that only one man knew how to turn on all the stations and switches in the right order without causing fatal instabilities. That is a large-scale version of the same phenomenon.

It is a daunting thought that the Universe, which is some ten thousand million years old, may still be affected by a switch-on transient (of course, this is only on one view of cosmology).

More importantly, this analysis indicates that under a.c. conditions, not d.c. (which is what the erf alternative refers to), we cannot necessarily apply the standard analysis methods to the frequency dependence of the circuit at very, very low frequencies, since erf forms are equally appropriate. Especially when half-capacitances and half-inductances are built in, this feature must be checked carefully. In essence, $D(y)=y+$(terms decaying with time) can have a solution very different indeed from $D(y)=y$. And, since in practice differentiation takes time (even when done with Cs and Rs), after switch-on, the former is more relevant; for instance:

$$D(y)=y+1/t^2(\pi t)$$

has a solution similar to

$$y=\exp(t)\text{erf}(t^2[t]),$$

our erf function.

That is, blithe claims that 'this circuit works down to zero frequency' must be checked very carefully, since reactance is always present. ■

References

1. *Heaviside's Operational Calculus*, by Ernst Julius Berg, Sc.D., McGraw-Hill, New York and London, 1936.

2. *Electromagnetic Theory*, by O. Heaviside, Dover, NY, 1950.

3. "Augmented A-Matrices,...", by M.C. Soper, *Elektor Electronics*, May 1991.

4. *Quantum Theory*, by P.A.M. Dirac, OUP, 1978.

5. *Cybernetics*, by Norbert Wiener, Wiley, 1961.

Plus any book on Laplace Transforms.

DIFFERENTIAL TEMPERATURE INDICATOR

THE circuit in the diagram enables the monitoring of two temperatures, t_1 and t_2. The sensors are NTC resistors R_3 and R_4, which may be connected to the circuit via lengths of circuit wire that may be up a few metres long.

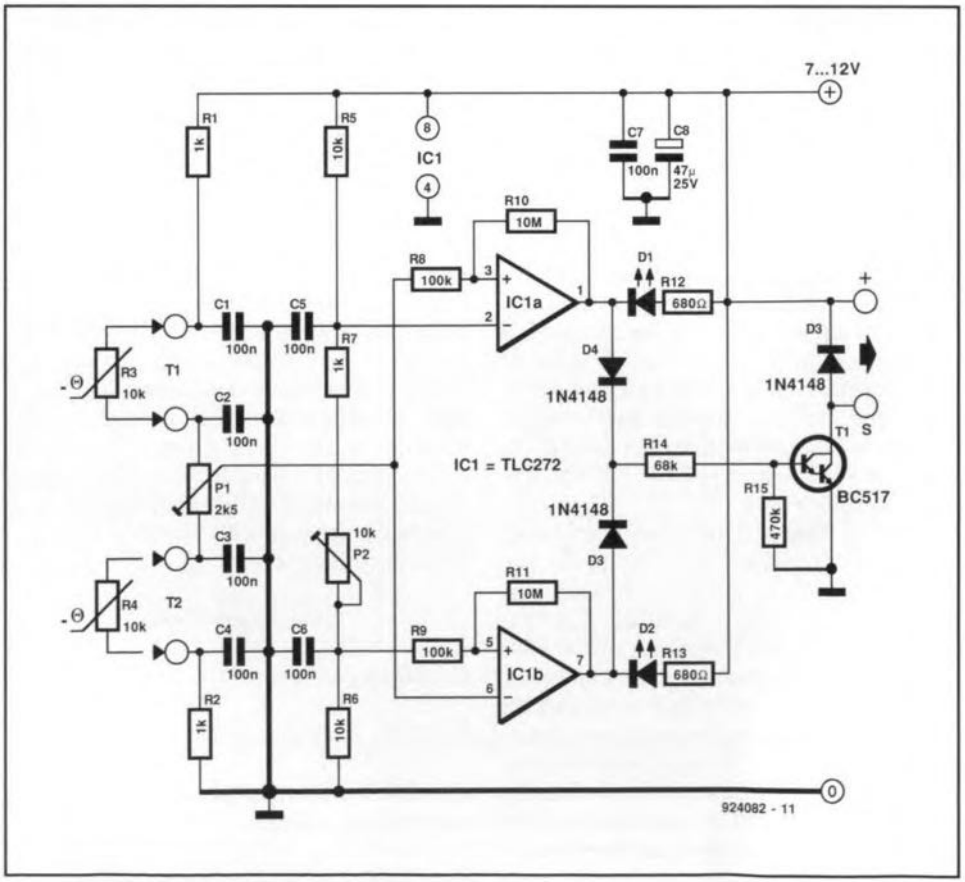
Diodes D_1 and D_2 indicate whether t_1 and t_2 are close to each other or not. 'Close' means that the difference between the two voltages from the sensors is smaller than the level set with P_2. If the temperatures are close, both LEDs light; if they are not, one LED will go out: D_1 if t_1 is higher than t_2, and D_2 if t_1 is lower than t_2. Apart from this optical indication, it is possible to obtain an acoustic one by connecting a d.c. buzzer to terminal S.

It is also possible to connect a 7–12 V relay with a maximum energizing current of 400 mA, to this terminal. Free-wheeling diode D_5 protects T_1 against a possible, destructive back-e.m.f.

The circuit draws a maximum supply current of 35 mA, largely on account of the LEDs.

A certain temperature off-set may be preset with P_1. Normally, this preset will be at the centre of its travel: when $t_1=t_2$, the potential at the wiper will then be half the supply voltage.

The 'window' within which temperatures are monitored may be preset with P_2 to a value of 1–25 °C at a regulated supply voltage of 8 V and t_1=25 °C.



[Amrit Bir Tiwana – 924082)

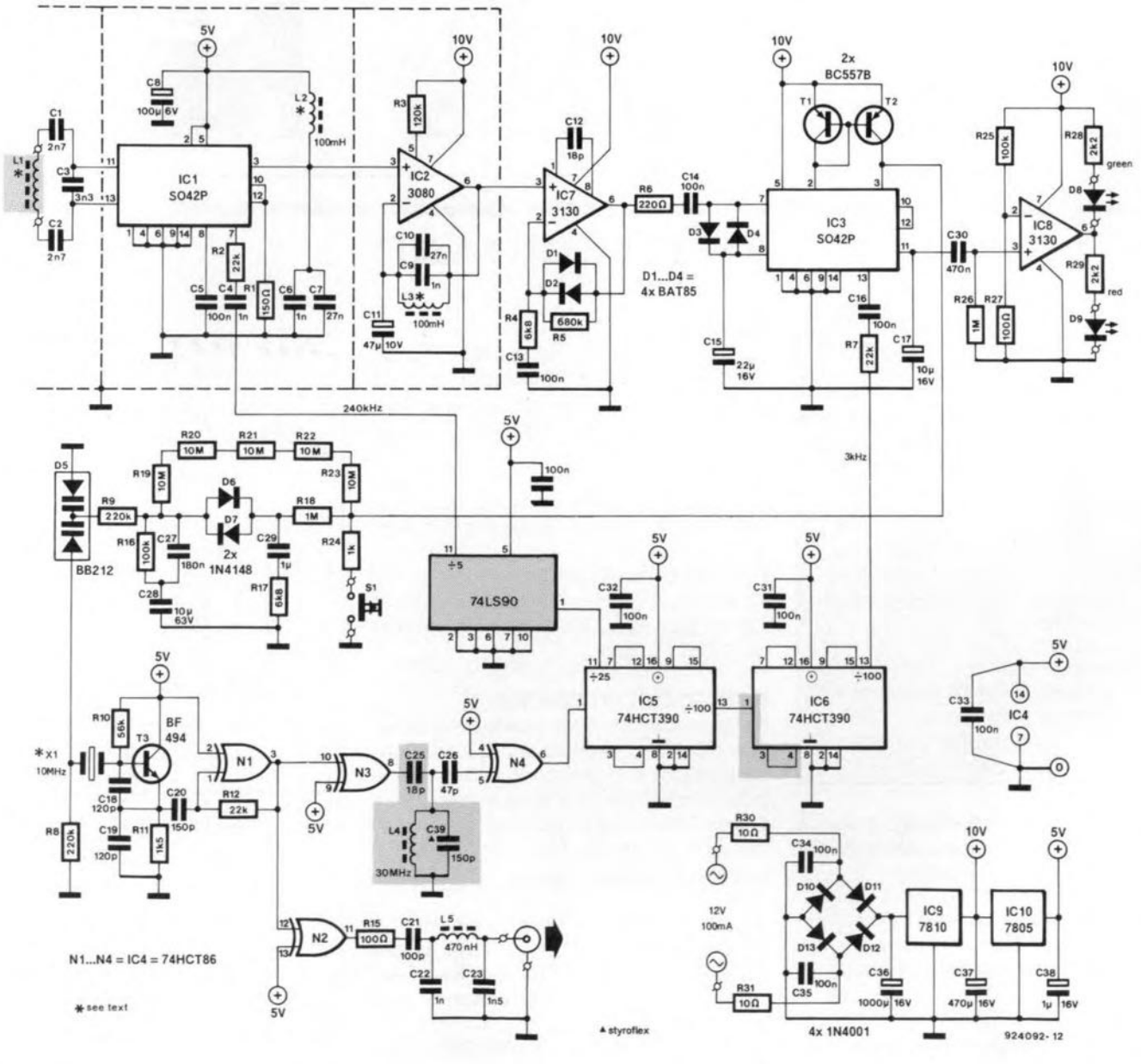
KALUNDBORG 10 MHZ FREQUENCY REFERENCE

EVER since the long-wave broadcast station Kalundborg changed its frequency from 245 kHz to 243 kHz to comply with the CCIR's recommendations for a 9 kHz raster in the LW and MW bands, it has become possible to use the carrier in the locked frequency standard described in Ref. 1. Kalundborg is a 300 kW long-wave transmitter in Denmark, with a range of about 500 km (300 miles). This article is, therefore, of particular interest to our Scandinavian readers.

Briefly, what is proposed here and in the next item ('preamplifier for Kalundborg frequency reference') is to change the divider in the frequency reference such that a carrier input frequency of 243 kHz can be used instead of 77.5 kHz (the transmit frequency of DCF77 in Germany), for which the circuit was originally designed. The changes are outlined in the simplified block diagram, Fig. 2, which is best compared with Fig. 1 in Ref. 1. In practice, the original circuit of the reference is changed to the extent that a new circuit diagram is required—see Fig. 1. The new circuit is much simpler than the original, mainly because some circuit sections could be omitted, including the VLF preamplifier (T_1-T_4 in the original design), the 10 MHz 'locked only' output (IC_7 and T_{12} in the original design) and the 'error' detector (N_2, N_3, N_4 and the beeper in the original design).

In the 'Kalundborg' circuit shown here, the 10-MHz signal supplied by X_1 and T_3 is multiplied by 3 by parallel tuned circuit L_4-C_{39}. The 30-MHz signal is subsequently divided by 100 (IC_5) and again by 100 (IC_6) to obtain the 3 kHz reference for multiplier IC_3. The 240 kHz signal used to heterodyne with the 243 kHz carrier is

1



obtained by dividing the 30 MHz signal by 25 (IC_5) and then by 5 (74LS90).

The antenna, formed by an inductor wound on a ferrite rod and resonated by capacitors C_1, C_2 and C_3, is connected direct to the balanced inputs of the S042P mixer (IC_1). The error signal at the output of the multiplier (IC_3) is filtered and converted into a tuning voltage, which is applied to a dual varicap, D_5. The varicap is capable of detuning (to a small extent) the 10 MHz quartz oscillator, and so closes the phase-locked loop (PLL). Provided Kalundborg is received with adequate strength (rotate the ferrite rod), the LED at the output of IC_8 lights, and a 'rock-steady' 10 MHz reference signal is available at the output of N_2.

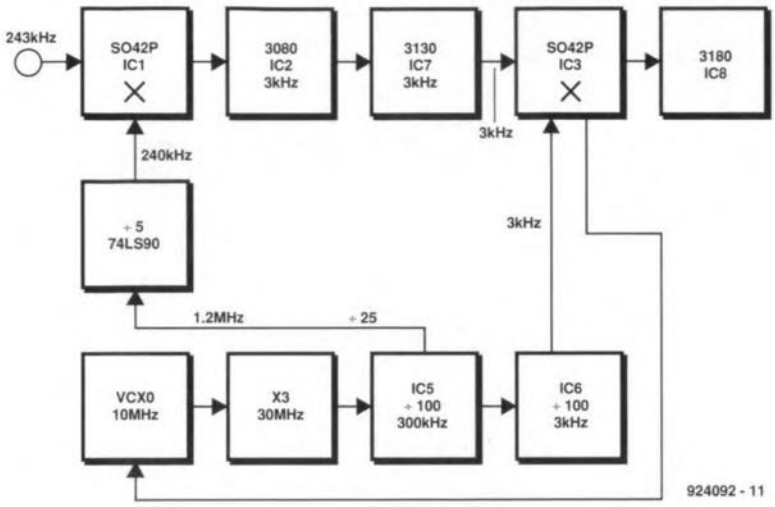
Figure 3 shows a detailed diagram of the ×3 multiplier. Inductor L_4 consist of 4.5 turns of 0.5 mm dia. enamelled copper wire on a former with a ferrite core. The former has an outside diameter of 6 mm, and L_4 is drawn out to a length of about 8 mm. The operation of the multiplier is easily checked with the aid of an oscilloscope and/or a frequency meter, the signal levels being quite high. The core in L_4 is adjusted for the highest 30 MHz level at pin 5 of N_4.

(L. N. Jensen, OZ6LV – 924092)

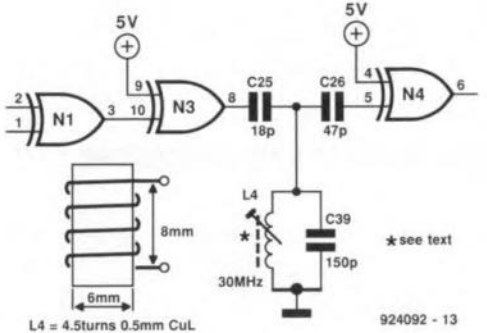
Reference:

1. "DCF77 receiver and locked frequency standard", *Elektor Electronics* January 1988.

2



3



PREAMPLIFIER FOR KALUNDBORG FREQUENCY REFERENCE

IN all cases where reception of Kalundborg is marginal using the ferrite rod at the input of the S042P, the two-stage preamplifier shown here can help you ensure longer 'lock' peri ods of the frequency standard.

The antenna inductor, L_1, consists of 150 turns of 0.3 mm dia. enamelled copper wire on a 12.3 mm dia plastic, thin cardboard or paper former, positioned centrally on a ferrite rod with a length of 238 mm and a diameter of 9.6 mm. The inductor is resonated at 243 kHz by a fixed capacitor, C_9, and a trimmer, C_{10}. To keep the load on the antenna inductor, as small as possible, the first stage of the preamplifier is formed by a FET Type BF245.

The amplfied 243-kHz signal is fed to one of the inputs of the S042P at the input of the frequency standard (see previous article). Using the preamplifier, the author (who lives in Denmark) measured a signal level of 1.4 Vpp on pin 6 of IC_2 in the frequency reference.

The noise level normally measured after Kalundborg switches off at 0.30h CET is about 100 mV_{pp}.

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