RS

ELEKTOR ELECTRONICS

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Greenweld's
Summer Supplement

Special 200th issue

Competition:
lots of prizes to be won!

Digital short-range radio
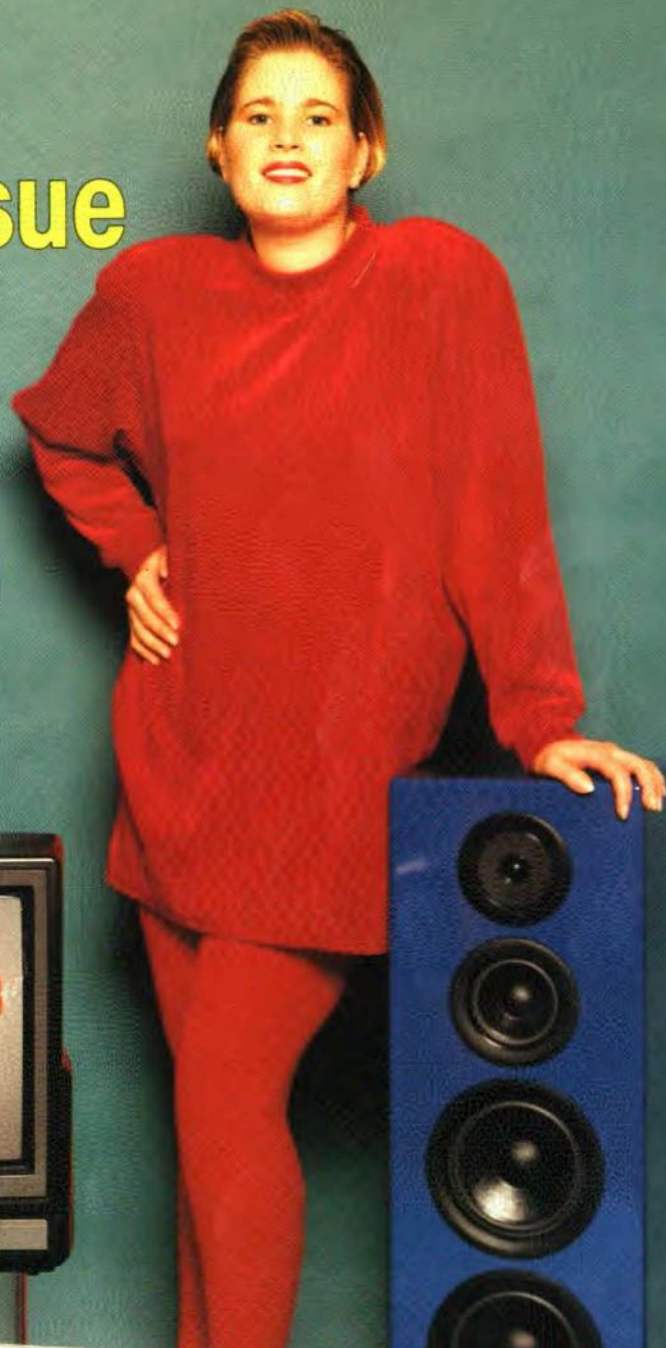
1.3 GHz prescaler

NICAM decoder

GAL programmer

Z80 card

Compact mains supply

NICAM-728
STEREO

NICAM DECODER

POWER   DUAL MODE   STEREO DUAL

NICAM DECODER

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ELEKTOR ELECTRONICS

CONTENTS

May 1992
Volume 18
Number 200

Front cover
Stereo TV is with us in the shape of NICAM, a system developed by the BBC and now also adopted in several other countries. Moreover, it is incorporated in a draft CCIR recommendation. In this issue, we give you the background of the system and also a practical NICAM decoder. The decoder is suitable for PAL B/I/G formats and can be built as a stand-alone unit or be incorporated in an existing TV receiver.

Win a prize in our 200th issue competition
p. 63

Multi-purpose Z80 card – p. 14

Compact mains power supply - p. 21
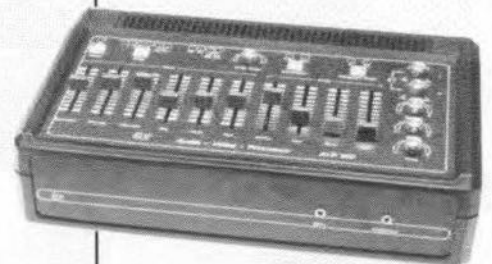
Audio-video processor – p. 43

GAL programmer – p. 55

MULTI-PURPOSE Z80 CARD

PART 1: SYSTEM DESCRIPTION
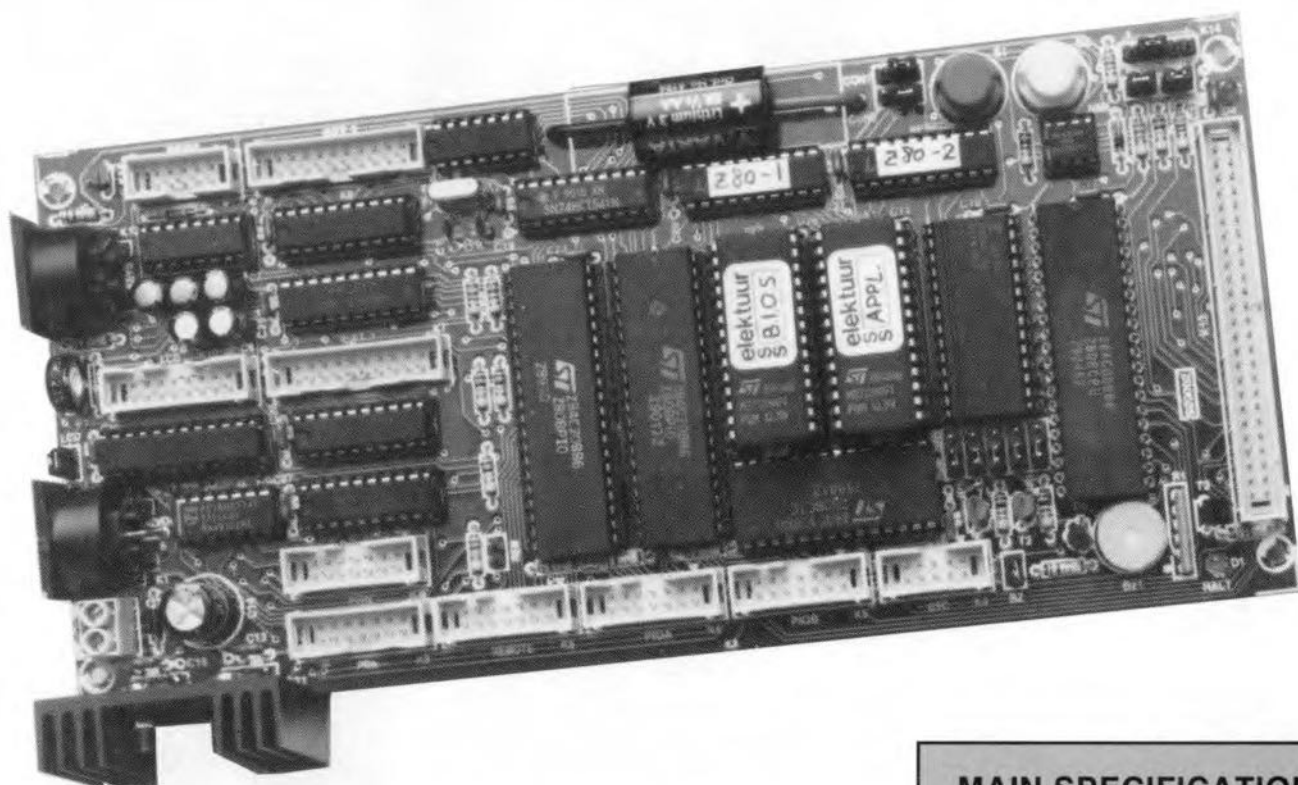
Although microcontrollers are now firmly established, we are pretty sure that the present Z80 processor card will appeal to many of you. Easy to use in combination with such options as a liquid crystal display and an infra-red remote control, and supported by a BIOS that takes the hassle out of I/O programming, this is the nineties-style way of dealing with an 'evergreen' 8-bit microprocessor.

Design by A. Rietjens

THIS Z80 card is easy to use for a wide range of applications thanks to its solid base formed by a number of Z80-family ICs. Remarkably, the multi-purpose character of the card is not compromised in any way by the I/O options available. These options provide functions that normally call for the soldering iron to be switched on because you have to build them yourself, not even mentioning the effort that goes into writing suitable control software. The hardware and software proposed here ensures, in the best possible way, that non-used functions do not interfere with the ones that are used, or can be adapted easily for other purposes. An example of this is a PC-XT keyboard that may be used as an input device with the present card.

Block diagram

As may be expected, a system as outlined above requires quite a bit of electronics. To keep you from losing track at this point already, have a look at the block diagram in Fig. 1. The Z80-CPU is used alongside two Z80-PIOs and one Z80-CTC. Together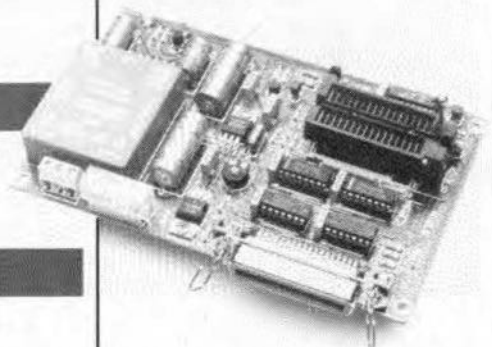 with the memory, these ICs form the heart of the Z80 card, which is completed with the usual I/O decoding and memory addressing logic. The latter supports the use of bank switching, so that up to 128 Kbyte may be addressed.

As you can see in the block diagram, there is no shortage of I/O and interfacing capacity: RS232, a parallel printer and a display are all catered for. The card receives

MAIN SPECIFICATIONS

Hardware:

- Z80B-CPU running at 5 MHz
- 32 I/O lines, min. 8 and max. 16 for internal use
- 4 timers
- Up to 64 Kbyte RAM and 64 Kbyte ROM or EPROM
- 8-bit A-D/D-A converter
- Standardized RS232 serial interface; all standard baud rates between 50 and 38,400
- Centronics-compatible parallel printer interface
- Two connections for 'universal I/O interface' extension cards
- On-board watchdog
- Input device: PC/XT keyboard or RC5 infra-red receiver
- Connection for LC display with up to 2×40 characters
- On-board battery backup

Software:

- BIOS available to control and test all card functions
- BIOS is MSX-compatible
- Built-in test routines
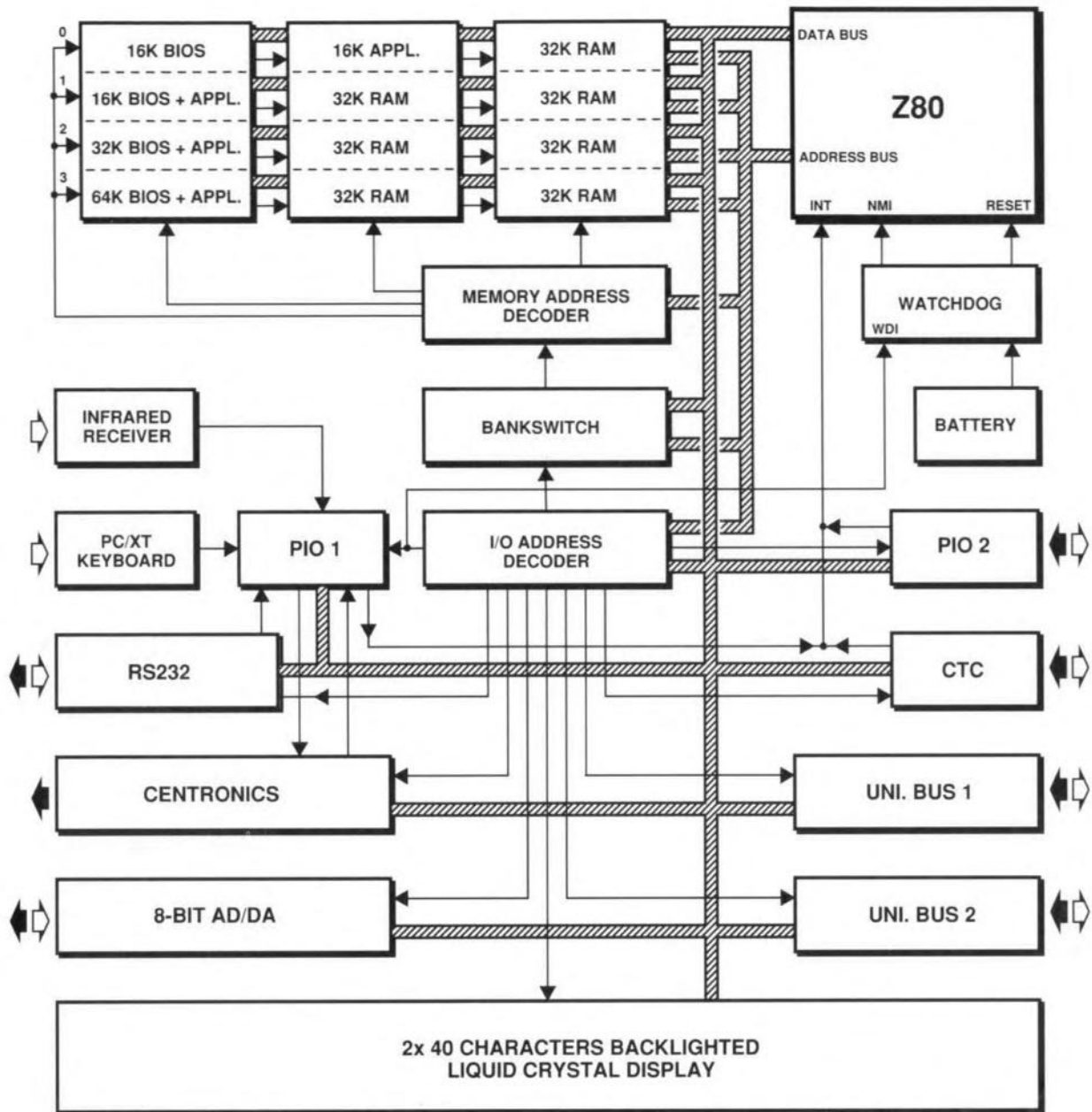
Fig. 1.   This block diagram clearly shows the structure of the Z80 card. The Z80-CPU is supported by two Z80-PIOs and one Z80-CTC. Together with the memory, these four ICs form the heart of the system.

data either from a terminal via the RS232 link, or more directly via an XT-compatible keyboard or any RC-5 compatible infra-red remote control. Apart from the digital interfaces, the card also offers an analogue interface in the form of an 8-bit ADC/DAC.

Those of you who require even more I/O capacity will be pleased to find two universal buses that carry the (buffered) databus, a select line and two address lines. This extension bus is readily connected to any peripheral device or card that does not require more than four addresses in the I/O range. Examples of cards that can be connected are the relay card for the universal bus (Ref. 1) and the opto interface card for the universal bus, to be published in a future issue.

The Z80 card has a watchdog that serves

to signal power supply failures. When such a failure occurs, it arranges for the 'current state of affairs' to be stored in time by issuing a non-maskable interrupt (NMI). It also serves to re-initialize the card by means of a reset after a software crash, and to switch between the battery and the power supply to prevent data loss when the system is switched on and off.

Memory structure

To operate the Z80 requires an external memory in the form of an EPROM or a RAM. As shown in the block diagram, the present card offers four memory configurations. The standard system configuration consists of two 16-KByte PROMs and one 32-KByte

RAM. One EPROM contains the application program, the other the system BIOS (basic input/output system). The basic software available in the system allows an application program (stored in the first EPROM) to be started automatically. The other memory configurations allow the BIOS to be combined with user software run from a 27128, 27256 or a 27512, with a 64-KByte RAM in parallel. Further information on the exact memory and address allocations for each configuration may be found in Figs. 2a and 2b.

The Z80 BIOS

A BIOS is basically a program structure that enables the basic hardware and software in a

CON0	0	1	0	1	
CON1	0	0	1	1	
BANK0	32K ROM	16K ROM	32K ROM	32K ROM	
	32K RAM	32K RAM	32K RAM	32K RAM	
BANK1		32K RAM	32K RAM	32K RAM	
				32K ROM	
IC1	27128	27128			00000H - 03FFFH
			27256		00000H - 07FFFH
				27512 1/2	00000H - 07FFFH
				27512 1/2	18000H - 1FFFFH
IC2	27128				04000H - 07FFFH
		43256	43256	43256	10000H - 17FFFH
IC3	43256	43256	43256	43256	08000H - 0FFFFH
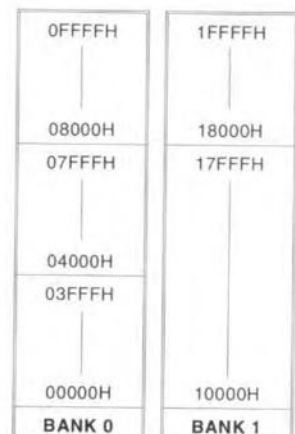
920002-I-13

920002-I-14

Fig. 2. (left) The memory configuration is determined by the position of jumpers CON1 and CON2, and the associated ICs. (right) Bank switching is used to enable the processor to address up to 128 Kbyte of memory.

```
                 0059H
;**************************************************************
;name:         ldirmv
;function:     load increment repeat into memory from video
;
;input:        BC=length, DE=ram address
;              HL=display character pointer
;output:       none
;changes:      AF, BC, DE
;**************************************************************
```

920002-I-15

Fig. 3. Example of BIOS routine documentation.

microprocessor system to be upgraded without having to scrap or rewrite existing software. In most cases, the BIOS is a list of start addresses that are the same for each version of the software. A specific function of the system may be called by calling such a start address. The start address contains a jump to the real address of the subroutine required. Thus, the BIOS user must keep in mind:
- the function of the subroutine;
- the call address;
- the variables required, i.e., the use and content of certain registers;
- how the registers contents are changed upon returning from the subroutine.

Only when all these features are known, the BIOS becomes 'transparent', and the user need not have a detailed knowledge of the exact operation of the subroutine.

A BIOS subroutine may be described as shown in Fig. 3. This definition provides all the data on the subroutine required to use it without knowing exactly how it works.

Memory and I/O address decoders

The selection signals of the main components in the Z80 system must be decoded to realize different memory configurations while avoiding conflicts. The configuration chosen and the bank switching information together affect the memory addressing. The configuration is selected before the system is started, and the bank switching is arranged by software. However, provision is made in a hardware to ensure that bank switching is possible only if allowed in the configuration used.

For those of you who do not know what bank switching is all about, the following explanation. Since the Z80 can only address 64 Kbytes of memory, certain provisions must be made if we want it to access a larger memory. In this case, we wish to address 128 KByte, divided into blocks of 32 Kbyte each. This means that there are four possibilities to select a total of 64 Kbytes of mem-

ory. Hence, two bits are required to implement bank switching — each bit selects two blocks of 32 Kbyte. When switching such a bit, we must take care not to switch off the block currently used by the CPU. Fortunately, the BIOS contains routines that make bank switching smooth and easy, as required, for instance, to access the RAM 'alongside' the BIOS EPROM in configurations 1, 2 and 3. The bank switching information is stored in a latch that can be written to via I/O addressing.

PIOs: parallel I/O

The Z80 card has two PIO (parallel input/output) ICs, each of which contains two 8-bit ports. The PIOs are initialized to bit input/output mode, which means that each bit may be used individually as an input or an output. PIO1 is partly used for internal functions, while PIO2 is available to the user, and is programmed as an input (this can be changed as required via the BIOS).

One port of PIO1 is used for internal signals, and the other to decode the signals supplied by the infra-red receiver. When the IR receiver is not used, the port is, of course, free for other applications. Among the functions of the other port in PIO1 are Centronics handshaking, decoding the PC-XT keyboard, and detecting interrupt signals issued by the RS232 interface. Evidently, these port functions can not be redefined via the BIOS.

CTC: four timers

The Z80-CTC on the present card contains three counters/timers. Of these, timer 3 is used to generate interrupts at 10-ms intervals during which time-dependent functions
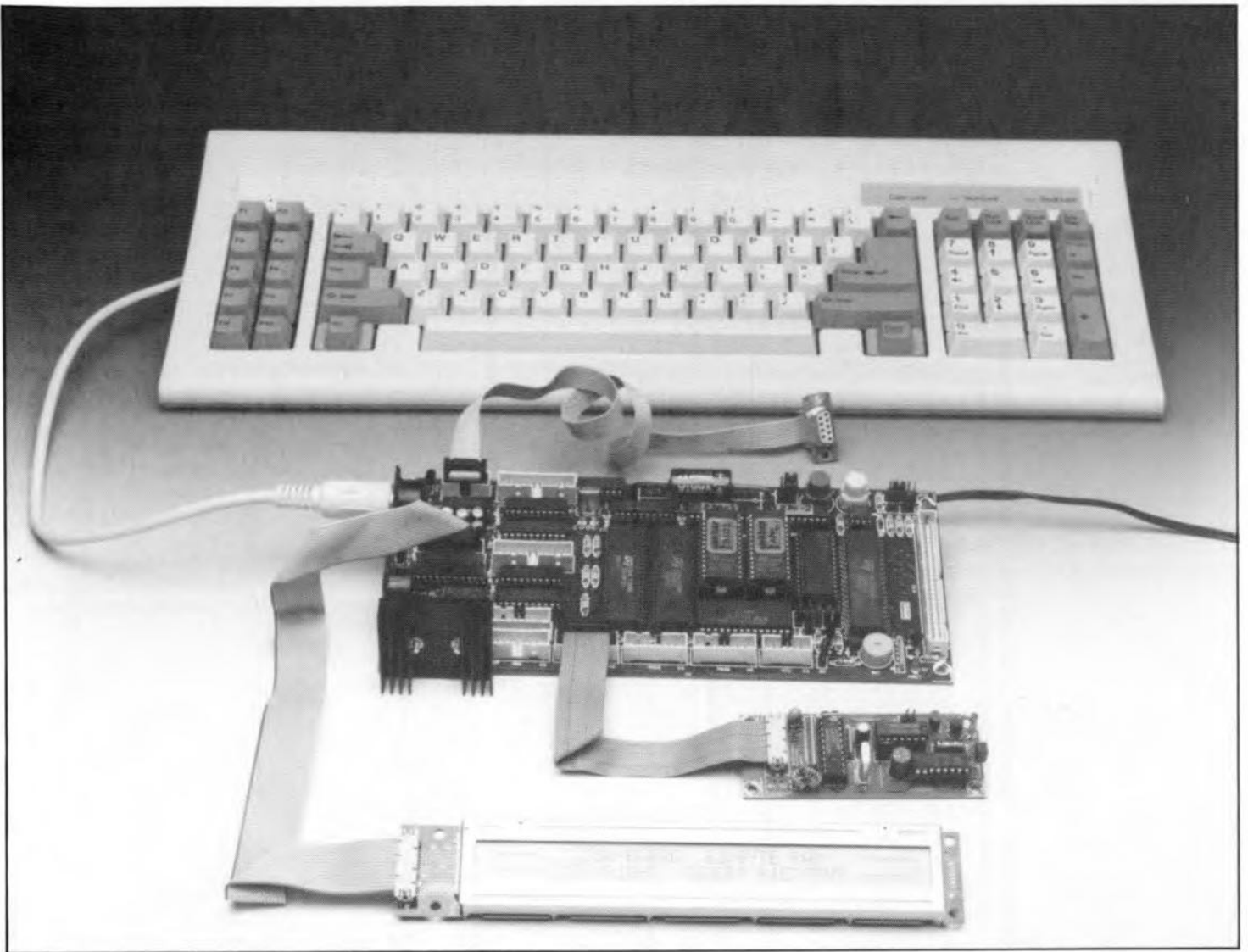
can be completed. A software 'hook' is provided to extend this interrupt routine with your own software. A hook is the software equivalent of a road diversion. The system area of the memory contains addresses that are filled with return instructions after the card is switched on. A number of BIOS routines start with a call to one of these addresses. Normally, this address contains a 'return' instruction to the BIOS routine. However, by replacing this return with a call to a user routine, the program can be diverted to an extension of the BIOS routine, which is thus 'hooked' to the basic one. Five addresses are available for each hook, which is sufficient to place a call and a return. If a jump instruction is used at the hook address, the extension subroutine does not return to the hook and the basic BIOS routine, which is then simply not executed. The diskette supplied with this project (order code ESS 1711) contains an example of the use of a hook.

Returning to the functions of the timers, the interrupt routine for Timer 3 counts down the 'on' time of the on-board buzzer, so that the software need not wait for this. Timer 0, Timer 1 and Timer 2 in the CTC are free for your own use.

Keyboard and IR control

Parallel input to the Z80 card is furnished either by a PC-XT keyboard or the RC-5 code infra-red receiver described in Ref. 2. The PC keyboard is connected to the board via its curly cord and 5-way DIN plug. The Z80 card automatically detects the parallel input device at power-on.

Any type of RC-5 compatible IR transmitter may be used. The push-button with the number '1' on it is defined as the escape (ESC) key, while the other buttons are assigned an ASCII value equal to their code plus 32. The key definitions are stored in RAM, which allows them to be readily changed. The jumper marked REM was orig-ibnally designed into the circuit to select remote control data tables. Its function has been scrapped, however, leaving it free for your own programming experiments.

RS232 and Centronics interfaces

The RS232 and Centronics interfaces on the Z80 card enable it to be controlled from a distance, and to print data respectively. The RS232 interface is suitable for full-duplex

communication with a terminal (or a PC running communication software). The interface gives the Z80 card the function of DCE (data communication equipment) which means, among others, that the Z80 card will only 'do' something via the RS232 if so requested. The software contains routines that allow parts of the memory to be read or written via the RS232 interface. It is also possible to adapt the baud rate and the transmission format. The interface supports all standard baud rates between 50 and 38,400.

Watchdog and battery backup

As already mentioned, the watchdog has a number of functions on the Z80 card. To begin with, it ensures the minimum required length of the CPU reset pulse when the card is switched on. In addition, the watchdog monitors the unregulated and the regulated supply voltages, and arranges the switching between the 5-V supply and the battery, and vice versa. The watchdog has an input that continually checks if the card has not 'crashed'. If a crash occurs, the watchdog resets the card. The latter function of the watchdog will be particularly valued with
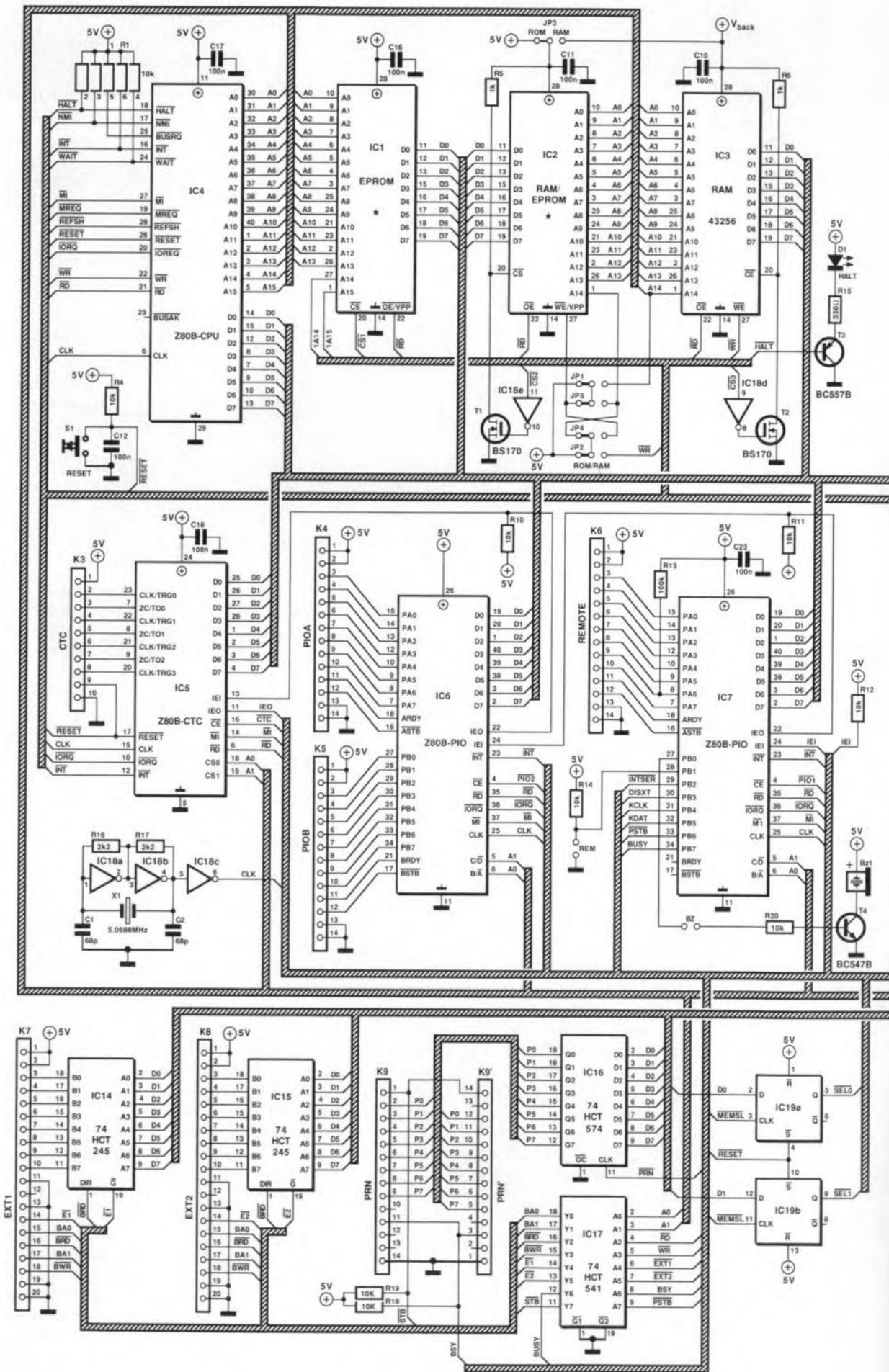
Fig. 4. Complete circuit diagram of the Z80 card. Among the advantages of using Z80-family components is their downright simple connect

measurement and control applications that run unattended.

Liquid crystal display

The Z80 card offers the possibility of connecting a liquid crystal display (LCD) of the normal or back-lighted type. Although LCDs with up to 80 characters are supported, the preferred type has 2×40 characters. However, one-line and four-line LCDs may be connected also. Nearly all of these intelligent LCDs are based on the HD44780 display controller from Hitachi, and have basically the same connections, albeit that the pins are sometimes arranged differently.

Circuit description

After a rather lengthy tour along the various functions shown in the block diagram of the Z80 card, it is time to see how these functions take on their practical shape.

The circuit diagram is given in Fig. 4. In the upper left-hand corner of the diagram we find the Z80B-CPU. A 6-MHz processor is used here because the system clock frequency is 5.0688 MHz. This frequency is used by the serial interface circuit to derive the standard baud rate series, starting at 50 bits/s.

The memory and I/O components are seen to the right of the Z80B-CPU and below it respectively. The I/O ICs are, of course, also B-versions because of the system clock frequency. The advantages of using Z80 family I/O components are basically that they are inexpensive, widely available, and extremely easy to implement. Essentially, once all the system and data lines of the components are connected, only the 'select' lines remain. Further, we must give some thought to the priority level assigned to each source that can generate an interrupt. This is arranged via the IEO (interrupt enable output) and the IEI (interrupt enable input) terminals, which are connected into a chain. The priority order is defined as follows: (1) IC7 (PIO1 for internal use); (2) IC6 (PIO2 for external use); IC5 (CTC).

In the basic software, only POI1 and the CTC generate interrupts. The PIO interrupts originate from the RS232 port and/or the PC/XT keyboard. The CTC generates an interrupt every 10 ms, during which, among others, the IR keyboard is checked. Without the pull-up resistor at pin 8, the keyboard buffer would be filled with random characters if the IR remote control is not used. Resistor R23 has a similar function, and prevents unwanted interrupts if IC12 is not fitted.

The connection of the EPROM(s) and the RAM(s) is not entirely straightforward because of the different memory configurations that are allowed. Position IC2 can hold either a RAM or an EPROM, which requires jumpers JP1 to JP5 to be set accordingly. The circuit diagram shows the jumpers set to the 'EPROM' positions (memory configuration '0').

Position IC1 accommodates one of three
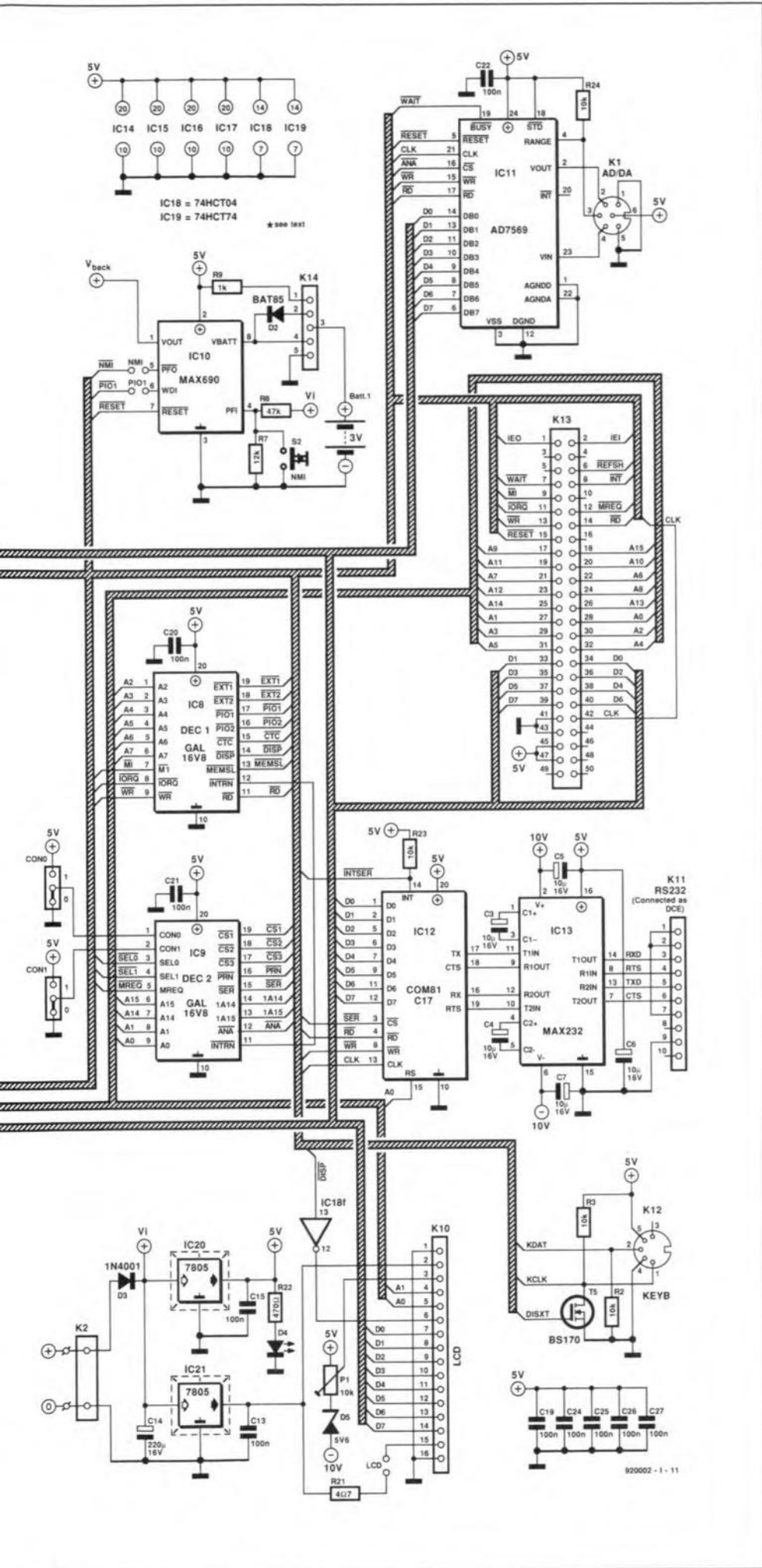
nd low cost.

EPROM types: the 27128, 27256 or 27512, so that address lines A14 and A15 need to be given their appropriate level. These lines are controlled by the memory address decoder located in IC9, a GAL Type 16V8. The configuration is determined directly by the setting of connectors CON0 and CON1. These are pre-set to give the memory configuration shown in Fig. 2a, and determine whether or not address lines A14 and A15 are passed. The GAL also arranges the selection of the three memory components, which, apart from A14 and A15, also depends on the memory configuration and the SEL0 and SEL1 signals furnished by IC19. SEL0 and SEL1 allow you to switch between BANK0 and BANK1 in blocks of 32 KByte (see Fig. 5).

Transistors T1 and T2, and resistors R5 and R6, ensure that the RAMs do not remain selected at power-down, so that their data is available again when the system is switched on. The power supply connections of IC2 and IC3 are connected to pin 1 of IC10, which takes care of the battery backup switch-over function.

The MAX690 watchdog (IC10) switches between 5 V and the battery voltage, U_{batt}, as soon as the voltage at pin 2 drops below ($U_{batt}-50$ mV), or rises above ($U_{batt}+70$ mV). Further, watchdog types MAX690 and MAX694 generate a reset if the supply voltage drops below 4.65 V. Those of you who want a wider margin are advised to use the MAX692, which issues a reset at 4.4 V. Finally, the watchdog supplies a defined reset pulse at power-on (MAX690 and MAX692: 50 ms; MAX694: 200 ms). The input voltage to the card is monitored with the aid of R7 and R8. If the voltage at pin 4 of the watchdog drops below 1.3 V, output $\overline{PFO}$ goes low. Provided the NMI jumper is installed, this low level can trigger a non-maskable interrupt that allows the current situation to be saved before the supply voltage drops below 4.65 V, and IC10 resets the card. This option is supported only by a software hook coupled to the NMI.

Apart from monitoring the supply voltages, the watchdog is also capable of checking if the Z80 card is still running. The watchdog timer monitors the WDI input, to which a signal must be applied that changes at least every 1.6 ms. If this signal fails, the watchdog resets the card. The WDI input may be connected to the selection signal of IC7 via jumper PIO1. Since, if the BIOS is used, the CTC generates an interrupt every 10 ms, and the associated subroutine addresses IC7, the presence of the selection signal is a good sign that the card is still running.

A second GAL, IC8, contains the address decoding logic for the I/O circuits. Here, the advantage of a GAL is a drastic reduction of the chip count for an address decoder that allows the I/O ICs to be addressed fully and without 'image' areas elsewhere in the memory. An address overview of the I/O components is given in Fig. 6.

The analogue interface is built around an AD7569 8-bit A-D/D-A converter. This IC

Memory select	SEL0	SEL1
00000H - 07FFFH	1	x
08000H - 0FFFFH	x	1
10000H - 17FFFH	0	x
18000H - 1FFFFH	x	0

920002-I-17

Fig. 5. Memory selection by means of the SEL0 and SEL1 lines.

I/O addresses	
EXT1	0FCH - 0FFH
EXT2	0F8H - 0FBH
PIO1	0F4H - 0F7H
PIO2	0F0H - 0F3H
CTC	0ECH - 0EFH
DISP	0E8H - 0EBH
RS232	0E6H - 0E7H
PRN	0E5H
ANALOG	0E4H
MEMSEL	0E0H - 0E3H

920002-I-18

Fig. 6. Addresses of the I/O components that are realized with the aid of GALs.

was chosen because it is simple to interface, and reasonably fast: the D-to-A and A-to-D conversion times are 1 μs and 2 μs respectively. Since the $\overline{BUSY}$ signal (which is low during the A-to-D conversion) is connected to the $\overline{WAIT}$ terminal of the CPU, the ADC can be read simply with an IN instruction. Hence, the instruction

IN A,(ANALOG)

directly provides the input voltage as a hexadecimal value in the accumulator (provided, of course, that ANALOG equals the I/O address of the A-D/D-A converter), without the need to arrange the timing for this read operation. Writing to the DAC is equally simple: instruction

OUT ANALOG,A

puts the desired voltage on the output.

Depending on whether the range input is high or low, the input and output voltage range is from 0 V to 2.5 V, or 0 V to 1.25 V. The range input is held high via R24, and can be made low by connecting pin 3 of K1 to ground.

The RS232 interface consists of two ICs: a 20-pin UART (universal asynchronous receiver/transmitter) Type COM81C17, and a level converter Type MAX232. The COM81C17 contains everything to set up a serial interface quite easily. The system clock frequency used enables all standard baud rates between 50 bits/s and 38,400 bits/s to be programmed. In addition, the UART ar-

ranges the handshaking protocol on the serial link, which does away with the need for any software equivalents. The step-up converters contained in the MAX232 ensure RS232 signal levels of +10 V and −10 V, which will work in most, if not all, applications. Connector K11 is wired such that the Z80 card forms a DCE that is readily connected to a DTE (data terminal equipment; a computer in most cases) via a 9-way flatcable.

At this point we have nearly completed our tour along the main components in the circuit diagram. Connector K12 serves to hook up a PC/XT keyboard. Such keyboards are widely available at very low prices from PC surplus outlets. If you happen to have a PC XT/AT type with automatic switching, the Z80 card ensures that it is set to PC XT mode. The keyboard is reset by software following a hardware reset. This is done via transistor T5.

The contrast of the LCD connected to K10 is controlled via preset P1. A back-lighted display may be used in low ambient light conditions. Because of the possible need for a back-light supply, and to keep display multiplexing noise away from the processor, the LCD is powered separately by IC21, while the rest of the circuit is powered by IC20. The back-light supply depends on the LCD type used. There are types that require a supply voltage of 5 V (replace R21 with a wire link), and types that require a certain current (in which case R21 must be given an appropriate value). The back-light connections are pins 15 and 16 of connector K10. The jumper marked 'LCD' provides a simple way of switching the back-light on and off.

The printer datalines are furnished by latch IC16, while the control signals to and from K9 and K9' are buffered by IC17. This IC also buffers the control signals to the two external bus connections. The databases are buffered by IC14 and IC15. The pinning of connectors K7 and K8 is compatible with the universal bus (Ref. 1).

That concludes the description of the Z80 card as far as its concept is concerned. Next month we will tackle the construction and testing of the card, as well as making use of the associated test software contained in the BIOS EPROM. ❑

References:
1. "Relay card for universal I/O interface". *Elektor Electronics* November 1991.
2. "Universal RC5-code infra-red receiver". *Elektor Electronics* January 1992.

Digital Audio/visual system (Multi-purpose Z80 card)

May and June 1992

An extensive description of a modification to the memory backup circuit on the Multi-purpose Z80 card is available free of charge through our Technical Queries service.

FM stereo signal generator

May 1993

Capacitors C17 and C19 should have a value of 33nF, not 3nF3 as indicated in the circuit diagram and the parts list of the multiplex generator.

Workbench PSU

May 1993

The polarity of capacitor C15 is incorrectly indicated on the PCB component overlay (Fig. 5a), and should be reversed. The circuit diagram (Fig. 2) is correct.

Transformer TR2 is incorrectly specified in the circuit diagram (Fig. 2) and in the parts list. The correct rating of the secondary is 2 × 12V/5A. Also note that the secondary windings are connected in series to give 24 V.

Audio DAC

September 1992

The polarity of capacitors C25 and C58 is incorrectly indicated on the component overlay of the D-A board (order code 920062-2), and should be reversed.

CORRECTIONS AND UPDATES

U2400B NiCd battery charger

February 1993

The value of resistors R17 through R27 should be 2.7kΩ, not 12.7kΩ as stated in the parts list.

VHF/UHF receiver

May 1993

In Fig. 4, the connections to ground of the AF amplifier outputs, pins 5 and 8, should be removed. The amplifier outputs are connected to the loudspeaker only. The relevant printed circuit board is all right.

COMPACT MAINS POWER SUPPLY

Design by A. Roßrucker

THE proposed mains power supply is a versatile unit for use where a stable voltage, medium power and good parameters are required. The quality of its output is easily comparable to that of good-quality commercial products, but it is considerably less expensive than those units.

The circuit

The circuit of the supply is just as compact as its mechanical design: a transformer, a rectifier, two ICs and some additional passive components are all that is required. The design is based on IC_1, a 5-pin, voltage regulator Type L200 with integral, presettable current limiting and thermal overload protection.

To ensure correct regulation of the output voltage, the device has an internal 2.75 V reference source. The voltage at pin 4 is compared with the reference voltage to enable the correct level of output voltage, U_o, to be set with potential divider R_3-R_4-P_1. With values as shown in Fig. 1, the output voltage can be set between 5 V and 26 V with P_1.

It should be borne in mind that the maximum input voltage to IC_1 is 40 V and the maximum difference between its input and output voltage is 32 V. That means that the secondary voltage of the mains transformer must not exceed 24 V≈. This gives an unregulated voltage input into IC_1 of 32 V, resulting in a maximum output voltage of 24 V. To set P_1 for an output voltage >24 V would not be a good idea, because the regulation at fairly high output currents would then no longer function correctly, owing to the inadequate voltage reserve. The result would be an unacceptable 100 Hz ripple on the output.

To enable correct functioning of the integral current limiting, the voltage drop across R_2, connected between pins 2 and 5 is monitored; when it reaches 450 mV, current limiting begins. The maximum output current, I_o, is therefore given by

$$I_o = 450 / R_2 \text{ (mA)}.$$

With $R_2 = 0.22 \ \Omega$ as in the diagram, the maximum output current is thus 2 A.

Voltage monitoring

The voltage monitoring circuit is based on IC_2. When the load draws too high a current, the current limiting in IC_1 operates, resulting in a drop in the output voltage. This reduction is detected by IC_2, which then causes D_3 to light. Even very brief drops in the output voltage are indicated by this LED for a period, t, that depends on the capacitance of C_5 and may be calculated from

Virtually all electronic circuits need some sort of power supply, often a high-quality one. For the latter, if an output current of not more than 1.5 A and an output voltage of 5–20 V are required, the supply described here is ideal. Its design is compact: even the transformer and heat sink are housed on the printed-circuit board. It provides overload indication, current limiting and protection against short-circuits.
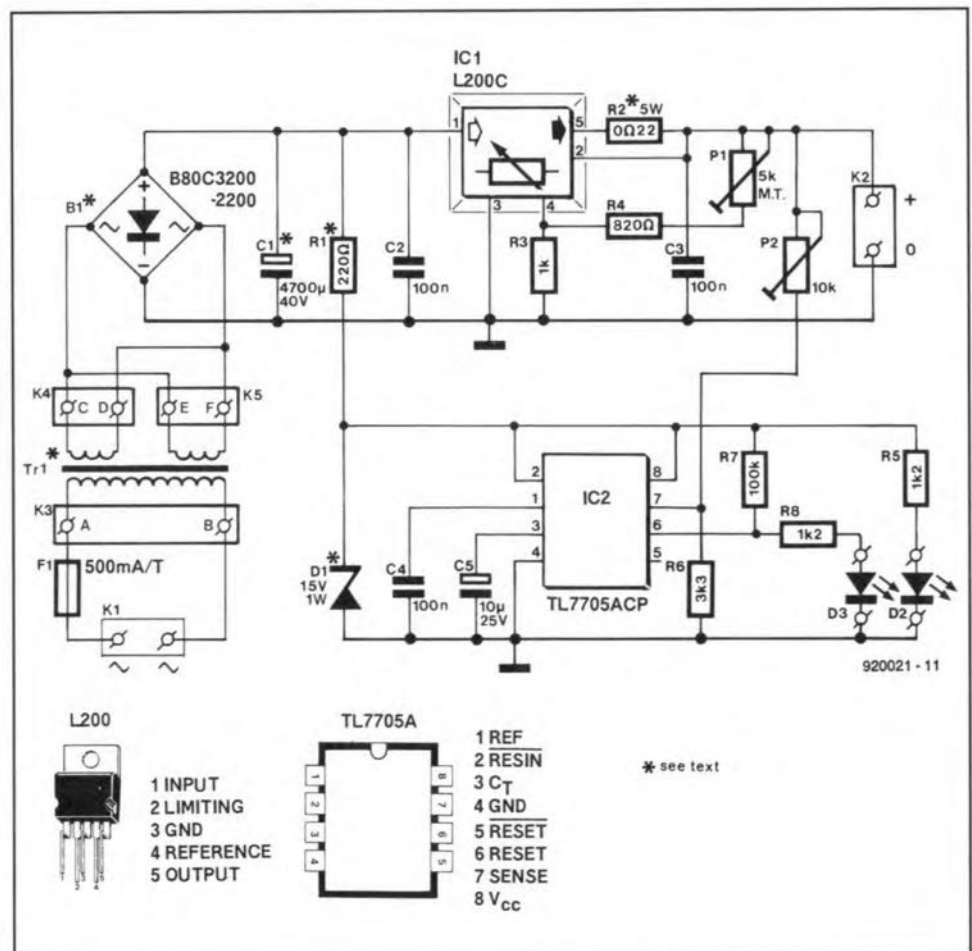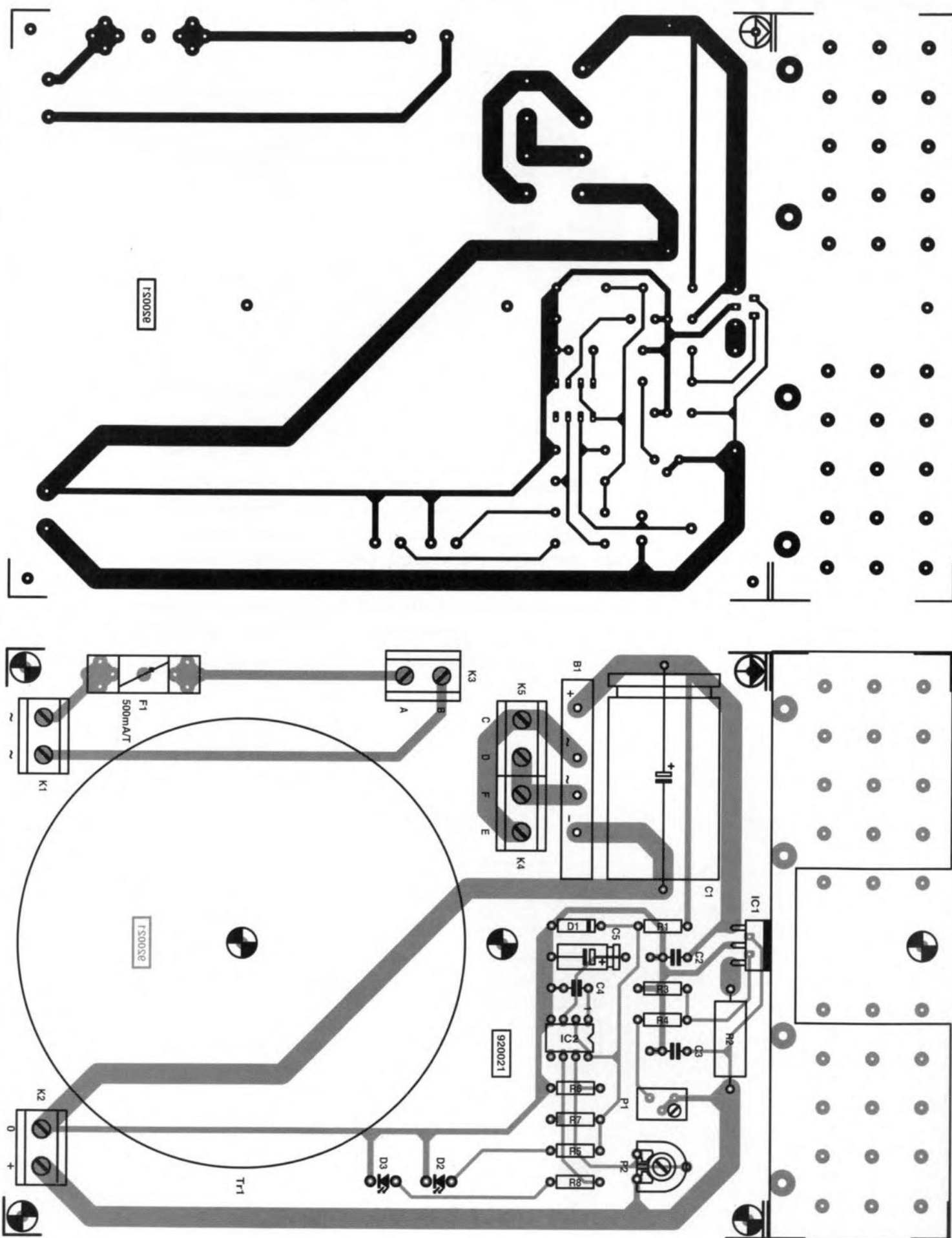
Fig. 1. Circuit diagram of the compact mains power supply.

Fig. 2. Printed circuit board for the compact mains power supply.

$t = 0.013C_5,$

where t is in seconds and C_5 in µF. With $C_5 = 10$ µF as in the diagram, the LED will light for 0.13 s. If a longer period is required, the value of C_5 must be increased.

In normal operation, the potential at pin 7 of IC_2 is 4.55 V. When that voltage drops below this value, D_3 lights. The level of the output voltage at which D_3 begins to light is determined by voltage divider R_3–P_2. With component values as in Fig. 1, the output voltage can be set to 4.55–26 V with P_2.

Since IC_2 was originally designed for use in computers, it also causes D_3 to light briefly when the supply is switched on. Also because of its origins, the device must not operate with voltages above 18 V; that is why R_1–D_1 limits the voltage to 15 V. That voltage results from transformer secondary voltages of 12 V≈ and higher. If, therefore, a transformer is used with a 12 V secondary, D_1 may be omitted and R_1 replaced by a wire link.

Diode D_2 and series resistor R_5 serve purely to indicate whether the supply is switched on.

If neither voltage monitoring nor supply-on indication is required, IC_2, D_1–D_3, R_1, R_5–R_8, C_4 and C_5 may be omitted. The supply functions perfectly satisfactorily without these circuits.

Transformer

Before the components for the mains supply are bought, it should be decided what level

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PARTS LIST

Resistors:
R1 = 200 Ω*
R2 = 0.22 Ω*
R3, R5, R8 = 1.2 kΩ
R4 = 820 Ω
R6 = 2.2 kΩ
R7 = 100 kΩ
P1 = 10 kΩ multi-turn preset
P2 = 10 kΩ preset for PCB mounting

Capacitors:
C1 = 4700 µF, 40 V*
C2–C4 = 100 nF
C5 = 10 µF, 25 V, horizontal

Semiconductors:
B1 = B40C3200/2200*
D1 = zener diode 15 V, 1 W*
D2 = LED, green
D3 = LED, red
IC1 = L200, Pentawatt housing
IC2 = TL7705

Miscellaneous:
K1–K5 = 2-way terminal block, 7.5 mm grid
F1 = 500 mA fuse, slow acting
Fuse holder for PCB mounting
Tr1 = toroidal transformer*
Heat sink for IC1
PCB Type 920021

* See text

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of output voltage is, or will be, required. It would not make much sense to fit a 24 V transformer and then set P1 permanently for 5 V output. The consequent dissipation in IC_1 would be high, whereupon load currents of up to 2 A would not be available, since the integral thermal protection circuit would limit the output current. Component values differing from those in the parts list and on the diagram are, therefore, given below for the most usually required output voltages.

■ **5 V:**
$Tr_1 = 8$ V secondary; $R_1 =$ wire link; D_1 is not required; $C_1 = 16$ V.
■ **6 V:**
$Tr_1 = 8$ V secondary; $R_1 =$ wire link; D_1 is not required; $C_1 = 16$ V.
■ **9 V:**
$Tr_1 = 9$ V secondary; $R_1 =$ wire link; D_1 is not required; $C_1 = 25$ V.
■ **12 V:**
$Tr_1 = 12$ V secondary; $R_1 =$ wire link; D_1 is not required; C1 = 25 V.
■ **15 V:**
$Tr_1 = 15$ V secondary; $R_1 = 220$ Ω; $C_1 = 25$ V.
■ **18 V:**
$Tr_1 = 18$ V secondary; $R_1 = 330$ Ω, $1/2$W; $C_1 = 40$ V.

It should be borne in mind when ordering the transformer that the alternating secondary current should be about ×1.4 the desired direct output current. At the same time, the value of R_2, the rating of C_1 and the current rating of B_1 should be considered. Component values and ratings differing from those stated in the parts list or on the circuit diagram for a number of load currents are given below.

■ **500 mA:**
$Tr_1 = 700$ mA; $R_2 = 0.82$ Ω, 1 W; $C_1 = 1000$ µF; $B_1 =$ B40C1000.
■ **650 mA:**
$Tr_1 = 1$ A; $R_2 = 0.68$ Ω, 1 W; $C_1 = 2200$ µF; $B_1 =$ B40C1000.
■ **800 mA:**
$Tr_1 = 1.2$ A; $R_2 = 0.56$ Ω, 1 W; $C_1 = 2200$ µF; $B_1 =$ B40C1500.
■ **950 mA:**
$Tr_1 = 1.5$ A; $R_2 = 0.47$ Ω, 1 W; $C_1 = 2200$ µF; $B_1 =$ B40C2200/1500.
■ **1.15 A:**
$Tr_1 = 1.7$ A; $R_2 = 0.39$ Ω, 1 W; $C_1 = 2200$ µF; $B_1 =$ B40C3200/2200.
■ **1.35 A:**
$Tr_1 = 2$ A; $R_2 = 0.33$ Ω, 5 W; $C_1 = 4700$ µF; $B_1 =$ B40C3200/2200.
■ **1.5 A:**
$Tr_1 = 2.2$ A; $R_2 = 0.27$ Ω, 5 W; $C_1 = 4700$ µF; $B_1 =$ B40C3200/2200.

It is, of course, important that the transformer fits on to the PCB, which has been designed for a toroidal type. Apart from causing little or no interaction with adjacent components and circuits, this type of transformer fits more readily on to a PCB.

It is not necessary for the transformer to have only one secondary winding; indeed, toroidal transformers with two secondary windings are often more easily available. For instance, a 12 V / 2 A supply would work perfectly well with 2×12 V / 1.4 A secondary windings, which are then connected in parallel. Provision for this is already made on the PCB (K_4 and K_5 in Fig. 1 and Fig. 2). Obviously, a transformer with 2×6 V / 2.8 A secondaries would also be fine: the secondaries are then connected in series.

Construction and testing

When all the components have been selected and bought, construction can be started. Begin with the resistors and terminal strips, followed by the fuse holder, capacitors, diodes, rectifier and the two ICs. The transformer comes last. Make sure that the enamel has been removed from the ends of the wires that are inserted into the terminal strips.

Regulator IC_1 must be fitted on to a heat sink without insulating washer but with some heat conducting paste. The heat sink will be at earth potential, since the housing of IC_1 is internally connected to pin 3.

When the board is finished, set P_2 to maximum resistance, that is, fully anti-clockwise, as a precaution to prevent the potential at pin 7 of IC_2 exceeding the maximum permissible level of 10 V.

Connect the mains supply to the board, whereupon D_2 should light permanently and D_3 briefly. The output voltage can then be set to the desired value with the aid of P_1.

The voltage monitoring circuit is preset by first turning P_2 until D_3 just lights and then turning it till D_3 just goes out. Because of the time-constant, P_2 should be turned very slowly.

If the transformer hums and the fuse blows, either C_1 is connected with incorrect polarity or the two secondary windings of Tr_1 have been connected in anti-parallel instead of parallel.

If there is no output voltage, it is likely that the two secondary windings of Tr_1 that should have been connected in series are, in fact, linked in anti-series.

Do not connect two of these power supplies in parallel. However, connecting them in series to obtain a higher output voltage is perfectly all right. It is also possible to use two power supplies to construct a symmetrical supply.   ■
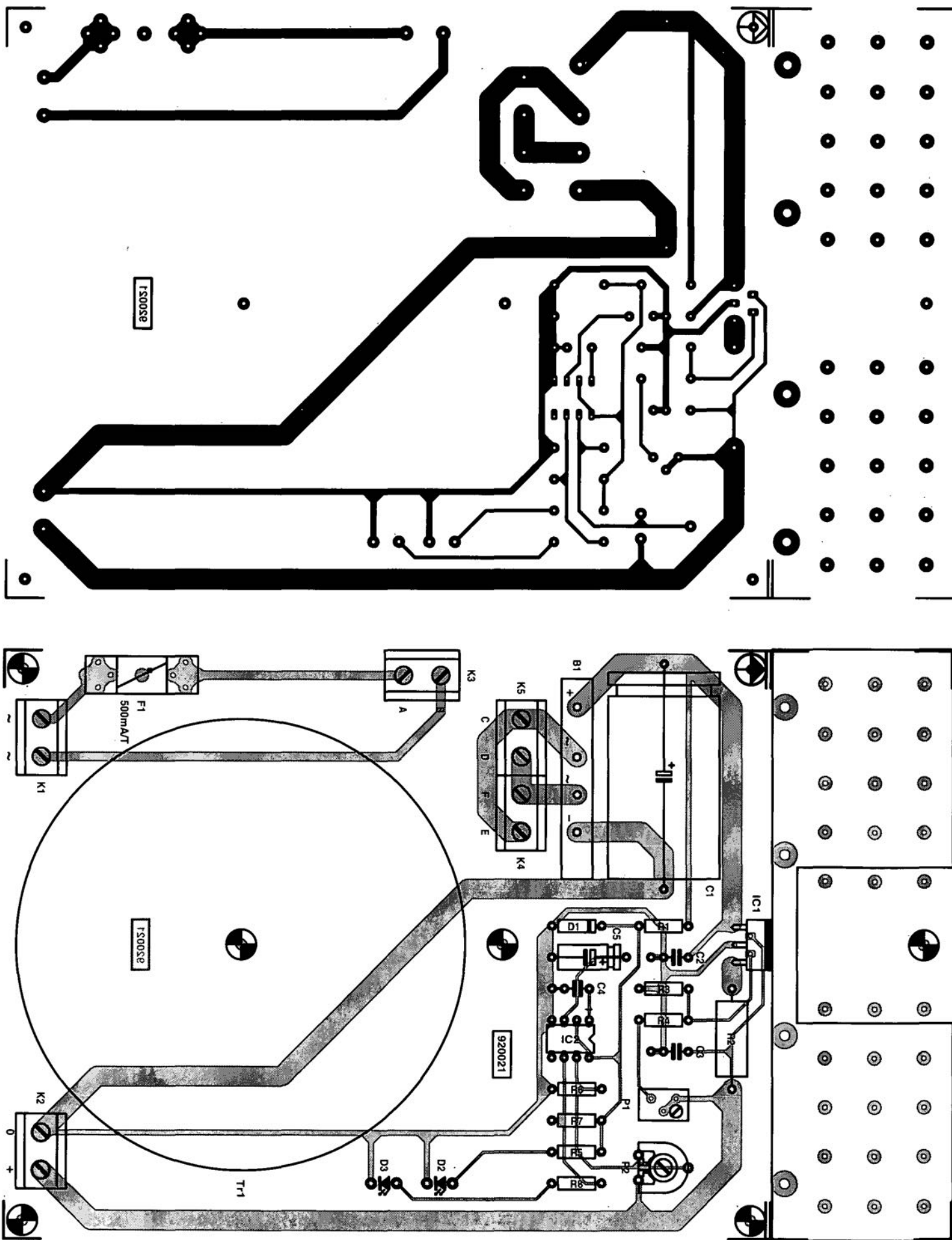
Fig. 2. Printed circuit board for the compact mains power supply.

1.3 GHZ PRESCALER

Design by P. Esser

Not only do the majority of frequency counters found in smaller workshops and laboratories not operate above 10 MHz, but usually they cannot be modified to work at higher frequencies either. To overcome that problem, here is a prescaler that delivers a clean rectangular signal at TTL level at frequencies up to 1.3 GHz and which can be used with virtually any frequency counter.

THE prescaler proposed here offers several advantages. Firstly, it increases the measurement range of the frequency counter to which it is linked and, secondly, it makes it possible to use a much shorter cable between counter and instrument on test—see Fig. 1. A disadvantage is, of course, that, to see the selected metering range, you must look at both the counter and the prescaler.

Scaler ICs

A first scaling down of the input signal is effected by a chip specially designed for this purpose. This can be either the Telefunken Type U664B or the Siemens Type SDA4211. Block diagrams of these circuits are shown in Fig. 2.

The U664B was originally developed for use in the frequency synthesizer of a television receiver. Without any additional components, it divides by 64. In the absence of an input signal, it operates in the highest frequency range. Normally, the only external components required are two small capacitors.

The SDA4211 offers two scaling factors: 64 or 256, depending on the potential at pin 5. If that pin is at +5 V, the input signal is divided by 64; when the pin is at earth, scaling is by 256. On the PCB,—see Fig. 4— this selection is facilitated by a 3-way terminal strip and a jump link.

The two circuits are fully interchangeable as regards pinout and function, but not, of course, in scaling factor.

Two paths

The measured signal (frequency f_s) is split into two immediately after the input socket—see Fig. 3. One part is fed to the prescaler proper (lower part of the diagram) via C_4, while the other is taken to a processing and amplifying section (upper part of the diagram) via L_1.

Anti-parallel connected diodes D_2 and D_3 limit the level of the input signal to not more than ±700 mV. The signal is then applied to pin 2 of IC_3. The symmetrical input of this circuit is connected asymmetrically, since the second input, pin 3, is connected to ground via C_{11}. Jumper JP_1 is the earlier mentioned scaling selector if the SDA4211 is used. If the U664B is used, the 3-way terminal strip and

jump link are not required.

The measured signal (frequency f_s:64) is available at pin 6, from where it is applied to potential divider R_7-R_8-P_1. From there it is fed to amplifier T_3, whose output is applied to the first of three cascaded Type 74LS90 decade counters, IC_4, IC_5, and IC_2.

Each of these counters divides its input signal by 2.5. This somewhat unusual scaling factor comes about as follows. The upper half of the IC divides by 5. For every five input pulses, the Q_8 output goes high twice; in other words, the Q_8 output delivers an output pulse for every 2.5 input pulses. The out-

put of the cascaded threesome is thus a signal of frequency f_s:1000.

The other part of the input signal is applied via L_1 and C_2 to T_1, which, connected as an common-emitter circuit, behaves exactly like an inverting opamp. The voltage amplification of the stage is roughly the same as the open-loop amplification of the transistor, but it is dependent on the source impedance. Diode D_1 limits the negative half of the signal to not more than –700 mV.

The output of the stage is taken from the collector of T_1 and then further amplified in T_2, which is also connected as a common-emitter circuit. It is then taken from the collector of T_2 and applied to NAND Schmitt trigger IC_{1b}, which, with the other three NAND gates, ensures clean edges and correct gating of the two signals. When switch S_1 is open, the original signal (f_s) is available at the output; when it is closed, the scaled down signal (f_s:1000) is at the output socket.

Construction

Populating the printed-circuit board shown in Fig. 4 is straightforward, but greater care than usual is required around the input socket where surface-mount components are used. Inductor L_1 must be wound by the constructor. It consists of 2–3 turns enamelled copper wire (dia. 0.4 mm) on a small ferrite core.
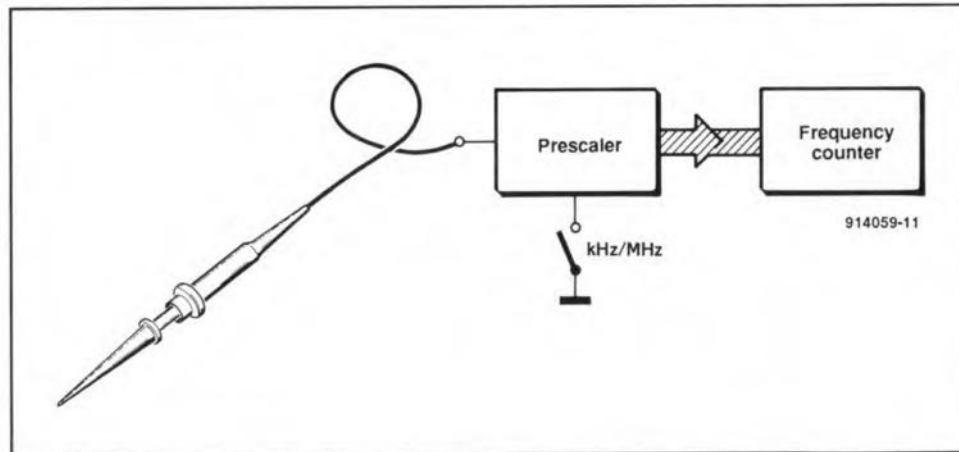

Fig. 1. Measuring set-up of counter, prescaler and probe.
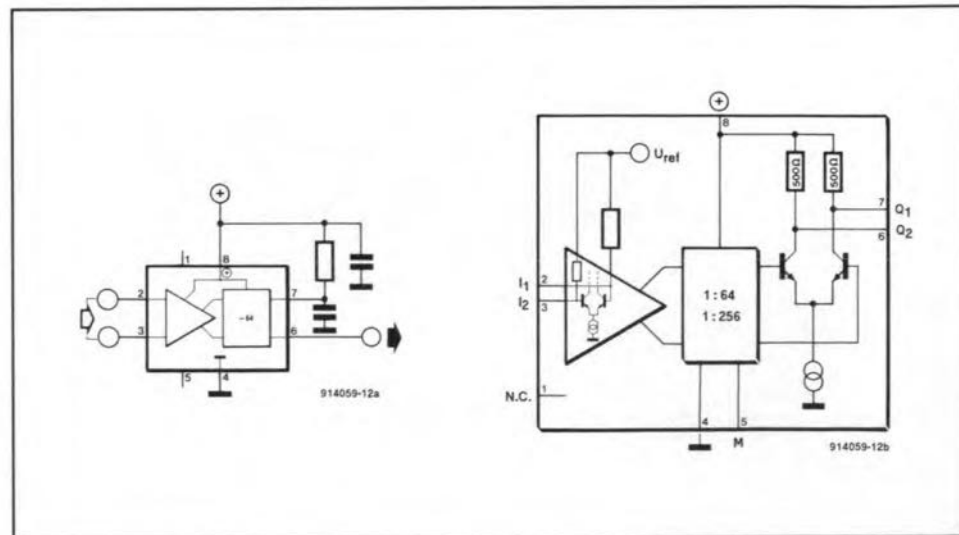
Fig. 2. Circuit diagram of the U664B (left) and the SDA4211 (right).

The input socket is a BNC type for PCB mounting; this obviates the need of screened cable at the input.

If the SDA4211 is used (IC$_3$), the link at JP$_1$ should connect the +5 V line to pin 5 of IC$_2$. If the U664B is used, the jumper should not be used. Nothing more can go wrong here than the scaling factor. ∎

Brief specification

- Two switchable measurement ranges: 1:1000
- Upper frequency limit 1.3 GHz
- Input sensitivity <100 mV
- Compact, economical design
- Power supply 5 V
- Single board construction

Fig. 3. Circuit diagram of the 1.3 GHz prescaler.

Clock	74LS90 ouputs			
	Q_A	Q_D	Q_C	Q_B
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	1	0	0	0
6	1	0	0	1
7	1	0	1	0
8	1	0	1	1
9	1	1	0	0

Fig. 4. Printed circuit board for the 1.3 GHz prescaler.

PARTS LIST

Resistors:
R1, R3 = 1 kΩ
R2, R4 = 47 kΩ
R5 = 390 Ω
R6 = 560 Ω
R7 = 150 Ω
R8 = 2.2 kΩ
R9 = 330 Ω
P1 = 10 kΩ preset, horizontal

Capacitors:
C1 = 10 µF, 16 V
C2, C3 = 1 µF
C4 = 120 pF, surface mount
C5 = 1 nF, surface mount
C6–C10 = 10 nF
C11 = 820 pF, surface mount

Semiconductors:
D1 = 1N4148
D2, D3 = BAT81, BAT82 or BAT83
T1, T2 = 2N918
T3 = BF324
IC1 = 74LS132
IC2, IC4, IC5 = 74LS90
IC3 = U664B or SDA4211

Miscellaneous:
L1 = see text
S1 = single-pole on/off switch
K1 = BNC socket for PCB mounting
JP1 = 3-way terminal strip
PCB 914059

The input socket is a BNC type for PCB mounting; this obviates the need of screened cable at the input.

If the SDA4211 is used (IC$_3$), the link at JP$_1$ should connect the +5 V line to pin 5 of IC$_2$. If the U664B is used, the jumper should not be used. Nothing more can go wrong here than the scaling factor. ∎
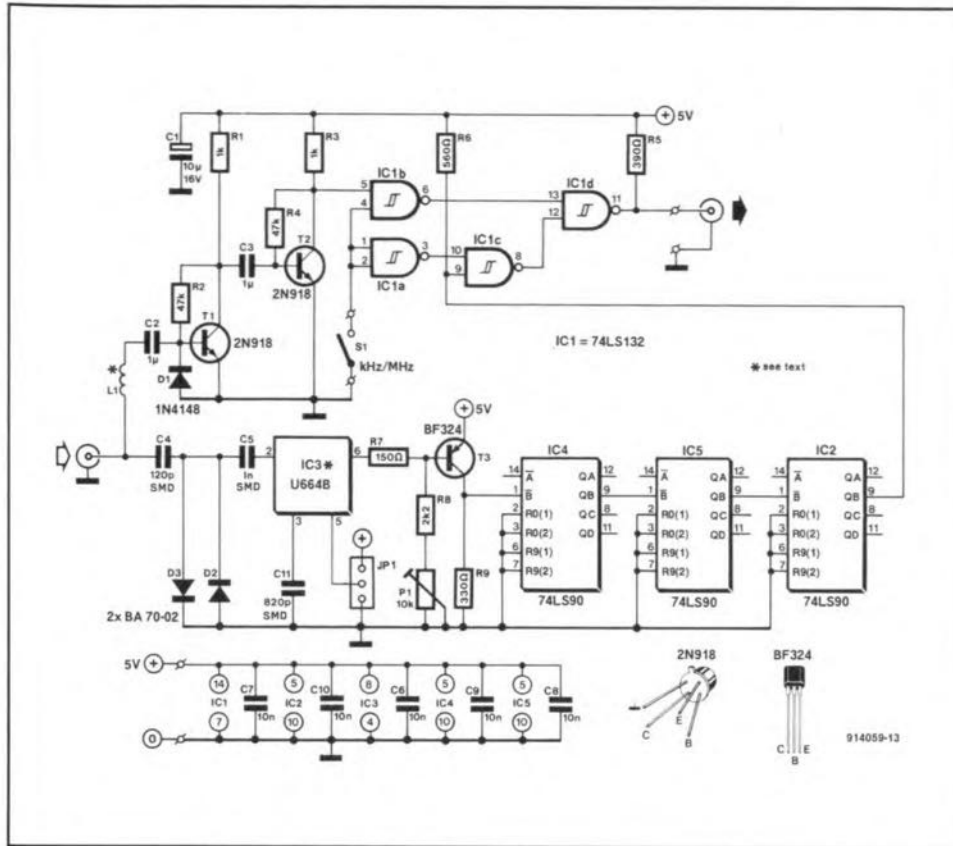
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6	1	0	0	1
7	1	0	1	0
8	1	0	1	1
9	1	1	0	0

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PCB 914059

ELEMENTS OF PASSIVE ELECTRONIC COMPONENTS

PART 1: THE INDUCTOR

by Steve Knight, B.Sc.

IF you don't ponder things too deeply, it might appear as if the whole edifice of electronics is supported solely by the transistor and the chip, just as once it was supported by the thermionic valve. But a fat lot of good these dynamic components would be if it weren't for the passive Cinderellas of resistance, capacitance and inductance. In other words, a stick of carbon, two pieces of metal separated by some sort of dielectric and a length of wire fashioned into a helix. Not an impressive picture in terms of the actual make-up of these components, to be sure, but their physical behaviour, when examined carefully, more than makes up for their apparently simple physical construction.

Let us look particularly at the humble inductor, a much neglected component on the electronics scene, and see what properties it possesses to make it just as important as its often more glamourized partners.

When an electric current flows in a wire, one of its most important manifestations is the establishment of a magnetic field in the immediate vicinity of the wire. This field is composed of so-called lines of magnetic force or magnetic flux, which takes the form of concentric circles around the wire that lie both within and outside the conductor. Figure 1 shows the kind of field set up and how the directions of current and lines of force are related. Strictly, of course, the concentric circles are concentric tubes and the field is at its most intense, that is, has its greatest flux density, at the surface of the conductor. This intensity falls off as the distance from the conductor increases, which is indicated on a magnetic field diagram by the variations in line spacing. We notice, too, that lines of force always form closed loops whatever the situation. A magnetic line doesn't sud-denly come to a stop with nowhere to go. The direction in which the magnetic force would act on an isolated north pole placed within the field is indicated by the arrowheads; this direction reverses if the current in the conductor is reversed. Keep in mind, of course, that the concept of lines is a conventional

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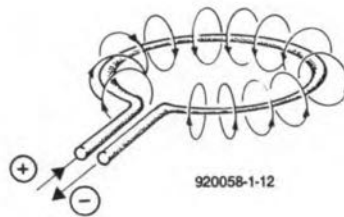
fiction; a real field does not have barren spaces between the lines. We simply use them as a convenient way of representing magnetic field densities and nowadays these are not measured in lines (as they once were) but in terms of the electromagnetic effect the field will produce.

If the wire carrying the current is formed into a loop, rather as shown in Fig. 2, the lines of force all pass through the loop in the same direction. A conventional coil of wire, or solenoid as it is usually called, is nothing more than a number of continuous loops, and a current flowing in such a coil establishes the lines of force in a lengthwise direction through the centre of the coil, emerging from the end and completing their circuits through the surrounding medium. Figure 3 shows how the concentric loops merge together to give a resultant field of considerable intensity, rather as the field surrounding a permanent bar magnet (of iron filings memory!) displays

its characteristic pattern. Like the bar magnet, too, the field around a current-carrying coil exhibits a north and a south pole; these poles change place when the current in the coil is reversed. The field vanishes when the current flow ceases.

It is the appearance—and the disappearance—of the field established around a current-carrying conductor that determines the whole phenomenon of electrical inductance.

Self inductance

So, what do we mean by inductance, anyway? Well, let us return to Fig. 2. If the magnetic flux caused by the current in a single loop of wire is looked at closely, it is seen that every line must pass through the loop somewhere or, put into other words. every line must 'link' with the loop. The number of lines enclosing the loop in this way are referred to as the flux linkages and in this basic example the number of such linkages must be the same as the number of flux lines.

Now, thinking about the flux associated with the solenoid of Fig. 3, we see that the majority of the lines link with every turn of the coil, although there are those that link with a few of the turns only.

If we consider each turn separately, the total linkages with the coil consist of the summation of the number of lines linking each

1

direction of current

direction of lines of force

right hand

direction of lines of force

direction of current

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3

Current

920058-1-13

4

920058-1-14
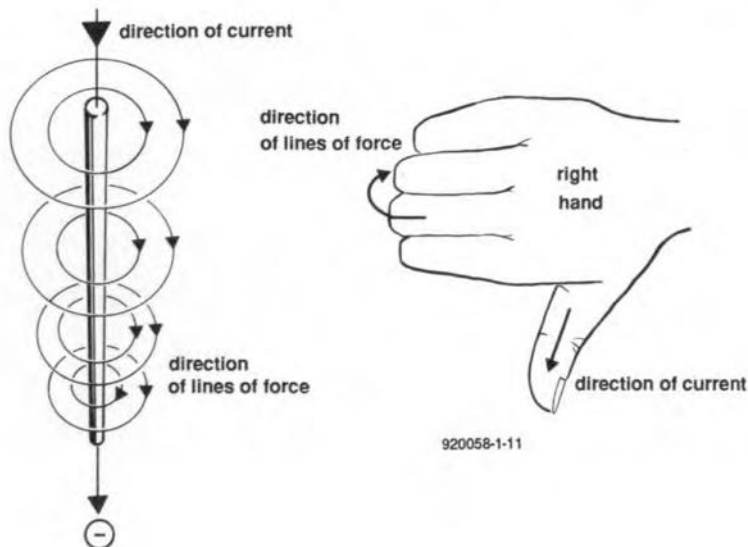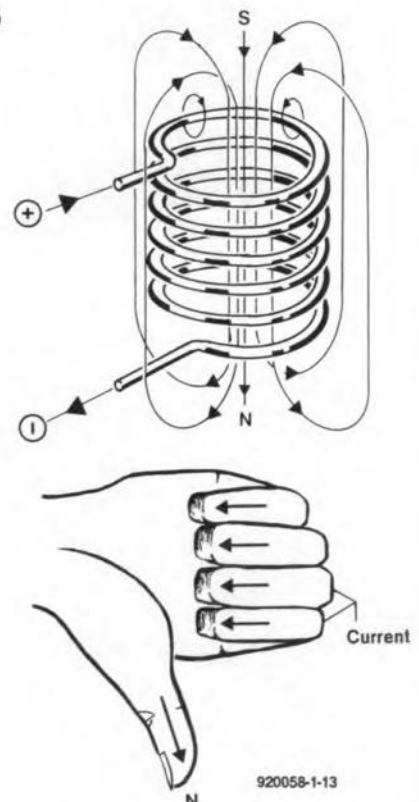
turn and it is now evident that this total is much greater than the number of flux lines. Flux linkage, then, is simply the flux multiplied by some constant that itself depends upon the shape, the closeness of the turns and the physical dimensions of the circuit, that is, the opportunities that exist for the flux to link with as much of the circuit as possible.

Since the total flux is proportional to the current, so also will be the total flux linkages; hence, we can say that the ratio flux-linkage to current is constant for any given circuit arrangement. This constant is the self-inductance of the circuit and is symbolized by the letter L.

Now, a bold statement of this sort is likely to leave the majority of us a bit frustrated. So, to get our teeth into the problem, let us have a brief look at the work of Michael Faraday and see what effect the electromagnetic field associated with a solenoid has on its surroundings.

Mutual inductance

Faraday used a circuit rather like that shown in Fig. 4. Here we have the coil of Fig. 3 in a circuit consisting of a switch S and a source of e.m.f., battery B. We call this coil the primary winding. In close proximity to this primary winding there is another coil, the terminals of which are connected to a current sensing meter, G. This coil is the secondary winding. Faraday noticed that as long as a *steady* current was maintained in the primary winding, that is, as long as the field surrounding this coil remained constant, there was no deflection on the meter. When, however, switch S was opened or closed, there was a transient deflection, a momentary flick of the pointer that returned quickly to zero as the field either established itself to a constant value (switch closed) or collapsed from a value to zero (switch open). Faraday de-

duced that whenever flux linkages between the two circuits were changing, a current flowed in the circuit of the secondary winding., and this in turn im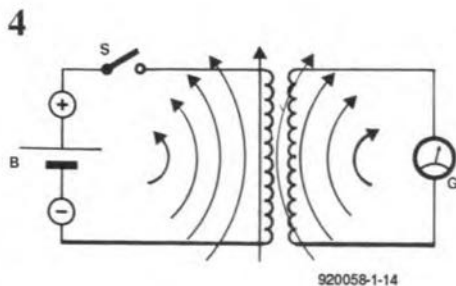plied that an e.m.f. must be acting on it. On top of this, the meter deflections were in opposite directions according as switch S was being closed or opened; that is, the current flowed (and the e.m.f. acted) in opposite sense according as the flux linkages between the coils were increasing or decreasing.

This little bit of electrical history, easy to appreciate in retrospect, illustrates the phenomenon of electromagnetic induction: the current in the secondary winding is an induced current and the e.m.f. producing it is an induced e.m.f. A changing field always sets up an e.m.f. in any conductor situated within the field.

On this basis, the question naturally arises as to whether any corresponding effect occurs when the magnetic field associated with the secondary winding, set up by the *induced* current, interacts with the primary winding. We have seen that the direction of the induced e.m.f. depends on whether the change in the mutual flux linkages is increasing or decreasing. The current induced in the secondary winding will set up a magnetic field of its own and this will provide linkages with the primary winding. These linkages may either increase or reduce the total linkage between the coils according to the direction of the secondary current. Now, it is found that when the mutual flux linkages caused by the primary current are increasing (S being closed), the secondary current flows in that direction which *reduces* the total mutual linkages. Conversely, when the current in the primary winding is falling (S being opened), the direction of the secondary current is such that the mutual linkage is increased. We can interpret this as an attempt by the current in the secondary coil to keep the flux linkage constant, whether the current in the primary is increasing or decreasing.

So, what we have in effect is a kind of electrical inertia; both a rise and a fall in the circuit current are resisted by the appearance of an induced voltage that works to maintain the existing conditions.

What about a single coil on its own? Does the same thing happen there? Consider the primary coil of Fig. 4 to be on its own. As soon as S is closed, the magnetic field builds

up and sweeps outwards from the turns of the coil; in doing this, it must induce a voltage in any conductors situated within the field and that includes the coil which is producing the changing field. Hence, as the linkages are increasing in the coil after the switch is closed, the induced e.m.f. acts so as to oppose the increase, that is, it opposes the e.m.f. of the battery which is endeavouring to send current through the coil. This effect is known as the back-e.m.f. of self-induction: as one of my teachers put it many years ago, all inductors have suicidal tendencies. Thus, the current in an inductive circuit does not assume instantaneously the value it would have if this were calculated by Ohm's law, that is, on the basis of the *resistance* of the inductor. This must not be confused with inductance.

Similarly, when the switch is opened, on an Ohm's law calculation, the current should fall immediately to zero, but this does not happen. As the current falls, the magnetic energy stored in the field must decrease proportionally, and an e.m.f. is induced in the coil that this time tends to prevent the reduction in flux linkages. The manner in which the current changes in the circuit for both switch-on and switch-off is illustrated in Fig. 5, which also shows the corresponding changes in a circuit containing pure resistance only.

Conservation of energy

The effects of inductance accord with the principles of the conservation of energy. Nature never gives us something for nothing: every bit of energy in a system has to be accounted for in one way or another. In the coil, the magnetic energy is caused by the current and that current in turn is derived from the chemical energy stored in the battery. While the current is steady, the magnetic field and hence the magnetic energy stored in the field will remain constant and the only energy drawn from the battery is that of heat energy, which is dissipated in the resistance of the coil. If the battery voltage is increased, the current, in accordance with Ohm's law, should increase in proportion. This involves an increase in magnetic energy, but while this transformation from chemical to magnetic energy is taking place, *all* the chemical energy cannot change immediately into heat energy. Thus, the current cannot change immediately to a new level as dictated by Ohm's law, that is, on the grounds that all the energy supplied by the battery is converted to heat. The back-e.m.f. is consequently the effect that limits the current to a smaller value; once the magnetic field is established at its new level, the current reaches its greatest value and the back-e.m.f. vanishes.

In the same way, when the current is switched off, it should, in accordance with Ohm's law, fall immediately to zero, since no more energy is being supplied from the battery. But, as the current falls, the energy stored in the field must also fall proportionally, that is, it must be transformed into another form. This transformation is actually to heat energy in the circuit conductors and takes the form of

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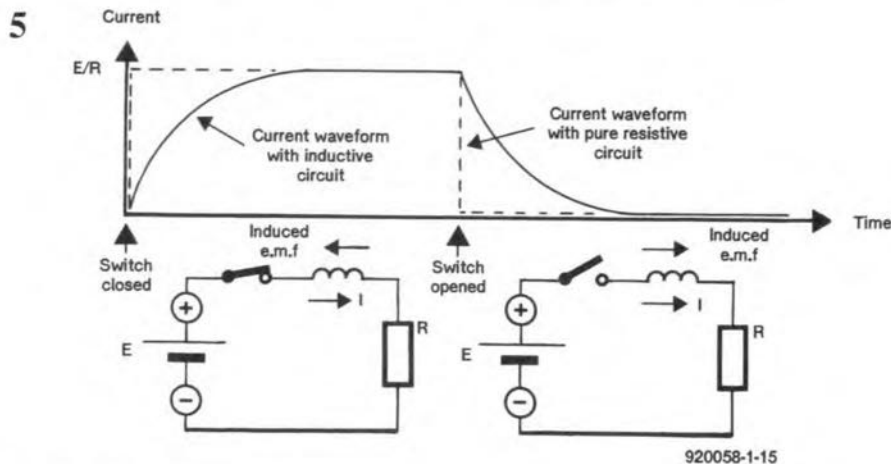
an e.m.f. that tends to maintain the current flow and permit the conversion to heat to take place.

It should be obvious that the greater the time rate at which the current changes, the more rapidly the corresponding changes in magnetic energy must occur and the greater the induced e.m.f. will be. This is embodied in Faraday's law which states that the induced e.m.f. is equal to the product of inductance and rate of change of current. The unit of inductance is the *henry*, H, named after Joseph Henry (1797–1878), the American physicist and pioneer of electromagnetism, who was a contemporary of Faraday. Sub-units are the millihenry, mH, and the microhenry, μH. A circuit has a self-inductance of 1 H when the current through it changes at the rate of 1 A sec^{-1} and causes an induced e.m.f. of 1 V.

Types of inductance

Broadly speaking, inductances as found in general electronics may be classified as (a) coils that have very large inductance values in the minimum of space and reasonably large current-carrying capacity—these types usually have iron cores and take the forms of power transformer or choke, or armature and field coil in motors and generators; (b) coils used in circuits of radio and television receivers, small transmitters and general amplifier systems. The latter types generally consist of relatively small windings wound on non-ferrous supports such as paxolin or polystyrene tubing or, in some cases, as self-supporting coils in air. They have inductances of at most a few hundred millihenries and normally carry only small radio-frequency currents.

In the case of air-cored inductors, the inductance for a given configuration will be constant since the field is set up in a non-ferrous region, which cannot be 'overloaded' or saturated with magnetism. For coils wound on iron cores, the inductance is roughly constant for small values of direct current, but beyond a certain point, the iron saturates and there is no further increase in the field intensity with an increase in the magnetizing force. The inductance of iron-cored chokes is usually stated at a specified level of current, for instance, 10 H at 100 mA.

The other commonplace coil with a closed

iron core is the low-frequency transformer. This may use the conventional laminated stack of iron or be wound on a toroid or 'anchor' ring circuit.

7

Shape factor $X = \dfrac{R}{l+D}$

920058-1-17
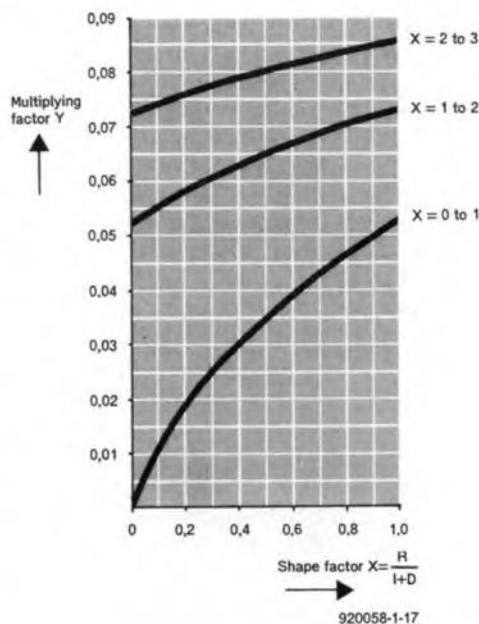
As in the case of Faraday's experiment, transformers depend for their action on mutual inductance. Two coils are wound in close proximity on a common core as shown in Fig. 6. If a current flows in the primary winding, some of the lines of flux established in the core will link with the turns of the secondary winding. The actual linkages between the coils will depend on the current in the primary winding and the positions of the two coils relative to each other. Because of the closed iron core, the linkages are very high and the field is confined closely to the iron circuit. The number of linkages with the secondary winding caused by the current in the primary winding is thus a mutual function of the two circuits.

Circuits of this sort have a mutual inductance of 1 H if the e.m.f. induced in one of them is 1 V when the current in the other is changing at the rate of 1 A sec^{-1}.

Iron cores act as conducting paths as far as the magnetic fields set up in the coils are concerned: hence, an e.m.f. is induced in the core material of a choke or transformer whenever it is operating from an alternating current, a.c., supply. This causes random (eddy) currents to circulate within the core, which in turn creates heating and, therefore, a loss of efficiency. Such currents are reduced by laminating the cores and re-

stricting the currents to small and isolated regions of the core.

In the years leading up to the Second World War, the tuning of circuits at radio frequencies was carried out almost universally by fixed inductors and variable capacitors. Owing to eddy current and other losses, it was then not practicable to use iron-cored inductors at high frequencies, although audio frequency range transformers were available with very thin 'radio metal' laminations and sectionalized windings. Low-loss cores, the so-called ferrites or 'dust-iron' cores, have since been developed and are now commonplace as tuning slugs, which make it possible not only to adjust the inductance, but also lead to very compact forms of r.f. tuning coil.

Winding inductors

Unless there is an inductance bridge available, winding an inductor to a specified value of inductance is a bit of a hit-and-miss affair. Inductance is proportional to the square of the number of turns, N^2, so that, if the number of turns is doubled, the inductance increases four-fold. Other factors that affect the inductance are the length and diameter of the winding, the spacing of the turns, whether the coil is a single-layer or multilayer type, and the core material.

Provided the coil is air-cored, it is not difficult to estimate with reasonable accuracy the inductance of a coil that is close-wound in a single or multiple layer. This is where the curves of Fig. 7 come in. These graphs take care of the factors relating to coil length and radius as well as the depth of the winding or the diameter of the wire. Figure 8 shows these measurements made with respect to a single-layer coil at (a) and a multi-layered one at (b).

To find the inductance of such coils, first of all work out the ratio $R : (l + D)$, where R is the radius of the coil, l is the length of the winding, and D is the diameter of the wire (single layer) or the depth of the winding (multi-layer). Whether you use metric or imperial measures is not important, since we are only seeking a ratio; nevertheless, metric is probably more practical. Call the ratio X. Look up X along the horizontal SHAPE axis of the graph and read off the corresponding value for the MULTIPLYING FACTOR Y on the vertical axis. The inductance can then be calculated from the formula

$$L = N^2 R Y \ (\mu\text{H}).$$

Next month's instalment will deal with the iron-cored transformer.

6

$\sim V_2 = \dfrac{T_2}{T_1} V_1$

920058-1-16

8

920058-1-18a

Lenght of winding l
Mean radius of winding R
Wire diameter D

920058-1-18b
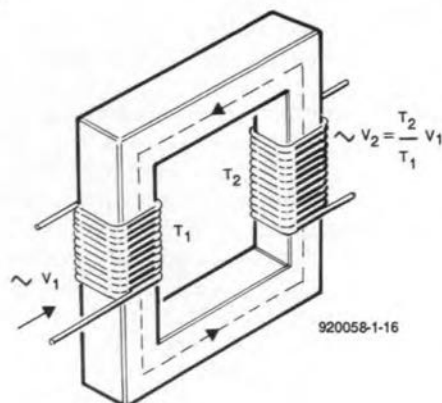
THE NICAM SYSTEM

Stereo TV sound has finally come of age with the progressive introduction over the past few years of a digital system called NICAM. This article aims at providing a background to the operation of the NICAM (near-instantaneously companded audio multiplex) system, which is now in use in most of the UK, Scandinavia, Belgium and Spain. NICAM-728, with subversions for PAL systems B/G and I, is also recommended by the EBU as the system for multi-channel sound transmission with terrestrial television. It has been adopted for use in several countries, including the UK, and now forms part of a draft CCIR recommendation.

By J. Buiting, technical editor.

WHEN we talk about different television standards, the discussion is usually about different ways of conveying the picture to the viewer. Up to ten years ago, the sound was taken for granted, which is remarkable because the stereo age was well under way at that time. Following a German initiative, some European countries introduced stereo TV sound based on an auxiliary subcarrier above the main (mono) FM carrier. Although this works, the NICAM system offers 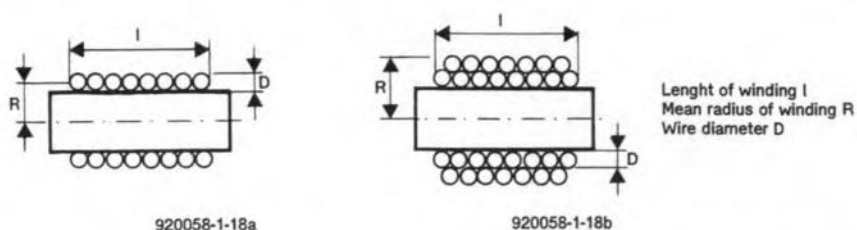superior sound quality at a roughly equal bandwidth requirement. Originally developed by the BBC, the NICAM-728 specification has been formally approved by the Department of Trade and Industry as the United Kingdom standard for two-channel digital sound with terrestrial television broadcasts.

A brief history of stereo TV sound

Since 1979, a number of stereo TV sound systems have been introduced that were aimed at downward compatibility with the existing mono sound systems. Among the requirements for the new sound systems were:

- minimum interference and crosstalk between the channels;
- quality of existing (main) mono channel must not be affected;
- equipment to upgrade transmitters and receivers must remain as simple as possible.

The need of maintaining downward compatibility, as well as the limited bandwidth available for the new sound systems, have forced the designers of analogue stereo TV sound systems to drop some of their target specifications, and agree on certain compromises that reduce the quality that could have been achieved in theory. Analogue stereo sound systems can be made downward compatible in two ways:

- by modifying the audio signal before it is modulated on to the carrier (single-carrier principle);
- by adding a second sound carrier just above or below the existing (mono) sound carrier (dual-carrier principle).

In both cases, a decoder matrix is required to separate the left and right channels, and produce the stereo sound image. Some systems also require de-emphasis and/or de-companding to improve the signal-to-noise ratio and the dynamic range.

The dual-carrier system is basically analogue, and offers quite reasonable sound quality. However, in this day and age of digital sound, it is not surprising that alternatives have been sought, based on the technology already familiar from CD players and the sound transmission standard developed for the MAC system. In particular the channel separation offered by NICAM is much higher than that achieved by any form of analogue dual-carrier system. Overall, the sound quality of a NICAM broadcast is so close to that of a compact disk that it is hard to tell the difference by just listening.

NICAM-728 digital sound transmission

Strictly speaking, the NICAM-728 system should be classified as a dual-carrier system, because a second sound signal is introduced in the baseband spectrum (see Fig. 1). The spectrum shown is for PAL system-I as used in the UK, with the main sound carrier at 6.0 MHz above the vision carrier, and a total channel bandwidth of about 8 MHz. Most other European countries use PAL system B or G, where the main sound channel is at +5.5 MHz, and the channel bandwidth is about 7 MHz.

The NICAM signal is recovered from a QPSK (quadrature phase shift keying) spectrum with a bandwidth of about 600 kHz. The centre frequency of this
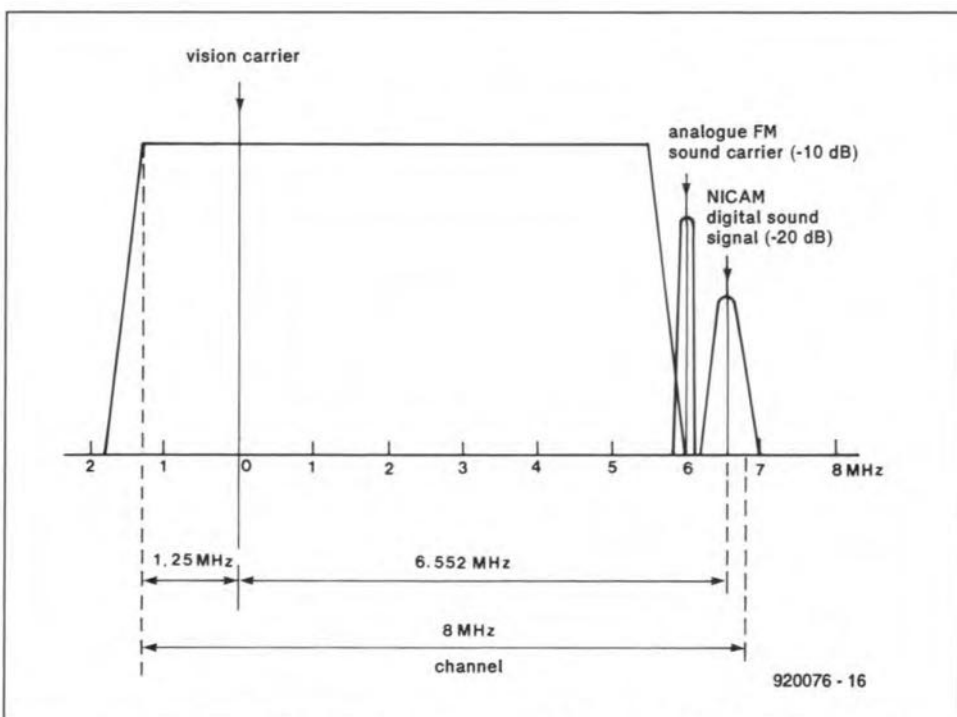

Fig. 1. The frequency band occupied by the NICAM-728 digital sound signal in relation to the picture and mono (analogue FM) sound signal components in the TV baseband.

'molehill' (that is what it looks like on a spectrum analyser) is +6.552 MHz (system I), or +5.850 MHz (system B/G). The level is about −20 dB with respect to the vision carrier. In the rest of this article, we will refer to the UK standard (PAL system-I) only.

Contrary to the analogue dual-carrier systems, the NICAM signal contains all the information necessary to reproduce the two stereo channels, i.e., it is completely independent of the main FM carrier at +6.0 MHz (except for the fixed frequency and phase relation), which is currently transmitted only to ensure downward compatibility with existing TV sets.

Sound multiplex and sound coding methods

To understand how the NICAM system works, we will take a look at the structure of the serial data stream at the transmitter side.

Frame structure and bit interleaving

As shown in Figs. 2 and 3, the data consists of 728-bit frames which are transmitted continuously without gaps. One frame is transmitted every millisecond, so the overall bit-rate is 728 Kbit/s, whence the system designation NICAM-728.

The 720 bits that follow the frame alignment word (FAW) have a structure that closely resembles that of the first-level protected, companded sound signal blocks in the systems of the MAC family. After the control bits and the additional data bits follows a block of 704 interleaved sound data bits. The interleaving pattern relocates data bits which are adjacent in the frame structure of Fig. 2 to positions at least 16 clock periods apart in the transmitted data stream.

Energy dispersal scrambling

The transmitted bit stream is scrambled for spectrum-shaping purposes (remember the restrictions as regards the baseband bandwidth). The scrambling operates synchronously to the multiplex frame. The FAW is not scrambled, and used to synchronise the pseudo-random sequence generator used for descrambling in the receiver. Figure 4 shows the general layout of the scrambler. The following parameters apply:

- the bit that follows the FAW is the first scrambled bit, and is added modulo-two to the first bit of the pseudo-random sequence;
- the bit that precedes the FAW is the last scrambled bit;
- scrambling takes place immediately after interleaving (and descrambling is therefore prior to de-interleaving in the receiver);
- the pseudo-random sequence is defined by a generator polynomial
$x^9 + x^4 + 1$
and an initialisation word ('seed')
1 1 1 1 1 1 1 1 1.
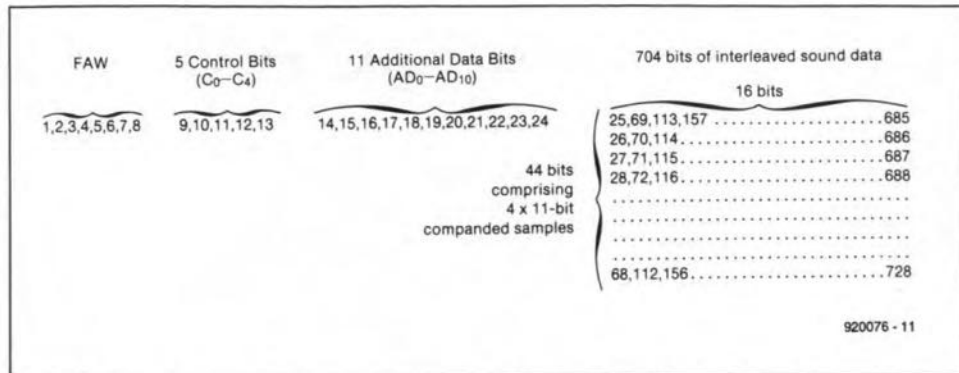
Fig. 2. Each frame consists of four groups of bits, each with its own function.
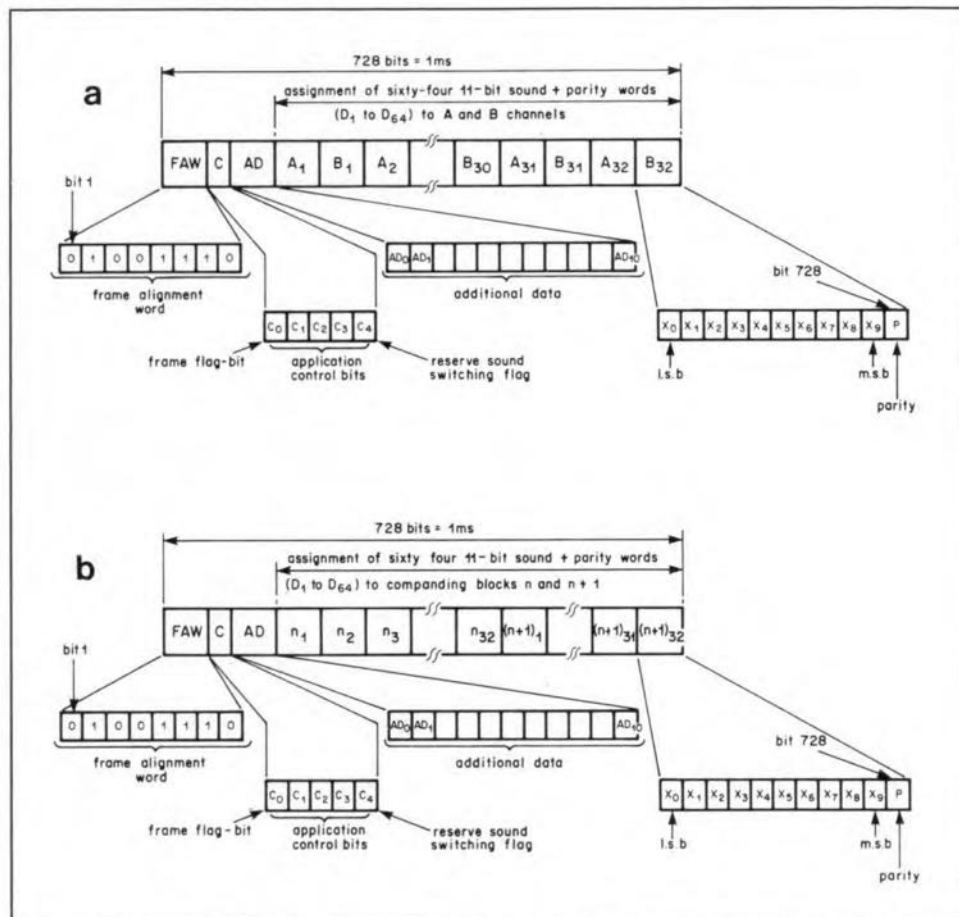
Fig. 3. (a) Structure of a 728-bit frame containing a stereo sound signal (before interleaving); (b) the same for a mono sound signal (also before interleaving).

Thus, with reference to Fig. 2, the sequence starts:
0000 0111 1011 1110 0010.

FAW and control information block

The FAW is 01001110, which is a series of bits transmitted in that order. The control information converged to the receiver consists of a frame flag bit, C_0, three application control bits, C_1, C_2 and C_3, and a reserve sound switching flag, C_4 (see Fig. 3). The frame flag bit, C_0, is set to '1' for eight successive frames, and to '0' for the next eight frames. The frames are numbered within the sequence as follows: the first frame (Frame 1) of the sequence is defined as the first of the eight frames in which $C_0=1$. Hence, the last frame (Frame 16) of the sequence is the last of the eight frames in which $C_0=0$. This frame sequence is used to synchronise changes in the type of information being carried in the

channel.

The function of the three application control bits, C_1, C_2 and C_3, is to define the current application of the last 704 bits in each frame, which may be used to convey either sound samples or data. The available options are shown in Table 1. When a change to a new application is required, these control bits change (to define the new application) on Frame 1 of the last 16-frame sequence of the current application. The 704-bit sound/data blocks change to the new application on Frame 1 of the following 16-frame sequence.

The reserve sound switching flag, C_4, contained in the control information block is used to switch back to the output of the conventional FM demodulator when the digital sound decoding system fails. This is, of course, acceptable only if the FM sound channel carries the same programme as the failing digital channel. The means to

Table 1. Applications of 704-bit sound/data blocks.

Application control bits			Contents of 704-bit sound/data block
C_1	C_2	C_3 *	
0	0	0	stereo signal comprising alternate A-channel and B-channel samples
0	1	0	two independent mono sound signals (designated M1 and M2) transmitted in alternate frames.
1	0	0	one mono signal and one 352-kBit/s transparent data channel transmitted in alternate frames.
1	1	0	one 704-Kbit/s transparent data channel.

* $C_3=1$ provides for signalling additional sound or data coding options. When $C_3=1$, decoders not equipped for these additional options should provide no sound output.

Table 2. Coding/protection range selection.

Coding range	Protection range	Scale factor value		
		R_2	R_1	R_0
1st	1st	1	1	1
2nd	2nd	1	1	0
3rd	3rd	1	0	1
4th	4th	0	1	1
5th	5th	1	0	0
5th	6th	0	1	0
5th	7th	0	0	1
5th	7th	0	0	0

inhibit such switching is incorporated in the control information. Control bit C_4 is set to '1' when the FM channel carries the same sound programme as the digital stereo signal or the digital, mono signal (where two digital mono signals are transmitted, this refers to the M1 signal only). When the FM channel is not carrying the same programme as the digital sound channel, C_4 is set to '0'. In this state, it can be used to prevent switching to the FM sound. Finally, C_4 has no meaning in the case of data transmission.

Additional data and the sound/data block

Data bits AD0 to AD10 (see Fig. 3) are reserved for future applications yet to be defined.

The last 704 bits in any frame form a block of either sound or data (the two types of information are not mixed within one frame). One frame contains 64 sound samples (D1 to D64). The structures of a stereo sound frame and a mono sound frame are shown in Figs. 3a and 3b respectively.

In stereo mode (AC: $C_1=C_2=C_3=0$), the odd-numbered samples convey the A-channel, and the even-numbered samples the B-channel. Thus, 32 samples of each channel are transmitted in every frame.

If two independent mono sound channels, M1 and M2, are transmitted (AC: $C_1=0$; $C_2=1$; $C_3=0$), M1 is transmitted in odd-numbered frames, and M2 in even-numbered frames.

If one mono sound channel is transmitted (AC: $C_1=1$; $C_2=0$; $C_3=0$), it is contained in odd-numbered frames, and data are transmitted in even-numbered frames.

Thus, for mono sound signals, each frame with sound information in it contains 64 consecutive sound samples, which will span two complete companding blocks, shown as blocks n and $(n+1)$ in Fig. 3. No format has yet been defined for data information.

Sound signals

Sound signals are sampled at 32 kHz, and coded initially with a resolution of 14 bits

per sample. Near-instantaneous companding is used to reduce the number of bits per sample from 14 to 10, and one parity bit is added to each 10-bit sample word for error detection and scale-factor signalling purposes.

The companding process forms the 14-bit digital samples corresponding to each of the sound signals into blocks of 32. All of the samples in each 1-ms block are subsequently coded, using a 10-bit 2's complement code, to an accuracy determined by the magnitude of the largest sample in the block, and a scale factor code is formed to convey the degree of compression to the receiver. Figure 5 illustrates the coding of companded sound signals.

Prior to compression, a pre-emphasis to CCITT recommendation J17 (Ref. 2) is applied to the sound signals, either by using analogue pre-emphasis networks before digitisation, or by using digital filters with the digital signals.

For stereo transmissions, the signals of the left and right sound channels are sampled simultaneously. The Channel-A samples convey the left-hand (L) sound signal, and the Channel-B samples the right-hand (R) sound signal.

One parity bit is added to each 10-bit

sound sample to check the six most-significant bits for the presence of errors. The parity group so formed is even (i.e., the modulo-2 sum of the six protected sample bits and the parity bit equals 0). Subsequently, the parity bits are modified to signal the 3-bit scale factor word associated with each sound signal block.

In addition to signalling the coding range, the scale factor signals seven protection ranges. This information may be used in the receiver to provide extra protection for the most significant bits of the samples. Table 2 shows the coding ranges and protection ranges associated with each 3-bit scale factor word. The five coding ranges indicate the degree of compression to which the block of samples has been subjected for the near-instantaneous companding process. The 3-bit scale factor R_2-R_1-R_0 associated with each 32-sample sound block is conveyed by modification of the parity bits (see Fig. 5).

When a stereo sound signal is being transmitted, FE1 (facteur échelle; scale factor) is the scale-factor word R_{2A}-R_{1A}-R_{0A} associated with the 'A' samples, and FE2 the scale-factor word R_{2B}-R_{1B}-R_{0B} associated with the 'B' samples. If P_i is the parity bit of the ith sample, this is modified
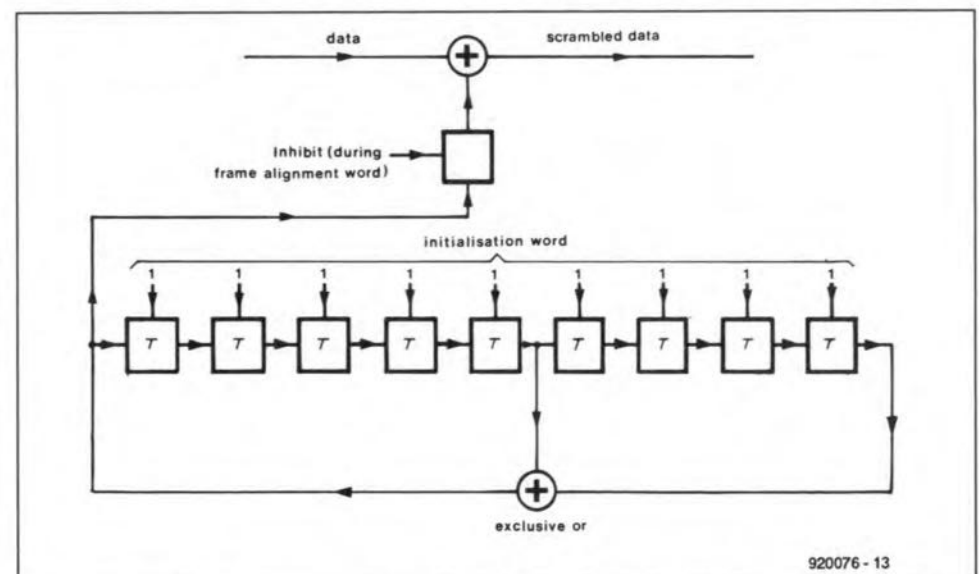

Fig. 4. Pseudo-random sequence generator (PRSG) for spectrum shaping (energy dispersal scrambling).

to P'_i, by modulo-2 addition of one bit of one of the scale-factor words according to the following relationship:

$P'_i=P_i \oplus R_{2A}$ for i = 1,7,13,19,25,31,37,43,49
$P'_i=P_i \oplus R_{1A}$ for i = 3,9,15,21,27,33,39,45,51
$P'_i=P_i \oplus R_{0A}$ for i = 5,11,17,23,29,35,41,47,53

$P'_i=P_i \oplus R_{2B}$ for i = 2,8,14,20,26,32,38,44,50
$P'_i=P_i \oplus R_{1B}$ for i = 4,10,16,22,28,34,40,46,52
$P'_i=P_i \oplus R_{0B}$ for i = 6,12,18,24,30,36,42,48,54

When a mono signal is being sent, FE1 is the scale-factor word R_{2n}-R_{1n}-R_{0n} associated with the first block of 32 samples in the frame, and FE2 is the scale-factor word R_{2n+1}-R_{1n+1}-R_{0n+1} associated with the second block of 32 samples in the frame. As in the case of stereo sound, the parity bit of the ith sample, P_i, is modified to P'_i by modulo-2 addition of one bit of one of the scale-factor words. However, in the mono case, the modification of the parity bits relates to the block structure of the mono signal, as follows:

$P'_i=P_i \oplus R_{2n}$ for i = 1,4,7,10,13,16,19,22,25
$P'_i=P_i \oplus R_{1n}$ for i = 2,5,8,11,14,17,20,23,26
$P'_i=P_i \oplus R_{0n}$ for i = 3,6,9,12,15,18,21,24,27

$P'_i=P_i \oplus R_{2n+1}$ for i = 28,31,34,37,40,43,46,49,52
$P'_i=P_i \oplus R_{1n+1}$ for i = 29,32,35,38,41,44,47,50,53
$P'_i=P_i \oplus R_{0n+1}$ for i = 30,33,36,39,42,45,48,51,54

It should be noted that some of the scale-factor information in the second block of samples is conveyed in the parity coding of samples 28 to 32, which are in the first block. This conforms with the specifications for the MAC/Packet family of transmission standards drawn up by the EBU (Ref. 1)

The scale-factor coding range and protection range information are extracted at the decoder by majority decision logic. Subsequently, the original parity is restored for the purpose of error concealment.

The control information described in Section 6.2.3 of Ref. 1 (Chapter 3, Part 3) is not used. However, other information could be transmitted by the same means, i.e., two information bits such that one modifies samples 55 to 59, and the other samples 60 to 64. NICAM receivers should be designed to take account of this facility.

Modulation parameters

The characteristics of the AM vision (vestigial sideband) and FM sound are defined in the UK specification for PAL system-I transmissions (Ref. 3), with the exception that the FM sound carrier power is 10 dB down with respect to the vision carrier, instead of 7 dB. In the case of PAL system-B/G transmissions, the definitions given in CCIR Report 624-3 apply.

The NICAM signal in the baseband is classified as differentially encoded quadrature phase shift keying (DQPSK or 4-phase DPSK). This is a four-state phase
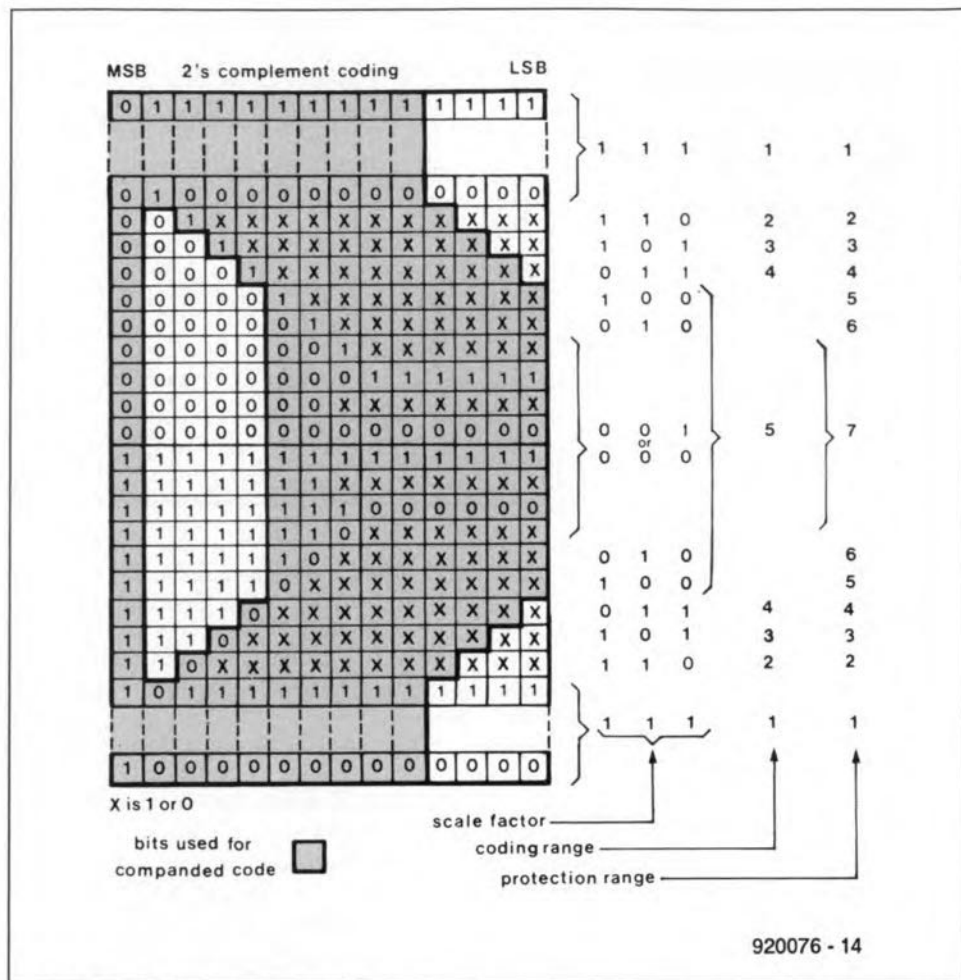
Fig. 5. Coding of companded sound signals.

modulation system in which each change of state conveys two data bits. The input data stream at the modulator is differentially encoded. This is done in two steps: (1) serial to two-bit parallel conversion, and (2) coding of the transmitted phase changes. The amounts of the changes of carrier phase which correspond to the four possible values of the input bit pairs (A_n-B_n) are shown in Table 3.

Table 3. DQPSK carrier state changes.

Input bit-pair		Amount by which the carrier changes phase
A_n	B_n	
0	0	0° (no change)
0	1	−90°
1	0	−270°
1	1	−180°

Thus, the carrier phase can be at one of four rest-states which are spaced at intervals of 90° apart (Fig. 6a). An input bit-pair will shift the carrier phase into a different rest-state by the amount of phase change assigned to that particular value of bit-pair. The transmitted phase-changes and resulting carrier rest-states for the input bit-pair sequence 00, 01, 11 and 01 are illustrated in Fig. 6b. In the receiver, the transmitted datastream may be unambiguously recovered by determining the
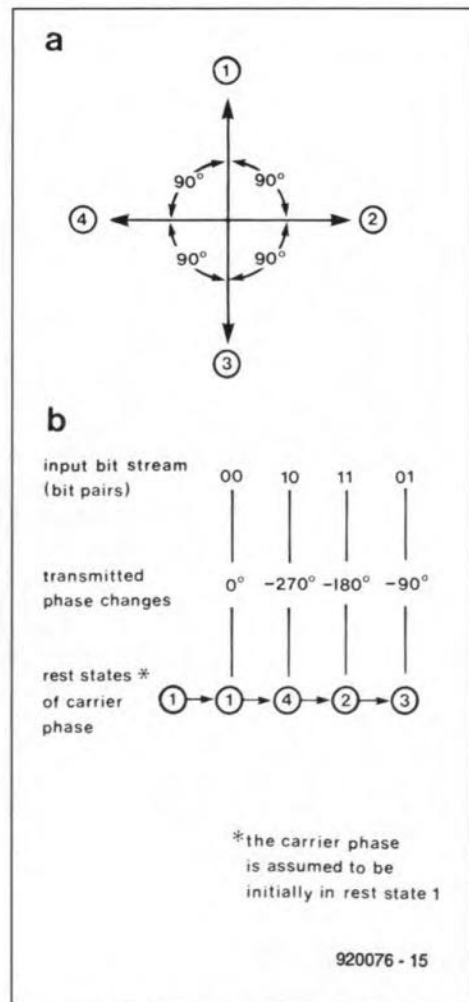
Fig 6. DQPSK modulation principle.
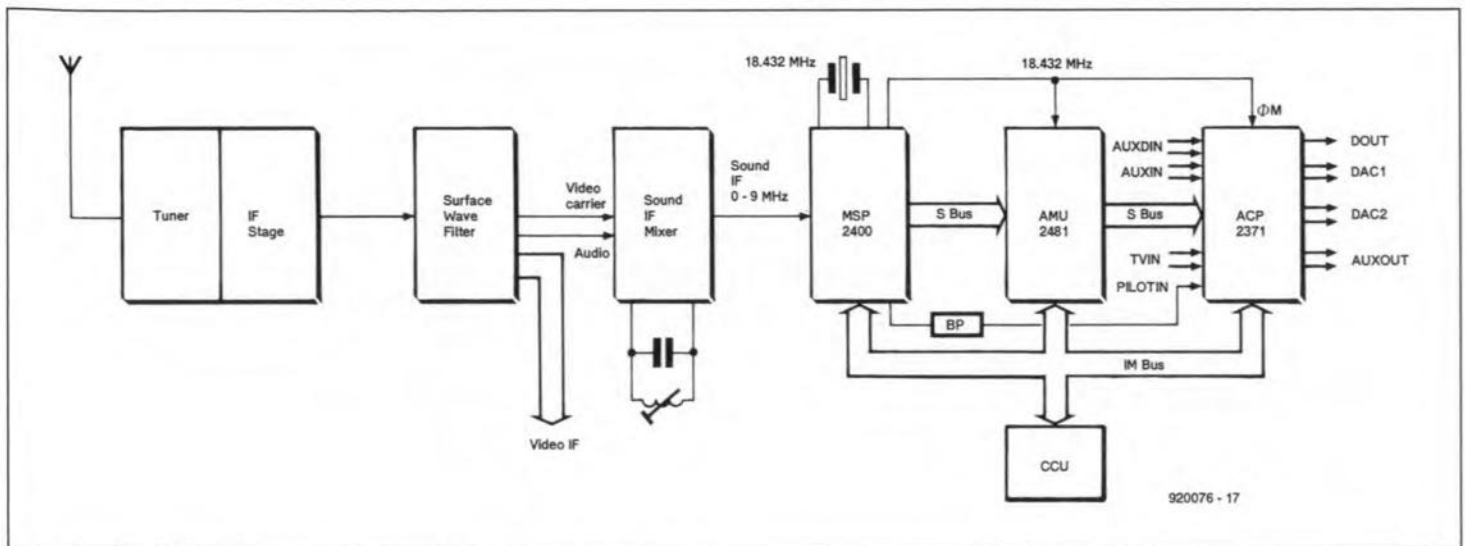
Fig. 7.   NICAM decoder concept proposed by ITT Semiconductors.

phase-changes between one bit-pair and the next.

It was already mentioned that spectrum-shaping techniques are applied to keep the bandwidth of the NICAM signal in the baseband within limits. For best performance in the presence of random noise, the amplitude-frequency response of data spectrum-shaping filters at the receiver should be identical to that at the transmitter. The target amplitude frequency response, $H_T(f)$, is given by

$$H_T(f) = \begin{cases} \cos\dfrac{\pi f t_s}{2} & \text{if } 0 \le f \le \dfrac{1}{t_s} \\ 0 & \text{if } f > \dfrac{1}{t_s} \end{cases}$$

where $t_s = \dfrac{1}{364,000}$ s

and the filter has a constant group delay for all frequencies $\le 1/t_s$. The filter made on the basis of the above transfer characteristic has a 100% cosine rol-off (for PAL systems B and G a filter with 40% cosine roll-off is required).

In the UK, the NICAM subcarrier is located at 6.552 MHz above the frequency of the vision carrier (see Fig. 1). This frequency is obtained by multiplying the transmitted bit-rate (728 Kbit/s) by 9. In countries where PAL system-B or -G is used, the subcarrier frequency is +5.850 MHz.

NICAM decoder concepts

Among the IC manufacturers that have developed NICAM processors for use in commercial-grade receivers are ITT Semiconductors of Germany, and Micronas, Inc. of Finland. A decoder based on ICs from the latter manufacturer is described elsewhere in this issue.

ITT Semiconductors have integrated their NICAM processors, the MSP2400 and MSP2410, into the Digit 2000 TV system. Figure 7 shows the block diagram of
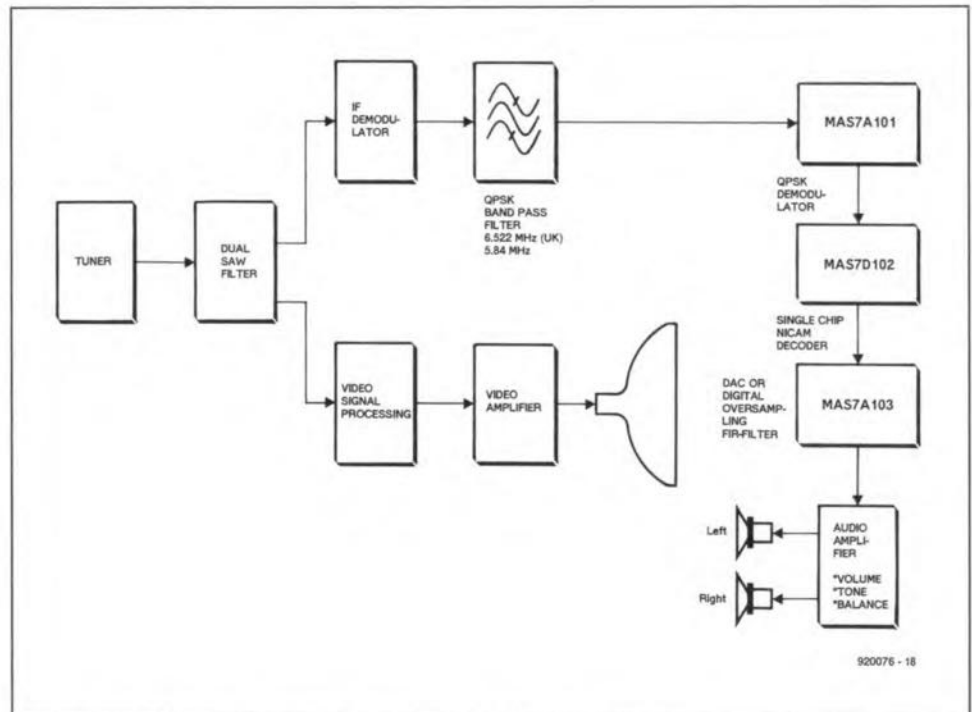
Fig. 8.   NICAM decoder concept proposed by Micronas Inc.

the ITT approach. Apart from the MSP2400 or MSP2410, two additional ICs are required, the AMU2481 and the ACP2371. Remarkably, the MSP2400 has a digital filter to extract the NICAM information from the baseband spectrum (0 to 9 MHz). This is in contrast to the Micronas circuit (Fig. 8), which uses a conventional *L-C* bandpass filter tuned to 5.84 MHz (PAL system B/G) or 6.552 MHz (PAL system I). The ITT circuit has a number of interesting options such as multistandard sound processing and automatic standard recognition and switching. The configuration as shown in Fig. 7 is capable of handling mono FM, stereo FM (the German dual-carrier system) and all NICAM modes (a special version of the ACP2371 is available for satellite TV sound). The disadvantage of the ITT circuit is, however, that it can not work without control software, and this is where the Micronas system has the edge on the ITT system: it can work 'stand alone', and offers an op-

tional way of computer control.   ∎

Sources:
(1) NICAM-728: specification for two additional digital sound channels with System-I television.
(2) Document SPB 424, 3rd revised edition, European Broadcasting Union.

References:
1. *Specification of the system of the MAC/Packet family.* European Broadcasting Union (EBU) Technical Document 3285 (1986).
2. CCITT Red Book, Volume III, Fascicle III.4: *Transmission of sound-programme and television signals, recommendation J.17 'Pre-emphasis used on sound-programme circuits'.*
3. *Specification of Television Standards for 625-line System-I transmissions in the United Kingdom.* Department of Trade and Industry, Radio Regulatory Division, London, 1984.

NICAM DECODER

The decoder described here is aimed at the experienced radio and TV enthusiast who wants to upgrade an existing TV set or video recorder with NICAM digital stereo sound. Suitable for PAL TV systems 'I' (UK) and 'B/G' (Scandinavia, Belgium, Spain and others), the decoder is a compact and simple to control circuit that can either be built as a set-top extension, or incorporated into a TV set.

**Design by Rob Krijgsman
PE1CHY**

THIS decoder is based on a NICAM chip set developed by Micronas Inc. of Finland. The set consists of the MAS7A101 QPSK demodulator, the MAS7D102 NICAM decoder, and the MAS7A103 dual D-A converter. The chip set allows two high-quality audio channels (stereo or dual-language mode) to be recovered from a NICAM signal at 5.85 MHz or 6.552 MHz (if broadcast, and depending on the PAL system used) in the TV baseband spectrum. All that is needed to be compatible with either of the two PAL systems is to fit the correct input filter, a jumper and a quartz crystal for the demodulator clock.

Three ICs

As shown by the block diagram in Fig. 1, the upper part (say, above 5 MHz) of the TV baseband spectrum is first filtered to extract the NICAM signal centred around 5.85 MHz

(system B/G) or 6.552 MHz (system I). The insertion loss of the band-pass filter is compensated by an amplifier.

MAS7A101 QPSK demodulator

The NICAM signal is applied to the MAS7A101 QPSK demodulator IC. This is a pretty complex integrated circuit, whose internal architecture is given in Fig. 2. The QPSK signal at the input is buffered before it is applied to a multiplier circuit which consists of analogue switches. The switches are opened and closed by a signal derived from a phase-controlled quartz crystal oscillator. The crystal frequency equals four times the NICAM subcarrier frequency, i.e.,

$$5.850 \times 4 = 23.400 \text{ MHz}$$

for PAL systems B and G, or

$$6.552 \times 4 = 26.208 \text{ MHz}$$

for PAL system I. The quartz oscillator is locked to the received NICAM signal by means of a PLL. The demodulated signal is

taken through a switchable low-pass filter, and subsequently split into two.

One signal is sent to a second PLL which serves to recover the 728-kHz NICAM bit clock from the demodulated signal. The crystal-controlled VCO in this PLL operates at eight times the NICAM bit clock, or 5.824 MHz. This VCO also provides the central clock signal for the other ICs in the decoder.

The other demodulated signal is sent to a slicer circuit where it is converted into a bi-
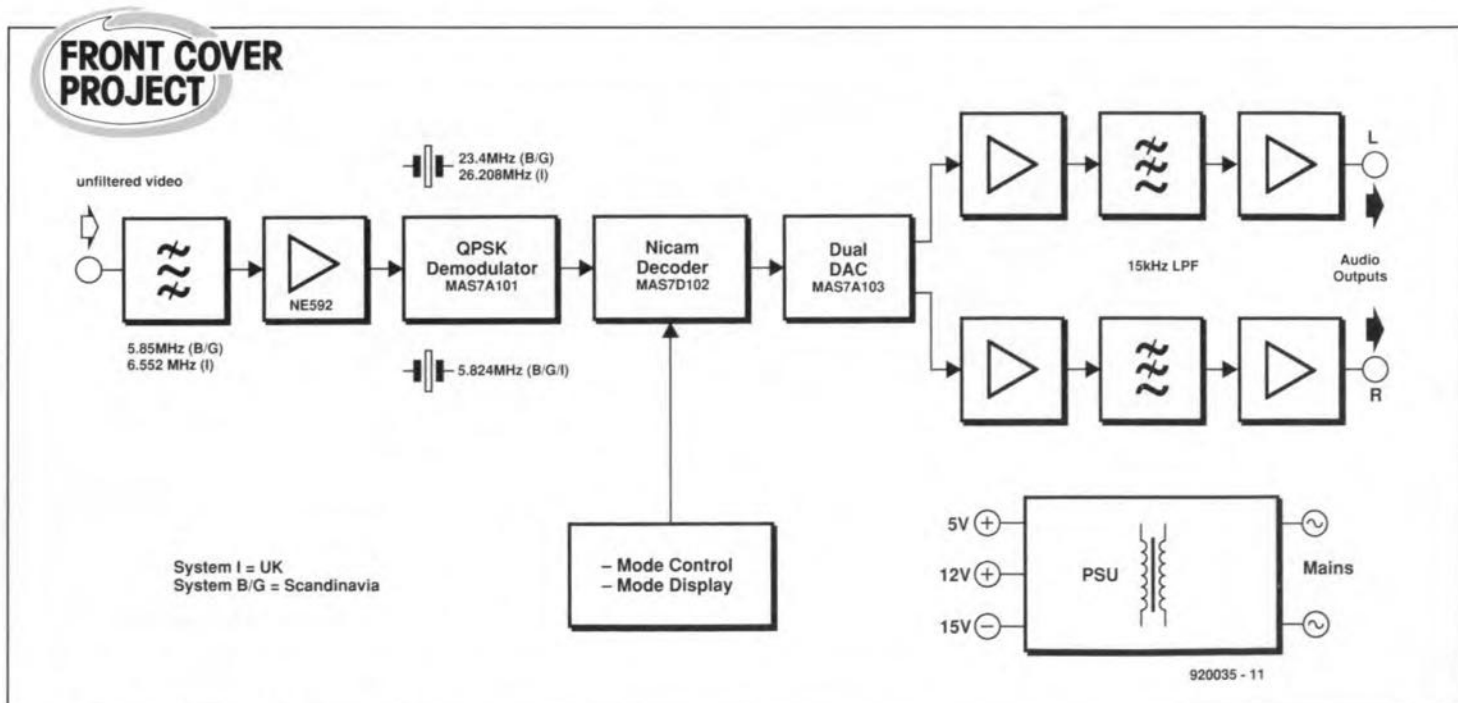

FRONT COVER PROJECT

Fig. 1. Block diagram of the decoder.

nary digital signal. The recovered clock signal and the binary signal are available at the corresponding outputs of the MAS7A101.

MAS7D102 NICAM decoder

The MAS7D102 NICAM decoder (Fig. 3) uses the recovered NICAM bit clock to tackle the decoding proper of the bitstream supplied by the QPSK demodulator. The decoding process involves quite a lot: descrambling, de-interleaving, error detection and correction, and reconstruction of the original 14-bit sound samples in both channels. The MAS7D102 can be programmed or wired to supply digital output signals suitable for one of three different bus systems: the I^2S-bus (Philips), the S-bus (ITT), or the DAC-bus (Toshiba). Many functions of the IC can be controlled either via an I^2C link, or by means of external hardware. The latter option is exploited here, and has the advantage of obviating a microcontroller and a dedicated control program.

With reference to the IC architecture shown in Fig. 3, it is seen that the digital signal supplied by the QPSK demodulator is split into two. One signal is fed to a synchronisation logic section where the FAW (frame alignment word) is detected and extracted. The FAW is never scrambled. The other copy of the digital signal is sent to the descrambler circuit, which serves to counteract the energy dispersal (spectrum-shaping) scrambling applied at the transmitter. When the decoder chip is first switched on, it uses the standard descrambling initialisation word '11111111', which enables reception of non-encrypted NICAM broadcasts. External hardware is required to be able to change the initialisation word (or 'seed') 'on the fly' when the system is used for reception of Pay-TV transmissions using encrypted NICAM audio.

Returning to the operation of the MAS7D102, the control information bits C_1-C_2-C_3-C_4 are extracted from the datastream. These bits enable the receiver to determine the type of programme material: i.e., dual-language or stereo. The decoded control bits are available in an I^2C register as well as on an output port. The latter allows a simple display to be connected that indicates the receiver mode. The sound samples are fed to the de-interleaver, and from there to the error detection/correction circuit. Finally, they are de-companded to their original 14-bit resolution, and fed to the output of the IC according to the selected signal format (I^2S-bus, S-bus or DAC-bus). The format selection is effected via the I^2C bus, or via logic levels applied to the configuration (CONFIGx) pins, which in addition allow you to select between mono-A or mono-B during dual-language broadcasts. The functions of all registers contained in the MAS7D102, and the configuration options that can be set in hardware, are given on page 41.

MAS7A103 dual DAC

This IC converts the 14-bit sound samples furnished by the decoder into two analogue audio signals. Since the output datastream of
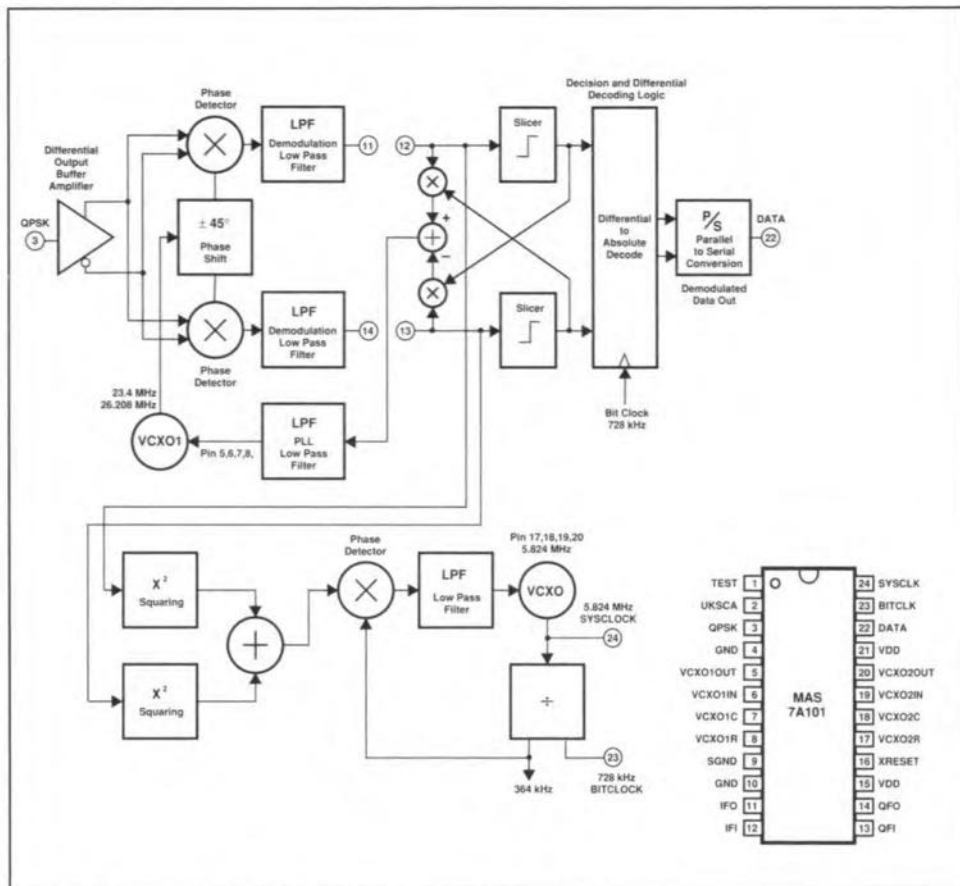
Fig. 2.   MAS7A101 QPSK demodulator architecture and pinning.
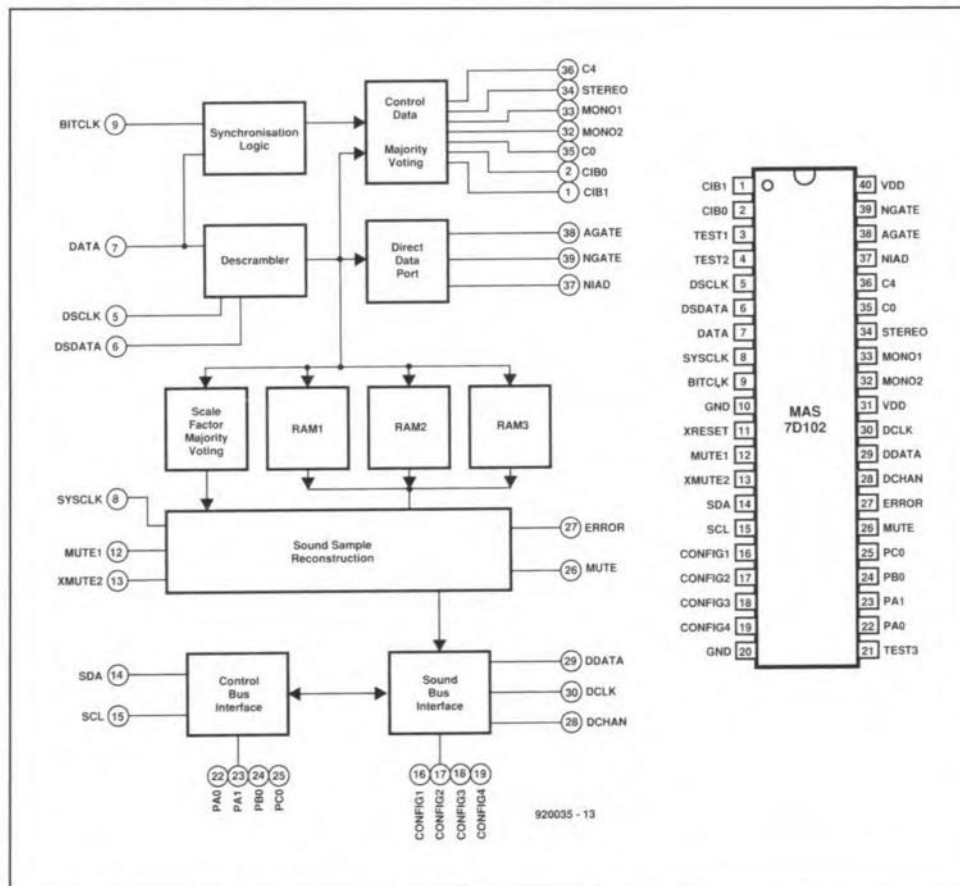
Fig. 3.   MAS7D102 NICAM decoder architecture and pinning.

the decoder IC is multiplexed, the first task of the DAC is to extract and separate the information that belongs with each channel. Next, the two digital signals are converted into analogue ones by R-$2R$ ladder networks. These supply output currents rather than

voltages, so that two external opamps are required to obtain audio signals that can be fed to an amplifier. Before that can be done, however, the audio signals need to be taken through a 15-kHz low-pass filter to remove the residue of the 32-kHz sampling signal.
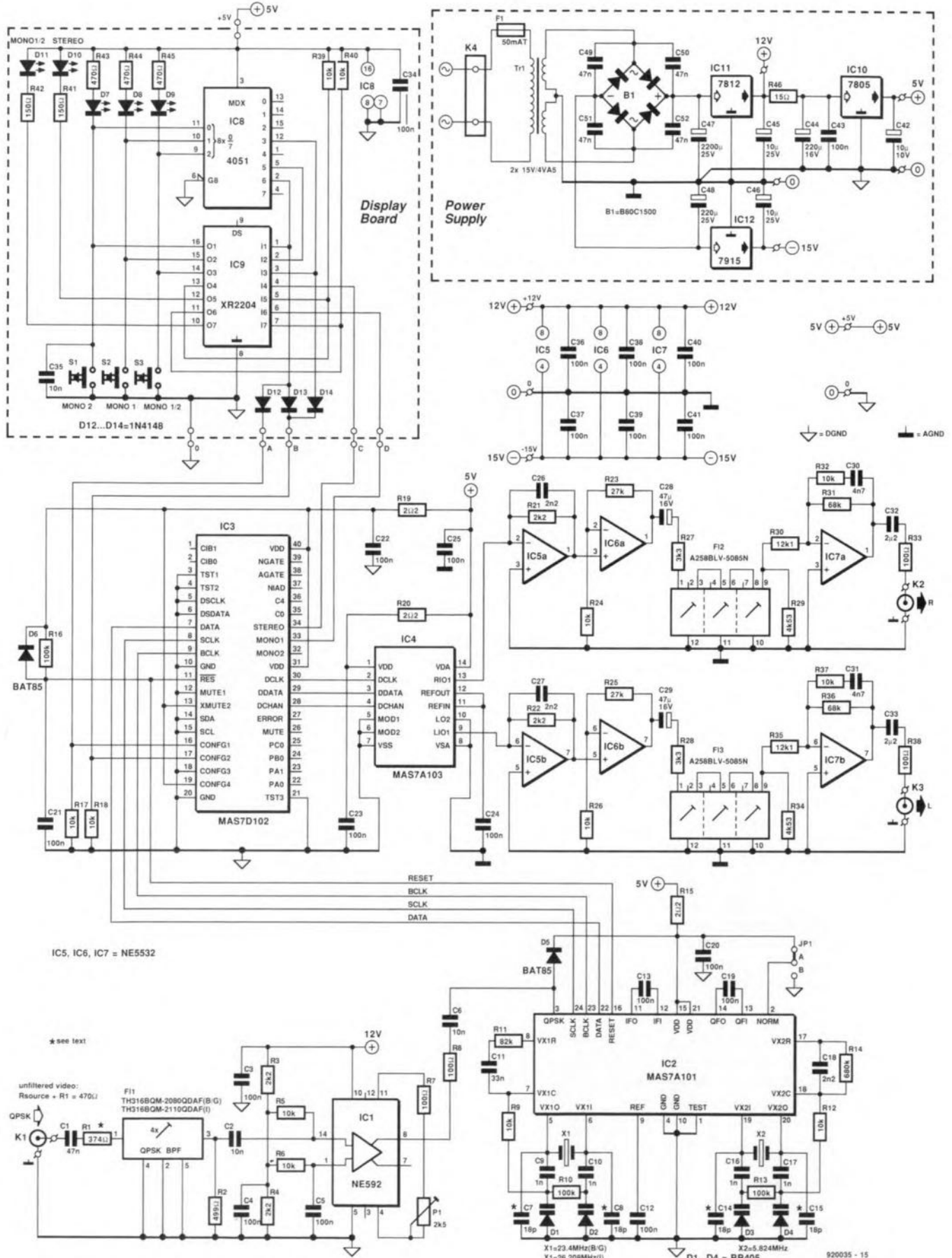
Fig. 4.   Circuit diagram of the NICAM decoder.

Country	TV system	Stereo sound	Main sound subcarrier	Stereo subcarrier	QPSK filter Fl1	Quartz X1	Jumper JP1
Scandinavia	PAL B/G	Digital; NICAM-B	5.5 MHz	5.850 MHz	TH316BQM-2080QDAF	23.400 MHz	A
United Kingdom	PAL I	Digital; NICAM-I	6.0 MHz	6.552 MHz	TH316BQM-2110QDAF	26.208 MHz	B
Germany; Switzerland; Benelux	PAL B/G	Analogue	5.5 MHz	5.740 MHz	—	—	—
Italy; Spain	PAL B/G	Digital; NICAM-B	5.5 MHz	5.850 MHz	TH316BQM-2080QDAF	23.400 MHz	A

Table 1.   The choice of two components in the NICAM decoder, and the position of a jumper, depends on the country you live in.

This filter takes us back to the block diagram in Fig. 1, with the final remark that J17 de-emphasis is applied on the audio signals.

Practical circuit

After studying some of the background theory on NICAM (to be found elsewhere in this issue), and having acquired samples and datasheets of the NICAM chip set, the author set out to work, and was able to design and build a simple NICAM decoder that was tested with the aid of NICAM broadcasts received from the Belgian national TV station BRT (these broadcasts were experimental at the time, and are currently regular). The BRT transmits NICAM-728 according to PAL standard B/G. Initially, the application circuits suggested by Micronas were built, and from there on further experiments evolved to produce a repeatable decoder.

The final result is an uncluttered circuit shown in Fig. 4. The unfiltered video signal taken from a suitable point in the TV tuner (more about this further on) is applied to the input of a four-section bandpass filter tuned to 5.85 MHz (6.552 MHz for the UK system-I). The input impedance of the decoder is about 900 Ω. To ensure that the input of the bandpass filter is correctly terminated, the sum of the source impedance and resistor R1 must be 470 Ω, as indicated in the circuit di-

agram. The Type TDA2541 demodulator IC, for instance, has an output impedance of about 100 Ω. The bandpass filter used is a ready-made, pre-aligned module from Toko (note that different types are required for systems B/G and system I). Its insertion loss lies between 8 dB and 16 dB. This is compensated by amplifier IC1, whose gain can be set as required with the aid of preset P1 to give a signal level of 200 to 800 mV$_{pp}$ at the input of the QPSK demodulator, IC2.

As indicated in the diagram, the frequency of quartz crystal X1 is determined by the PAL TV system used in your country. Jumper JP1 should also be fitted in accordance with the system used, to select the appropriate low-pass characteristic in the demodulator. Information on the options in the circuit depending on the TV system used is summarized in Table 1.

Depending on the characteristics of the crystals used in positions X1 and X2, the exact values of C7-C8 and C14-C15 may have to be changed from those shown in the circuit diagram. Given that the quartz crystals probably have to be cut to order (the frequencies being non-standard as far as we have been able to find out), some experimenting may be required to obtain the correct oscillator frequencies.

The demodulator, IC2, supplies the recovered 728-kHz bit clock, the digital

NICAM signal, and the 5.824-MHz system clock to the decoder, IC3. An R-C network, R16-C21, resets the demodulator and the decoder ICs at power-on.

Mode selection is effected with configuration bits config1 and config2. The available options are mono-2, mono-1 and mono-1/2 (dual language mode). The logic bit combinations required for these settings are supplied by IC8, IC9 and three push-buttons, S1, S2 and S3. The combination of these parts forms a kind of three-position flip-flop with a built-in latch function, a debounce circuit and an indication (on five LEDs). Capacitor C25 ensures that the 'mono-2' mode is automatically selected at power-on.

Diodes D12, D13 and D14 provide the required logic levels at the CONFIG inputs of the decoder IC. LEDs D10 and D11 indicate the currently transmitted mode: dual-language (mono-1/2) or stereo. This indication can not be changed by pressing the MODE switches.

Like the QPSK demodulator IC, the NICAM decoder, IC3, is used in a standard application circuit as suggested by the manufacturer. Similarly, few surprises are found in the link to the dual DAC, IC4, and the subsequent two-stage opamp-based current-to-voltage converters/amplifiers. It will be noted, though, that the opamps work from a symmetrical (+12 V/–15 V) supply. The gain of IC6a and IC7a in the right (R) output channel is set such that the loss introduced by the 15-kHz low-pass filter, Fl2, is overcome whilst ensuring an audio output level that is compatible with other equipment driving a amplifier 'line' input. The same goes, of course, for the corresponding components in the left (L) channel. The low-pass filters are, again, ready-made pre-aligned modules from Toko. Here, we are dealing with two A258BLV-5085N three-section L-C filters (the designer apologizes for the type numbers). Finally, the J17 de-emphasis networks in the right and left audio channels are formed by R32-C30 and R37-C31 respectively. The outputs of the NICAM decoder are capable of driving amplifier 'line' inputs.

Construction

First, cut the printed circuit board (Fig. 5) into three to separate the power supply
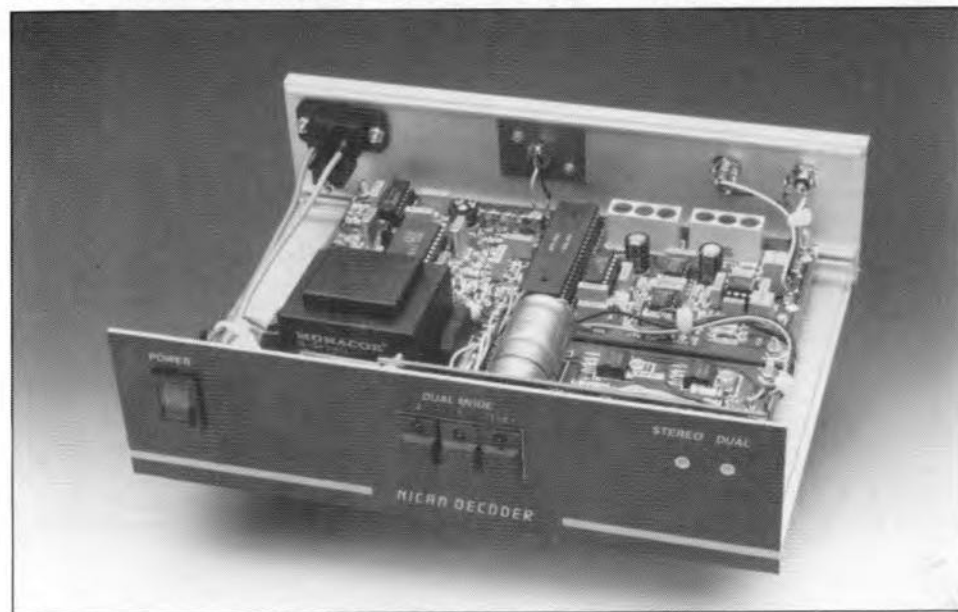
A look into the completed prototype of the decoder.
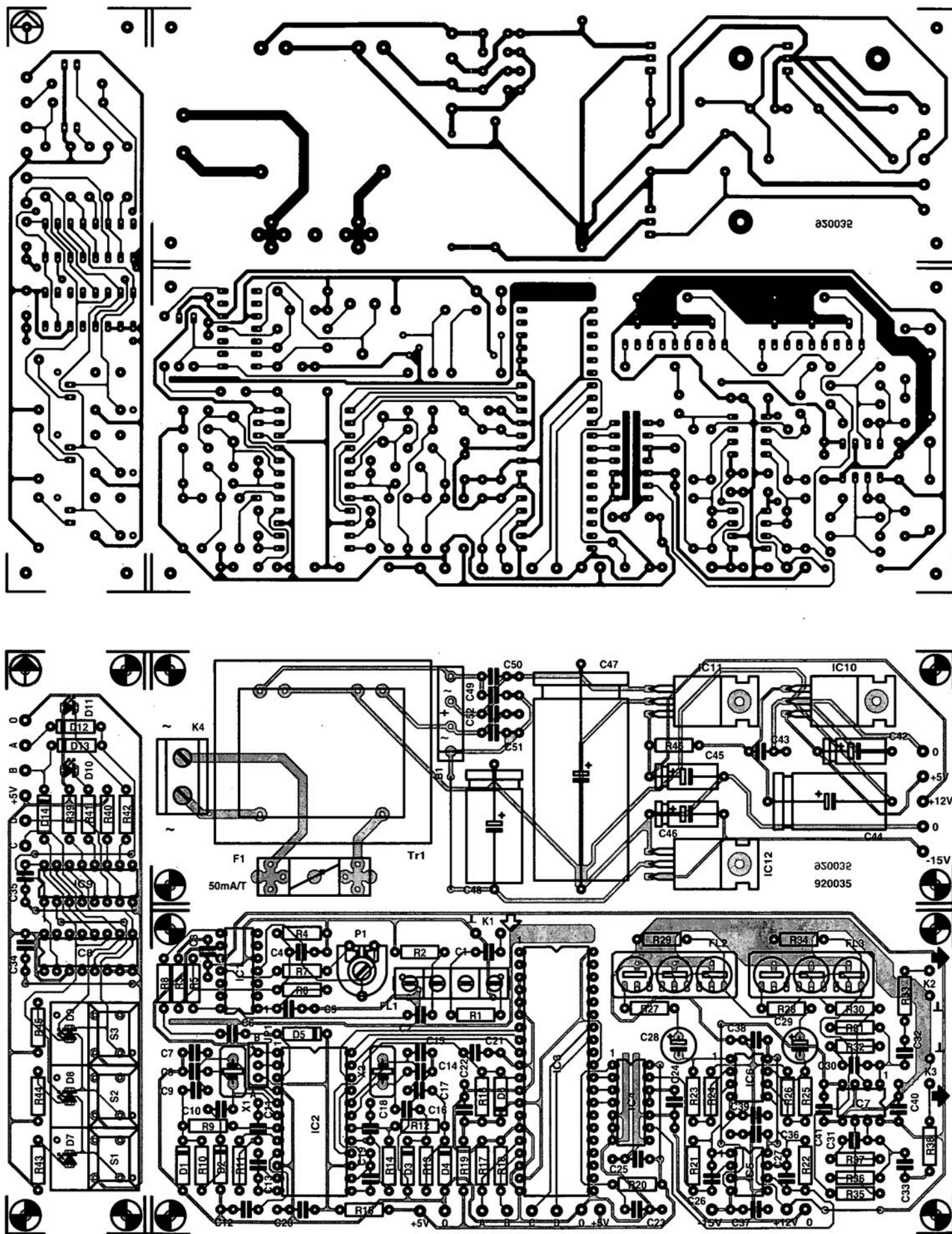
Fig. 5.   Track layout and component mounting plan of the single-sided PCB for the NICAM decoder.

board, the decoder board and the keyboard. The population of these boards is entirely straightforward, and should not present problems. It is recommended to use IC sockets. The voltage regulators are bolted straight to the power supply board, and do not need heat-sinks. The fuse is fitted in a holder with a protective plastic cap. On the decoder board, the section with the blue (or red) core in the QPSK bandpass filter, Fl1, is at the side of the NICAM decoder chip, IC2.

The keyboard/display section of the printed circuit board has on it three Digitast press-keys with a built-in LED. The front panel of the enclosure for the NICAM decoder (if used) must be cut and drilled to allow the push-buttons and the two LEDs to the right of the board to protrude—more about this further on.

For an initial test, the completed boards are interconnected. Switch on, and check the presence of the correct supply voltages at a number of points. Press the keys and see if the associated LEDs light. If this works all right, stop, and start thinking very hard about

Finding the input signal

The present NICAM decoder is intended as an upgrade for existing TV sets, set-top TV tuners or video recorders. In nearly all cases, this equipment will have to be opened or modified to find or create a point where the NICAM signal can be 'tapped' and fed to the decoder. The following points should be taken into account:

1. Opening your TV set or VCR in most cases voids your warranty on this equipment.
2. The chassis of most older TV sets is connected direct to the mains. **Never** work on such a TV set without using an isolating transformer.
3. Make sure you have the service documentation (or at least a circuit diagram) of the equipment.

The intrepid among you should be looking for a for a point at the input of the sound demodulator where a signal is available that contains as little video information as possible. In most cases, the input signal of the main FM demodulator (5.5 MHz for system-B/G, or 6.0 MHz for system-I) is taken through a ceramic band-pass filter to suppress the components in the video spectrum. In general, it is best to 'tap' the signal ahead of this filter. The minimum level of the signal to be fed to the NICAM decoder is about 50 mV. In all cases, the load presented by the input of the NICAM decoder should be as small as possible. This may require an emitter follower to be fitted as discussed below.

A little more complex, but certainly more convenient as far as the filtering is concerned, is a TV set or a VCR with a so-called quasi-parallel sound demodulator system. The designer used his HR-S5000E video recorder from JVC to supply the NICAM signal. After studying the service documentation that came with the VCR, it

COMPONENTS LIST

Resistors:

1	374Ω (see text)	R1
1	499Ω 1%	R2
4	2kΩ2	R3;R4;R21;R22
12	10kΩ	R5;R6;R9;R12;R17; R18;R24;R26;R32; R37;R39;R40
4	100Ω	R7;R8;R33;R38
3	100kΩ	R10;R13;R16
1	82kΩ	R11
1	680kΩ	R14
3	2Ω2	R15;R19;R20
2	27kΩ	R23;R25
2	3kΩ3	R27;R28
2	4kΩ53 1%	R29;R34
2	12kΩ1 1%	R30;R35
2	68kΩ	R31;R36
2	150Ω	R41;R42
3	470Ω	R43;R44;R45
1	15Ω	R46
1	2kΩ5 preset H	P1

Capacitors:

5	47nF ceramic	C1;C49-C52
2	10nF ceramic	C2;C6
20	100nF	C3;C4;C5;C12;C13; C19-C25;C34; C36-C41;C43
4	18pF	C7;C8;C14;C15
4	1nF ceramic	C9;C10;C16;C17
1	33nF	C11
3	2nF2	C18;C26;C27
2	47µF 16V radial	C28;C29
2	4nF7	C30;C31
2	2µF2 50V solid MKT	C32;C33
1	10nF	C35
1	10µF 10V	C42
1	220µF 16V	C44
2	10µF 25V	C45;C46
1	2200µF 25V	C47
1	220µF 25V	C48

Semiconductors:

4	BB405	D1-D4
2	BAT85	D5;D6
5	LED red 3mm	D7-D11
3	1N4148	D12;D13;D14
1	B80C1500	B1
1	NE592	IC1
1	MAS7A101	IC2
1	MAS7D102	IC3
1	MAS7A103	IC4
3	NE5532AN	IC5;IC6;IC7
1	4051	IC8
1	XR2204 or ULN2004	IC9
1	7805	IC10
1	7812	IC11
1	7915	IC12

Miscellaneous:

1	3-way pin header with jumper	JP1
3	RCA (phono) socket	K1;K2;K3
1	2-way PCB terminal block; pitch=7.5mm	K4
3	Digitast push-button (narrow) with integral LED	S1;S2;S3
1	mains transformer 2×15V @ 4.5VA; Monacor (Monarch) type VTR-4215	Tr1
1	TH316BQM-2080QDAF *	Fl1
1	TH316BQM-2110QDAF **	Fl1
2	A258BLV-5085N	Fl2;Fl3
1	Quartz crystal 23.400 MHz *	X1
1	Quartz crystal 26.208 MHz **	X1
1	Quartz crystal 5.824 MHz	X2
1	Fuse 50mA slow; with PCB mount holder and cap	F1
1	Printed circuit board	910035
1	Front panel foil	910035-F
1	Metal enclosure Telet 55205	

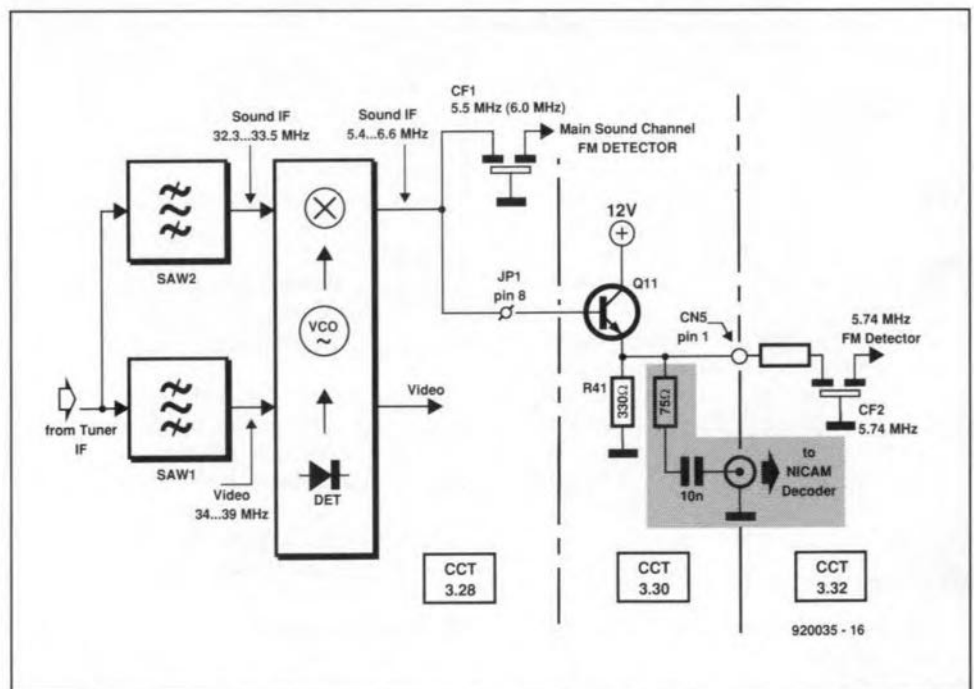* PAL TV system B or G
** PAL TV system I

Fig. 6.   This drawing illustrates how a suitable decoder input signal was found in the JVC HR-S5000E video recorder.
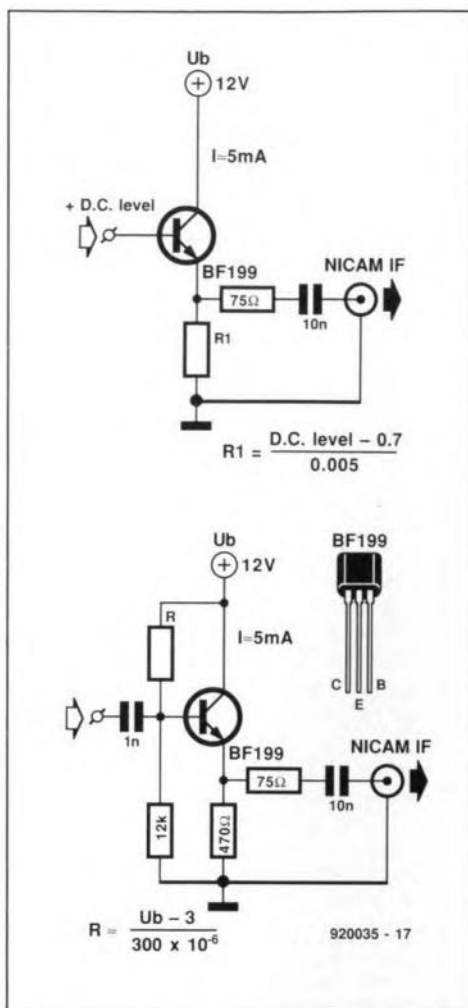
Fig. 7. Emitter followers for NICAM signals on a relatively small d.c. component (7a), and NICAM signals on a d.c. component so large that a.c. coupling is required (7b).

$$R1 = \frac{D.C.\ level - 0.7}{0.005}$$

$$R = \frac{Ub - 3}{300 \times 10^{-6}}$$

was decided to try the output signal of an emitter follower located between the 'sound IF' output and the input of the 5.74 MHz ceramic filter fitted for the German 'dual-language' demodulator. The search for this emitter follower, Q11, was complicated by the fact that it happened to 'reside' between three pretty large circuit diagrams. Figure 6 shows essentially what has been added to the VCR: one resistor, a coupling capacitor and a 'phono' socket do a perfect job.

As already mentioned, an emitter follower may have to be used to prevent the input signal of the sound demodulator disappearing when the NICAM decoder is connected. One of the circuits shown in Fig. 7 will be adequate. The first, Fig. 7a, may be used when the signal is superimposed on a d.c. level between 0.3 and 0.7 times the supply voltage. The other, Fig. 7b, has an input coupling capacitor, and is used in all other cases. Remember, you are dealing with signals of 5 MHz and higher here, so keep component wires as short as possible.

Testing

The input impedance of the NICAM decoder is fairly high: about 900 Ω. This means that conventional coax cable with an impedance of 50 Ω or 75 Ω can not be used unless its length remains below 50 cm or so. Longer

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cables of either type will cause reflections and serious mismatches, resulting in attenuation of the NICAM subcarrier. If you can not go round the use of a relatively long, low-impedance, coax cable between the TV set and the NICAM decoder, be sure to fit a terminating resistor across socket K1. This resistor prevents reflection and high-frequency loss to some extent. When a 50-Ω cable is used, fit a 52.9-Ω terminating resistor, and change R1 into 444 Ω. Similarly, when a 75-Ω cable is used, terminate it with 81.8 Ω, and change R1 into 431 Ω. In some

cases, ordinary screened cable as used with audio equipment, or car radio coax cable (if you can get it), is the best alternative. In any case, do not fit BNC or similar low-impedance RF sockets at the TV side and the decoder input. On the prototype we used an insulated 'phono' (RCA-style) socket for chassis mounting. An insulated socket is required to prevent an earth loop between analogue and digital ground rails.

Demodulator input level
Switch on the NICAM decoder, and tune the

PROGRAMMING THE MAS7D102 NICAM DECODER

The bus format can be selected either by applying logic levels to pins Config4 and Config3, or by programming control bits Config4 and Config3 via the I²C microprocessor interface.

Config 4	Config3	DAC bus format
0	0	High-Z
0	1	S-bus
1	0	I²S bus
1	1	Toshiba DAC bus

The pins Stereo, Mono1 and Mono2 are active-low outputs that indicate the current NICAM transmission mode.

Stereo	Mono1	Mono2	Type of transmission
0	1	1	Stereo signal
1	0	1	Dual language transmision
1	1	0	One mono sound channel and 352 Kbit/s data channel
1	1	1	No sound signal. Transparent 704 Kbit/s data transmission, or no NICAM encoded transmission

During dual-language transmissions, the main language selection is controlled by input pins Config2 and Config1.

Config2	Config1	DAC bus	Sound sample order			
0	0	I²S/Toshiba	M1	M1		
0	1	I²S/Toshiba	M1	M2		
1	0	I²S/Toshiba	M2	M1		
1	1	I²S/Toshiba	M2	M2		
0	0	ITT	M1	M1	M1	M1
0	1	ITT	M1	M1	M2	M2
1	0	ITT	M2	M2	M1	M1
1	1	ITT	M2	M2	M2	M2

The decoder has two addresses on the I²C bus. Address 4E (hex) is for writing to the decoder, and address 4F (hex) for reading from the decoder.

There are three status registers (read) and three control registers (write) that can be accessed. The three control registers can be addressed individually by the two most significant bits of each control word. The three status registers can be addressed as a complete set only.

Control register	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	Test1	Test2	MuteS	MuteA	x	Reset
2	0	1	x	x	Config4	Config3	Config2	Config1
3	1	Da	Db	Dc	Pa1	Pa0	Pb0	Pc0

- Test1 and Test2 are reserved for test purposes, and must be set low.
- The MuteS control bit mutes sound output. Active high.
- The MuteA control bit mutes sound output and resets the synchronisation of the decoder completely. Active high.
- The Reset control bit resets the decoder completely. Active high.

The function of the Da, Db and Dc control bits is to define external ports Pa, Pb and Pc as inputs or outputs, as shown below.

Da	Db	Dc	Pa1	Pa0	Pb0	Pc0
0	0	0	out	out	out	out
0	0	1	out	out	out	in
0	1	0	out	out	in	out
0	1	1	out	out	in	in
1	0	0	in	in	out	out
1	0	1	in	in	out	in
1	1	0	in	in	in	out
1	1	1	in	in	in	in

The **status registers** of the MAS7D102 have the following structure:

Status register	D7	D6	D5	D4	D3	D2	D1	D0
1	Osn	CI1	CI0	C4	C3	C2	C1	C0
2	Ser10	Ser9	Mute	TestS	Pa1	Pa0	Pb0	Pc0
3	Ser8	Ser7	Ser6	Ser5	Ser4	Ser3	Ser2	Ser1

- The Osn status bit goes high when the decoder is not synchronised.
- CI0 and CI1 are the two CI bits extracted from each NICAM frame.
- C4-C0 are the C bits associated with the current NICAM transmission, and they indicate the mode as shown below.

C1	C2	C3	NICAM transmission mode
0	0	0	Stereo transmission
0	1	0	Dual language transmission
1	0	0	One mono channel plus data transmission
1	1	0	One 704 Kbit/s data channel

- C0 is the Frame Flag bit that indicates the super frame pattern of the NICAM transmission.
- C4 is the Reserve Sound Switching flag, which goes high when the FM mono signal carries the same programme as the digital stereo signal.
- The Mute status bit goes high to indicate that the decoder has been muted for some reason.
- TestS is a test status indication bit reserved for test purposes.
- Pa1 and Pa0, Pb0 and Pc0 indicate the status of the corresponding external pins, when they are configured as input ports.
- The Ser10-Ser1 bits show the value contained in the sample error counter. This counter is incremented whenever an erroneous sample is detected. The control processor can read the error count at suitable time intervals, and take decisions depending on the error rate.

TV set or the VCR to a station transmitting NICAM sound. Use an oscilloscope to check the signal level at pin 3 of the QPSK demodulator, IC2. The level should be between 200 mV$_{pp}$ and 800 mV$_{pp}$. If necessary, adjust preset P1 to achieve a level of about 500 mV$_{pp}$.

QPSK demodulator PLL adjustment
Connect the scope to pin 11 of the QPSK demodulator IC. You should see a so-called 'eyes' waveform (which may be very difficult for the scope to trigger on). Adjust P1 so that the tops of the waveform are just below the supply voltage; i.e., they are just not clipped. This gives a signal level of about 5 V$_{pp}$. Move on to pin 7 of IC2. This supplies the error voltage of the demodulator PLL. It is a fairly 'messy' signal superimposed on a direct voltage, which will look like a broad band on the scope. Tune to a non-NICAM station, and back to the NICAM station again, to see how the PLL responds by locking on to the NICAM signal. For best performance of the PLL, the d.c. component in the error signal should be at about half the supply voltage, i.e., 2.5 V. When it is too close to either 0 V or +5 V, change the crystal matching capacitors, C7 and C8, until the centre of the band is at about 2.5 V. Increase the capacitor values (to 22 pF or 27 pF) when the d.c. component is too low, and decrease them (to 15 pF or 12 pF) when the d.c. component is too high. Try to get as close to 2.5 V as you can. The exact oscillator frequency will be very difficult to measure at pin 5 of IC2 because the impedance is high locally. This means that any capacitive load, however small, formed by a test probe will detune the crystal oscillator to some extent.

Clock recovery PLL adjustment
The 5.824-MHz PLL for the NICAM clock signal recovery is adjusted in a similar manner to the QPSK PLL as discussed above. Connect the scope to pin 18 of IC2, and check that the error voltage has a d.c. component of about 2.5 V. If not, change the values of C14 and C15. It will be found that this error voltage is much 'cleaner' than the one used for
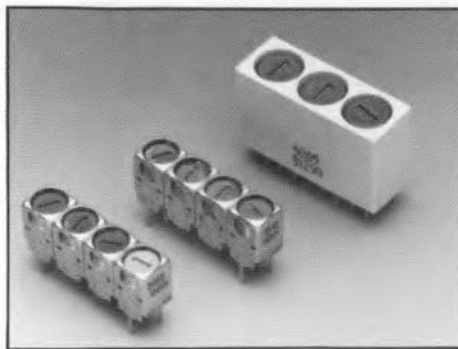

Fig. 8.   The Toko QPSK bandpass filter (either for system I or B/G) and the 15-kHz low-pass filter used in the decoder.

controlling the first PLL. If the second PLL frequency is correct, pin 23 of the demodulator IC supplies a clock signal of 728 kHz, which is easily measured with a frequency meter.

That completes the adjustment of the NICAM decoder. If you have not already done so, connect a stereo amplifier to the outputs, and enjoy the programme!

Finishing touch

Some of you may want to fit the decoder permanently inside a TV set, while others may want to use it as a self-contained unit.

The prototype of the decoder was housed in an aluminium enclosure Type 55205 from Telet. The decoder and supply boards were fitted on a perspex plate that could be slid horizontally into the railings provided along the inside of the front and rear panels.

The keyboard PCB and the mains switch are fitted on to the front panel, for which a ready-made self-adhesive foil is available. This foil is used as a template to determine the locations of the holes to be cut in the front panel. A jig-saw is used to cut the rectangular clearances for the mains switch and the three push-buttons.

The keyboard PCB is mounted on four screws of which the (countersunk) heads are glued to the inside of the front panel. Plastic

stand-offs are used to fit the PCB at the right distance behind the front panel.

The rear panel is drilled to hold the mains socket, the NICAM input socket and the two audio output sockets.

Conclusion

The NICAM decoder described here has been in use for some time now, and provides excellent stereo sound on broadcasts received from BRT1 and BRT2. Regrettably, the unit could not be tested in the UK, although suitable components (a 6.552-MHz QPSK bandpass filter and a 26.208 MHz quartz crystal) were available.

Although the construction and adjustment of the unit are fairly simple, finding a suitable input signal may be daunting if you have little experience in TV and VCR technology. We feel, therefore, that it is fair to warn beginners not to undertake this project until a dedicated TV tuner is available, which will be described in a future issue of *Elektor Electronics*.

Postscript for advanced users

As already mentioned, the MAS7D102 NICAM decoder has optional I²C control, which may be used to access most of the internal registers. The SDA and SCL inputs of this IC are TTL-compatible, and may be connected to an I²C bus via appropriate interfaces. If you have a PC available fitted with an I²C interface (Ref. 1), you may use the information given in the MAS7D102 inset to implement software control on the NICAM decoder.

The descrambler on board the MAS7D102 can be loaded with a descrambling key other than the standard 'seed' used for non-encrypted NICAM broadcasts. Changes to the scrambling keys must occur synchronously at the transmitter and the receiver(s). The NICAM decoder IC provides a serial data input, Dsdata (pin 6), and a clock input, Dsclk (pin 5) to access an internal shift register. This register contains the descrambler key that is loaded in parallel into the descrambler one per frame. The shift register contents can be updated at any time with a maximum clock rate of 5 MHz. The time interval between the falling edge of the Ngate signal (pin 39) and the rising edge of the Agate signal (pin 38) is not allowed for descrambler key updating. During this interval, Dsclk (pin 5) must be held static. Output signals C0 (pin 35), Agate and Ngate may be useful for synchronisation purposes.

Happy listening!   ∎

Reference:
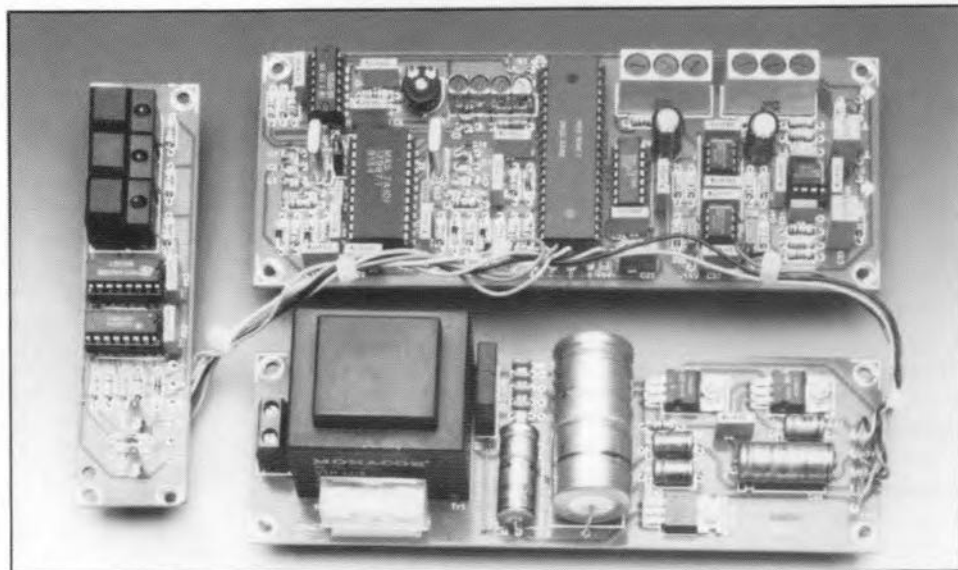1. I²C interface for PCs. *Elektor Electronics* February 1992.

Fig. 9.   Completed printed circuit boards: main decoder board, keyboard and PSU.

AUDIO-VIDEO PROCESSOR TYPE AVP300 – PART 1

An ELV design

THE audio-video processor is best compared to the control amplifier in an audio system. That, too, gives a choice of input signals. Where required, the signal standard may be changed. The quality of the signal can be modified in a manner comparable to tone control. Finally, the signal is output in a number of ways (as in tape and line outputs).

The design of the processor can be seen in the block diagram in Fig. 1. In the first instance, this diagram will be analysed stage by stage; this will at the same time give a sort of user instruction. The technical aspects will follow naturally when the various circuit diagrams are discussed.

Inputs and outputs

At the rear of the processor are no fewer than 16 different connectors—see Fig. 2. Which of these are required in any given situation depends on the type of termination of the relevant cable and on the available signal.

Video 1/6 is an input with dual function via a SCART* connector (also called Euroconnector). When used as Video 1 input, it is fed with a CVBS (Chroma, Video, Blanking, Synchronization) signal, which is sometimes just called composite video signal.

When used as Video 6 input, it accepts signals from an S-VHS recorder or camera. These signals consist of two components: chroma for colour information and VBS (black-and-white) for brightness.

The audio signals associated with these inputs are also applied via the Euroconnector.

Video 2 is a SCART* input for CVBS and RGB (Red, Green, Blue) signals; selection of either is effected by a slide switch. When the switch is in position CVBS, it is possible, with the aid of a computer and a genlock, to mix CVBS and RGB signals. It is planned to publish the design of a genlock later this year.

Video 3 is a BNC input for a CVBS signal. The associated audio signal is input via the two audio sockets next to the BNC socket.

Video 4 is a second SCART* socket that can also be used to input a CVBS signal. Moreover, it provides CVBS and RGB output signals. This arrangement is intended primarily for the standards conversion. To that end, the socket should be linked to the SCART socket on the television receiver. The tuner of the receiver will

The Type AVP300 audio-video processor is a multi-standard equipment that can be used almost anywhere in the world. It can translate between the three television standards (PAL, NTSC, and SECAM), hop from one type of signal to another (S-VHS, Hi-8, RGB, CVBS), and enables audio and video signals to be modified: video signals as regards colour saturation, contrast, brightness and the balance between red, green and blue, and audio signal(s) in respect of tone, balance and volume. Moreover, it has a (limited) facility for mixing signals.

then provide the CVBS signal, whether NTSC, SECAM or PAL, to the processor. The processor translates this signal into an RGB signal and sends it to the TV receiver. At the same time, the blanking line is switched to arrange the TV receiver displaying the signal at the RGB inputs, that is, the converted signal, instead of that from its integral tuner. There is only one but: not all TV receivers, particularly older models, have RGB inputs on the SCART socket.

Video 5 is a mini DIN socket for inputting S-VHS signals. The associated audio signals are fed to the processor via audio sockets.

Video 7 is a mini DIN socket for outputting S-VHS signals. Again, the associated audio signals are output via standard audio sockets.

Video 8 is another SCART* socket for out-

putting CVBS or S-VHS signals: which one is determined by a switch adjacent to the socket. If the socket is used for S-VHS signals, nothing must be connected to Video 7, because of the terminating impedance of the S-VHS output. If a recorder or TV receiver is connected to Video 7, Video 8 may be used as a CVBS output only.

Audio 1–8 are the audio inputs and outputs associated with the correspondingly numbered video inputs and outputs.

Audio 9 (two sockets) is intended for feeding independent audio signals to the processor. These signals can either be mixed with the original sound or replace it.

Audio 10 (3.5 mm jack socket) is a stereo microphone input.

* Named after the French organization that proposed this 21-way connector in the early 1980s: **S**yndicat des **C**onstructeurs d'**A**ppareils **R**adiorécepteurs et **T**éléviseurs. The connector has since become a European standard.

Audio 11 is a headphone output via which the signals before *and* after the control amplifier can be heard.

Port is an 8-way DIN socket, via which external equipment can be used to control various functions of the processor. It will enable, for instance, the inputting of yet-to-be-developed video effects in the future without any further work on the processor.

Standards conversion

The processor can handle video signals of the following standards: PAL, SECAM, NTSC 3.58 MHz and NTSC 4.43 MHz. It is able to recognize these standards automatically and modify the chroma-VBS separation filter accordingly. Which standard is recognized is indicated by LEDs. Selection of positive or negative video signals is effected manually by a switch at the rear of the processor.

Also at the rear panel are the switches for setting the standard of the output signal, which is PAL or NTSC. In the case of NTSC, a further selection must be made of the colour carrier (3.58 MHz or 4.43 MHz). In the case of PAL, the switch *must* be set to 4.43 MHz.

Furthermore, the processor can be used to transform a conventional TV receiver into a multi-standard model (for relevant connections, see under Video 4).

Formats conversion

Apart from video standards, the processor can convert each of the signal formats S-VHS, RGB and CVBS to either of the other two. This is largely a matter of choosing the correct input and output connectors. Note that the CVBS/RGB-in switch (next to the Video 2 input) *must* be set to CVBS if an S-VHS or CVBS signal is input, irrespective of to which socket.

S-VHS to RGB: S-VHS signals can be input via the Video 5 or Video 6 sockets; the input switch must be set accordingly. The RGB signal is available at output Video 4: the CVBS/RGB-out slide switch must be set to RGB.

S-VHS to CVBS: S-VHS signals are input via the Video 5 or Video 6 sockets. The output may be taken from Video 4 or Video 8; both of these may be used simultaneously. The associated switch near these outputs must be set to CVBS.

RGB to S VHS: RGB signals are input via Video 2. The corresponding RGB/CVBS switch must be set to RGB. If this switch is in position CVBS, it may be changed over to RGB by applying a voltage of 1–3 V to pin 16 (blanking). The S-VHS signal may be taken from Video 7 or Video 8 (*not* simultaneously). The switch associated with Video 8 must be set to S-VHS.

RGB to CVBS: RGB signals are input via Video 2. The CVBS signal may be taken from Video 4 or Video 8; both of these may be used simultaneously. The switches at both the outputs must be set to CVBS.

CVBS to S-VHS: CVBS signals may be input via Video 1, Video 2 or Video 3. The converted signal is available at Video 7 or Video 8.

CVBS to RGB: CVBS signals may be input via Video 1, Video 2 or Video 3. The converted signal is available at output Video 4; the associated switch must be set to RGB.

Quality of converted formats

Retention of quality during the conversion from one format to another is ensured by special stages similar to those found in modern television receivers. However, in the case of conversion of CVBS signals. there may be a slight loss of quality. This is because the stripping of the chroma information from the signal tends to be troublesome: this, together with the limited bandwidth of standard VHS recorders, is the reason that the chroma and VBS components of the signal are kept separated in S-VHS recorders. In the conversion to a CVBS signal, there is no loss of quality. This assumes, of course, that the TV receiver and recorder connected to the processor are of good quality.

Controls

A close look at the block diagram in Fig. 2 shows that the processor resembles a modern multi-standard television receiver less the RF and CRT sections. The video section is the largest and most interesting part of the processor. Input signals follow two paths to the video colour controller. RGB signals from Video 2 are fed directly to this stage, but S-VHS and
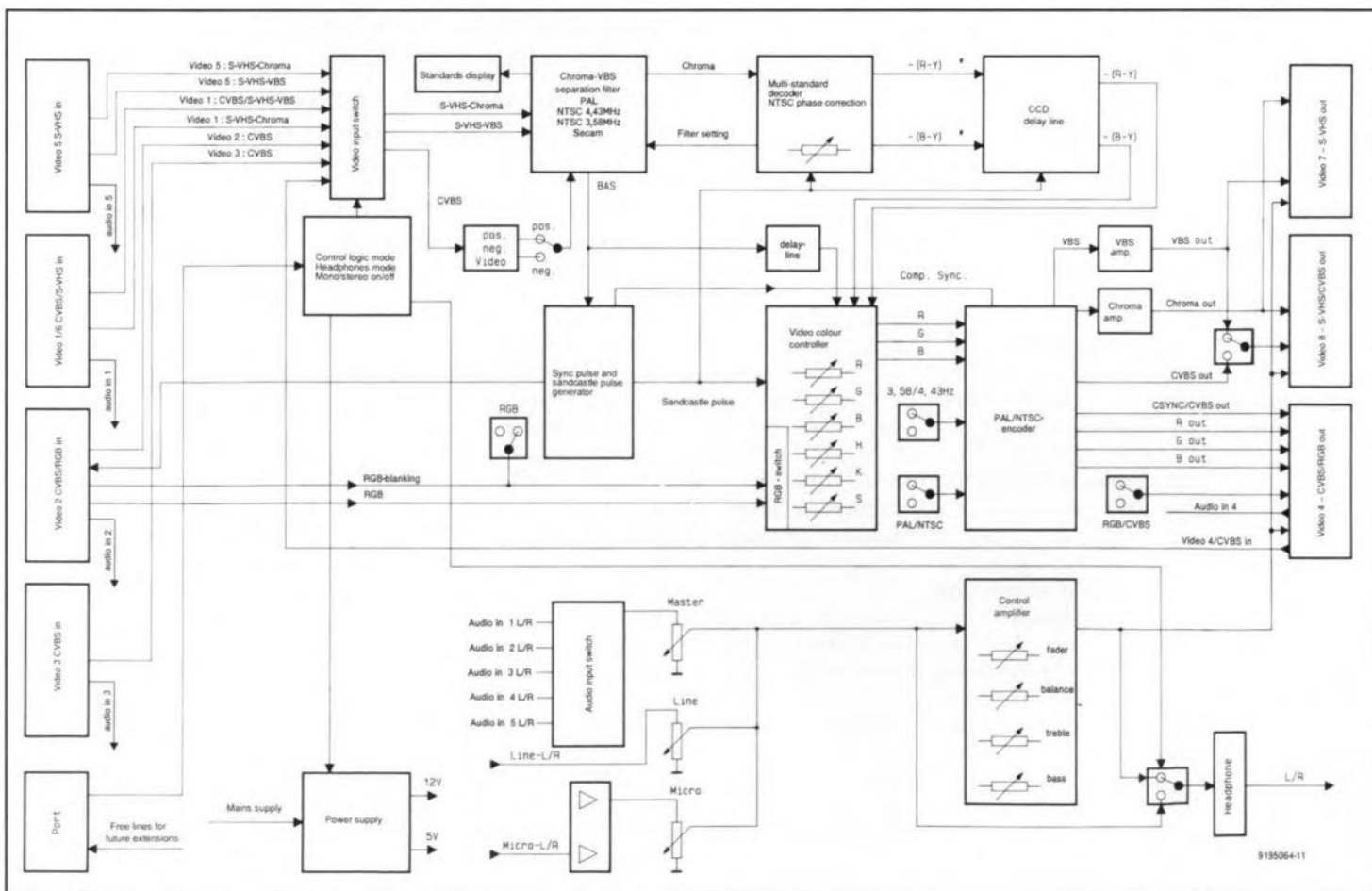

Fig. 1. Block diagram of the Type AVP300 audio video processor.

Fig. 2. Rear view of the audio video processor showing the 16 input sockets and the various switches.

CVBS signals must be decoded first. Switching between the decoded signals and RGB signals is carried out electronically in the decoder. The control signal for that is the RGB blanking signal. If the CVBS/RGB switch is set to position RGB, the output signals of the decoder relating to S-VHS and CVBS components are switched off by the controller. This is why it was emphasized earlier on that this switch must be set to CVBS.

S-VHS and CVBS signals are first applied to an input selector, an electronic switch that is operated by press button MODE on the processor. S-VHS signals are taken from the switch directly to the chroma-VBS separation filter. CVBS signals are first passed through a switchable inverter to enable positive as well as negative video signals to be processed. Normally, the switch is set to negative.

Readers may well ask why S-VHS signals are applied to the chroma-VBS separation filter, since these components are already separated in this format. That is, of course, so and with S-VHS signals the filter therefore serves as a buffer only. If, however, a CVBS signal is applied, the filter separates the sub-carrier and colour signal from the black-and-white (VBS) signal. The filter has two settings: one for PAL, SECAM and NTSC with a colour subcarrier of 4.43 MHz and the other for NTSC with a colour sub-carrier of 3.58 MHz. The setting is determined by the multi-standard decoder as soon as this stage has detected which TV standard is used. At the same time, the type of standard is indicated by LEDs.

Following the filter, the chroma and VBS signals follow separate paths. To begin with, the VBS signal is applied to the sync pulse and sandcastle pulse generator, which derives new sync pulses from it. Separate line and field sync pulses, as well as sandcastle pulses, are fed to the Video 2 input. Sandcastle pulses indicate the various stages of the line, field and blanking pulses by voltage levels.

The sandcastle pulse is also applied to the video colour decoder, the multi-standard decoder and the CCD (**C**harge **C**oupled **D**evice) delay line to ensure that these stages perform their functions at the right moment.

The sync pulse and sandcastle pulse generator also provides a composite sync (BS or **B**lanking/**S**ynchronization) signal. This is used to re-render the picture signal, after it has been processed, into a VBS or CVBS signal, and also serves as sync signal for the RGB output.

The black-and-white signal is applied not only to the sync pulse and sandcastle pulse generator, but also to the video colour controller. In its path there is a delay line that prevents it arriving too early at the controller: the chroma signal is also delayed during decoding.

The chroma signal is fed to the multi-standard decoder, where it is demodulated (stripped of the 4.43 MHz or 3.58 MHz sub-carrier) and split into two colour-difference signals. To give the correct colour to the colour-difference signals, the decoder needs a reference, and this is provided by the NTSC phase preset. That control is not required with PAL or SECAM, because signals in those formats already contain a reference. With NTSC signals, the preset needs to be adjusted until the colours appear natural or as natural as possible.

From the multi-standard decoder, the two colour-difference signals are applied to a CCD delay line. There, the incoming picture line is compared with the previous picture line stored in the delay line. This arrangement enables the removal of any errors in the colour-difference signals.

The input signals have then been processed to the stage where they can be applied to the video colour controller—the heart of the audio video processor. Although the colour information has not been completely decoded at this stage, the video colour controller correctly converts the colour-difference signals to RGB (bear in mind that the controller is just one IC). The recaptured RGB signal is applied to the RGB switch of the video colour controller. This electronic switch enables the selection of either the S-VHS/ CVBS signal or the RGB signal. It is so fast that it is suitable for mixing the S-VHS/CVBS signal with the RGB signal. Although this requires external effects equiment, the actual mixing takes place in the video colour controller.

After the RGB signal has passed the RGB selector, the video colour controller lives up to its name: it enables changing the depth of each of the three colours (red, green and blue) by up to ±40%; it also has controls for adjusting the brightness, contrast and colour saturation.

After it has been processed in the video colour controller, the RGB signal must be revamped for transmission. That is simple if an RGB output is wanted: only a composite signal then needs to be added to it. If an S-VHS or CVBS is required, a modulator is needed: in Fig. 1, this is called PAL/NTSC encoder. That name already indicates that both PAL and NTSC signals can be provided. The standard of the output signals is determined with a switch. If that is set to NTSC, a second switch allows setting either of two frequencies for the chroma sub-carrier.

The audio section is arranged in a similar manner, but contains far fewer components. Audio signals are also input via switches, which are operated together with those for the video signals. In that way, the audio signal at the master potentiometer is always associated with the present video signal.

There are also two inputs for independent audio signals that can be mixed with the original sound. If the master potentiometer is turned off, the audio signals at these inputs can be used as a new sound for the present picture.

One of the two inputs is for line signals, the other for microphone signals. Microphone signals are first amplified to the same level as other audio signals.

After the audio signals have been mixed with the aid of the three slide potentiometers, they are applied to the control amplifier. A fader allows the volume of the mixed audio signals to be altered gradually.

The control amplifier also has controls for high and low tones and balance, as well a a mono/stereo selector.

Audio signals can be listened to with headphones. These signals may be taken either from the input or from the output of the control amplifier: selection is by means of a switch. This enables the audio input to be monitored with the fader 'off'. ∎

Next month's instalment will describe the circuit of the video section.

SCIENCE & TECHNOLOGY

DIGITAL SHORT-RANGE RADIO

by Brian P. McArdle

1. Introduction

An interim standard for Digital Short Range Radio (DSRR) has been approved recently by the European Telecommunications Standards Institute (ETSI). The institute was established by the European Community to assist with the harmonization of equipment specification and frequency allocations in member countries. The DSRR interim standard is one of its first radio specifications. It will go forward for public enquiry and, in due course, become a standard applicable in every community state. There could be modifications, but the interim standard will probably remain the basis of the final specification. After the standard has been finalized, no modifications can be introduced by individual states. In time, DSRR should become a true European radiocommunications system.

DSRR is a major advancement in business radio and should reduce many of the present problems. There are explained further in Section 2. The interim standard has a number of requirements in regard to control signalling and protocols which, at present, are not in general use. Because of developments in digital signal processing, these should not create major problems for manufacturers in the various countries. However, it also proposes the use of two frequency bands of 888–890 MHz and 933–935 MHz, known as the Low Band (LB) and the High Band (HB) respectively. The significance of two separate bands is explained in Section 3. This could result in difficulties, because EC countries are still far away from true frequency harmonization. Since the EC is committed to harmonization and the removal of trade barriers, it is considering a directive to all member states that, in order to reduce any problems in the introduction of DSRR, priority should be given to DSRR over other services in the proposed bands. At present, DSRR appears to be on target for wide use within a few years.

2. PMR channels

The channels are usually assigned for dual frequency operation, which means that a unit transmits and receives on different frequencies as in Fig. 1. If a base station has f_c and f_r as its transmit and receive frequencies, a mobile station operating to the base station must have f_r and f_c as its transmit and receive frequencies respectively. In the United Kingdom, equipment for this service must conform to the Performance Specification MPT1326. This is a fundamental specification and DSRR units must meet a similar specification—see Appendix 5. The difference is the method of operation and the use of the channels.

In the PMR (Private Mobile Radio) service, the main barrier to further development is the method of using the radio frequency spectrum. In assigning channels to users, there is insufficient spectrum for every user to have his own channel. That means that a number of users must share the same channel. This, in turn, causes a nuisance effect and loss of confidentiality since every message on a channel is detected by every receiver irrespective of the intended destination. Tone control, like EEA or ZVEI, can be used to minimize this effect. At the start of a message a transmitter sends a specific sequence of tones. Only the intended receiver can identify the sequence and is activated from the point of the operator. If an incorrect sequence, that is, a sequence for a different receiver, is detected, the receiver remains deactivated. Unfortunately, this process does not solve the problem of channel sharing. A common occurrence is that two users wish to use the channel at the same time. Therefore, each user must monitor the channel to ascertain that it is free before he can commence operation. Queues often occur despite the fact that many channels are regularly idle. DSRR should reduce this problem by making more efficient use of the spectrum. It should also improve user confidentiality without the need of secrecy operations, that is, encryption procedures.

3. DSRR frequency bands

There are two bands of 2 MHz in which channels are assigned with 25 kHz channel spacing as follows.

Channel	High band	Low band
01	933.025 MHz	888.025 MHz
02	933.050 MHz	888.050 MHz
03	933.075 Mhz	888.075 MHz
...	...	...
77	934.925 MHz	889.925 MHz
78	934.950 MHz	889.950 MHz
79	934.975 MHz	889.975 MHz

Channels 01 and 79 are used as control channels for selective signalling (SSC) and cannot be used to transmit or receive voice or data. The traffic channels are 02 to 78 inclusive: the usual type of operation illustrated in Fig. 2. Two units, A and B, operate to each other through a repeater or master unit. This is dual-frequency operation with repeaters and master units transmitting in the High Band and receiving in the Low Band. Units (mobiles) transmit in the Low Band and receive in the High Band. If A and B want to operate directly to each other, single frequency operation would be used. In this method, the units transmit and receive on the same channel in the same band: High Band.

In operation, a unit will scan and identify a free traffic channel which is subsequently used for voice or data. The number of the

1

Base Station
Transmit Frequency f_c
Receive Frequency f_r

Mobile Station
Transmit Frequency f_r
Receive Frequency f_c

920057 - 11

2

Low Band

Master Unit or Repeater

Low Band

High Band

user A

user B
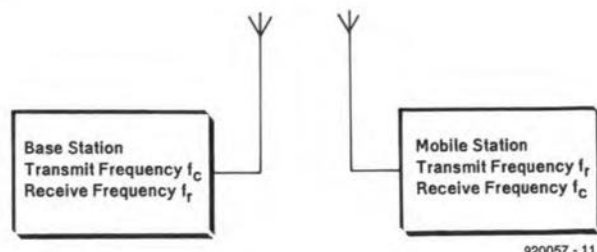
920057 - 12
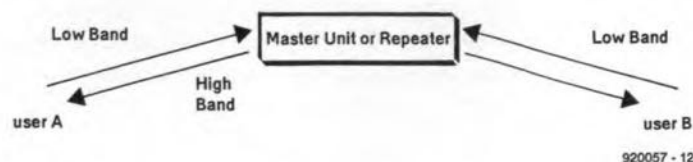
particular traffic channel plus certain control signals are transmitted to the intended receiver on the control channels. In order to avoid congestion, where a number of units would be considering the same traffic channel, there is a specific algorithm for channel spacing:

$$N_j = (N_{j-1} + 1) \bmod 77 + 2 \qquad [Eq.1]$$

for j>0 where N_0 is the seed. Thus, the mathematical operation is an additive congruence generator where N_j will only take values between 2 and 78 inclusive. The two control channels, 01 and 79, will be excluded automatically. If a different seed is used by different units, the chances of two or more units identifying and choosing the same channel would be greatly reduced. On switch-on, the seed is the least significant 7 bits of the call code (refer SSC). For successive seeds, the least significant 7 bits of the 16 check bits of the previous SSC is used. This is discussed in more detail in Section 5.

4. DSRR modes of operation

There are three main modes of operation.
a) In the *standby mode* a unit monitors 2 control channels for the appropriate control signals. It does not transmit or receive voice or data.
b) In *call set-up mode* a unit transmits and receives control signals but no voice or data.
c) In *communication mode* a unit is in full operation, that is, transmitting and receiving voice or data. Control signals are also transmitted and received in this mode.

Consider an example where user A wishes to contact user B in single-frequency operation. The main steps can be summarized by the following procedure, in which it has been assumed that A has just been switched on and is in the standby mode.
i) A enters call set-up mode. The traffic channels are scanned to find a free channel. If no channel is available, the unit will return to standby mode.
ii) A transmits an SSC on the control channel to B. This code includes identifiers for A and B, number of proposed traffic channel, and so on. The format of the code words is discussed in Section 5. A switches to receive mode on the control channel.
iii) B transmits an ACK to A on the control channel and switches to receive mode on the traffic channels specified in the SSC from A. On receipt of the ACK from B, A switches to the traffic channel. If no ACK or another SSC different from ii) is received by A, a set of retry procedures is implemented.
iv) A transmits the call set-up SSC as in ii) on the traffic channel to B. B sends an ACK and both units enter communication mode. If no voice or data is transmitted after 10 seconds, or if the traffic channel has become busy between ii) and iv), or the SSC or ACK is not received, both units revert to standby mode.
v) In communication mode, all transmissions are preceded by a full SSC. There is a limit of three minutes to the time in communication mode in order to avoid congestion. In addition, if no valid voice or data is received after a certain period (5 seconds, or 10 if the unit has just entered the mode), both units return to the standby mode.

This is a simplified description and the reader should consult the official standard for a proper explanation. For operation through repeaters or master units, the procedure must be varied. However, the entire operation is a major change from the present method for PMR. The digital signal processing as in the SSC and ACK control signals is central to the system.

5. Selective signalling code

The selective signalling code (SSC) is a block of 568 bits which is fundamental to DSRR operation in all mode. It is sub-divided into the following blocks.
a) Preamble of 256 bits of 1010...,etc. (bit reversal) for bit synchronization of the decoder in the receiver.

b) Frame synchronization of 16 bits to establish code word framing in the decoder of the receiver.
c) Code word of 88 bits.

b) and c) are transmitted three times as in Fig. 3.

3

| Preamble 256 | Frame Synchronization 1 16 | Code Word 88 | Frame Synchronization 2 16 | Code Word 88 | Frame Synchronization 3 16 | Code Word 88 |
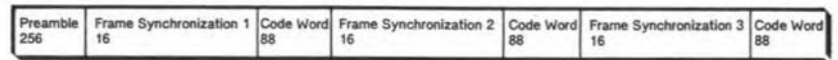
920057 - 13

The code word in c) is sub-divided further as follows.

SSC number	1
Traffic channel code	7
First call code	24
Command code	4
Reserved	2
Code word counter	2
Manufacturer's code	8
Second call code	24
Cyclic redundancy check	16

72 bits

The 16 check bits are generated from the 72 other bits by a (88, 72) cyclic code which has as its generator polynomial

$$x^{16}+x^{14}+x^{12}+x^{11}+x^9+x^8+x^7+x^4+x+1.$$

This should be a factor of $(x^{88}+1)$ as per the mathematical conditions for cyclic codes. Refer to Appendix 1 for the various factors and other information. The code is supposed to have a *Minimum Distance* of 6 which will permit detection of up to five errors per word. This is the minimum number if differences in any two code words of 88 bits and is explained further in Appendix 2. The encoding operation can be summarized in the following steps.

1) Code word $(d_{72}\, d_{71}\, d_{70} \ldots d_3\, d_2\, d_1)$ before the check bits are generated.
2) Code word

88 87 86 ... 19 18 17	16 15 14 ... 3 2 1
$d_{72}\, d_{71}\, d_{70} \ldots d_3\, d_2\, d_1$	* * * ... * * *
Data bits	Check bits

3) Code word can be written as a polynomial over GF(2) as follows:
$$d_{72}\, x^{87} + d_{71}x^{86} + \ldots d_3 x^{18} + d_2 x^{17} + d_1 x^{16}$$
with the check bits taken to be zero in each of the terms from x^{15} to x^0.
4) Polynomial in 3) is divided by the generator polynomial and the remainder, which is a polynomial of degree 15 with terms from x^{15} down to x^0, is added back to the original polynomial in 3) to produce the new revised polynomial of the final code word The * in each location from 1 to 16 has now been replaced by a '1' or '0' as appropriate.
5) The final check bit corresponding to the coefficient of x^0 is inverted in order to give protection against misframing in the decoding operation.

The format for the ACK signal is exactly the same as for the SSC, but there are some variations. For example, the First Call Code for the SSC becomes the Second Call Code for the corresponding ACK signal.

6. Speech codec

Each speech frame of 20 ms is encoded into 76 speech parameters and this in turn is processed as a block of 260 bits. It should be noted that these bits are not of equal value. However, there is no need to examine this point. The codec is similar to that for the GSM

(Groupe Special Mobile formed by CEPT in 1982 to write a Pan European Digital Cellular Telephone Standard).

The 34 significant bits, known as Class 1 bits, from the 260 bit block are expanded to 39 by the addition of five parity bits. A cyclic code with generator polynomial $(x^5 + x^2 + 1)$ produces the additional bits. The procedure is exactly the same as in Section 5 with the exception that the block size is 39. The generator polynomial should be a factor of $(x^{39} + 1)$ as per the mathematical requirements. Refer to Appendix 1 for the various factors and additional information. The check bits represent the lower powers of the new polynomial for x^4 down to x^0.

4

Location 43 Tail Bits (4)	Location 39 Data Bits (34)	Location 5 Check Bits (5)	LSB

920057 - 14
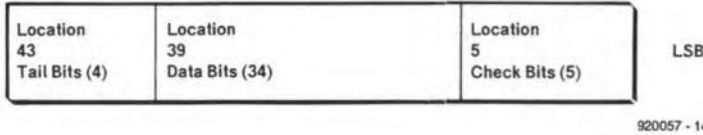
The 39 bit block is again expanded to 43 by four tail bits that are set to '0'. The positions are shown in Fig. 4. This new 43-bit block is re-ordered by a permutation operation as follows:

position $(n) \Rightarrow$ position $(17+n)$ for $n = 1$ to 5;
position $(n) \Rightarrow$ position $(n/2-2)$ for $n = 6, 8, 10, 12 \ldots 38$;
position $(n) \Rightarrow$ position $[42-(n-1)/2]$ for $n = 7, 9, 11 \ldots 39$.

The positions in the actual standard are numbered from 0 to 42 and 0 represents the least significant location. The data bits are given as d(0) to d(33) with d(33) corresponding to the term x^{38} of the polynomial. Refer to Appendix 3 for the complete table.

The 43-bit block is expanded to 86 with a convolutional code as follows:
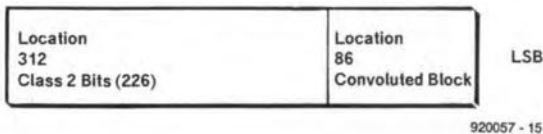
43-bit block $\quad (d_{43}\ d_{42}\ d_{41} \ldots d_3\ d_2\ d_1)$

86-bit block $\quad (b_{86}\ b_{85}\ b_{84} \ldots b_3\ b_2\ b_1)$
$b_{2n} = (d_n + d_{n-3} + d_{n-4})$ mod 2
$b_{2n+1} = (d_n + d_{n-1} + d_{n-3} + d_{n-4})$ mod 2

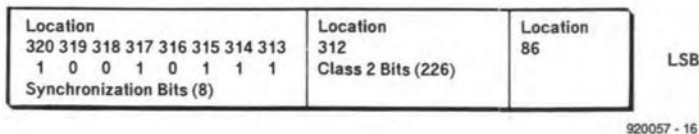for $n = 1$ to 43 and $d_m = 0$ for $m \le 0$.

5

Location 312 Class 2 Bits (226)	Location 86 Convoluted Block	LSB

920057 - 15

A new 312-bit block is formed by the 86 bits and the unused 226 bits, known as Class 2 bits, from the original block as in Fig. 5.

6

Location 320 319 318 317 316 315 314 313 1 0 0 1 0 1 1 1 Synchronization Bits (8)	Location 312 Class 2 Bits (226)	Location 86	LSB

920057 - 16

A new block of 320 bits is generated as in Fig. 6 by the addition of eight synchronization bits. The bits are re-ordered according to the equation

position $n \Rightarrow$ position $[16 (k \bmod 20) +$ INTEGER $/(20 + 1)]$

for $k = 0$ to 319. n refers to the position in the new block. The first bit ($n = 1$) is transmitted first.

7. Summary

The overall situation can be summarized in the following points.

(1) DSRR is more efficient in the use of spectrum since High Band and Low Band require a total of 4 MHz.

(2) DSRR provides a higher level of confidentiality and protection for the average user. In business radio, each user is licensed for a specific channel that must be shared with other users. A channel could be unintentionally or deliberately blocked by an unmodulated carried. Te Co-channel Rejection Test in MPT 1326 (which was not in the previous specification MPT 1301) does reduce, but not eliminate, this problem. In addition, users can obtain low-cost scanning equipment to monitor messages to and from competitors. However, in DSRR, a user does not actually know the traffic channel that is chosen automatically by a scanning algorithm.

(3) The DSRR Standard has no requirement for an encryption facility as in the GSM. The method of encryption for the GSM has not been made public, but is believed to be a stream cryptosystem. A pseudo-random binary sequence is generated by an arrangement of shift registers and applied to the sequence of data bits in an addition modulo 2 operation. For the DSRR, there is no reason that an encryption device, such as a scrambler, cannot be added, but this is not required to meet the standard.

(4) DSRR has scope for further development and expansion. In business radio, a reduction in the channel spacing to $6^1/_4$ kHz would provide more channels, but would not be considered an improvement.

(5) The encoding operation for data other than voice transmission is left to the manufacturer. The decoding operation for control signals, voice and data is also left to the manufacturers.

Appendix 1

The following factors were obtained using MATHEMATICA by Stephen Wolfram.

$(x^{88} + 1) = (x + 1)^8 (x^{10} + x^9 + x^8 + x^7 + x^6 + x^5 + x^4 + x^3 + x^2 + x + 1)^8$.

$(x^{16} + x^{14} + x^{12} + x^{11} + x^9 + x^8 + x^7 + x^4 + x + 1) =$
$= (x + 1)^2 (x^7 + x^6 + x^3 + x + 1) (x^7 + x^6 + x^5 + x^4 + x^3 + x^2 + 1)$.

$(x^{39} + 1) = (x + 1) (x^2 + x + 1) (x^{12} + x^{10} + x^9 + x^8 + x^7 + x^3 + x^2 + x + 1) (x^{12} + x^{11} + x^{10} + x^9 + x^5 + x^4 + x^3 + x^2 + 1) (x^{12} + x^{11} + x^{10} + x^9 + x^8 + x^7 + x^6 + x^5 + x^4 + x^3 + x^2 + x + 1)$.

$(x^5 + x^2 + 1)$ has no real factors.

The interim standard does not include an analysis of the generator polynomials and, consequently, the choice of the factors in each of the two cases is not known.

Appendix 2.

Consider a simple 3-bit word that has an additional bit for even parity. Any two code words differ in at least one position in order to have distinct code word. When the parity bit on the right in the table is included, the minimum variation becomes 2. To correct a single error per word, the minimum variation would have to be 3. This is know as the *Minimum Distance*. A typical example is the (7, 4) Hamming Code, which has four data and three check bits. A code of Minimum Distance 5 would be able to detect up to four errors per word or be capable of correcting up to two errors per word.

```
0 0 0 0
0 0 1 1
0 1 0 1
0 1 1 0
1 0 0 1
1 0 1 0
1 1 0 0
1 1 1 1
```

Appendix 3.

Permutation 1

Position	New position	Notation in DSRR Standard		
1	18	0	p(0)	17
2	19	1	p(1)	18
3	20	2	p(2)	19
4	21	3	p(3)	20
5	22	4	p(4)	21
6	1	5	d(0)	0
7	39	6	d(1)	38
8	2	7	d(2)	1
9	38	8	d(3)	37
10	3	9	d(4)	2
11	37	10	d(5)	36
12	4	11	d(6)	3
13	36	12	d(7)	35
14	5	13	d(8)	4
15	35	14	d(9)	34
16	6	15	d(10)	5
17	34	16	d(11)	33
18	7	17	d(12)	6
19	33	18	d(13)	32
20	8	19	d(14)	7
21	32	20	d(15)	31
22	9	21	d(16)	8
23	31	22	d(17)	30
24	10	23	d(18)	9
25	30	24	d(19)	29
26	11	25	d(20)	10
27	29	26	d(21)	28
28	12	27	d(22)	11
29	28	28	d(23)	27
30	13	29	d(24)	12
31	27	30	d(25)	26
32	14	31	d(26)	13
33	26	32	d(27)	25
34	15	33	d(28)	14
35	25	34	d(29)	24
36	16	35	d(30)	15
37	24	36	d(31)	23
38	17	37	d(32)	16
39	23	38	d(33)	22
40	40	39)		
41	41	40) tail bits set to '0'		
42	42	41)		
43	43	42)		

Appendix 4.

Permutation 2

Position	k	$16(k \bmod 20)$	Integer $(k/20)$	New position (n)
1	0	0	0	1
2	1	16	0	17
3	2	32	0	33
...	...	...	...	...
20	19	304	0	305
21	20	0	1	2
22	21	16	1	18
...	...	...	...	...
40	39	304	1	306
41	40	0	2	3
42	41	16	2	19
...	...	...	...	...
319	318	288	15	304
320	319	304	15	320

Appendix 5.

Radio frequency characteristics

Transmitter

Frequency error	±2.5 kHz (maximum)
Carrier power	4 watts (maximum)
Adjacent channel power	≥70 dB below carrier power or 0.2 µW (maximum)
Spurious emissions	0.25 µW (maximum) 2 nW (maximum) in standby mode
Intermodulation attenuation	≥40 dB for any component

Receiver

Sensitivity	6 dB µV e.m.f. (maximum) for a bit error rate of 10^{-2}
Co-channel rejection	−18 dB (minimum)
Adjacent channel selectivity	50 dB (minimum)
Intermodulation response	55 dB (minimum)
Spurious response rejection	60 dB (minimum)
Blocking	84 dB (minimum)
Spurious radiations	2 nW (maximum)

For the actual methods of measurement, the reader should consult the standard.

CORK
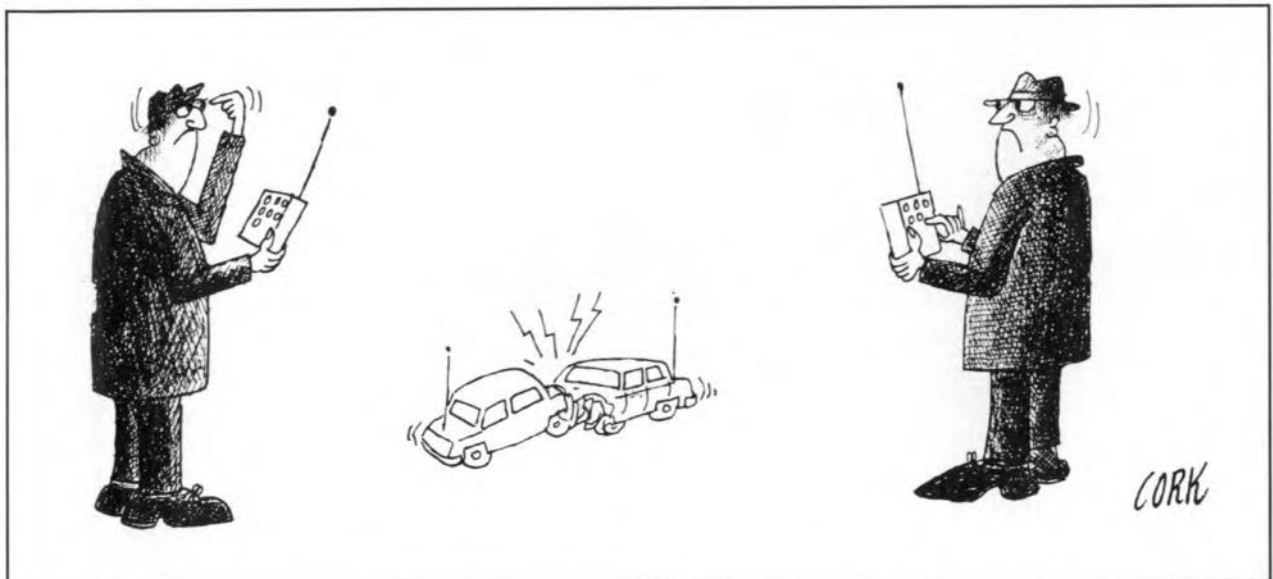
FM TUNER

PART 3: SYNTHESIZER (CIRCUIT DESCRIPTION) AND POWER SUPPLY (CONSTRUCTION)

The greater part of this month's instalment is devoted to the operation of the microprocessor-controlled synthesizer used to tune the RF board, and to program and memorize station presets.

When it comes to designing a tuning system for a high-quality FM receiver, we are faced with the choice between two evils: synthesizer tuning or variable capacitor tuning. The first is for ever and a day tied up with the problem of digital noise, the second with the problem of component availability, complex adjustment and repeatability. Bear in mind that a single tuning capacitor will not do here; what we require is a type with, say, six synchronized sections. Moreover, implementing a station preset facility on a tuner with a multi-section synchronized tuning capacitor is something that (we fear) is best left to instrument engineers. Also, most of you will not like the noise such a preset produces when a station is selected: it rather throws up memories of radios and TV sets used in the sixties and early seventies.

So, a synthesizer it will be. Although this does require special integrated circuits, these are by no means as costly and difficult to obtain as a six-way synchronized tuning capacitor. Since the tuner module used on the RF board is tuned by variable capacitance diodes (varicaps), there are no capacitors or inductors to adjust. What's more, the synthesizer concept proposed here can work without any adjustment whatsoever. As to tuning noise and phase jitter, this will not pose limitations in modern synthesizer concepts, by virtue of the high working frequency of today's synthesizer ICs, and the use of high-performance phase detectors.

A possibly more serious problem, particularly in home-made receivers, is formed by the noise generated by the digital components in a synthesizer. Given the fact that the digital noise level is determined to a large extent by the number and length of printed-circuit board tracks, the advantages of a microcontroller (with on-chip ROM, RAM and interfaces) over a system with external (E)PROM and peripheral ICs are fairly obvious. The only problem with mask-programmed microcontrollers is that they are produced in large quantities only. Hence, an alternative is used here in the form of a 80C32 microcontroller combined with an external EPROM that contains the control software. This has two advantages: first, the 80C32 is a low-power, inexpensive, and easily programmable device (witness our assembler course). Second, the external EPROM allows you to make changes to the control software should you so desire.

This leaves us with the problem of digital noise generated by the synthesizer. Unfortunately, such noise is hard to suppress completely, even when all the rules of RF screening are strictly observed. The solution to the problem is fairly drastic: switch off the source of the interference, i.e., the microcontroller, when it is not needed. This can be done with impunity because the microcontroller is active for very short periods as it changes or stores frequencies. During normal reception, the microcontroller is switched to the 'sleep' state, which also disables its clock oscillator.

Functions

Although a single-chip solution is not feasible because of the above aspects, the circuit of the synthesizer (Fig. 11) is fairly simple. The main components of the synthesizer are a control loop amplifier (opamp IC412, a type TL082), a prescaler (IC410, a Type SP8795), and a synthesizer proper (IC409, a Type NJ8821). All other ICs in the circuit form part
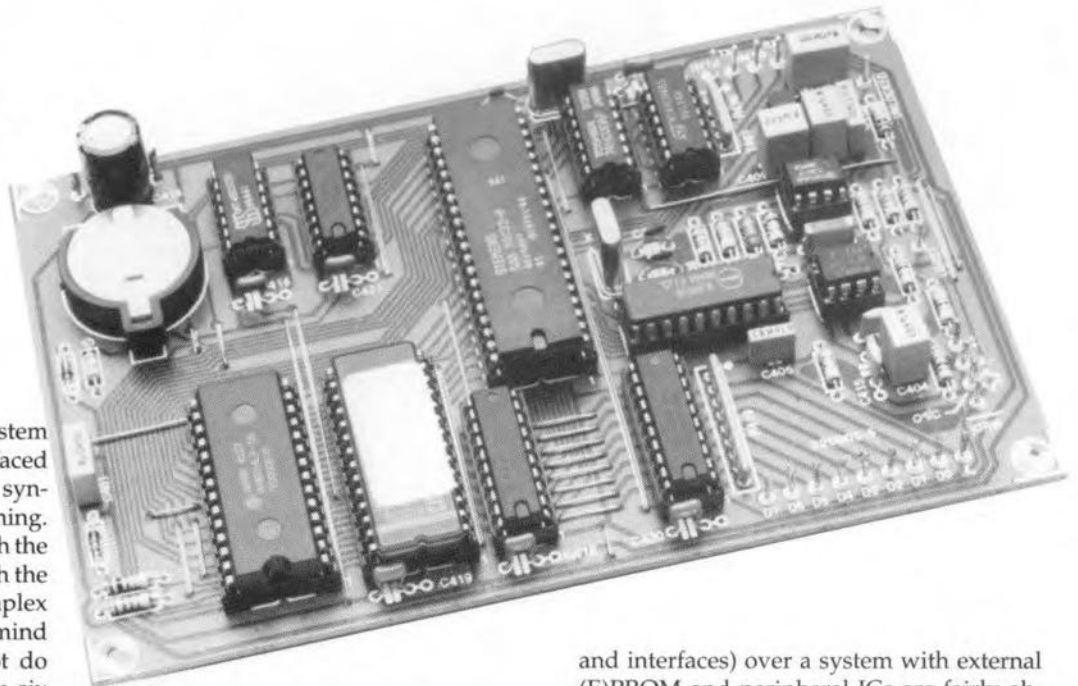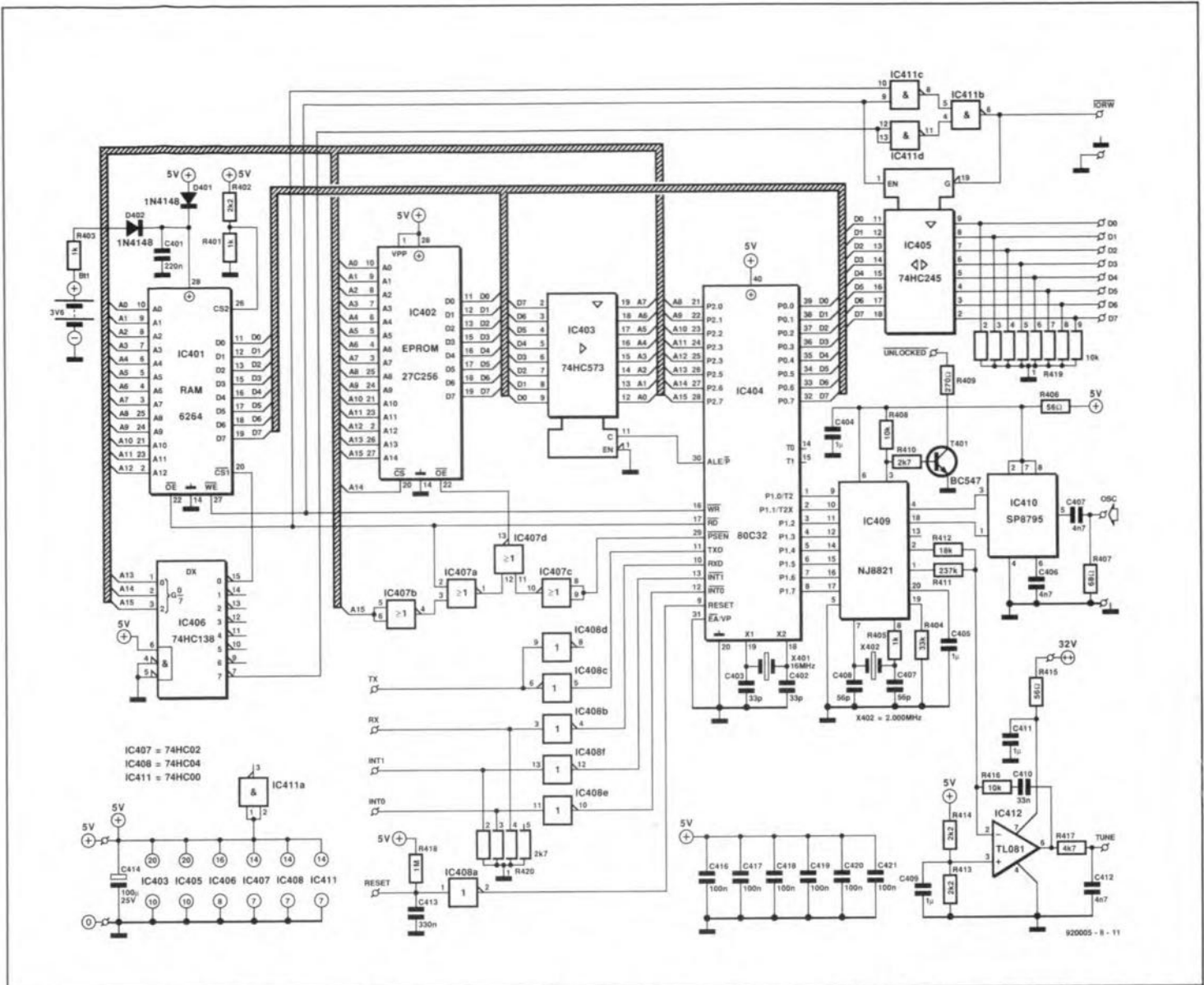
Fig. 11.   Circuit diagram of the synthesizer board. The 'brains' of the receiver are formed by a 80C32-based microcontroller circuit.

of the microcontroller system, and serve to control the synthesizer, which offers a microcontroller interface via its pins 9 to 17. These pins convey the tuning frequency from the microcontroller to the synthesizer. This information is presented in binary form as eight datawords of four bits each. The function of the microcontroller is to gather all the data required to build these datawords, and also to store and display them.

One source for the tuning data gathered by the microcontroller is a 15-key keypad, which will be described in next month's instalment. This keyboard is located on the single-sided 'controls' PCB, and is constantly scanned for activity. It has 10 numeric keys for direct entry of a frequency or a station preset number, as well as ENTER, STORE and EXECUTE keys to enter, store and call up station frequencies. The other two keys, UP and DOWN, allow the receiver to be tuned up or down in 50-kHz steps.

The station frequency and preset number are indicated on a large, bright, 7-digit, LED display that is also accommodated on the 'controls' board.

A single bisectional 8-bit port is used to scan the keys and drive the displays. This

function requires an output current of 5 mA to be supplied at the logic 'high' as well as the logic 'low' level. Figure 11 shows that this port is formed by a 74HC245 (IC405). The address decoder of the display is actuated by the $\overline{\text{IORW}}$ signal. The display driving function has priority over the keyboard scanning function. Hence, if a key is pressed while the display is being updated, the 1-kΩ resistors in the keyboard matrix function as pull-up resistors only.

Enter the 80C32 SBC

The microcontroller system used here is basically a stripped-down version of the 80C32 single-board computer (Ref. 1) used for writing and testing the control software for the present FM tuner. The 80C32 is the ROMless, CMOS, version of the 8052. One reason for using the 80C32 here is that it can be switched to a 'sleep' mode, which is necessary to prevent digital noise in the RF sections of the receiver. The external EPROM, IC402, is a 32-KByte type divided into two 16-KByte memory areas starting at 0000H and 8000H.

The static CMOS RAM, IC401, is a Type 6264LP-2. When the receiver is switched off,

the RAM is powered by a lithium battery, which ensures that stored frequencies remain intact for at least 10 years. The software allows you to enter up to 99 presets, which is more than the maximum number of stations that can be contained by the entire FM band, even if a 250-kHz raster were used.

To make sure that the RAM is timely disabled when the supply voltage drops, RAM input CS2 (pin 26) is held at a slightly lower voltage with the aid of resistors R401 and R402. This prevents the microcontroller writing random data into the RAM when the receiver is switched off.

IC406 decodes the address ranges for the RAM, and address 0E00H for the I/O port, IC405. The NOR gates contained in IC407 form the address decoder for the EPROM. Circuit IC403 demultiplexes the lower 8 address bits and the datalines.

The inverters contained in IC408 allow a serial interface (RS232) to be connected, if this can work with a voltage swing of 5 V. The interface may be modified as follows when it is to be connected to a device that works with ±12 V swings: fit a 3.3-kΩ resistor in series with the Rx line. Together with the 2.7-kΩ resistor in array R420, this forms a
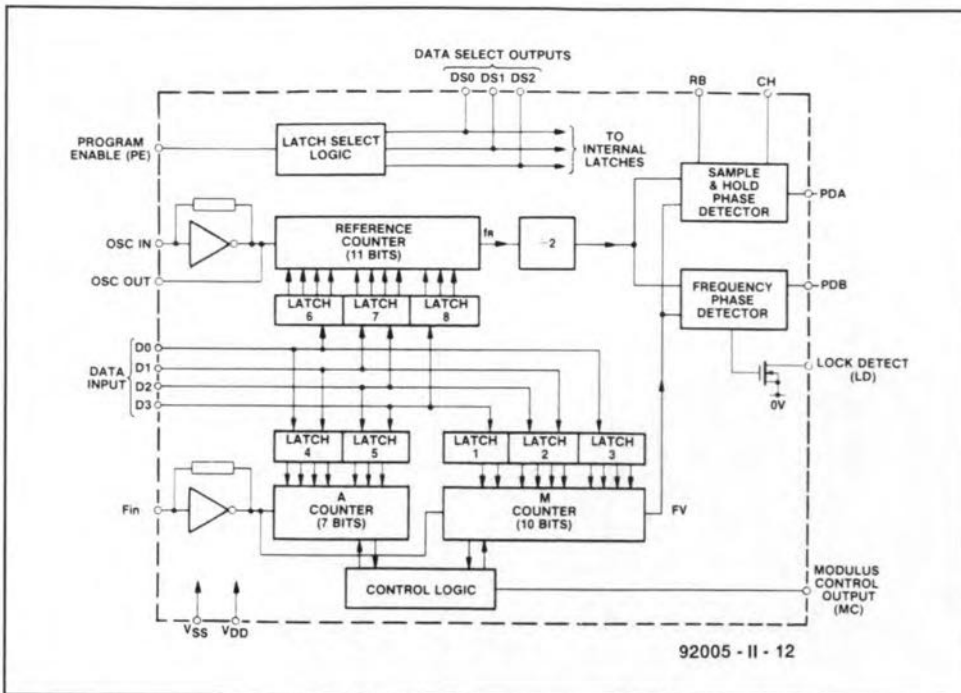
Fig. 12. Internal architecture of the NJ8821 synthesizer IC (courtesy Plessey Semiconductors).

Fig. 13. NJ8821 pinning (courtesy Plessey Semiconductors).

voltage divider that changes +12 V to +5 V. To convert the negative (–12 V) level at the Rx input into (approximately) 0 V, connect a diode Type 1N4148 between the Rx line and ground. The cathode goes to Rx, the anode to ground.

The two interrupt inputs, INT0 and INT1, respond to logic 'high' signals, provided, of course, that interrupts are enabled (in software).

The processor is reset by applying a logic 'low' level to the RESET input of the synthesizer board. R-C network R418-C413 supplies the reset pulse at power-on.

The control software for the synthesizer is all machine code, and fast enough to scan the keyboard as a part of the normal program. Hence, an interrupt request is not required when a key is pressed.

The synthesizer

The heart of the synthesizer is formed by the NJ8821, a CMOS IC from Plessey. This IC is marked by a high-performance, high-frequency, phase detector, and low current consumption (3.5 mA typ.). In a PLL circuit, this IC allows excellent phase stability and low noise to be achieved.

Each PLL-based synthesizer consists of four basic components, whose function and materialization are discussed below.

Voltage-controlled oscillator (VCO)

This is contained in the FD12 tuner module on the RF board. Its output frequency is supplied to the prescaler in the synthesizer via the UOSC socket on the module.

Reference oscillator

As shown in Fig. 2, this is contained in the NJ8821. The oscillator works with an external 2-MHz quartz crystal, which is connected to the OSC IN and OSC OUT pins of the IC. The crystal operates in parallel-resonance mode, and is 'flanked' by the usual parallel capacitors to ground.
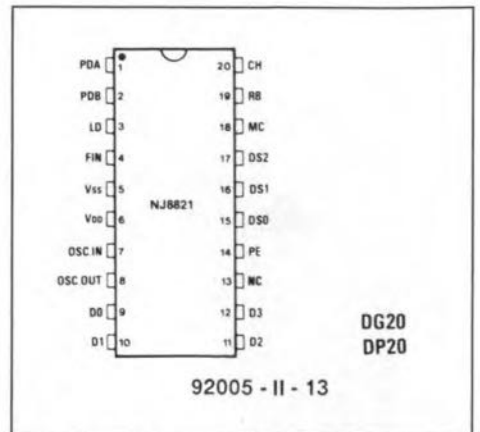
Reference counter and prescaler

The reference frequency, f_R, is derived from the reference oscillator frequency by a programmable 11-bit counter (divider), whose divisor can be set between 6 and 4,094 in steps of 2. A binary (÷2) scaler is connected to the output of the reference counter to achieve an output signal with a 50% mark/space ratio. This means that the total divisor is two times the programmed divisor.

The oscillator signal, which is to be compared to the reference signal, is supplied by the VCO in the FD12 tuner, and fed to the synthesizer input, FIN (pin 4), via a Plessey Type SP8795 prescaler. The prescaler output is divided by two programmable dividers in the NJ8821: a 7-bit divider, 'A', and a 10-bit divider, 'M'. Both are connected to the prescaler via the 'MC' signal at pin 18. The 'MC' signal is low at the start of a counter cycle, and remains low until counter 'A' has completed one cycle. Next, MC goes high, and remains high until counter 'M' has completed its cycle. Next, both counters are reset. The resulting divide ratio is

$$M \times N + A$$

where N and $N + 1$ are the divisors of the prescaler controlled by the 'MC' signal.

The divisors that can be programmed are 0 to 127 for counter 'A', and 3 to 1,023 for counter 'M'. For this so-called modulo-2 counting principle to operate correctly, divisor M must always be greater than divisor A.

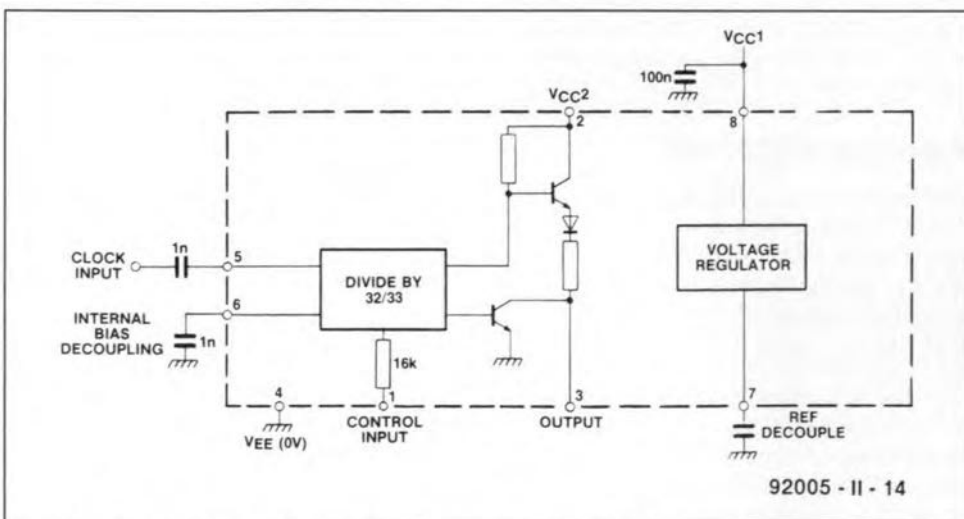Port 1 of the 80C32 is used to program the

Fig. 14. Block diagram of the SP8795 prescaler (courtesy Plessey Semiconductors). The control input of the IC allows the divisor to be switched between 32 and 33.
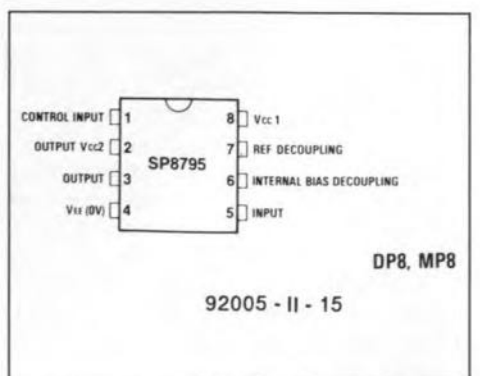

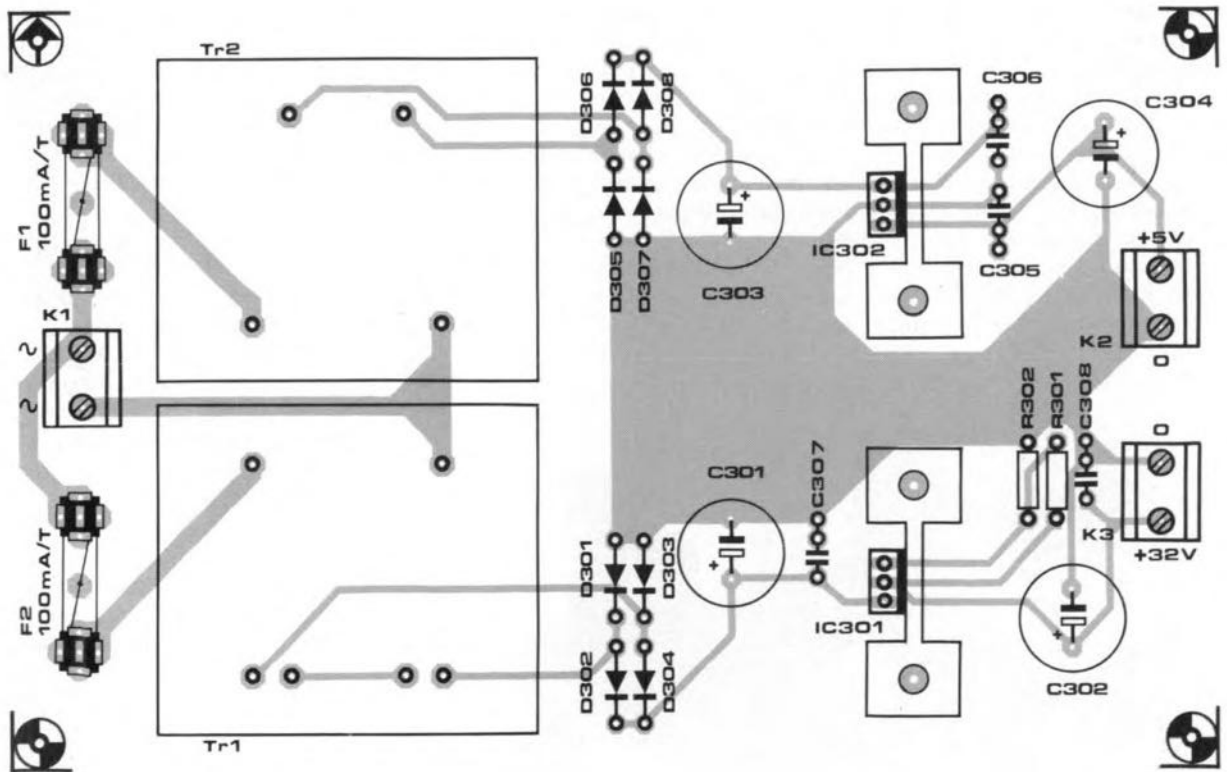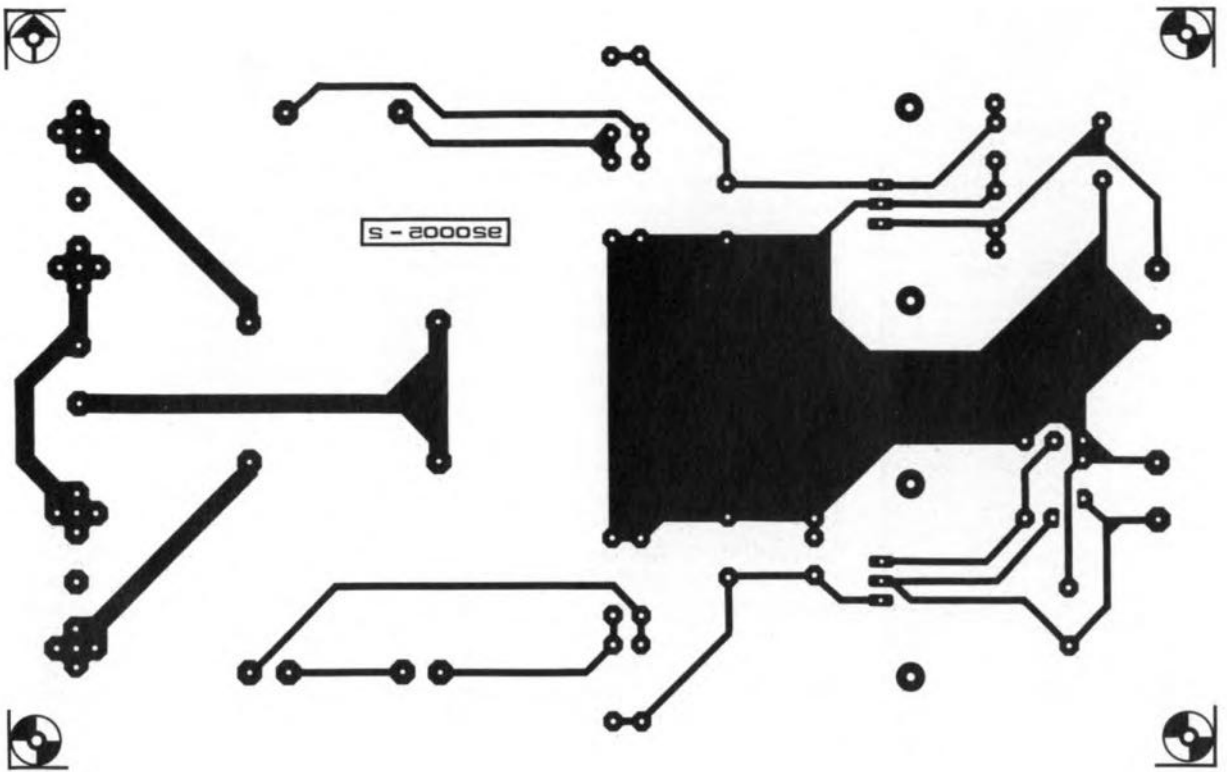Fig. 15. SP8795 pinning (courtesy Plessey Semiconductors).

Fig. 16.   Track layout (mirror image) and component overlay of the PCB for the power supply unit.

COMPONENTS LIST

Resistors:

1	150kΩ 1%	R301
1	3kΩ57 1%	R302

Capacitors:

2	470µF 63V radial	C301;C302
2	1000µF 16V radial	C303;C304
3	220nF	C305;C307;C308

Semiconductors:

8	1N4001	D301-D308
1	LM317	IC301
1	7805	IC302

Miscellaneous:

1	Mains transformer 2×7.5V @ 18VA, e.g., Block VR7,5/2/18	Tr1
1	Mains transformer 1×7.5V @ 8VA, e.g., Block VR7,5/1/8	Tr2
3	3-way PCB terminal block	K1;K2;K3
2	Fuse 100mA	F1;F2
2	Fuseholder for PCB mounting, with plastic cap	
2	Heat-sink SK104 (Fischer)	
1	Printed circuit board	920005-2

counters. As shown in Fig. 12, a 4-bit dataword is applied to inputs D0 to D3 (pins 9 to 12 of the NJ8821). A dataword is copied into a counter latch when a logic 'high' strobe pulse is applied to the PE (program enable) input. The three data select inputs DS0, DS1 and DS2 are used to select the latch to which the dataword is written (DS0, DS1 and DS2 are erroneously marked as outputs in the block diagram, Fig. 12, which is reproduced here from an original supplied by Plessey).

To program the synthesizer, eight latches must be loaded successively with a 4-bit dataword. The transfer of all data from a latch to the associated counter occurs simultaneously with the loading of latch 1. This means that latch 1 is addressed as the last one when a different counter state (= tuning frequency) is required.

The counters are always programmed

such that the divider output frequency, f_v, equals the reference frequency, $f_R/2$ (behind the binary scaler), given the desired oscillator frequency after prescaling at pin FIN.

Phase comparator

The $f_R/2$ and f_v signals are compared in a phase comparator, which is actually a two-stage phase detector. The first stage is a digital phase/frequency detector, which enables the PLL to lock fast by supplying a 'coarse' error signal that can signal one of three conditions: output PDB supplies positive-going pulses when the tuner oscillator frequency is too high ($f_v > f_R/2$); negative-going pulses when the tuner oscillator frequency is too low ($f_v < f_R/2$); or no signal (PDB switched to high impedance) when the two frequencies are equal or sufficiently close. In the latter case, the MOSFET at the LOCK output (pin 3) starts to conduct. Consequently, transistor T1 conducts also, and causes a LED to light, indicating that the PLL is locked. The inverted 'lock' signal may also be used to mute the receiver when the PLL is out of lock.

As soon as the PDB output of the digital phase comparator is at high impedance, an analogue sample-and-hold starts to work on the fine tuning. Its output signal, PDA (pin 1) is at about half the supply voltage when the PLL is locked. Starting at that level, the voltage rises when the phase of $f_R/2$ lags that of f_v, and drops when f_v lags $f_R/2$. The linear range of the output voltage is determined by an external resistor, R404, connected to the RB terminal (pin 19). The RB output controls the amplification of the sample-and-hold comparator. The value of R404 is determined by the reference frequency used. The 'hold' capacitor is connected between the 'CH' terminal (pin 20) and ground.

The output voltages of the two phase comparators are added by two resistors at the inverting input of the control loop amplifier, opamp IC412. The opamp is wired in a so-called pi-configuration, and its non-inverting input is held at a well-decoupled level of +2.5 V, i.e., half the supply voltage. The speed of the control loop and the suppression of high-frequency components in

the comparator output signals are determined by the time constant formed by the feedback circuit, and a passive low-pass filter, R417-C412, at the output of the opamp. The opamp output signal is the synthesizer-generated tuning voltage for the FD12 tuner module on the RF board.

Prescaler

It will be recalled that the FD12 tuner module is basically a superheterodyne receiver, in which the local oscillator (= VCO) frequency is 10.7 MHz higher than the receive frequency. This means that the VCO frequency range must be 98.7 MHz to 118.7 MHz to cover the entire FM band (88 MHz to 108 MHz). However, the synthesizer IC can handle frequencies up to about 15 MHz only, whence the need for a prescaler that reduces the VCO frequency to under 10 MHz.

Figures 14 and 15 show the block diagram and the pinning respectively of the SP8795 prescaler, whose input frequency range extends from 20 MHz to about 225 MHz. This prescaler is marked by high sensitivity (200 mV$_{pp}$) and low current consumption (approx. 5 mA). An on-board voltage regulator enables the IC to be used with supply voltages between 6.5 V and 9.5 V. Alternatively, 5-V operation is possible by not using the on-board regulator. This option is used in the present circuit: pins 7 and 8 are connected direct to the supply voltage (pin 2).

A special feature of the SP8795 when used in combination with the NJ8821 is the modulo-2 divider, which can switch between divisors N and $N+1$, where N equals 32, and is selected by a logic 'high' level at pin 1. When a 'low' level is applied, the IC divides by 33. Here, this means that the frequency range of the synthesizer input signal is about 3 MHz to 3.7 MHz.

Power supply board

The power supply circuit discussed last month (Fig. 10) is constructed on the printed circuit board shown in Fig. 16. The fuses on this board are inserted into the mains lines, which requires plastic caps to be fitted on the holders. A double-pole mains on/off switch is connected between the mains inputs of the PSU board and the appliance socket on the rear panel of the tuner case.
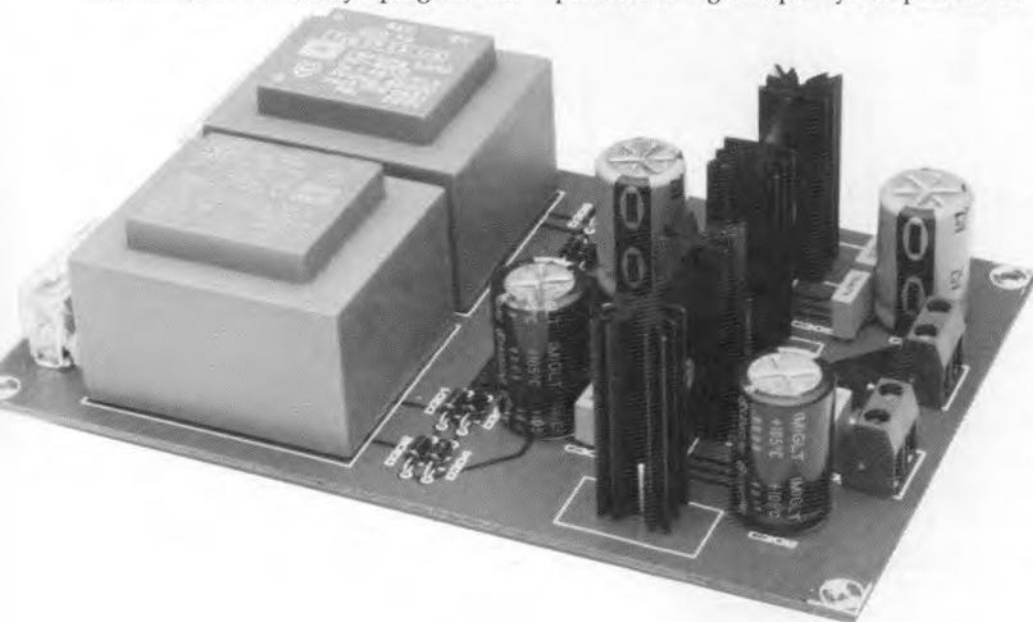
To prevent confusion, note again that the +32-V output voltage at connector K3 of the PSU unit powers the entire RF board. This means that it is not required to connect separate wires from the PSU to the '+' and 'UABST' (tuning voltage) pins of the RF board. Instead, interconnect these two pins at the RF board, and run a single wire from K3 on the PSU board to the '+' pin on the RF board. The 5-V output of the PSU board is used to power the synthesizer circuit. ❑

Next month we will tackle the construction of the synthesizer, and discuss the operation of the 'controls' board.
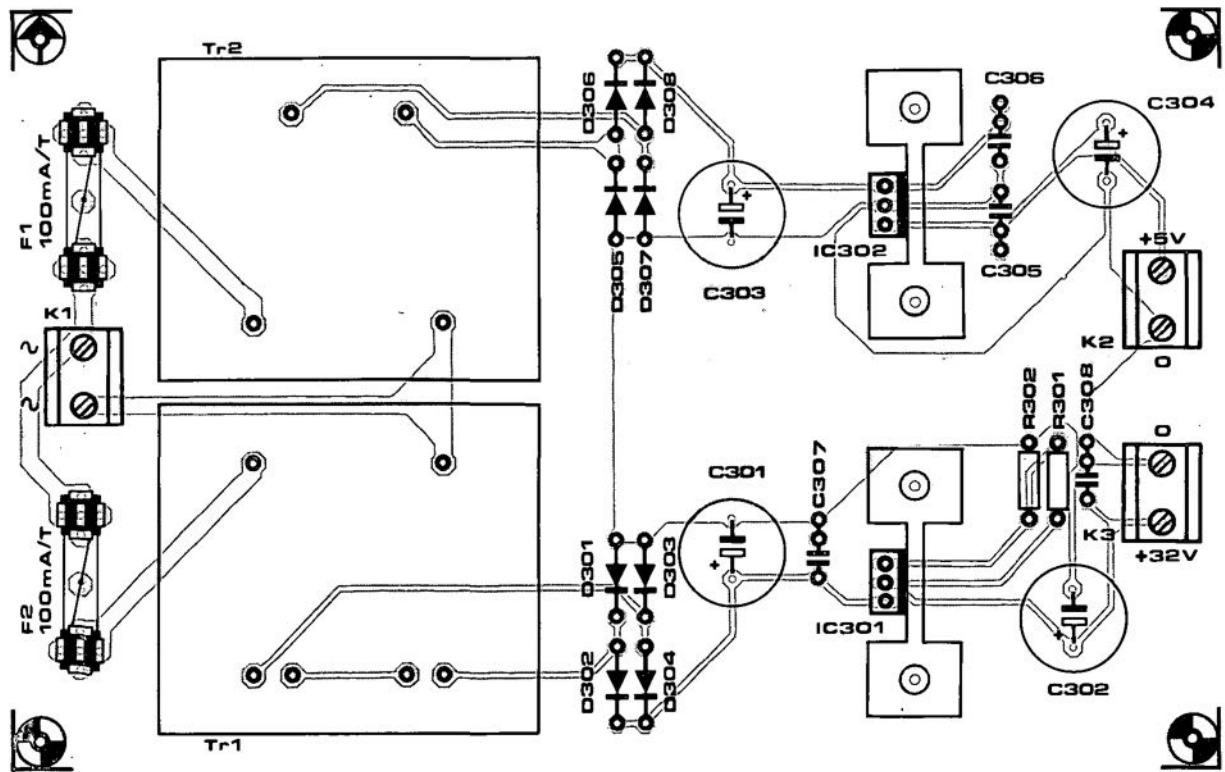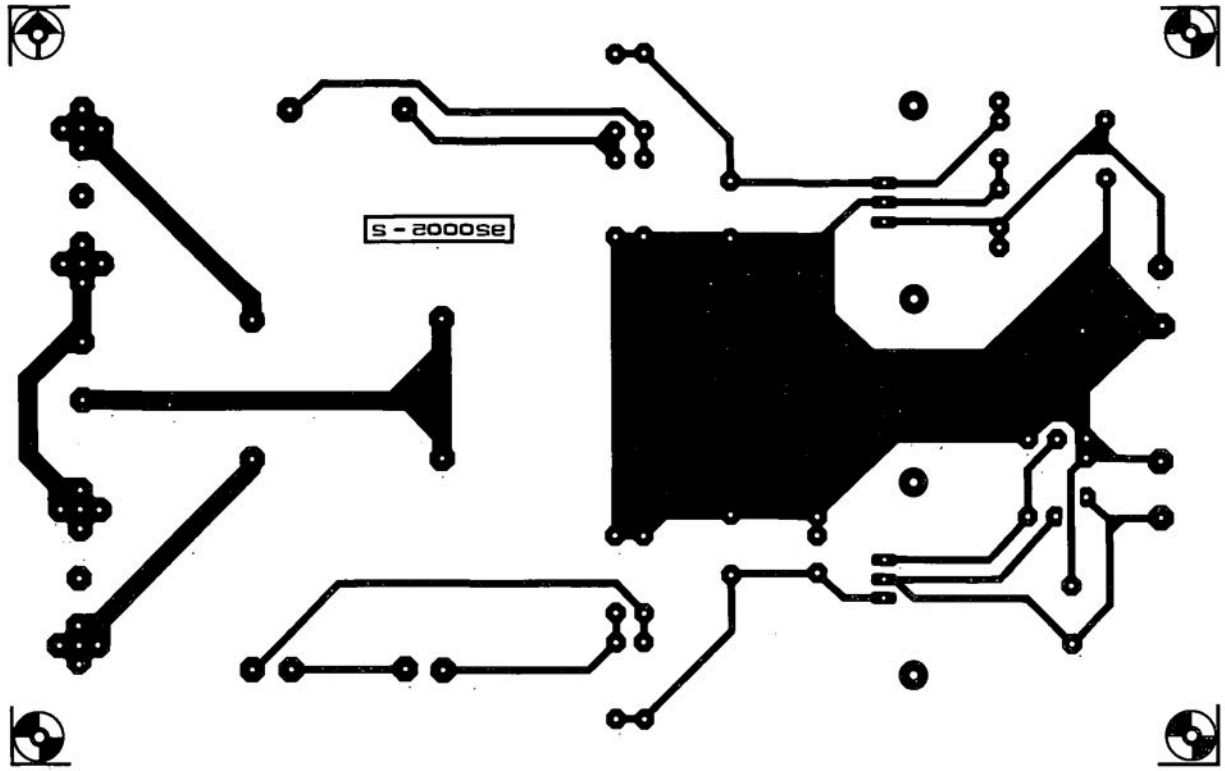
Fig. 16.   Track layout (mirror image) and component overlay of the PCB for the power supply unit.

Mains (power line) voltages are not listed in the articles. It is assumed that our readers know what voltage is standard in their part of the world.

Readers in countries that use 60 Hz supplies, should note that our circuits are usually designed for 50 Hz. This will not normally cause problems, although if the mains frequency is used for synchronization, some modification may be required.

The international letter symbol 'U' is used for voltage instead of the ambiguous 'V'. The letter V is reserved for 'volts'.

CORRECTIONS

Plant warmer (June 1992)

Resistor R_c was omitted from Fig. 2. The correct diagram is shown below.

920050 - 12
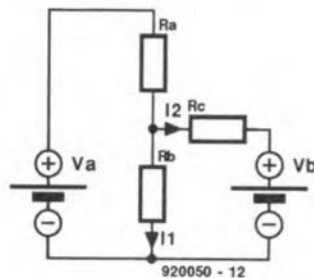
Inductance-capacitance meter (March 1992)

The value of R_{16} and R_{17} should be 39 Ω, not 30 Ω as shown in the parts list.

8751 Emulator (March 1992)

The features list in the first column on page 53 should read:
- download, modify, and upload 8751 programs without having to erase and program an 8751.
- put breakpoints in programs.
- display register and memory contents.
- ...
  etc.

FM tuner – Part 3 (May 1992)

In the PSU parts list on page 54, R_{301} should be 150 Ω, 1%, not 150 kΩ, 1%.

Video enhancer (July 1992)

Preset P_2 is best adjusted for a signal level of 2 V_{pp} at the collector of T_2. Output transistor T_3 may run fairly hot: this is normal.

The third paragraph of the text on page 73 should read: The frequency characteristic of the signal at the base of T_3 is shaped by P_1, R_6 and C_8, and is, therefore, to a certain extent under the control of the user (with P_1).

Mark 2 QTC 80/40 loop antenna (July 1992)

The frequency '3800 kHz' mentioned twice under **2. 40-metre band** (page 90) should have read '7300 kHz'.

Audible fluid level indicator (July 1992)

Owing to a printing error, the diagram in this article is incorrect. The right diagram is shown below.

914110 - 11
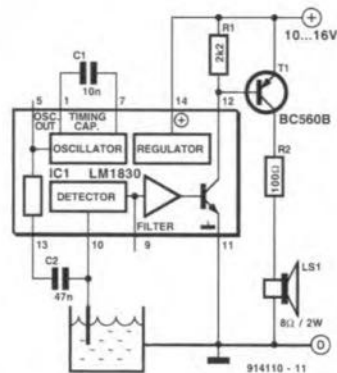
GAL PROGRAMMER
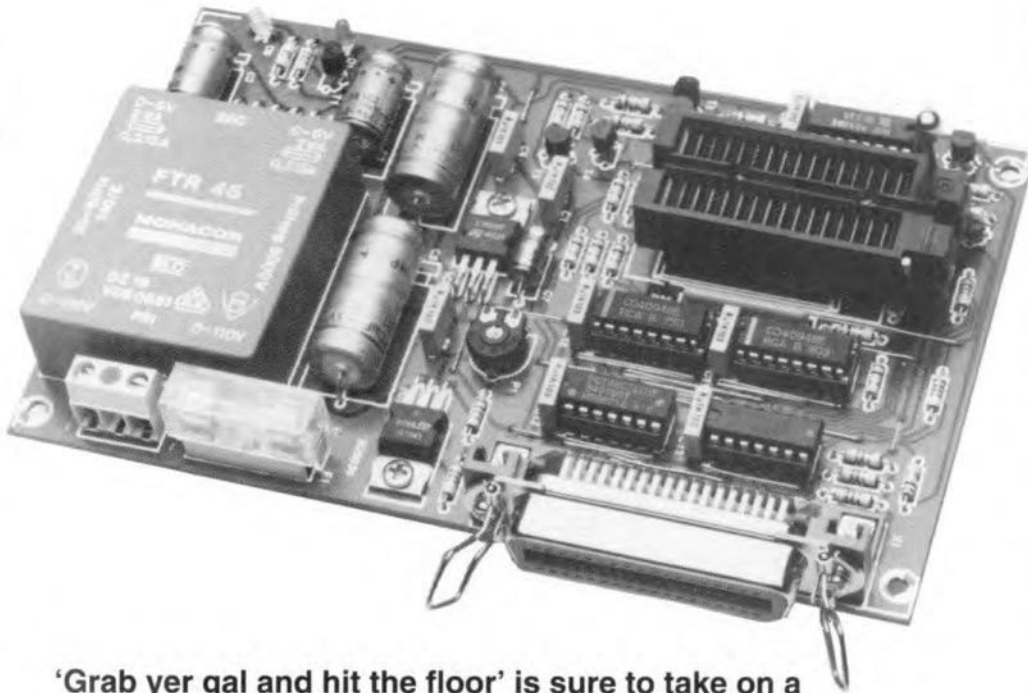
'Grab yer gal and hit the floor' is sure to take on a completely new meaning before long. Now while gals in the more traditional sense of the word are often pretty difficult to control, let alone to be forced into 'tailor-made' behaviour (which adds considerably to their charm), the electronic versions we are dealing with here (identified by three capital letters, GAL) are admittedly less exciting, but much more easy-going. The GAL programmer described in this article offers everything needed to burn complex logic functions into today's most popular GALs. The software used to control the programmer is menu-driven, and can be run on all IBM PCs and compatibles.

MAIN SPECIFICATIONS

Software:
• **Programs 16V8, 20V8, 16V8A, 20V8A**
• **Protection against wrong GAL selection**
• **Simple to control**
• **Menu driven**
• **For XT/AT and compatible PCs**
• **Reads and writes normalized JEDEC-Files**
• **In colour**
• **Integrated line editor**
• **Hard copy of cell matrix on printer**
• **Configuration file to adapt software to personal needs**
• **Opal Junior ™ EQN-to-JEDEC converter and GAL programming utilities supplied free of charge with control software ESS1701**

Hardware:
• **Eurocard PCB 160 ×100 mm**
• **Communication via 5 lines on Centronics port**
• **Internal power supply**
• **Only one ZIF socket required**
• **Based on standard components only**

GAL:
• **Electrically erasable and reprogrammable logic**
• **Maximum flexibility for complex logic design**
• **Read protection**
• **Electronic signature**
• **Speed: 10ns maximum propagation delay (A-Types)**
• **Inexpensive**

Design by M. Nosswitz

FOLLOWING last month's introductory article on features and functions of GALs (general array logic) we now take more a practical look at things with the description of a powerful, low-cost, GAL programmer for use with PCs.

The advantages of GALs over discrete logic circuits are significant. At reasonable cost, you obtain a piece of programmable logic that can be erased, too! Apart from their remarkable flexibility, GALs offer the possibility to 'stamp' them electronically with an identification code, as well as to protect them from being read out (and copied). Further, GALs are pretty fast, A-versions achieving propagation delays of the order of 10 ns only.

The operation of the programmer described here is strictly controlled via the Centronics port of an MS-DOS compatible computer running the software developed for the programmer. The control software was developed with the aid of Turbo Pascal 6.0, and is capable of programming GAL Types 16V8, 20V8, 16V8A and 20V8A. The control software is available ready-programmed, and comes on a diskette supplied through the Readers Services.

The programmer and the computer communicate via the Centronics port, using a serial format to exchange data and commands. Remarkably, only five lines are required to handle all functions. At the programmer side, a shift register is used to convert the serial data into parallel. Despite this converter, the total circuit of the programmer is not too complex.

The hardware

Just like almost any other electrically programmable component, a GAL needs a programming voltage that is higher than the normal supply voltage. As shown in the circuit diagram (Fig. 1), this has been taken into account in the design of the power supply of the programmer, which caters for the normal board supply voltage of 5 V as well for an auxiliary voltage of 16.5 V. Preset P1 serves to adjust the latter voltage accurately. Fortu-
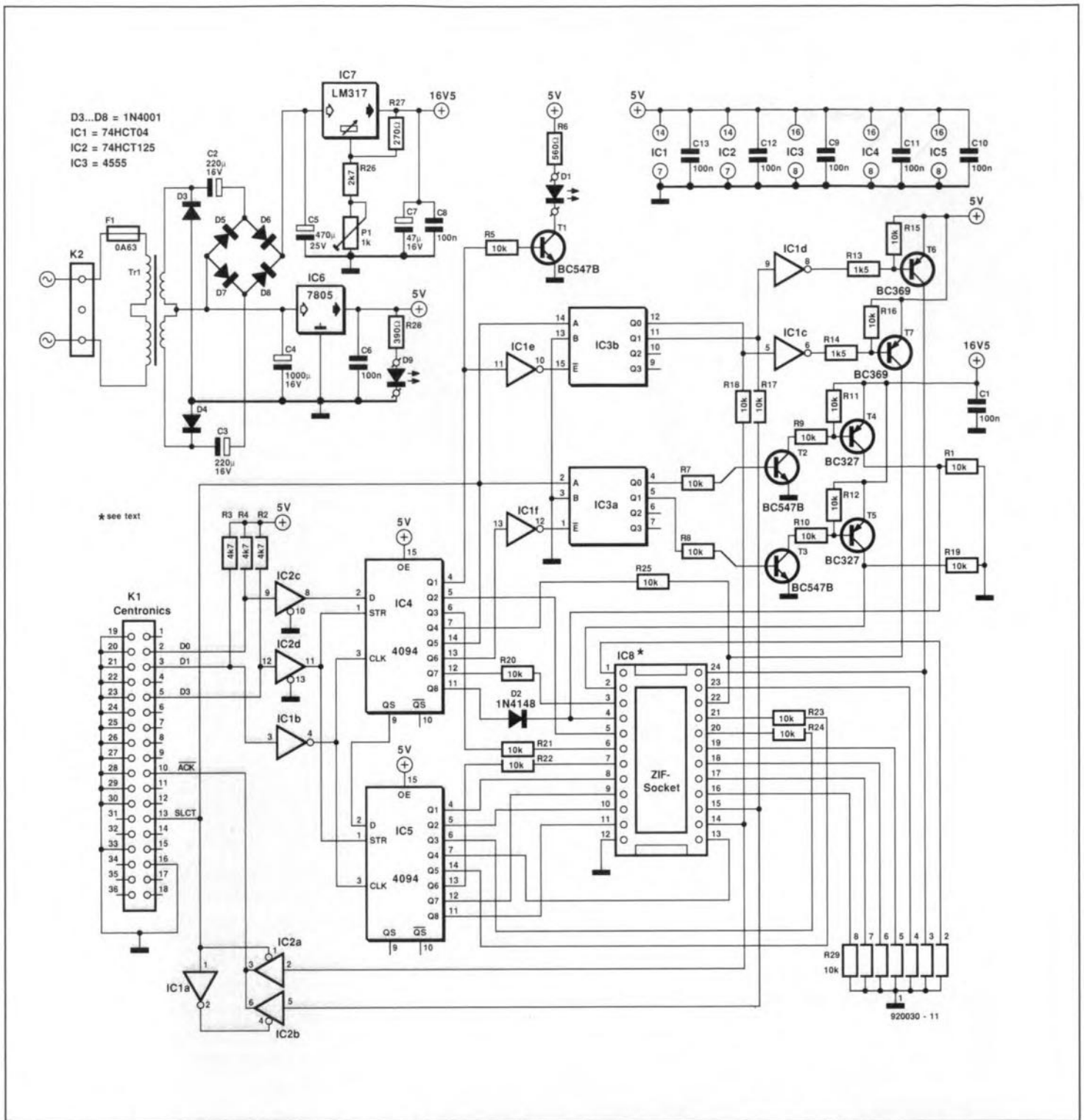
Fig. 1. Circuit diagram of the GAL programmer. The programmer communicates with the computer via the Centronics port using a serial protocol.

nately, the current consumption of the programmer is low, so that a small (4-VA) mains transformer may be used, while the two regulators can make do without heat-sinks.

The control signals needed for shift registers IC4 and IC5 are supplied via three of the eight data lines on the Centronics interface. Dataline D0 carries the serial data, while D1 and D3 supply the shift register clock and strobe signal respectively. Pull-up resistors R2, R3 and R4 ensure correct signal levels during the data exchange. The two shift registers are connected in series via the serial output QS (pin 9 of IC4) and the data input (pin 2 of IC5). The three-state outputs of IC4 and IC5 are always active because the OE

(output enable) inputs are tied to +5 V. The 16 databits at the parallel outputs Q0-Q8 of IC4 and IC5 determine the operation of the rest of the circuit.

One half of a dual 2-of-4 decoder, IC3b, switches the supply voltage via transistors T6 and T7. The other half, IC3a, controls the presence of the programming voltage at the respective pins of the GAL socket, via transistor pairs T2-T4 and T3-T5. This is possible only if the decoder outputs have been enabled beforehand by a low level at the EN-ABLE (E) inputs.

Resistors R20-R25 reduce the short-circuit currents at the register and GAL outputs to safe values when these are switched to the

read mode. R1, R19 and R29 are the pull-down resistors needed for the programming mode. Diode D2 protects output Q8 of IC4 against the programming voltage.

The computer can read the GAL data matrix via Centronics handshaking line ACK. This requires a selection operation via the select (SLCT) signal. By virtue of SLCT, the software is capable of checking if the programmer hardware is connected, and if a GAL is fitted. If desired, this function may be switched off by modifying the file GAL.CFG (Fig. 6). If hardware checking is not required, the SLCT line may be omitted.

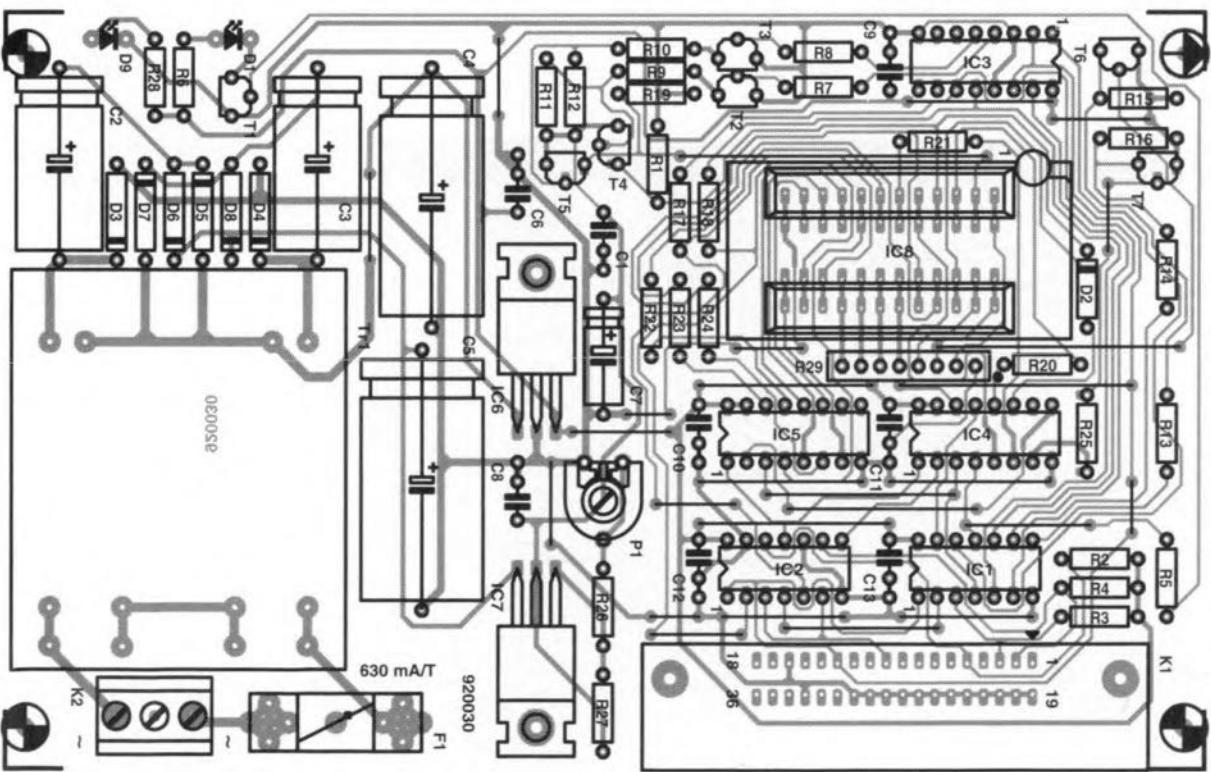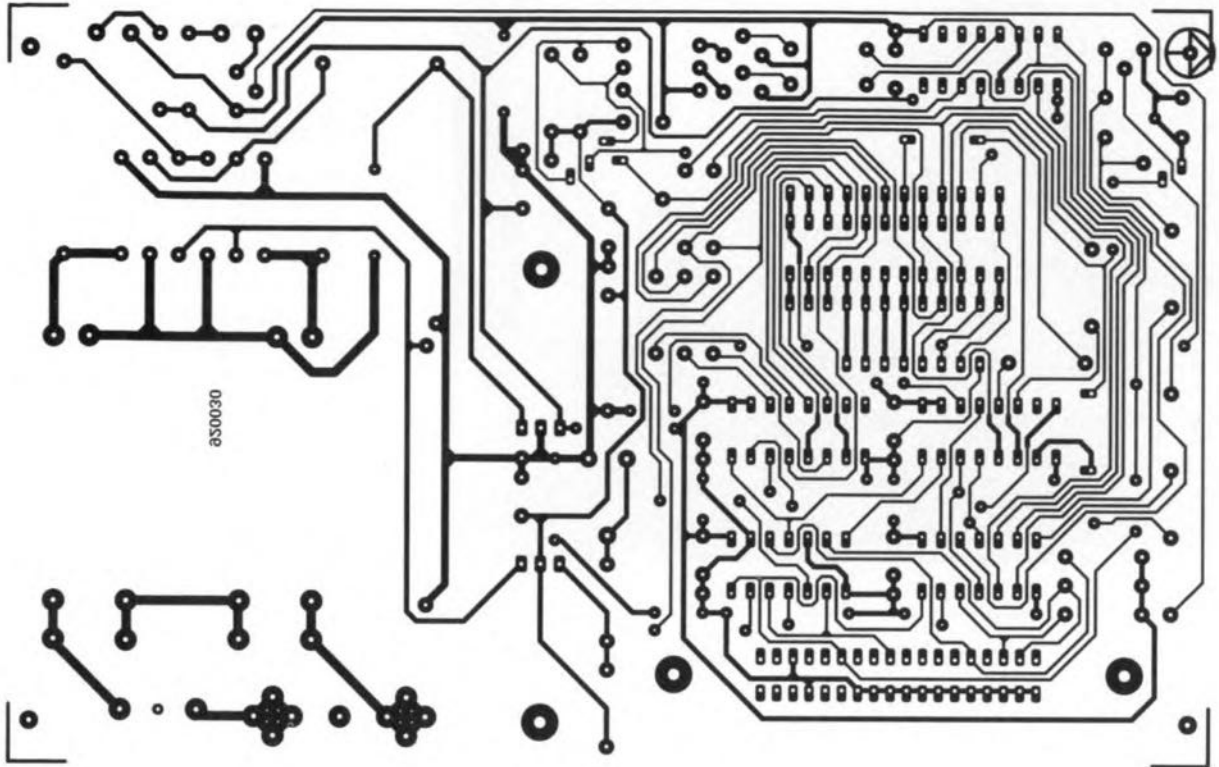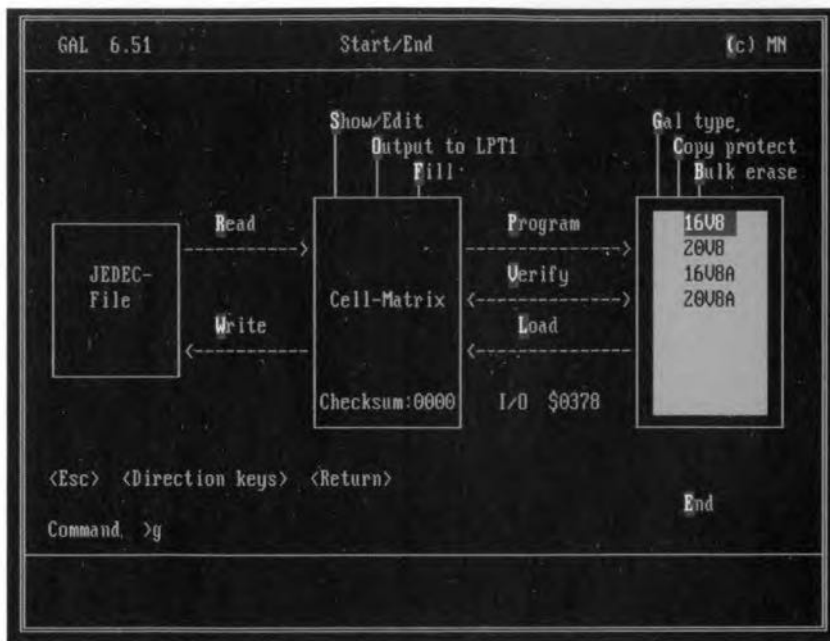The GAL is fitted into a zero-insertion force (ZIF) socket. Finally, LED D9 lights

Fig. 2.   Track layout (mirror image) and component mounting plan of the single-sided PCB for the GAL programmer.

when the programmer is active, and D1 when the GAL receives its supply voltage. It is recommended to insert the GAL only when D1 is out.

Software development for GALs

To begin with, use any ASCII-compatible word processor to produce an equations file that describes the desired function of the GAL. 'GALDEMO.EQN' (Fig. 3) contained on the disk supplied for this project is such a file, and may serve as an example. Basically, variables are assigned to the inputs and outputs, and the logic function is described by a Boolean equation. If desired, an 8-bit identification code ('signature') can be burned into the chip.

Next, run a check on the program syntax. This requires an auxiliary program such as 'EQN2JED' included in the Opal Junior ™ GAL programming software package from National Semiconductor (this package is supplied free of charge with your GAL programmer software, how's that?). When no errors are detected, EQN2JED generates the documentation file GALDEMO1.DOC (Fig. 5), and the associated JEDEC file, GALDEMO1.JED (Fig. 4). The JEDEC file produced with the aid of EQN2JED contains all information on the cells contained in the GAL, and serves to actually program the device.

The software

After starting the control program, GAL651AE.EXE, the screen shows the start and end indicators. Further, the screen graphics indicate three blocks: the JEDEC file, the matrix memory and the GAL's hardware environment. The command names are shown in between the blocks, and can be selected by typing the highlighted letter. Command abbreviations may also be used. An error 'beep' sounds when you enter a nonexisting command.

The **GAL TYPE** command allows you to select the device type to be handled. This selection must be completed before the GAL is inserted into the ZIF socket on the programmer board. While executing the GAL commands, the software automatically checks if the right GAL type is being used.

The **READ** command is used to transfer the JEDEC file into the matrix memory. After entering '1' and a return, the listing is displayed of the JEDEC file in the selected subdirectory. Alternatively, you may enter the full path and file name. After requesting a file list (for instance, A:*.*), the screen shows all JEDEC files found. The desired file is selected by moving to it using the PageUp and PageDown keys and the arrow keys. The return key activates the selected command, which then operates on the selected file.

The use of the **WRITE** command is similar to that of the READ command described above. An 'overwrite?' alert is shown if you save a file under a name that is already in use in the selected (sub-) directory. All file names are automatically saved with the '.JED' extension appended.

Selecting **PROGRAM** from the menu

COMPONENTS LIST

Resistors:

19	10kΩ	R1;R5;R7-R12; R15-R25
3	4kΩ7	R2;R3;R4
1	560Ω	R6
2	1kΩ25	R13;R14
1	2kΩ7	R26
1	270Ω	R27
1	390Ω	R28
1	7-way 10kΩ SIL	R29
1	1kΩ preset H	P1

Capacitors:

8	100nF	C1;C6;C8;C9-C13
2	220µF 16V	C2;C3
1	1000µF 16V	C4
1	470µF 25V	C5
1	47µF 16V	C7

Semiconductors:

1	LED 3mm red	D1
1	1N4148	D2
6	1N4001	D3-D8
1	LED 3mm green	D9
3	BC547B	T1;T2;T3
2	BC327	T4;T5

2	BC369	T6;T7
1	74HCT04	IC1
1	74HCT125	IC2
1	4555	IC3
2	4094	IC4;IC5
1	7805	IC6
1	LM317	IC7
1	24-way ZIF socket *	IC8

Miscellaneous:

1	36-way Centronics socket for PCB mounting	K1
1	3-way PCB terminal block	K2
1	Mains transformer 2×6V @4VA, e.g., Monacor (Monarch) FTR46	Tr1
1	Fuse 630mA slow, with PCB mount holder and cap	F1
1	Printed circuit board	920030
1	Control software package	ESS1701

* Aries Electronics. Distributor info from Aries Electronics (Europe), Unit 3, Furtho Court, Towcester Road, Old Stratford, Milton Keynes MK19 6AQ. Tel. (0908) 260007, Fax (0908) 260008.

```
title Basic gate
pattern GATES
revision A
author Nosswitz
Date 05.02.92

chip GATES GAL16V8

;pin 1  2  3  4  5  6  7  8  9  10
     C  D  F  G  M  N  P  Q  IX GND
;pin 11 12 13 14 15 16 17 18 19 20
     JX KX L  RX O  H  E  B  A  VCC

@UES MB123456

equations
   B = /A
   E = C * D
   H = F + G
   L = /IX + /JX + /KX
   O = /M * /N
   RX= P * /Q + /P * Q

; end of GATES
```

Fig. 3. Example of a GAL equation file.

```
GAL16V8
EQN2JED - Boolean Equations to JEDEC file assembler (Version V003)
Copyright (R) National Semiconductor Corporation 1990,1991
Assembled from "galdemo1.eqn". Date: 2-19-92
title Basic gate
pattern GATES
revision A
author Nosswitz
Date 05.02.92
*
QF2194*QP20*F0*
L0256
11111110111111111111111111111111*
L0512
01011111111111111111111111111111*
L0768
11110111111111111111111111111111
11111110111111111111111111111111*
L1024
11111111111101110111111111111111*
L1280
11111111111111111110111110111111
11111111111111111111101101111111*
L1536
11111111111111111111111111111011
11111111111111111111111111111110
11111111111111111111111111101111*
L2048
01111110*
L2056
010011010100001000110001001100100011001100110100001101010100110110*
L2120
10000001*
L2128
000000001000000010000001100000010000001100000011100000000000000*
L2192
10*
C2B31*
0000
```

Fig. 4. JEDEC output file produced by the EQN2JED utility from National Semiconductor.

```
EQN2JED -- Boolean Logic to JEDEC
file assembler (Version 1.00)
Copyright (R) National Semiconductor
Corporation 1990

Document file for galdemo1.txt
Device: 16V8

Pin  Label   Type
---  -----   ----
1    C       com input
2    D       com input
3    F       com input
4    G       com input
5    M       com input
6    N       com input
7    P       com input
8    Q       com input
9    IX      com input
10   GND     ground pin
11   JX      com input
12   KX      com input
13   L       pos,com output
14   RX      pos,com output
15   O       pos,com output
16   H       pos,com output
17   E       pos,com output
18   B       pos,com output
19   A       com input
20   VCC     power pin

EQN2JED -- Boolean Logic to JEDEC
file assembler (Version 1.00)
Copyright (R) National Semiconductor
Corporation 1990

        Chip diagram (DIP)

          C  | 1     20 |  VCC
          D  | 2     19 |  A
          F  | 3     18 |  B
          G  | 4     17 |  E
          M  | 5     16 |  H
          N  | 6     15 |  O
          P  | 7     14 |  RX
          Q  | 8     13 |  L
          IX | 9     12 |  KX
          GND| 10    11 |  JX
```
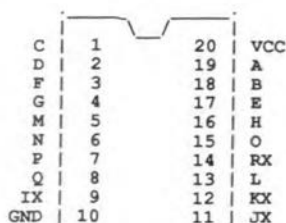
Fig. 5. Example of a documentation file produced by EQN2JED.

The **COPY PROTECT** command may be used to actuate the copy protection ('security bit') in the GAL. When the security bit is set, it is impossible to read anything from the GAL except the identification code and the GAL configuration.

The **BULK ERASE** command may also be used on its own, i.e., not as part of a programming sequence, to clear the contents of a GAL. This obviates the need for an erase operation before programming.

OUTPUT TO LPT1: directs the matrix contents to a printer connected to the LPT1: output of the PC. Needless to say that hard copy of the matrix contents may be very useful for documentation purposes.

The **SHOW/EDIT** command allows you to examine, on the screen, the content of the selected location. If a specific cell is selected, the cursor starts to flash at this location. At the same time, the identification code, if given in the source code, is shown in hexadecimal as well as ASCII notation.

The F10 key takes you to the edit mode, which makes it possible to change the cell contents with the aid of the cursor keys. The 'Fill' function may be used to fill a block in the GAL with ones or zeroes.

Selecting the **Program**, **Verify** or **Load** commands causes the number of programmed cells, the GAL manufacturer, and the checksum to be shown in the GAL symbol on the screen.

The function of the **End** command will be obvious.

Finally, any command entered may be terminated with the aid of the ESC (escape) key. ∎

sets off a sequence of activities. First, a 'bulk erase' operation is performed. Next, the device is programmed. Finally, the contents of the GAL are verified against the program file. If an error is found, the relevant cell in the GAL is indicated, along with the relevant data in the GAL and in the file.

```
GAL.CFG
{licence number}
{user number}
$378  Adress of Centronics port for GAL data exchange
2000  error display time in ms
2000  error beep frequency in Hz
75    beep length in ms
1     Check if GAL hardware accessible               no=0    yes=1
0     Switch for general RESET (EPROM, PROM, GAL)  no=0    yes=1
1     Basic GAL type selection  16V8=1, 20V8=2, 16V8A=3, 20V8A=4
1     Background colour: Text (blue)
7     Foreground colour: Text (bright grey)
5     Background colour: Error reports (magenta)
7     Foreground colour: Error reports (bright grey)
5     Background colour: Letters (magenta)
15    Foreground colour: Figures (white)
7     Background colour: Selection window (bright grey)
1     Foreground colour: Selection window (blue)
5     Background colour: Selection bar (magenta)
14    Foreground colour: Selection bar (yellow)
4     Background colour: Changed cells (red)
7     Foreground colour: Changed cells (bright grey)
12    Line distance to upper paper edge (printing)
12    Line distance between page 1 and page 2 (printing)
20    Empty lines after page 2 (printing)
8     Character distance from left-hand paper edge (printing)

Addresses of Centronics ports
LPT2: 278H
LPT1: 378H
LPT1: 3BCH (on Hercules-compatible card)
```

Fig. 6. The control program for the GAL programmer reads 25 parameters from a configuration file called GAL.CFG. This file can be produced or edited with any simple word processor, such as EDLIN or the one in PCTools. All 25 parameters must be present in the order shown here. The meaning of the values is apparent from the comment in each line.
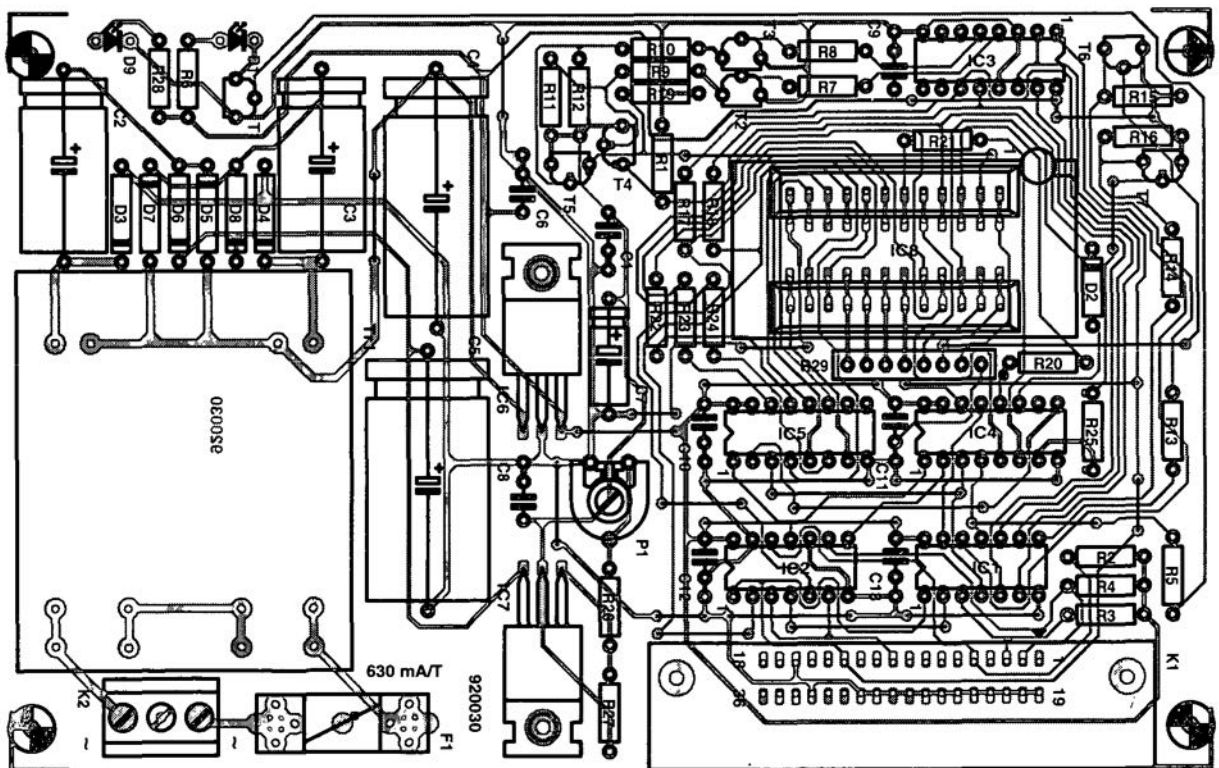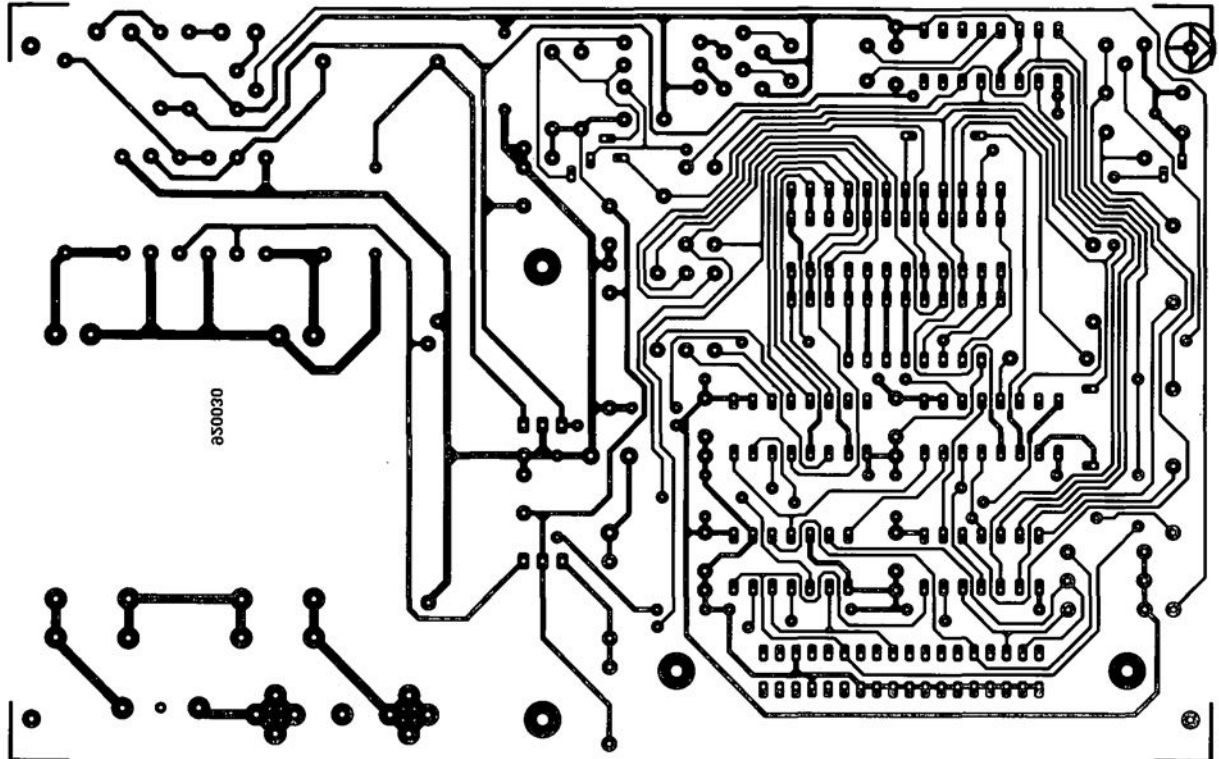
Fig. 2. Track layout (mirror image) and component mounting plan of the single-sided PCB for the GAL programmer.

8751 Emulator

(Corrections; component information)
While in emulation mode, the register contents are displayed with an offset of one vertical line from the associated register designations. This error occurs on early releases of the system software, item ESS 1741, and is caused by one superfluous 'space' character in the DEV.EXE program. This 'space' (20H) should be changed into a 'line feed' (0AH). First, make a backup copy of your original diskette. Next, use a hex editor to change the byte at address offset DE0DH from 20H into 0AH. Using the hex editor of PCTools V6, for instance, this byte is found in relative sector 111 (decimal!), at offset 0DH.

Pins 52, 53 and 54 of the SC80C451 must be connected to ground to give proper access to (simulated) Port 0. For no apparent reason, this is not indicated in the Signetics datasheets. Port 0 is actually

CORRECTIONS AND UPDATES

simulated by Port 6 of the SC80C451. For further information on this compatibility problem with generic 8051 assembler files, consult the SC80C451 (Signetics) or 8xC451 (Intel) datasheets.

In addition to your local Signetics (Philips Semiconductors) distributors, two suggested suppliers of the controller Type SC80C451CCN64 are:

(1) Macro Marketing Ltd., Burnham Lane, Slough SL1 6LN. Telephone (0628) 604383.

(2) C-I Electronics, P.O. Box 22089, 6360 AB Nuth, Holland. Fax: +31 45 241877.

GAL programmer

(Update)
The transistors Type BC369 in positions T6 and T7 are apparently difficult to obtain, and may be replaced by BC640s.

The most recent version of the software is V. 6.53dt, June 1992. The README file contains an update note on problems with the programming of certain GAL makes, as well as a suggestion to make GALs with a damaged electronic signature (type identifier) useable again.

8051 Single board computer

(Update)
Since the publication of this article, we have been advised that the telephone number of Suncoast Technologies is +1 (904) 596-7599.

herhaling zie mei 92

NEW LOGIC SYMBOLS

by our technical staff

IN the late 1960s, the International Electro-technical Committee, IEC, set up a working group to devise symbols for binary logic. The work of this group culminated in the early 1980s in IEC Publication 617: Graphical Symbols for Diagrams, Part 12: Binary Logic Elements. This standard, published in 1983, went into general circulation in early 1984. It takes into account the use of computer-aided drafting equipment and all symbols are designed on a grid.

The symbology contained in the standard provides that each symbol has one meaning only; rules are given how these symbols can be united to form the most complex logic functions. In a way, it may be compared to the higher programming languages: these, too, contain symbols (letters, ciphers, punctuation marks) that have one meaning; syntax is used to unite them into complete computer programs.

In spite of the standard having been published in 1983, even today many manufacturers feel obliged to give the 'old' symbol alongside the new IEC symbol. The reason for this is that, although the new symbols are far more informative than the previous ones, they have to be learned like a new language. And it remains true that most of us are conservative: we don't like change.

Nevertheless, we feel that the time has come to start using the new symbols in our drawings. Most technical schools and colleges, as well as the semiconductor industry, have been using them for years. The reason that we have been slower than usual in adopting a newer and better technique is a very practical one. Our design department has been investing in the acquisition and further development of computers and software that are able to provide the desired quality of graphics output—note that a 'normal' CAD system is *not* suitable. However, these systems have recently come 'on stream' and the department can now start using electronic means of reproducing the new symbols.

Do not think, though, that we are changing overnight: the move to using the new symbols will be a gradual one and will probably take until the end of the year. To prepare you for the change, a number of symbols for the basic functions, as well as a few more complex ones, are shown in the illustrations. We will publish the illustrations again in a number of future editions.

An important point to bear in mind is, though, that we are not adopting the new IEC symbols automatically in all cases: several are far larger than the previous symbols and their use might mean that the relevant circuit diagrams would become rather unwieldy for reproduction in the magazine. In such cases, we may choose a simplified sym-bol that is more akin to the old one. This will, of course, be made absolutely clear in the text, on the diagram or in the caption to the diagram.

Do not be put off by a first sight of the new symbols: they may seem complicated at first, but they offer excellent facilities for specifying designs without requiring precise forms of implementation. At the same time, they retain a precise specification of the required logic functions with the minimum amount of support documentation.

An excellent book for learning to understand the new symbols is *A practical introduction to the new logic symbols* by Ian Kampel, ISBN 0 408 01461 X, published by The Butterworth Group, Borough Green, Sevenoaks TN15 8PH, England.

TABLE 1

Dependency notation

The letter x in this table is used to denote an identifying number; substitution of an appropriate number is required in normal usage.

Ax	ADDRESS dependency
Cx	CONTROL dependency
ENx	ENABLE dependency
Gx	AND dependency
Mx	MODE dependency
Nx	NEGATE dependency
Rx	RESET dependency
Sx	SET dependency
Vx	OR dependency
Zx	INTERCONNECTION

TABLE 2

### General qualifying symbols

&	AND gate or function
≥1	OR gate or function
=1	XOR gate or function
=	Logic identity
1	The single input must be active (i.e, non-inverting buffer)
$2k$	An even number of inputs must be active
$2k+1$	An odd number of inputs must be active
X/Y	Coder or code converter (e.g., DEC/BCD, BIN/7-SEG)
MUX	Multiplexer
DMUX	Demultiplexer
Σ	Adder
P–Q	Subtractor
CPG	Look-ahead carry generator
π	Multiplier
COMP	Comparator
ALU	Arithmetic logic unit
⊓	Retriggerable monostable
1⊓	Non-retriggerable monostable
G⊓	Astable, general symbol
!G⊓	Astable, synchronously starting
G!⊓	Astable, synchronously starting, stopping after completion of last pulse
SRGm	Shift register where substitution for m specifies number of bits
CTRm	Counter where substitution for m specifies number of bits
CTRDIVm	Counter/divider where substitution for m specifies cycle length
RCTRm	Asynchronous counter where substitution for m specificies cycle length
FIFO	First-in first-out memory
CT=m	If output: active if the counter state of the register content is m. If input: when active, the counter state of the register content is set to m
I=0	Element is reset at power-up
I=1	Element is set at power-up
RAM	Random-access memory
DRAM	Dynamic random-access memory

Table 3 (opposite page). Qualifying symbols and symbols used inside the outline.

Symbol	Description	Symbol	Description	Symbol	Description
General logic symbol		Output with larger than usual output power (indicates direction of signal current)		BI	Borrow-in input
Logic with common control		Data input	D	BG	Borrow-generate input
Logic with common output		J input	J	BG	Borrow-generate output
Polarity indicator at input		K input	K	BO	Borrow-out output (e.g., ripple)
Polarity indicator at input (for information from right to left)		R (reset) input	R	BP	Borrow-propagate input
Polarity indicator at output		S (set) input	S	BP	Borrow-propagate output
Polarity indicator at output (for information from right to left)		T (toggle) input	T	CI	Carry-in input
Dynamic input (edge triggered)		Shift right (down)		CG	Carry-generate input
Dynamic input		Shift left (up)		CG	Carry-generate output
Internal connection		Count up	+	CO	Carry-out output
Internal connection with negation		Count down		CP	Carry-propagate input
Internal connection with dynamic character		Query (interrogate) input	?	CP	Carry-propagate output
Internal connection with negation and dynamic character		Compare output of an associative memory	!	CT=m	Content input
Internal (virtual) input		Bit grouping symbol for inputs	o...m	CT=m	Content output
Internal (virtual) output		Bit grouping symbol for outputs	o...m		Line grouping symbol for inputs
Output of a pulse-controlled element		Operand (P) input	P		Line grouping symbol for outputs
Bi-threshold (input with hysteresis)		Operand (Q) input	Q		Non-logic input
Open-circuit output		Greater-than input	>		Non-logic output
Open-circuit H-type output		Less-than input	<		Input for analogue signals
Open-circuit L-type output		Equal input	=	#	Input for digital signals
Passive pull-down output (similar to 19 but containing internal pull-down resistor)		Greater-than output of a comparator	*>*		Analogue output
Passive pull-up output (similar to 20 but containing internal pull-up resistor)		Less-than output of a comparator	*<*	#	Digital output
3-state output		Equal output of a comparator	*=*		
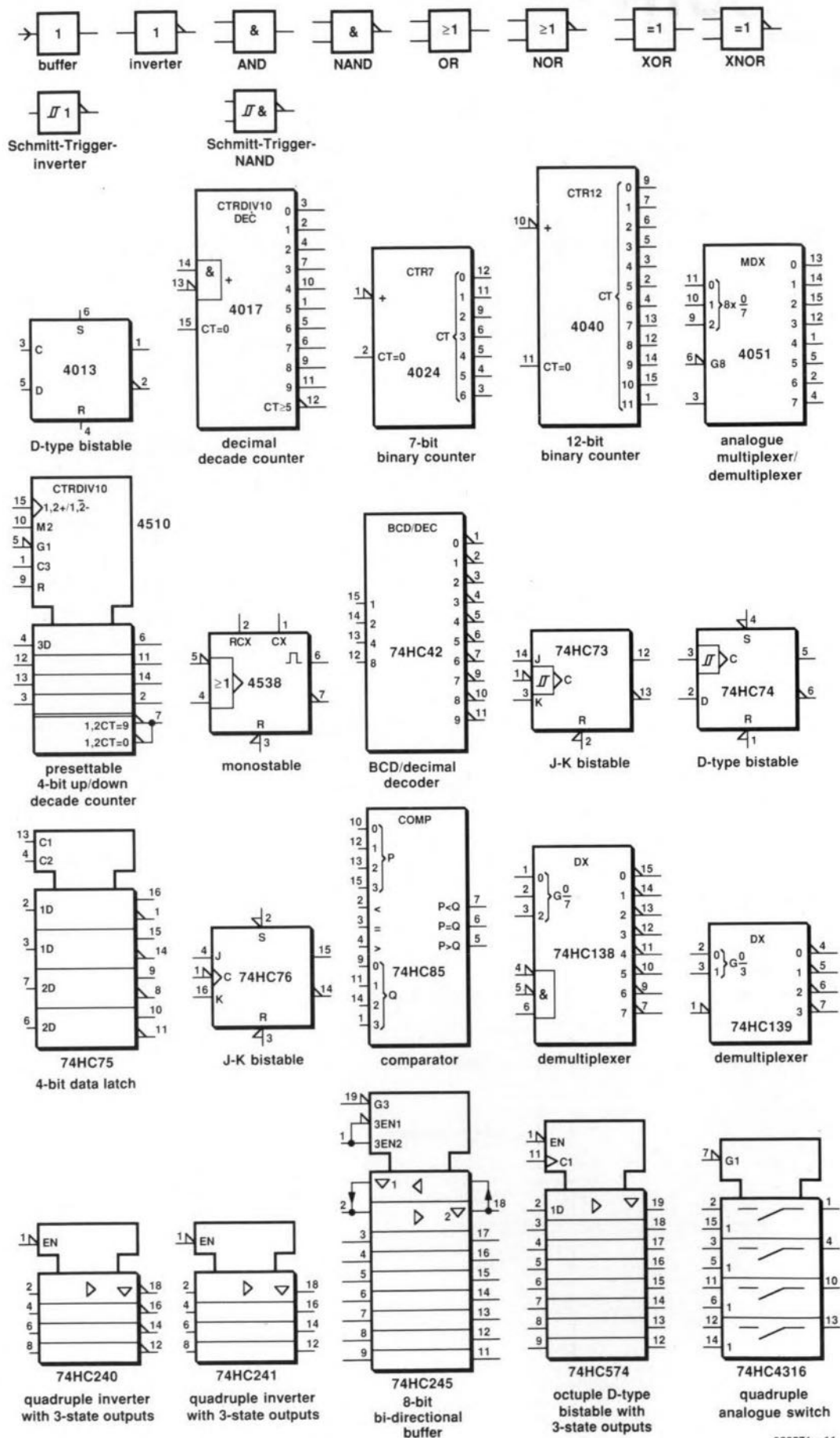
Fig. 1. A number of examples drawn according to IEC standard No. 617.