ELEKTOR ELECTRONICS

Top-of-the-range FM tuner

Comb generator

AD232 converter

Generic array logic

2 metre receiver

Red-light diode lasers

Super sign

Review of Pulsar
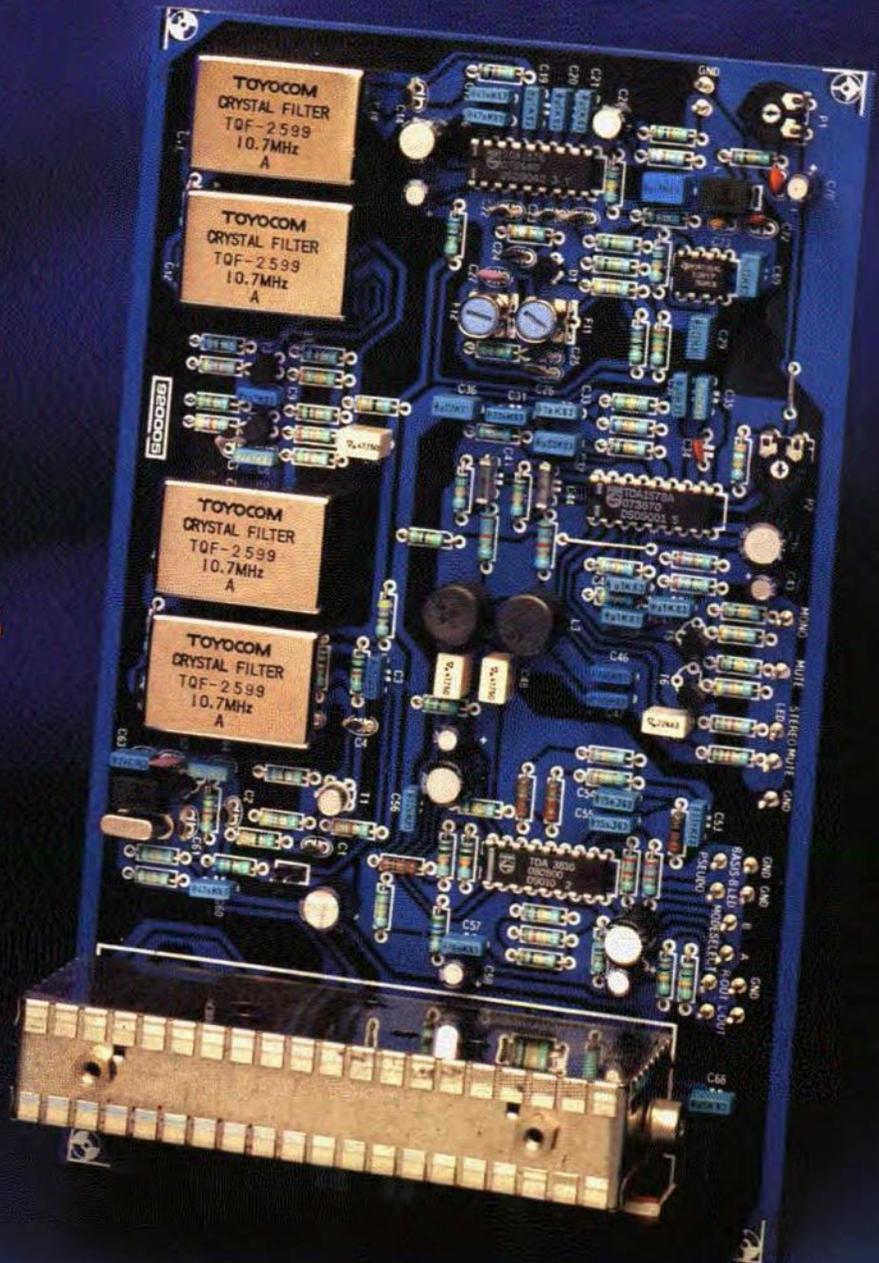
ELEKTOR ELECTRONICS

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Front cover
The FM tuner described in a series of articles that started last month has specifications that challenge those of the best commercial tuners available. Shown is the finished main tuner board. The (ready-made) tuner module used prevents problems with building and adjusting the RF circuitry.

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COMB GENERATOR

The name of the test instrument described here is based on the frequency spectrum it produces. The circuit will be particularly valued by owners of (ex-surplus trade) spectrum analyzers, because it produces hundreds of harmonics of 1 MHz or 10 MHz, of which the first 45 or so have the same output level within 3 dB.

Design by J. de Belie

Here's something to put your hair in order! Comb-type output spectrum from DC to about 1 GHz (VHF mode).

INSERTING a filter between the output of the comb generator and the input of a spectrum analyser allows you to ascertain, and, if necessary, adjust, the filter characteristic. Similarly, the comb generator allows the frequency characteristic of an ex-surplus trade spectrum analyzer to be checked.

Basic operation

A comb generator is basically a circuit that generates a very short pulse periodically. Its operation is predicted (or, if you like, confirmed), by Fourier analysis.

Assuming that a purely digital pulse is generated with a duty factor of 1% ($t_{on}/t_{off}=0.01$), the amplitudes of the harmonics are weighted to $(\sin x)/x$ (sine roll-off). This means that
- the amplitude of the first couple of harmonics will be 1% of that of the original pulse;
- the amplitude does not drop to:
  −1 dB up until the 26th harmonic;
  −2 dB up until the 37th harmonic;
  −3 dB up until the 44th harmonic;
  −5 dB up until the 55th harmonic;
  −10 dB up until the 74th harmonic.

The attenuation will be infinite (in principle) at the 100th harmonic, and multiples thereof. In practice, the deviation from the theoretical model is small (for a change), in particular in the HF section of the present generator.

Circuit description

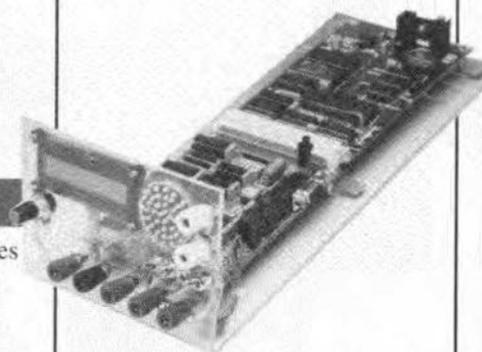The recently introduced family of AC (Advanced CMOS) logic devices allows very fast pulses to be generated at relatively high output power levels. Here, the fundamental generator frequencies are 1 MHz (HF mode) and 10 MHz (VHF mode).

HF pulse generator

With reference to the circuit diagram in Fig. 1, when switch S1 is set as shown, the VHF part of the circuit is disabled via gate IC2a. One section of dual decade ripple counter IC3 divides the 10-MHz clock signal by 10. The 1-MHz output signal is buffered

by an ACL gate, IC2c, to make sure that the signal edges are sufficiently steep. The output of the buffer is loaded with an R-C network that results in 7.6-ns long 'low' levels of the 1-MHz (1 μs) output signal. A further ACL gate, IC2d, is used to provide sufficient drive power at the HF output, K2. Capacitor

C19 in combination with resistors R13 and R14 provides a termination impedance of about 50 Ω.

The use of AC logic means that the duty factor of the output signal depends to a small extent on the supply voltage and the ambient temperature. Fortunately, this does not seem

to be a problem for the first tens of harmonics, whose level was found to remain virtually constant. Here, a slightly higher than normal IC supply voltage is used (5.7 V) to keep duty factor reduction as small as possible. Remember, the speed of the gates increases with the supply voltage, so that the duty factor would become smaller; this in turn would cause a lower pulse level.

The –3 dB roll-off frequency of the HF section lies at about 50 MHz. The first minimum occurs at about 130 MHz. The output level, about –25 dBm, will be sufficient for most applications (in RF design, 0 dBm equals 1 mW into 50 Ω).

The level of the multiples of the second harmonic may deviate by a maximum of ±3 dB. This effect may be reduced to a minimum by decoupling the 74AC11000 supply pins. If necessary, relocate C1 (a 1-μF tantalum capacitor) from its normal position on the board to the underside, where it is soldered directly across the supply pins of the 74AC11000.

VHF pulse generator

When VHF mode is selected with switch S1, divider IC3 is disabled to prevent subharmonics occurring in the output spectrum. The clock buffer is followed by a fast switching transistor Type BSX20 (T1), which is operated in class C. The transistor stage produces a 10-MHz output signal with a power of about 50 mW. The transistor drives the pulse shaper proper via an inductor, L1.

An old trick is rehashed to generate a pulse with a very short, accurately defined, length. Here, 1 ns (1×10⁻⁹ s) is required. The pulse shaper is formed by a short-circuited length of 50-Ω coax cable plus a fast diode. The length of the coax cable is calculated from

$$\tfrac{1}{2} \cdot 0.6 \cdot 3{\times}10^{8} \cdot 1{\times}10^{-9} = 0.09 \text{ m.}$$

in this equation, the factor 0.6 is the velocity factor of the coax cable, and $3{\times}10^{8}$ is the speed of light in a vacuum.

A number of diodes were tried out in position D1. Remarkably, the inexpensive and fairly common Type BA482, a VHF band switching diode, was found to give the best results.

The output level of the VHF section is about –20 dBm. This level drops by –2 dB at about 200 MHz, and by –8 dB at about 400 MHz. The first minimum occurs at about 1 GHz, the second at 2 GHz, etc. This means that no further filters are required to prevent base line shift when the comb generator is used with the popular HP8551 spectrum analyser.

Construction

The repeatability of the circuit is pretty good when constructed on the printed circuit board shown in Fig. 2. All parts are fitted with the shortest possible lead lengths. The metal film resistors are preferably from the SFR25 series (Philips Components). All non-electrolytic capacitors are ceramic types, al-

Fig. 1.   Circuit diagram of the comb generator. The 1-ns pulse shaper in the VHF section is formed by a piece of coax cable and a fast switching diode.

though MKT or polycarbonate will also work for the larger values (47 nF and 100 nF).

Do not use sockets to fit the ICs, and take care not to overheat the trimmer and the quartz crystal when soldering. The centre pins of the BNC sockets, K1 and K2, are soldered directly on to the board, and the threaded parts of the shafts are secured to the PCB with a clamp.

The coax stub is cut to a length of 9 cm. One end is short-circuited, the other soldered to the points marked 'K3' on the PCB (the coax braid is soldered direct to the PCB ground plane).

The inductor, L1, consists of 9.5 turns of 1 mm dia. (SWG20) silver-plated wire. The inductor has an internal diameter of about 21 mm, and is conveniently wound on a tube lighting starter. Wind the 9.5 turns close-spaced, and remove the former you have used. Next, draw out the coil, and spread the turns evenly (introductory photograph). A tap is made at 3 turns from one side. Solder

the inductor on to the PCB, and correct the spacing if necessary. Make sure that the turns can not touch the ground plane at the component side of the board, and fix them with a small amount of candle wax.

The circuit must be screened all around by a 25-mm high piece of tin-plate. The shape of the screen is indicated by the dashes on the printed circuit board. Drill an 8-mm hole to enable the coax stub to pass through, and two 9-mm holes for the BNC sockets. Solder the screen securely to the board with the aid of a powerful soldering iron. The screen and the PCB together form a box, for which a lid is easily made from a 75×95-mm piece of tin plate (bend approx. 2.5-mm at the four edges to enable it to be clamped on to the screen on the PCB). The lid is drilled to hold the HF/VHF switch. The positive power supply connection is preferably made via a 1-nF feedthrough capacitor fitted into one of the sides of the box. The unit thus made may be fitted into another, larger, enclosure that may also contain the 15-V power

Fig. 2.   Double-sided printed circuit board design for the comb generator.

COMPONENTS LIST

Resistors:

2	47Ω	R1;R3
1	150Ω	R2
2	100Ω	R4;R6
1	68Ω	R5
2	1kΩ	R7;R12
1	22Ω	R8
1	2kΩ2	R9
1	1MΩ	R10
1	10kΩ	R11
1	120Ω	R13
1	82Ω	R14

Capacitors:

1	1µF 15V tantalum	C1
2	10µF 25V	C2;C3
5	47nF ceramic	C4;C5;C7; C14;C17
1	10µF 16V	C6
2	150pF ceramic	C8;C11
1	1nF ceramic	C9
1	10nF ceramic	C10
1	100pF trimmer	C12
1	82pF ceramic	C13
2	39pF ceramic	C15;C16
1	15pF ceramic	C18
1	100nF ceramic	C19
1	1µF 16V radial	C20

Inductor:

L1 Made from 1-mm dia. (SWG20) silver-plated wire; for construction details see text.

Semiconductors:

1	BA482	D1
1	1N4148	D2
1	BSX20	T1
1	7805	IC1
1	74AC11000N	IC2
1	74HC(T)390	IC3

Miscellaneous:

2	BNC socket	K1;K2
10cm RG58 50Ω coax, velocity factor 0.6		
1	miniature on/off switch	S1
1	10MHz quartz crystal	X1
1	Printed circuit board	920003

supply. Alternatively, you may want to fit the PCB into a diecast (Eddystone) enclosure, from which the BNC sockets protrude.

The unit must be powered by a regulated 15-V source. A 'classic' supply based on the 7815 will be adequate for this purpose. Current consumption is smaller than 50 mA.

Adjustment

The adjustment of the comb generator is straightforward, and involves only one trimmer. Connect a spectrum analyzer to the VHF output, and peak C12 for highest signal level. Lacking a spectrum analyzer, connect an oscilloscope via a 10:1 probe to the collector of T1 (test point '1'). Adjust C12 for best sine shape and highest amplitude of the waveform. In most cases, this adjustment will be entirely satisfactory, although the trimmer may have to be set to a slightly larger capacitance afterwards to compensate the probe capacitance.

Finally, for advanced users: if you require a smaller frequency interval, change the divisor (IC3; VHF output), or (better) change the crystal frequency. In most cases, it will also be necessary to change the pulse duration appropriately; if this is not done, the output level will almost certainly drop. Note, however, that although increasing the pulse duration keeps the output power at the old level, it lowers the maximum usable frequency.   ■
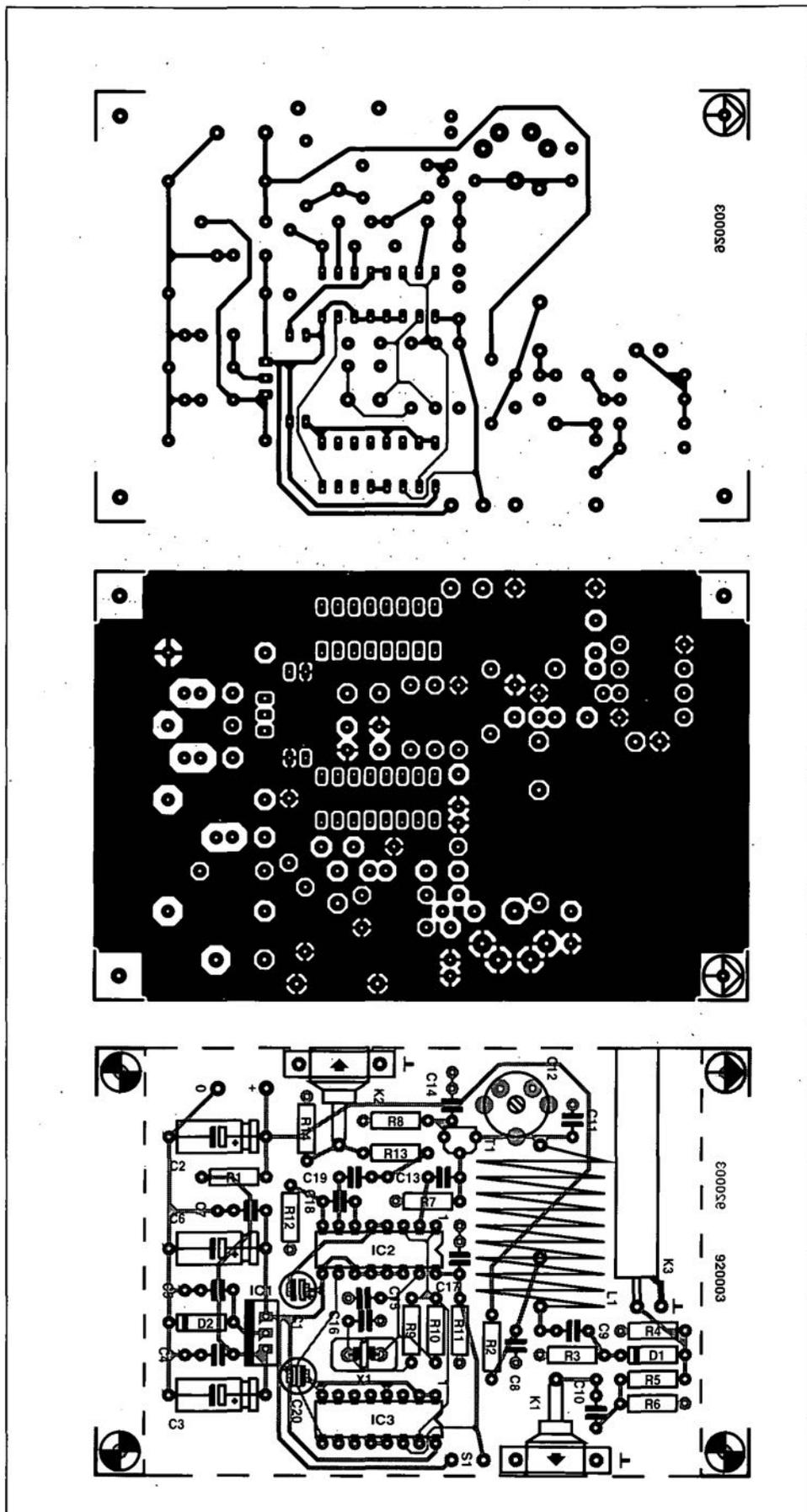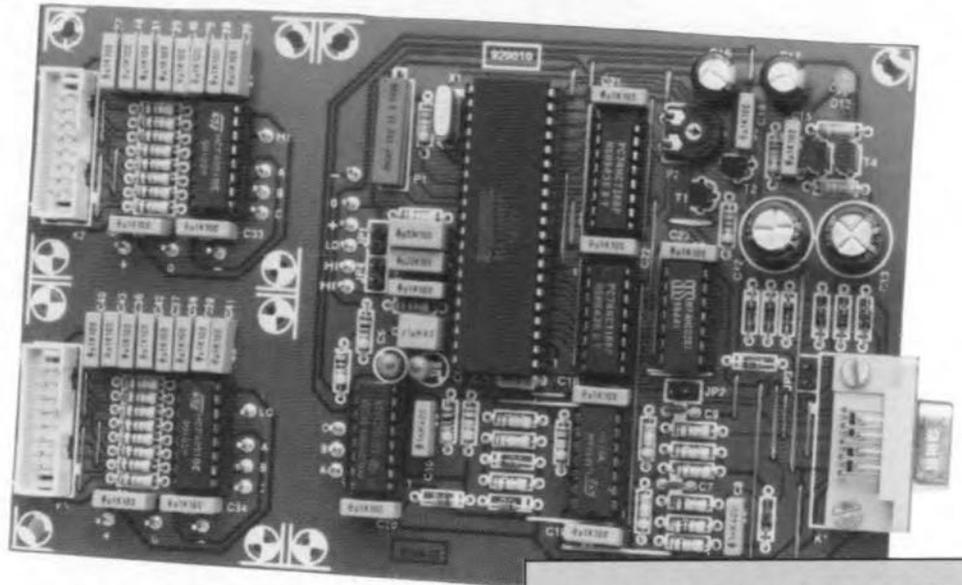
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1	10nF ceramic	C10
1	100pF trimmer	C12
1	82pF ceramic	C13
2	39pF ceramic	C15;C16
1	15pF ceramic	C18
1	100nF ceramic	C19
1	1μF 16V radial	C20

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AD232 CONVERTER

The well-known ICL7106 A-D converter IC has been with us in many generations of digital multimeter. A special version of it, the ICL7109, offers the same accuracy, comes at a low price also, but sports a parallel interface instead of a 7-segment driver. The ICL7109 requires only a handful of components to build a versatile measuring box with an RS232 interface that is easy to manage thanks to some hardware tricks. Software for IBM PCs and compatibles is available to control this unit, which is basically a multiplexed A-D converter with an RS232 interface.

MAIN SPECIFICATIONS

- For every PC with a serial port
- 16-channel input multiplexer
- 12-bit A-D converter
- Powerful graphics-based menu-driven control software
- Based on inexpensive ICs
- Powered by PC

Design and software by Ing. B.C. Zschocke and A. Arnold

THE concept of the circuit is illustrated in the block diagram in Fig. 1. At the left are three input blocks with low-pass filter characteristics, marked HI', HI and LO. The HI and LO blocks represent eight input channels, each of which can be selected individually by the block marked 'select'. The part behind the input selection circuitry allows switching between the HI' (direct) input and the switchable inputs.

The A-D (analogue-to-digital) converter behind the input circuitry supplies its digital output data to a parallel-to-serial converter via a parallel bus. Unusually, the output information of the format converter is connected the CTS (clear to send) handshaking line of the RS232 port, rather than the RxD (received data) line. This arrangement results in a much simpler control of the measuring box than would be possible if the RxD line were used.

The circuit is powered by the RS232 port on the PC. The power supply block shown in the diagram provides a regulated output voltage of ±5 V for the converter, and ±12 V (approximately) for the serial interface.

Connection problems

The serial (RS232) interface is used here because the parallel (Centronics) interface can not furnish enough current to power the RS232 A-D converter. Furthermore, in most cases it is easier to find a free serial port on a PC than a free Centronics port, while the use of longer cables is also a boon. On the down side, a serial link is much slower than a parallel link, so that relatively slow ADCs can be used only. Fortunately, this is not always a disadvantage, because slow but very accurate ADCs are inexpensive and widely available. Also, it is not always necessary to
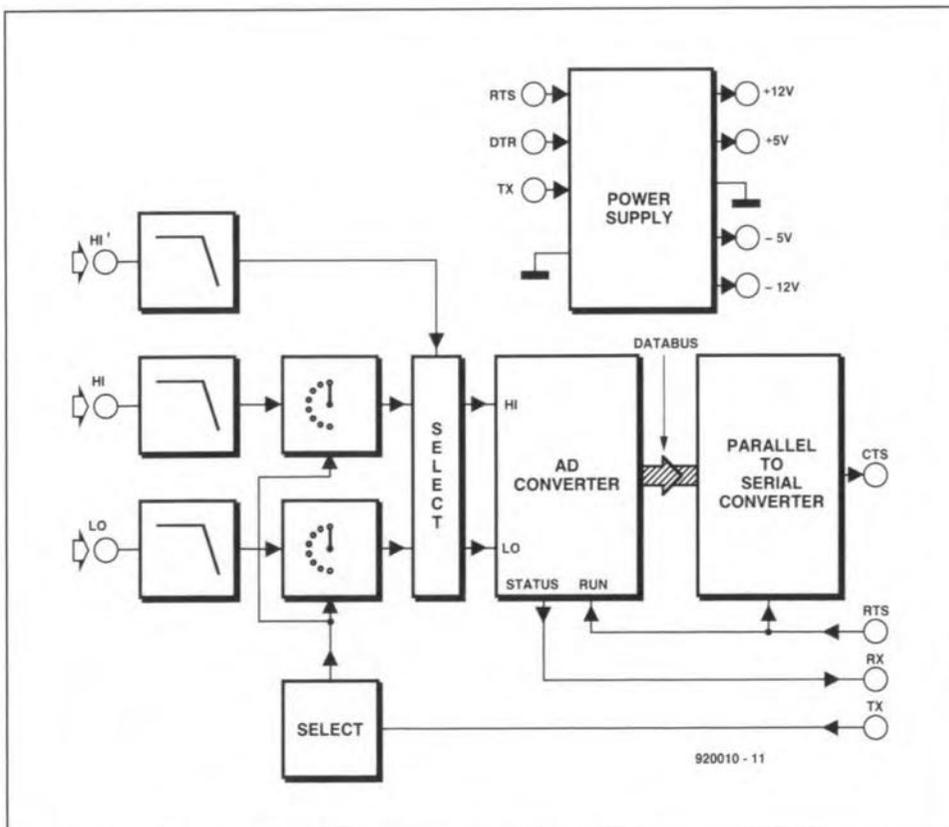
Fig. 1. Block diagram of the RS232-controlled A-D converter.

sample slowly varying measuring quantities at kHz rates.

The ICL7109 ADC used here differs from the ubiquitous ICL7106 by the digital interface only. The input circuitry is almost identical for both ICs.

Interface parameters can be a real problem when implementing an RS232 link and keeping to the standards. For instance, the link will work correctly only if the transmitter and the receiver are set to the same data format (number of data bits and start/stop bits), but also to the same data rate (in bits per second, or baud). Many of you will know the difficulties and frustrations in setting up a serial link, with obstacles such as DIP switches, configuration files, MODE commands, and long series of parameters.

Here, the RS232 link is used in a nonstandard way to avoid some of the problems mentioned above. Data is conveyed via CTS, and clocked by another handshaking line, RTS (ready to send). Four good reasons can be given for this choice:

- The control software determines when and how fast data is conveyed. It is not necessary to configure the serial port. This is particularly attractive when the interface is used for several different peripherals.
- Conveying data via a 'standard' RS232 link requires either special interfacing circuits with internal or external oscillators, or complex discrete alternatives.
- The AD232 board can be linked to interfaces that are not fully RS232 compatible, or directly to a microcontroller.
- The component count is quite low.

Details

The circuit diagram is given in Fig. 2. A quadruple opamp, IC6, forms the RS232 interface. Circuits IC4, IC7 and IC8 form a simple input multiplexer. IC1 is the ADC proper. The two 74HCT166s, IC2 and IC3, form a 16-bit shift register for the parallel-to-serial conversion. The four XOR gates in the 74HC02 package, IC5, control the timing of the A-D conversion, and generate a clock signal for the shift registers.

The power supply takes its input voltage from the RS232 interface in the PC, and provides the stabilized ±5 V rails for the converter circuitry. The analogue-to-digital conversion starts when a level transition is detected at the RTS input. Opamp IC6a makes the RTS signal TTL compatible, and its output signal causes bistable IC5c-IC5d to toggle. The high level at pin 10 of IC5 triggers the A-D conversion in IC1. When the conversion result is available, the ICL7109 supplies a $\overline{\text{LOAD}}$ signal to the shift register, IC2, via gates IC5a and IC5b. First, the high (most significant) byte is loaded into IC2, then the low (least significant) byte into IC3. The signals $\overline{\text{HBEN}}$ (high byte enable) and $\overline{\text{LBEN}}$ (low byte enable) are treated in an unusual manner here. When low, these signals switch the associated register from shifting to loading. Because $\overline{\text{HBEN}}$ and $\overline{\text{LBEN}}$ can never be low
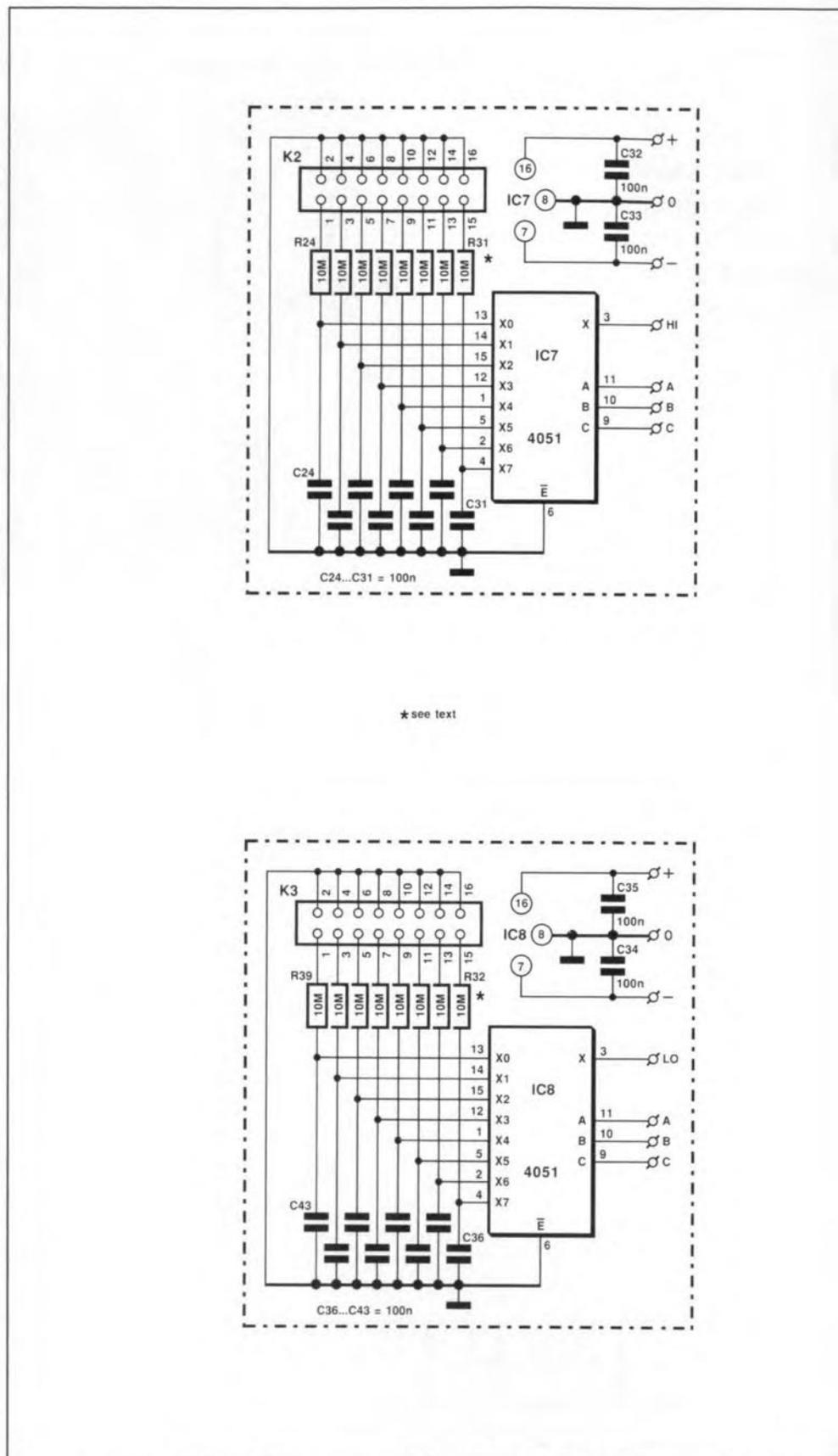

★ see text

Fig. 2.   Circuit diagram of the measurement system. The two input multiplexers are optional, a

at the same time, and the clock inputs of the registers are interconnected, this results in the shift registers being in opposite mode all the time, i.e., when one loads, the other shifts. This has no significance for the loading of the high byte, while the high byte is shifted one position in IC3 during loading. Bits 7 and 8 in the high byte, which are not used by the converter, are made permanently high. This is done to bring about a

level change on the CTS line after the shifting, when the low byte is loaded. This change can be used as an interrupt request in the PC, or as a 'conversion ready' status signal when the CTS line is 'polled' (i.e., continuously monitored).

Before the software can read the content of the shift registers with the aid of 16 clock pulses on the RTS line, it is necessary to wait 1.5 clock cycles (about 30 µs) for the $\overline{\text{LBEN}}$
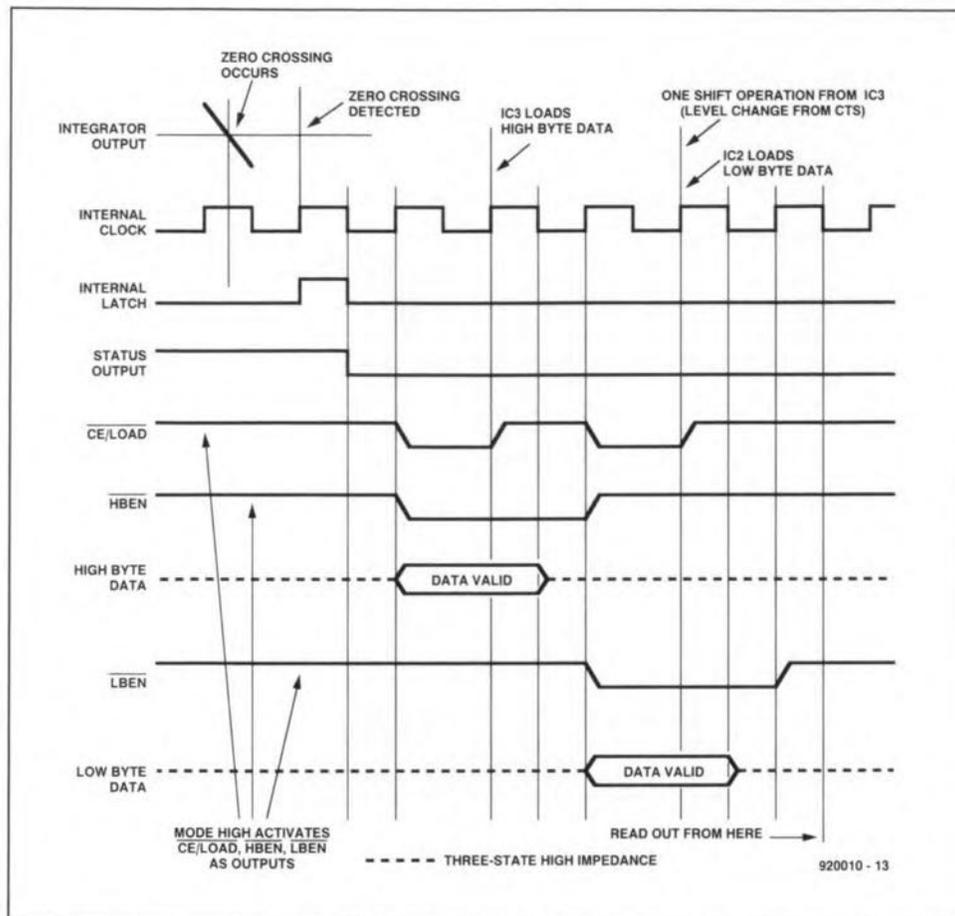
struct ed on separate printed circuit boards. Note that the entire circuit is powered via the RS232 link to the PC.

signal to return to high. This time can be used, for instance, to switch the multiplexer to the right channel.

The function of the bits in the datastream is shown in Table 1. The first clock pulse sets bistable IC5c-IC5d. This causes the RUN input to return to logic high, whereupon the A-D converter starts a new conversion cycle. The bistable is reset by a high level on the status line of IC1 (pin 2). The high level at the

serial input of the low-byte shift register ensures that the output returns to high (–12 V on the CTS line) after the value has been read.

The ICL7109

The ICL7109 is a low-cost 12-bit dual-slope A-D converter with additional polarity and overflow outputs. Figs. 3 and 4 shed light on

the operation of the digital part of the converter. First, Fig. 4: the upper signal represents the voltage at the capacitor (C3; the component numbers in brackets refer to the actual circuit). Below, some signals of the ICL7109, the internal clock, the clock signal of the output latch, the status output and the RUN/Hold input.

The conversion is started when a high level appears at the RUN input. During the

Fig. 3.   Timing diagram of the data and command transfer protocol used.

Table 1. Overview of bit functions in dataword (16 clock pulses)

Clock on RTS	Function
1	Overrun (OR)
2	Polarity (POL)
3	B12
4	B11
5	B10
6	B9
7	High
8	B8
9	B7
10	B6
11	B5
12	B4
13	B3
14	B2
15	B1
16	High

conversion, the status output is held logic high. First, the integrator capacitor (C3) is charged with a current, I_c:

$$I_c = (U_{HI} - U_{LO})/R3.$$

This takes 2,048 internal clock cycles (oscillator frequency divided by 58). Subsequently, C3 is discharged with a constant current, I_d, that is proportional to the input voltage:

$$I_d = U_{ref}/R3.$$

During the discharging, the number of internal clock pulses is counted. The first leading edge of the internal clock that occurs after the capacitor voltage drops below 0 V causes the counter state to be transferred to the output register. Next, the status output changes from high to low, and so indicates the end of the conversion. Thus, we have:

counter state = 2,048 U_{in}/U_{ref}.

If the RUN input remains high during the conversion, a new conversion cycle is started after the auto-zero phase. Conversely, if RUN remains low, the new conversion starts 7 internal clock pulses after a new high level is present.

Figure 3 illustrates the handshaking of the ICL7109 with the external circuits, when the Mode and Sense inputs are held logic high. To the signals shown in Fig. 4 are added $\overline{LOAD}$, $\overline{HBEN}$, $\overline{LBEN}$ and the data lines. A low level on $\overline{HBEN}$ signals the presence at the output of the high byte of the counter state and the status signals Overrun and Polarity. The high byte can be copied on the leading edge of the $\overline{LOAD}$ signal. The subsequent transfer of the low byte is similar.

The input of the ICL7109 may be considered symmetrical within the bounds of the supply voltage, and has an input resistance of the order of a few giga-ohms. To make sure that sufficient charge reserve is available for the switches in the analogue part of the converter, the voltage source to be measured must be buffered by a low-loss capacitor. This means that capacitor C1 must be connected in parallel with the two inputs when measurements are made without the multiplexer. This is achieved by fitting jumper J4. For measurements on symmetrical voltages, the voltages (with reference to ground) at the two inputs must lie within the bounds of the supply voltage of the ICL7109. For asymmetrical measurements, the LO input can be tied to ground by fitting jumper J1. Resistor R1 prevents discharging via the measured voltage source.

More inputs, more channels

A multiplexer is provided for those of you who want to measure more than one voltage source. The multiplexer consists of IC7 for the selection of the Hi line, and IC8 for the se-

Fig. 4.   ICL7109 analaogue-to-digital conversion timing.

```
Uses Crt;

CONST
    PosOver=MaxInt;          { value for pos. overflow }
    NegOver=-MaxInt;         { ditto neg. overflow }

VAR
    SIOAdr:Word;             { to be assigned with 8250 base address }
                             { e.g. COM1: SIOAdr:=$3f8 }
                             {      COM2: SIOAdr:=$2f8 }

{-------------------------------------------------------------------}

{ set channel for next conversion: }

        PROCEDURE SetChannel(Channel:Byte);
CONST
    PulseBytes:ARRAY[1..5] OF Byte=(0,14,51,21,85); { -> 1 - 5 pulses to TX }

        PROCEDURE WaitTx;
BEGIN
    { wait until transmit shift register is free }
    REPEAT UNTIL Port[SIOAdr+5] AND 32<>0;
END;

BEGIN
    IF Channel>5 THEN        { 2 characters required? }
      BEGIN
        WaitTx; Port[SIOAdr]:=PulseBytes[5];
        WaitTx; Port[SIOAdr]:=PulseBytes[Channel-5];
        Waittx;
      END
    ELSE IF Channel>0 THEN { 1 character required? }
      BEGIN
        WaitTx; Port[SIOAdr]:=PulseBytes[Channel];
        WaitTx;
      END
    ELSE;                     { no pulse for Channel 0 }
END;

{Read value from shift registers. Call only when conversion is ready !!}

        FUNCTION ReadAD:Integer;
BEGIN
    Inline(
$8B/$16/>SIOAdr/  {      mov   dx,[SIOAdr]  ; DX at SIO-Port }
$83/$C2/$04/      {      add   dx,4         ; and on ModemCtrl there }
$BE/>0002/        {      mov   si,2         ; to switch address }
$33/$DB/          {      xor   bx,bx        ; clear shift accu }
$B5/$10/          {      mov   ch,16        ; 14 data +2 dummy clocks }
$B1/$04/          {      mov   cl,4         ; shift to CTS }
$EC/              {@read:in   al,dx        ; send pulse via RTS }
$24/$FD/          {      and   al,0fdh      ; RTS high }
$0C/01/           {      or    al,1         ; DTR complementary low }
$EE/              {      out   dx,al        ; set lines }
$51/              {      push  cx           ; short wait loop, }
$B9/>$1F4/        {      mov   cx,500       ; to allow levels }
$E2/$FE/          {      loop  $            ; to settle }
$59/              {      pop   cx           }
$0C/$02/          {      or    al,2         ; and restore }
$24/$FE/          {      and   al,0feh      ; DTR complementary high }
$EE/              {      out   dx,al        ; reset lines }
$51/              {      push  cx           ; ensure }
$B9/>$1F4/        {      mov   cx,500       ; smallest pulse length }
$E2/$FE/          {      loop  $            }
$59/              {      pop   cx           }
$80/$FD/$0A/      {      cmp   ch,10        ; pass dummy after 7 clocks }
$74/$0A/          {      je    @nuse        }
$03/$D6/          {      add   dx,si        ; DX to ModemStatus }
$EC/              {      in    al,dx        ; read status bits }
$D2/$E0/          {      shl   al,cl        ; shift CTS bit into carry }
$F5/              {      cmc                ; observe Inverting }
$D1/$D3/          {      rcl   bx,1         ; shift into result }
$2B/$D6/          {      sub   dx,si        ; DX back to ModemCtrl }
$FE/$CD/          {@nuse:dec   ch           ; outer loop counter }
$75/$D4/          {      jnz   @read        }
$D1/$EB/          {      shr   bx,1         ; shifted once too many }
$80/$F7/$10/      {      xor   bh,10h       ; change sign }
$F6/$C7/$20/      {      test  bh,20h       ; overrun set? }
$75/$0D/          {      jnz   @Over        ; yes--> }
$F6/$C7/$10/      {      test  bh,10h       ; polarity negative? }
$74/$16/          {      jz    @WErg        ; no-->result o.k. }
$80/$F7/$10/      {      xor   bh,10h       ; yes: clear Pol-Flag }
$F7/$DB/          {      neg   bx           ; ..and form 2's complement }
$EB/$0F/$90/      {      jmp   @WErg        }
$F6/$C7/$10/      {@Over:test  bh,10h       ; negative overrun? }
$75/$06/          {      jnz   @ONeg        ; yes--> }
$BB/>PosOver/     {      mov   bx,PosOver   ; constant pos. overflow }
$EB/$04/$90/      {      jmp   @WErg        }
$BB/>NegOver/     {@ONeg:mov   bx,NegOver   ; constant neg. overflow }
$89/$5E/$FE);     {@WErg:mov   @result,bx   ; function result = BX }
END;

{ check if a valid result is available: }

        FUNCTION AD232_Ready:Boolean;
BEGIN
    AD232_Ready:=Port[SIOAdr+6] AND 16<>0;
END;

{ Initialisation of AD232. No timeout; endless loop created when AD232 is not found! }

        PROCEDURE AD232_Init;
VAR
    Dummy:Integer;
BEGIN
    Port[SIOAdr+4]:=2;        { only DTR low }
    Delay(100);               { allow supply voltage to stabilize }

    REPEAT UNTIL AD232_Ready; { wait for first result }
    Delay(1);
    Dummy:=ReadAD;            { discard result }
END;
```

Fig. 5.   A 'bare bones' control program for the converter (Pascal with in-line assembler).

lection of the Lo line. Both are controlled by IC4, which counts the clock pulses on the Tx line. To select a channel, the software puts certain characters on the Tx line, such that the total number of clock pulses corresponds to the desired channel (see the programming example 'setchannel' listed in Fig. 5). The set baud rate is irrelevant, but the (rarely used) parity function must be taken into account. To ensure a fixed starting configuration, the counter is automatically reset to channel 1 after each conversion.

When the multiplexer is used, capacitor C1 must be disconnected from the input (J4 is not fitted), and the ground reference must be raised (J1 is not fitted). Capacitors C24-C31 and C36-C43 then take over the function of C1.

COMPONENTS LIST

Resistors:

17	10MΩ	R1;R24-R39
3	22kΩ	R2;R3;R22
4	100Ω	R4;R5;R9;R14
6	100kΩ	R6;R10;R11;R15;R1*;R19
2	180kΩ	R7;R12
2	390kΩ	R8;R13
1	270kΩ	R17
1	220kΩ	R18
1	68kΩ	R20
1	2kΩ2	R21
1	27kΩ	R23
1	2kΩ multiturn preset	P1
1	1MΩ multiturn preset	P2

Capacitors:

19	100nF	C1;C14;C15;C18-C43
1	1µF	C2
1	220nF	C3
1	330nF	C4
2	4µF7 6V3 tantalum	C5;C6
2	100pF	C7;C9
2	1nF	C8;C10
1	12nF	C11
2	220µF 16V radial	C12;C13
2	47µF 16V radial	C16;C17

Semiconductors:

11	1N4148	D1-D11
1	green LED	D12
1	BF245B	T1
1	BC550C	T2
2	BC560B	T3;T4
1	ICL7109	IC1
2	74HC166	IC2;IC3
1	74HC161	IC4
2	74HC02	IC5
1	LM324	IC6
2	4051	IC7;IC8

Semiconductors:

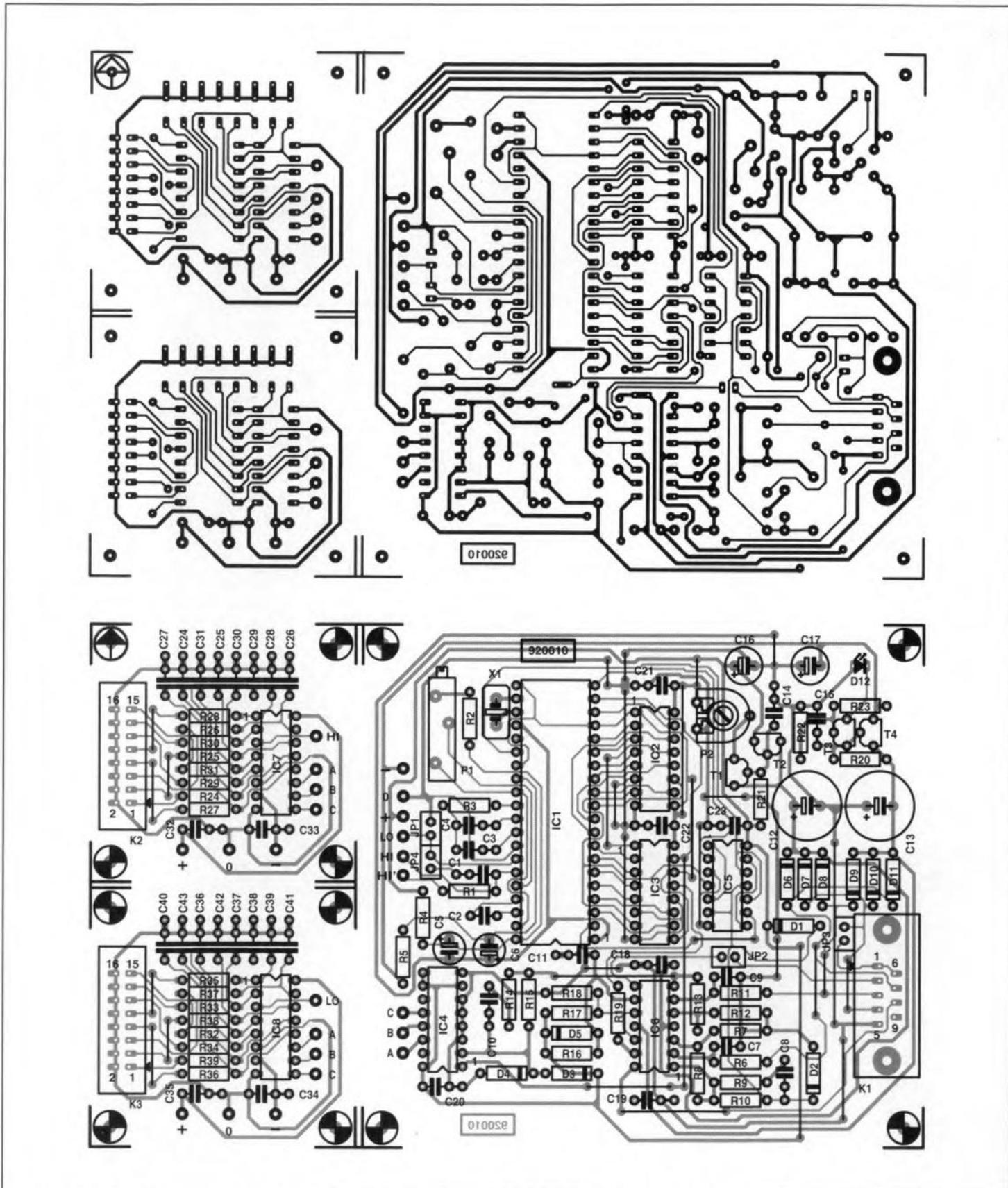|		
1	9-way PCB-mount female sub-D connector	K1
2	16-way pin header	K2;K3
1	3-MHz quartz crystal	X1
1	Printed circuit board	920010
1	Control program on disk	ESS1691

The multiplexers also allow symmetrical measurements to be made within the bounds of the converter's supply voltage. When asymmetrical measurements are performed, the inputs of multiplexer IC9 must be tied to ground, for instance, by fitting jumpers on header K3.

Unfortunately, the 4051 and the high converter input resistance of the converter introduce an offset voltage that differs from channel to channel. Although the asymmetrical construction reduces the effect of the offset to a minimum, it can not be eliminated completely. For very accurate measurements, this means that the multiplexer must either not be used, or replaced by one with better specifications. For 'everyday' use, however, a correction in software of the measured voltage with the aid of a zero calibration is perfectly adequate.

RS232 level changer

The four opamps in IC6 are used as voltage level converters. Actually, they function as inverting switches, and so provide the inverting function defined in the RS232 standard. Diodes D1-D4 and resistors R10 and R15 limit the signal to +5 V and ground. R-C combinations R9-C8 and R14-C10 ensure that the input capacitances formed by IC5 and IC4
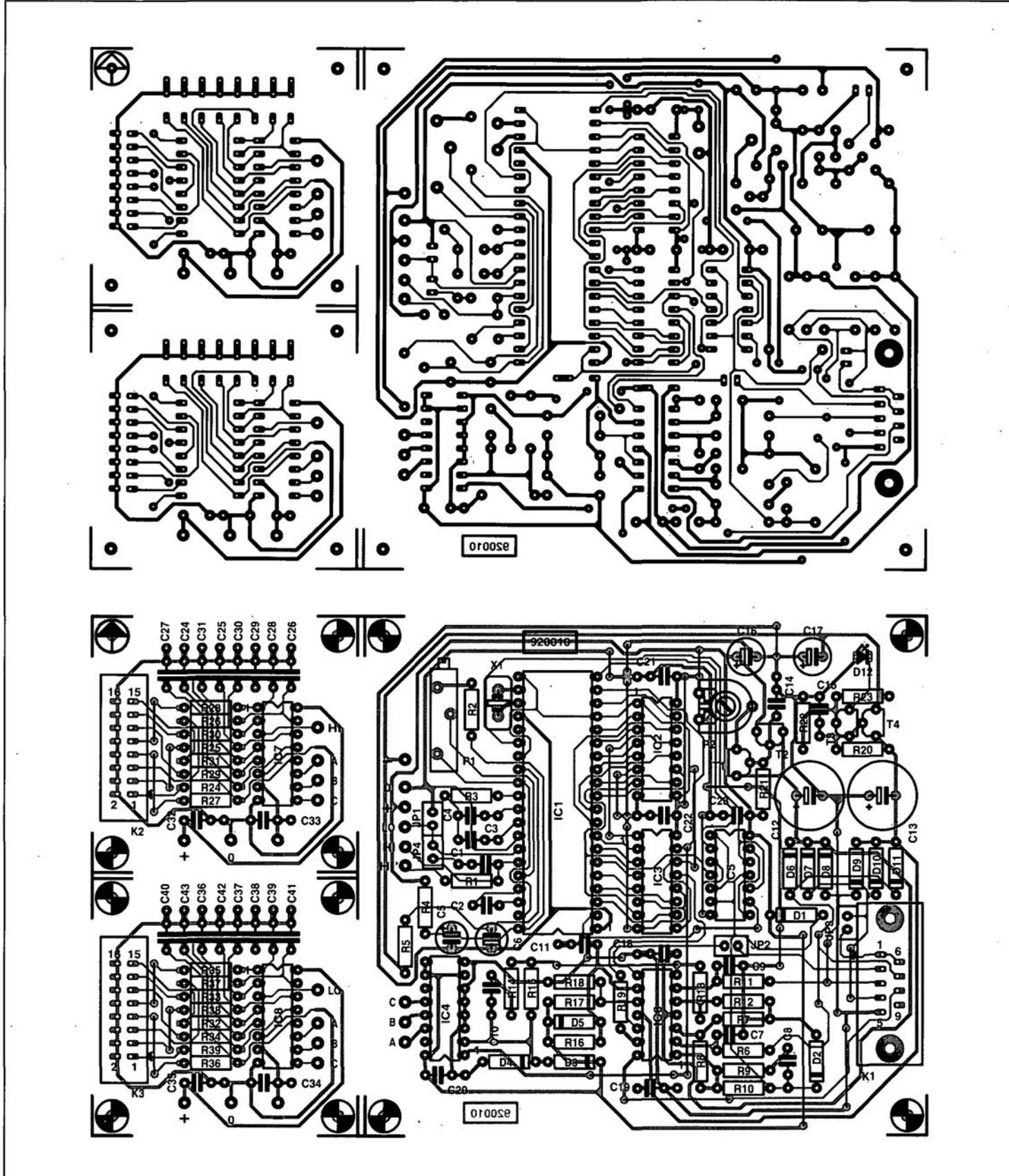

Fig. 6.   Single-sided printed circuit board (track layout and component mounting plan) for the AD232.

```
╔══════════════ AD232-Multimeter ══════════════╗
  (P)rotocol   (D)isplay   (C)onfiguration   (M)iscellaneous   (E)nd
                              ┌─ Config ─┐
  1:-529.4 mV  ▇▇▇▇▇▇▇▇▇│ Channel 1 │▇▇▇
                        │ Channel 2 │
  2:-223.8 mV  ▇│     ══════ help ══════    ════│
               │  Menu config / Channel x :
  3:-215.3  V  ▇│
               │  This menu arranges all settings for
  4:-213.4 mV  ▇│  the displaying of the measurement
               │  values on the selected channel:
  5:-215.2 mV  ▇│
               │   ┌Channel active┐  Unit
  6:-217.7 mV  ▇▇│   Range            Symmetrical
               │   Logarithmic       Hold
  7:-217.6 mV  ▇│   Erase memory      Settle
               F1=index                        PgDn
  8:-216.1 mV  ▇▇▇▇│   lower bound:-409.6m
                   │   upper bound:+409.6m
                   │    adjust offset
                   │    offset manual
╚══════════════════════════════════════════════╝
 F1 HELP  F2 CALC  F3     F4     F5     F6     F7     F8     F9     F10
```

This program is completely menu-driven, runs in colour, accepts mouse as well as keyboard control, and is written to run on IBM PCs and compatibles, from XTs to 486-based machines. A colour video card (EGA or VGA) is not strictly required, although you will miss a lot of the presentation graphics' power when you have monochrome video only.

Installation

The program can be run from floppy disk or hard disk. When it is run from floppy disk, make sure the write protection is removed, because the program writes a configuration file on the disk. An installation proper is not required—simply copy all files to your working disk, or to the hard disk.

Running the program

The AD232 control program is started by typing MULTI from the DOS prompt. First, go the (M)iscellaneous option, and select the serial port to which the AD232 board is connected. On leaving this menu, the voltmeter should work, indicating the voltages on all eight channels by means of horizontal bars and an absolute readout. (see Fig. 7). When fewer than eight channels are used, the screen is automatically enlarged.

Options (configuration menu)

The channel settings are not limited to switching on and off. Measuring ranges, multipliers and units (mV; V, etc.) can be taken into account in the graphics readout. The bar that indicates the magnitude of the measured voltage can be asymmetrical or symmetrical, and linear or logarithmic. Use 'symmetrical' for measured quantities that can go positive and negative. The menu also includes program options for offset calibration and a smoothing (delta) factor to stabilize the display.

Protocol

Apart from being shown on the screen in the form of horizontal bars, the measured values may also be sent to a file or an output device such as a printer. All output is in straight ASCII to a simple protocol, which makes further processing by other software easy.

Extras

All screen elements (text, highlighted text, borders, background) can be displayed in a number of user-selectable colours (VGA/EGA). Irrespective of your whereabouts in the program, a scientific (UPS compatible) desktop calculator and context sensitive help are always to hand. The help texts used in the program are stored in a file called MULTI.HLP, which is generated by adding WINHELP.TXT and MULTI-HLP.TXT on the diskette, as explained in README.DOC. All files and menus are in English. ∎

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need not charge via R10 and R15, and so reduce the effects of the relatively low slew rate of the opamps. Opamp IC6c is not strictly required for the correct function of the circuit. However, fit jumper J2 if you wish to feed the 'end of conversion' signal to your PC via the RxD line (for use with an appropriate interrupt routine).

Power supply

As already mentioned, the AD232 board is powered by the RS232 port of the computer it is connected to. The minimum requirement for this to be achieved is that the PC holds one RS232 line at +12 V and another at –12 V. Since the TxD line is at –12 V when it is not active, the +12 V supply will have to be supplied by the RTS and/or the DTR line. Diodes D6-D11 and capacitors C12 and C13 add and buffer the line levels to provide two discrete regulators with their input voltages. The voltage across the capacitors is also used to power the quadruple opamp. By omitting jumper JP3, the loading of the interface can be made as small as possible, if it can not supply enough current.

The voltage regulators in the ±5 V supply are low-drop, high efficiency, types built from discrete components. The negative regulator consists of a pseudo-zener diode with a series transistor formed by T3 and a green LED, D12. Adjustment of the negative output voltage is not necessary because the A-D converter has a fairly large negative voltage range. Not so with the positive supply, where the pinch-off voltage of a FET serves as the reference. Although this voltage is reasonably stable, it has a fairly high device tolerance, and needs to be adjusted with the aid of P2. To save on parts, protection against overvoltage as a result of an incorrect adjustment is not provided. This means that the wiper of P2 must be turned to ground before calibrating the AD232 board.

The +5-V voltage must be adjusted with the nominal load connected.

Construction and adjustment

The single-sided PCB designed for the circuit is shown in Fig. 6. The construction will be mostly plain sailing. The multiplexers are built as separate units, and connected to the ADC proper in accordance with the component overlay. The HI' input serves for initial tests without the multiplexer. It is important to ensure adequate screening of all signal lines—remember, the high input resistance makes the circuit sensitive to noise. Hum suppression will be optimum when a quartz crystal of 2.969600 MHz is used. Unfortunately, this is not a standard frequency, whence the use of a 3-MHz crystal here.

The adjustment of the ADC by P1 depends on the application. In principle, the fine adjustment can be done by programming. The external circuitry around the ADC is designed for a maximum input voltage of about 400 mV. For other voltages, R3 must be changed:

$$R_3 = U_{max}/20 \ \mu A.$$

The reference voltage, U_{ref}, should be a little higher than $U_{max}/2$, because the converter produces an overflow when $U_{max} \geq 2U_{ref}$.

Connect the AD232 board to the PC, and advance preset P2 slowly until the positive regulator supplies +5 V.

The software package

Although the routines listed in Fig. 5 can be expanded into a full-blown control program for the AD232 board, you will be pleased to know that such a program is available on a disk supplied that can be ordered through our Readers Services (order code 1691).

The multiplexers also allow symmetrical measurements to be made within the bounds of the converter's supply voltage. When asymmetrical measurements are performed, the inputs of multiplexer IC9 must be tied to ground, for instance, by fitting jumpers on header K3.

Unfortunately, the 4051 and the high converter input resistance of the converter introduce an offset voltage that differs from channel to channel. Although the asymmetrical construction reduces the effect of the offset to a minimum, it can not be eliminated completely. For very accurate measurements, this means that the multiplexer must either not be used, or replaced by one with better specifications. For 'everyday' use, however, a correction in software of the measured voltage with the aid of a zero calibration is perfectly adequate.

RS232 level changer

The four opamps in IC6 are used as voltage level converters. Actually, they function as inverting switches, and so provide the inverting function defined in the RS232 standard. Diodes D1-D4 and resistors R10 and R15 limit the signal to +5 V and ground. R-C combinations R9-C8 and R14-C10 ensure that the input capacitances formed by IC5 and IC4

Fig. 6.   Single-sided printed circuit board (track layout and component mounting plan) for the AD232.

GENERIC ARRAY LOGIC (GAL)

based on an original article by D. Gembris

In the development of Programmable Array Logic (PAL) devices, the design target was to make available to the user/designer as many 'free' logic gates on the device as possible. Lattice Semiconductor Corporation has further developed the device into the Generic Array Logic—GAL. In essence, both devices are electrically erasable CMOS memory ICs that provide the user with re-configurable logic and bipolar performance. This makes the GAL suitable for a wide variety of applications. Note that a PAL IC can be programmed only once, whereas a GAL IC can be programmed time and again. This makes the use of GAL ICs much more cost effective than PAL ICs.

The internal design of GALs is practically identical to that of PALs: both devices have a large programmable AND matrix to which a number of fixed OR gates may be connected. The connections between the AND and OR gates are made in silicon. In contrast, a PROM (Programmable Read Only Memory) has a fixed AND matrix and programmable OR gates.

The design

The availability of EEPROM (Electrically Erasable Read Only Memory) ICs was of fundamental importance in the development of GAL ICs. Apart from being erasable and re-programmable, the GAL ICs from Lattice are guaranteed for a minimum of 100 erasure/write cycles with data retention up to 20 years.

To further make the user's life easy, GAL ICs have provision for an individual 'signature' of up to eight bytes. This may be used, for instance, to give the device a specific code.

Like PAL devices, GAL ICs can be protected against unwanted reading by actuating a specific cell (through the software). It must be said, however, that this protection is much more effective in PAL than in GAL devices. This is because the fusing of a link in a PAL IC is permanent, whereas in a GAL IC it can be erased, after which the device can be reprogrammed or read.

The logic diagram of a Type 16V8 GAL IC is shown in Fig. 1 and that of a Type 20V8 in Fig. 2. Each type has 8 programmable output logic macrocells (OLMCs) that allow the user to configure each output as desired. The figures in the type numbers refer to the design: the first, 16 or 20, is the number of inputs, and the second, the number of outputs.

The following data refer to the 16V8 (see Fig. 1). The eight inputs (pins 2–9) are available at the AND matrix in either original or inverted form and thus give rise to 16 columns. The other 16 columns are connected to the outputs, which are also inverted or non-inverted. There are thus a total of 32 signals available.

When the IC is erased, there is no contact between the 64 rows (eight OR-gated rows per output) and the 32 columns. Therefore, changes at the inputs have no effect on the outputs. Only when programming is begun will the connections be restored. Each connection represents an AND gate.

Output Logic Macro Cells

The key to the universality of GAL ICs lies in the *output logic macro cells* (OLMCs). The design of such a cell is shown in Fig. 3. The distinct configuration of an OLMC is laid down in an *Architecture Control Word* (see Fig. 10). Bits SYN, AC0 and AC1(n) determine the status of the output of the cell. The SYN and AC0 bits take effect on all outputs

simultaneously, but the AC1(n) bit can be set for each output individually. Because of this, only two of the four possible configurations can be realized in a GAL IC at the same time as shown below.

Normal output—SYN=1; AC0=0; AC1(n)=0 (Fig. 4).

Three-state output with disable via a product term and output return. Of the eight rows, only the lower seven are OR-gated, while the eighth determines whether the result will be shown at the output or not. SYN=0 or 1; AC0=1; AC1(n)=1 (Fig. 5).

Three-state output with disable, output return and register. The result will be at the output only when a clock pulse is applied to pin 1
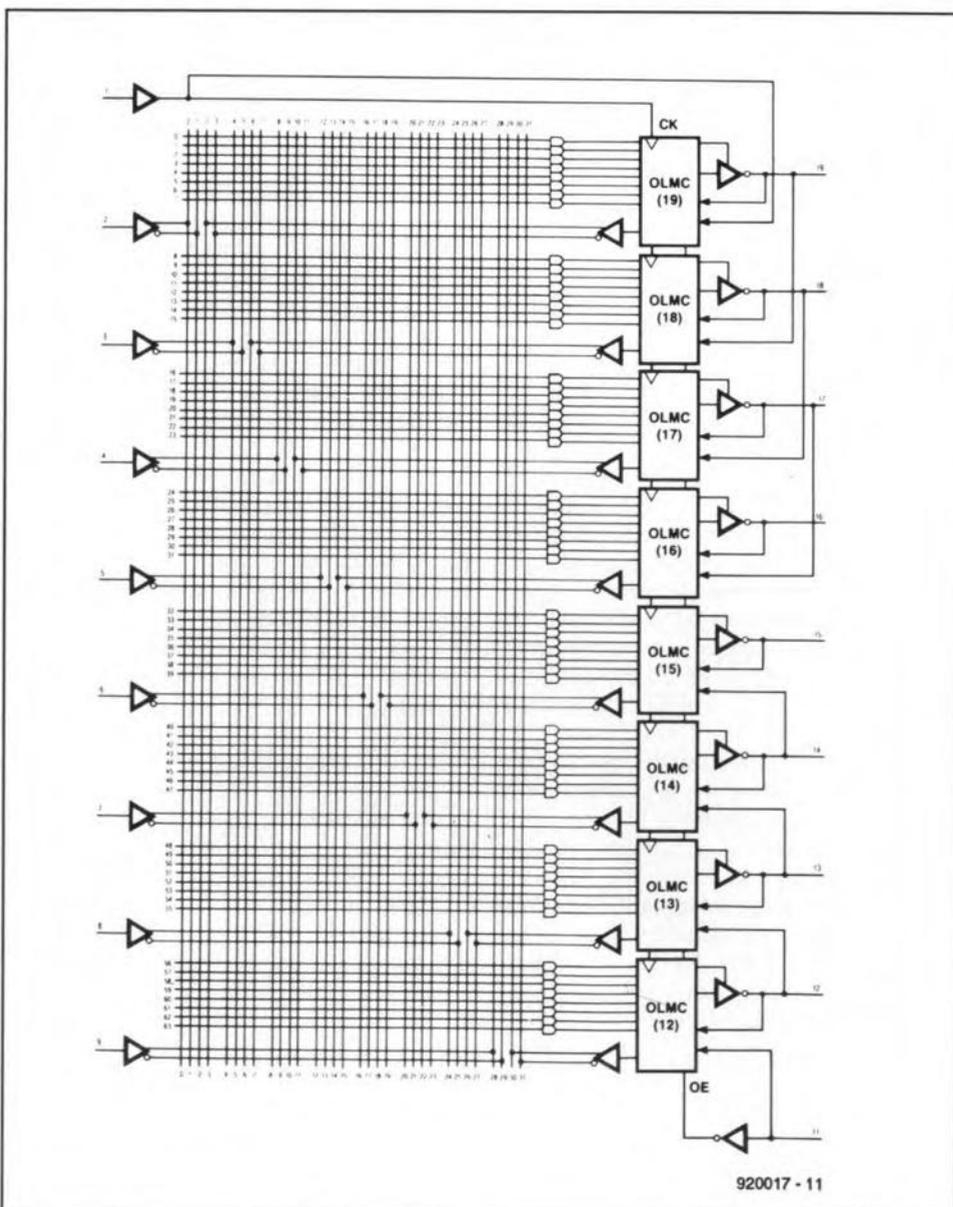
Fig. 1. Logic diagram of the 16V8 GAL IC.

Fig. 2. Logic diagram of the 20V8 GAL IC.

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Fig. 3. Output Logic Macro Cell of 16V8 GAL IC.

(CLK) and pin 11 is low. SYN=0; AC0=1; AC1(n)=0 (Fig. 6). There are two possible versions of this output (see Fig. 7)

Input: SYN=1; AC0=0; AC1(n)=1 (Fig. 8).

Programming

Apart from the supply line connections, each pin of a GAL IC has two different functions. Which function is active depends on whether the IC is being programmed (Edit mode) or operates in normal mode. The pin functions of both the 16V8 and the 20V8 are shown in Fig. 9: the inner ones give the Edit mode functions and the outer ones, the normal operating functions. In the Edit mode, which is set by applying 16.5 V DC to pin 2, the IC can be read, programmed or erased.

A GAL IC is internally divided into 64 rows, as shown in the row address map in Fig. 10. There are 36 unique row addresses available to the user when programming the device

Row addresses 0–31 each contain 64 bits of input term data. This is the user array where the custom logic pattern is programmed. Row 32 is the electronic signature word. It has 64 bits available for any user-defined purpose.

Rows 33–59 are reserved by the manufacturer and are not available to the user.

Row 60 contains the architecture and output polarity information. The 82 bits within this word are programmed to configure the device for a specific application—see Fig. 11.

When row 61 (security cell, see Fig. 10) is programmed, the enabling array is disabled, preventing further programming or verification of the array.

When row 63 is addressed during a programming cycle, the entire array and the architecture programming word are erased.

The outputs of the AND array are fed into an OLMC, where each output can be set individually to active high or active low with combination (asynchronous) or registered (synchronous) configurations respectively. A common output enable can be connected to all outputs, or separate inputs or product terms can be used to provide individual output enable controls.

The various configurations of the OLMC are controlled by programming cells SYN, AC0, AC1(n) and the XOR(n) polarity bits within the 82-bit architecture control word (see Fig. 10).

The SYN bit determines whether or not a device will have registered output capability or will have purely combinational outputs. It also replaces the AC0 bit in the two outermost macro cells, OLMC(12) and OLMC(19).

Architecture control bit AC0 and the eight AC1(n) bits direct the outputs to be wired always on, always off (as an input), have common OE control (pin 11), or to be three-state controlled separately from a product term. The architecture control bits also determine the source of the array feedback term through the FMUX, and select either combinational or registered outputs.
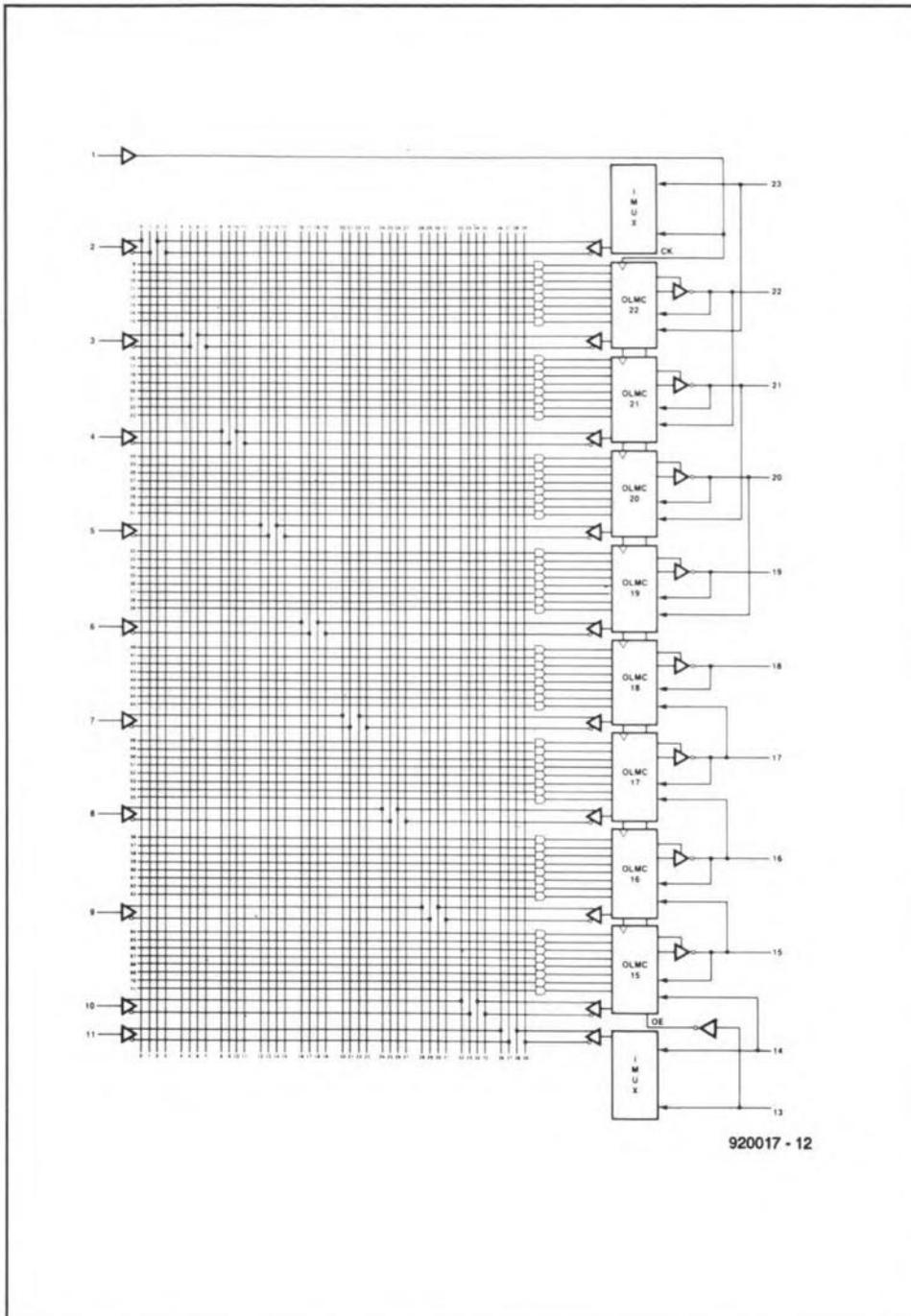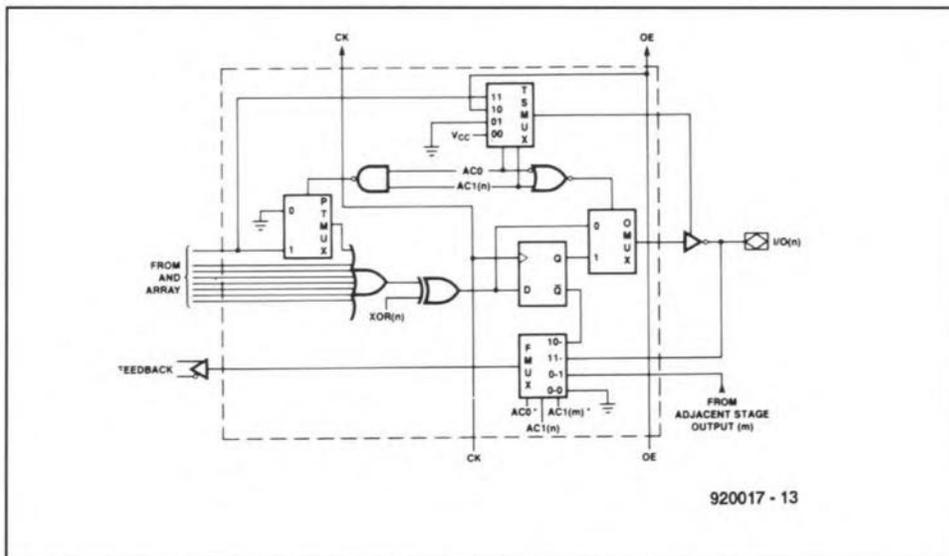
The five valid macro cell configurations are shown in Fig. 4–8. In all cases, the eight XOR(n) bits individually determine each output's polarity. The truth table associated with each figure shows the bit values of the SYN, AC0 and AC1(n) that set the macro cell to the configuration shown.

If a product term is allocated a 0, it is ignored during the OR gating. The product term censures PAL compatibility, even with older PALs that have fewer than 64 product terms. PAL listings are transformed into GAL listings.

The rows are addressed by means of an internal shift register. The transfer protocol is

Pin P/N̄: 1 = writing; 0 = reading.
RAGO-5: row selection.
STR̄, SCLK, SDOUT:
reading – the shift register is loaded with an STR̄ pulse and the data are read by a clock SCLK at SDOUT;
writing – the data at SDOUT are clocked into the shift register with SCLK, whereupon the selected row is written into with a 10 ms STR̄ pulse.
Jump to RAGO-5 as long as no registers are being read or written to.

Compared with that of PALs, this protocol is trivial. This is one of the reasons that GALs have become inexpensive and this in turn has contributed to the wide use of these devices. Of late, some other manufacturers have also entered the GAL market, particularly SGS-Thomson and AMD. The latter bring out their GAL ICs under the name PALCE.

Row address map description

Details of the various row addresses are given below.

Electronic signature word
An electronic signature word is provided with every GAL 16V8 chip. It resides at row 32 and contains 64 bits of reprogrammable memory that can contain user-defined data. The signature data is always available to the user independent of the state of the security cell.

Architecture control word
All of the various configurations of the GAL 16V8 ICs are controlled by programming cells within the 82-bit architecture control word that resides at row 60. The location of specific bits within the architecture control word is shown in Fig. 10. The function of the SYN, AC0 and AC1(n) bits have already been explained. The eight polarity bits determine each output's polarity individually by selectively correct logic. The numbers below the XOR(n) and AC1(n) bits in the architecture control word diagram show the output device pin number that the polarity bits control.

Security cell
Row address 61 contains the security cell (one bit). This cell is provided on all GAL 16V8 devices as a deterrent against unauthorized

SYN	AC0	AC1(n)	FUNCTION
1	0	0	ALL OUTPUTS COMBINATIONAL (i.e. 10L8, 12H6)

IN THIS ARCHITECTURE MODE,
PINS 1 AND 11 ARE DATA INPUTS.
ALL OUTPUTS ARE COMBINATIONAL AND ALWAYS ACTIVE.

XOR(n)	OUTPUT POLARITY
0	ACTIVE LOW
1	ACTIVE HIGH

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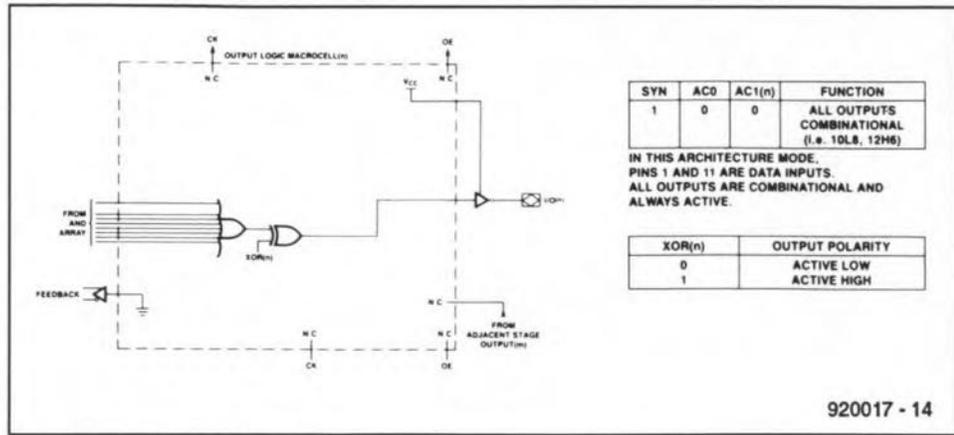
Fig. 4. Dedicated combinational output.

SYN	AC0	AC1(n)	FUNCTION
1	1	1	ALL OUTPUTS COMBINATIONAL (i.e. 16L8, 16H8)

IN THIS ARCHITECTURE MODE,
PINS 1 AND 11 ARE DATA INPUTS.
ALL OUTPUTS ARE COMBINATIONAL.

XOR(n)	OUTPUT POLARITY
0	ACTIVE LOW
1	ACTIVE HIGH

920017 - 15a

Fig. 5. Combinational output.

SYN	AC0	AC1(n)	FUNCTION
0	1	1	COMBINATIONAL OUTPUT IN A REGISTERED DEVICE

IN THIS ARCHITECTURE MODE,
PIN 1 = CK, PIN 11 = OE. THIS MACROCELL IS COMBINATIONAL, BUT AT LEAST ONE OF THE OTHERS IS REGISTERED OUTPUT.

XOR(n)	OUTPUT POLARITY
0	ACTIVE LOW
1	ACTIVE HIGH

920017 - 15b

Fig. 6. Combinational output in a registered device.

SYN	AC0	AC1(n)	FUNCTION
0	1	0	OUTPUT REGISTERED (i.e. 16R8)

IN THIS ARCHITECTURE MODE,
PIN 1 = CK, PIN 11 = OE.

XOR(n)	OUTPUT POLARITY
0	ACTIVE LOW
1	ACTIVE HIGH

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Fig. 7. Registered active high or low output.
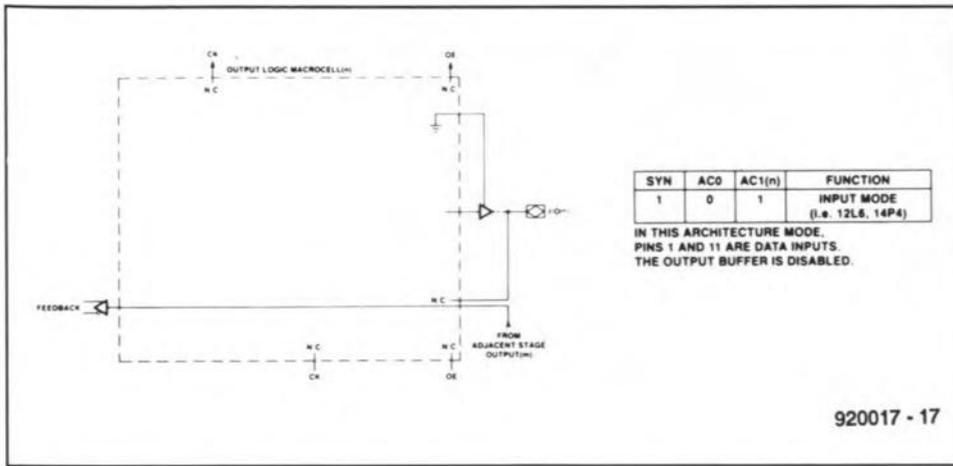
Fig. 8. Dedicated input mode.

SYN	AC0	AC1(n)	FUNCTION
1	0	1	INPUT MODE (i.e. 12L6, 14P4)

IN THIS ARCHITECTURE MODE,
PINS 1 AND 11 ARE DATA INPUTS.
THE OUTPUT BUFFER IS DISABLED.

920017 - 17
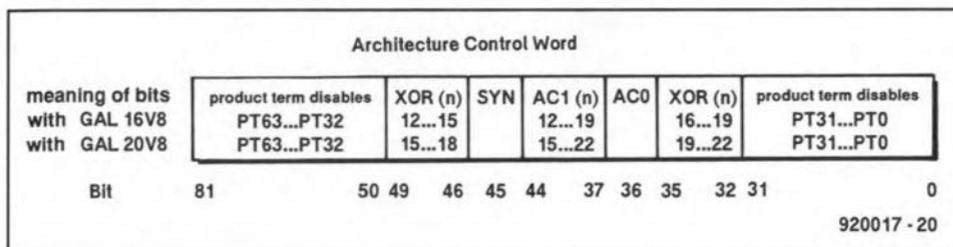
copying of the array configuration patterns. Once programmed, the circuitry enabling array access is disabled, preventing further programming or verification of the array (rows 0–31). The cell can be erased only in conjunction with the array during a bulk erase cycle, so the original configuration can never be examined once this cell is programmed. Signature data is *always* available to the user.

Bulk erase mode
By addressing row 63 during a programming cycle, a clear function performs a bulk eras of the array and the architecture word. In addition, the electronic signature word and the security cell are erased. This mode resets a previously configured device back to its virgin state.

References

GAL Data Book, Lattice Semiconductor Corporation, 1988.

'Field programmable Logic Arrays', *Elektor Electronics*, October 1988, p. 41.

'Programmable array logic', *Elektor Electronics*, May 1985, p. 52.

Fig. 9. Pinout of the 16V8 and 20V8 – see text for symbol identification.

Fig. 10. Row address map block diagram.

Architecture Control Word

meaning of bits	product term disables	XOR (n)	SYN	AC1 (n)	AC0	XOR (n)	product term disables
with GAL 16V8	PT63...PT32	12...15		12...19		16...19	PT31...PT0
with GAL 20V8	PT63...PT32	15...18		15...22		19...22	PT31...PT0
Bit	81	50 49 46	45 44	37 36	35 32	31	0

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Fig. 11. Architecture control word diagram.

INTERMEDIATE PROJECT

A series of projects for the not-so-experienced constructor. Although each article will describe in detail the operation, use, construction and, where relevant, the underlying theory of the project, constructors will, none the less, require an elementary knowledge of electronic engineering. Each project in the series will be based on inexpensive and commonly available parts.

AUTOMATIC NICAD BATTERY CHARGER

Although it is bound to be replaced within a foreseeable period by environmentally safer types, the nickel-cadmium (NiCd) battery is still the most popular around when it comes to powering anything that is portable and electronic. This article describes a low-cost charger that gives the best possible protection to your NiCd batteries by incorporating a timer and two constant current sources.

by L. Pijpers

ONE of the most common causes of 'early death' of a NiCd battery is wrong charging. Both the charging time and the charging current are critical, and often not observed in inexpensive chargers, which appear to work all right when used with new NiCd batteries. In the long run, however, the batteries seem to lose power, and suddenly, often within days, give up the ghost. On investigating such chargers, they often have a current source with poor regulation characteristics. It also happens that they lack a timer, in which case you (the user) are to blame for forgetting to turn the charger off after the recommended charging time.

The present charger is fully automatic in that it provides a current sources that can be geared to the battery type, and a fairly accurate timer offering three charge periods with automatic switch-off. Both provisions serve to prevent any risk of overcharging.

Practical realisation

The circuit diagram, Fig. 1, shows that the charger consists of three parts: a power supply, a clock circuit, and two current sources. Two identical current sources are used to enable the charger to charge up to 12 batteries at the same time.

The power supply is as simple as it could be. The circuit is powered by a mains adapter with a direct output voltage of about 15 V. This voltage is fed directly to the two current sources. A voltage regulator, IC3, supplies a regulated supply voltage of 10 V for the clock (timer) circuit.
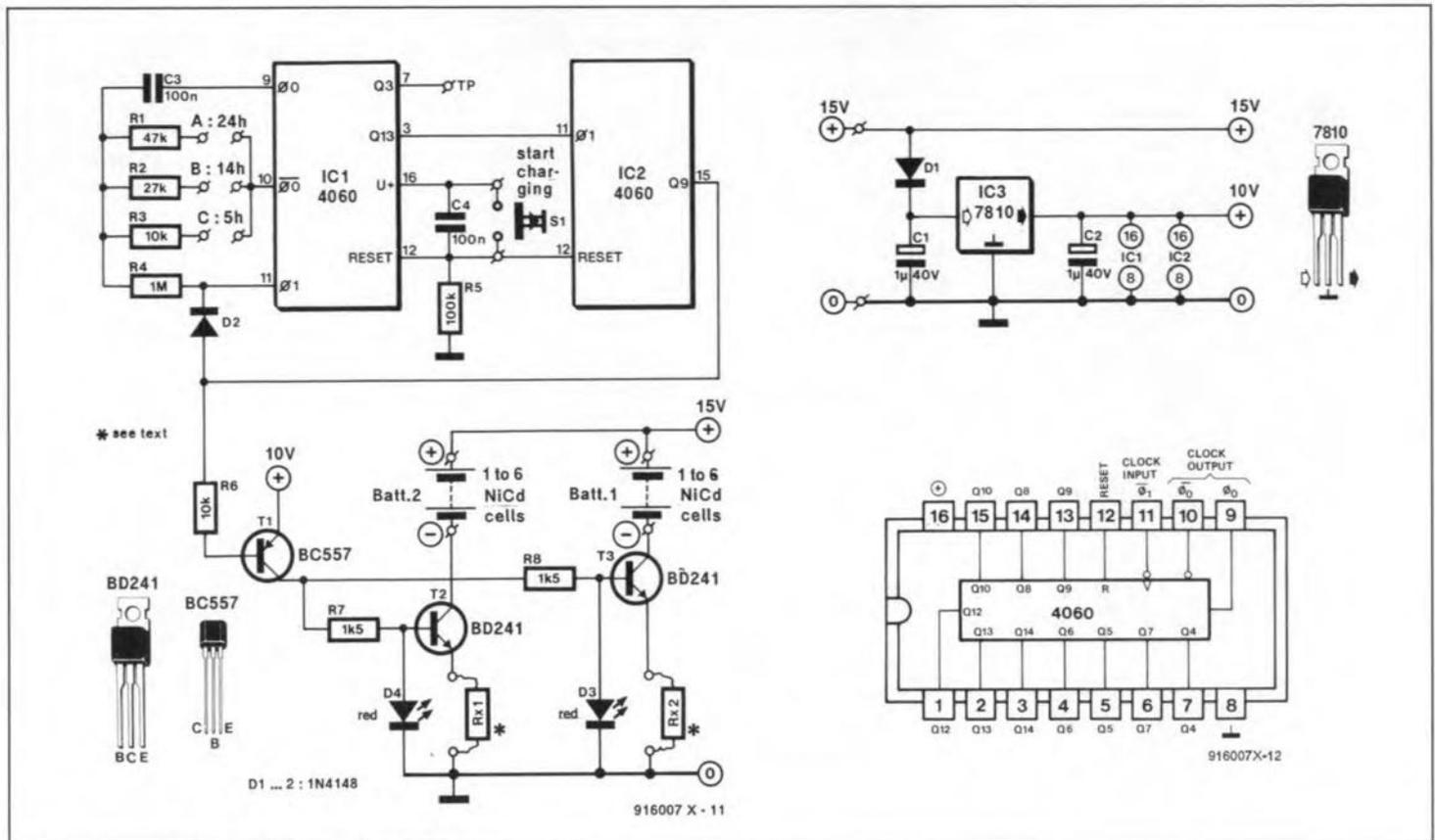
Fig. 1.   Circuit diagram of the NiCd charger.

The clock circuit is formed by two ICs Type CD4060. As shown insert in the circuit diagram, the 4060 contains an oscillator and a 14-stage ripple counter, which is essentially a chain of 14 bistables, each of which divides by two. The oscillator section on board the CD4060 is only used with IC1. Capacitor C3 and resistors R1-R4 are external parts required to make the oscillator operate. The components that determine the oscillator frequency are C3 and the resistor connected to pin 10 of the CD4060. The circuit diagram shows that we have a choice of three oscillator frequencies, which, after dividing, result in an equal number of charging times.

If you would calculate the CD4060 oscillator frequency on the basis of the component values given, you may wonder why this is so high. Could it not be made lower, so that fewer dividers are required for the same charging time? The answer is negative, because a low-frequency oscillator based on the CD4060 is far less stable than a high-frequency one. This is mainly owing to the loss of the timing capacitor (C3), which would

take rather unwieldy values were the oscillator designed to work at a low frequency (say, 10 Hz). Also, low-loss large value capacitors are expensive and difficult to obtain. Briefly, an extra CD4060 solves this problem elegantly, and will not cause too large a hole in your pocket.

Given the oscillator frequency, a total of 24 dividers is necessary to arrive at the three possible charging periods of 24 hours, 14 hours and 5 hours. The total divide factor is, therefore, 2^{24}. Since a CD4060 contains only 14 dividers, two of these ICs are used here, the 'slowest' output of the first IC1) being connected to the clock input of the second (IC2).

To make sure that the charging process stops after the predetermined time, output Q9 of IC2 is connected to the clock input of IC1 via diode D2. When output Q9 of IC2 goes high (after 2^{24} oscillator periods), the oscillator is disabled, which causes the current state of all dividers to be 'frozen' until pushbutton S1 is pressed.

When S1 is pressed, the reset inputs of the two ICs are taken logic high, which resets all

dividers to zero. Evidently, since we do not want to start at an undefined time in the charging period, IC1 and IC2 must be reset also, when the charger is first switched on. The power-on reset circuit is formed by capacitor C5 and resistor R5. During the charging time of the capacitor, the reset inputs of the CD4060s are held high briefly after switching the unit on. This ensures that the clock always starts to count from zero.

The current sources

The moment the clock is reset, output Q9 of IC2 goes low to signal that the batteries may be supplied with their charge current. This signal is processed via transistor T1. Since the Q9 output is 'low', a base current is allowed to flow. Consequently, the collector of T1 will swing to a level virtually equal to the emitter voltage (approx. 10 V). This voltage enables a current to flow through the LEDs via R7 and R8. At the same time, a part of the current is sent into the base of the transistors connected in parallel with the LEDs. The resulting emitter current supplied by T2 and T3 is the charge current for the battery. Actually, the charge current is the sum of the (small) base current and the emitter current. The value of the emitter current depends on the value of Rx1 or Rx2 and the threshold voltage of a red LED.

Referring to the circuit around T2, the base of the transistor is held at a fixed voltage of about 1.6 V. The base-emitter junction of the transistor then acts as a conducting diode, and it is readily seen that the emitter will be at about 1.0 V (1.6 V–0.6 V). This value is fixed because it is derived from the forward drop across diodes, and therefore

Table 1.   Dimensioning the current sources in accordance with the battery type and the charging period.

	Normal (14 hours) and long (24 hours)		Fast (5 hours)	
Penlight	45 mA	22Ω/0.25W	147 mA	6.8Ω/0.25W
Baby	179 mA	5.6Ω/1W	455 mA	1.8W/1W
Mono	370 mA	2.2Ω/1W	1 A	1Ω/3W *
9-V PP3	10 mA	100Ω/0.25W	30 mA	33Ω/0.25W
* or 2 × 2.2Ω/1W in parallel				
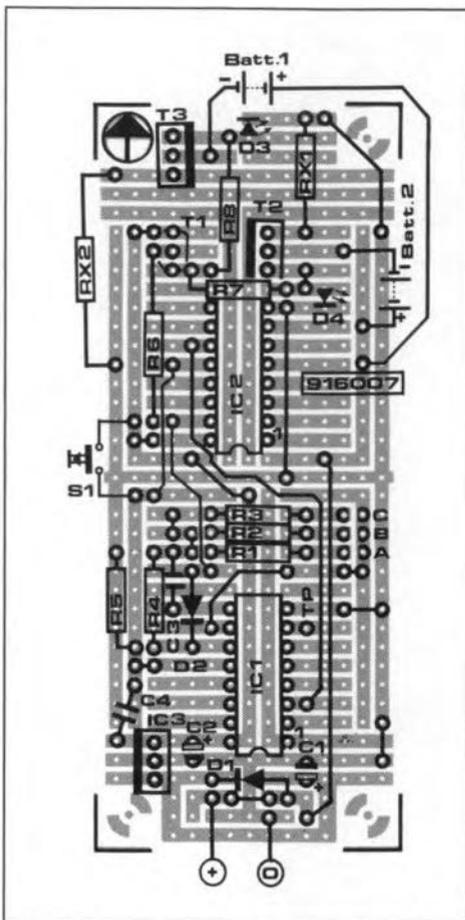
Fig. 2. Suggested component layout on UPBS-1.

COMPONENTS LIST

Resistors:

1	47kΩ	R1
1	27kΩ	R2
2	10Ω	R3;R6
1	1MΩ	R4
1	100kΩ	R5
2	1kΩ25	R7;R8

Rx1;Rx2: see Table 1

Capacitors:

2	1µF 40V radial	C1;C2
2	100nF	C3;C4

Semiconductors:

2	1N4148	D1;D2
2	red LED	D3;D4
1	BC557B	T1
2	BD241	T2;T3
2	CD4060	IC1;IC2
1	7810	IC3

Miscellaneous:

1	SPST push-button	S1
1	Printed circuit board	UPBS-1
1	Mains adapter 15V DC out	

causes a fixed voltage across Rx1. This, in turn, results in a constant current. The charge current is supplied by the transistor, and the current through the base-emitter junction gives rise to a collector current whose value causes a voltage drop of 1 V across Rx1 (again, to be precise, the voltage across Rx1 is the result of the base current and the emitter current).

Should the current through Rx1 become larger (for whatever reason), the voltage across this resistor rises, and so reduces the base-emitter voltage. This can only happen when the base current, and with it the collector current, is reduced accordingly.

From the above it can be deduced that the value of resistor Rx is calculated from

$$Rx = 1\ V/I_{charge}.$$

As indicated in the circuit diagram, the maximum number of 1.5-V NiCd batteries that can be charged simultaneously via one current source is six. More is not possible because the total battery voltage would then be so high that the current sources become unstable (remember, the input supply voltage is about 15 V). For instance, when 9 batteries are connected in series, they supply more than 13 V, to which must be added the voltage across Rx. This gives a total of more than 14 V, leaving only 1 V for the collector-emitter junction of the series transistor. This is a value that can not be achieved or guaranteed even when the transistor is driven with the maximum base current. Hence, the current source will fail, and the output current drop.

A useful feature of the charger is that the LEDs go out when the battery is disconnected. This happens because the collector current is then interrupted, leaving only the base current to flow through Rx1. This causes a voltage drop that is much smaller than 1 V, so that the base voltage drops below the minimum level at which the LED lights.

Charge current and time

As already mentioned, resistors Rx allow us to determine the charge current, while the charge period is selected by connecting the appropriate resistor to pin 10 of IC1.

If you have a set of brand new batteries, it is best to give them an initial charge period of 24 hours (connect point A to pin 10). When the batteries have been used for some time, the charge period is reduced to 'normal', or 14 hours (B to pin 10). The 5-hour period (C to pin 10) is used only if the battery type is suitable for fast charging.

The recommended charge current depends on the type of battery, and is often printed on it. The associated values of Rx are listed in Table 1 for 'long', 'normal' and 'fast' charging. Note that fast charging is not possible with all batteries; when in doubt see the battery specifications, or ask your supplier.

Soldering and testing

The NiCd charger is not difficult to build. Figure 2 shows a suggested components arrangement on universal prototyping board size '1' (UPBS-1), which is available ready-made through our Readers Services. Start the construction by fitting the wire links. Use insulated wire for the longer ones, and uninsulated wire for the shorter ones. Proceed with fitting the IC sockets, the resistors and the capacitors. The semiconductors are mounted last. Make sure you mount the diodes and the transistors the right way around. Lastly, insert the ICs into their sockets, also observing the orientation.

After a close inspection of your solder work, the completed circuit is ready for testing. First, check the current sources. Connect a battery pack in series with an ammeter. The LED in the current source used should light. Check this on the other source also. Measure the current, and check it against the relevant value from Table 1.

Next, check the operation of the timer. Temporarily move the wire to pin 3 of IC1 to the test point marked 'TP'. This shortens the charge period by a factor 1,024, so that the original charging periods of 24 hours, 14 hours and 5 hours are reduced to 84 seconds, 49 seconds and 18 seconds respectively, which are easily checked with a watch. If they are correct, return the wire link to its original position.

The charger may be built into a suitable plastic enclosure. A rotary switch may be worthwhile if the current selection (value of Rx) needs to be changed often. Similarly, a switch may be used to select between the three charging periods. ∎
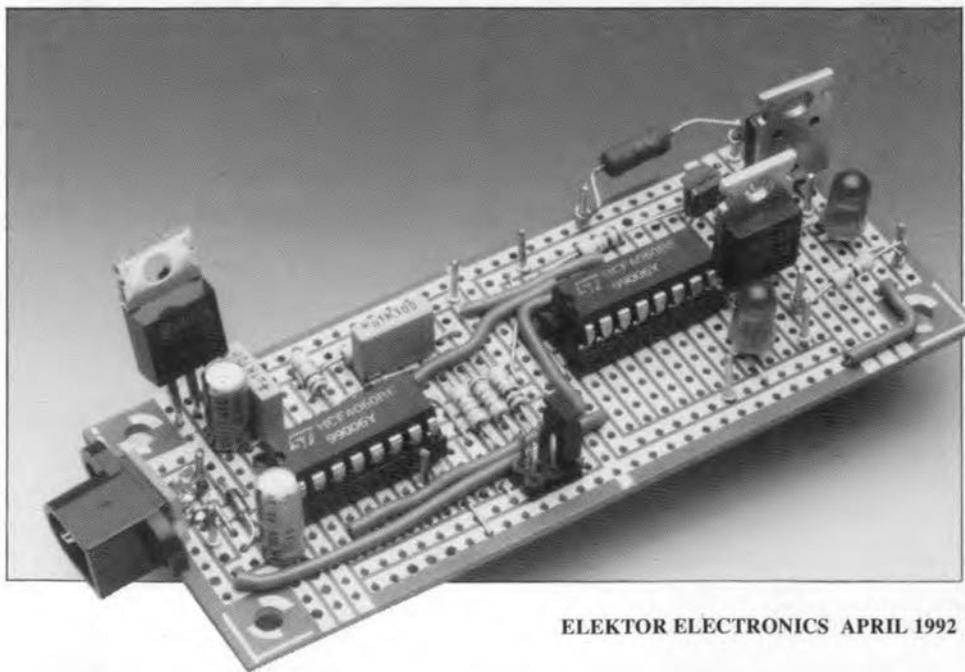
SCIENCE & TECHNOLOGY

UNDERSTANDING WAVEFORM HARMONICS

by Dr K. A. Nigim

Many is the time when a strange, unexpected or distorted waveform appears on your oscilloscope screen. A lot of head scratching and book searching s usually needed to solve the mystery. However, these days, with the rapid advances in Computer Aided Engineering (CAE) software, only a few steps or drag and click with the mouse attached to the computer are required to give you the answer instantly.

Among the easy electronic circuit analyser software available at moderate cost and not too complex is the Micro-cap III electronic circuit package (about £120 or $200 student version). The program is exceptionally easy to operate in entering the electrical/electronic circuit into the PC (AT with math coprocessor advised). Simulation is performed on the circuit with realistic results. A feature included in the package is Fourier Analysis, which evaluates the discrete Fourier transform of many distorted waveforms.

It is not the aim of this article to focus on the software, but rather use its programming facility to demonstrate and simplify the theory behind waveform harmonic content.

Background

Fourier analysis is the mathematical ground for analysing the periodic or repetitive (and perhaps distorted) waveforms. Fourier theory simply breaks the waveform into several ideal sinusoidal waves that each has its own period and amplitude.

Consider the waveform shown in Fig. 1a. It is said to consist of the two ideal waves shown in Fig. 1b. The first large wave is called the fundamental component and has an amplitude of, say, 100% at a frequency of 50 Hz. The second, smaller, wave is called the third harmonic with an amplitude of 30% at a frequency of 150 Hz.

In general, any periodical or repetitive waveform is defined by:

repetitive wave = DC component (A_0) + fundamental component (F_f) + harmonics (E_3)

In Fig. 1, the waveform is represented mathematically by:

$$e_r = A_0 + A_1\sin\omega t + A_3\sin 3\omega t.$$

If $A_3 = \frac{1}{3} A_1$, the distorted wave is said to have 30% third harmonic.

Mathematically, any periodical wave can be represented in the form:

$$Y(\omega t) = A_0 + A_1\sin(\omega t) + A_2\sin(2\omega t) + \dots$$
$$+ A_n\sin(n\omega t) + B_1\cos(\omega t) + B_2\cos(2\omega t) + \dots$$
$$+ B_n\cos(n\omega t),$$

where

A_0 is the direct (constant) component;
$A_1 \dots A_n$ is the fundamental and odd harmonic components;
$B_1 \dots B_n$ is the fundamental and even harmonic components.

Odd components exist when the wave is shaped by identical positive and negative cycles, that is, symmetrical around its axes. Even components occur when the wave is shaped by non-symmetrical half cycles.

Many CAE software packages present the wave by its vector form, which is then plotted in two informative scales. The first scale gives the magnitude and phase angle of the discrete harmonic components shaping the waveform. The second scale gives the cosine and sine values of the discrete harmonics. Both scales are related and either scale will be sufficient to determine the extent of distortion. Mathematically, these scales are represented as follows.

$$Y(t) = A_n \sin(n\omega t) + B_n \cos(n\omega t)$$
$$= Y_n \sin(n\omega t + \Phi_n)$$

$$Y_n = \sqrt{A_n^2 + B_n^2} \Rightarrow \text{magnitude}$$

$$\Phi_n = \arctan\left(\frac{B_n}{A_n}\right) \Rightarrow \text{phase}$$

The terms A_n and B_n can be found from

$$A_n = \frac{1}{\pi}\int_0^{2\pi} Y(\omega t)\sin(n\omega t)\mathrm{d}(\omega t)$$

$$B_n = \frac{1}{\pi}\int_0^{2\pi} Y(\omega t)\cos(n\omega t)\mathrm{d}(\omega t)$$

The DC component, if present, is given by:

$$A_0 = \frac{1}{2\pi}\int_0^{2\pi} Y(\omega t)\mathrm{d}(\omega t)$$

But wait. Do we really need to go into inte-

1a

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1b

920052-12
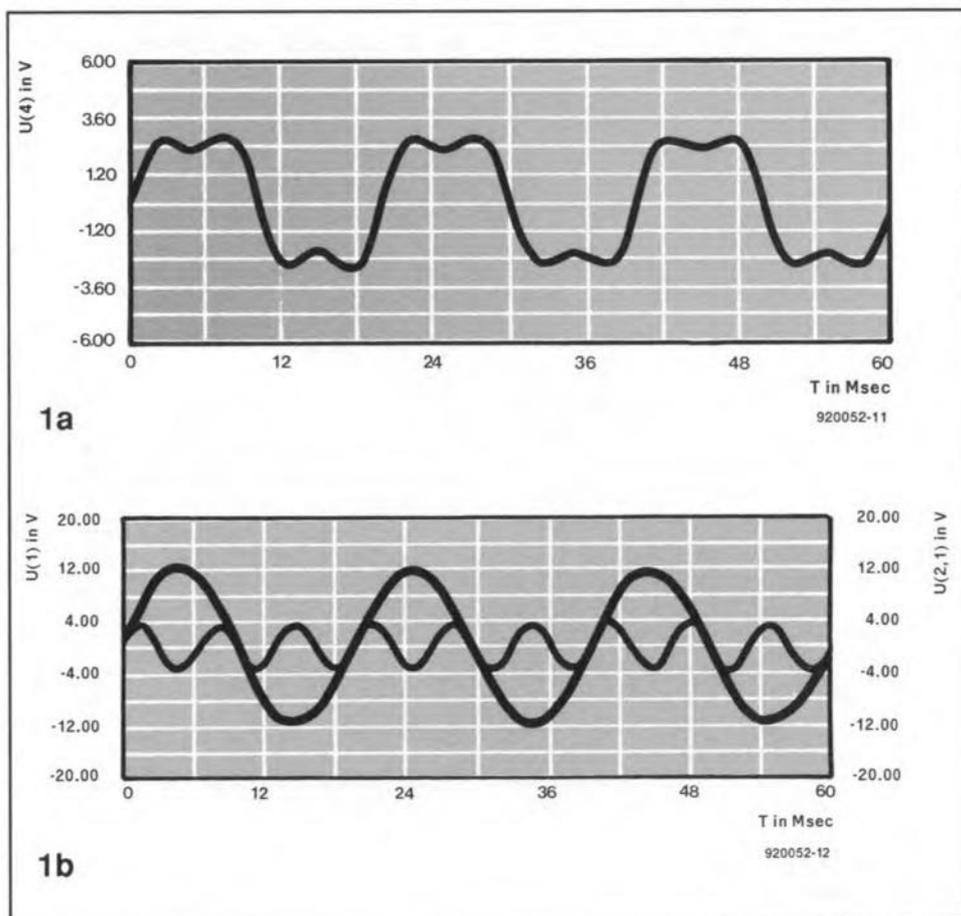
gration and vector calculations to understand waveform distortion? Relax, not in the 90s. By using software available on the market and, of course, basic practice in electronic circuit analysis, it is quite possible to analyse almost any waveform and in effect produce the proper optimally designed system and this could be by introducing filters or by modifying the control concept.

Sinusoidal waves

In this section, several AC shaped waves, produced by a rectifier or phase-controlled power device, are presented and their harmonic content is simplified.

The ideal or smooth waveform is the sinusoidal wave that is produced by large generators in power stations. Figure 2 shows its waveform and its Fourier analysis is presented in the shape of the harmonic magnitude and the phase angle. The cosine and sine terms discussed in the previous section are plotted at the right. The analysis shown is the screen printout of the Micro-cap III software Fourier analysis section.

It can be seen from Fig. 2 that the wave contains no DC nor any sort of harmonic, either odd or even. Thus, the fundamental component dominates the wave shape.

The absence of distortion means that no filtering is required and that all the generated energy is effectively transferred to its destination. Although such pure waveforms exist along the electrical power lines, they may not be so pure any more by the time they reach domestic or industrial power outlets, because the mass of electrical and electronic equipment connected to these outlets nowadays generates a myriad of spurious frequencies that are transferred to the power lines. One apparatus that is very sensitive to impure mains power is the computer, which is why a power conditioner or UPS is normally recommended for its protection

Selected practical waveforms are compared with the ideal wave in Table 1.

Wave I lists the ideal wave with its clear position of transmitting faithfully 100% power to the load without any distortion.

Wave II shows a phase-controlled AC source as found in many light-dimmer circuits using bi-directional semiconductor devices to produce the desired variable AC source as the one shown. For a 50% control ratio, that is, half the power transmitted, the print screen of the Fourier analysis shown in Fig. 3 reveals a handful of harmonics despite the fact that only half the power is transmitted. Practically, the level of harmonics can be neglected as long as its magnitude does not exceed 20% of that of the fundamental component.

It is important to realize what this distortion might cause. High-frequency, high-level harmonics cause excessive heat loss and disturbance in the performance of the controlled system. All industrial and domestic systems are designed to operate from the ideal supply wave shape and frequency. If a mains supply with a high content of harmonics is used to

% of fundamental component	I	II	III	IV	V	VI
dc	0	0	63.5	150	70	150
Fund.	100	100	100	100	100	100
2	–	–	42	20	37	18
3	–	54	–	8	23	–
4	–	–	8	–	17	27
5	–	18	–	–	14	90
6	–	–	–	–	18	27
7	–	18	–	–	9	–
8	–	–	–	–	–	–
9	–	10	–	–	–	23
10	–	11	–	–	–	63

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Table 1. Fourier analysis of 'sinusoidal' waves.
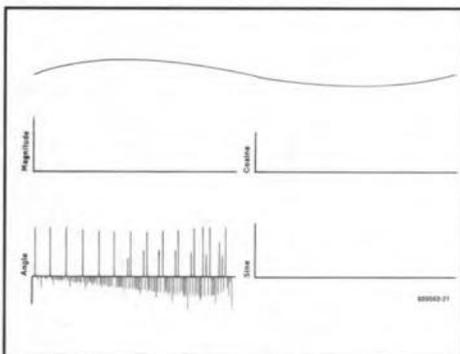
Fig. 2. Sinusoidal wave (ideal shape).
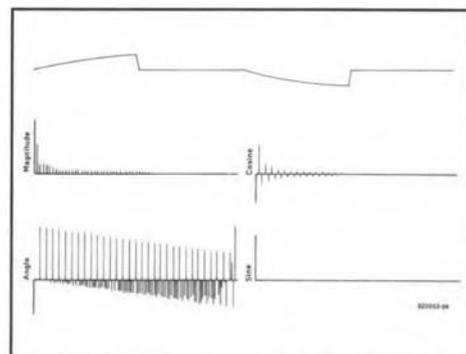
Fig. 3. Phase-controlled AC wave.
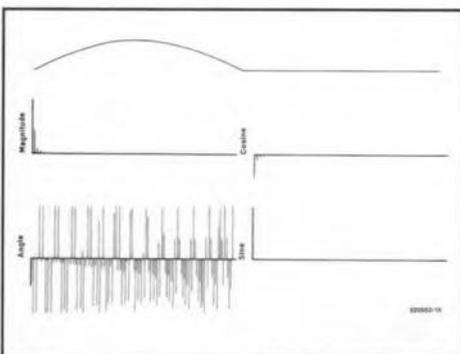
Fig. 4. Half-wave rectified wave.
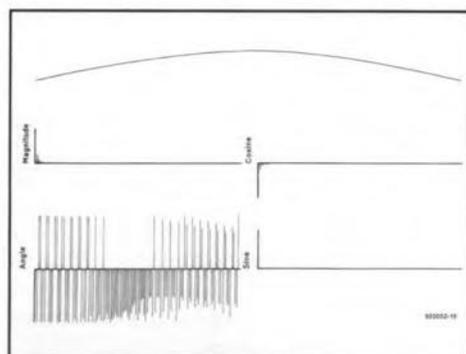
Fig. 5. Full-wave rectified wave.
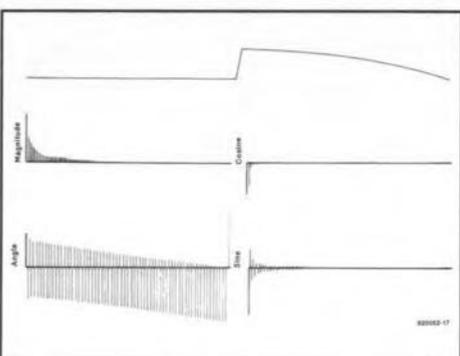
Fig. 6. Controlled (full) rectified wave.
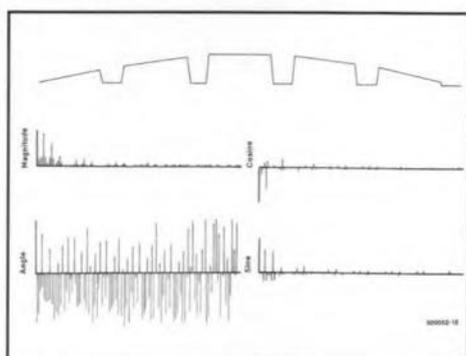
Fig. 7. PWM rectified wave.

power, say, a universal motor such as hand drill or food mixer, the motor is faced with several AC supply signals at high frequencies and at different phase angles. This causes a good deal of extra heat in the motor windings, noise and a drop in efficiency.

More high-level harmonics contained in the wave cause excessive radio interference and requires wide-band filters. Moreover, when a complex power source is supplied across a circuit containing inductance and capacitance, it may happen that the circuit resonates at one of the harmonic frequencies, which is called selective resonance. It is es-

sential, therefore, to include chokes or more complex filters or change the power source, both of which add to the final cost of the product.

Wave III is a half-wave rectified wave that has a 61% DC level (amplitude/π) and a handful of odd harmonics. Simply connecting a capacitor across the load is normally enough to reduce the harmonics to an acceptable level. The Fourier analysis is plotted in Fig. 4.

Wave IV is a full-wave rectified wave. Its DC level is 150% of the fundamental, that is

twice amplitude/π and, again, a handful of odd harmonics that are, however, of a lower level than those in the half-wave rectified wave. Again, a capacitor across the load will reduce the harmonic level substantially. The Fourier analysis is plotted in Fig. 5.

Wave V is a full-wave rectified wave under phase control, resulting practically in a variable DC source. At a 50% control ratio, the DC level is 67% and the harmonic content is worse than in Wave III. The Fourier analysis is plotted in Fig. 6. Although this yields a variable DC source, there is a problem in the filter selection: the smoothing capacitor chosen must be capable of by-passing high frequencies up to five times the supply frequency.

Wave VI is produced by pulse-width modulation (PWM) techniques to generate a variable DC source. Depending on the rate of on/off switching, the harmonic content rises alarmingly, indicating the importance of well-designed filter elements for a wide range of frequencies. Te Fourier analysis is plotted in Fig. 7. As the switching frequency increases, the harmonic level shifts to the higher frequencies which makes it difficult to attenuate them by simple filters.

From these examples, it is seen that distortion is at its worst when the supply changes state suddenly as in Waves III and VI. A smooth transition and composition of the wave has the least distortion and this makes filtering straightforward.

DC or pulsed waveforms

	VII	VIII	IX	X	XI
d c	0	79	0	0	0
Fund.	100	100	100	100	100
2	–	–	–	–	–
3	–	33	33	–	–
4	–	–	–	–	–
5	–	20	20	18	20
6	–	–	–	–	–
7	–	14	14	15	14
8	–	–	–	–	–
9	–	11	11	–	–
10	–	–	–	–	–

% of fundamental component

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Table 2. Fourier analysis of DC or pulsed waveforms.

In this section, we look at harmonics in DC or pulsed waveforms—see Table 2.

Wave VII is, again, the ideal sine wave.

Wave VIII is a square wave as produced by, for instance, a multivibrator oscillator. By inspection, the average value is half the amplitude for a 50% mark-space ratio. The fundamental is equal to twice the amplitude divided by π. Only odd harmonics (all cosine terms are zero) are present owing to the nature of the wave. A low-pass filter with a transfer function equal to zero at high frequencies will by-pass high-order harmonics but will introduce phase distortion in the output. Fourier analysis is plotted in Fig. 8.

Wave IX is a periodical DC wave, typical of that generated by many commercial transistorized inverters. An inverter is a circuit to convert a DC voltage into a periodical waveform. The Fourier analysis is plotted in Fig. 9. High-level third, fifth and seventh harmonics contribute to the shape of the wave. Note that the more higher harmonics are contained, the sharper the wave will be.

It is difficult to filter out the third and fifth harmonics as both are at high level and close to the fundamental. The filter design must be a good compromise between inductance and capacitance values. Large induc-

Fig. 8. Fourier plot of square wave.
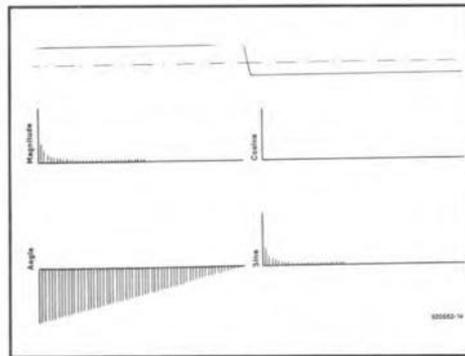
Fig. 9. Fourier plot of periodical DC wave.
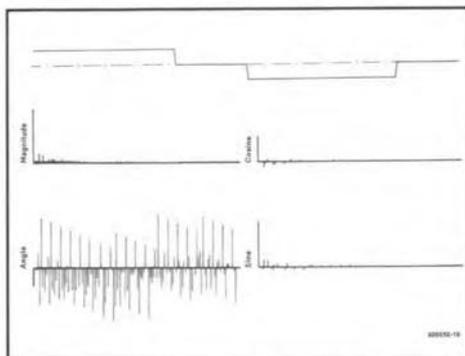
Fig. 10. Quasi-square periodical wave.

Fig. 11. Quasi-sinusoidal wave.

tances and small capacitances cause the inverter regulation to become poor. Small inductances and large capacitances improve regulation but increase the current through the inverter. Regulation is the ratio between no-load and full-load output voltage.

Wave X is, again, the inverter waveshape but with a different control. Its Fourier analysis is plotted in Fig. 10. The waveform, which has fewer harmonic peaks, is known as a quasi-square-wave. The analysis shows the existence of a small percentage of third harmonic content, but the fifth and seventh are not noticeable.

Wave XI is a quasi-sinusoidal wave that can be detected in many industrial motor drive controller. The distortion over a wide frequency spectrum contains 20% fifth and 13% seventh harmonics, but at low level. Single filter elements are, therefore, effective in many cases. If the smoothing filter in the DC path is capacitive, the system is called a constant-voltage source; if it is inductive, the system is a constant-current source. The Fourier analysis is plotted in Fig. 11.

Summary

Most pulse-shaped waves contain odd harmonics. If the periodical amplitude swings between equal positive and negative peaks, the average DC component is nought. If the amplitude remains above the zero level, there is always a DC component.

The waveforms shown in this article are, unfortunately, all real-life shapes used intensively in the motion control of electric machines. Simple filters have not much effect, and are often bulky and expensive. The existence of harmonics produces torque pulsation in motors, which causes extra heat, vibration and noise.

With the advances of microprocessor-controlled inverters, harmonic attenuation by pulse-width modulation is now available. As always, however, one should consider complexity and cost against performance. ∎

RED-LIGHT DIODE LASERS

based on an original article by S. von Fehren

DIODE lasers that operate from the near-ultraviolet to well into the infra-red region are commonplace and used, among others, in optical fibre communication, optical memories and compact-disc players. Until a few years ago, the only lasers producing visible light were He-Ne lasers. Some of the He-Ne lasers emit a deep red light at a wavelength of 632.8 nm, that is in the visible light region, while others operate at 1.15 μm or 3.39 μm. In spite of the fact that they are (relatively) large, require a power source of kilovolts, cannot be modulated and are highly sensitive to mechanical phenomena, these gas lasers have become very popular because they are inexpensive and easy to manage.

These lasers now have a serious competitor in a diode laser, announced by Toshiba in 1987, but not commercially available until recently, that operates at 660 nm (red light).

Diodes that emit visible light have, of course, been available for many years. Such light-emitting diodes (LEDs) are made from a variety of semiconductor material to obtain a particular colour of light. Gallium-arsenide (GaAs) for near-infra-red; gallium-arsenide-phosphide (GaAsP) for red and yellow; gallium-phosphide (GaP) for green and blue. See Table 1 for light and near-light wavelengths and associated colours.

Without repeating its derivation (see Ref. 1), the formula from which the wavelength, λ, can be calculated is

$$\Delta E = h\nu = hc/\lambda, \qquad [1]$$

where ΔE is the energy released when an electron passes from one energy level to another, h is the Planck constant (4.14×10^{-15} eV·s), ν is the frequency of radiation, c is the speed of light in a vacuum and λ is the wavelength (colour) of the emitted light. The quantity $h\nu$ is a quantum of energy commonly called a photon.

From formula [1], it is seen that, since h and c are constants, the wavelength depends entirely on ΔE. In semiconductors, energy difference is called the energy gap, expressed in eV (electronvolts). One eV = 1.60210^{-19} joule (J). The energy gap cannot be measured: it is determined empirically, that is, by measurement. The energy gap between gallium and arsenide is 1.4 eV. Entering the various quantities in formula [1] results in a wavelength:

$$\lambda = hc/\Delta E =$$
$$= 4.14 \times 10^{-15} \times 3 \times 10^8 / 1.4 =$$
$$= 8.86 \times 10^{-7} \text{ m} = 886 \text{ nm},$$

which is in the near-infra-red region.

To obtain shorter wavelengths (that fall in the visible region), different materials must be used.

Standard laser diodes are made from gallium-aluminium-arsenide (GaAlAs), which has an energy gap of 1.6 eV, corresponding to a wavelength (computation as before) of 775 nm. Because of high production quantities and standardized manufacture, these diodes cost only about a few pounds ex-factory. They are used extensively in CD players and laser printers.

New techniques

The new laser diodes, Toshiba Types TOLD9220 and TOLD9222, are made from indium-gallium-aluminium-phosphide (InGaAlP), which has an energy gap of about 1.9 eV to give a wavelength of 660 nm. Prices of these devices have been coming down rapidly.

Currently, Toshiba research scientists are working on a laser diode that will emit blue light (500–445 nm). The difficulty, as before, is finding suitable semiconductor materials that can be doped appropriately to yield a p-n junction with the required energy gap of about 2.2 eV.

The (index-based) construction of the TOLD9220 is shown in Fig. 1. Its major parameters (at 25 °C) are

- wavelength, λ: 660 nm
- threshold current, I_{th}: 75 mA (max. 90 mA)
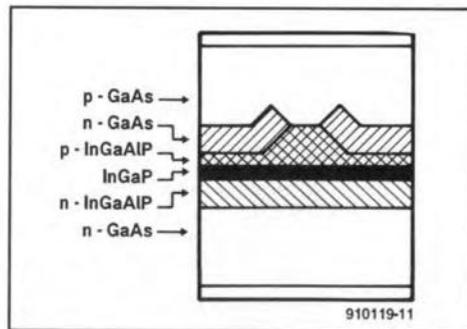
Fig. 1. Layer construction of the new Toshiba laser diodes.
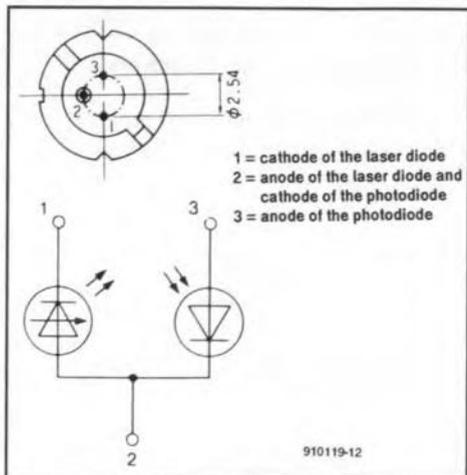
Fig. 2. Pinout of the TOLD9220.

- operating current, I_o: 85 mA (max. 100 mA)
- break-down voltage, U_p: 1.5 V
- operating voltage, U_o: 2.5 V (max 3.0 V)

- luminous power, P_L: 3 mW
- max. housing temperature: +40 °C.

The pin-out of the TOLD9220, shown in Fig. 2, corresponds to that of CW (continuous wave) laser diodes, which emit light constantly. As in LEDs, the light emission may be raised by increasing the current. However, that also increases the dissipation, which, in LEDs, because of their relatively large emission surface, can be tolerated for some time, but which in laser diodes can be fatal. This is because the actual emission surface in laser diodes is tiny: only 2.5 μm^2.

A semiconductor crystal emits light not only forward, but also from its backplane. This back emission, amounting to about 5% of the forward emission, falls on to a photodiode whose resistance varies in direct proportion to the luminous intensity. This makes it possible for a circuit controlled by the photodiode to regulate the current through the laser diode, and thus its dissipation. In other words, the temperature of the laser diode is, to some degree, controlled by the light emission.

An artist's impression of a cross-sectional view of the diode is shown in Fig. 3. The laser diode chip (A) is the semiconductor crystal shown in Fig. 1. Although the photodiode is contained in the same housing, the whole construction is referred to as the 'laser diode'. The construction is typical of CW diodes, which nowadays are produced in far greater numbers than pulse lasers.

Control circuit

A suitable circuit for controlling the new Toshiba laser diodes is given in Fig. 4. Zener diode D_2 holds the voltage at the emitter of T_1 at 2.2 V with respect to earth. Provided that the photodiode receives no light, its resistance is a maximum. The base of T_1 is connected across that resistance and the preset is, therefore, at minimum voltage. Since T_1 is a p-n-p type, it is switched on, whereupon its collector current drives T_2 also into conduction. The latter transistor thereupon switches on the laser diode, which then draws a current that is limited by R_3.

The laser diode emits the maximum permissible light flux, part of which is received by the photodiode. The resistance of the photodiode decreases, whereupon the base

potential of T_1 rises. This causes a decrease of the current through T_1 and T_2, and thus through the laser diode. In that way, the light emission of the laser diode is kept at a more or less constant value, which depends on the setting of P_1 (the voltage across D_1 is, of course, the reference). The current through the laser diode is inversely proportional to the active resistance of P_1. Resistor R_3 prevents the current rising above the maximum permissible value of 100 mA.

Since the laser diode operates in CW mode, it reaches its maximum operating temperature of 40 °C within about a minute. Because of this rapidity and in spite of the control circuit, it is recommended that the laser diode is mounted on a suitable (TO-5 or TO-39) heat sink.
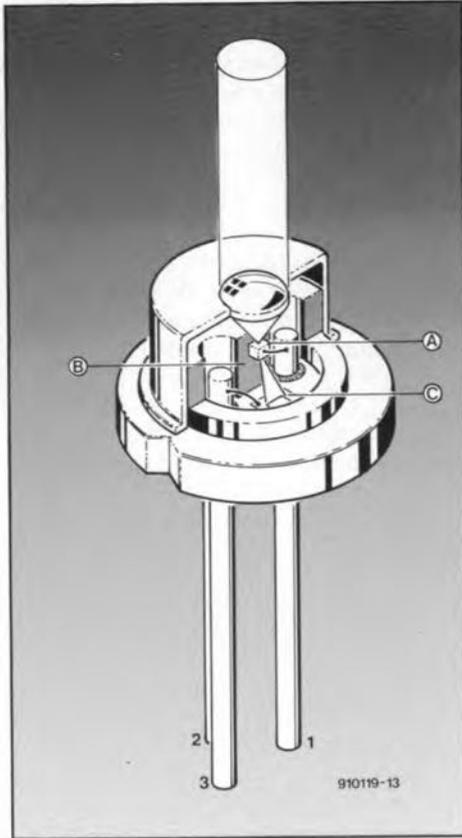
Sample of the new Toshiba laser diodes.

Applications

Red-light laser diodes can be used in many applications, because, compared with He-Ne lasers, their operation and installation are far less complicated (and, moreover, they are cheaper). A glance at Fig. 4 and at a comparable circuit for an He-Ne laser will verify this.

An important industrial application is in barcode readers, which, already in use in thousands of shops and other business, will be almost universal before the end of this decade. Such readers scan the black and white bars of a barcode: the white ones reflect the light, which is then applied to a photodiode, whereas the black ones absorb it. The contrast between the reflected and absorbed light becomes greater as the wavelength becomes smaller; wavelengths above 780 nm cannot be used in barcode readers. Red-light diode lasers are, therefore, very suitable. Moreover, because of their small size, they can be used in portable and mobile barcode readers, which is not really possible with (the rather larger) He-Ne lasers.

At this point, it should be borne in mind that, apart from coherence and power density, monochromaticity, that is, the absence of all other wavelengths, is *the* advantage of laser light over traditional light. Barcode readers and CD players cannot function properly with polychromatic (multi-colour) light.

Fig. 3. Artist impression of the cross-sectional view of the new Toshiba diodes.

Fig. 4. Simple control circuit for CW operation of the new Toshiba laser diodes.
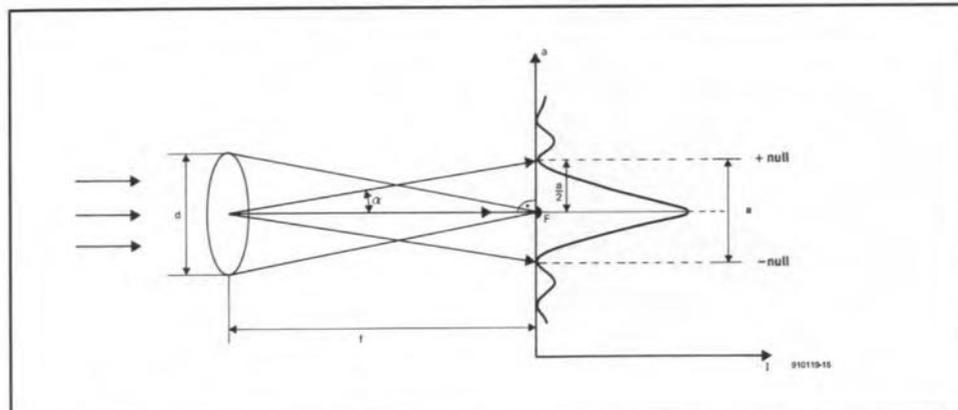
Fig. 5. Focusing of rays of light and consequent light-intensity diagram.

Another interesting application is in the light pointer as used nowadays on projected images in lectures, film shows, and so on. The red-light laser diode is far more suitable than the He-Ne laser for fitting into a reasonably small tubular holder terminated in a convex (focusing) lens. Moreover, it can be powered by alkaline batteries. Such a pointer would cost about a third of the price of an He-Ne laser, and be only a third of the size and weight of an He-Ne laser.

Use in compact and video disk players?

Believe it or not, the price of a compact or video disk player is determined to a larger extent than generally known by the laser it uses. Why this is so will be clear from the following.

In Fig. 5, light falls on to a convex lens of diameter d. The lens concentrates the light at principal focus F, which is a distance f (the focal length) from the optical centre of the lens. The ray of light along the principal axis passes unhindered through the lens to F, but most other rays are refracted to F. Some rays, however, are refracted to points other than F on the focal plane by an angle, α, with respect to the principal axis. From the curve at the right of Fig. 5 it is seen that the light-intensity varies around F. Indeed, when focusing is poor (normally caused by a cheap lens), light at F is not a sharply defined point, but a disc of diameter a around the principal focus. This disc

colour	wavelength (nm)
infra-red	1000–740
red	740–620
orange	620–585
yellow	585–575
green	575–500
blue	500–445
indigo	445–425
violet	425–390
ultraviolet	390–5

is bright at its centre and becomes virtually dark at the nulls. Note that by convention the null below the principal axis is negative and that above is positive.

The angle of aberration, α, is found from

$$\tan\alpha = (a/2)/f, \qquad [2]$$

where $a/2$ is the distance between the nulls and the principal axis.

The angle is also related to the wavelength of the light in the formula

$$\sin\alpha = 1.22\lambda/d. \qquad [3]$$

These two formula can be combined, provided α is small (the normal case) into

$$a = 2.44f\lambda/d.$$

In an ideal lens, $f = d$, so that the diameter of the focal disc is

$$a = 2.44\lambda. \qquad [4]$$

To ensure error-free scanning of the pits on the compact or video disc, the focal disc of the light must not be larger than the pits or wider than the tracks between the pits. This has two important consequences.

First, since the wavelength of the light determines the diameter of the focal disc, non-chromatic light will cause several (overlapping) discs. Only a laser will thus give one focal disc.

Second, the smaller the wavelength, the smaller the diameter of the focal disc, and the smaller the pits and track-width of the compact or video disk can be.

Currently, the wavelength of the laser light in CD players is 780 nm. This makes possible a distance of 1.9 μm between tracks and, consequently, about 18 000 tracks on the 33 mm wide recording surface of a CD. If the wavelength of the laser light is brought down to 660 nm, the number of tracks on a CD, and thus the playing time, can be increased by 18%. The same applies to video disks and CD-ROM. ∎

References

"Lasers: an overview"; *Elektor Electronics*, July/August 1987. p. 27.

"The compact disc"; *Elektor Electronics*, July/August 1987, p. 39.

LCD FOR INDUCTANCE/CAPACITANCE METER

Design by L. Pijpers

The liquid crystal display described in this article and shown in the photograph below is intended primarily for usewith the indutance-capacitance meter published last month

IN the design of a $3^1/_2$ digit voltmeter module, IC Type ICL7106 has attained virtually the same status as a 555: universally known and suitable for almost any application. It has nearly everything needed on board: an analogue-to-digital (A–D) converter with automatic zero-setting and the required display drivers. All that is needed additionally are a reference voltage source and some passive components.

The signal that renders the display black must be in anti-phase with the signal at the back-plane (BP) of the display. The same is true for that controlling the decimal points and the LoBat indication. Unfortunately, the 7106 does not provide these signal and, therefore, transistor T_1 has been added to invert the BP signal. By connecting board pins dp_n, dd_p, and bat to BP, the associated parts of the display become visible.
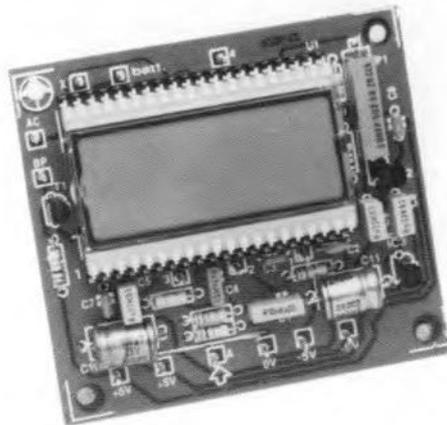
If non-connected pins or the LoBat indication pick up noise that cause the relevant information to become visible, the former can be linked to pin 40 (AC) direct and the latter via a 10 MΩ resistor.

The input circuit is a low-pass filter with a cut-off frequency of 16 Hz that refrains any noise at the input from reaching the A–D converter.

The clock that 'motivates' the 7106 has a frequency, determined by C_2, that makes two measurements per second possible.

Resistor R_4 and capacitors C_3–C_5 form part of the A–D converter circuit.

The supply voltage is high enough to ensure that the reference voltages, connected
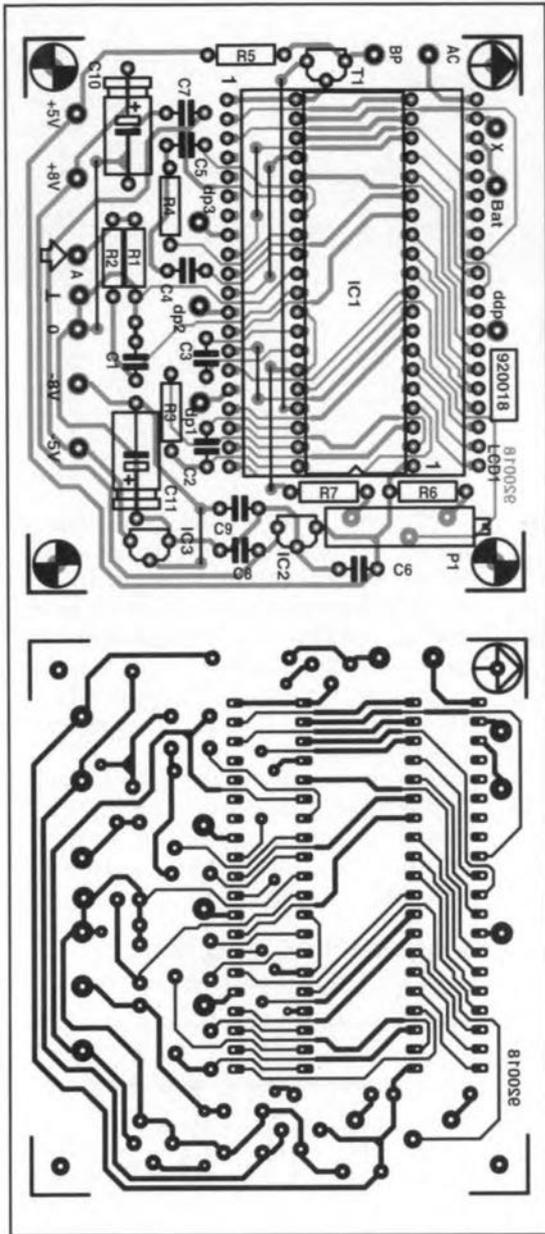
PARTS LIST

Resistors:
R1 = 22 MΩ
R2, R5 = 1 MΩ
R3 = 100 kΩ
R4 = 470 kΩ
R6 = 18 kΩ
R7 = 10 kΩ
P1 = 10-turn preset, 4.7 kΩ

Capacitors:
C1 = 10 nF
C2 = 150 pF
C3, C6, C7 = 100 nF
C4 = 47 nF
C5 = 220 nF
C8, C9 = 330 nF
C10, C11 = 100 µF, 25 V, radial

Semiconductors:
T1 = BS170
IC1 = ICL7106
IC2 = 78L05
IC3 = 79L05

Miscellaneous:
LCD1 = 3$^1/_2$ digit display
40-pin low-profile IC holder
2 off 20-pin terminal strip
PCB 920018

to V+ and Comm of IC$_1$, are sufficiently stable for the A–D conversation to be accurate to 1 digit. This assumes, of course, that the reference voltages, REF HI and REF LO, have been preset correctly with P$_1$. The voltage between REF HI and REF LO must be half the full-scale value, that is, here 1 V. Presetting is easiest by applying a voltage of 1.9 V to the input and adjusting P$_1$ till the display indicates the same value as the meter with which the input voltage is measured. Do not make the input voltage much higher, because if P$_1$ is then turned a little too far, IC$_1$ will indicate an 'overload' which complicates the setting.

To make the circuit suitable for supply voltages of ±8–±20 V, it has been provided with two voltage regulators, IC$_2$ and IC$_3$, which provide a supply of ±5 V. If such a supply is already available, IC$_2$, IC$_3$ and C$_8$–C$_{11}$ may be omitted.

The circuit is best built on the printed-circuit board shown in Fig. 2. Start the construction with the wire links and end with placing the display into its holder. Since the display is mounted over IC$_1$, it is important that the 7106 is fitted in a low-profile holder. If the display does not fit properly on to the two terminal strips, plug another pair of terminal strips into the first and then the display into the second pair.

It is, perhaps, interesting to note that the type of display specified is also suitable for (diffused) back lighting. ∎

PARAMETERS

Metering range	±2 V with respect to earth
Accuracy	±1 digit (see text)
Supply voltage	Regulated: ±5 V
	Unregulated: ±8–±20 V
Display connections	dp1–dp3; ddp (:); LoBat

PARTS LIST

Resistors:
R1 = 22 MΩ
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R3 = 100 kΩ
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C4 = 47 nF
C5 = 220 nF
C8, C9 = 330 nF
C10, C11 = 100 μF, 25 V, radial

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IC1 = ICL7106
IC2 = 78L05
IC3 = 79L05

Miscellaneous:
LCD1 = 3½ digit display
40-pin low-profile IC holder
2 off 20-pin terminal strip
PCB 920018

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PARAMETERS

Metering range	±2 V with respect to earth
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DESIGN IDEAS

The contents of this column are based solely on information supplied by
the author and do not imply practical experience by *Elektor Electronics*

SUPER SIGN

by Dr K. A. Nigim

S UPER SIGN is a 'light-weight' power-
ful circuit that is capable of switching,
manually or automatically, three independent
groups of lamps arranged as desired.

The first group of lamps is switched on and
off at a preset frequency produced by a pulse
generator. The other two groups are switched
alternately by bistables at half the preset fre-
quency.

The output signals from the pulse gener-
ator control the switching of a triac con-
nected between the lamps and the mains
power supply. The triac gate is isolated by a
zero-crossing optoisolator. Figure 1 shows
the major parts of the circuit, which is suit-
able for automatic and manual switch modes.

The pulse generator is built around a Type
4047 monostable/astable multivibrators shown
in Fig. 2. Three different clock signals are
available: (a) at pin 13 (oscillator output);
(b) at pin 10 (Q); and (c) at pin 11 ($\overline{Q}$). The
pulse width (on-time) is controlled through
an *RC* circuit connected between pins 1, 2,
and 3.

Control circuit

The logic for the control circuit is designed
for either manual or automatic initiation as
set by S_1. When the auto mode is selected,
photovaristor R_{16} controls the biasing current
flowing into the base of T_1.

When light falls onto R_{16}, its resistance
decreases, resulting in too small a base cur-
rent into T_1: the transistor then switches off.
At dusk, or at any level of 'darkness' set by
P_2, the resistance of R_{16} increases, whereupon
the base current into T_1 becomes sufficient
to switch the transistor on. Relay Re_1 is then
energized and its contact connects the power
lines to IC_1.

Duty factor

When the duty factor of the pulse at pin 13
is 50% (square wave), the on-time, *T*, (in
seconds) is given by

$$T = 2.2(P_1+R_3)C_1.$$

This time is halved at pins 10 and 11. The
pulse width cannot exceed 20 ms so as to allow
sufficient time for the lamps to switch off.

Power circuit

Each group of lamps is connected to the

**Whether you are advertising
your merchandise, welcoming
your mother-in-law, or
celebrating a day of success,
SUPER SIGN will add light to
the occasion.**

mains supply through a suitable triac, whose
rating depends on how many lamps the par-
ticular group contains. For example, if ten
lamps rated at 100 W each are connected in
parallel, the r.m.s. load current will be 5 A;
whereas if ten 10 W lamps are used, the load
current will be 0.5 A.

The table gives a rough guide between
the number of lamps connected in parallel,
the wattage per lamp and the suggested triac.
It is good practice to mount the triac on a
suitably rated heat sink a little distance from
the logic control circuit.

The gate of each triac is connected to the
relevant output of IC_4 via zero-crossing op-
toisolators IC_1–IC_3—see Fig. 3. This ar-
rangement ensures that the control circuit is
buffered and isolated from the mains. At the
same time, triggering of the triac at the zero-
crossing points greatly reduces radio/TV in-
terference.

Construction and testing

A 12 V DC regulated power supply, rated at
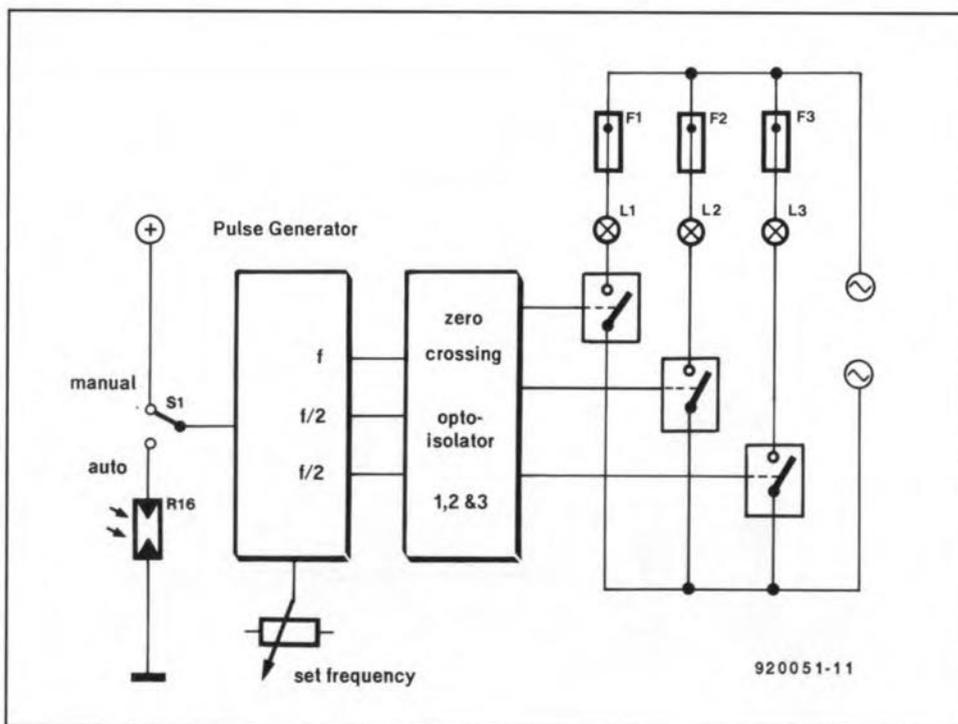
Fig. 1. Three-line super sign.

number of lamps per group	wattage per lamp	RMS current per group	triac type (on heat sink)
10	10	0.5	C206D
10	60	3.0	C226D
10	100	5.0	SC146D
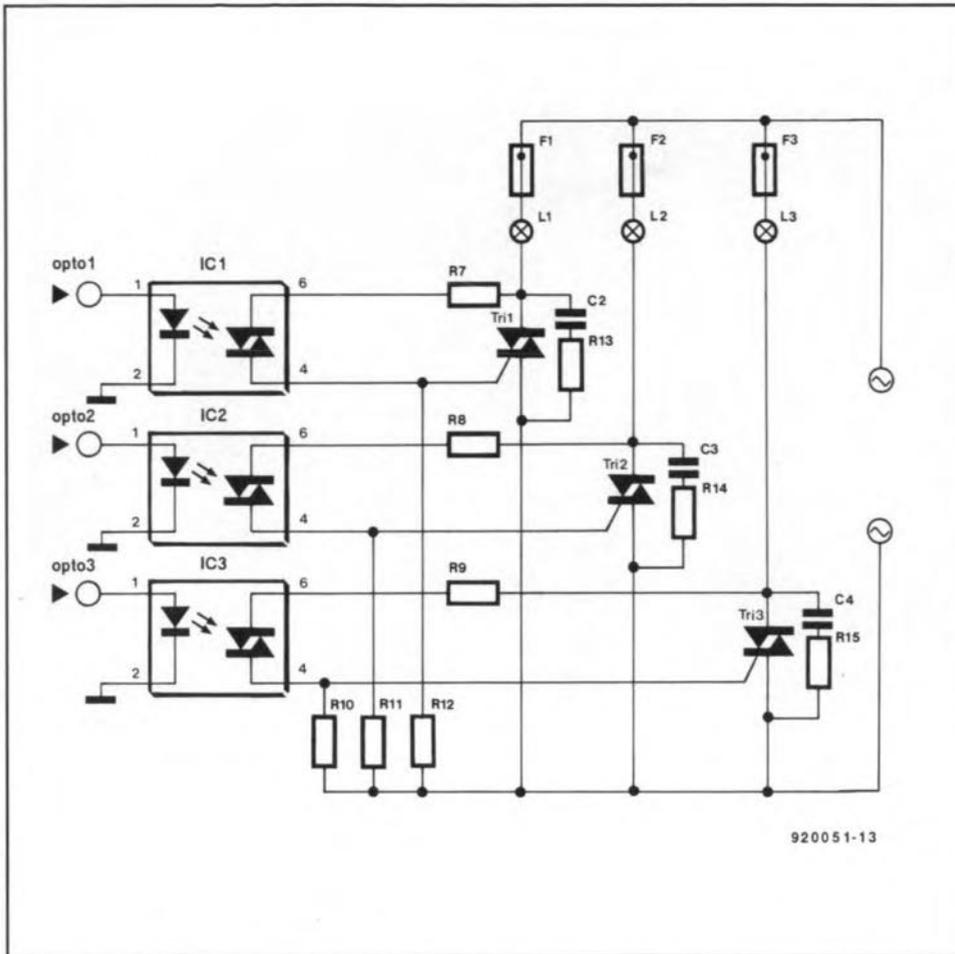
Fig. 2. Automatic/manual control circuit.

500 mA, is required to power the circuits.

The circuit in Fig. 2 is best constructed on an individual small PCB. The location of photovaristor R_{16} depends on individual requirements. Adjust P_2 for the desired level of 'darkness' as indicated by the lighting of D_0 (and the relay changing state). The pulse width is controlled by P_1, which is normally set for a value of 330 ms ($\approx$3 Hz).

The optoisolators and triacs are assembled on a second small PCB. The two boards can be stacked in multi-storey style with the triac board at the bottom. It is recommended that the triacs be fitted on a suitable heat sink.

Variations

The control circuit can be altered to any desired frequency pattern: the use of two PCBs makes replacement of the control board easy. The photovaristor can be replaced by a push-to-make switch (for instance, for a birthday party) in series with a 1–2 kΩ resistor. ■

Fig. 3. Circuit of power triacs.

PARTS LIST

Resistors:
R0, R1 = 1.2 kΩ
R2 = 470 Ω
R3 = 5.6 kΩ
R4, R5, R6 = 200 Ω
R7, R8, R9, R10, R11, R12= 330 Ω, 1/2 W
R13, R14, R15 = 10 Ω, 3 W
P1 = 4.7 kΩ
P2 = 100 kΩ

Capacitors:
C1 = 1 µF
C2, C3, C4 = 0.1 µF, 400 V, polypropylene

Semiconductors:
D0 = LED, red
D1 = 1N4001
T1 = BC107
IC1, IC2, IC3 = MOC3062
IC4 = 4047
Triac = see text

Miscellaneous:
Re1 = 12 V, 400 Ω, sub-miniature for PCB mounting

FM TUNER

PART 2: QUARTZ FILTERS, POWER SUPPLY AND ADJUSTMENT

This second part of the article was originally intended to deal with the adjustment of the main tuner board only. However, following many readers' enquiries, we will first give some additional information on the quartz filters used in the design.

The shape of the filter is apparent from this month's front cover photograph: the TQF-2599 from Toyocom is a small block made of nickel-plated steel. The dimensions of the device are: 31 mm long, 21 mm wide and 18 mm high (approx. $1^{7}/_{32}\times^{13}/_{16}\times^{11}/_{16}$ inch). At the underside of the device are five solder terminals that allow it to be fitted direct on to a printed circuit board. The solder pins are located at the short sides of the enclosure: one side has two pins, the other, three.

Figure 6 shows the electrical equivalent of the quartz filter. Two terminal pairs are connected to the input and the output inductors. The remaining terminal is connected to the filter enclosure. Note that the input inductor allows a balanced connection, while the output of the filter is single-ended (unbalanced or asymmetrical) because the 'lower' end of the output coupling inductor is connected to the enclosure (i.e., to ground).
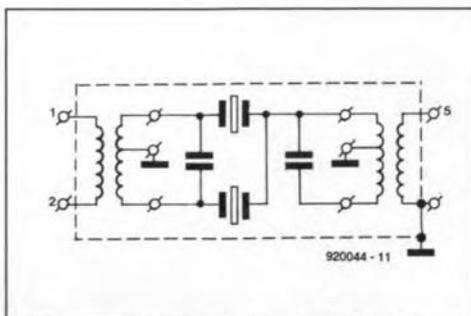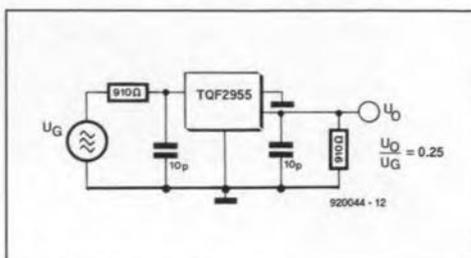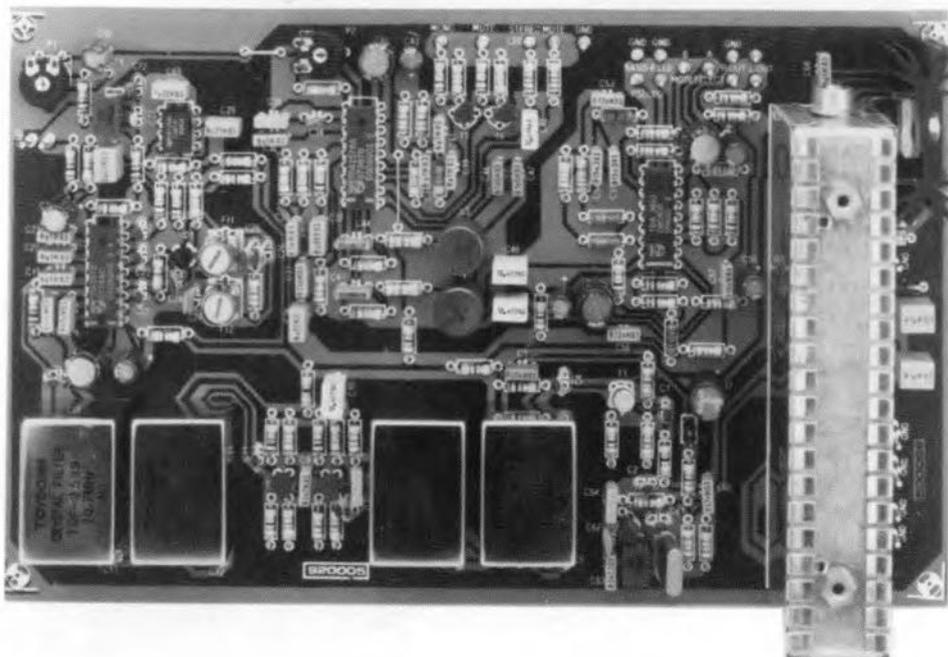
Between the input and the output sit two quartz crystals, whose resonance frequencies differ by an amount equal to the filter bandwidth. The input and output inductors serve to reverse the phase, and to match the crystal impedances. They also determine to some extent the pass-band ripple and the bandwidth. In the present FM tuner, the TQF-2599 meets the requirement for a filter with a small pass-band ripple and good phase linearity. The selectivity, i.e., the rejection of frequencies outside the pass-band, is not a prime requirement, but can be made so by using a number of these filters in series.

The measurement circuit shown in Fig. 7 produces the pass-band characteristic and the pass-band ripple characteristic shown in Figs. 8 and 9 respectively. Although the pass-band curve (Fig. 8) is not entirely symmetrical, the pass-band ripple is very small indeed (Fig. 9): less than 1 dB. Further technical data on the TQF-2599 is given in Table 1. Note that the 'attenuation' shown in Figs. 8 and 9 is relative to the insertion loss of the filter.

As already mentioned, the filters are used two by two to achieve the required skirt steepness. When four filters are cascaded as in the present tuner, the –40-dB bandwidth is reduced to ±180-kHz, while an attenuation of 60 dB is reached at ±300 KHz already. The use of four filters significantly reduces the dip in the pass-band of an individual filter at about +350 kHz, and in addition ensures an image rejection that obviates the use of additional devices to ensure sufficiently high receiver selectivity.

Construction

The main tuner board is fairly large, but simple to populate. This month's front cover shows the finished prototype. All parts must have the correct terminal spacing (pitch) to ensure the shortest possible connections. As always, start with the wire links, of which there are only two on the present PCB. The FD12 tuner module may be fitted with the aid of solder pins, which are soldered on to

Fig. 6.   Internal diagram of TQF-2599.

Fig. 7.   Filter test circuit.

Table 1. TQF-2599 main technical data

Centre frequency:	10.7 MHz ±9 kHz
–3-dB bandwidth:	240 kHz min.
–20-dB bandwidth:	600 kHz min.
–30-dB bandwidth:	–400 kHz to +450 kHz max.
–40-db bandwidth:	–450 kHz to +550 kHz max.
Insertion loss:	–7 dB max.
Pass-band ripple:	1 dB max.
Source and load impedance:	900Ω ±10%; 10 pF ±2 pF parallel

the contact fingers on the edge connector that protrudes from the underside of the unit (see the introductory photograph in part 1 of this article).

The dual varicap used in the demodulator circuit, D1, is a device that looks very much like a transistor in a TO-92 enclosure. The two outer terminals are the anodes, the inner terminal is the common cathode. Although we did not use IC sockets on the prototype, it may be safer to do so. A second prototype built with IC sockets showed no problems.

The two voltage regulators on the board are fitted vertically, and bolted on to a common heatsink. Insulating washers are required for both regulators to prevent short-circuits should the heatsink touch the tuner enclosure, which is at ground potential.

After populating the board, give it a final, thorough, check as quite a few components are involved.

Power supply

The main tuner board works from an adequately smoothed direct voltage of between 23 V and 32 V, which need not be regulated. This supply must be capable of sourcing a maximum current of about 300 mA. The main supply voltage is connected to the PCB terminal marked '+'. The LM317T on the board reduces the unregulated voltage to a stabilized supply of 20 V for the FD12 tuner module. The 20-V supply rail is also connected to the input of the second voltage regulator, an 7815 (IC5), which powers all ICs on the board. The tuning circuit in addition requires a supply voltage of which the maximum value lies between 30 V and 33 V.

Figure 10 shows a suggested power supply that caters for a regulated 32-V output for the main board and the tuning circuit, as well as a 5-V output for the synthesizer (to be described next month). The +32-V output of the supply may be connected to the supply terminals marked '+33 V' and '+' on the tuner board. The tuning voltage proper varies between about 3 V and 30 V, and is determined by the synthesizer. For an initial test of the tuner, the synthesizer is not required, and the tuning voltage, U_{TUNE}, may be taken from the wiper of a multiturn potentiometer connected between ground and +33 V.

Connection and wiring

Apart from the supply connections mentioned above we have the antenna cable, which is connected to the input marked 'Ant.', and the input cable of the stereo amplifier, which is connected to the R-OUT and L-OUT terminals on the tuner board. Both the antenna and the audio connections have separate ground pins on the board to connect the cable screening.

The remainder of the wiring is for the indicator LEDs and the MODE control of the stereo decoder and the audio processor. The signal strength (S-meter) terminals are pro-
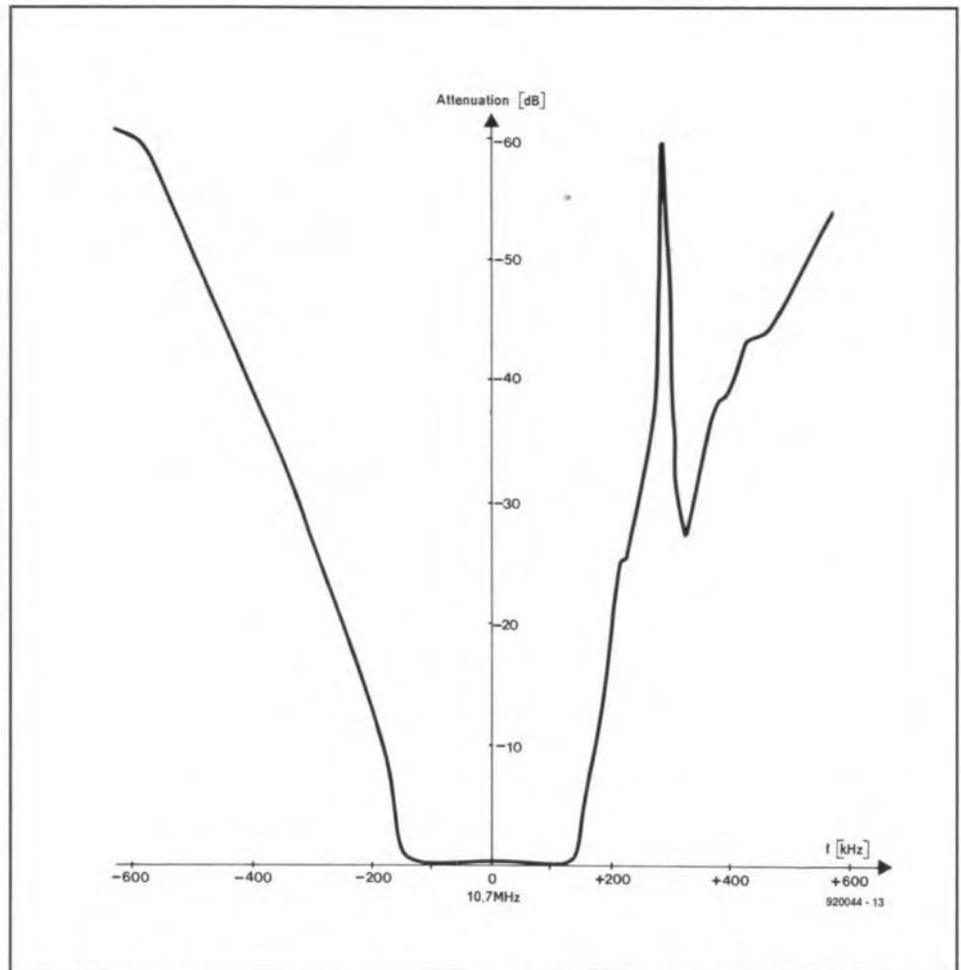
Fig. 8.   TQF-2599 selection characteristic (measured with test circuit shown in Fig. 7).
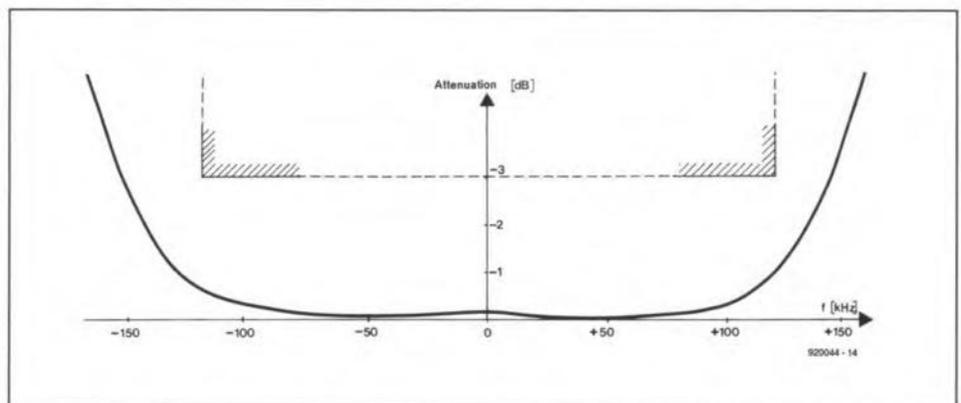
Fig. 9.   TQF-2599 attenuation characteristic within pass-band. The ripple is quite small at less than 1 dB.

visionally connected to a multimeter.

Circuits IC2 and IC3 indicate their current mode with the aid of LEDs. The cathode of the 'STEREO' LED is connected to resistor R47, and the cathode of the 'MUTE' LED to R46. The anodes of these LEDs are connected to +15 V. The LED drivers in IC3 are constant-current types. The cathodes of the 'P-STEREO' (pseudo-stereo) and 'BASIS-B' (widened image) LEDs are connected to ground, and the anodes to the respective PCB terminals.

The mode setting of IC2 and IC3 is effected by a combination of logic levels applied to the corresponding control inputs. The stereo decoder, IC2, switches to mono when a voltage greater than about 3 V is applied to the 'MONO' input. The operation of the 'MUTE' input is similar. By contrast, the

switching levels at the MODE SELECT A and MODE SELECT B inputs are TTL-compatible, i.e., 'low' (L) corresponds to <0.8 V, and 'high' (H) to >2.4 V. This allows the different modes to be set as follows:

Normal operation:	A = L
	B = irrelevant
Wide image:	A = H; B = H
Pseudo stereo:	A = H; B = L

When the inputs are left open (i.e., not connected), they are internally pulled to +5 V. This causes the 'wide image' mode to be selected.

The audio outputs on the board may be connected to any hi-fi amplifier or preamplifier via line (type 'RCA' or 'phono') sockets and a conventional stereo screened cable.
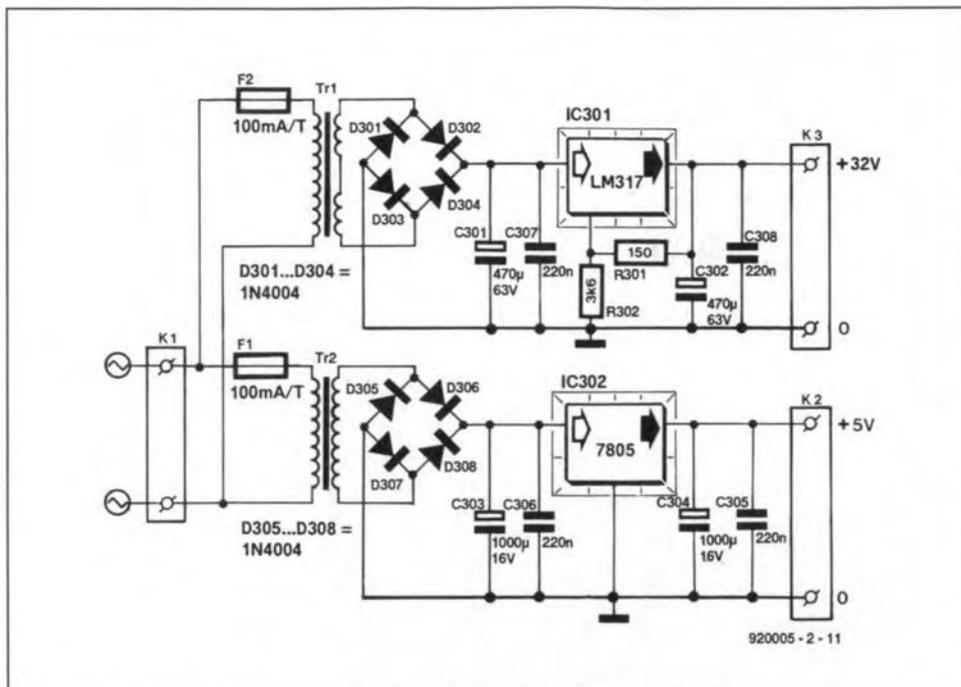
Fig. 10. Suggested power supply for the main tuner board and the synthesizer.

Table 2. Main tuner board connection overview

Terminal	Signal/function		
Ant.	Antenna; 75-Ω unbalanced (coax)		
+33V	Supply voltage for tuning circuit		
UABST	Tuning voltage 3-30 V		
+	+23 V to +32 V		
MONO	>3 V switches to mono		
MUTE (R45)	>3 V mutes AF outputs		
MUTE (R46)	LED to +15 V; lights when mute off		
STEREO LED	LED to +15 V; indicates stereo broadcast		
P-STEREO	LED to ground; indicates pseudo-stereo mode		
BASIS-B LED	LED to ground; indicates wide image mode		
L-R OUT	Left and right audio outputs		
MODESELECT A,B	Select TDA3810 mode		
	Mode	A	B
	Stereo	L	x
	Wide image	H	H
	Pseudo stereo	H	L

Table 2 provides an overview of all board connections and their functions.

Adjustment: easy!

For an initial adjustment of the tuner it is sufficient to connect the main supply only to the tuner board. First, check the output voltages (+20 V and +15 V) of the two regulators. Next, fit wire jumper 'C' to switch on the on-board 10.7-MHz reference oscillator. Connect a voltmeter to pin 6 of IC6, and adjust the core in filter Fi1 until the meter reads about 7 V. A tip: turn the core downward if the measured voltage is initially smaller than 7 V, or upward if the voltage is higher than 7 V. Next, turn the core in Fi2 to the same depth as that in Fi1.

From then on, the quadrature demodulator circuit will keep itself centred at 10.7 MHz. Remove jumper 'C' to switch off the auxiliary oscillator.

Switch off, and prepare the tuner for 'real' FM reception. 'MODE SELECT' is set to 'normal' by wiring terminals 'A' and 'B' to ground. The 'MONO' and 'MUTE' terminals may be left open. Further, connect the antenna cable (a 75-cm long straight piece of wire soldered to 'Ant.' will also function if you are not too far away from an FM transmitter). Lastly, connect the tuning voltage via the (temporary) multiturn potentiometer, and, of course, the audio amplifier. Set P1 and P2 to their mid-way positions.

Switch on again, and tune to a relatively strong FM stereo station. Adjust the PLL centre frequency (P2) until the stereo LED lights. Next, turn the wiper of P2 alternately left and right, and note the positions where the 'STEREO' LED goes out. Set the wiper in between these two positions. This concludes the adjustment of the stereo PLL.

Finally, adjust preset P1 for optimum channel separation. For this you either have to wait for a stereo test transmission, or have access to a stereo test generator. Failing both, leave the preset at the centre of its travel, when the channel separation is at least 40 dB.

□

Next month: description of the synthesizer.
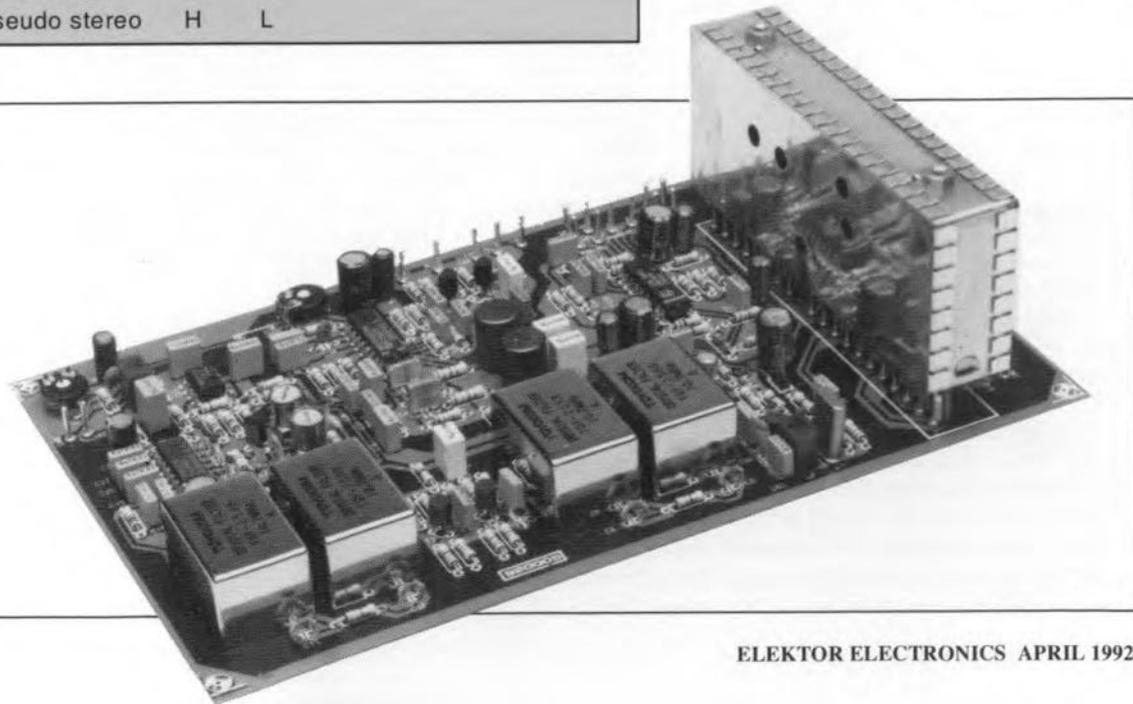
2-METRE FM RECEIVER

The 2-metre band has been popular for three decades and longer for short, medium-range and mobile communication between radio amateurs, and it is usually pretty crowded in and around large cities, with activity centring around repeater stations. The predominant mode for local traffic is FM, and listening in can be a great way to expand your knowledge of electronics as well as get to know fellow enthusiasts. The receiver presented here is aimed at those of you who are not yet bitten by the 'radio' bug. Alternatively, for hams already on the air, the present design is an excellent stand-by receiver to monitor band activity.
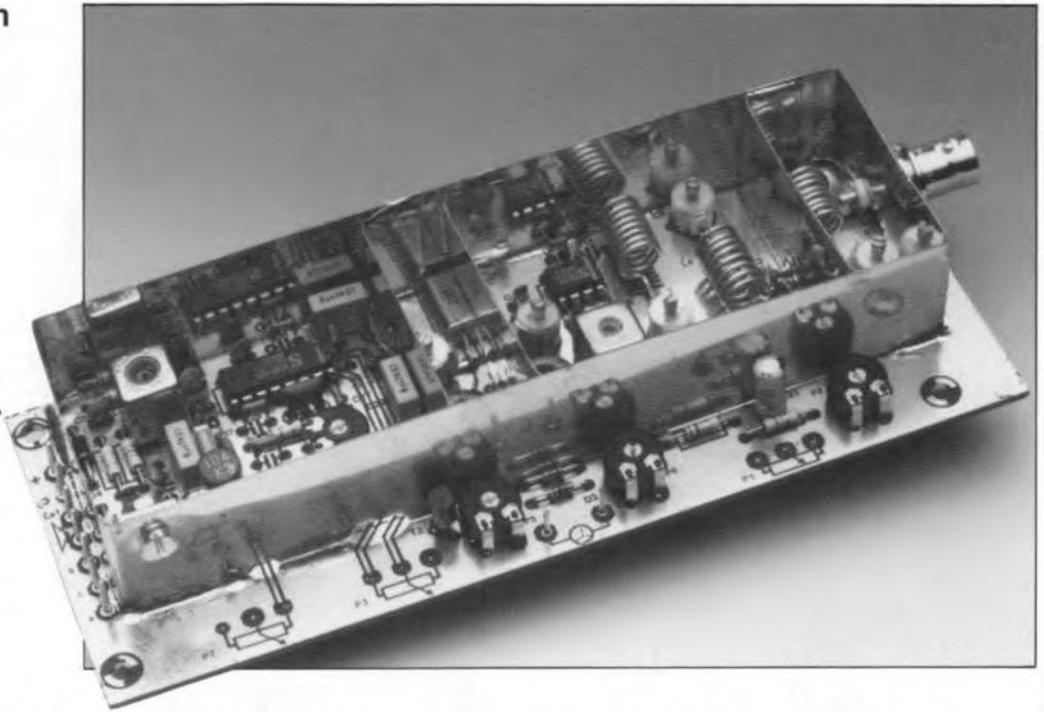
design by J. Barendrecht and L. Lemmens

THE receiver described is remarkably compact, based on three ICs only, and fairly simple to build since a well-designed printed circuit board is available ready-made.

The block diagram (Fig. 1) of the receiver shows that it is a 'classic' superheterodyne with a single intermediate frequency (IF) of 10.7 MHz. The antenna signal is amplified and passed through a band filter before it is applied to an integrated double-balanced mixer. The local oscillator signal is supplied by a varicap-tuned voltage-controlled oscillator (VCO). The IF signal at 10.7 MHz is passed through a crystal filter to ensure the required selectivity of the receiver. Next, it is amplified and filtered again. One integrated circuit combines the functions of demodulator (FM only), squelch (automatic muting) and S-meter driver. It is followed by an AF amplifier capable of driving a pair of headphones or a small loudspeaker.

Practical circuit

The circuit diagram of the 2-metre receiver, Fig. 2, follows the block diagram quite closely. At the RF input there is a low-noise preamplifier based on the BF981 dual-gate MOSFET. The antenna signal is connected to a 50-Ω tap on inductor L1. The amplifier output signal is coupled inductively to the IF amplifier via L4-C9 and L5-C11. These two VHF L-C tuned circuits form a critically coupled bandpass filter with a bandwidth of about 2 MHz to give the receiver the initial preselection required to cope with strong out-of-band signals.

The NE612 (IC1) is an integrated double-balanced mixer and oscillator from Signetics (Philips Components). It is an improved version of the NE602, on which design notes were published in Ref. 1. The block diagram of the NE612 is given in Fig. 3. Here, the on-
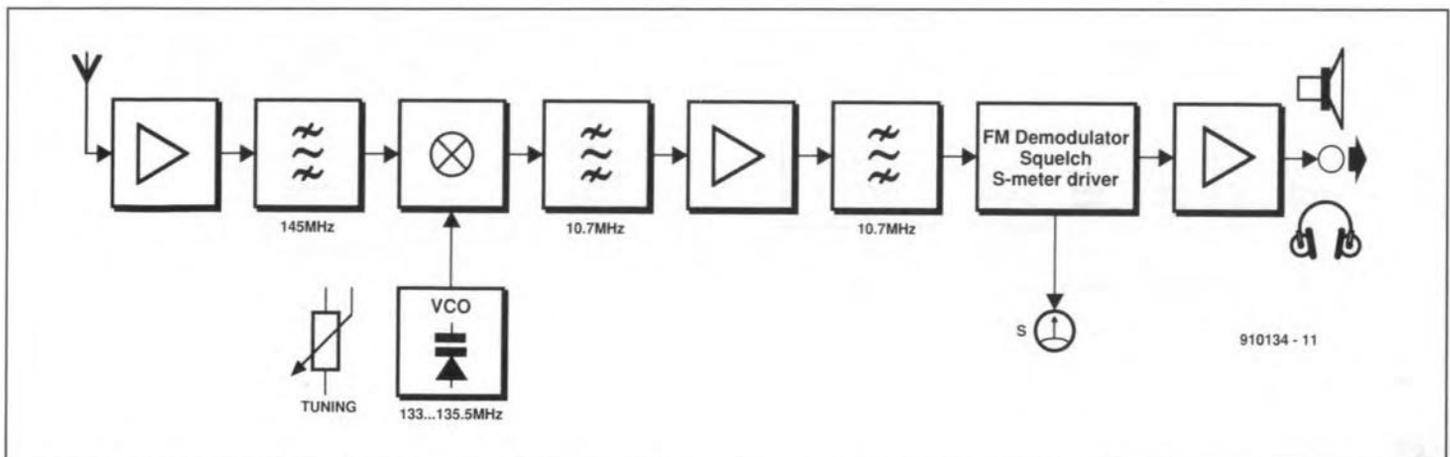
Fig. 1. Block diagram of the receiver: a classic superheterodyne.
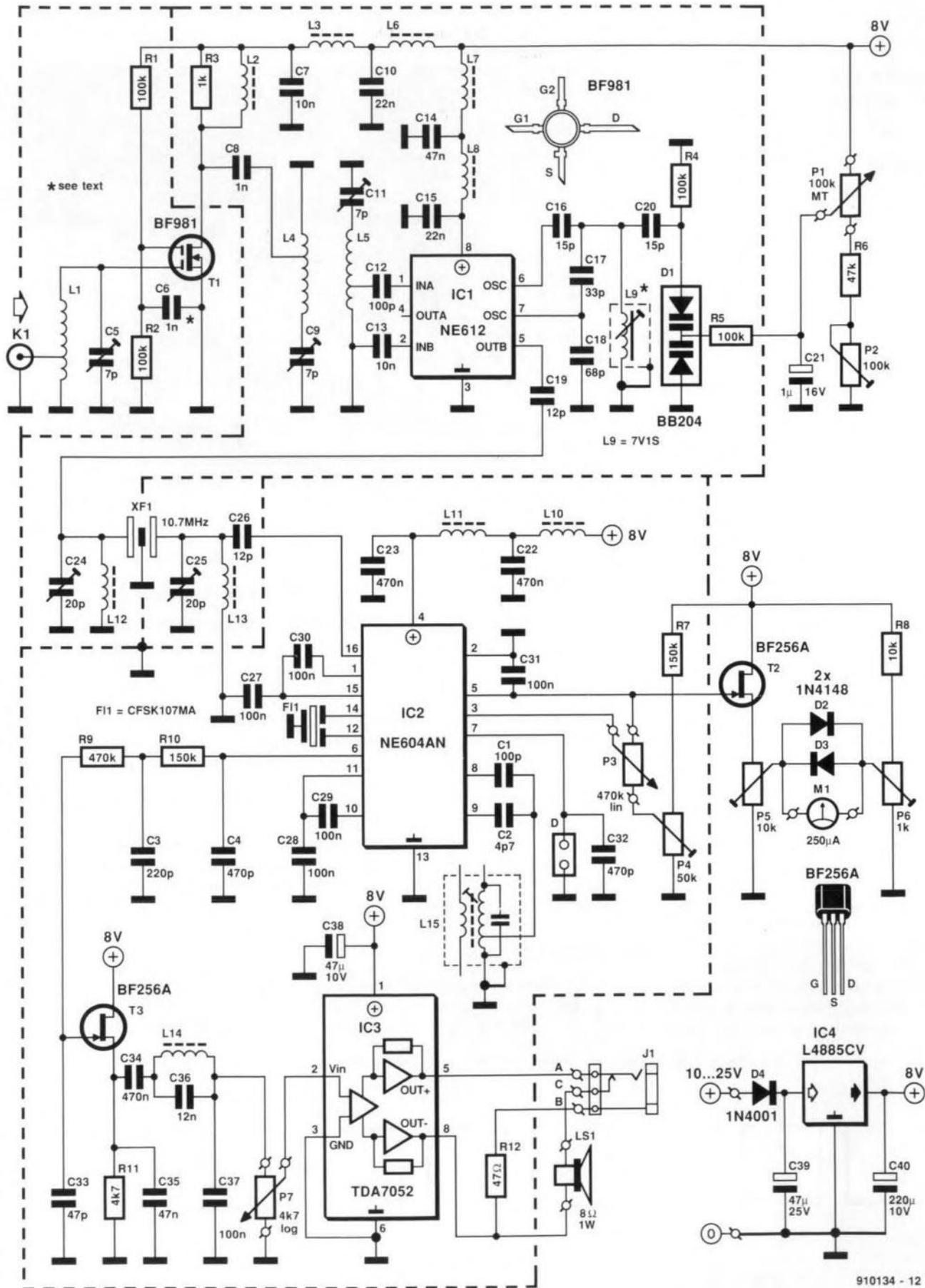
Fig. 2.   Circuit diagram of the 2-metre FM receiver. Note that the IF amplifier, limiter, FM demodulator, S-meter driver and squelch functions are all combined in a single IC, the NE604.
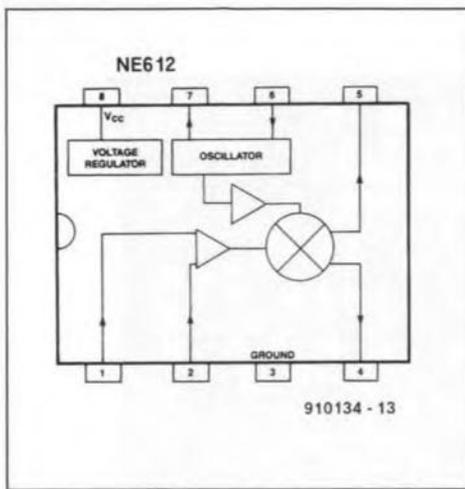
Fig. 3. Block diagram of the NE612 integrated double-balanced mixer (courtesy Signetics).

chip oscillator is connected to an *L-C* tuned circuit of which the resonant frequency is determined by a pair of variable capacitance diodes. The tuning voltage is supplied by a combination of a multiturn potentiometer, P1, a fixed resistor, R6, and a preset potentiometer, P2. Correctly aligned, the VCO has a tuning range from about 133 MHz to 135.5 MHz, which covers the 2 metre band adequately. Depending on the setting of P2 and the value of C17, the VCO range can be made larger, for instance, in the USA where the 2-metre band extends from 144 MHz to 148 MHz (note, however, that the lower end of the band is not used for FM traffic).

The IF output signal is taken single-ended from the mixer output and fed to the 10.7-MHz IF quartz filter via a coupling capacitor, C19. The input and the output of the quartz filter, XF1, are matched by tuned circuits L12-C24 and L13-C25 respectively.

As already mentioned, the NE604 (IC2) combines a number of functions in this circuit. The block diagram in Fig. 4 tells the whole story. A 10.7-MHz ceramic filter, FL1, is inserted between the output of the first IF amplifier and the limiter input of the second IF amplifier on board the NE604. The quadrature (FM) detector is connected to a ready-made 10.7-MHz inductor, L15, via coupling capacitors C1 and C2. Pin 7 of the NE604 supplies the demodulated signal ahead of the mute circuit (see the block diagram). This unmuted signal may be used for AFSK decoders and other equipment (packet radio TNC) that must always work, irrespective of the set mute level. The signal is brought out to a jumper block marked D, which allows ready connection to a screened cable.

The mute (squelch) level is set by potentiometer P3, with preset P4 acting as a 'coarse' control. The S-meter (signal strength) driver consists basically of a FET, T2, and two anti-parallel diodes, D2-D3, connected across a moving-coil meter, M1. The meter may be given a meaningful range by adjusting presets balancing presets, P5 and P6.

The demodulated FM signal is taken through a de-emphasis section, C4-R10-C3, and is then applied to a FET stage that pro-

vides sufficient drive for the AF output amplifier, IC3. An *L-C* series filter is included in the signal path to suppress frequencies above 3 kHz. The audio output signal is fed to a loudspeaker, or to a pair of headphones via an external jack socket with a break contact, J1. When a plug is inserted in the headphones socket, the loudspeaker is automatically disconnected.

The receiver has an on-board 8-V supply based on a low-drop voltage regulator Type L4885CV, which enables input voltages down to about 10 V to be used (battery operation!). Where the L4885CV can not be obtained, it may be replaced by an 7808, which works with input voltages of 12 V and higher. The 8-V supply voltage is decoupled at a number of places in the circuit with the aid of small ferrite chokes and ceramic capacitors to ground. The current consumption of the receiver depends on the output volume, and lies between 45 mA and about 200 mA.

Construction

It is strongly recommended to build the receiver on the ready-made double-sided printed circuit board supplied through the Readers Services. This board, of which the artwork is shown in Fig. 5, is pre-tinned, double-sided, pre-drilled, and has a component layout printed on the component side. Start the construction by winding the inductors as indicated in Table 1. Next, insert the coffin-style capacitor, C6, into its slot in the PCB. The 'shoulders' of this capacitor should rest on the component side of the PCB. Solder the device carefully at the two sides, and check that it does not form a short circuit. Put the MOSFET, T1, in the hole, and align its terminals over the three copper tracks (gate 1; gate 2, drain). The type indication printed on the MOSFET is legible from the component side. If necessary cut the g1 and g2 terminals. Solder all four terminals. The source terminal is soldered direct on to the ground plane.

Use pliers to bend the stator terminals of all five foil trimmers horizontally. Fit trimmer C5, and solder the stator terminal flush on to the copper track to g1 of the MOSFET. The two rotor terminals are soldered at the

solder side of the board. The g2 biasing resistors, R1 and R2, are soldered direct to the g2 side of the coffin capacitor. Similarly, the drain resistor, R3, is soldered direct to the copper track for the drain. C2 is 'in the air' between the drain track and the tap at the earthy ('cold') side of L4. The solder junctions between the trimmers, the matching inductors and the input and output terminals of the quartz filter are also 'in the air'.

The 'hot' side of L4 and L5 is soldered direct to the stator terminal of the respective trimmer capacitor, C9 and C11. The air-cored inductors, L1, L4 and L5, are stretched by spacing the turns evenly. After soldering, the toroidal core inductors, L12 and L13, are secured to the PCB with a drop of wax. Do not yet mount the screening can of the VCO inductor, L9.

The remainder of the construction is fairly straightforward. All components are mounted with the shortest possible lead length. IC sockets must no be used. Fit solder pins for the connections to the external parts.

Inspect your work so far, paying particular attention to short-circuits between component terminals and the copper ground plane.

Next, cut and bend a 20-mm wide piece of tin plate or thin brass, and place it vertically on the dashed outline printed on the component side of the PCB, outside the solder pins in the four corners. Look at the position of the input BNC connector, and make a clearance in the screening large enough to pass over the teflon shaft. Another clearance is required where the screen passes over the tracks to potentiometer P3.

Solder the screening all around to the ground plane. Next, cut three 50-mm long, 20-mm high, pieces of the same material, and align these between the long sides of the screening, over the dashed lines on the PCB. Look at where the screen passes over the drain track of T1, and make a small clearance to prevent a short circuit. Similarly, the screen that separates the input and output of the quartz crystal filter must have a clearance at one side for the quartz filter. Do not solder the screen to the quartz filter enclosure, as the device is easily damaged by overheating.
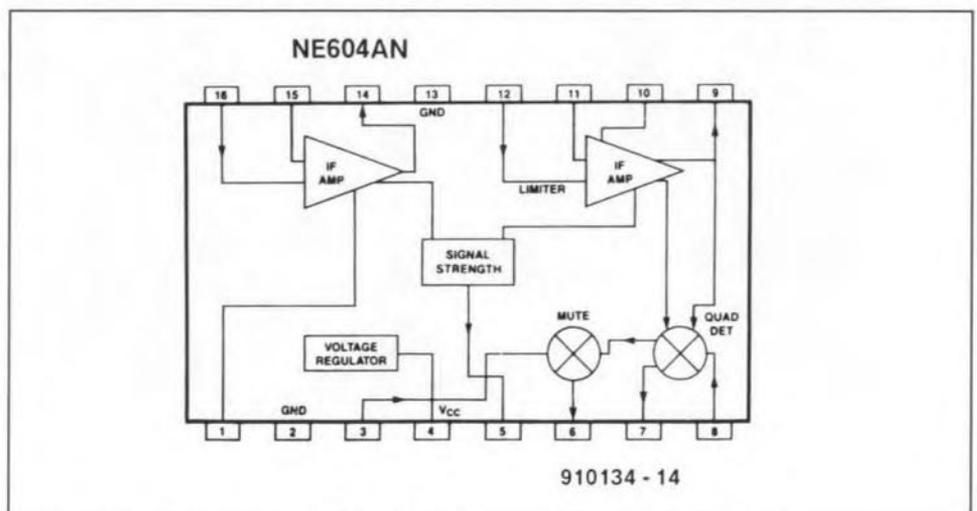

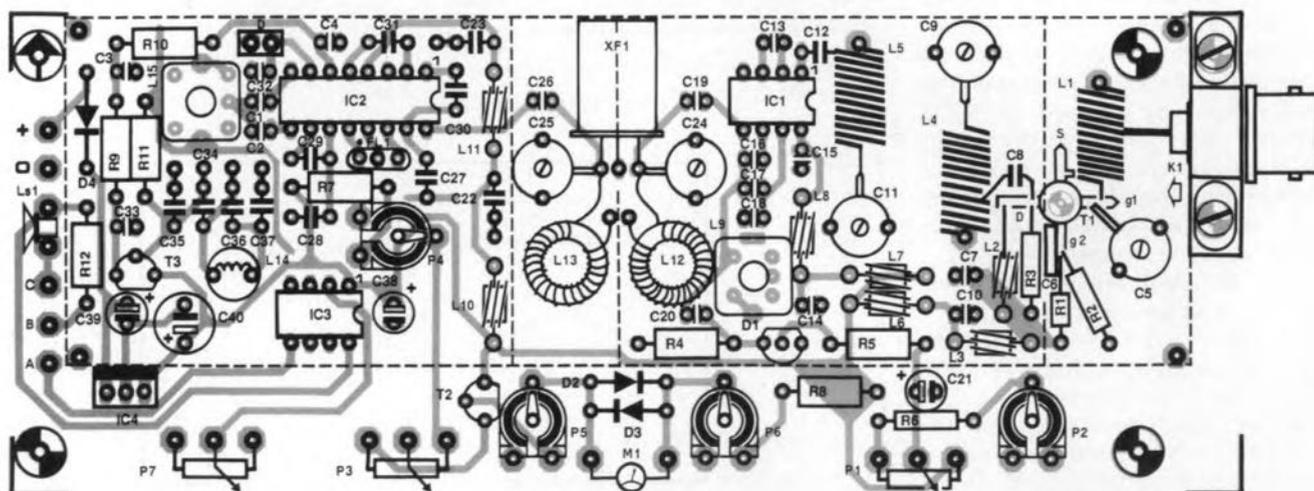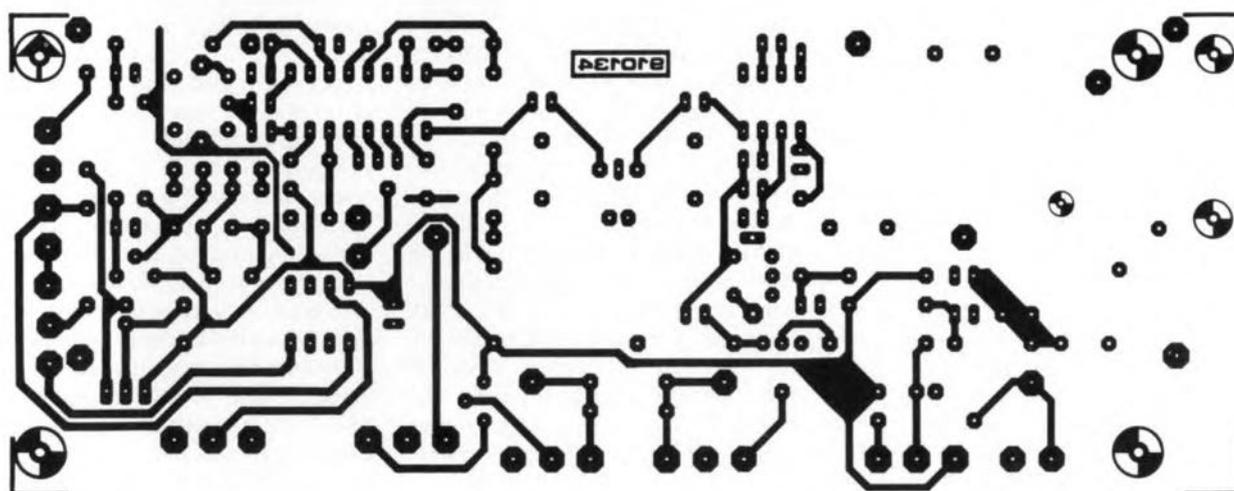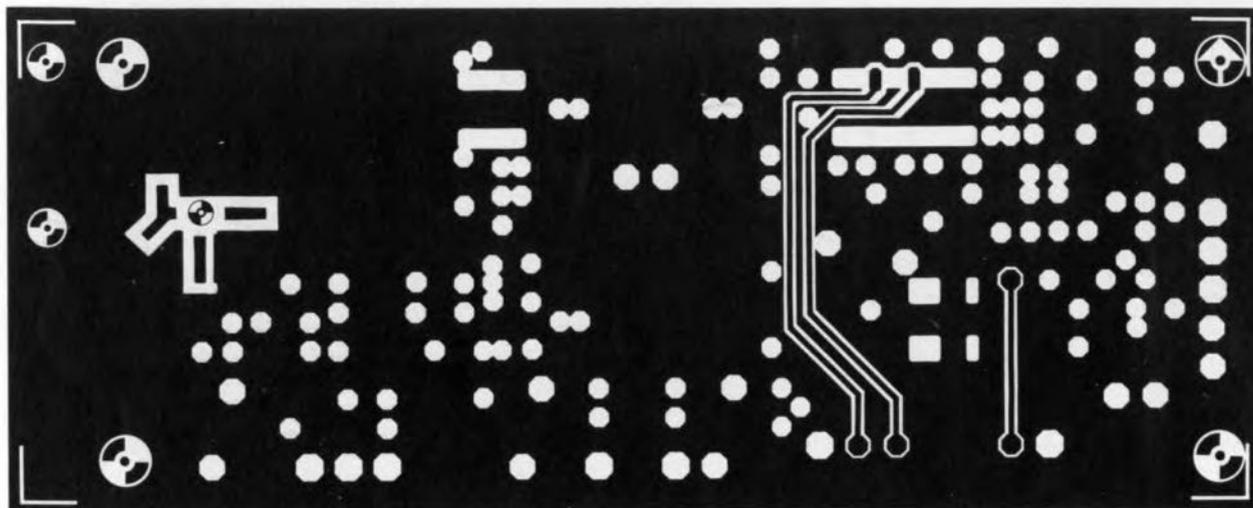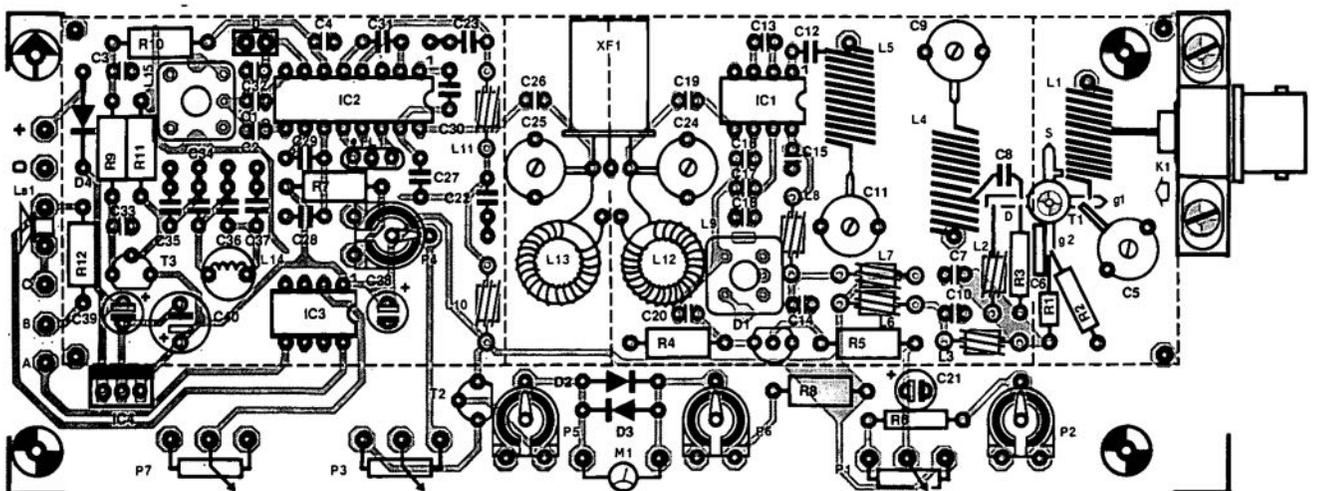Fig. 4. Block diagram of the NE604A FM IF system (courtesy Signetics).

Fig. 5.   Component side and solder side layouts (mirror images), and component mounting plan of the PCB for the 2-metre receiver.

COMPONENTS LIST

Resistors:

4	100kΩ	R1;R2;R4;R5
1	1kΩ	R3
1	47kΩ	R6
2	150kΩ	R7;R10
1	10kΩ	R8
1	470kΩ	R9
1	4kΩ7	R11
1	47Ω	R12
1	100kΩ linear multiturn	P1
1	100kΩ preset H	P2
1	470kΩ lin. potentiometer	P3
1	50kΩ preset H	P4
1	10kΩ preset H	P5
1	1kΩ preset H	P6
1	4kΩ7 log. potentiometer	P7

Capacitors:

2	100pF	C1;C12
1	4pF7	C2
2	20pF trimmer (green)	C24;C25
3	7pF trimmer (grey)	C5;C9;C11
1	1nF coffin	C6
2	10nF	C7;C13
1	1nF	C8
2	22nF	C10;C15
2	47nF	C14;C35
2	15pF	C16;C20
2	12pF	C19;C26
1	33pF	C17
1	68pF	C18
1	1μF 16V radial	C21
3	470nF	C22;C23;C34
1	47pF	C33
1	220pF	C3
1	12nF	C36
6	100nF	C27-C31;C37

2	470pF	C4;C32
1	47μF 10V radial	C38
1	47μF 25V radial	C39
1	220μF 10V radial	C40

Inductors:
Winding details are given in Table 1.
Required materials:

7	3-mm long ferrite bead
1	7V1S assembly (Neosid)
2	T37-6 toroid core (Amidon)
1	10mH radial choke (Toko 181LY103)
1	KACS(K)4520A or KALS4520A (Toko)

1 mm dia. silver-plated wire
0.8 mm dia. enamelled copper wire
0.2 mm dia. enamelled copper wire

Semiconductors:

1	BB204B	D1
2	1N4148	D2;D3
1	1N4001	D4
1	BF981	T1
2	BF256A	T2;T3
1	NE612	IC1
1	NE604AN	IC2
1	TDA7052	IC3
1	L4885CV	IC4

Miscellaneous:

1	BNC socket	K1
1	250μA moving coil meter	M1
1	8Ω/1W loudspeaker	LS1
1	jack socket w. break contact (not on PCB)	J1
1	10.7M15A crystal filter	XF1
1	CFSK107M3 ceramic filter (Toko)	
1	Printed circuit board	910134

Finally, secure K1 to the PCB surface by bolting it down with a clamp.

Adjustment

The adjustment of the receiver requires a VHF signal generator and a frequency meter. If you do not have access to a signal generator, you may need to call in the help of a local radio amateur willing to set up a test signal 'on the air'.

Connect the external controls, the loudspeaker and the S-meter to the board. Initially, set all trimmers and presets to the centre of their travel. Connect the signal generator (or the antenna) to the receiver input.

First, concentrate on the VCO. Apply power, and check that the board supply voltage is 8 V. Couple the frequency meter inductively to L9 (with a small coupling loop), or capacitively (with 10 pF or so) to pin 7 of IC1. Adjust the core in L9 until you are roughly at 134 MHz, then adjust P2 until the VCO range is about 133 MHz to 135 MHz. If necessary, stretch or compress the turns of L9 carefully until the desired VCO frequency

range is obtained (remember, the IF is 10.7 MHz). In some cases, it may be necessary to change the value of C17, or increase the number of turns of L9 from 1.5 to 2.

Switch off, fit the screening can on L9 and measure the VCO range again. Redo the above adjustments as required to compensate the effect of fitting the can. Do not solder the tabs at the sides of the can until you are satisfied with the VCO range.

Tune the demodulator to 10.7 MHz by turning the core in L15 for highest noise output (you may have to adjust the squelch control, P3, to hear the FM noise). Next, peak C24 and C25 for maximum noise output also.

Apply an FM-modulated 2-m test signal to the RF input. Start with a fairly high level, say, 500 μV. Tune the receiver to this signal, and adjust C5, C9 and C11 for minimum noise. Reduce the signal level as you approach the optimum setting of these trimmers. In particular the 2-m band filter will be found to be pretty selective, i.e., critical to adjust.

If necessary redo the adjustment of L15 for undistorted output (it is best to use a test tone for this).

Reduce the RF input level until the signal is just about audible. Again peak the IF and RF trimmers for minimum noise, and if necessary 'throttle' the RF signal even further. Our prototype was adjusted in this way, and achieved a sensitivity of between 0.1 μV and 0.15 μV for an S/N (signal-to-noise ratio) of about 12 dB. This was found comparable to the performance of a typical commercial-grade receiver as used in mobile 2-metre transceivers (the test was made against an FT227RA mobile rig from Yaesu).

Finally, adjust the two presets at either side of the S-meter connections until the meter gives a sensible indication of the signal strength (switch the generator between low and high output levels). Since S-reports have little meaning in FM communication, and the standards used to indicate and compare signal strength are a subject of hot debate between radio amateurs, it makes little sense to try and calibrate the meter in S points. ∎

Reference:
1. "NE602 Primer". By Joseph J. Carr. *Elektor Electronics* January 1992.

Table 1. Inductors

| Position	Description	Core	No. of turns	Wire dia.	Note(s)
L1;L5	VHF air-cored	none	8	1mm CuAg	Tap at 2 turns from cold end; internal diameter 6mm; space turns to fit PCB.
L2;L3;L6;L7; L8;L10;L11	VHF choke	3mm ferrite bead	4	0.2mm CuL	
L4	VHF air-cored	none	8	1mm CuAg	Tap at 1 turn from cold end; internal diameter 6mm; space turns to fit PCB.
L9	VCO 135MHz	Neosid 7V1S	1.5	0.8mm CuL	Space turns.
L12;L13	10.7MHz	T37-6 toroid	50	0.2mm CuL	Secure core with wax; approx. 10μH.
L14	10mH choke	-	-	-	Toko 181LY103 radial.
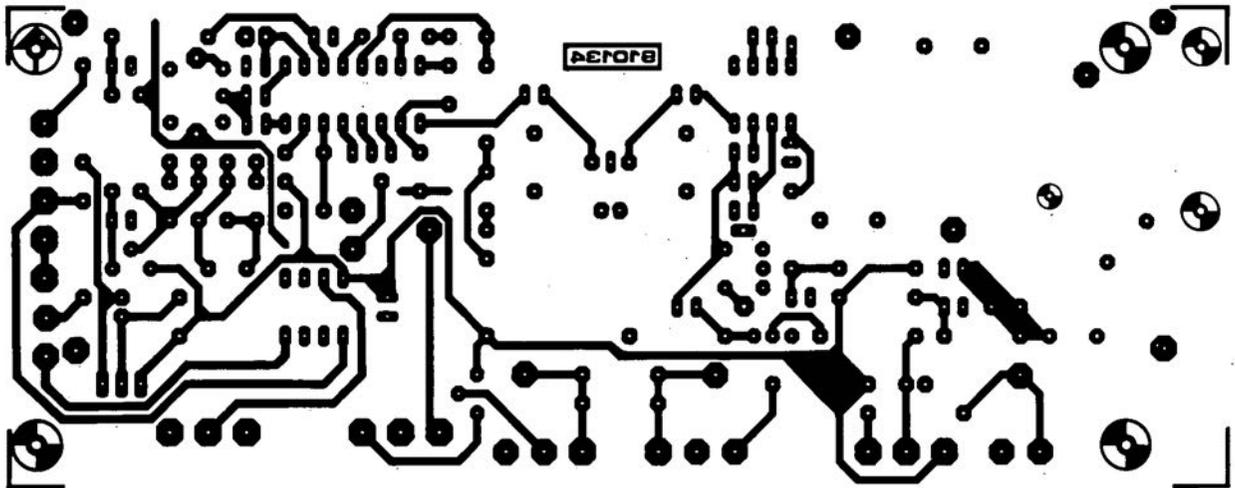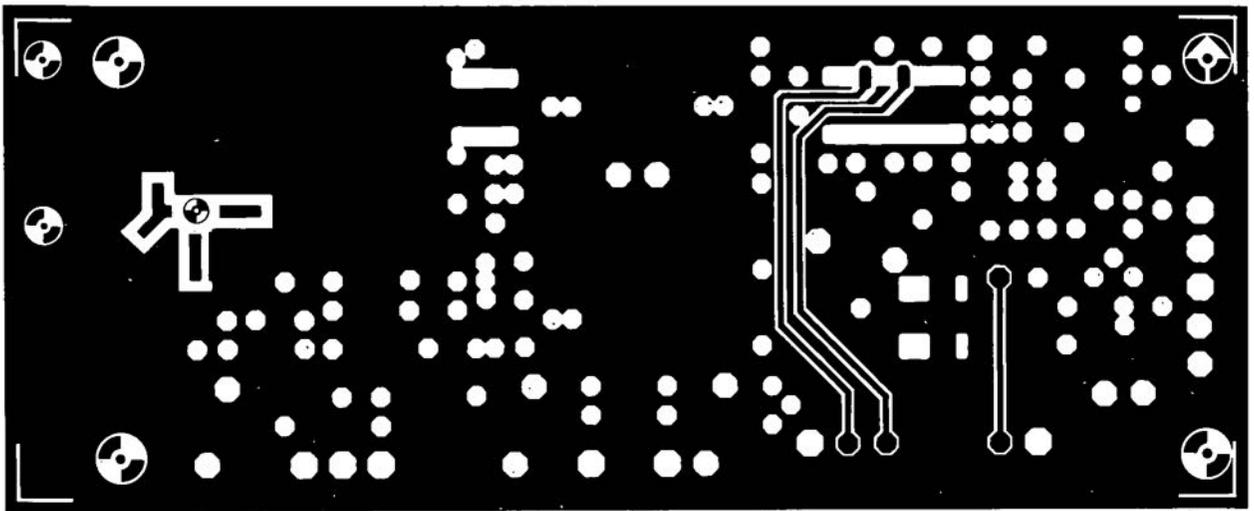
Fig. 5. Component side and solder side layouts (mirror images), and component mounting plan of the PCB for the 2-metre receiver.

8051/8032 ASSEMBLER COURSE

PART 3: HARDWARE EXTENSIONS FOR THE 80C32 SBC

glolog- II !

N.B.

by Dr. M. Ohsmann

After our first dealings with programming in assembly language, we now present an intermezzo in the course. Some useful hardware extensions are proposed for the 80C32 single-board computer described roughly a year ago in this magazine. All extensions are accommodated on a single printed circuit board.
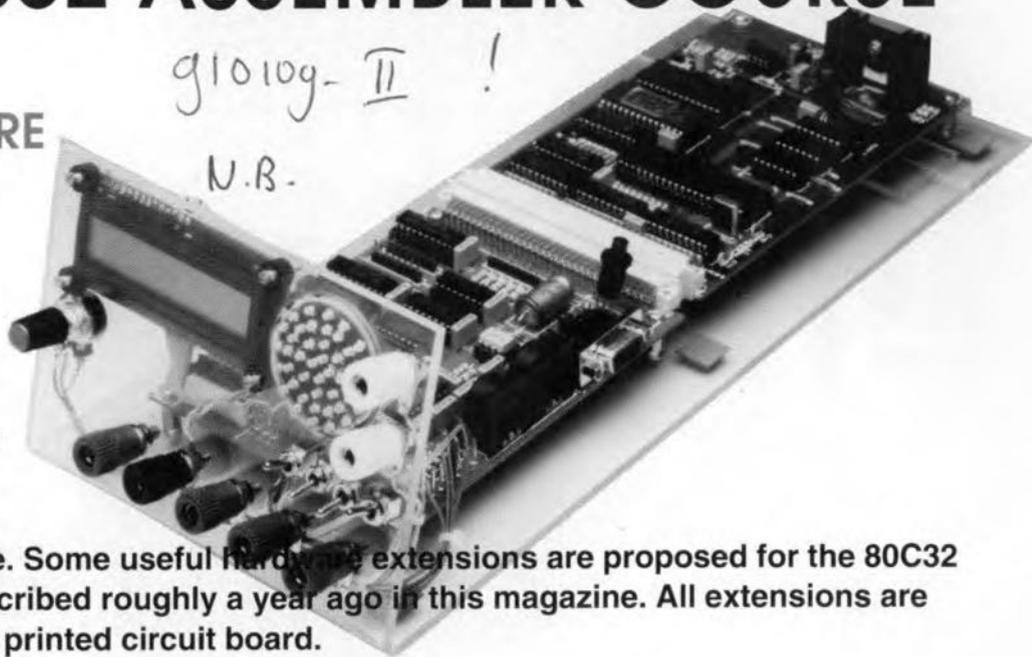
The extension board is simply connected to the 64-way DIN a-c plug on the single board computer (SBC). All inputs and outputs of the present extension card are conveniently located at the edge of the PCB, and have suitable connectors where these are useful. The combination of the SBC and the extension card forms a simple and versatile microcomputer system based on a MCS52 microcontroller IC. The many possibilities of the extension card will be discussed with reference to the circuit diagram in Fig. 11.

The interfaces

Reset
Push-button S1 resets the SBC. After a reset, all four LEDs D1-D4 light. When the SBC runs the courseware monitor program, EMON51, the reset key must be pressed before a download operation to start the monitor.

Serial interface
The SBC has a serial interface that can be used to link the board to a terminal (or 'console') or the RS232 port of a PC running communication software. The interface transmits data via the TxD line (pin c8 on the 64-way DIN plug), and receives data via the RxD line (pin c7). The link to a PC is readily made by connecting TxD, RxD and ground to the appropriate pins of a 9-way sub-D connector, and fitting jumper JP1 in position 'A', and jumper JP2 in position 'B'. With some other applications, the TxD and RxD lines of the SBC may be used for MIDI communication, in which case the jumpers must be removed altogether.

Port P1
The bidirectional driver used on port P1 of the SBC allows the whole port to be used as an input or an output only, i.e., input/output programming of individual lines is not possible. On the extension board, port P1 is used as an output. The port line functions are listed in Table 1.

Table 1. Port P1 bit functions

P1.0	Serial output (JP1=B), or MIDI (JP3=B)
P1.1	Loudspeaker output
P1.2	Positive edge triggers monostable IC8a
P1.3	Not used
P1.4	LED D1
P1.5	LED D2
P1.6	LED D3
P1.7	LED D4

MIDI input
Socket K6 supplies the MIDI signal to a fast optocoupler, IC7. The output signal of the optocoupler is fed to jumper JP2 via a Schmitt-trigger. When the MIDI is used, jumper JP2 must be set to position 'A' to enable the MIDI signal to be conveyed to the serial interface of the SBC. In some cases, voltage divider R20-R21 on the SBC may attenuate the signal to the extent where it is no longer TTL-compatible. Should this happen, R20 may be reduced to 1 kΩ. Fortunately, this was not necessary on our prototype.

MIDI output
Jumper JP3 allows you to determine which signal is taken to the MIDI output, socket K5. In position 'A', the TxD signal of the serial interface on the SBC is used, in posi-

tion 'B' bit 0 of port P1. The latter option may be useful when the internal serial interface of the 80C32 is used for other functions. The MIDI output signal on P1.0 is then generated by software simulating a serial output device.

Memory-mapped I/O
The SBC reserves the address range above 0C000H in the external data memory for input/output operations. Decoders IC1 and IC2 'map' the address range as shown in Table 2.

Table 2. Address functions in I/O range

C000H	Read:	data in latch IC9
	Write:	value to DAC
C001H	Read:	LCD command status
	Write:	LCD commands
C002H	Read:	data in IC3
	Write:	data to IC5
C009H	Read:	data from LCD
	Write:	data to LCD

These options can be used for the I/O functions listed below.

D-A and A-D converter
Resistors R12-R26 and R31 form an *R-2R* network that functions as a digital-to-analogue (D-A) converter in combination with IC9 and IC6a. The content of latch IC9 (which is addressable at 0C000H) is available as an analogue value at the output. The maximum value of the output voltage is reached when IC9 contains 0FFH, which corresponds to about 2.5 V. The D-A out-

put voltage is also applied to comparators IC6b, IC6c and IC6d. These allow the output voltage to be compared to three levels at the analogue inputs. The comparator outputs may be read via address 0C000H, which creates a simple 3-input ADC. The individual functions of the ADC bits at 0C000H are listed in Table 3.

Keys and monostable

The functions of the remaining bits stored at address 0C000H are shown in Table 3.

As you can see, four switches (or pushbuttons) are available for your own applications, e.g., for starting certain functions. Monostable IC8a makes it possible to implement a simple capacitance meter. The capacitor to be measured is connected to K9. Software is used to trigger the monostable via bit 2 on port P1, and then read the time that lapses before the monostable toggles again. This can be monitored by reading bit 3 at address 0C000H. See also the assembler file EBTST6.A51 on your course disk!

Table 3. I/O bit functions

Read IC10; address = C000H

Bit 0:	High when U_{in} (input 1) > U_{DAC}
Bit 1:	High when U_{in} (input 2) > U_{DAC}
Bit 2:	High when U_{in} (input 3) > U_{DAC}
Bit 3:	High when monostable active
Bit 4:	High when key S5 not pressed
Bit 5:	High when key S4 not pressed
Bit 6:	High when key S3 not pressed
Bit 7:	High when key S2 not pressed

Parallel 8-bit input/output

The eight logic levels (bits) at connector K3 may be read at address 0C002H. The same address is also used to output 8-bit datawords via latch IC5 and connector K4. This creates byte-wide input/output interfaces.

LC display

A liquid crystal display (LCD) may be connected to K1. The LCD types that may be used, and their connection details, are shown in the inset. Although the control signals generated by the extension board do not meet the exact timing requirements of the LCDs, they caused no problems in our set-up. The timing may be more critical, however, with displays other than the types listed. The LCD signals (on connector K1) and their functions are listed in Table 4.

Power supply

The extension board is conveniently powered by the 5-V regulator on board the SBC. Make sure that the regulator is sufficiently cooled when further loads such as LEDs or relays are connected.

Construction and test

The construction of the extension board is mostly straightforward soldering work.
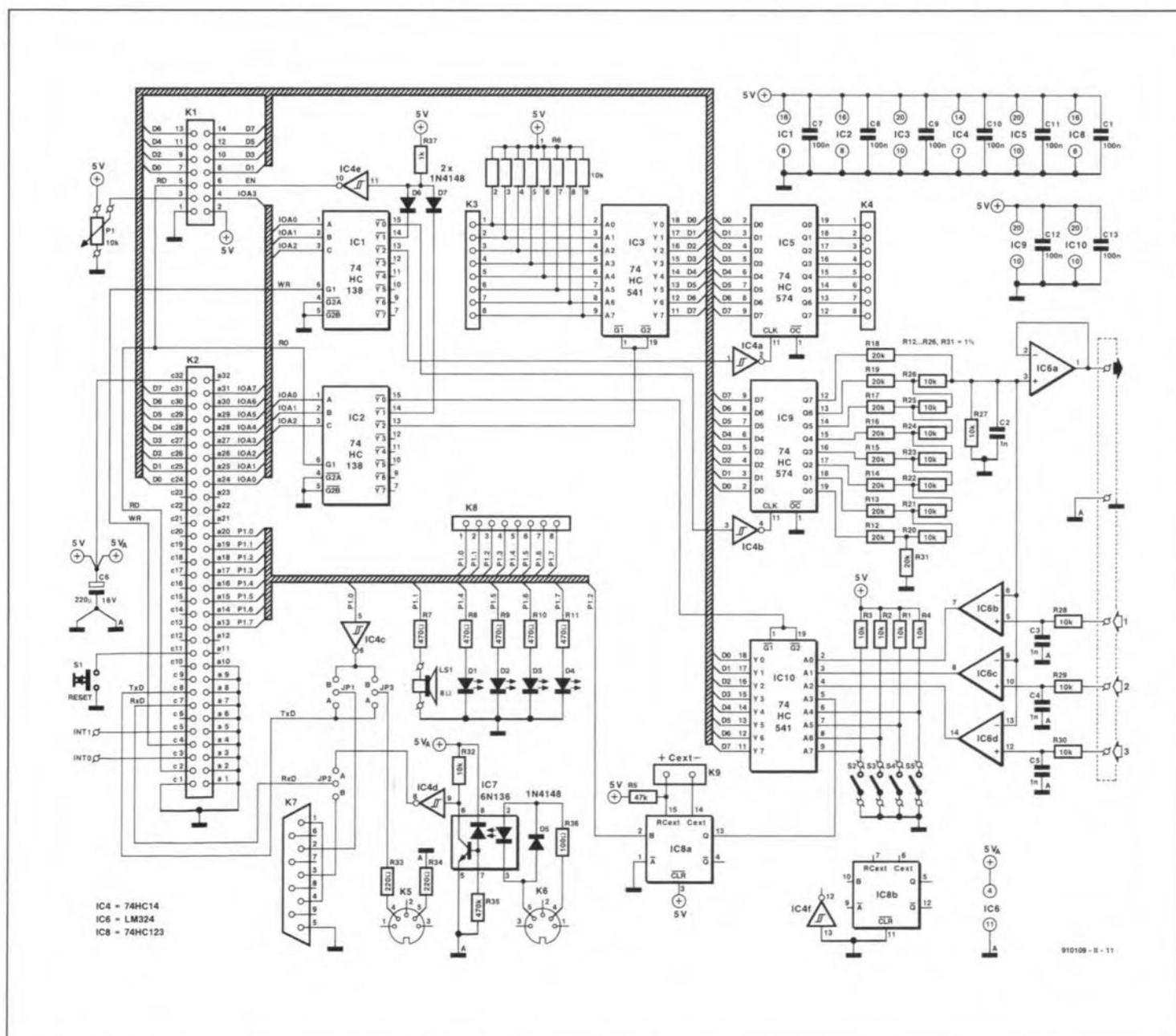
Fig. 11. Circuit diagram of the extension board for the 80C32 single-board computer.
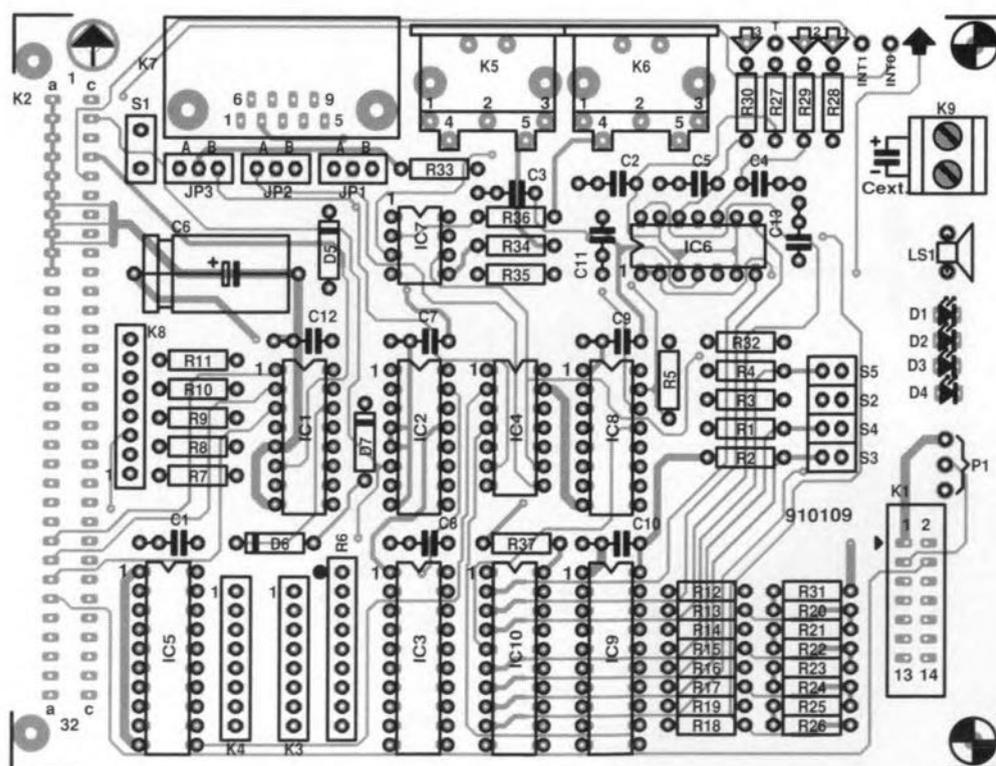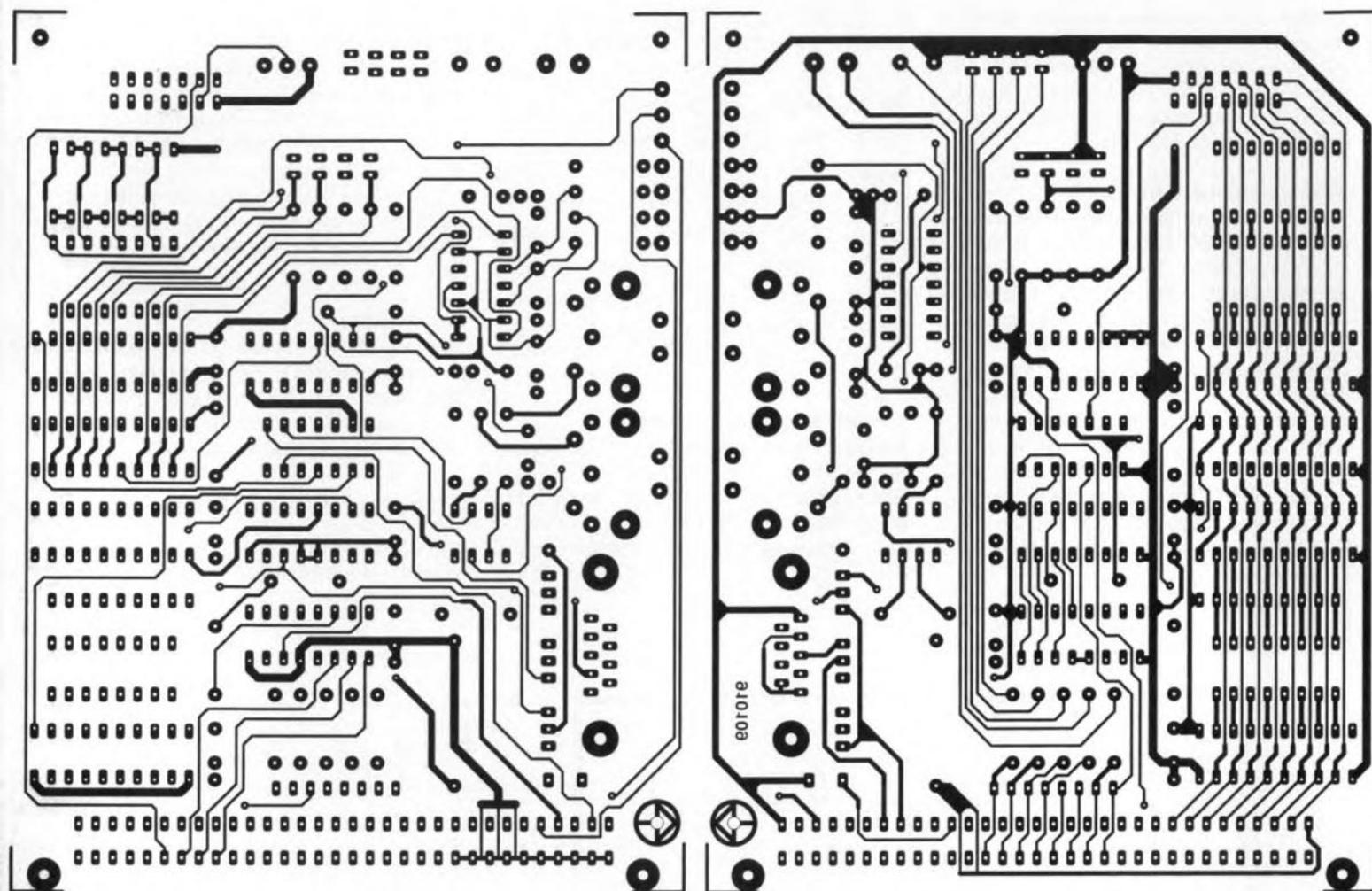
Fig. 12. Track layouts (component side and solder side; mirror images) and component overlay of the printed circuit board.

COMPONENTS LIST

Resistors:

9	10kΩ	R1-R4;R27-R30; R32
1	47kΩ	R5
1	8-way 10kΩ SIL	R6
5	470Ω	R7-R11
9	20kΩ 1%	R12-R19;R31
7	10kΩ 1%	R20-R26
2	220Ω	R33;R34
1	470kΩ	R35
1	100Ω	R36
1	1kΩ	R37
1	10kΩ linear	P1

Capacitors:

8	100nF	C1;C7-C13
4	1nF	C2-C5
1	220µF 16V	C6

Semiconductors:

4	rectangular LED	D1-D4
3	1N4148	D5;D6;D7
2	74HC138	IC1;IC2
2	74HC541	IC3;IC10
1	74HC14	IC4
2	74HC574	IC5;IC9
1	LM324	IC6
1	6N136	IC7
1	74HC123	IC8

Miscellaneous:

1	14-way box header	K1
1	64-way a-c row, female, angled, DIN	K2
3	8-way pin header	K3;K4;K8
2	5-way PCB-mount DIN socket	K5;K6
1	9-way PCB-mount female sub-D connector	K7
1	2-way PCB-mount terminal block, pitch 5mm	K9
1	Push button SPST	S1
4	Switch SPST	S2-S5
1	8Ω miniature loudspeaker	LS1
1	Printed circuit board	910109

Table 4. LC display connections

Pin	Function
1	Ground
2	+5 V
3	Contrast (adjust with P1)
4	RS; register select = IOA3 0 = command 1 = data
5	RD; read (active high) 0 = write 1 = read
6	E; enable (active high when address selected) 0C001H = command transfer to/from LCD 0C009H = data transfer to/from LCD
7 to 14	Databus bit 0 to 7

LCDs: types and connections

Type	Lines × characters	Manufacturer
H2570	1 × 16	Hitachi
H2572	1 × 40	Hitachi
LM016L	2 × 16	Hitachi
LM018L	2 × 40	Hitachi
LM038L	1 × 20	Hitachi
LM1612A	1 × 16	Sharp
VK2116L	1 × 16	Vikay
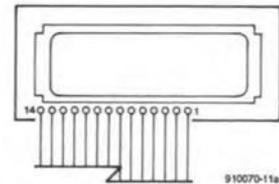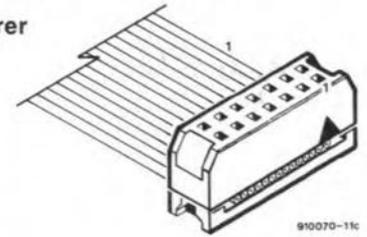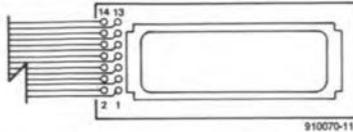
An LCD module has 14 connections, arranged in a single row of solder points, or in two rows of 7 at either side of the PCB. It is best to solder these points directly to a piece of 14-way flatcable. Pin 1 is marked by a '1' on the display board. Attention: when there are two connection rows, the solder points are numbered in pairs (see drawing above).
The wire numbers 1-14 at the other end of the flatcable are connected to the corresponding pin numbers on header K1 on the extension board via an IDC socket (see drawing). Wire '1' in the flatcable should go to the side with the marker on the IDC socket as shown.

The artwork of the double-sided PCB is shown in Fig. 12. It is recommended to use IC sockets because the board will be connected frequently to experimental circuits, which may not work as expected, and damage ICs on the extension board quite easily. Along the same train of thought, it is better not to fit the SBC and the extension board in an enclosure. The introductory photograph shows our prototype with the two boards fitted on a length of perspex—a readily accessible system!

Although you may follow this course without building the proposed hardware extensions, it must be noted that the programming examples that make use of the added hardware (files EBTST*.* on the course disk) are an excellent introduction to practical harware-software interfacing, ranging from simple input/output devices (push-buttons and LEDs) to more complex applications: a capacitance meter, ADC and DAC control, and, of course, LCD control.

Likewise, some of you may be interested in the present hardware only to extend the possibilities of the 80C32 computer or a similar MCS52 microcontroller system. The following procedure is recommended to test the extension board if this is used independent of the programming course. First, test the output function of port P1. This is easiest done by driving the loudspeaker, and making the LEDs flash. Next, check the function of the serial interface after fitting the jumpers appropriately. Proceed with the DAC: output a sawtooth via address 0C000H, and use an oscilloscope to check the waveform and the peak amplitude (approx. 2.5 V). Apply a test voltage between 0 V and 2.5 V to the analogue inputs, and check the function of the comparators by reading the data at ad-

dress 0C000H. The correct function of keys S2 to S5 is verified similarly. Next, carry out a couple of read and write operations to and from 0C002H to check that the parallel input/output interfaces (K3 and K4) work. Finally, test the LCD and the MIDI interface with the aid of small programs. Suitable examples to do so may be found on the course disk.   ❏

Next time: we continue the course with assembly language programming.

JOIN THE COURSE!

What you need to follow this course:

- a 8032/8052AH-BASIC single board computer as described in Elektor Electronics May 1991. The preferred CPU is a 8051 or a 80C32. Alternatively, any other MCS52-based microcontroller system (but read part 1 of the course);

- a course diskette (order code ESS 1661) containing programming examples, utilities, and an assembler;

- a monitor EPROM (order code ESS 6091).

- an IBM PC or compatible operating under MS-DOS, or an Atari ST with a monochrome display.

Appeared so far:
Part 1: Introduction (February 1992);
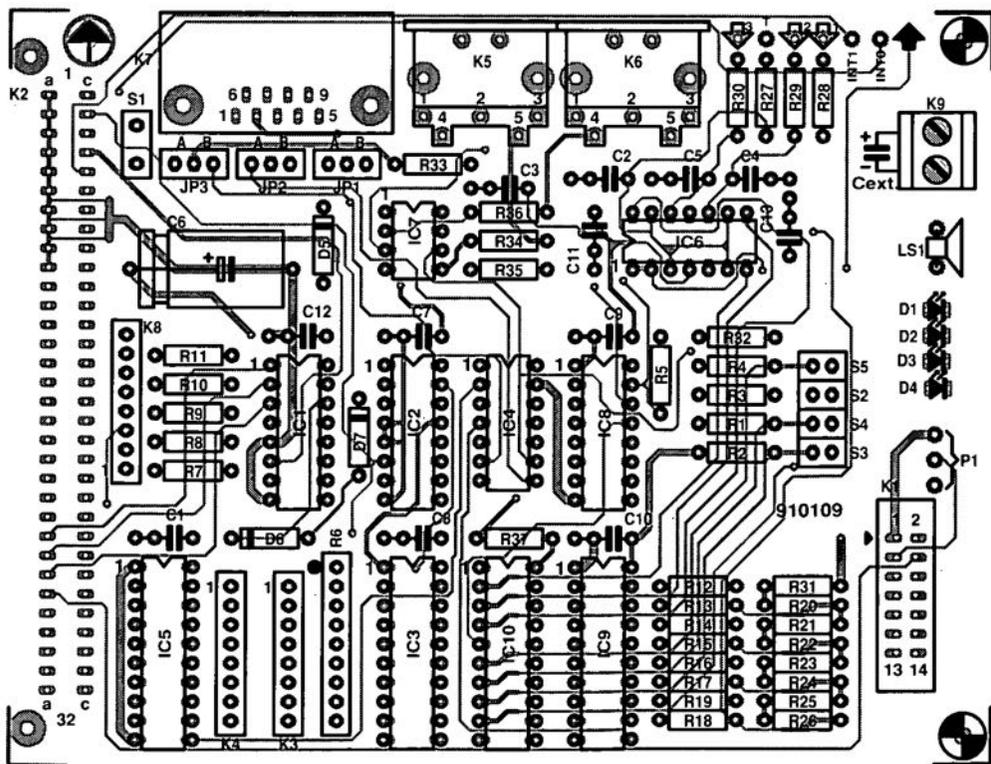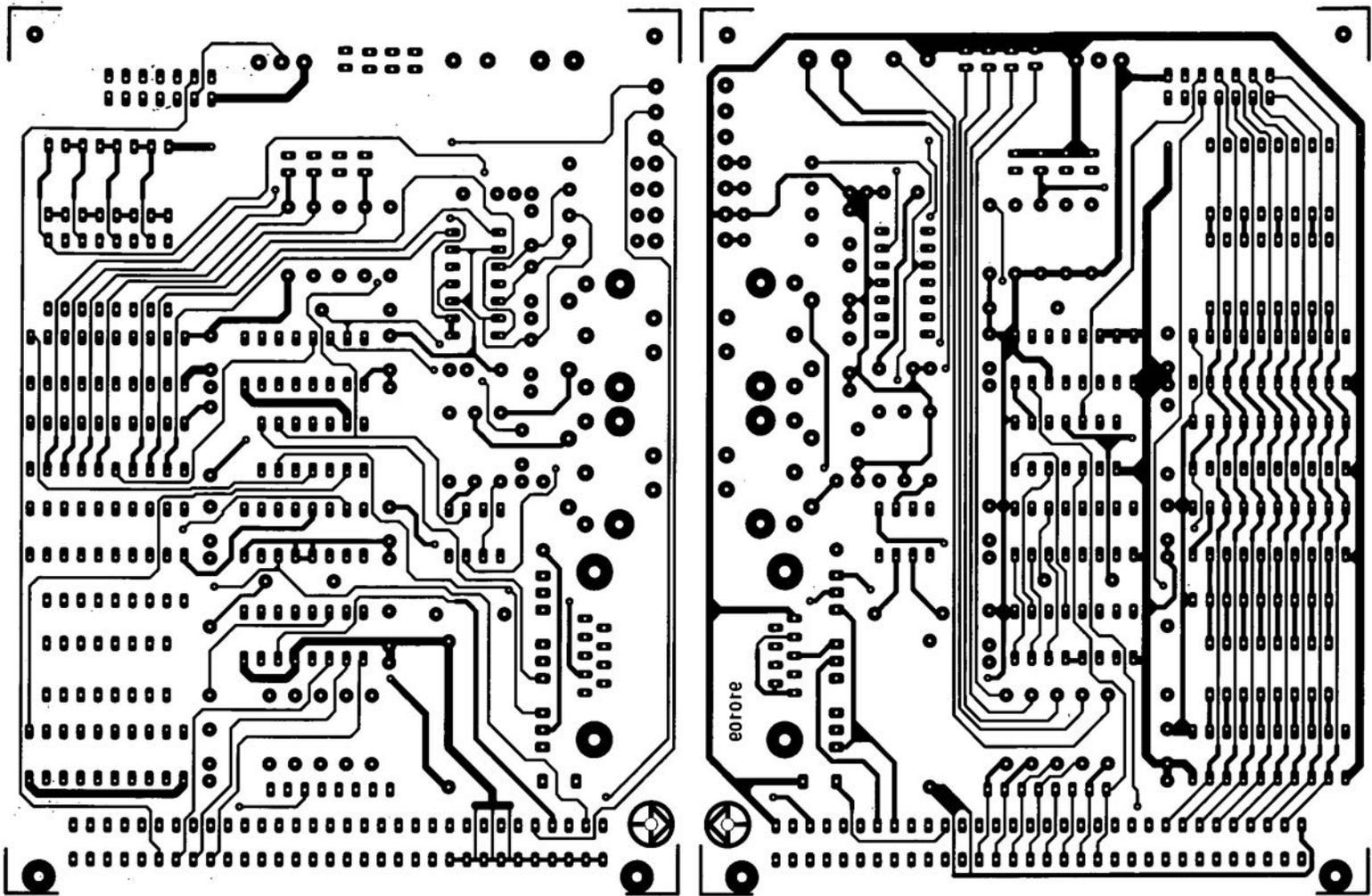Part 2: First 8051 instructions (March 1992).

Fig. 12. Track layouts (component side and solder side; mirror images) and component overlay of the printed circuit board.

PULSAR — A REVIEW

g20056

by Mike Wooding G6IQM

DESIGNERS of digital equipment are fully aware of the difficulties of testing their designs to confirm that the logic of the design works according to plan. Even more difficult, rather as with computer programs, is the ability to conduct the infinite number of tests to prove that there are no bugs or glitches in the design some of which may only appear when an unusual set of conditions exists, or perhaps only once every billion clock pulses or so.

Furthermore, it is very expensive in time and labour to build breadboarded prototypes to conduct the tests on. The probability of destroying expensive digital devices is even more off-putting! However all is not lost! A recent addition to the professional software packages produced by Number One Systems Ltd. is 'PULSAR' a **digital logic circuit simulator program**.

Pulsar is a full featured simulator that allows designs to be tested without the need of constructing those expensive breadboards and prototypes. The circuit design can be tested on your PC and modifications made until the circuit functions as required — all without using a soldering iron in anger, or blowing up any expensive ICs.

Pulsar

Pulsar is a digital logic circuit analyser program that runs on PC/XT/AT/286/386/ or 486 computers running under MS-DOS 3.0 or later and with either EGA or VGA graphics, preferably colour. The minimum

RAM requirement is 512 KBytes, and the software is supplied on both 5.25" and 3.5" format floppy discs.

It is almost imperative to have a hard disk drive, as the program keeps a high proportion of its temporary data on disk during operation, and if using a floppy-only based machine the operation of Pulsar will be extremely slow.

The program also supports the use of a mouse and a choice of either 9 or 24-pin dot-matrix printers or HP Laserjet II printers.

The user manual

The comprehensive user manual is packaged in an A5 ring binder, which will allow for the easy insertion of upgrade instructions, personal notes, etc. The opening pages of the manual deal with the installation and running of the program.

The next section in the manual is called 'First Impressions' and gives an overview of the screen presentations and some of the basic commands used to manipulate these screens and move around in them. Once the user is familiar with these basic commands then it's on to the next section, 'The Grand Tour'.

The 'Grand Tour' comprises the greater part of the user manual and takes the user through a step-by-step simulation; from entering the initial design netlist, to the final proven circuit. To assist with the instruction, a predesigned divide-by-three circuit is used as a practical example, from

which a netlist is compiled.

Note: a netlist is simply a file of logic connections between the various devices within a digital circuit and their relative logic states. The libraries available within Pulsar contain netlist outlines for basic logic gates, 74LS series and 4000 CMOS series devices.

After the chapter dealing with the netlist editor and the making of a netlist for the circuit, the section explaining how to actually run the analyser is reached. Firstly, selecting a signal source, or generator, for the input, is dealt with and then a detailed look at the simulated circuit follows.

The 'Grand Tour' then goes on to deal with modifying the circuit to correct any faults, creating generators, selecting printers, combining circuits and using the libraries.

The remaining sections of the user manual deal with customising Pulsar to your exact requirements, using DOS within the program and using the DOS shell. Finally, there are lists and explanations of the three built-in libraries of Pulsar, which will be discussed later.

The analyser

Once a circuit netlist has been created and a suitable generator selected, Pulsar simulates the circuit operation and displays on the screen a timing diagram, such as one sees on a conventional logic analyser. As with a conventional logic analyser, one can also see if any spurious signals are present on the timing waveforms. However, here the similarity really ends.

The display screen is divided into three main areas. The top of the screen contains the main menu, showing Pulsar's top-level commands, with the currently active mode highlighted. The program defaults to the analyser mode on start-up. The other modes are:

Configuration	Customises Pulsar.
Generators	Sets up Pulse Generators.
Libraries	Maintains Component libraries.
!DOS	Manipulates Files and Directories
F1Help	On-line help information.
Quit	Leave Pulsar.

Also shown in the menu area are the file name and cursor control characters.

Configuration: this command selects a set of menus which allow the default parameters for Pulsar to be set according to the users choice. The default search paths for
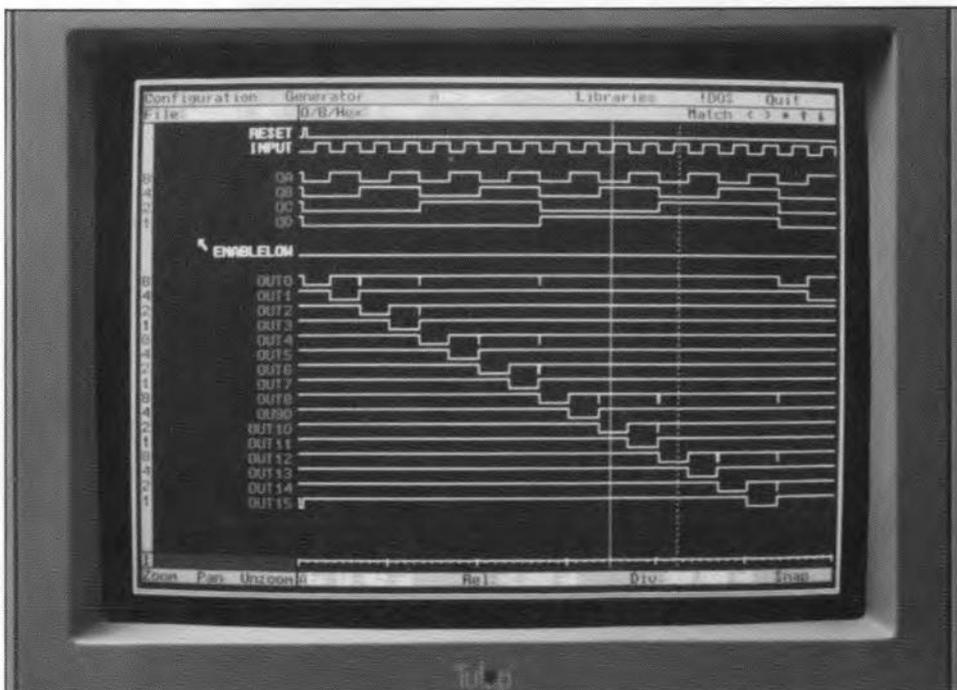
files, the time and date format, etc., can all be preset by the user and the configuration saved.

Generators: this menu allows generators (input signals) to be modified or developed according to the requirements of the simulation.

Libraries: the library command allows the various libraries to be scanned and manipulated.

!DOS: selecting this command displays a menu of basic DOS commands which are available for use without leaving Pulsar. Also selectable is a DOS Shell, which allows you to exit Pulsar to the DOS prompt, but without losing any data currently held in Pulsar. Quitting the DOS Shell returns you to Pulsar, exactly where you left it.

F1HELP and **Quit** are self-explanatory.

The main area of the screen is devoted to the analyser display, with the two moveable cursors.

At the bottom of the screen is a sub-menu of control commands and the time readouts for the cursor positions and the time scale factor of the display area.

With Pulsar you are not limited to how many pods (connecting ports) are available (conventional logic analysers have 8 or 16, sometimes 32, but we are talking expensive here!), as the display shows all the input, clock and output waveforms detailed in the netlist. If you want to see the timing diagram at a particular point in the circuit, you simply add it to the netlist.

Furthermore, another feature of Pulsar which makes it superior to a conventional analyser is that it is not limited to a window in time; i.e., conventional analysers are, to all intents and purposes, not real-time machines, the display is limited to a particular period of time. However, with Pulsar the simulation is continuous, and you can zoom in or out in time, so that even glitches that occur very seldom can be captured.

n essential feature of the zoom facility is that, because you can expand the displayed time zone down to a few nanoseconds if you wish, the actual widths of any glitches or pulses can be measured accurately. To enable this to be achieved Pulsar has two moveable cursors on the display; an 'Absolute' one and a 'Relative' one. Both cursors are easily positioned anywhere on the display by simple keyboard/mouse actions, and at the bottom of the display time values for each cursor are displayed.

The 'Absolute' cursor time display is given as the cursor position in time from the start of the simulation. The 'Relative' time display is given as the difference in time, positive or negative, between the two cursors.

Thus, by positioning the 'Absolute' cursor at the start of a pulse or whatever, and then positioning the 'Relative' cursor at the end of the pulse or zone to be measured, the pulse width or the elapsed time can be read directly. Facilities to enable quick positioning of the cursors are available. A 'Snap' command will ensure that the cursor being moved will align itself exactly with the nearest leading/trailing edge to the mouse/keyboard pointer when moved. A 'Scroll' facility is also available to quickly move the active cursor (the one selected for moving) across the display. A 'Pan' command always centres the display around the currently active cursor, so that when zooming in or out the selected area of the display will always be visible.

An important aspect of Pulsar is the ability to define the signal source, or generator. From a simple 50:50 mark:space square wave at any defined frequency, to an extremely complicated pulse train can be used. When specifying the generator, simply typing anything beginning with a number and containing the letters 'HZ' is interpreted as a simple frequency generator. Typing in anything else will prompt Pulsar to search for a generator file with that name.

Complex generators can be created in the Generator screen and saved with an appropriate file name for use whenever required. Generators in use at any time can be modified in the generator screen, and the effect of the changes on the circuit under analysis displayed immediately on the analyser display screen.

There are more features of Pulsar than I have covered here, but to attempt to explain them and their uses is somewhat pointless as you really need to have Pulsar 'live' in front of you to understand their actions. Suffice it to say that they are well explained in the user manual.

The libraries

As I mentioned earlier there are three inbuilt libraries in Pulsar, which make the creating of netlists much quicker. The libraries are:

1. PRIM.LIB; a library of primitive logic elements, such as buffers, inverters, AND gates, OR gates, latches, etc.

2. 74LS(1).PLB AND 74LS(2).PLB; a library of over 120 component models covering the low-power Schottky TTL family.

3. 4000.PLB; a library of over 90 component models covering the 4000 CMOS family.

When building up netlists for a circuit, then by naming the component type being used, Pulsar responds by reading the pin and parameter information from the library for the device. All you have to do is enter the various connection details.

Circuit blocks previously designed and tested can be added to the libraries, which is a useful feature if you are using a common circuit time and time again.

A useful feature of the basic logic elements found in the PRIM.LIB is that the transition delay through an element can be varied to emulate circuit and design conditions. A sub-menu from the Generator menu gives various delay parameters that can be modified. A feature of the delay modifiers is that the delays, both minimum and maximum, can be set to values which exceed the nominal values for the device(s) in the circuit. Another useful feature is that the delays can be modified on a global basis, thus allowing the simulation of the circuit to show the results of using different families of logic devices.

Conclusions

Creating a netlist for a circuit design is not as daunting as it may first appear, and never having done so before I followed the instructions, and in a very short time got to grips with the concept and created the netlist for the example circuit. Following the instructions I then connected my generator. Pulsar simulated the circuit and presented the results on the screen.

Upon running the analyser and playing with the many and varied features, it soon became evident that the facilities available are quite extensive. The versatility of the package as a design testing tool is unquestionable. Having used conventional logic analysers in the past I can imagine that in a development environment Pulsar would be far more ideal. The fact that a design circuit does not actually have to be built would be one great advantage. That, coupled with the ability of Pulsar to detect glitches down to 1 picosecond per week for example, proves that the system is a must for digital designers.

Although I barely scraped the surface of Pulsar's capabilities, I can recommend it to anyone engaged in digital design and testing work. Armed with his/her trusty PC and this software, a designer should be able to clear all but the most deeply nested bugs in any complex logic circuit. Highly recommended. ∎

MOTOR SPEED LIMITER

Design by K. Walraven

Small, compact motors as used in circle saws, lawn mowers and other small electric tools burn out when overloaded. Before that happens, its speed will drop appreciably. If, therefore, the speed is monitored carefully by the circuit described here, burning out of the motor may be prevented.

SMALL motors used in domestic tools are often required to carry out tasks for which they were not designed: a lawn mower mowing a lawn that should have been done a month previously; a circle saw that uses a blade that should have been replaced a dozen or more kerfs ago. As a consequence, the motor is overloaded and gets hot. The thermal protection, if fitted, is then actuated and the motor must be given time to cool off. In many apparatuses, the thermal protection is not close to the motor, but elsewhere in the appliance where it monitors the motor current. Since that current increases proportionally with the load, overload can, indeed, be detected this way.

However, this arrangement does not monitor the temperature of the motor, so that consequently the motor still overheats in spite of three or four cooling-off periods. Nevertheless, the thermal protection will enable the motor (since the current has dropped to a 'safe' value) and the result is often that after a little while the insulation of the copper wire in the motor gives up the ghost. In general, that means that the motor is a write-off; it can be rewound, but that is usually almost as expensive as a new motor.

The circuit described here ensures that the situation does not develop to its fatal end. Even before the motor begins to get warm, the protection becomes active, because it monitors the speed of the motor with the aid of an electronic sensor. When the speed drops as a result of overload, an alarm indicator is actuated. If the user ignores this, the motor is switched off automatically. This ensures that, provided the circuit is set up properly, the motor can never get too hot.

Circuit description

The circuit in Fig. 1 was designed in the first instance for use with squirrel-cage motors that have a nominal speed of 2600 rev/min. Under no-load conditions, this speed will rise to about 2900 rev/min. Below 2500 rev/min, the motor is clearly overloaded and will get warm. There are, of course, squirrel-cage motors with a different nominal speed: for these, the parameters of monostable IC_{1b}-IC_{1c} must be altered slightly. The same applies to the small series-motors used in electric hand-tools. The nominal speed is invariably marked on the housing of the appliance.

Sensor IC_3 is a reflection sensor that de-

tects the passing of a white dot that the user must place on the motor spindle. Every time the light of the LED reflected by the white dot falls on to the sensor, the motor has travelled one revolution. This (reflected) light causes the sensor's transistor to conduct briefly, whereupon the transistor's collector potential drops. This voltage pulse is converted into a digital pulse by network T_1-IC_{1a}-R_2-R_3-C_1, which is used as a clock for IC_{2a}. A nominal motor speed of 2500 rev/min (which is a normal speed of motors running with a nominal load) corresponds to a pulse rate of about 42 Hz (period=24 ms).
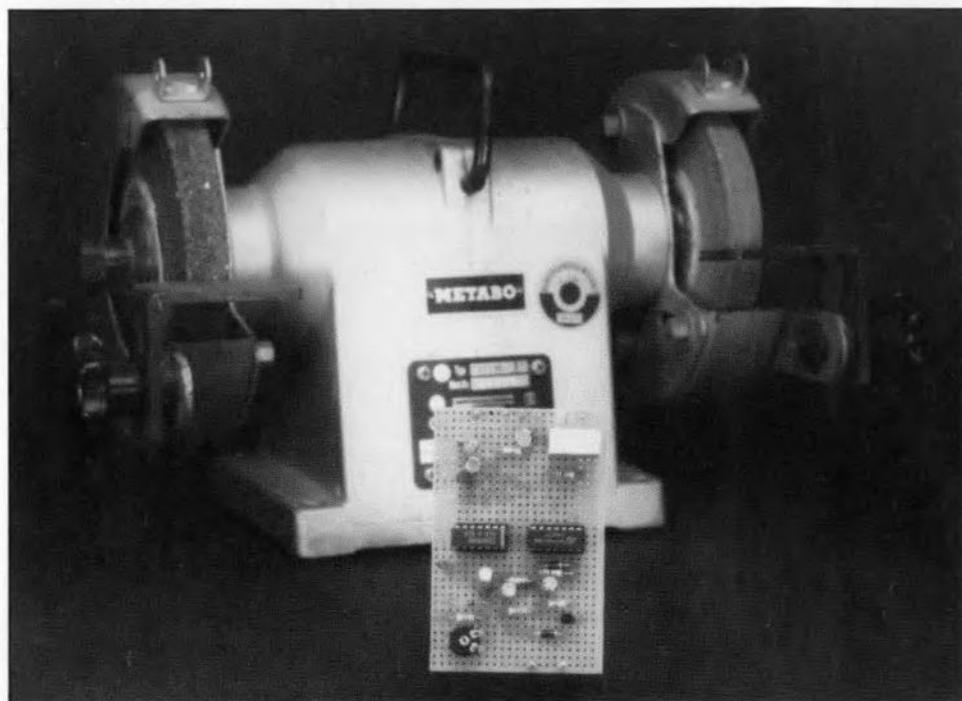
Since the duty factor depends, among others, on the width of the white dot, the signal is divided by two by bistable (flip-flop) IC_{2a}. The output signal of this bistable is a square wave.

Gates IC_{1b} and IC_{1c} form a monostable, whose period is determined by C_2-R_4-P_1. The time during which the output of the monostable is low is set by P_1: a good, practical value when a motor with a minimum speed (overload limit) of 2400 rev/min is used, is about 24 ms.

The output of the monostable is processed by comparator IC_{2b}. The monostable clocks the bistable at a first transition (rising edge). If the input to the bistable at that instant is still high, its Q output also goes high. This

PARTS LISTS

Resistors:
R1 = 330 Ω
R2 = 470 kΩ
R3 = 2.2 MΩ
R4 = 10 kΩ
R5 = 10 MΩ
R6 = 3.9 MΩ
R7 = 1 MΩ
R8 = 220 kΩ
R9 = 220 Ω
P1 = 25 kΩ

Capacitors:
C1 = 1 µF, 63 V
C2 = 2.2 µF, 63 V
C3, C6 = 1 µF, 63 V
C4 = 1 µF
C5 = 10 µF, 63 V

Semiconductors:
D1–D3 = 1N4001
D4 = LED
T1 = BC560C
T2 = BC517
IC1 = 4093
IC2 = 4013
IC3 = CNY70

Miscellaneous:
S1 = SPST switch
Re1 = 12 V/10 A coil, c/o contact

indicates that the motor speed has dropped too low and that an error message must be given. The exact motor speed at which an error must be indicated can be set with P_1. The longer the mono-time, the lower the motor speed can drop before an error is indicated.

When the supply voltage is switched on, the comparator, IC_{2b}, is reset automatically, so that power can be supplied to the motor. If the motor takes longer than eight seconds (standard) to come to full revs, some extra seconds can be obtained by pressing reset switch S_1. As long as that switch is operated, the protection circuit cannot disable the supply to the motor.

Networks R_8-C_6 and R_5-C_3 integrate the output of the bistable in the comparator. If the error persists for more than two seconds, the alarm indicator, D_4 will light, and after eight seconds, the motor is switched off altogether. In this way, it should be virtually impossible for a motor to burn out. But . . .

Construction

The circuit is best constructed on a small prototyping board. The reflection sensor must be mounted in the motor housing close to the spindle. The distance between the white

dot and the detector must not exceed a few millimetres. If the spindle is a light colour, so that a white dot would not give enough contrast, try a black dot, or make the spindle black (black insulation tape). Use screened cable to connect the sensor to the circuit to prevent the circuit action being degraded by noise pulses emanating from the motor.

It is also possible to use an optocoupler as the light barrier. A disc with a hole in it must then be mounted securely on to the motor spindle. At each and every revolution of the motor, the LED will then briefly illuminate

the phototransistor. As with the reflection sensor, the optocoupler provides the necessary pulses for proper operation of the circuit.

Output relay Re_1 is connected between the mains supply and the motor. Extreme caution must, therefore, be observed when the relay is energized: touching the mains supply may be fatal!

Fit the circuit in a small, man-made-fibre case. The circuit can be powered simply via a 9-V mains adaptor. Omission of an on-off switch is deliberate: since the motor runs when the relay is not energized, it is easy to forget to switch on the protection circuit. Therefore, *never* forget to plug the adaptor into a mains socket. It makes good sense to connect the adapter to the mains in parallel with the motor, for instance, by linking it to the supply cable of the protected appliance between the mains plug and the appliance's on-off switch. ∎

Alternative reflection sensors	
Sharp	GP2S04
Toshiba	TLP903
	TLP904
TRW	OPB125A
	OPB253A
	OPW703A
	OPW708
	OPW709
Texas	TIL138
	TIL139

900121 - 11

geen nn!
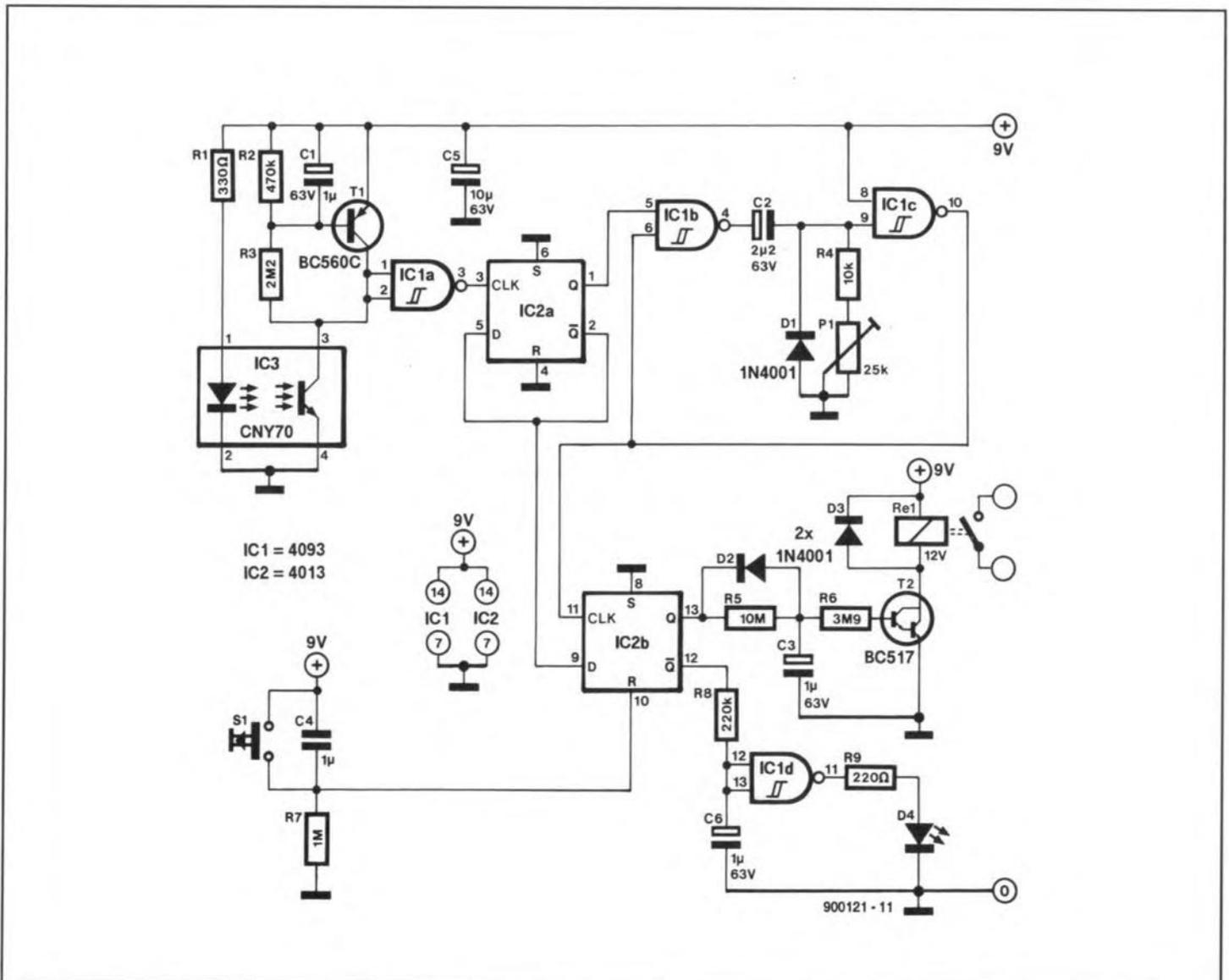
APPLICATION NOTE

The content of this note is based on information received from manufacturers in the electrical and electronics industries and does not imply practical experience by *Elektor Electronics* or its consultants.

LAMP/SOLENOID DRIVER UGQ5140K

THE UGQ5140K unipolar Hall effect switch is a monolithic IC designed for magnetic attenuation of low-power incandescent lamps or inductive loads such as relays or solenoids. Included on the chip is a darlington power output that is capable of continuously sinking more than 300 mA. Internal protection circuitry limits surge (lamp turn-ON) or fault currents to about 900 mA. A sensitive magnetic threshold allows the device to be used in conjunction with inexpensive magnets or in applications that require relatively large operating distances.

Each sensor/driver includes a magnetic
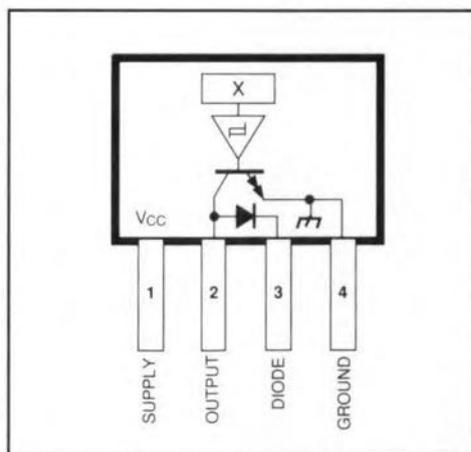
Fig. 1. Pinout viewed from branded side.

sensing Hall voltage generator, opamp, Schmitt trigger, voltage regulator and an open-collector, high-gain darlington power output stage. The regulator allows use of the device with supply voltages of 4.5–28 V. On-chip compensation circuitry stabilizes switch-

point performance over temperature.
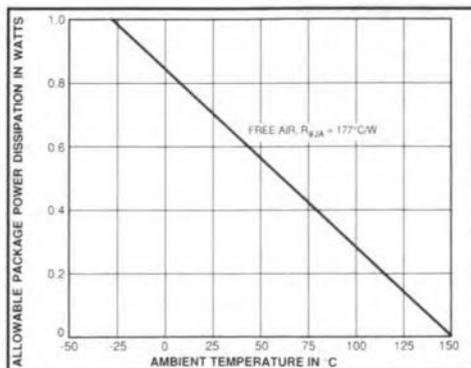
Circuit description

The UGQ5140K merges state-of-the-art Hall effect sensing and power driving technologies to allow precision non-contact actuation of incandescent lamps or inductive loads. It is rated for operation over a temperature range of –40 °C to +85 °C as typically required in automotive applications.

Magnetic operation. As shown in Fig. 3, the output of the device (pin 2) switches low when the magnetic field at the Hall sensor exceeds the operate point threshold (B_{op}). At this point, the output voltage is $V_{out(sat)}$. When the magnetic field is reduced to below the release point threshold (B_{RP}), the device goes high. The difference in the magnetic operate and release points is called the hysteresis (B_H) of the part. This built-in hysteresis allows clean switching of the output even in the presence of external mechanical vibration and electrical noise.

Current and thermal limiting. Output short circuits may be caused by faulty connectors, crimped wiring harnesses, or blown loads. In such cases, current and thermal limit circuitry will protect the output transistor against destruction.

Current through the output transistor is sensed with a low-value on-chip aluminium resistor. The voltage drop across this resistor is fed back to control the base drive of the
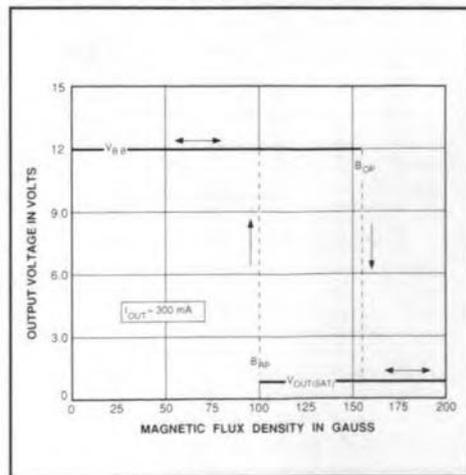
output stage. This feedback prevents the output transistor from exceeding its maximum current density rating by limiting the output current to about 900 mA. It may also the output voltage to increase*. In this mode, the device will dissipate an increased amount of power**, and the output transistor will be thermally stressed. This stress, unless protected against (as in the UGQ5140K), will cause the device junction temperature to rise until it fails catastrophically.

Thermal stress protection is provided in two manners: delta temperature protection and junction temperature protection. Under worst-case conditions (Fig. 4 and Fig. 5) if
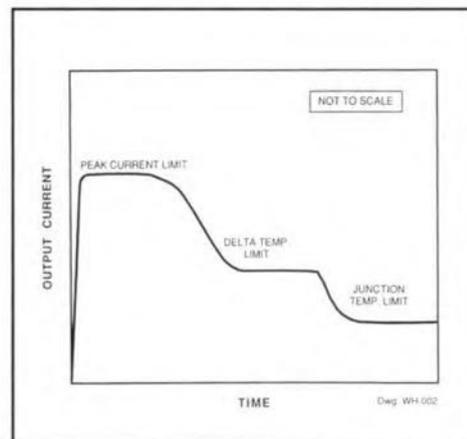

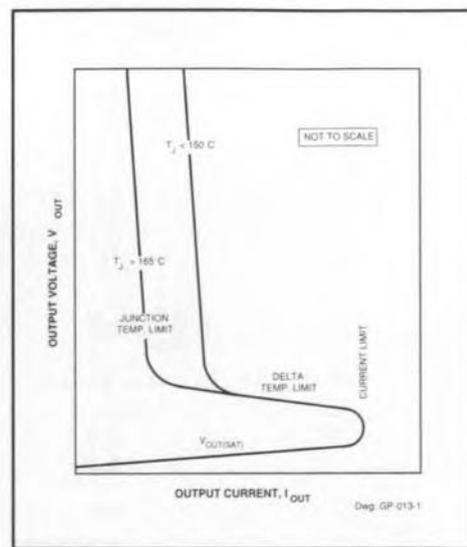**Fig. 4. Output current under short-circuit**
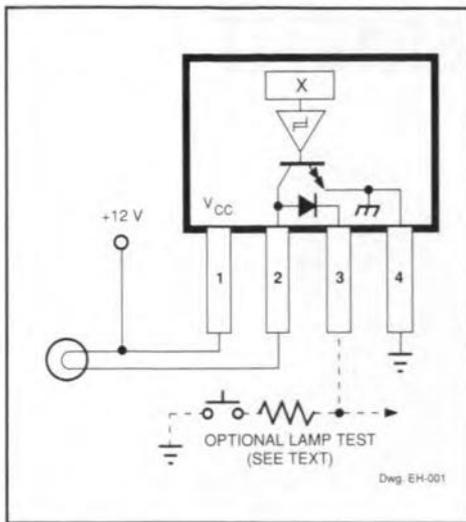

Fig. 5. Output voltage vs output current.

Fig. 2. Allowable power dissipation vs temperature characteristic.

Fig. 3. Typical transfer characteristics at T_A=+25 °C.

Fig. 6. Typical lamp driver application.

Fig. 7. Lamp current vs time.

Fig. 8. Lamp turn-on time.

the output is shorted to supply, the output transistor will heat up much faster than the rest of the IC. This condition could cause localized failure in the output transistor. To prevent damage, a delta temperature limiting scheme is used. If a large thermal gradient is sensed across the device, the output transistor base drive is reduced to lower the output current. This reduces the power (heat) generated by the output transistor.

When thermal stresses cause the junction temperature to reach about +165 °C, a linear thermal limiting circuit is activated. This circuit linearly reduces the base drive of the output transistor to maintain a constant junction temperature of +165 °C. In this mode, the output current will be a function of the heat dissipating characteristics of the package and its environment. Linear thermal limiting eliminates the low-frequency thermal oscillation problems experienced by thermal shutdown (ON-OFF) schemes.

The output characteristics are shown in Fig. 4 and Fig. 5. Note the three distinct op-

erating regions: peak limit, delta limit, and thermal limit. In practice, the output voltage and current may exhibit some oscillations during peak current limiting owing to output load characteristics. These oscillations are of very short duration (typically 50 ms) and may be damped with an external capacitor between pins 2 and 4.

When the fault condition that caused the output overload is corrected, the device returns to normal operating mode.

Typical applications

Incandescent lamp driver. High incandescent lamp turn-ON currents (commonly called in-rush currents), can contribute to poor lamp reliability and destroy semiconductor lamp drivers. Warning resistors protect both driver and lamp but use significant power when the lamp is OFF, while current-limiting resistors waste power when the lamp is ON. Lamps with steady-state current ratings to 300 mA can be driven by the UGQ5140K
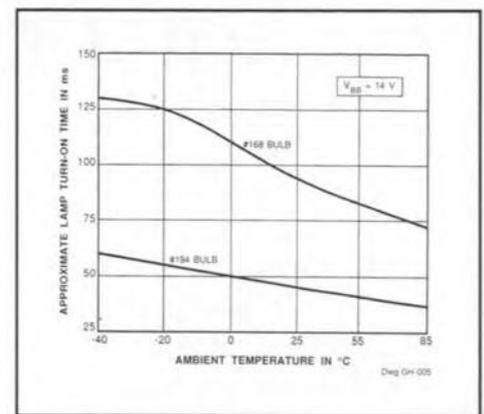
(Fig. 6) without the need for warming or current limiting resistors. In applications using several sensor/drivers to control multiple lamps, the internal clamp diodes may be connected together to an appropriate current-limiting resistor and simple 'lamp test' switch.

As shown in Fig. 7, when an incandescent lamp is initially turned ON, the cold filament is at minimum resistance and will normally allow a ×10 to ×12 peak in-rush current. As the lamp warms up, the filament resistance increases to its rated value and the lamp current is reduced to its steady-state rating. When switching a lamp with the UGQ5140K, the internal current-limiting circuitry limits the peak current to about 900 mA. The device will stay in the current limit and delta temperature limit modes until the lamp resistance increases to its rated steady-state value (Fig. 7). A side-effect of this current-limiting feature is that lamp turn-on times will increase. Typical lamp turn-on times are shown in Fig. 8.

Inductive load driver. Connecting the internal clamp diode (pin 3) to the positive supply allows relays or other inductive loads to be driven directly, as shown in Fig. 9. The internal diode prevents damage to the output transistor by clamping the high-voltage spikes that occur when an inductive load is turned OFF. An optional external zener diode can be used to increase the flyback voltage, providing a much faster inductive load turn-OFF current decay, resulting in faster dropout (reduced relay contact arcing), and improved performance. The maximum zener voltage, plus the load supply voltage, plus the clamp diode forward voltage should not exceed 35 volts. ∎

* $V_{out} = V_{BB} - (I_{LIMIT} \times R_L)$
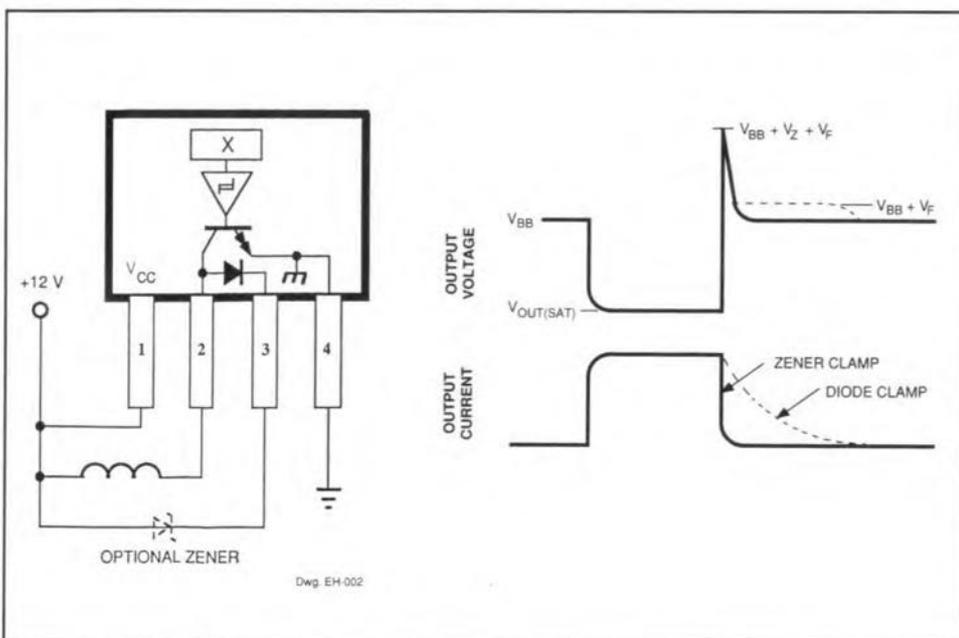
** $P_D = V_{out} \times I_{LIMIT}$

Fig. 9. Typical relay/solenoid driver application.

MILLI-OHM MEASUREMENT ADAPTOR

Prices of digital multimeters have come down to a level where they are affordable by almost any hobbyist. Although most multimeters offer a fair number of measurement ranges, including, on some of the latest models, frequency and capacitance, they are not really suited to measuring very small resistance values, say, in the milli-ohm range. The adaptor described here overcomes this problem.
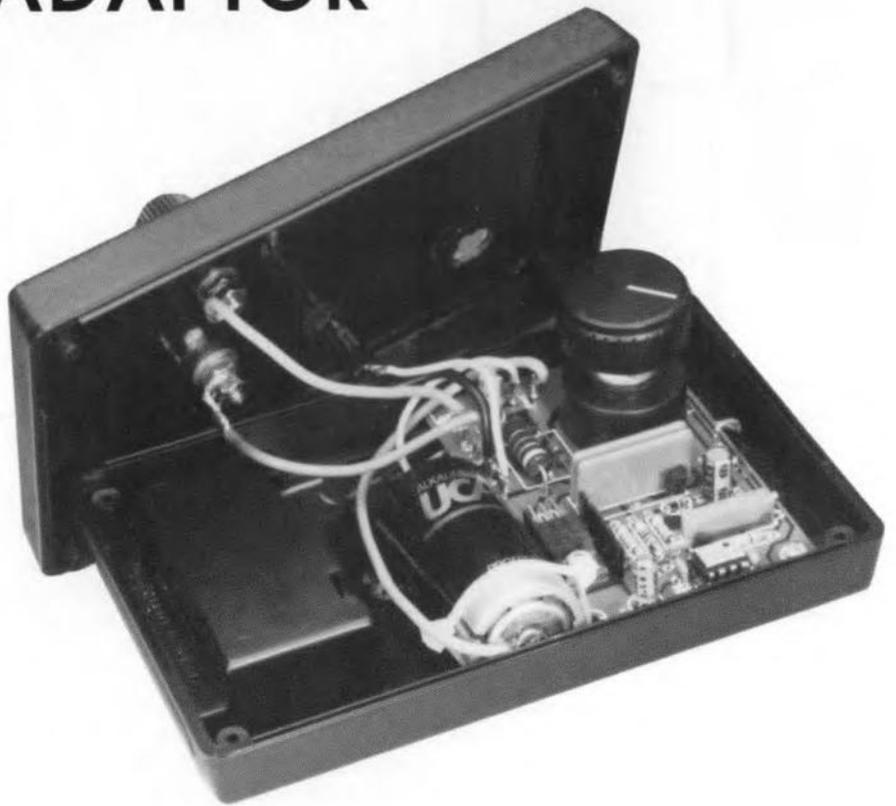
Design by Ing. B.C. Zschocke

RESISTANCE values smaller than 10 Ω or so are notoriously difficult to measure because multimeters often lack a suitable range, or run into tolerances so high that measurement results are at best 'approximate'. Examples of low-value resistors are shunts used with moving-coil meters, and emitter resistors in transistor power amplifiers and power supplies. Typically, such resistors have values in the milli-ohm range, and are almost impossible to measure accurately with the aid of a normal multimeter.

Since low-value resistance measurements will not be required too often, most of you will be reluctant to buy a dedicated milli-ohm meter. Therefore, a simple circuit is described that functions as a mΩ-adaptor for use with any 3½-digit digital multimeter. The measurement ranges created by the adaptor are 20 Ω, 2 Ω and 0.2 Ω for full-scale deflection. The accuracy that can be achieved depends on the multimeter used and the tolerance of the reference resistor in the adaptor.

The resistor to be measured is connected to the multimeter (set to the 200 mV d.c. range) as well as to the adaptor. This creates a four-point resistance measurement.

The basics

The basic operation of the circuit is easily explained with reference to Fig. 1. As soon as the resistor to be measured, R_x, is connected into the circuit, opamp IC1, power FET T1 and resistor R1 supply a reference voltage U_1. This means that a measurement current U_1/R_1 flows through the opamp and R_x. In the present circuit, a reference voltage of 100 mV is used, in combination with selectable reference resistors of 10 Ω, 1 Ω and 0.1 Ω. This results in measurement currents of 10 mA, 100 mA and 1 A. The multimeter is set to the 200-mV range, and connected in parallel with the test sockets on the adaptor.

When the multimeter has an accuracy of 0.1 mV, a resistance of

$$0.1\ mV/1\ A = 100\ \mu\Omega$$

can be measured in the highest current range. The simplicity of this type of measurement has one disadvantage: the measurement result can not be read directly from the multimeter, which gives a mV indication. Depending on the selection of the reference voltage and the reference resistor, the conversion boils down to a simple multiplication with 0.001 (or 1 for mΩ values), 0.01 or 0.1. For example, a meter indication of 167.8 mV in the 20-Ω range corresponds to a resistance of 16.78 Ω.

Practical circuit

The circuit diagram in Fig. 2 is the practical implementation of what has been discussed above concerning the principle of four-point resistance measurement. In fact, the circuit diagram is hardly more complex than Fig. 1: only the range resistor selection and the reference source are added.

A pseudo-zener diode Type TL431C is used as the reference source. The zener takes its unregulated input voltage from a 9-V (PP3) battery. The reference voltage at the – input of the opamp is set by a multiturn
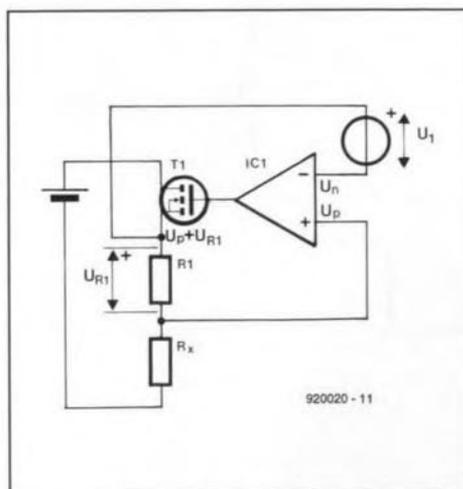
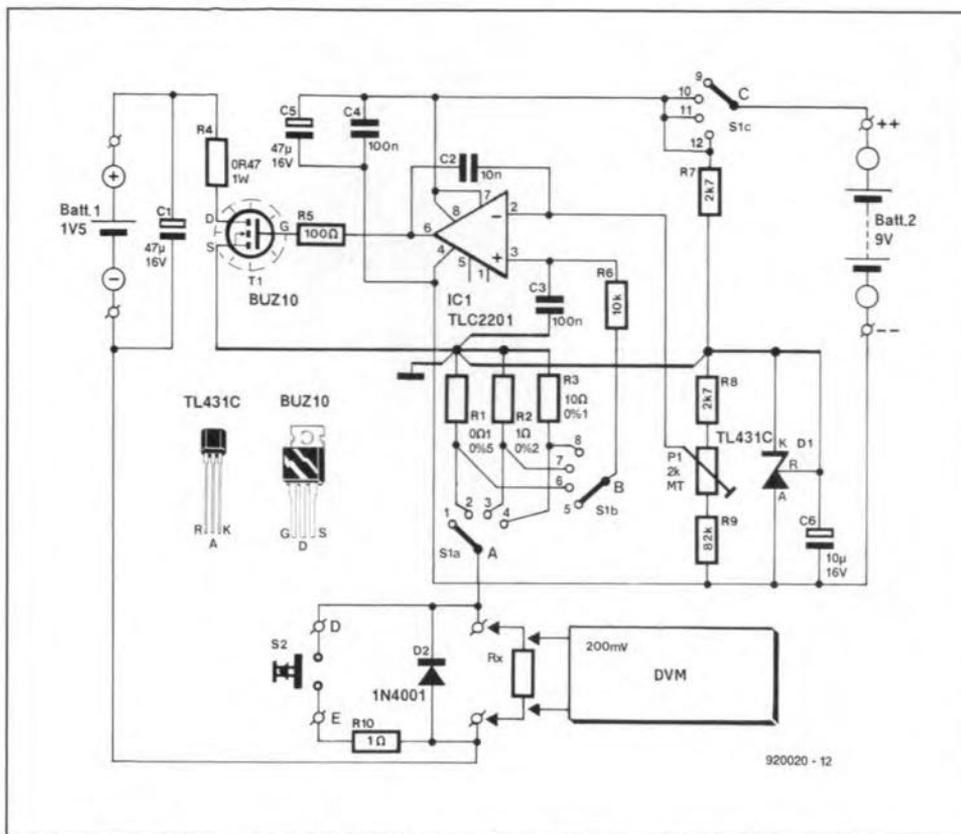Fig. 1. Principle of four-point resistance measurement. The opamp is assumed ideal here.

Fig. 2. Circuit diagram of the mΩ adaptor for digital multimeters.

MAIN SPECIFICATIONS

- Suitable for all digital multimeters with a 200-mV d.c. range
- Added measurement ranges: 20 Ω, 2 Ω, 0.2 Ω
- Resolution: 10 mΩ, 1 mΩ, 0.1 mΩ
- Measurement error: 0.1%, 0.2%, 0.5% (depending on DMM tolerance)
- Four-point resistance measurement

preset, P1, which forms part of a potential divider connected across the reference source. To eliminate the off-set voltage introduced by the opamp, the voltage at the – input is set to 100 mV minus the off-set voltage. All voltages in the circuit are referenced against the cathode of the TL431C.

The opamp adapts the gate drive of FET T1 until the voltage drop across the selected reference resistor (R1, R2 or R3) equals the reference voltage. When this is achieved, the current through Rx is either 1 A, 100 mA or 1 mA.

An *R-C* network, R6-C3, and a capacitor, C2, ensure a high d.c. amplification of the opamp, while keeping the a.c. amplification as small as possible to prevent instability.

There are good reasons for using a less than common opamp in this circuit. The TLC2201 from Texas Instruments offers a large drive margin right up to about 0.1 V below the supply voltage, while its off-set voltage remains stable despite changes in the ambient temperature and the supply voltage. Also, its input bias current is very small thanks to the use of input FETs. The large drive margin is essential here to ensure sufficient gate drive for the FET at a relatively

low supply voltage (battery operation).

Given the relatively high measurement currents, the contact resistance of the range switch must be taken into account. That is why the opamp input, pin 3, is connected to the selected measurement resistor via R6 and an extra deck on switch S1, rather than directly to the pole of S1a (point 'A').

The functions of the rest of the components in the circuit are easily explained. Resistor R4 reduces the power dissipation in the FET. It can be made smaller when high contact resistances are to be compensated in the measurement circuit. Push-button S2 and resistor R10 are included to check the correct function of the adaptor and the multimeter ('battery test'). The 1.5-V battery marked 'Batt.1' in the circuit diagram may be a 'mono' (IEC R20) or 'baby' (IEC R14) type, or a 'mignon'-size (IEC R6) NiCd battery. The internal resistance of all these three battery types is sufficiently small. The battery marked 'Batt.2' is a 9-V PP3 (IEC 6F22) power pack.

Diode D2 protects the circuit against back e.m.f. produced when inductances are measured. A protection against external voltages is **not** provided. Also, be careful

when measuring the resistance of transformer windings—the voltage induced in the primary winding may be dangerous!

Construction and adjustment

The adaptor is built on a small single-sided printed circuit board, of which the artwork is shown in Fig. 3. Because of the relatively high measurement current, it is recommended to use fairly thick wires (e.g., 0.75 mm² multi-strand wire). Do not use solder terminals—instead, solder the wires directly to the board, the battery holder and the terminal posts on the front panel. The terminal posts (or 'wander sockets' as they are sometimes called) are types with a horizontal through hole in the threaded shaft. These holes are used to clamp down the wires of the resistor to be measured, while the probes of the multimeter are inserted into the vertical cylinders in the terminals.

To adjust the adaptor, set it to the highest measurement range (reference resistor R3, switch S1a to position '4'). Short-circuit the measurement posts. Connect the multimeter probes directly across reference resistor R3, and adjust preset P1 until the DMM indicates 100 mV. It is recommended to repeat this adjustment from time to time.

In principle, the adaptor may also be adjusted in any of the two other ranges. However, adjustment in the 20-Ω range will provide the highest accuracy because the measurement resistor in this range has the smallest tolerance (0.1%). In any case, fit new batteries before adjusting the adaptor.

A few remarks on the battery voltages: the BUZ10 (T1) starts to conduct at gate voltages between 2.1 V and 4 V. A drain current of 1 A requires a gate-source voltage of 4.5 V or more. In practice, this means that the battery voltage of Batt.2 must not drop below 7 V. Theoretically, the lowest voltage of Batt.1 is

$$I_{max} (R4+R1+R_{max}) = 1 (0.47+0.1+0.2) = 0.77 \text{ V}.$$

Again in practice, the minimum battery voltage will higher at about 1 V to allow for the drain-source voltage (U_{d-s}) of T1, wire losses,

Table 1. DMM indication to value conversion

Measurement range (adaptor)	Indication (DMM)	Resistance (Rx)	Conversion
0.2 Ω	200mV	200 mΩ	readout × 1 mΩ/mV
2.0 Ω	200mV	2 Ω	readout × 0.01 Ω/mV
20 Ω	200mV	20 Ω	readout × 0.1 Ω/mV
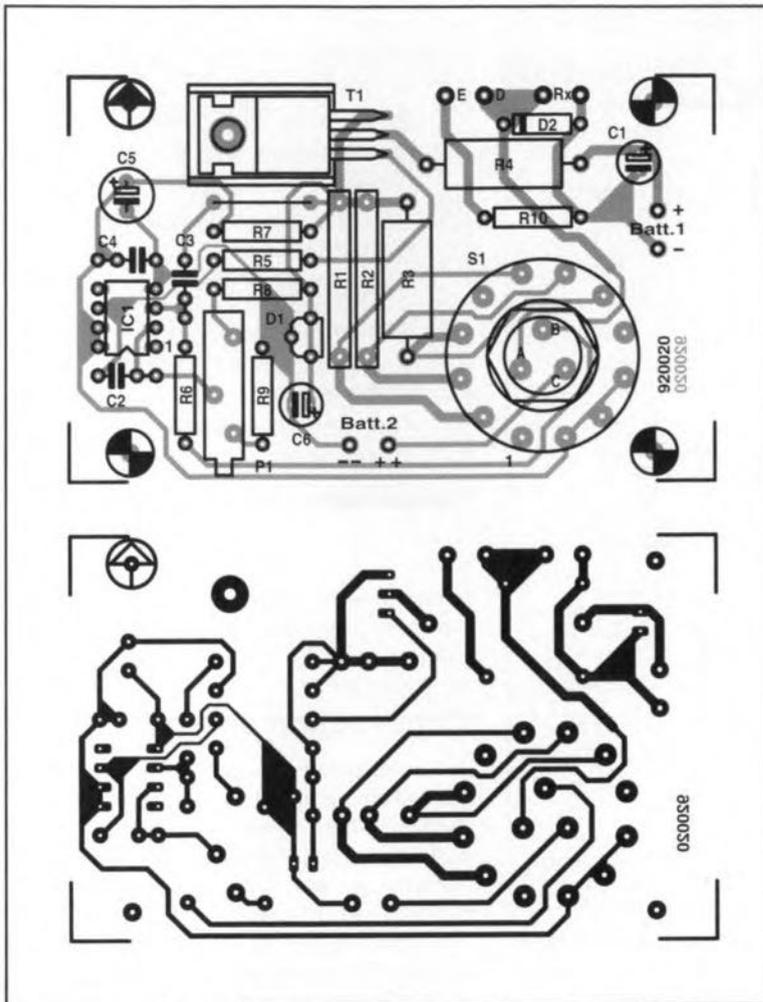
Fig. 3. Track layout (mirror image) and component mounting plan of the adaptor PCB.

Fig. 4. Suggested front panel design.

920020 - F

and copper track losses.

When long test wires are used between the adaptor and the resistor to be measured, or when high contact resistances are to be taken into account, resistor R4 should be made smaller, e.g., 0.22 Ω.

Practical use

The unknown resistor and the DMM are connected to the terminal posts on the front panel of the milli-ohm adaptor. The reading on the DMM is converted into a resistance value as shown in Table 1.

As already mentioned, care should be taken when measuring inductive components such as large chokes and transformer windings. When an inductive component is disconnected from the adaptor, it may produce an induced voltage. In the interest of safety, keep to the following order: (1) connect the unknown inductor to the adaptor; (2) connect the multimeter; (3) switch on the adaptor with S1. The opposite order applies when the measurement is finished: (1) turn off the adaptor; (2) disconnect the multimeter; (3) disconnect the inductor. Large inductances, for example, power transformers, are best short-circuited before disconnecting.

Fortunately, the above connection and disconnection order need not be observed when purely resistive components are measured.

Extensions

It is, of course, possible to extend the present adaptor into a dedicated milli-ohm meter: all that is required to do so is a separate power supply and a conventional DVM module. The inputs of the DVM are then connected directly between the pole of S1b and the ground. In this way, the DVM measures the ratio of the unknown resistance to the reference resistance, independent (within limits, of course) of the measurement current, which makes adjustment unnecessary. The accuracy of the instrument thus depends on the accuracy of the DVM module and that of the reference resistor.   ■
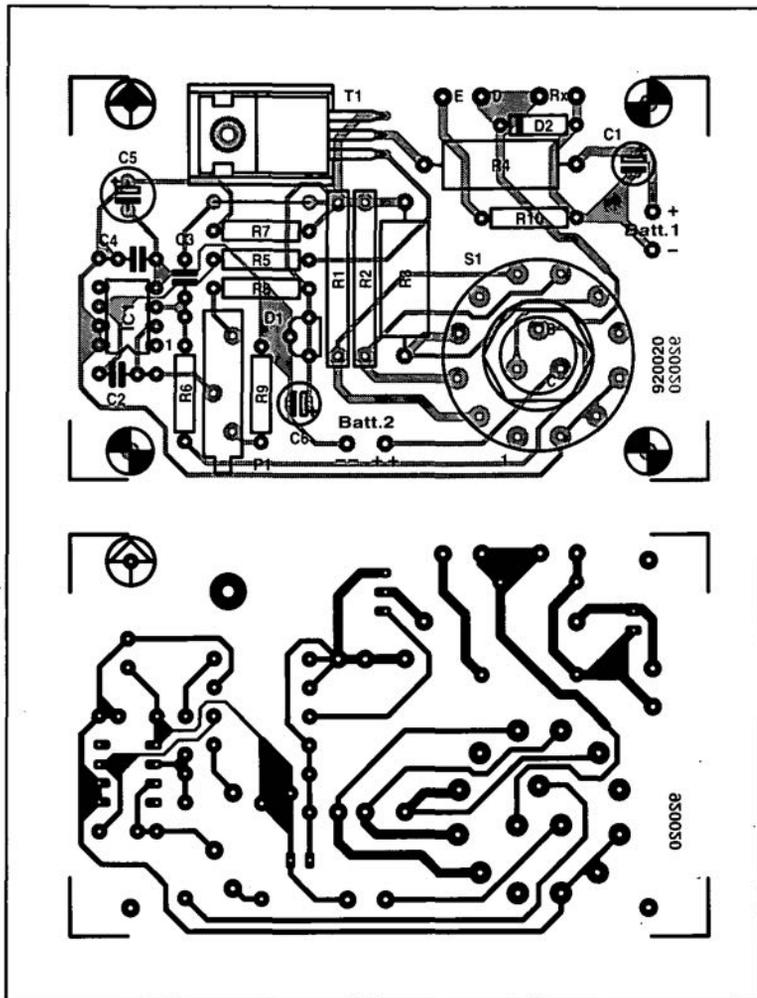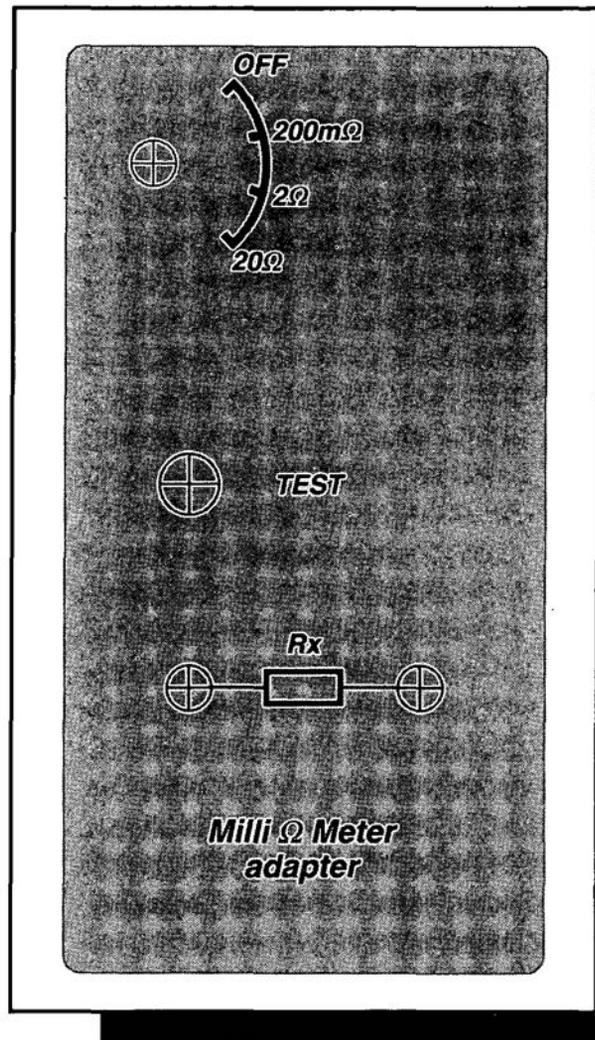
COMPONENTS LIST

Resistors:

1	0Ω1 0.5%	R1
1	1Ω 0.2%	R2
1	10Ω 0.1%	R3
1	0Ω47 1W	R4
1	100Ω	R5
1	10kΩ	R6
2	2kΩ7	R7;R8
1	82kΩ	R9
1	1Ω	R10
1	2kΩ multiturn preset	P1

Capacitors:

2	47µF 16V radial	C1;C5
1	10nF	C2
2	100nF	C3;C4
1	10µF 16V radial	

Semiconductors:

1	TL431C	D1
1	1N4001	D2
1	BUZ10	T1
1	TLC2201	IC1

Miscellaneous:

1	3-pole 4-way PCB mount rotary switch	S1
1	SPST push-button	S2
1	9V battery with clip	Batt.1
1	1.5V battery with holder	Batt.2
1	Heat-sink for T1	
1	ABS enclosure, size approx. 145×90×30mm	
1	Terminal post black	
1	Terminal post red	
1	Printed circuit board	920020

Fig. 3.   Track layout (mirror image) and component mounting plan of the adaptor PCB.

920020 - F

4-Megabyte printer buffer

June 1992

Two points regarding this project.

(1) The input of the buffer is designed to be Centronics compatible. Problems may occur when this standard is not respected by the computer or the software. A number of 'fast' PCs (in particular 386 and 486 based machines) appear to have printer interfaces derived from the Epson standard. These interfaces in general do not wait for the ACKNOWLEDGE signal, but instead process the BUSY signal.

Handshaking problems that may occur between these PCs and the printer buffer may be solved by combining the BUSY and ACKNOWLEDGE signals as shown in the diagram opposite. The result of the modification is that the printer buffer behaves like an Epson-compatible peripheral device.

(2) An updated version of the control software (in EPROM) is available that enables 1-Megabyte ($1M \times 8$ and $1M \times 9$) SIP/SIM modules with three ICs to be used in the printer buffer.

CORRECTIONS

★ see text

910110 - 99
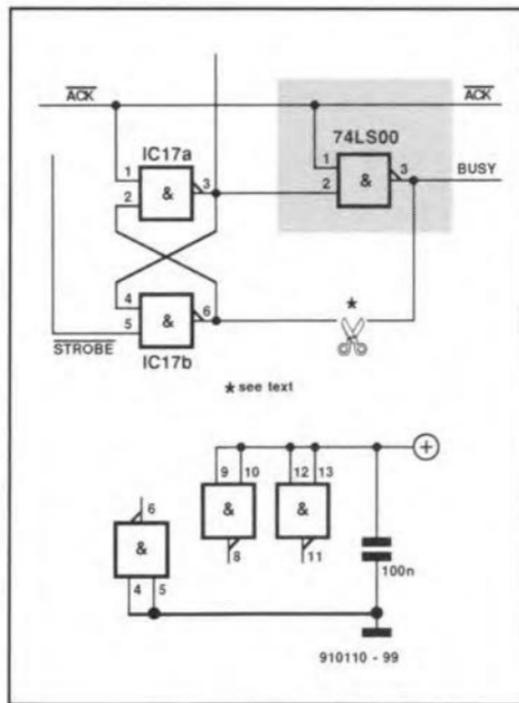
Inductance-capacitance meter

March 1992

Terminals 'A' and 'B' should be transposed in the circuit diagram of the meter circuit proper (Fig. 4 on page 32).

Milli-ohm measurement adaptor

April 1992

To prevent its contacts burning out, switch S_1 must not be operated when an inductive component is connected to the adaptor.

Contrary to what is said under the heading 'Extensions', the reference inputs of the DVM are connected to the pole of S_{1b} and ground, while the 'normal' DVM inputs are connected to the resistor to be measured.

READERS' CORNER

GENERAL INFORMATION

THE COMPLETE PREAMPLIFIER

In response to the requests of a number of readers, here is a list of technical data for 'The complete preamplifier' published in our January & March 1991 issues).

MEDIUM-POWER AF AMPLIFIER

Since we published the 'Medium-power AF amplifier' in our October & November 1990 issues, our design laboratories have taken delivery of some new, more sophisticated test instruments. Among this is an audio analyser that gives more precise measurements of THD, IM, TIM, and so on. The internal distortion of this instrument is way below 0.001% (20 Hz–20 kHz). The instrument also has a two-channel FFT analyser (sample frequency 192 kHz) with built-in 24-bit signal processors. This enables very accurate and rapid analyses of distortion.

Since the instrument was not available during the design of the 'Medium-power amplifier', our engineers felt it worthwhile to subject their prototypes to an analysis with the new instrument. Some of the results are shown in Figures 1–5.

It has become apparent that the power transistors specified, that is, the BD911 and BD912 in practice have a much larger spread than we were led to believe by the manufacturer's data sheets. A number of readers have reported that because of this their amplifier has broken down spontaneously. The reason for this is that one of the three parallel-connected transistors draws a larger current than the other two and that's the end of that, or rather, of the transistors.

To ensure that such mishaps cannot occur, the characteristics of the transistors should be measured before the devices are taken into use. A suitable instrument for this is the 'High-current h_{FE} tester' published in our September 1990 issue. It is advisable to use three transistors whose characteristics do not deviate from one another by more than about 20%.

It is, of course, also possible to use different types of transistor, for instance, the
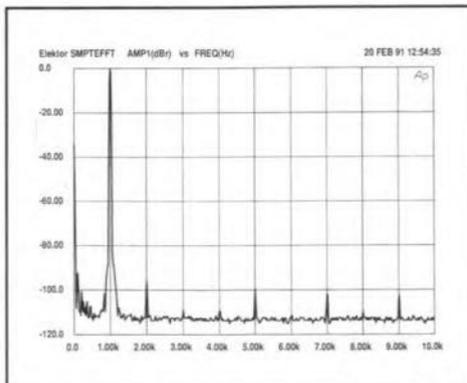
BDT95 and BDT96, or the BDT85 and BDT86. Furthermore, it cannot be overstressed that before the amplifier is tested, power resistors of 15–22 Ω are inserted into the supply lines.

No damage can then ensue and you can ascertain the current split between the three transistors (by means of the voltage across the 0.27 Ω emitter resistors). ∎
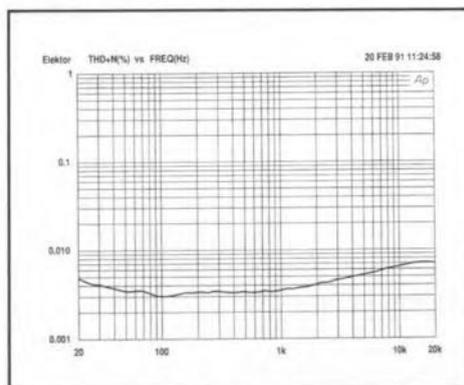

The complete preamplifier – Technical Data

Input sensitivity	
Microphone input	2.4 mV r.m.s.
Line inputs	150 mV r.m.s.
Input impedance	
Microphone input	47 kΩ
Line inputs	47 kΩ
Nominal output voltage	1 V r.m.s.
Output impedance (tape & line)	<100 Ω
Maximum output voltage	9.5 v r.m.s.
Bandwidth (10 kΩ load)	
Microphone input	20 Hz–20 kHz (±0.3 dB)
Line inputs	5 Hz–1 MHz (±0.5 dB)
Signal-to-noise ratio (inputs shorted)	
Microphone input	>80 dB (linear)
Line inputs	>100 dB (linear)
Channel separation (Z_{source} <600 Ω)	>100 dB (1 kHz)
(line inputs)	>70 dB (20 kHz)
Cross-talk between inputs	>100 dB (1 kHz)
(unused inputs terminated in 600 Ω)	>80 dB (20 kHz)
Harmonic distortion (1 V output)	<0.003% (20 Hz–20 kHz)
(line inputs)	
Intermodulation distortion (1 V output)	<0.005% (250 Hz/4 kHz; 4:1)
(line inputs)	

Fig. 2. THD from 20 Hz to 20 kHz at an output voltage of 2.83 V (1 W into 8 Ω).
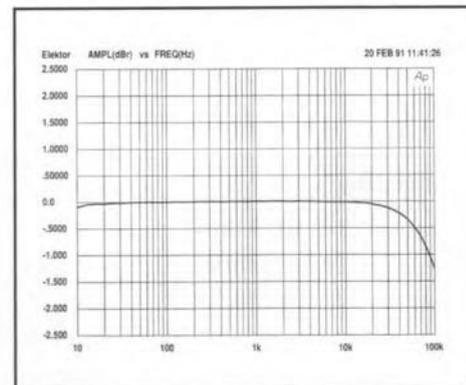
Fig. 3. Frequency characteristic at an output voltage of 2.83 V.

Fig. 1. Harmonic distortion at 1 kHz. Expressed as a percentage: 0.004%.
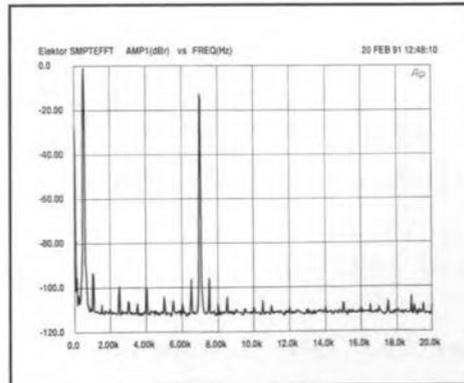

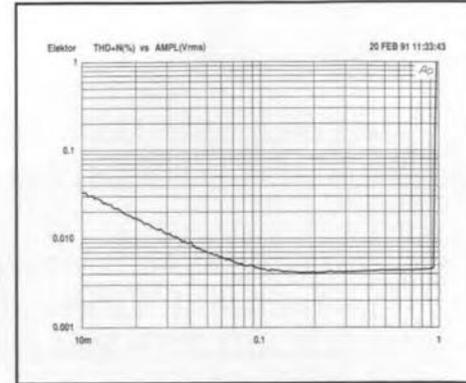**Fig. 4. Intermodulation distortion 500 Hz: 7 kHz; power ratio 4:1.**

Fig. 5. Harmonic distortion vs the drive voltage to the output amplifier stages.