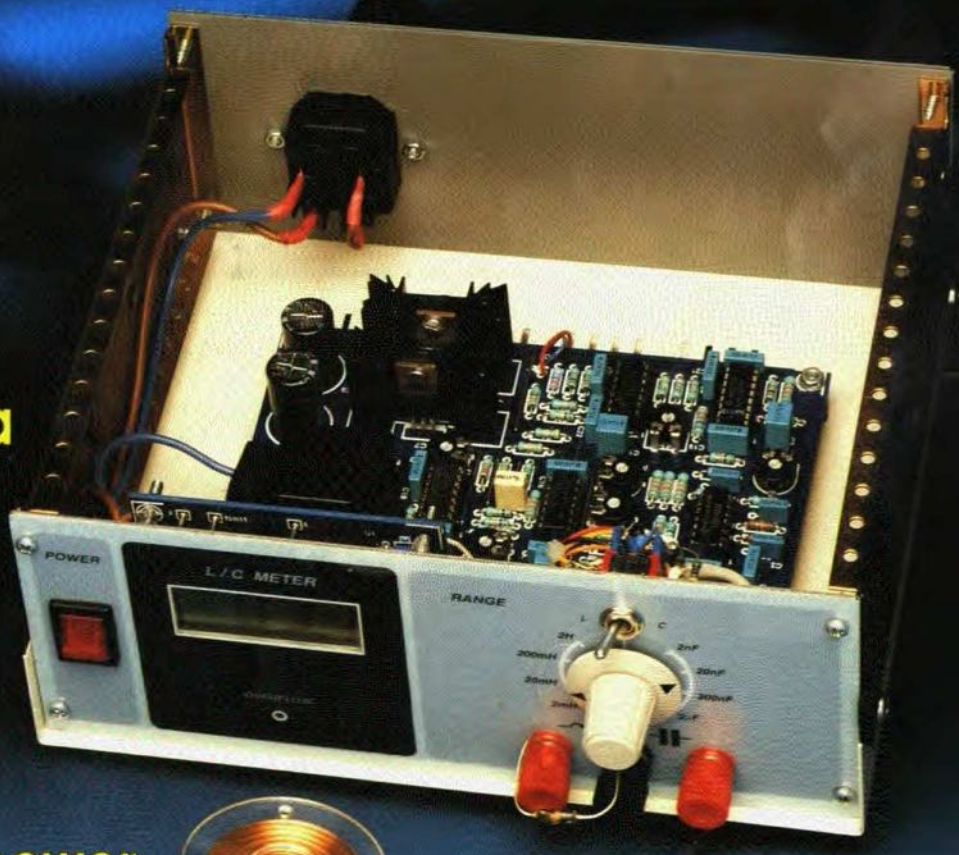
ELEKTOR ELECTRONICS

THE INTERNATIONAL ELECTRONICS MAGAZINE
MARCH 1992
UK £1.90

Inductance-capacitance meter



FM tuner-Part 1

Flat-top 80 antenna

8751 emulator

AF drive indicator

Measurements on power supplies

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ELEKTOR ELECTRONICS

March 1992
Volume 18
Number 198

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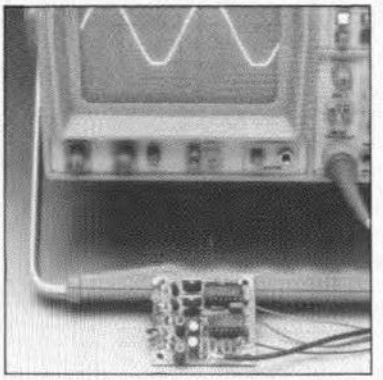
- Comb generator
- AD232 converter
- General array logic (GAL)
- Understanding waveform harmonics
- Super sign
- LCD for L/C meter
- 2 metre receiver
- Red-light diode lasers

Front cover

This month's instrument in our series of test and measuring instruments is an inductance/capacitance meter. Since it is essential that when the value of an inductor or capacitor is measured the ohmic losses do not affect the result, the meter has built-in automatic loss compensation.

ABC
MEMBER OF THE AUDIT BUREAU OF CIRCULATIONS

EXTRA IN THIS ISSUE: Greenweld's 16-page WINTER SUPPLEMENT (between pages 34 & 35) full of warming winter cheer and lots of bargains to boot; and Maplin's leaflet on a new range of Precision Gold Multimeters with unbeatable value and a multitude of features.



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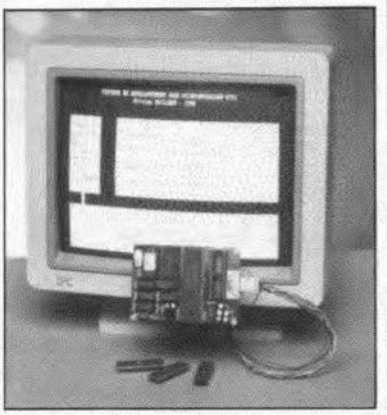

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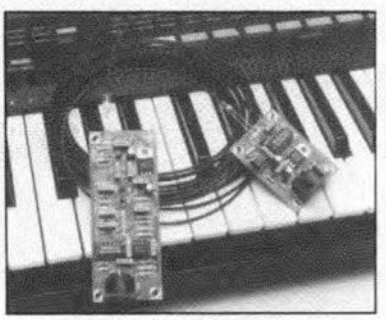

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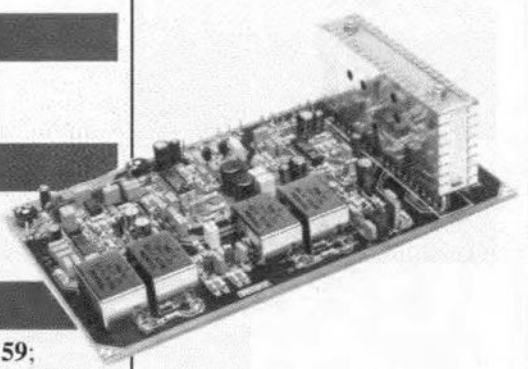

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MIDI DATA TRANSFER

based on a design by M. Schreiber

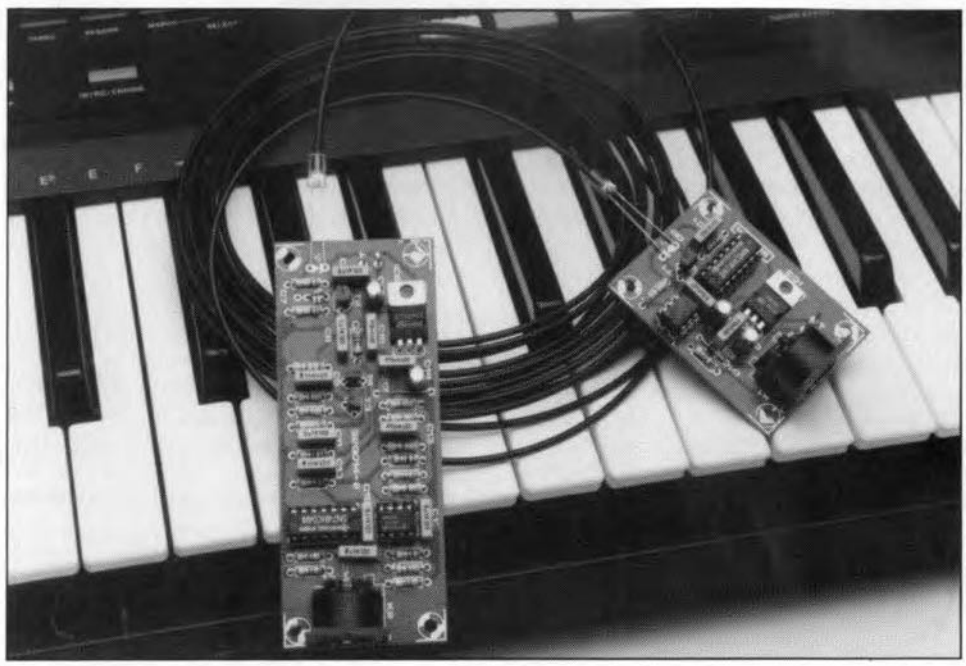
More and more musicians make use of musical instruments that are controlled by a computer or keyboard via a MIDI cable. This article proposes to replace that cable by an optical-fibre type. That makes the system less vulnerable to noise signals and increases the top speed of the serial connection to about 60 kbit s^{-1}. The cable may also be used for transferring non-MIDI asynchronous serial data.

DIGITAL techniques have found their way even into the world of music where analogue information is of paramount importance. Inexorably, more and more popular music is being translated into a series of digital commands. MIDI (Musical Instrument Digital Interface) is the keyword for modern musicians. Not only organs, keyboards, and pianos, but also guitars and saxophones are available with the familiar 5-way DIN plug for the MIDI. The interface enables the instrument to receive information about the keys that must be operated, the voices to be used, and the force and speed of the key stroke. The MIDI standard stipulates that the digital information must be interchanged between instruments at a speed of 32.5 kbit s^{-1}.

A MIDI cable usually consists of two cores that together form a current loop. The MIDI protocol does not provide handshaking: all data are presented by the transmitter and processed by the receiver asynchronously. The data, which are transferred from transmitter to receiver more or less continuously, normally contain, apart from a status byte, one or more data bytes.

Because of the simple design of the serial connection, it is fairly simple to replace the current loop by an optical link. The block schematic of a typical system so modified is shown in Fig. 2. Electrical digital signals are transformed by the E–O (electrical-to-optical) converter into light pulses that can be transmitted over fairly long distances via an optical conductor. In that conductor, the signals lose their sharp corners, but, because of the digital nature of the information, that does not affect the information itself, unless the link is long. The O–E (optical-to-electrical) converter in the receiver transforms the light back to electrical signals at their original quality.

The application of the circuit need not be restricted to the transfer of MIDI signals: it may just as well be used with other links operating at up to 60 kbit s^{-1}. A few that jump to mind are its inclusion in a data acquisition system that transmits serial data and as a primitive connection to a printer. Thanks to the optical-fibre cable, data are not or hardly mutilated even under



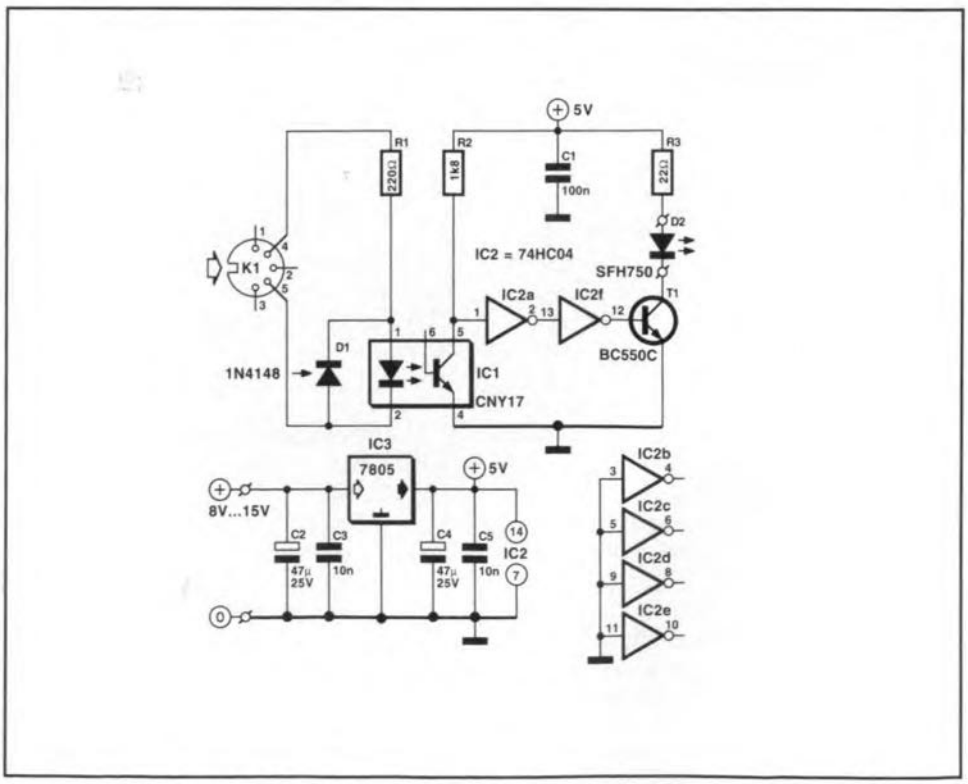


Fig. 1. Circuit diagram of the transmitter.

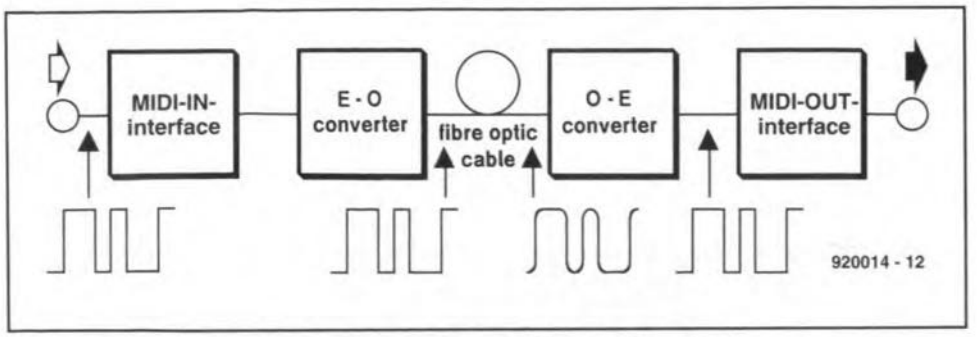


Fig. 2. Block schematic of typical system modified as described.

the most arduous operating conditions.

The electronics

The circuit of the transmitter is shown in Fig. 1 and that of the receiver in Fig. 3. The electrical information is applied to pins 2 and 4 of connector K_1. The current flowing in the current loop ensures that the LED in optoisolator IC_1 lights. In case of a logic 0 (negative logic on the MIDI bus), the current is limited to about 5 mA by R_1.

Because of the current pulses, the phototransistor in IC_1 conducts and changes the input level of inverter IC_{2a} in step with these pulses.

The signal is buffered and enhanced by IC_{2a} and IC_{2f} and then converted to an optical signal by transmit diode D_2 in the collector circuit of T_1. The current through D_2 is limited by R_3. This diode is of a type specially designed for straightforward connection to an optical-fibre cable. The 2.2 mm thick cable fits exactly into the hollow provided in the diode.

In the receiver, p-i-n diode D_3 has a similar hollow to receive the optical-fibre cable. The frequency range over which the diode remains usable is maximized by the negative bias obtained by connecting the cathode to the positive supply rail.

The sensitivity of the diode is determined by series resistor R_5. The value of this resistor should not be too high, otherwise the resulting integrating action will adversely affect the properties of the receiver.

High-pass filter R_6–C_7 suppresses noise and other spurious signals below 50 Hz. Its output is buffered and amplified by T_2, and then amplified again (×10) by cascode circuit T_3–T_4. The advantage of a cascode circuit is that it virtually nullifies the Miller (base–collector) capacitance of the transistors, thereby yielding a wide frequency range. The Miller capacitance normally restricts the frequency range when the transistor operates as a voltage amplifier. Here, since the collector of amplifier T_4 is coupled to the earthed base circuit of T_3 (very low input impedance), the Miller capacitance of T_4 is largely neutralized.

The design of the cascode circuit enables reliable reception of signals over optical-fibre cables up to 30 m (98 ft) long.

The output of T_3–T_4 is applied to comparator IC_4. This stage requires two reference voltages to convert this analogue output into digital signals. Resistor R_{14} serves to improve the common-mode rejection of the IC to ensure that the comparator switches reliably even when the level differences are small.

Since IC_4 has an open-collector output, a resistor, R_4, is required from this output to the positive supply line. The value of this resistor determines the transition durations of the signal. With the value shown (1 kΩ), these durations are 400 ns: they should be short compared with the period of the signal.

The output signal of IC_4 is fed to the customary MIDI consisting of gates IC_{5e} and IC_{5f}; resistors R_{20} and R_{21} determine the current flowing in the MIDI loop.

Construction & testing

The transmitter-receiver is best constructed on the printed-circuit board shown in Fig. 6. Before construction is started, however, this board should be cut into two.

Points to watch are the wire link on the transmitter board and the polarity of the electrolytic capacitors and diodes. If you are not a dyed-in-the-wool constructor, use sockets for the ICs to be on the safe side.

Connectors K_1 and K_2 are 5-way DIN types which are standard for interconnections in MIDI systems.

There are various types of transmit and receive diode that can be used—see Fig. 4. Those used in the prototype (and given in the Parts list) can be mounted directly on to the PCB. There are, however, other possibilities. For instance, Fig. 4 shows diodes integrated in a housing, to which the optical-fibre cable is fitted, that can be mounted directly on to the enclosure of the transmitter and the receiver. This type is connected to the PCB via two short lengths of wire. There are yet other types available: see the various mail order catalogues or ask your local retailer.

To test the transmitter and receiver, a function generator is required that can provide a square-wave voltage at a frequency of about 30 kHz and at a level of around 3 V_{pp}. Apply that signal and the generator earth to pins 4 and 2 of K_1 respectively and switch on the transmitter and receiver, whereupon the transmit LED should light. If an oscilloscope is available, check that the signal appears at the receiver output (assuming, of course, that the transmitter and receiver are interlinked by an optical-fibre cable). If these test instruments are not to hand, try the system in practice.

The absence of a power supply in the transmitter and receiver is deliberate: after all, most electrophonic instruments use 12 V supply lines so that 12 V will be available

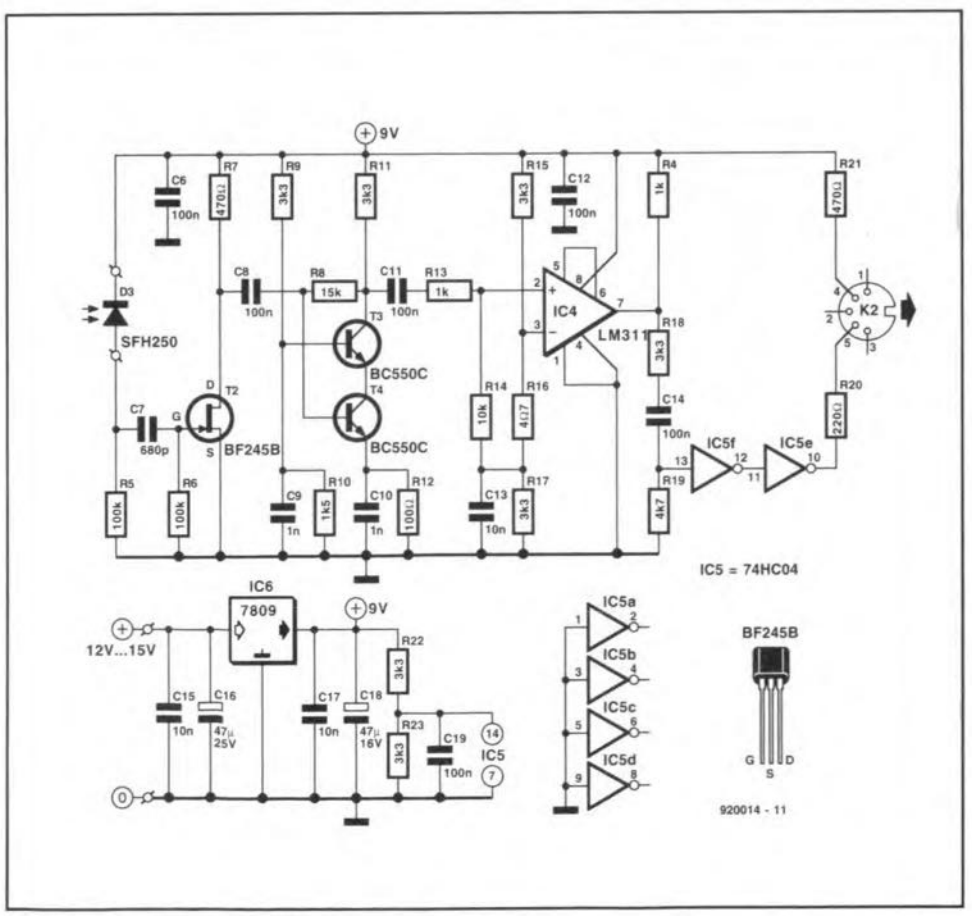


Fig. 3. Circuit diagram of the receiver.

somewhere. If that is not so, use a standard 12 V mains adaptor.

Finally

The design of the receiver provides compensation for signal losses of up to 30 dB. As available optical-fibre cables have an attenuation of about 0.3 dB m^{-1}, a distance of up to 30 m between transmitter and receiver can be spanned. Since the system is broad-band, it can handle signals at a considerably higher transmission speed (up to 60 kbit s^{-1}) than encountered in MIDI systems.

If the amplification of the cascode stage is increased by reducing the value of R_{12}, it becomes possible to work over even greater distances. Note, however, that dispersion may then degrade the pulse width: a phenomenon that is particularly noticeable in multi-mode cables. ■

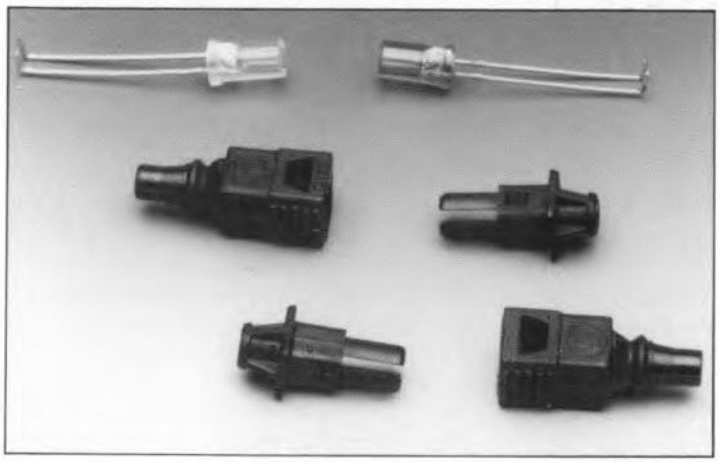


Fig. 4. Various transmit and receive diodes are available.

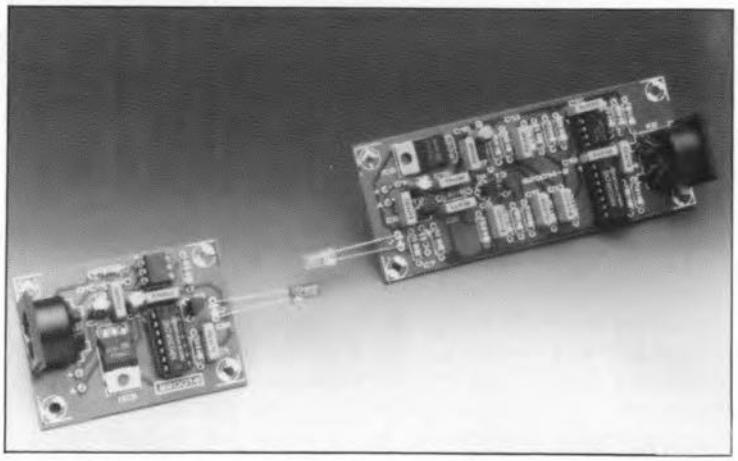


Fig. 5. The completed transmitter and receiver units.

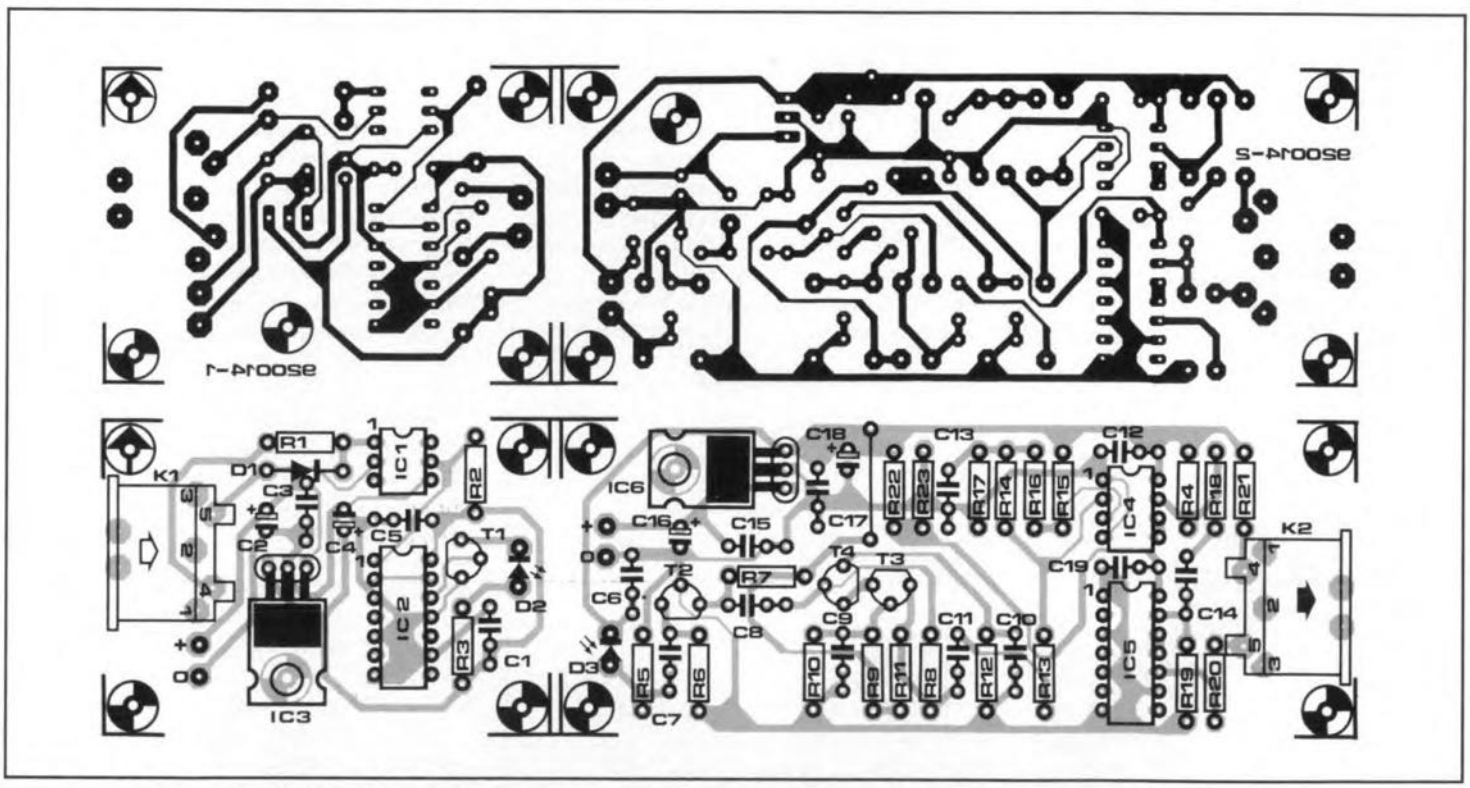


Fig. 6. The printed circuit board for the transmitter and receiver should be cut into two before construction is begun.

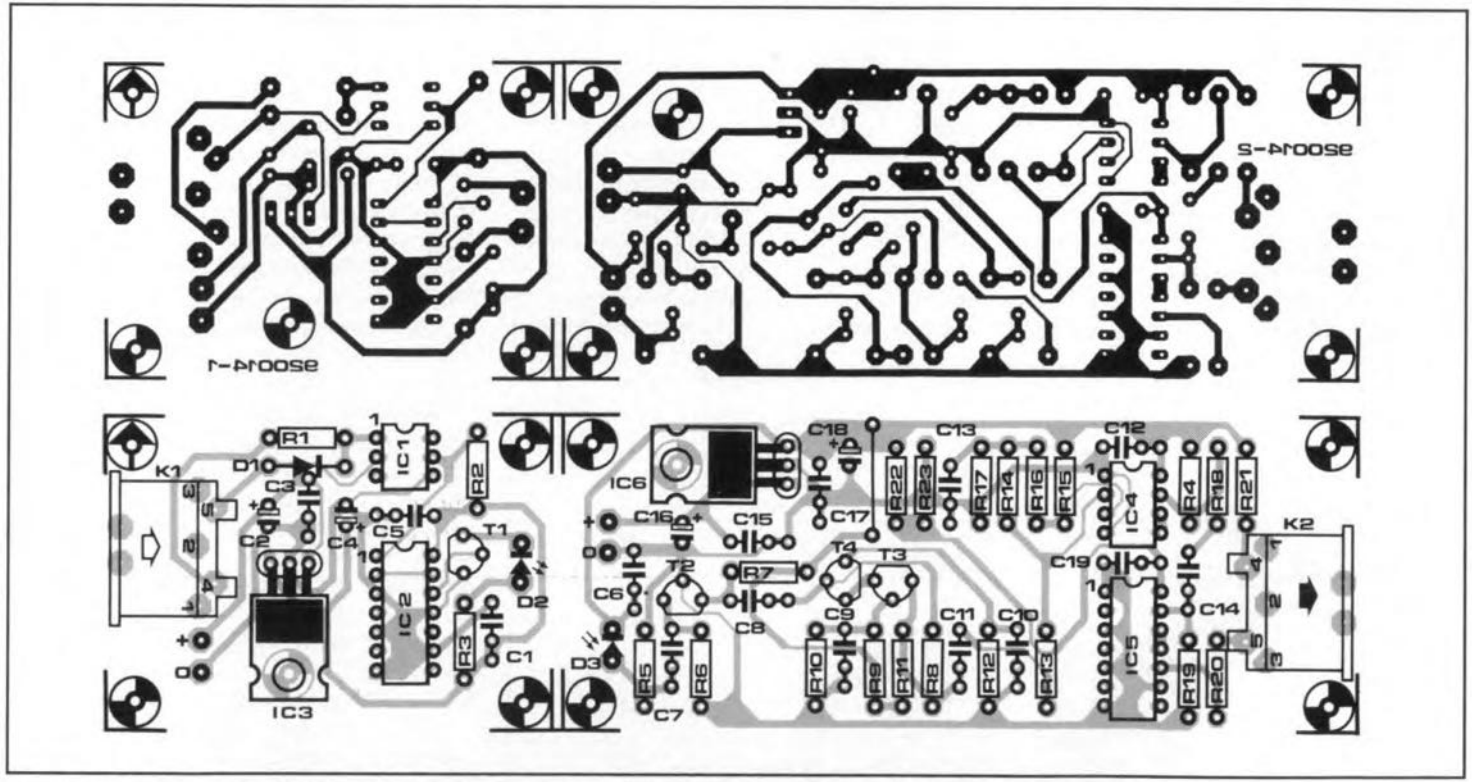
PARTS LIST

Resistors:
R1 = 220 Ω
R2 = 1.8 kΩ
R3 = 22 Ω
R4, R13 = 1 kΩ
R5, R6 = 100 kΩ
R7, R21 = 470 Ω
R8 = 15 kΩ
R9, R11, R15, R17, R18, R22, R23 = 3.3 kΩ
R10 = 1.5 kΩ
R12 = 100 Ω
R14 = 10 kΩ
R16 = 4.7 Ω
R19 = 4.7 kΩ
R20 = 220 Ω

Capacitors:
C1, C6, C8, C11, C12, C14, C19 = 100 nF
C2, C4, C16, C18 = 47 µF, 16 V, radial
C3, C5, C13, C15, C17 = 10 nF
C7 = 680 pF
C9, C10 = 1 nF

Semiconductors:
D1 = 1N4148
D2 = SFH750
D3 = SFH250
T1, T3, T4 = BC550C
T2 = BF245B
IC1 = CNY17
IC2, IC5 = 74HC04
IC3 = 7805
IC4 = LM311P
IC6 = 7809

Miscellaneous:
K1, K2 = 5-way DIN socket for PCB mounting
PCB Type 920014


850014-1
850014-2
K1
D1
R1
C3
C2
C4
C5
IC1
IC2
IC3
R2
R3
T1
D2
C1
IC6
C16
C15
C18
C17
T2
R7
T4
T3
C6
C8
C9
D3
R5
R6
C7
R10
R9
R11
R8
C11
R12
C10
R13
C13
R22
R23
R17
R14
R16
R15
C12
IC4
R4
R18
R21
K2
C19
IC5
C14
R19
R20

THE FLAT-TOP 80 ANTENNA

An experimental design with the apartment dweller in mind

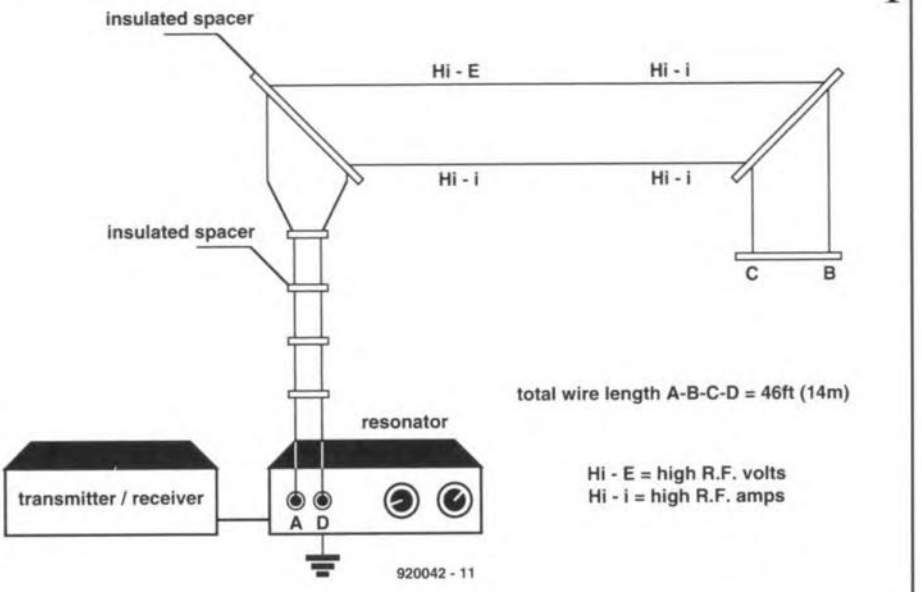
by Richard Q. Marris, G2 BZQ

OLDER readers will remember the original flat-top antennas of the 1920s, 30s and 40s festooning battleships and other warships, ocean-going passenger and cargo vessels, and various military and civil trans-world wireless telegraphy beam stations. Alas, historically speaking, only a few remain.

The original flat-tops, back in the early days of wireless, consisted of two or more parallel spaced horizontal wires with spreaders supported between two or more tall masts. They were usually, but not always, end-fed or T-fed by downleads descending from each wire and joined together and end-fed from the transmitter.

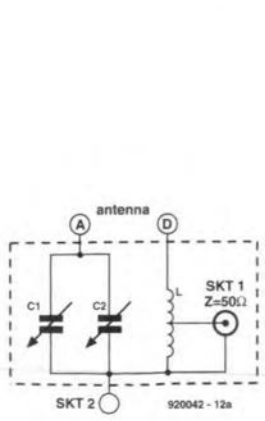
The Flat-top 80 described here has the appearance of an old-time flat-top, but is much smaller and electrically different in as much as it consists of two spaced horizontal wires folded back in series, with the resulting two ends connected to a resonator unit enabling it to be tuned to the operating frequency (here, the 80-meter or 3.5 MHz band)—see Fig. 1. It has been designed experimentally for the 3.5 MHz band for indoor use, in an apartment, where normal, full-size antennas are not a practical proposition. It can, of course, be adapted for use in other indoor situations or in a postage-stamp-sized outdoor back garden. The principle can also be used on other bands. Hopefully, it will encourage other experimenters to adapt the design to their particular needs and situations. After all, it is easy to use and produces quite acceptable results.

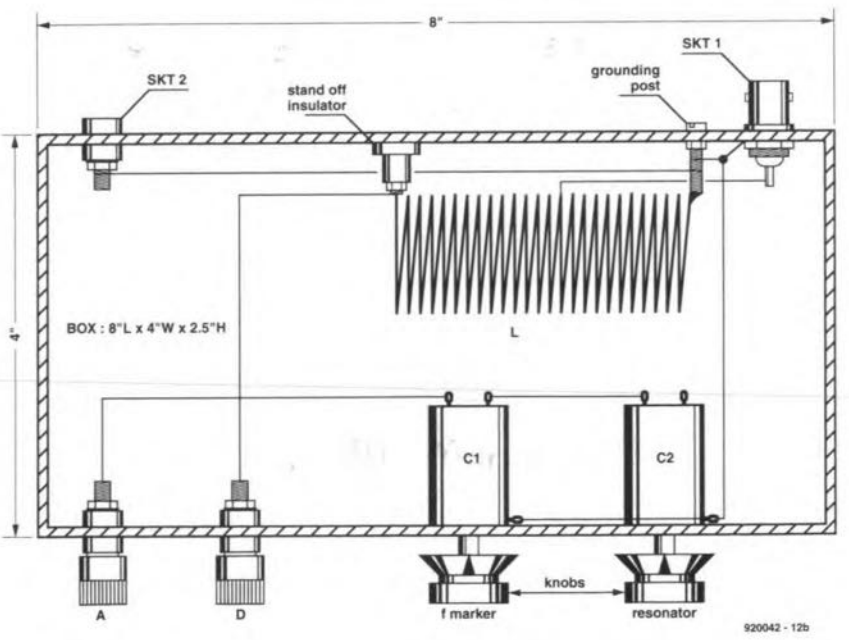
1



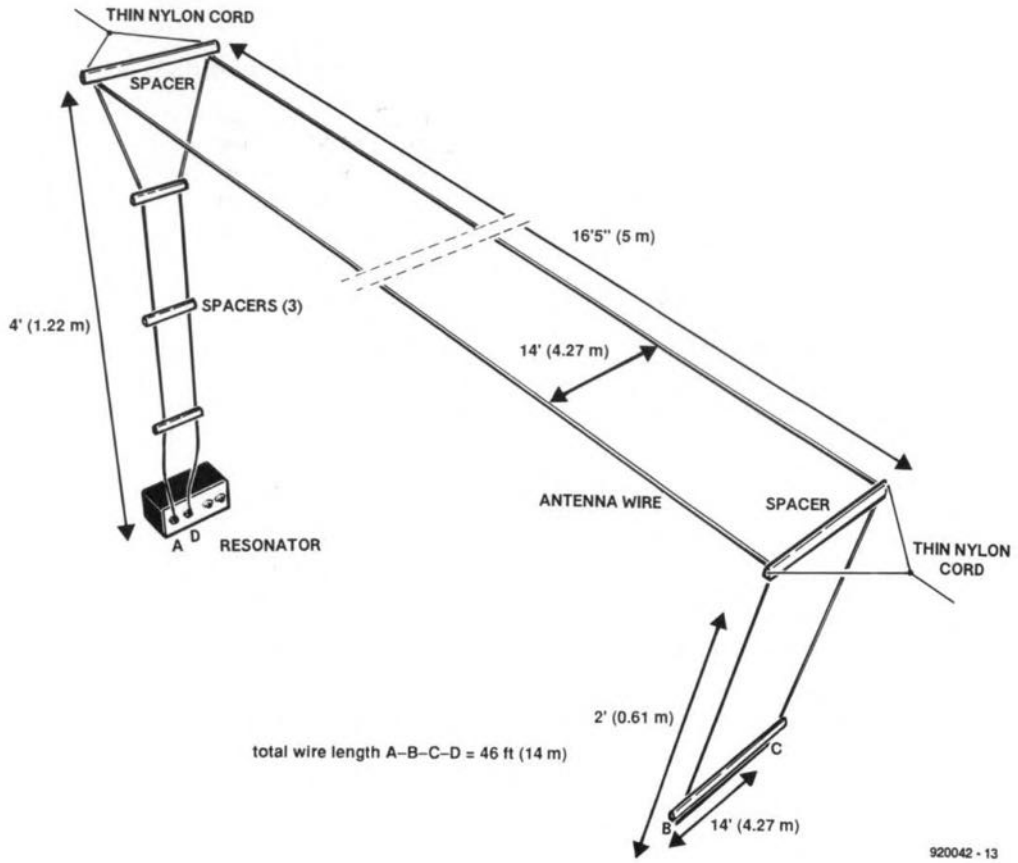
The simple configuration of the Flat-top 80 is shown in Fig. 1 and the novel resonator unit in Fig. 2. The two ends of the Flat-top arrive in parallel at the resonator input terminal posts. One down-lead is connected to loading coil *L*, which is tapped to form a correct 50 Ω impedance match to the RG58 coaxial feedline connected to the transmitter/receiver. The other end is connected to two parallel variable capacitors, C_1 and C_2, which tune the antenna: C_1 is a frequency marker and C_2 is the fine resonator control. For low power transmission, these capacitors should be ceramic-framed, air-spaced variable types such as the Jackson C809 or similar. Arrangements are also made for a socket, SKT_2, to which an optional ground or earth connection can be made. Few appartments, or other in-house locations, have a satisfactory RF ground available, but a nearby metal water piper may

2

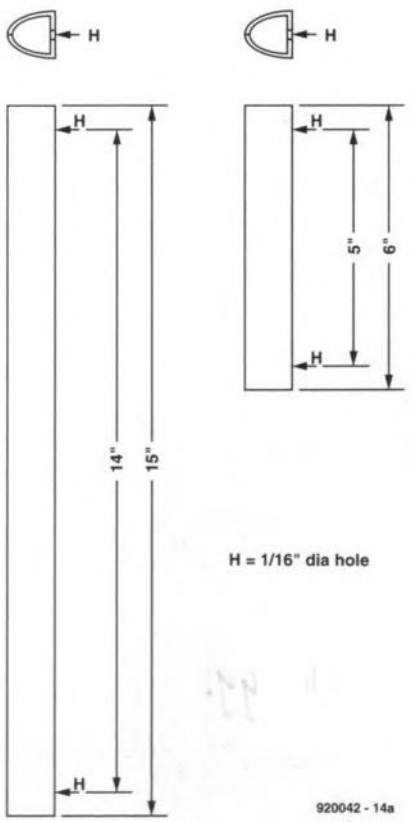




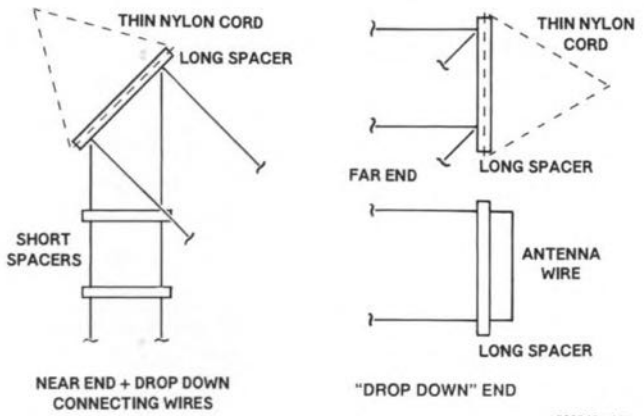
3


THIN NYLON CORD
SPACER
16'5" (5 m)
SPACERS (3)
4' (1.22 m)
14' (4.27 m)
ANTENNA WIRE
SPACER
THIN NYLON CORD
A
D
RESONATOR
2' (0.61 m)
total wire length A–B–C–D = 46 ft (14 m)
C
B
14' (4.27 m)
920042 - 13

4a


H
H
H
H
5"
6"
H
14"
15"
H
H = 1/16" dia hole
920042 - 14a

4b


THIN NYLON CORD
LONG SPACER
SHORT SPACERS
NEAR END + DROP DOWN CONNECTING WIRES
THIN NYLON CORD
FAR END
LONG SPACER
ANTENNA WIRE
LONG SPACER
"DROP DOWN" END
920042 - 14b

well suffice. DO NOT CONNECT THE AC MAINS TO SKT_2! Note that the Flat-top 80 will work equally well with or without a ground connection.

If the Flat-top 80 is erected indoors, in the interest of domestic household safety, only low RF transmitting power should be used. The writer uses 5–10 watts CW transmitter output and achieves quite satisfactory result.-

Construction

The antenna.

Figure 3 shows the construction of the antenna, which consists of a total of 46 ft (14 m) white PVC covered 7/0.2 mm stranded wire. The insulated spacers, shown in Fig. 4, are made of white plastic sprung edging strip obtainable from most DIY stores. White was used throughout for spacers and wire since it is inconspicuous against a white ceiling. Thin white nylon cord supports the end of the Flat-top 80 diagonally across the room.

Three 15 in (38 cm) and three 6 in (15 cm) long spacers are cut as shown in Fig. 4; in each of these, two 1/16 in (1.5 mm) holes are drilled 1/2 in (12.5 mm) inside the ends as shown (H).

Commencing at one end, the wire is fed through the 1/16 in holes in the three short and the three long spacers (Fig. 3 and Fig. 4). The sprung plastic spacers securely grip the wire. The spacers are next adjusted by sliding them along the wire to form the lengths shown in Fig. 3. Thin nylon cord is fed through the two end spacers of the horizontal section (Fig. 4) and fastened to hooks in the diagonal corners of the room, leaving the 4 ft (1.22 m) drop down to the resonator and the 2 ft (61 cm) down at the far end. At this stage, the spacers can be moved slightly on the wires to balance up the assembly.

If there is not sufficient space for the 16 ft 5 in (5 m) flat-top horizontal section, it can be shortened as required, but the length of the far-end drop-down section should be increased pro-rata--more about this later.

The resonator

The prototype resonator—see Fig. 2—was built into an aluminium box 8 in (20 cm) long by 4 in (10 cm) wide by 2.5 in (6.5 cm) high. The box was a double U shape with the front, bottom and back made from one piece of aluminium. The inverted U cover slips over this.

The size of the box is not very important, as long as good clearance is provided for coil *L*, which consists of 19 one-inch (25 mm) dia. turns of 16 SWG (1.6 mm dia) tinned copper wire with the turns spaced about 3/32 in (2.5 mm). The impedance matching tap on the prototype was located 10.75 turns up from the bottom end.

The coil was supported by a 1 in ceramic stand-off insulator at one end and at the other by the common grounding post formed by a thin 1.25 in (30 mm) long brass screw. Coaxial socket SKT_1 and banana socket SKT_2 are fitted at either end of the back as shown.

Variable capacitors C_1 and C_2 are fitted directly to the front panel. Though the rotor plates are obviously connected to the front panel, a wire is also taken from them to the common grounding post to reduce possible RF losses.

To bring the twin spaced down-leads of the antenna through the front panel, it is necessary to fit robust, well-insulated terminal posts or sockets. In the prototype, Archer 1.75 in (4.5 mm) nylon binding posts (Tandy/Radio Shack Type 274-662) were used. Internal unit wiring was in 16 SWG (1.6 mm dia) tinned copper wire with securely wrapped and soldered joints to keep potential RF losses to an absolute minimum.

Testing & operation

Assuming that the transmitter has a pi-network output, the resonator can be connected directly to the transmitter output socket ($Z=50\Omega$) via a few inches of RG58 coaxial cable. If the transmitter does not have a pi-network outpot, a good T-network transmatch should be inserted in the cable between resonator and transmitter.

The resonator will cover the entire 3.5–3.8 MHz (up to 4.0 MHz in some countries) band. This can be checked in the first instance with the receiver with C_2 set to minimum capacitance and C_1 set to 3.8 MHz (or, where appropriate, to 4.0 MHz). Rotation of C_2 then covers the whole band down to 3.5 MHz.

The impedance matching tap on coil *L* was earlier stated to be at 10.75 turns up from the common grounding post. As individual installations may vary slightly, the tap should be tried at one or two turns higher or lower to obtain minimum SWR (standing-wave ratio). On the prototype, no measurable harmonic radiation was detected, nor any TVI with the rod aerial of a portable TV close to the flat-top.

In operation, the usable bandwidth is about 60 kHz, which can be moved up or down the band with minimum adjustment of resonator control C, without touching frequency marker C_1 which can be locked once set. It was found that it was worth while trying to reverse the twin down-leads at the terminal posts, since radiation from the flat-top is slightly higher from the high-*i* limb—see Fig. 1.

The Flat-top 80 is quite amenable to adaptation to fit the space available. Assuming it is installed indoors, it should be slung diagonally across the room with the transmitter-receiver in the corner. The dimensions shown in Fig. 3 are as used on the prototype. However, the length of the flat-top can be reduced to about 12 ft 5 in (3.8 m) if the far-end drop-down leads are increased to about 6 ft (1.8 m) or some similar arrangement. There is plenty of scope for experiment.

If the Flat-top 80 is to be used outdoors, the twin down leads should arrive at the window with the resonator located just inside. Outdoors, of course, a higher power is permissible, but it will be necessary to make the 15 in and 6 in (38 cm and 15 cm) spacers of more rigid insulating material, and, perhaps, insert a few more spacers along the flat-top. If higher power is used, a higher working voltage may be required for C_1 and C_2, and possibly a thicker gauge of PVC covered wire. Experiment is the life blood of amateur radio . . . ■

Useful reading

Antennas, 2nd Edition, by Dr John D. Kraus (McGraw-Hill International).

and if you're lucky enough to have or find a copy:

The Admiralty Handbook of Wireless Telegraphy 1938

Handbook of Technical Instruction for Wireless Telegraphists, 7th Edition, 1942, by H.M. Dowsett & L.E.Q. Walker.

AF DRIVE INDICATOR

Design by T. Giesberts

A universal drive indicator is described that can be used with virtually any AF output amplifier. It indicates precisely when the –3 dB cut-off point and the clipping level of the amplifier are exceeded.

THE idea for the indicator arose during the development of the Class-A power amplifier[1]. That amplifier delivers 25 W into 8 Ω in Class A or 50 W in Class B. The 3 dB difference between these two levels seemed an excellent starting point for the design of a drive indicator that, with the aid of two LEDs, would show the –3 dB point and the point at which clipping would set in. That gives an an indication as to if and when there is power in reserve; moreover, the –3 dB LED will indicate when the transition from Class A to Class B takes place.

Nevertheless, the final design of the indicator is such that it can be used with any power amplifier operating from a symmetrical power supply of ±30–70 V. A –3 dB indicator is, of course, also very useful with Class-AB amplifiers, because the difference in sound pressure corresponding to a change of 3 dB in output power cannot be heard (in many cases, it is just *loud*).

As long as the –3 dB LED lights and the 0 dB (clipping) LED does not, the output is free of overdrive distortion. When the clipping LED lights, however, the output contains a great number of harmonics. The present indicator is, therefore, recommended for use with any power amplifier not provided with a drive indicator.

Circuit description

Although the circuit in Fig. 1 appears rather larger than expected, a glance at Fig. 2 shows that all the components fit readily on a fairly small printed-circuit board.

The monitoring section of the circuit consists of two pairs of comparators contained in a single LM339. That IC is not very fast, but fast enough for the present application. Its major advantage is that it draws only a tiny current, which is important in view of the fact that the indicator is intended for use with a large range of supply voltages.

One input of each comparator is connected to a potential divider, R_3–R_8, which provides the various reference voltages. Since the divider is connected directly to the supply voltage of the power amplifier via zener diodes D_1 and D_3, the switching levels of the comparators are adapted automatically to that supply voltage.

The two 2.7 V zener diodes at the ends of the divider serve to compensate the knee voltage that, with full drive to the output amplifier, remains across the power transistors and associated emitter resistors. This causes the clipping LED to light just before the actual clipping level is reached. In MOS-

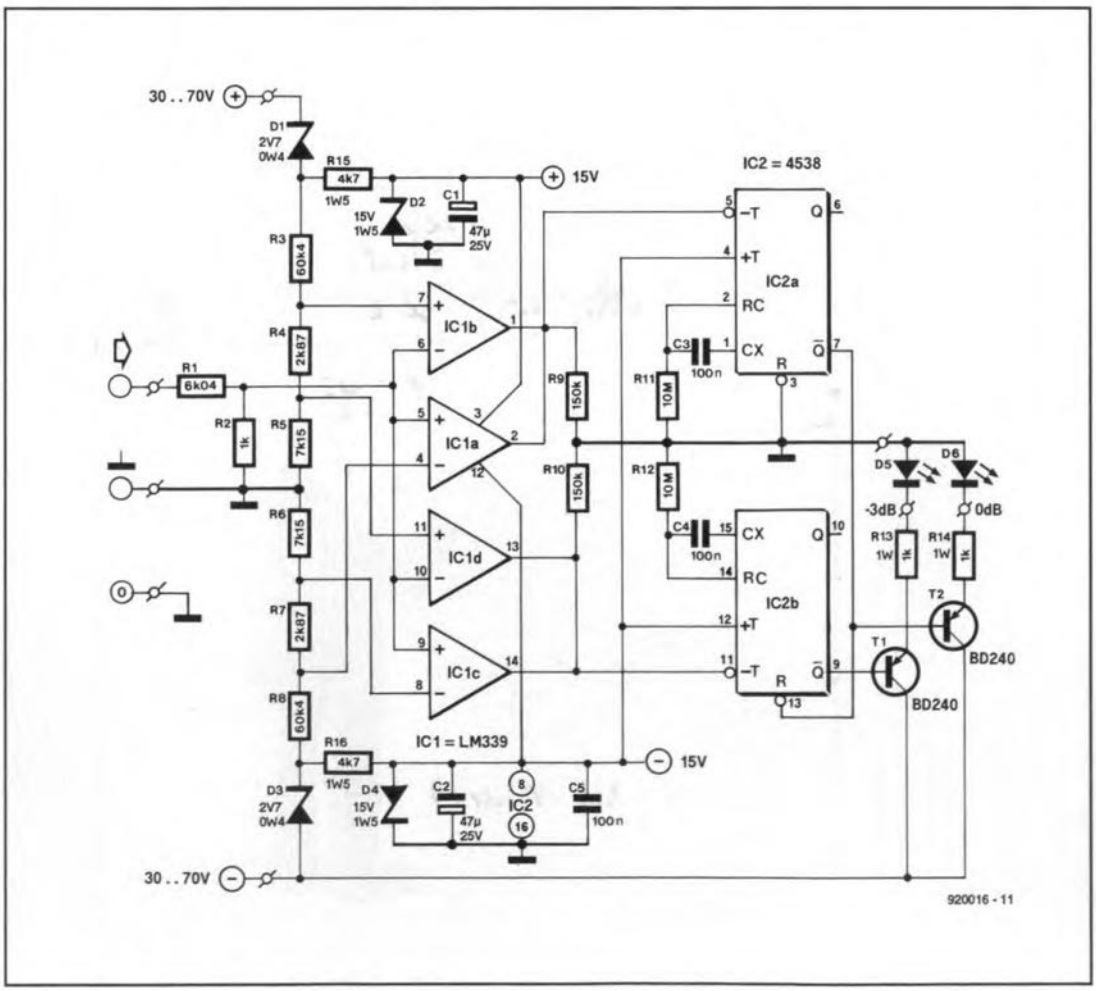


Fig. 1. Circuit diagram of the AF drive indicator.

PARTS LIST

Resistors:
R1 = 6.04 kΩ, 1%
R2 = 1 kΩ, 1%
R3, R8 = 60.4 kΩ, 1%
R4, R7 = 2.87 kΩ, 1%
R5, R6 = 7.15 kΩ, 1%
R9, R10 = 150 kΩ
R11, R12 = 10 MΩ
R13, R14 =1 kΩ, 1 W
R15, R16 = 4.7 kΩ, 1.5 W

Capacitors:
C1, C2 = 47 µF, 25 V, radial
C3, C4, C5 = 100 nF

Semiconductors:
D1, D3 = zener, 2.7 V, 400 mW (see text)
D2, D4 = zener, 15 V, 1.5 W
D5 = LED, 3 mm, not red
D6 = LED, 3 mm, red
T1, T2 = BD240
IC1 = LM339
IC2 = 4538

Miscellaneous:
PCB Type 920016

[1] *Elektor Electronics* November-December 1991.

FET output amplifiers in a source-follower configuration, it is usually necessary to use 10–12 V zener diodes because of the much higher quiescent voltage across MOSFET devices. To be on the safe side, measure the maximum output voltage across the nominal load and choose correspondingly rated zener diodes.

The input signal to the indicator, that is, the output of the power amplifier, is applied across potential divider R_1–R_2. The resulting attenuation of the signal is necessary to prevent the inputs to the comparators exceeding 10 V. With values shown, the circuit is suitable for use with power amplifiers rated up to 300 W into 8 Ω.

The output of IC_{1d} toggles (changes state) when the half-power level (equivalent to 0.707 of the peak output voltage) is exceeded in the positive half period of the signal. The output of IC_{1c} toggles when the half-power level in the negative half period of the signal is exceeded.

When full power level is reached in the positive half-period, the output of IC_{1b} toggles. Similarly, when the full power level is reached in the negative half period, the output of IC_{1a} changes state.

In this way, an accurate indication is obtained of a power excess in the positive as well as in the negative half period of the signal.

The (open-collector) outputs of IC_{1d} and IC_{1c}, and those of IC_{1a} and IC_{1b}, are interconnected in parallel. Each linked pair is connected to a monostable, IC_{2a} and IC_{2b} respectively. These multivibrators ensure that short pulses emanating from the comparators are stretched sufficiently to guarantee a reasonably long lighting time of the LEDs. Their mono period is set to 1 second (time constants R_{11}-C_3 and R_{12}-C_4).

The LEDs are connected to the $\overline{Q}$ outputs of IC_{2a} and IC_{2b} via switching transistors T_1 and T_2. Combinations T_1-R_{13} and T_2-R_{14} form current sources, because the $\overline{Q}$ outputs of the monostables switch neatly between 0 V and –15 V, irrespective of the output amplifier power supply. Consequently, the current drawn by the diodes—about 15 mA per diode—need not be regulated.

To recap the switching operation: when the reference level of one of the comparators is exceeded, the output of that comparator goes low. The resulting (negative) transition triggers the –T input of the relevant monostable, whose $\overline{Q}$ output (high during quiescent operation) thereupon becomes 0 for 1 s (mono period). The transistor connected to that output is switched on and the associated LED lights.

The $\overline{Q}$ output of IC_{2a} and the reset input of IC_{2b} are interlinked to ensure that when the 0 dB LED lights, IC_{2b} is reset and the –3 dB LED goes out. At any one time, therefore, only one of the LEDs can light.

The supply for the ICs is derived from the power amplifier supply via R_{15} and R_{16} and regulated by D_2 and D_4. Because IC_1 draws only a small current, the diode current is a mere 2.5 mA. That is sufficient to ensure correct operation and low dissipation in R_{15} and R_{16}, even with high supply voltages in the power amplifier.

Construction

The printed-circuit board—see Fig. 2—is small enough to be fitted in almost any power amplifier. Note that the board must be cut into two if the indicator is to be used with mono amplifiers or stereo amplifiers with split power supplies. The indication remains correct, even when the supply voltage for one channel drops temporarily owing to a high drive level. The board can, of course, be left intact when used with a stereo amplifier.

Virtually all components are mounted upright. Start with placing the wire links between IC_1 and IC_2. The ICs may be inserted in appropriate sockets, but that is not essential.

In view of their dissipation, mount R_{13}–R_{16} a little above the board.

The connections to the power amplifier consist of three wires to its power supply, for instance, +, 0 and –, which are usually within easy (soldering) reach, and a single-core screened wire between each loudspeaker terminal (after the relay) and each indicator input. Earth the screen of the latter cable only on the indicator board (beside the input terminal). DO NOT CONNECT THE 0 AND EARTH LINES WITH THE AMPLIFIER BECAUSE THAT CREATES A (POTENTIALLY DEGRADING) EARTH LOOP.

If at all possible, place the board directly behind the front panel of the amplifier so that the LEDs can be seen through two small holes (to be drilled). Otherwise, the two LEDs can be fitted behind the front panel and the PCB elsewhere: interconnection between them is by simple circuit wire, whose length is not critical. ■

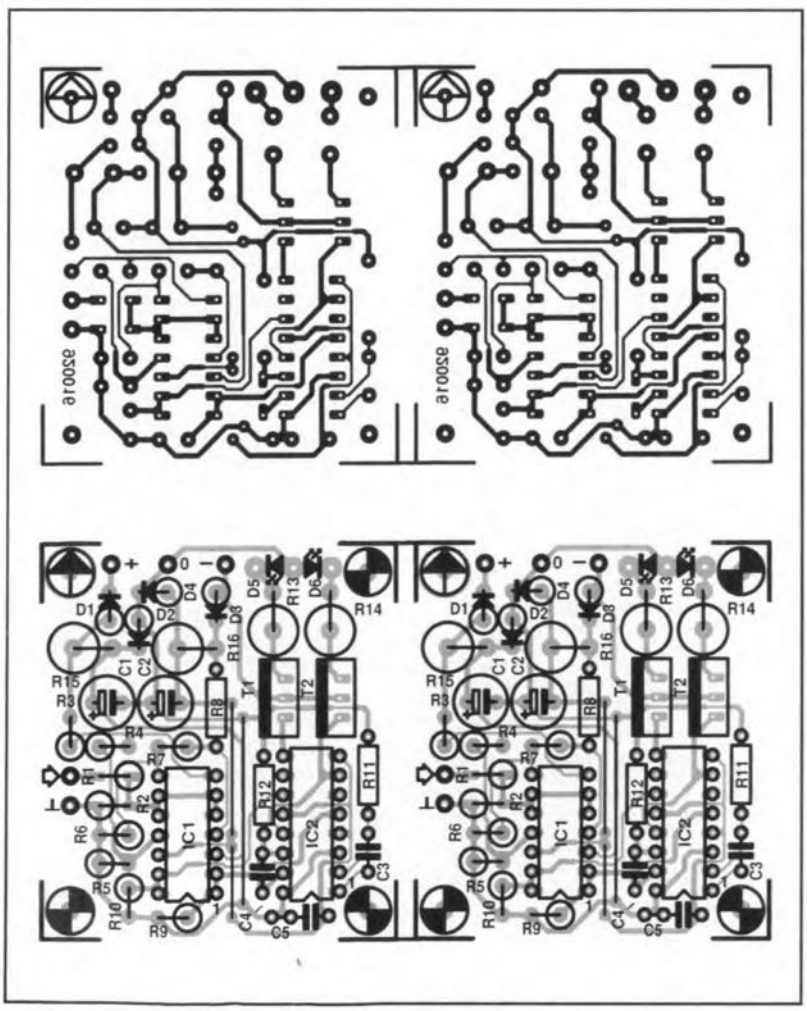


Fig. 2. Printed-circuit board for the AF drive indicator.

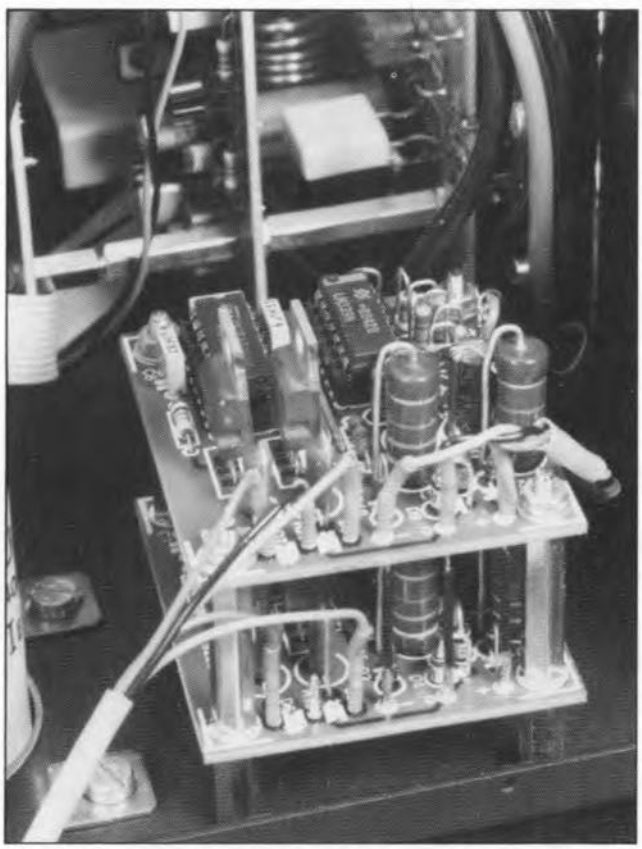


Fig. 3. One way of fitting the drive indicator in the power amplifier.

holes (to be drilled). Otherwise, the two LEDs can be fitted behind the front panel and the PCB elsewhere: interconnection between them is by simple circuit wire, whose length is not critical. ■

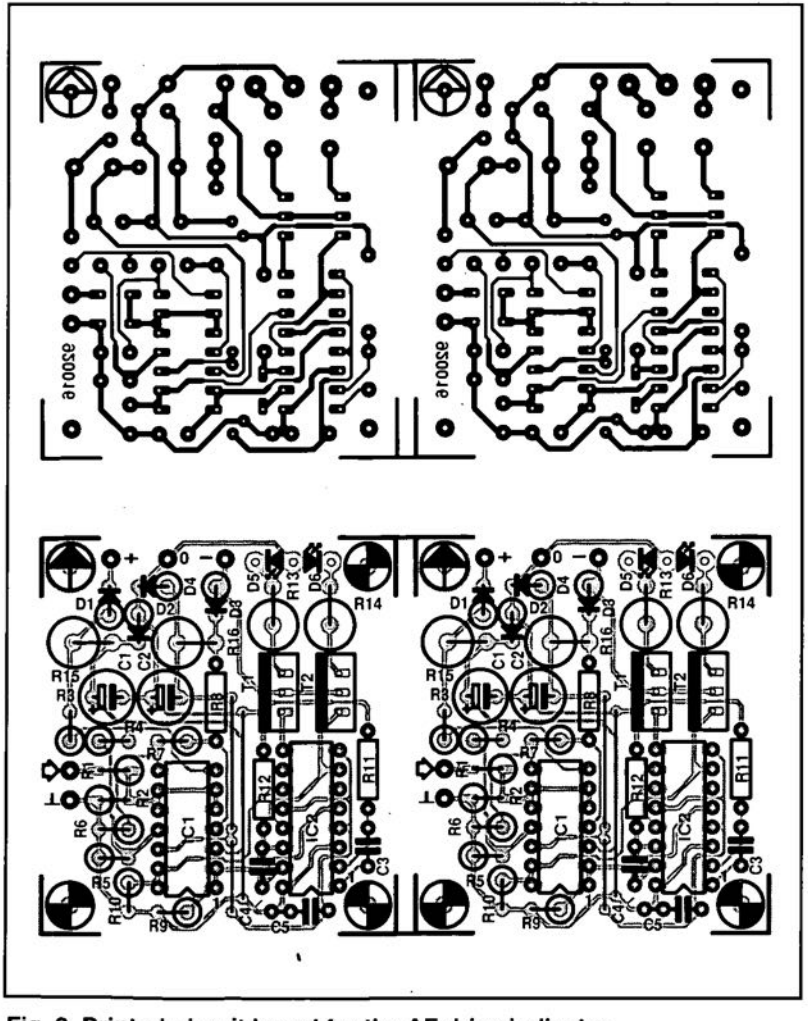


Fig. 2. Printed-circuit board for the AF drive indicator.

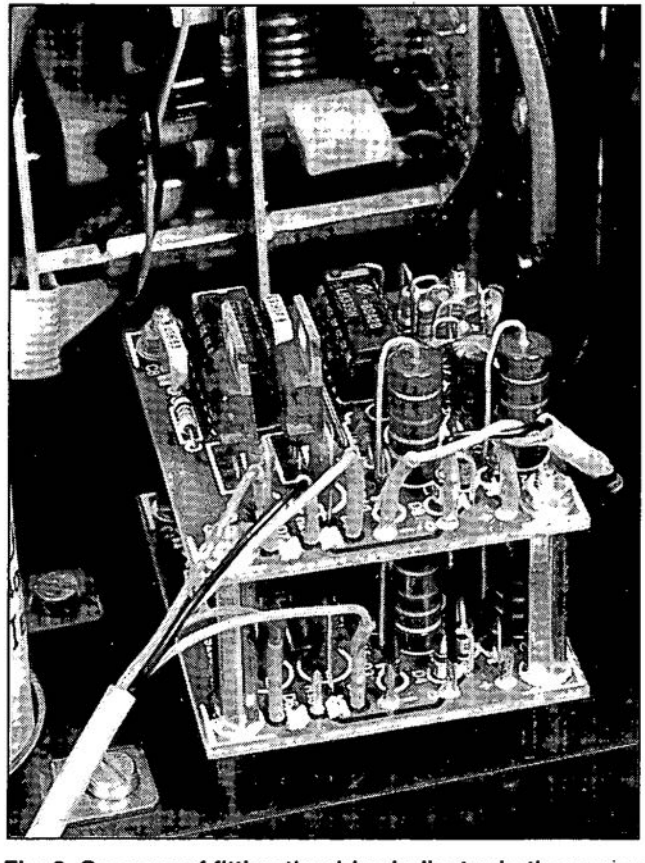


Fig. 3. One way of fitting the drive indicator in the power amplifier.

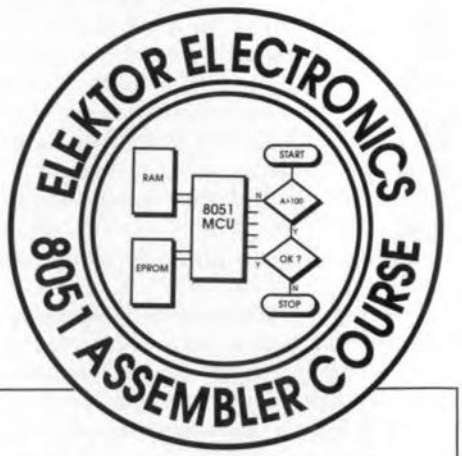
8051/8032 ASSEMBLER COURSE

PART 2: FIRST 8051 INSTRUCTIONS

by Dr. M. Ohsmann

g10109-III

Following last month's introduction to the course, we are now well armed and ready to discuss the first instructions of the 8051 family of microcontrollers. At the same time, addressing methods are tackled, all with the aid of the programming examples and other utilities contained on the course diskette.



ARITHMETIC OPERATIONS

Mnemonic		Description	Byte	Cyc
ADD	A,Rn	Add register to Accumulator	1	1
ADD	A,direct	Add direct byte to Accumulator	2	1
ADD	A,@Ri	Add indirect RAM to Accumulator	1	1
ADD	A,#data	Add immediate data to Accumulator	2	1
ADDC	A,Rn	Add register to Accumulator with Carry	1	1
ADDC	A,direct	Add direct byte to A with Carry flag	2	1
ADDC	A,@Ri	Add indirect RAM to A with Carry flag	1	1
ADDC	A,#data	Add immediate data to A with Carry flag	2	1
SUBB	A,Rn	Subtract register from A with Borrow	1	1
SUBB	A,direct	Subtract direct byte from A with Borrow	2	1
SUBB	A,@Ri	Subtract indirect RAM from A w/ Borrow	1	1
SUBB	A,#data	Subtract immed. data from A w/ Borrow	2	1
INC	A	Increment Accumulator	1	1
INC	Rn	Increment register	1	1
INC	direct	Increment direct byte	2	1
INC	@Ri	Increment indirect RAM	1	1
DEC	A	Decrement Accumulator	1	1
DEC	Rn	Decrement register	1	1
DEC	direct	Decrement direct byte	2	1
DEC	@Ri	Decrement indirect RAM	1	1
INC	DPTR	Increment Data Pointer	1	2
MUL	AB	Multiply A & B	1	4
DIV	AB	Divide A by B	1	4
DA	A	Decimal Adjust Accumulator	1	1

LOGICAL OPERATIONS

Mnemonic		Destination	Byte	Cyc
ANL	A,Rn	AND register to Accumulator	1	1
ANL	A,direct	AND direct byte to Accumulator	2	1
ANL	A,@Ri	AND indirect RAM to Accumulator	1	1
ANL	A,#data	AND immediate data to Accumulator	2	1
ANL	direct,A	AND Accumulator to direct byte	2	1
ANL	direct,#data	AND immediate data to direct byte	3	2
ORL	A,Rn	OR register to Accumulator	1	1
ORL	A,direct	OR direct byte to Accumulator	2	1
ORL	A,@Ri	OR indirect RAM to Accumulator	1	1
ORL	A,#data	OR immediate data to Accumulator	2	1
ORL	direct,A	OR Accumulator to direct byte	2	1
ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive-OR register to Accumulator	1	1
XRL	A,direct	Exclusive-OR direct byte to Accumulator	2	1
XRL	A,@Ri	Exclusive-OR indirect RAM to A	1	1
XRL	A,#data	Exclusive-OR immediate data to A	2	1
XRL	direct,A	Exclusive-OR Accumulator to direct byte	2	1
XRL	direct,#data	Exclusive-OR immediate data to direct	3	2
CLR	A	Clear Accumulator	1	1
CPL	A	Complement Accumulator	1	1
RL	A	Rotate Accumulator Left	1	1
RLC	A	Rotate A Left through the Carry flag	1	1
RR	A	Rotate Accumulator Right	1	1
RRC	A	Rotate A Right through Carry flag	1	1
SWAP	A	Swap nibbles within the Accumulator	1	1

DATA TRANSFER

Mnemonic		Description	Byte	Cyc
MOV	A,Rn	Move register to Accumulator	1	1
MOV	A,direct	Move direct byte to Accumulator	2	1
MOV	A,@Ri	Move indirect RAM to Accumulator	1	1
MOV	A,#data	Move immediate data to Accumulator	2	1
MOV	Rn,A	Move Accumulator to register	1	1
MOV	Rn,direct	Move direct byte to register	2	2
MOV	Rn,#data	Move immediate data to register	2	1
MOV	direct,A	Move Accumulator to direct byte	2	1
MOV	direct,Rn	Move register to direct byte	2	2
MOV	direct,direct	Move direct byte to direct	3	2
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2
MOV	direct,#data	Move immediate data to direct byte	3	2
MOV	@Ri,A	Move Accumulator to indirect RAM	1	1
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
MOV	DPTR,#data16	Load Data Pointer with a 16-bit constant	3	2

DATA TRANSFER (cont.)

Mnemonic		Description	Byte	Cyc
MOVC	A,@A+DPTR	Move Code byte relative to DPTR to A	1	2
MOVC	A,@A+PC	Move Code byte relative to PC to A	1	2
MOVX	A,@Ri	Move External RAM (8-bit addr) to A	1	2
MOVX	A,@DPTR	Move External RAM (16-bit addr) to A	1	2
MOVX	@Ri,A	Move A to External RAM (8-bit addr)	1	2
MOVX	@DPTR,A	Move A to External RAM (16-bit addr)	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct	Pop direct byte from stack	2	2
XCH	A,Rn	Exchange register with Accumulator	1	1
XCH	A,direct	Exchange direct byte with Accumulator	2	1
XCH	A,@Ri	Exchange indirect RAM with A	1	1
XCHD	A,@Ri	Exchange low-order Digit ind. RAM w A	1	1

BOOLEAN VARIABLE MANIPULATION

Mnemonic		Description	Byte	Cyc
CLR	C	Clear Carry flag	1	1
CLR	bit	Clear direct bit	2	1
SETB	C	Set Carry flag	1	1
SETB	bit	Set direct Bit	2	1
CPL	C	Complement Carry flag	1	1
CPL	bit	Complement direct bit	2	1
ANL	C,bit	AND direct bit to Carry flag	2	2
ANL	C,/bit	AND complement of direct bit to Carry	2	2
ORL	C,bit	OR direct bit to Carry flag	2	2
ORL	C,/bit	OR complement of direct bit to Carry	2	2
MOV	C,bit	Move direct bit to Carry flag	2	1
MOV	bit,C	Move Carry flag to direct bit	2	2

PROGRAM AND MACHINE CONTROL

Mnemonic		Description	Byte	Cyc
ACALL	addr11	Absolute Subroutine Call	2	2
LCALL	addr16	Long Subroutine Call	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr11	Absolute Jump	2	2
LJMP	addr16	Long Jump	3	2
SJMP	rel	Short Jump (relative addr)	2	2
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if Accumulator is Zero	2	2
JNZ	rel	Jump if Accumulator is Not Zero	2	2
JC	rel	Jump if Carry flag is set	2	2
JNC	rel	Jump if No Carry flag	2	2
JB	bit,rel	Jump if direct Bit set	3	2
JNB	bit,rel	Jump if direct Bit Not set	3	2
JBC	bit,rel	Jump if direct Bit is set & Clear bit	3	2
CJNE	A,direct,rel	Compare direct to A & Jump if Not Equal	3	2
CJNE	A,#data,rel	Comp. immed. to A & Jump if Not Equal	3	2
CJNE	Rn,#data,rel	Comp. immed. to reg. & Jump if Not Equal	3	2
CJNE	@Ri,#data,rel	Comp. immed. to ind. & Jump if Not Equal	3	2
DJNZ	Rn,rel	Decrement register & Jump if Not Zero	2	2
DJNZ	direct,rel	Decrement direct & Jump if Not Zero	3	2
NOP		No operation	1	1

Notes on data addressing modes:

Rn	Working register R0–R7
direct	128 internal RAM locations, any I/O port, control or status register
@Ri	Indirect internal RAM location addressed by register R0 or R1
#data	8-bit constant included in instruction
#data16	16-bit constant included as bytes 2 & 3 of instruction
bit	128 software flags, any I/O pin, control or status bit

Notes on program addressing modes:

addr16	Destination address for LCALL & LJMP may be anywhere within the 64-Kilobyte program memory address space.
addr11	Destination address for ACALL & AJMP will be within the same 2-Kilobyte page of program memory as the first byte of the following instruction.
rel	SJMP and all conditional jumps include an 8-bit offset byte. Range is +127 –128 bytes relative to first byte of the following instruction.

Fig. 5. MCS-52 microcontroller instruction set (courtesy Intel Corp.).

```
****** LISTING of EASM51 (XAMPLE02) ******
LINE LOC  OBJ          T     SOURCE
   1 0000                    ; ****** FILE XAMPLE02.A51 ************************************
   2 0000                    ;
   3 0000                    ACC     EQU   0E0H          ; SFR Accumulator address is 0E0H
   4 0000                    P1      EQU   090H          ; SFR PORT1 Address is 090H
   5 0000                    xR3     EQU   3             ; Adress of register R3 in Bank 0
   6 0000                    VALU    EQU   100
   7 0000                    ;
   8 0000                            ORG   4100H         ; Program to run from 4100H
   9 4100 90 41 44 [2] START   MOV   DPTR,#txt1
  10 4103 31 49    [2]              ACALL STXT
  11 4105 74 00    [1]              MOV   A,#0          ; Initialise registers
  12 4107 78 FF    [1]              MOV   R0,#255       ; = 0FFH hexadecimal
  13 4109 79 0A    [1]              MOV   R1,#10        ; 10 decimal = 0AH hexadecimal
  14 410B 7A 10    [1]              MOV   R2,#10H       ; 10H hexadecimal is 16 decimal
  15 410D 7B 64    [1]              MOV   R3,#VALU      ; compare to EQU command above
  16 410F 90 40 00 [2]              MOV   DPTR,#04000H  ; load 16-bit constant
  17 4112 31 4F    [2]              ACALL SNAP          ; do first snapshot
  18 4114 74 14    [1]              MOV   A,#20         ; Addressing: immediate
  19 4116 F9       [1]              MOV   R1,A          ; Addressing: register,A
  20 4117 31 4F    [2]              ACALL SNAP
  21 4119 75 E0 12 [2]              MOV   ACC,#12H      ; Addressing: direct,immediate
  22 411C F5 03    [1]              MOV   xR3,A         ; Addressing: direct,A
  23 411E 31 4F    [2]              ACALL SNAP
  24 4120 78 02    [1]              MOV   R0,#2         ; Addressing: register,immediate
  25 4122 C6       [1]              XCH   A,@R0         ; Addressing: A,indirect
  26 4123 75 90 55 [2]              MOV   P1,#01010101B ; binary constant to port
  27 4126 31 4F    [2]              ACALL SNAP
  28 4128 90 41 2B [2]              MOV   DPTR,#addr1   ; point at MOV  A,#2 instruction
  29 412B 74 02    [1] addr1        MOV   A,#2          ; Address offset
  30 412D 93       [2]              MOVC  A,@A+DPTR     ; Addressing: A,code-byte relative
  31 412E 31 4F    [2]              ACALL SNAP
  32 4130 E0       [2]              MOVX  A,@DPTR       ; Addressing: A,external RAM
  33 4131 A9 02    [2]              MOV   R1,2          ; quizzzz
  34 4133 31 4F    [2]              ACALL SNAP
  35 4135 90 00 00 [2]              MOV   DPTR,#0       ; Addressing; DPTR,16-bit immediate
  36 4138 74 F2    [1]              MOV   A,#0F2H       ; external data latch Addr 0 = 0F2H
  37 413A F0       [2]              MOVX  @DPTR,A
  38 413B 74 00    [1]              MOV   A,#0          ; Program memory offset
  39 413D 93       [2]              MOVC  A,@A+DPTR     ; Addressing: A,code-byte relative
  40 413E 31 4F    [2]              ACALL SNAP
  41 4140 E0       [2]              MOVX  A,@DPTR       ; Addressing: A,external RAM
  42 4141 31 4F    [2]              ACALL SNAP
  43 4143 22       [2]              RET                 ; return to MONITOR
  44 4144 58 4D 50     txt1        DB 'XMP2',0
          32 00
  45 4149                   ;
  46 4149                   ;  MONITOR INTERFACE
  47 4149                   ccSTXT  EQU  2      ; MONITOR command to send text
  48 4149                   ccSNAP  EQU  020H   ; MONITOR commando to do snapshot
  49 4149                   COMMAND EQU  030H   ; MONITOR commando memory location
  50 4149                   MON     EQU  0200H  ; MONITOR start address
  51 4149                   ;
  52 4149 75 30 02 [2] STXT   MOV COMMAND,#ccSTXT  ; MONITOR set command
  53 414C 02 02 00 [2]        LJMP MON             ; jump to MONITOR (RET from there)
  54 414F 75 30 20 [2] SNAP   MOV COMMAND,#ccSNAP  ; MONITOR set command
  55 4152 12 02 00 [2]        LCALL MON            ; call up monitor
  56 4155 22       [2]        RET                  ; return to caller
  57 4156                     END
********** SYMBOLTABLE (13 symbols) **********
       ACC :00E0      P1 :0090      xR3 :0003     VALU :0064
     START :4100   addr1 :412B     txt1 :4144   ccSTXT :0002
   ccSNAP :0020 COMMAND :0030      MON :0200     STXT :4149
      SNAP :414F
```

Fig. 6. LIST file of example program XAMPL02.A51.

All information pertinent to the monitor EPROM and the operation of the assembler may be found in the documentation (.DOC) files on the course diskette. The programs discussed and listed in the course instalments are also available to you on the same disk, which allows you to modify them as required. All you need to examine and edit these programs is a word processor capable of handling ASCII files. How this word processor can be linked to the MENU program is explained in a text file on the disk.

Further details on the serial link between the 80C32 board and the PC will be given in next month's instalment, which will concentrate mostly on hardware extensions for the 80C32 computer (keyboard input, liquid crystal display, MIDI interface).

8051 (MCS52)micro controller instruction set

Figure 5 shows the instruction set of the MCS52 family of microcontrollers, of which the 8051 and 80C32 are members of particular interest to us. To begin with, we will discuss some of the simpler instructions in order to elucidate the operation of the example program listed in Fig. 6.

The structure of the list (.LST) file is pretty obvious: it consists of seven columns, each with a specific function. The list file shown is generated by assembling XAMPLE02.A51 on the course disk, with the aid of EASM51. The column marked **LINE** shows the line number of the source text, while **LOC** shows location of the object code on the program memory. The column **OBJ** shows the object code bytes, and **T** the execution time of the individual instructions in microseconds (based on a system clock frequency of 12 MHz). The **SOURCE** column repeats the information copied from the assembler (source) file (in this case, XAMPLE02.A51), and shows mnemonics, labels, addresses, equate statements and comment. As you can see, the list file is extremely useful because it relates opcode bytes to the line numbers by which they have been generated.

The format requirements for the source file (produced with the ASCII word processor) are found on the course disk. For now, you may simply use XAMPLE02.A51 and the associated documentation file, XAMPLE02.DOC, both of which are contained on the disk. Connect the PC and the 80C32 board via the serial link, and run the monitor on the SBC.

The various addressing methods of the MCS52 microcontrollers will be discussed in relation to the available MOV (move) instructions. To illustrate their practical use, a small program is discussed that lights a couple of LEDs, and produces tone sequences. A simple modification to this program allows you to realize a simple tea timer, which generates a tone after 2 minutes and 50 seconds.

Subroutines

What we call a computer program normally consists of a number of smaller subroutines. Once written, a subroutine can be called repeatedly later. In XAMPLE02 you find, for instance, a subroutine called STXT (send text), which sends text from the 80C32 board to the terminal via the V24 interface. In 8051 assembler, subroutines can be called in two ways:

ACALL addr11
LCALL addr16

Both instructions have the same result: they start a subroutine at the indicated address (addr11 or addr16). On finishing the

JOIN THE COURSE!

Here is a breakdown of what you need to follow this course:

- **a 8032/8052AH-BASIC single board computer as described in Elektor Electronics May 1991. The preferred CPU is a 8051 or a 80C32. Alternatively, any other MCS52-based microcontroller system (but read part 1 of the course);**
- **a course diskette (order code ESS 1661) containing programming examples, utilities, and an assembler;**
- **a monitor EPROM (order code ESS 6091).**
- **an IBM PC or compatible operating under MS-DOS.**

Appeared so far:
Part 1: Introduction (February 1992).

XAMPL02

A	B	PSW	SP	DPTR	R0	R1	R2	R3	R4	R5	R6	R7	
00	00	00	0D	4000	FF	0A	10	64	00	00	00	00	after line 17
14	00	00	0D	4000	FF	14	10	64	00	00	00	00	after line 20
12	00	00	0D	4000	FF	14	10	12	00	00	00	00	after line 23
10	00	01	0D	4000	02	14	12	12	00	00	00	00	after line 27
93	00	00	0D	412B	02	14	12	12	00	00	00	00	after line 31
74	00	00	0D	412B	02	12	12	12	00	00	00	00	after line 34
02	00	01	0D	0000	02	12	12	12	00	00	00	00	after line 40
F2	00	01	0D	0000	02	12	12	12	00	00	00	00	after line 42

Fig. 7. Output of XAMPL02, produced with the aid of the 'snapshot' (register freeze) utility in the system monitor.

subroutine, the processor continues with the instruction that follows the CALL.

ACALL (absolute call) is used when the subroutine address is in the same 2-KByte address area as the CALL. This means that the highest 5 bits of the 16-bit address must be equal. If, for example, ACALL is used at address 9A12H, the relevant subroutine may be anywhere in the range between 9800H and 9FFFH. ACALL requires two bytes.

LCALL (long call) enables a subroutine anywhere in the 64-KByte address area to be called. Obviously, in relatively large programs, subroutines may be pretty 'remote', and can not be called with ACALL. In that case, you must use LCALL, which requires three bytes. The assembler produces an error report if an ACALL is made to a too distant subroutine. An example of the use of the LCALL instruction may be found in line 55 in Fig. 6. Here, ACALL can not be used because the called subroutine (at 0200H) is too far away from the call location (at 4152H).

RET is used at the end of a subroutine to return to the call instruction. The RET instruction at line 43, for example, ends the example program, and returns us to the monitor.

Jump instructions

The first jump instructions to be discussed are:

SJMP rel
AJMP addr11
LJMP addr16

These instructions cause the processor to jump to the indicated address (rel, addr11 or addr16), and are unconditional. The A and L preceding JMP have the same meaning as those used for the two types of CALL instruction discussed above. In addition, there is SJMP (short jump), which allows jumps to addresses within the range +128 bytes and −128 bytes from the location of the SJUMP instruction. SJUMP is often used to skip a few bytes—an example is found in line 53 of the listing in Fig. 6.

Apart from unconditional jumps, there are also jump instructions that are not executed unless a certain condition is met. Conditional jumps are of the short jump type only, and will be discussed separately in due course.

Address indications

The target addresses of subroutines are entered into the source listing as **LABELS**, on which further information may be found in the file EASM51.DOC. In line 54 of the list file of XAMPLE02 (Fig. 6), a subroutine called **SNAP** (for snapshot) is assigned the value that equals the address of the next instruction, i.e., 414FH. In line 50, you find an equate (**EQU**) statement is used to assign the value 0200H to the routine labelled **MON** (monitor). Hence, the command

LCALL MON

calls up the monitor subroutine. Similarly, the command

ACALL SNAP

calls the snapshot routine at 414FH, which is basically a breakpoint analyser that sends the contents of the main processor registers (in hexadecimal notation) to the terminal, via the serial interface. The use of this debugging aid is shown in Fig. 7.

Assembler listings are far easier to follow if meaningful labels are used. An example is the label **COMMAND** in lines 49, 52 and 54 of the list file. The actual addresses given to the labels are easily found in the **symbol table**, which is automatically added to the list file by the assembler. Many assemblers have a maximum label length of six characters, hence the frequent use of labels such as V24COM (for the serial interface routines) or SNDCHR for send character. The EASM51 assembler (on your disk) allows up to eight characters to be used for labels.

Addressing methods

The function of the program XAMPLE02 (Fig. 6) is to elucidate the operation and application of the various addressing modes of the microcontrollers in the 8051 family. After a few initial assembler commands and some comment, the program proper starts at line 9. First, the accumulator, A, and a few registers are loaded. Line 17 calls up SNAP, which sends the first register overview to the terminal. The output produced by XAMPLE02 is shown in Fig. 7. This overview allows the operation of the instructions between lines 11 and 42 to be analysed in detail with the aid of a number of snapshots. Line 45 and further serve to re-establish the control of the monitor program, and are not so important at this stage.

The MOV (move) command is used to load a byte from the program, data or internal memory to a processor register or a PORT. The byte moved is referred to as the **operand**. A number of addressing modes are used depending on the source and target location of the operand, and the function required. The general notation of the MOV instruction is

MOV target,source

The target is, for instance, the accumulator, A, a register (R0 to R7), or one of the different types of memory. Constants may be used as the source, although not all combinations are possible (see the instruction set in Fig. 5).

The different addressing methods will be discussed with reference to the example program in Fig. 6. The so-called bit-addressing modes will be held over till part 4 of the course, together with a discussion on the processor flags.

Register addressing

The accumulator or registers R0 to R7 may be used as the source as well as the target.

For example, in line 11, the accumulator is used as the target, while in line 13 the target is register R1.

When register addressing is applied, the register is always one in the currently selected bank (bank 0 is used during this course).

Immediate addressing

This addressing mode is used when a constant is used as the (source) operand. The assembler recognizes such constants by the # (hash) typed in front of them. The constant may be entered in four ways: decimal (as in line 12), hexadecimal (as in line 14; note the affixed H), binary (as in line 26; note the affixed B), or it may be a label (as in line 15). To enable the assembler to differentiate between labels and hexadecimal numbers that start with a letter, hexadecimal numbers must start with a 0 (nought). For example, E0H is a label, and 0E0H a hexadecimal constant with the value 224 (decimal).

This information should enable you to understand the instructions in lines 11 to 15, which load the registers with the indicated values. At this stage, it may be useful to check if you understand what happens by taking a close look at the program output shown in Fig. 7.

Direct addressing

Direct addressing allows access to the lower 128 bytes of the internal RAM and the special function registers (SFRs). The internal RAM is selected when the indicated address is smaller than 128. Else, one of the SFRs is addressed. The accumulator can also be addressed as an SFR at location 0E0H. In line 3, this constant is labelled ACC. Line 21 causes a constant to be loaded into the accumulator. Note that this instruction has a length of three bytes.

On the 80C32 processor board, port P1 is made externally accessible, and is located at SFR address 090H (line 4). The instruction in line 26 sends bit pattern 01010101B to this port.

The 16-bit wide data pointer, **DPTR**, makes it possible to address the full 64 Kbyte large data and program memory. The DPTR consists of two 8-bit SFRs: the low byte pointer, DPL, at 082H, and the high byte pointer, DPH at 083H. A special MOV instruction is available to load the DPTR with a 16-bit value, as illustrated in line 9, where the DPTR is set to point at the first byte of the text 'txt1'. Figure 8 lists the functions of all SFRs.

Indirect addressing

This addressing mode is indicated by **@R0** or **@R1**. The address of the byte in the internal RAM is contained in register R0 or R1 as indicated. Registers R2 to R7 can not be used for indirect addressing. When, for instance, register R0 contains the value 43H, the instruction @R0 addresses the byte at location 43H in the internal memory. The use of this addressing mode is illustrated in line 25, where R0 is seen to point at internal memory location 2 (as defined in line 24). This is the same location, however, where register R2 in bank 0 is addressed (see Fig. 4 in part 1 of this course). Hence, this instruction changes the value contained in register R2. The instruction **XCH** swaps target and source bytes.

Contrary to direct addressing, addresses greater than 127 do not give access to the SFRs. Instead, they select the upper 128 bytes of the internal RAM. In fact, these RAM locations can be accessed via indirect addressing only.

```
Symbol    ADR   bit   binval        comment     name

ACC       0E0CH *     00000000B                 accumulator
B         0F00H *     00000000B                 aux. accumulator
PSW       0D0H  *     00000000B                 program status word
SP        081H        00000111B                 stack pointer
DPTR                                16-bit      data pointer
  DPL     082H        00000000B                 low byte of DPTR
  DPH     083H        00000000B                 high byte of DPTR
P0        080H  *     11111111B                 port 0 or addr./databus
P1        090H  *     11111111B                 port 1
P2        0A0H  *     11111111B                 port 2 or addr. bus MSB
P3        0B0H  *     11111111B                 port 3
IP        0B8H  *     xxx00000B     8051        interrupt priority reg.
                      xx000000B     8052
IE        0A8H  *     0xx00000B     8051        interrupt enable reg.
                      0x000000B     8052
TMOD      089H        00000000B                 timer mode register
TCON      088H  *     00000000B                 timer control
T2CON     0C8H  *     00000000B     8052 only   timer-2 control
TH0       08CH        00000000B                 timer-0 high byte
TL0       08AH        00000000B                 timer-0 low byte
TH1       08DH        00000000B                 timer-1 high byte
TL1       08BH        00000000B                 timer-1 low byte
TH2       0CDH        00000000B     8052 only   timer-2 high byte
TL2       0CCH        00000000B     8052 only   timer-2 low byte
RCAP2H    0CBH        00000000B     8052 only   capture reg. high byte
RCAP2L    0CAH        00000000B     8052 only   capture reg. low byte
SCON      098H  *     00000000B                 serial control
SBUF      099H        xxxxxxxxB                 serial buffer
PCON      087H        0xxxxxxxB     HMOS        processor control
                      0xxx0000B     CHMOS

ADR:     location of addressed SFR
bit:     * when SFR is bit-addressable
binval:  binary content after reset; x = not defined
```

Fig. 8. Identifications and addresses of the special function registers (SFRs) in the 8051.

Program memory addressing

The processor can only read from the program memory, which is normally a ROM or an EPROM. For this the **MOVC** instruction is used, where the C stands for code memory. The target of MOVC is always the accumulator. The real (effective) address is formed by adding the content of the accumulator to either the data pointer, DPTR:

```
MOVC A, @A+DPTR
```

or the program counter, PC:

```
MOVC A, @A+PC
```

In line 39, the effective address is 0, since both the DPTR and A are loaded with 0.

Tables and fixed texts can be stored permanently in the program memory, and read when required with the aid of the DPTR. The routine STXT in the monitor, EMON51, makes use of the DPTR in this way to transmit texts to the terminal.

(External) data memory addressing

The **MOVX** (move eXternal) instruction gives access to the external data memory, which is usually a RAM. When the notation @DPTR is used, as in line 37 or 41, the contents of the data pointer are used as a 16-bit address. Similarly, the notations @R0 and @R1 cause the contents of these registers to be used as the least significant address byte, and the contents of port P2 (at SFR location 0A0H) as the most significant address byte. On the 80C32 SBC, the address range between 0C000H and 0FFFFH in the data memory is used for memory mapped I/O. If, therefore, you wish to select output devices at these addresses, you must use the MOVX instruction.

Monitor calls

The EPROM-resident monitor on the 80C32 board has a number of subroutines that may be used in your own programs.

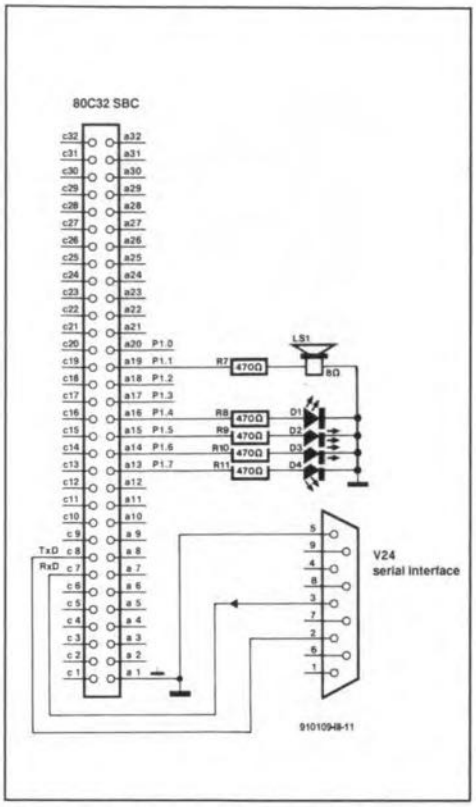


Fig. 9. Hardware extension for programming experiments with port 1.

Before these subroutines can be called, an appropriate command byte must be written into the internal RAM at address 030H (see lines 52 and 54 of XAMPLE02.LST). This byte forms an indication to the monitor as to which subroutine is to be used. The routines available in the monitor, along with the associated command bytes, are described in the file EMON51.DOC on your course diskette. These routines are useful, and can save you a lot of work. You are, therefore, well advised to examine them in detail, which is quite easily done because the source code of EMON51 can be loaded from the course disk.

A SNAP can be taken at any stage during a program. This requires command byte 20H before calling the monitor at address 0200H. A programming example:

```
MOV 030H,#020H
LCALL 0200H
```

This is, admittedly, not the easiest legible piece of assembler, as compared to, for instance, lines 52 and 54 in XAMPLE02.LST. Conclusion: the use of meaningful symbolic names (labels) makes programs easier to understand.

The course diskette contains all symbolic notations for the command bytes used. For instance, a monitor routine is available that sends a text string. The use of this routine, ccSTXT (command code send text; value 2) was shown already in part 1. The characters in the string to be transmitted must be available in the program memory. To enable the transmission routine to know where the text ends, the code 0H is used as the end-of-text marker (line 44). The start address of the text must be contained in the DPTR. All this is taken care of in lines 9 and 10, and 52 and 53.

Simple port output operations

Up to now, we have been using the 80C32 board as a kind of black box, without making use of the microcontroller's ports for external control functions. The external circuitry around the 80C32 (or 8051) on the SBC does not allow us to use the ports indiscriminately: remember, ports P0 and P2 are used as address and data bus for the external RAM and EPROM. The eight lines of port P1 are taken to expansion connector pins a20 to a13 via a bidirectional driver IC, of which the direction is controlled by the signal level at pin a21. If this pin is not connected, port P1 can be used as an 8-bit output port. The circuit in Fig. 9 enables four LEDs to be switched on and off, and simple sounds to be sent to a small loudspeaker.

The eight bits that form a byte are numbered from the right to the left starting with 0 (the least significant bit, or LSB) to 7 (the most significant bit, or MSB). Thus, when we refer to P1.3, we mean the fourth bit of port P1. Knowing this, we can switch on LED D3 by programming:

```
MOV P1,#01000000B  ;LED3 on, all
                    other bits 0
```

Line 26 of XAMPLE02 contains such an output command. After a reset, when P1 contains 11111111B (all LEDs on), the LED pattern changes when line 26 is executed.

The principle of port output programming are taken a little further in example program XAMPLE05.A51, which you find on your course disk as well as listed in Fig. 10. This program causes the four LEDs to flash (object code from 4100H onwards), or a 500-Hz tone to sound (object code from 4200H onwards). The signals are generated simply by sending certain bit patterns to port P1, waiting a number of clock cycles, and then sending a new bit pattern. Use is made of TIME, a monitor subroutine that introduces a delay equal to the number of milliseconds loaded into the DPTR.

Assembler language programming is not learned by reading only. To increase your knowledge on the subject, work as much as you can with the examples provided, and make sure you understand what happens if you make changes to them. Set yourself assignments based on what you have acquired so far. For instance, modify XAMPLE05 such that the loudspeaker produces a tone after 2 minutes and 50 seconds exactly. There you have your tea timer, what about a programmable rectangular wave generator as the next project?

❑

Next time: hardware extensions for the 80C32 single board computer.

```
****** LISTING of EASM51 (XAMPLE05) ******
LINE LOC  OBJ          T       SOURCE
   1 0000                ; ****** FILE XAMPLE05.A51 ****************************************
   2 0000                ;
   3 0000                P1      EQU   090H          ; SFR PORT1 address = 090H
   4 0000                ;
   5 0000                        ORG   4100H         ; First program to run from 4100H
   6 4100 75 90 10 [2] START     MOV   P1,#00010000B ; LED D1 on, the others off
   7 4103 90 01 F4 [2]           MOV   DPTR,#500     ; 500 milliseconds
   8 4106 51 12    [2]           ACALL TIME          ; Wait
   9 4108 75 90 E0 [2]           MOV   P1,#11100000B ; LED D2,D3,D4 on, D1 off
  10 410B 90 00 64 [2]           MOV   DPTR,#100     ; 100 milliseconds
  11 410E 51 12    [2]           ACALL TIME          ; Wait
  12 4110 80 EE    [2]           SJMP  START         ; Repeat
  13 4112                ;
  14 4112                       ORG   4200H         ; Second pogram to run from 4200H
  15 4200 75 90 02 [2] START2   MOV   P1,#010B      ; Loudspeaker +5 volt
  16 4203 90 00 01 [2]          MOV   DPTR,#1       ; 1 millisecond
  17 4206 51 12    [2]          ACALL TIME          ; Wait
  18 4208 75 90 00 [2]          MOV   P1,#000B      ; Loudspeaker 0 volt
  19 420B 90 00 01 [2]          MOV   DPTR,#1       ; 1 millisecond
  20 420E 51 12    [2]          ACALL TIME          ; Wait
  21 4210 80 EE    [2]          SJMP  START2        ; and again
  22 4212                ;
  23 4212                ;  MONITOR INTERFACE
  24 4212                ccLTIME EQU  021H   ; MONITOR command, DPTR millisecs delay
  25 4212                COMMAND EQU  030H   ; MONITOR command memory location
  26 4212                MON     EQU  0200H  ; MONITOR entry address
  27 4212                ;
  28 4212 75 30 21 [2] TIME     MOV   COMMAND,#ccLTIME
  29 4215 02 02 00 [2]          LJMP MON
  30 4218                       END
********** SYMBOLTABLE (7 symbols) **********
      P1 :0090     START :4100    START2 :4200   ccLTIME :0021
 COMMAND :0030       MON :0200      TIME :4212
```

Fig. 10. Two programs, one listing: a LED flasher (4100H) and a sound generator (4200H).

SCIENCE & TECHNOLOGY

A SYMMETRICAL ROUTE SWITCH FOR ELECTRONICS

by Michael Soper

THE logic relation 'exactly two of *a,b,c*, are true', or ((*a,b,c,*)), can perform all standard logic functions: for example, *a* = not *b* is ((T,*a,b,*)) where T denotes true.

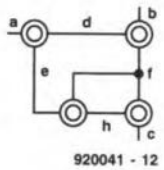
This enables the consideration of a new approach to circuitry also. We can move to see how relational approaches differ from standard ones. Suppose the function '*a* implies *b*' is T = *c* is required to have implementation. We may then use the symbol in

1

Fig. 1to denote ((*a,b,c,*)).

The network in Fig. 2 will perform this task. That is, ((*a,d,e*)), ((*b,d,f*)), ((*e,f,h*)), ((*f,h,c*)), since *a* implies *b* is true, is equivalent to ((— *a*) *v b*) is true, the auxiliary condition *c* = 1 or T, together with our NOT function above gives OR and NOT, from which all functional logic can be created. Each cell is almost equivalent to the XOR function, but, since XOR cannot create all logic alone, our relational system is simpler and more powerful, since it *can*.

2



This logic system can be amended somewhat to provide a practical type of circuit element. The essence of the system consists of a symmetrical element with three wires and the rule that only two of the wires can carry current in either direction at any one time. That is, the circuit appears as a pi circuit in which exactly one of the three impedances has a low value at any one time. 'At any one time' is important. There will be some impedance to the low state, but this impedance can be relatively low. Thus, we have a dynamic new type of circuit element. The rule is that the middle voltage on the three wires is the high-impedance input. We may make the low impedance a partially linear function of high impedance voltage if required.

We may be keen on this approach for various reasons: one of them is symmetry, another is operational simplicity. The manufacture of devices that are both logic and analogue is straightforward. The devices themselves would not be suitable for very high speeds until much development work is done, but this is not often a requirement.

The increased flexibility of use is a great advantage; for example, three-phase oscillators where the high impedance rotates about the device are possible. Many other standard approaches become simpler and with the devices any active circuit function, except the diode and very high speed, can be carried out. In theory, they can also be made to have no supply lines as operational amplifiers do, but the stability of this approach requires analysis. Thus, the distinct possibility exists of a new and useful three-wire device: the Symmetrical Route Switch—SRS.

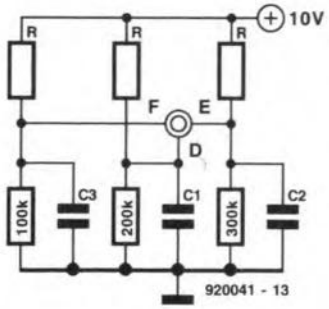
Liberation from directivity

The advantage of these devices is that they can be connected *any way* round at all. Thus, electronic methods can be non-directive in the sense that once a low-impedance link is established between two parts of the circuit, current can flow either way. This totally symmetrical property is new for an active element with three wires (the group of Symmetries is S3).

The ability to rearrange elements in this way is a very considerable advantage. The devices can be used for linear or digital application and are, therefore, apart from speed, more powerful than transistors. The power of the system lies in the fact that only capacitors, resistors, diodes and SRSs are required for circuit implementation (the occasional use of inductance, although rare, is not ruled out).

One more factor is that the device can float at any potential and is, therefore, free from the restrictions that separate power lines to the device impose (this would be difficult to achieve at low voltages, but then SRSs with separate power lines would be used). Thus, the device defines its own relative levels and will not fail, as opamps do, when inputs are at disparate levels from the output.

3



In other words, however complex the interior of the device, its behaviour is still intrinsically simple and the designer's friend.

One symmetrical route switch can serve as the active element in a circuit that oscillates while rotating the high impedance option about the centre of the device—see Fig. 3. In this circuit, on turn-on, D is high impedance so that C_1 is charged first until the voltage at D is greater than that at E, whereupon E becomes the high impedance and C_2 will be charged while the voltage across C_1 drops. If the values are chosen properly, C_3 is the next capacitor to be charged and the voltage on F increases. The cycle then begins again. In that way, a very simple one-device oscillator circuit has been designed.

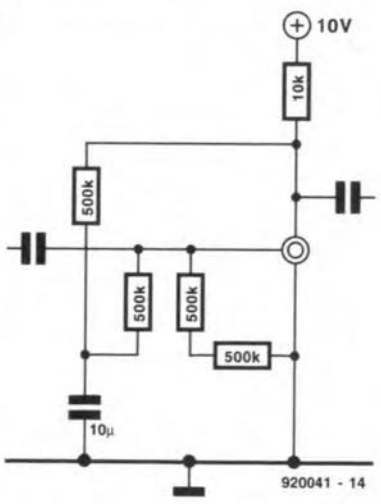
One device and perhaps six resistors and three capacitors is a component count that could be reduced if a slightly different operation is required, say, not such a symmetrical wave. Therefore, although one-transistor, coil-less oscillators can be designed, the circuit in Fig. 3 has a more predictable and usable response and can thus be used as required. That done, other circuits can be completed for similar purposes.

Now, the linear use.

Continuity

In order to use a symmetrical route switch for linear applications, we must bias the middle electrode so that it remains high impedance.

4



The circuit would then appear as shown in Fig. 4. Note that the low impedance is directly proportional to the input voltage and steps must, therefore, be taken to prevent positive feedback. Apart from those requirements, the circuit is standard. The main point to

make here, though, is that this is not the best utilization of a symmetrical route switch, since the sixfold symmetry is not used. But it must be said that linear amplification over the natural range of use of the device can be obtained. Multi-stage amplifiers with or without feedback can be built with the device. We thus already have dual types of operation: logical and linear.

Promotion

The reason that such a system should be promoted is clear: simplification. Although in extreme applications like very fast switching of low-noise amplifiers the SRS is probably best replaced, the neat and interesting possibilities the SRS creates suggest that it should ascend from the status of a theoretical curiosity to that of practical implementation.

One difficulty of the common transistor is that at the end of its standard range of operating conditions there is not always any discontinuous change into another mode, thus indicating a fault.

The system itself can be designed economically. Let U,V,W be the voltages at the three electrodes and I the current in the conducting branch. Then,

$$V + W - 2U = V_1 + |I| \tanh(\alpha V_1)$$
$$U + W - 2V = |I| \tanh(\alpha V_1) - V_1$$
$$U + V - 2W = V_1 - |I| \tanh(\alpha V_1)$$

where $I = \alpha V_1 = \alpha(V-U)$ [for transistor]
or $= \alpha \{(2V-U-W)/2\}$ [for SRS]
α = gain
$\tanh(x) = (e^x - e^{-x})/(e^x + e^{-x})$

These equations are included to give some idea of how a relational law can be defined. With this approach, the SRS can easily be modelled on a computer. The device is non-linear over a wide range with this law, but linear over a small range of signal inputs. Whether or not designers wish to appreciate the flexibility of the SRS depends on how skilful they are and, of course, on the cost of the device. In order to present a unified approach of relational logic and relational amplification in one object, it may be true and it must be admitted that many extreme active circuit functions cannot be performed by this device, but the very great advantage of flexibility coupled with symmetry should not be ignored.

In fact, these devices can be scaled up whenever required and will prove useful at any scale. Design techniques are very different and in a sense relational, not functional. Also, the positive feedback feature makes for more rather than fewer useful circuits.

Another oscillator circuit—a relaxation type—is shown in Fig. 5. This type can have an 'amplifier' positively coupled back to a shunt capacitor over any number of stages, since all stages in the SRS's 'common-emitter-like' configuration have positive feedback.

The chief strength of the SRS is for current routeing, which will be reverted to later.

However, the ease with which either oscillators or amplifiers can be made is encouraging and leads one to speculate on how active electronics would have turned out if active devices had originally had 'in-phase' output and input.

Transformation

A transformation that mirrors the behaviour of the symmetrical route switch with one electrode at high impedance is the following: $v = v_{in}$ (between the common electrode and the high impedance electrode, where v is referred to either the mid-voltage of the output electrodes or the voltage on one of them) and $R = R_{o(ut)}$ is the (variable) resistance of the low-impedance (output) electrode and the common electrode.

$$R = R_o + (1-\alpha v)u/(1+u) + \alpha v$$

where v is again referred to either the mid-voltage of the output electrodes or the voltage on of them, α is the gain and $u = (\alpha v)^{100}$.

The use of a formula like this makes design work easy. The formula is chosen to have an almost perfect ramp before cut-off when the output electrode become high impedance: a change of state. An explicit formula can easily be written into a computer program, after which a simulation can be run and new circuits tried out. The juxtaposition and connection of many such circuits can be simulated. Relational rather than functional thinking can be difficult to get accustomed to, but in the phase shift oscillator of Fig. 6 the ease of operation makes sense. Although this is a good example of the SRS used functionally, this really does not exploit the special properties of the circuit. In Fig. 7, however, our previous oscillator circuit produces a much better example of the use of a symmetrical route switch, since the switch is used symmetrically.

However, symmetrical use does involve a switching operation in the SRS and is thus not suitable for most linear circuits. An exception may be made for some class D or push-pull amplifiers. The distinction between linear and non-linear operation is also usually the distinction between stable use where small inputs produce small outputs and unstable use where a change of state in the device may occur. Class D amplifiers produce quasi-linear operation out of extremely non-linear components. The ramp function of our SRS combines both modes of operation—but may the effective slope of the amplification be changed? The best linear use of any symmetrical route switch is with a constant current tail of, say, current i, when

$$V_{out} = iR = iR_o + i\alpha V_{in}$$

under these conditions of linear use—see Fig. 8. Connecting a feedback impedance R_1 with feedback factor $1/n$, we find

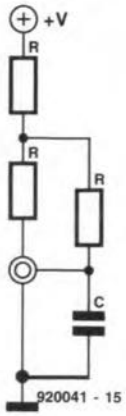
$$dv = V_{out}/n$$

so that

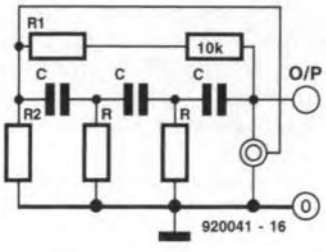
$$V_{out} = i\{R_o + \alpha(V_{in} + V_{out}/n).$$

In other words, the output resistance and the effective transconductance are increased; the gain of the stage increases also and is usefully a function of i, the quiescent current. The factor $1/n$ depends linearly on R_1 so that we may replace R_1 by another suitable SRS to obtain a stage with negative gain. Thus, when more than one SRS is used—see Fig. 9—we have the capability of building an inverting stage: with constant current

5



6



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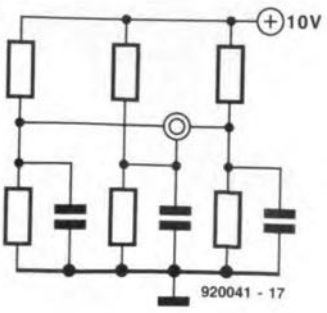

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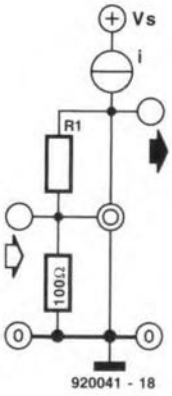

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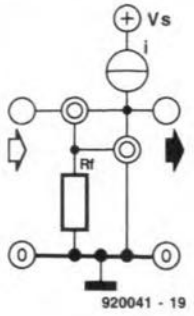


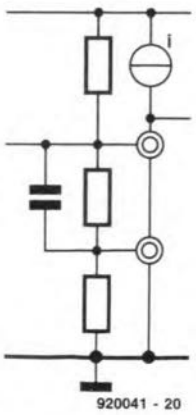
supplies, the linearity can be very good.

Buffer stages

The symmetrical route switch is naturally suitable as a buffer stage when it is used linearly—but, of course, this is not the best use, because the flexibility of the device is ignored. For good linearity, a constant-current stage can be used: the linearity of the SRSs is a direct function of the quality of the constant current supply. This fact and the symmetry of the high-impedance input connection means that stages can be paralleled for lower impedance or be put in series with no great problems as long as the input electrode sits at the correct point with respect to the output electrodes. Even this feature is simpler on the SRS, because, as long as the voltage on the input electrode lies between the voltage of the output electrodes, the behaviour will be linear at all times (given that the voltage is 'one side' of midway).

To reduce the output impedance of a transistor stage to low values, an emitter-follower is used: a circuit with negative feedback which similarly has non-linearity. The use of negative feedback is possible for the SRS when the input voltage is nearer the more negative 'through' electrode, because the gain is then negative and a simple impedance is enough. A diagram of the series connection is given in Fig. 10.

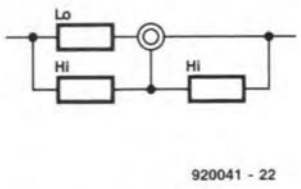
10



For the reason just given, a 'switching' symmetrical route switch can make an ideal method for shunting out large currents. A suitable circuit is shown in Fig. 11. Assume the left-hand side of this to be temporarily positive: as the current increases, the voltage across the low resistance increases also until the knee voltage of diode D is reached.

Since the circuit is symmetrical under some conditions, the same approach will work for alternating current also: a simple design for use with this case when the component values are correctly chosen is shown in Fig. 12.

11



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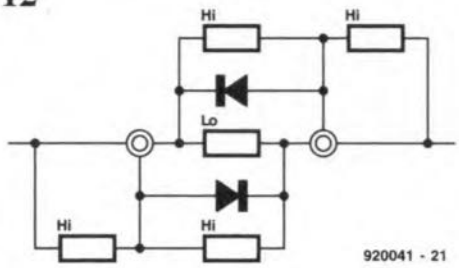
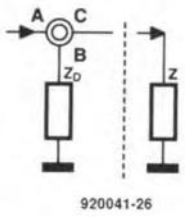


Routes

The name symmetrical route switch suggests also that they can be used for signal routeing: a task they are ideally suited for. Consider the simple arrangement in Fig. 13.

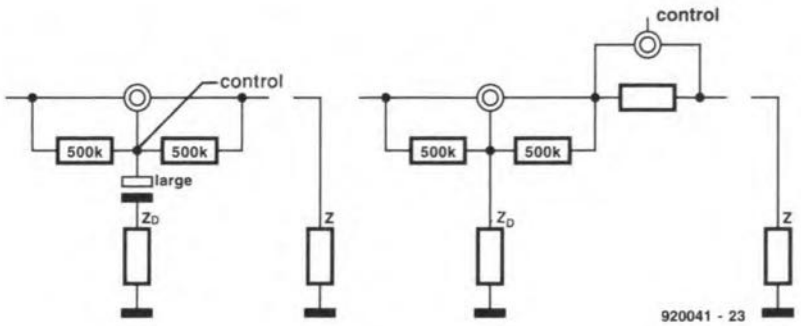
13



While electrode B has a voltage between that of A and C, the signal will actuate load Z. But when the voltage on electrode B is above that on A and C, the signal is dissipated in matched load Z_d. The advantage is almost perfect matching. Practical circuits for AC and DC are given in Fig. 14.

Designing a bistable from symmetrical route switches in conventional ways is possible but clumsy; a bistable based on an SRS on-impedance of 10 Ω is shown in Fig. 15. With 4.5 passive components per active device, this circuit is not very practical. The circuit in Fig. 16, however, is, mainly because it has greater natural stability.

14



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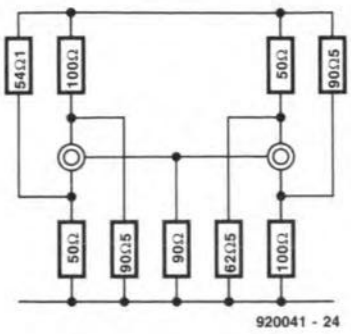
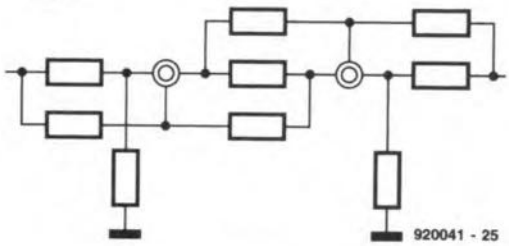


The symmetrical route switch combines a non-linear function, as required for switching and for load and power supply protection, with at least two kinds of linear function: transistor-like and symmetrical input function referred to midpoint, when required. Thus, two distinct circuit operations are combined in one circuit. Look inside many hi-fi amplifiers and you will see that until recently small relays were used for protection on overload. The symmetrical route switch combines this function also, because, although it is a three-terminal device, the control connection (at very high impedance with respect to the others) controls the output impedance. Hence, one device can perform all logic, linear action and protective switching.

16



The route ahead

Integration of circuits has led to a large pin-out count on many integrated circuits, followed by a partial reduction. Some useful ICs are three-terminal devices, usually unsymmetrical and polarized, although a few are symmetrical. The symmetrical route switch is the first three-terminal device capable of logic and linear action, which can be inserted *any way* into a circuit. The power it takes is absorbed from the current through the output impedance. ■

INDUCTANCE-CAPACITANCE METER

FRONT COVER PROJECT

based on a design by H. Kühne

When the value of a capacitor or inductor is measured, it is imperative that ohmic losses do not affect the result. The principle of measurement used in the meter presented here ensures that the influence of ohmic losses is reduced to nil.

BASICALLY, there are two problems in measuring inductance or capacitance: ohmic losses and frequency-dependence of the component. The effect of ohmic losses has been nullified in this design, while the frequency-dependence is, as usual, negated by choosing a measurement frequency that lies in the range in which the component is to operate. In the present design, the frequency lies in the audio range.

The principle of the design is shown in Fig. 1. The value of an inductance, L_x, is determined by passing a sinusoidal current of constant amplitude through the inductor and measuring the resulting voltage across it. The value of a capacitance, C_x, is determined by applying a constant-amplitude sinusoidal voltage across the capacitor and assessing the resulting current through it by measuring the voltage drop across R_C. In either case, that voltage (measured at A) is directly proportional to the inductance or capacitance plus the loss resistance. How that resistance is removed from the measurand (measured quantity) will be discussed later.

We will now consider how the current through the inductance, or the voltage across the capacitance, is held constant. The inverting input of the differential amplifier at the input of the circuit is fed with a sinusoidal measurement signal, U_E, and the non-inverting input with part of the voltage at G, U_A. Since the gain of the amplifier is unity, the voltage at B is U_A–U_E. The potential difference between A and B is U_A–(U_A–U_E), which is U_E. Assuming that U_E is a constant-amplitude sinusoidal voltage, depending on the setting of switch S_2, a constant voltage exists across R_L or C_x. This causes a constant current through R_L and thus through L_x. Since a constant current flows through the inductance, or a constant voltage exists across the capacitance, the loss resistances, R_L and R_C, have no effect on the measurement.

The signal at G consists of two components: a sinusoidal voltage that is *in phase* with U_E and a sinusoidal voltage that is 90° *out of phase* with U_E (cos U_E). Added together, the components form a sinusoidal voltage that is x° out of phase with U_E. The components are separated by synchronous rectification of the signal. The rectifier is driven by a square wave (F) that is shifted 90° with respect to sinU_E. That means that only the cosine component in the signal is rectified: the resulting mean value is directly proportional to the inductance or capacitance, whereas rectification of the sine component yields a mean value of zero.

TECHNICAL DATA

Measurement frequency	1 kHz
Measurement ranges:	
inductance	2, 20, 200 mH, 2 H
capacitance	2, 20, 200 nF, 2 µF
Accuracy (calibrated with 1% capacitor)	
with moving-coil meter	±(1.5% of reading + 2% of FSD)
with 3.5 digit digital voltmeter	±(1.5% of reading + 1 digit)

The various signals encountered in this process are shown in Fig. 2. Figure 2a shows the situation when a perfect inductance or capacitance is being measured. Since ideal components are considered, both the measured signal, U_A, and the square-wave voltage, U_F, driving the rectifier are 90° out of phase with U_E. This means that the rectifier will switch exactly at the zero crossings of the measured signal, which results in a voltage whose mean value is directly proportional to the measured reactance.

If a resistance is substituted for the inductance or capacitance—Fig. 2b—the measured signal will be in phase with U_E. The rectifier then switches exactly at the peaks of the signal, resulting in a mean voltage whose value is zero.

Although practical inductors and capacitors have parasitic or stray resistance, the effect of this is nullified in the synchronous rectification. When a practical inductor or capacitor is measured, the phase shift between the measuring signal, U_E, and the measured signal, U_A, will be somewhere between 0° and 90°. This means that the signal is neither wholly rectified nor reduced to zero: the resulting mean value will be representa-

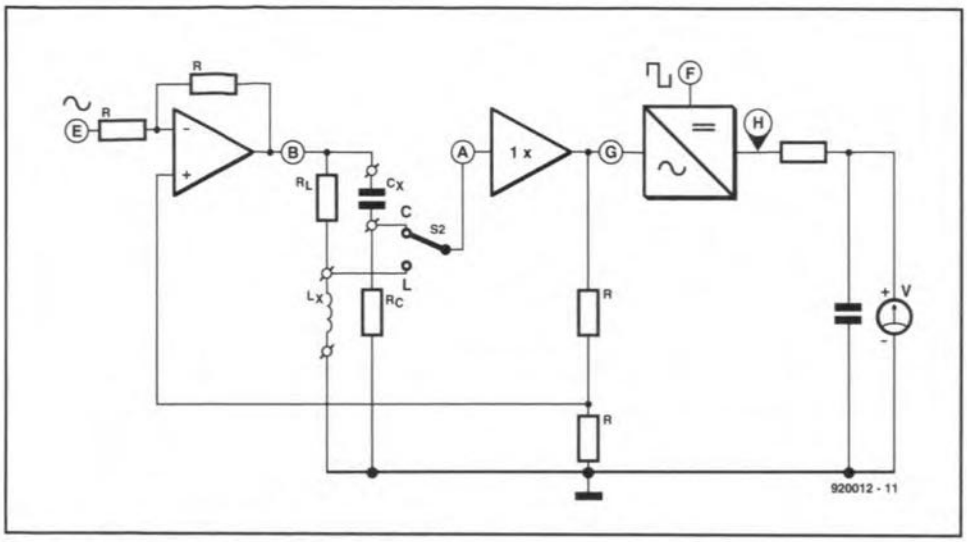


Fig. 1. Principle of the design of the meter.

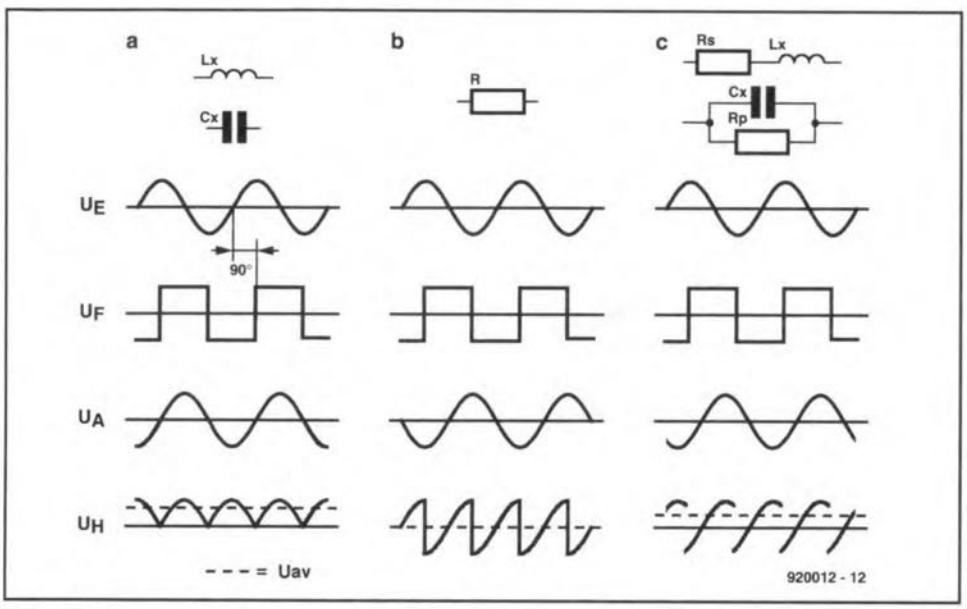


Fig. 2. Waveforms associated with the measurement process.

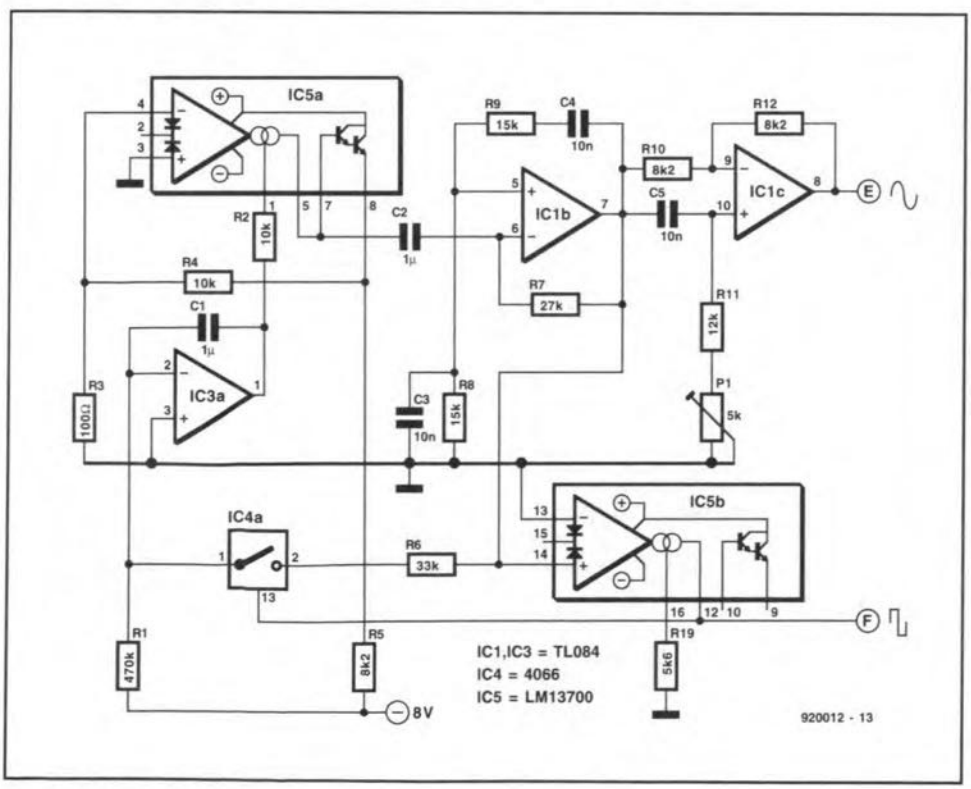


Fig. 3. The oscillator circuit.

tive of the real inductance or capacitance.

Returning to Fig. 1 for a moment, the rectifier is followed by an *RC* network which averages the rectified voltage before that is applied to a meter.

Oscillator

The measurement signal, U_E, and the square wave voltage, U_F, that drives the rectifier are generated by a Wien-bridge oscillator, IC_{1b}—see Fig. 3. The sinusoidal output of this stage is converted into a square-wave voltage by IC_{5b}, an operational transconductance amplifier (OTA) connected as comparator. Since the square-wave and sinusoidal signals are in phase, the latter is applied to phase shifter IC_{1c}. The required 90° phase difference between the two signals is set with P_1.

The remainder of the circuit in Fig. 3 serves to stabilize the level of the oscillator output. To that end, the output, pin 5, of IC_{5a} is used as a preset resistance in the feedback loop of IC_{1b}. That resistance is determined by the current entering via the control input, pin 1. This current, provided by integrator IC_{3a}, can be used to influence the gain of IC_{1b} and thus the amplitude of the sinusoidal signal. Its level is in turn determined by the amplitude of the positive halves of the sinusoidal signal. The negative halves are not passed by switch IC_{4a} since that is closed by IC_{5b} only during the positive halves of the signal.

Regulation is arranged so that the gain of IC_{1b} diminishes when the amplitude increases. and vice versa. Ultimately, the amplitude stabilizes around a value of 1.2 V.

Measuring circuit

Basically, of course, the measuring circuit in Fig. 4 is similar to Fig. 1 with the rectifier and meter omitted.

The differential input amplifier consists of IC_{1d}. Its output current is doubled in IC_{1a}, since the peak level should be about 15 mA, which a single TL084 cannot provide. The design ensures that the level of the voltage across R_{17} is identical to that across R_{16}. Consequently, the currents through these resistors are also identical. Observe that one half of the current fed to the measuring circuit is provided by IC_{1d} and the other half by IC_{1a}.

Range switch S_1 is provided with a section, S_{1c}, that enables the decimal points of a digital meter module, if used, to be controlled. In case of an LCD module, the pole of S_{1c} must be fed with the back-plane (BP) signal or, if an LED display is used, with a logic high or low, depending on the type of the display.

The various ranges are determined with the aid of 0.1% resistors. This has two advantages: calibration of only one range suffices and the tolerance of the resistors has a negligible effect on the total accuracy of the meter (if the tolerance were 1%, the meter accuracy would deteriorate by at least 1%). Note that the 1% resistors in parallel with R_{43}, R_{47}, and R_{48}, can be ignored since their tolerance is tiny compared with that of the parallel-connected low-value resistors.

Rectifier and power supply

The remainder of the circuit, that is, rectifier, meter, power supply and overflow indicator, is shown in Fig. 5.

The rectifier proper, IC_{2d}, is preceded by an amplifier, IC_{2c}, because the output of the metering circuit at full-scale deflection (FSD) is only 150 mV (assuming a perfect inductance or capacitance) and that is not enough to ensure a mean voltage of 2 V to the meter. The rectifier elements are not diodes, but two electronic switches, IC_{4b} and IC_{4d}, that are operated by the square-wave signal in step with the sinusoidal output of the oscillator. An inverter based on IC_{4c} controls IC_{4d}, so that IC_{4b} and IC_{4d} are alternately opened and closed. When IC_{4b} is closed, IC_{2d} amplifies ×1; when IC_{4d} is closed, IC_{2d} amplifies ×–1. This ensures operation in step with the square-wave signal.

The output of the rectifier is smoothed by network R_{27}-C_7. Because this network can be loaded only lightly, the potential across C_7 is buffered by IC_{2a} before the signal is applied to the meter. The meter may be a digital or an analogue type. The digital type may be connected directly to buffer IC_{2a}. Series resistors and protection diodes for a moving coil meter are provided.

At first glance, an overflow indicator may seem superfluous, since the meter, M_1 or DM_1, shows immediately if the meter range is exceeded. That is true enough, but consider that if the meter range is grossly exceeded, IC_{2c} will clip and the resulting mean value of the rectified voltage may then fall *under* 2 V, that is, *in* the meter range. The meter reading then means nothing and this would not be evident without the overflow indicator.

The indicator is based on IC_{3b} (connected as comparator) and IC_{3c}. The output of the rectifier is compared by IC_{3b} with a voltage set with P_5 to a level of 4 V. If the rectified output exceeds the set level, buffer capacitor C_8 is charged via D_3. This results quickly to the output of IC_{3c} changing state and D_4 lighting.

Construction and calibration

There should be no particular difficulties in the construction of the instrument if the PCB shown in Fig. 6 is used. As usual, start with the lowest-lying components, that is, the wire links. When the highest protruding components, that is, electrolytic capacitors, IC_6 and IC_7 and the mains transformer, have been fitted, wire up those components that are not fitted on the board.

The low-tolerance resistors should be soldered direct to the range switch, S_1. It is, therefore, advisable to use a type of switch that has solder eyelets and not

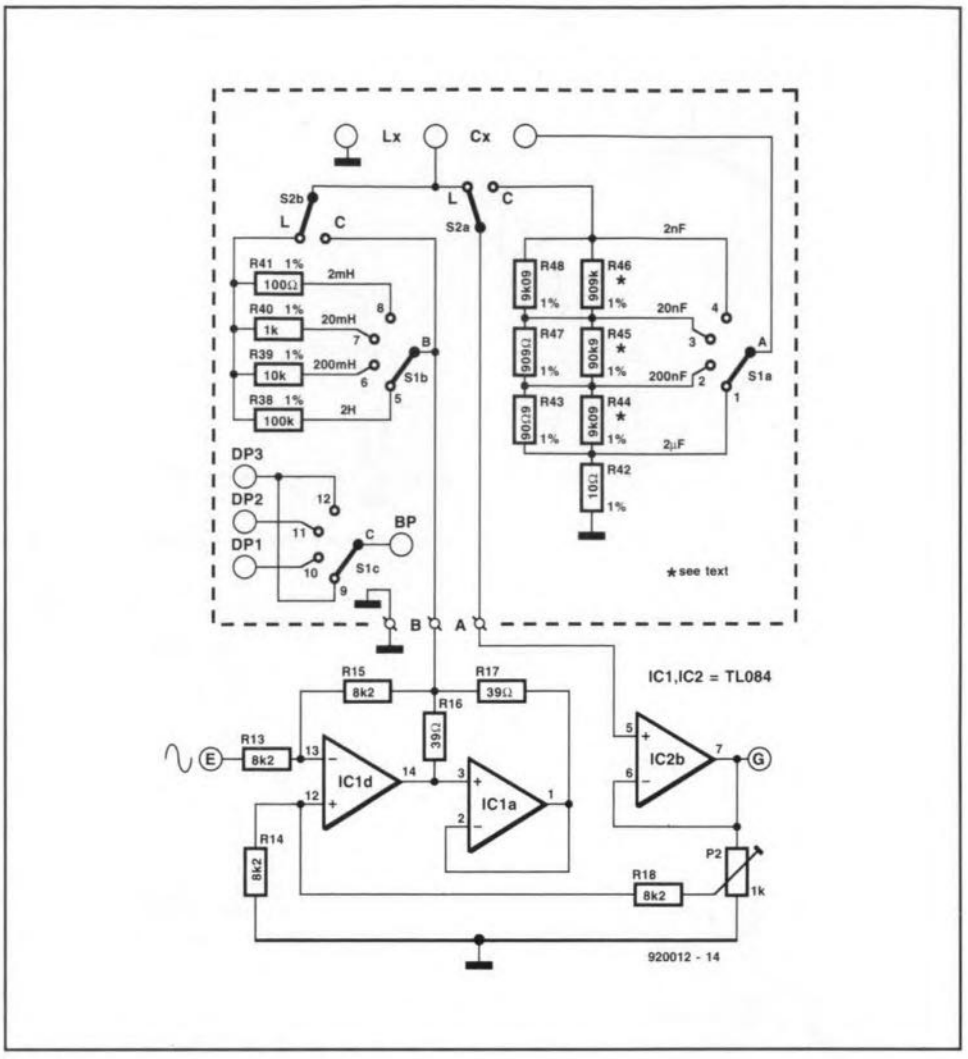


Fig. 4. The metering circuit proper.

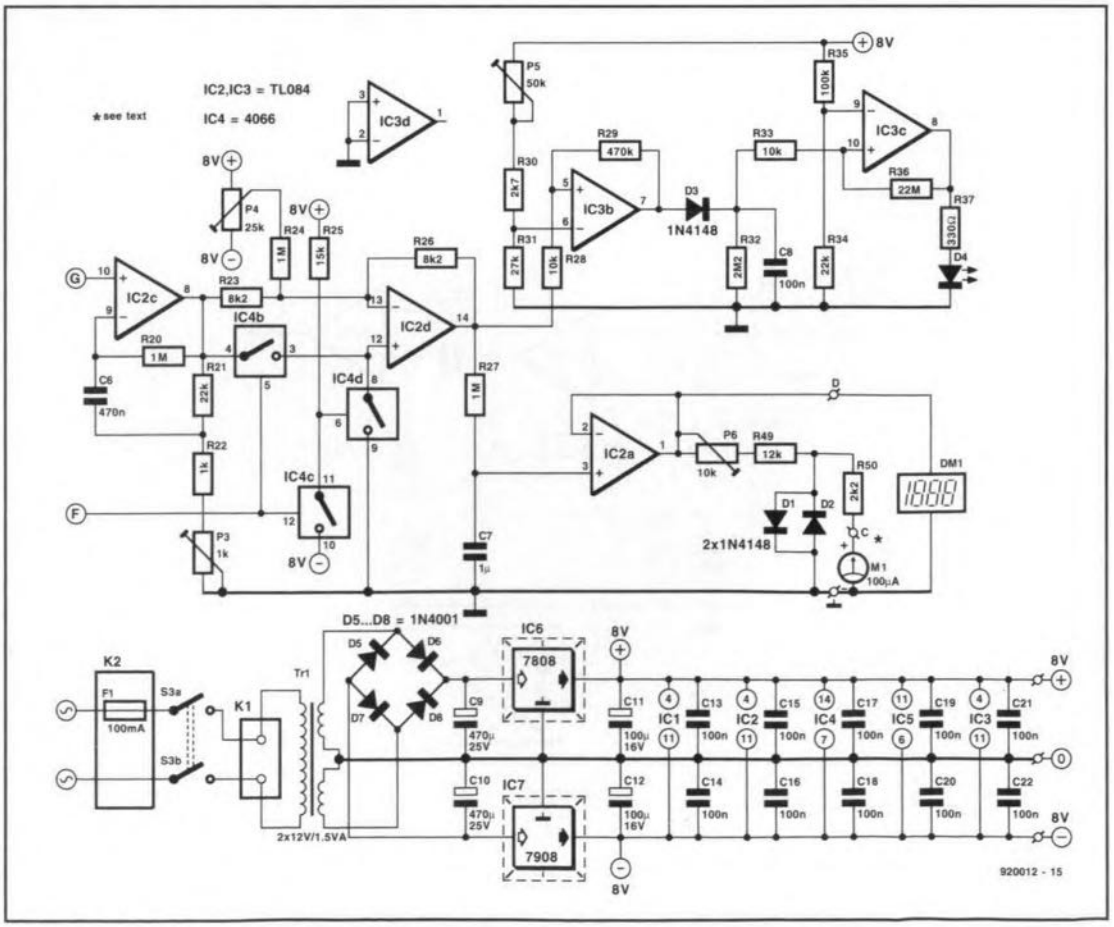


Fig. 5. Circuit of the rectifier, power supply, meter and overflow indicator.

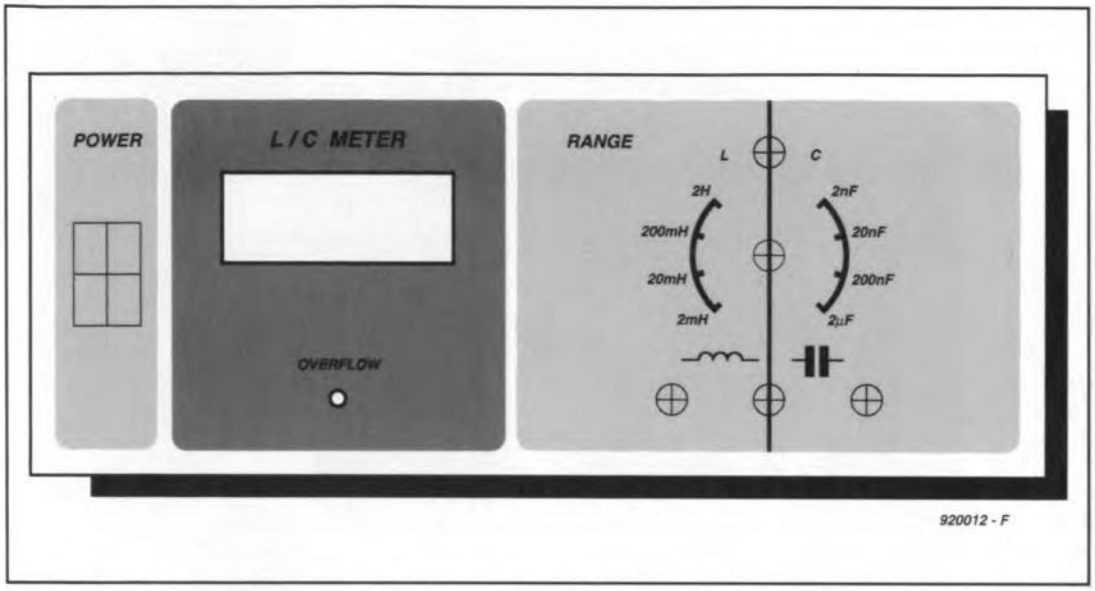


Fig. 6. Proposed front panel layout (foil Type 920012–F).

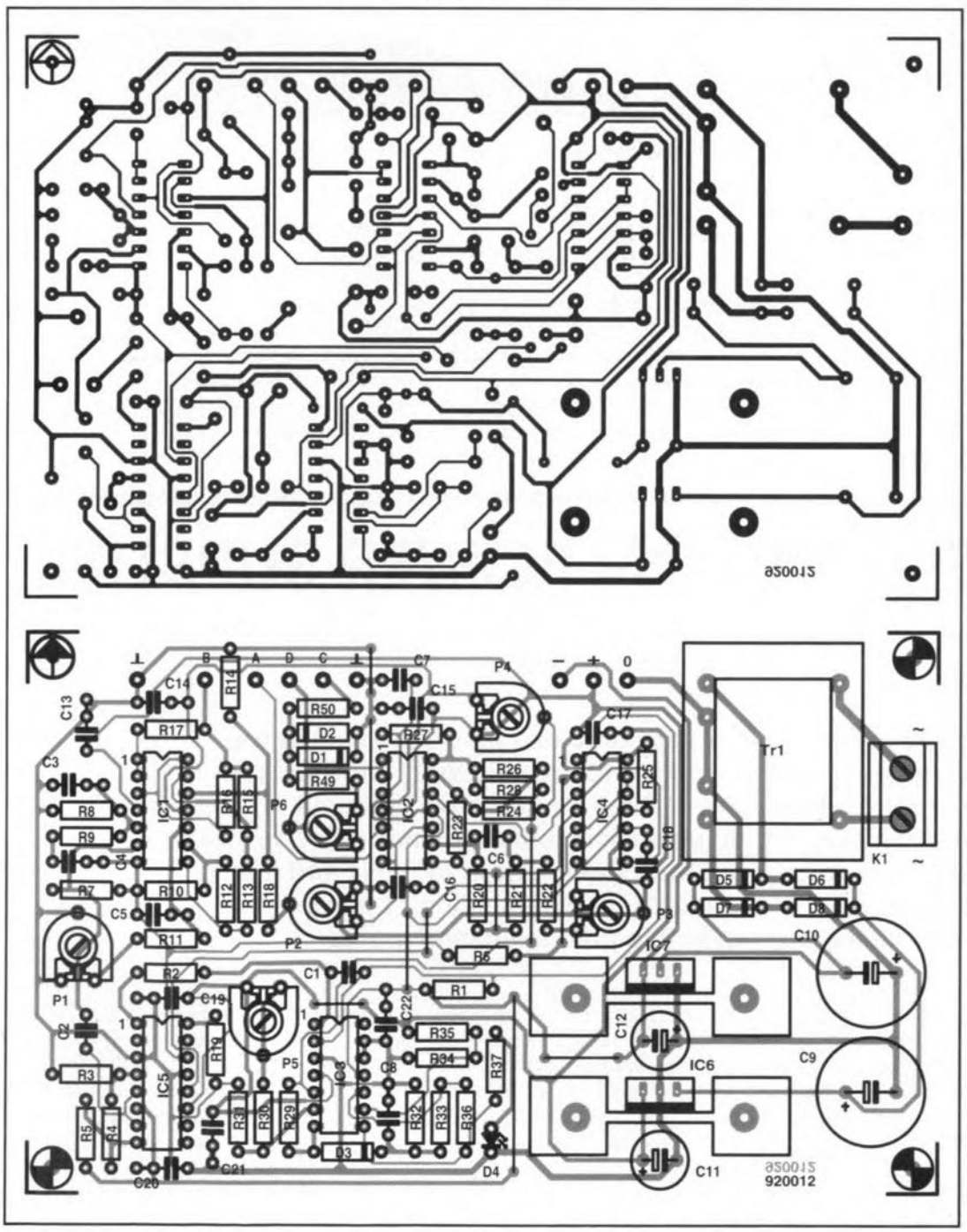


Fig. 7. Printed-circuit board for the inductance-capacitance meter – Type 920012.

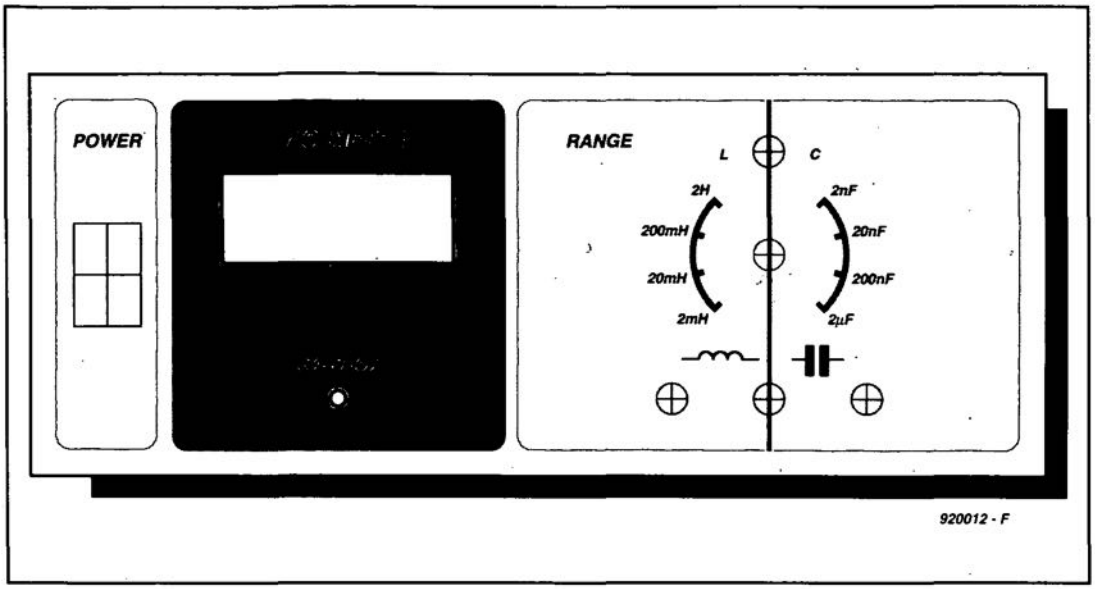
PARTS LIST

Resistors:
R1, R29 = 470 kΩ
R2, R4, R28, R33 = 10 kΩ
R3 = 100 Ω
R5, R10, R12–R15, R18, R23, R26 = 8.2 kΩ
R6 = 33 kΩ
R7, R31 = 27 kΩ
R8, R9 = 15 kΩ
R11 = 12 kΩ
R16, R17 = 30 Ω
R19 = 5.6 kΩ
R20, R24, R27 = 1 MΩ
R21, R34 = 22 kΩ
R22 = 1 kΩ
R25 = 15 kΩ
R30 = 2.7 kΩ
R32 = 2.2 MΩ
R35 = 100 kΩ
R36 = 22 MΩ
R37 = 330 Ω
R38 = 100 kΩ, 0.1%
R39 = 10 kΩ, 0.1%
R40 = 1 kΩ, 0.1%
R41 = 100 Ω, 0.1%
R42 = 10 Ω, 0.1%
R43 = 90.9 Ω, 0.1%
R44 = 9.09 kΩ, 1%
R45 = 90.9 kΩ, 1%
R46 = 909 kΩ, 1%
R47 = 909 Ω, 0.1%
R48 = 9.09 kΩ, 0.1%
R49 = 12 kΩ
R50 = 2.2 kΩ
P1 = 4.7 kΩ preset
P2, P3 = 1 kΩ preset
P4 = 25 kΩ preset
P5 = 47 kΩ preset
P6 = 10 kΩ preset

Capacitors:
C1, C2, C7 = 1 µF
C3–C5 = 10 nF
C6 = 470 nF
C8, C13–C20 = 100 nF
C9, C10 = 470 µF, 25 V, radial
C11, C12 = 100 µF, 16 V, radial
1×180 nF, 1%) for calibrating
2×100 nF, 1%) meters

Semiconductors:
D1–D3 = 1N4148
D4 = 5 mm LED, yellow
D5–D8 = 1N4001
IC1–IC3 = TL084
IC4 = 4066
IC5 = LM13700
IC6 = 7808
IC7 = 7908

Miscellaneous:
K1 = 2-way terminal block for PCB mounting, 7.5 mm pitch
K2 = mains panel plug with integral fuse holder and fuse, 100 mA delayed action
K3–K5 = banana socket
S1 = 3-pole, 4-position rotary switch with solder eyelets
S2 = 2-pole change-over switch
S3 = double-pole, double-throw switch with integral lamp
Tr1 = mains transformer, 2×12 V, 1.5 VA
M1 = 100 µA moving-coil meter
DM1 = 3.5 digit digital voltmeter, 2 V
Heat sinks for IC6 and IC7
PCB 920012
Front panel foil 920012-F



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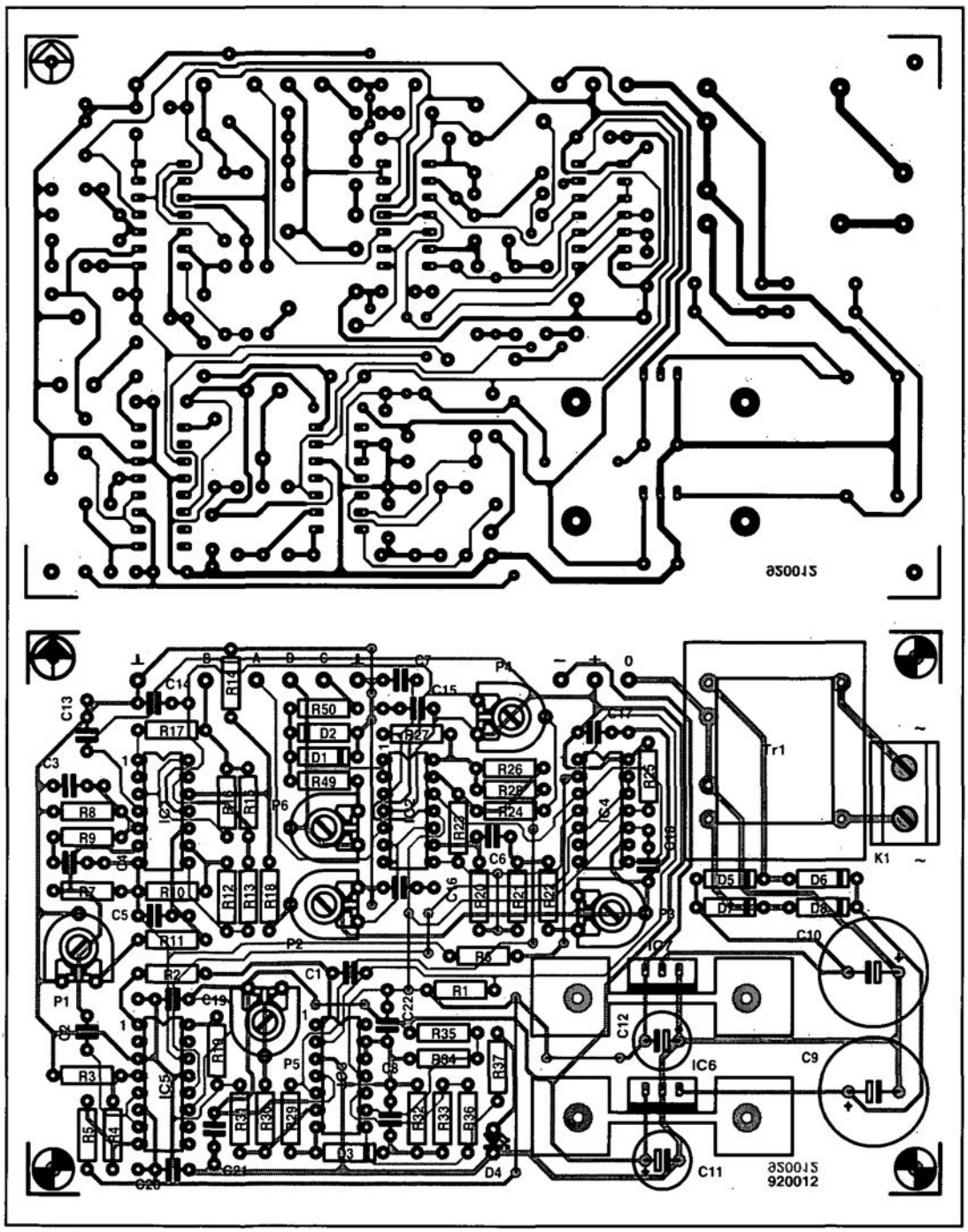

Fig. 7. Printed-circuit board for the inductance-capacitance meter – Type 920012.

PARTS LIST

Resistors:
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R3 = 100 Ω
R5, R10, R12–R15, R18, R23, R26 = 8.2 kΩ
R6 = 33 kΩ
R7, R31 = 27 kΩ
R8, R9 = 15 kΩ
R11 = 12 kΩ
R16, R17 = 30 Ω
R19 = 5.6 kΩ
R20, R24, R27 = 1 MΩ
R21, R34 = 22 kΩ
R22 = 1 kΩ
R25 = 15 kΩ
R30 = 2.7 kΩ
R32 = 2.2 MΩ
R35 = 100 kΩ
R36 = 22 MΩ
R37 = 330 Ω
R38 = 100 kΩ, 0.1%
R39 = 10 kΩ, 0.1%
R40 = 1 kΩ, 0.1%
R41 = 100 Ω, 0.1%
R42 = 10 Ω, 0.1%
R43 = 90.9 Ω, 0.1%
R44 = 9.09 kΩ, 1%
R45 = 90.9 kΩ, 1%
R46 = 909 kΩ, 1%
R47 = 909 Ω, 0.1%
R48 = 9.09 kΩ, 0.1%
R49 = 12 kΩ
R50 = 2.2 kΩ
P1 = 4.7 kΩ preset
P2, P3 = 1 kΩ preset
P4 = 25 kΩ preset
P5 = 47 kΩ preset
P6 = 10 kΩ preset

Capacitors:
C1, C2, C7 = 1 µF
C3–C5 = 10 nF
C6 = 470 nF
C8, C13–C20 = 100 nF
C9, C10 = 470 µF, 25 V, radial
C11, C12 = 100 µF, 16 V, radial
1×180 nF, 1%) for calibrating
2×100 nF, 1%) meters

Semiconductors:
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M1 = 100 µA moving-coil meter
DM1 = 3.5 digit digital voltmeter, 2 V
Heat sinks for IC6 and IC7
PCB 920012
Front panel foil 920012-F

one for PCB mounting. It may be possible to bend these eyelets slightly outwards to give more space for the resistors.

If a digital meter module is used, do not forget to wire switch section S_{1c}, which controls the decimal points.

In spite of there being six preset potentiometers, the calibration of the instrument is fairly straightforward. Start with setting all the presets to the centre of their travel.

If a moving coil meter is used, connect a voltmeter between D and earth. With the instrument switched off, zero the moving-coil meter manually. When a digital meter is fitted, an external voltmeter is not required.

Set S_2 to position C(apacitor) and leave the input terminals open. Adjust P_4 till the voltmeter (or internal digital meter) reads 0. This arranges the offset compensation.

Connect two 100 nF in parallel to the input terminals and set the range switch to 200 nF. The value of these capacitors need not be accurate, since this test only serves to set the gain of IC_{2c}. This is done by adjusting P_3 until the voltage at D is 2 V. Because of R_{27} and C_7 ($\tau = 1$ s), this voltage rises only slowly; P_3 should, therefore, be adjusted slowly also. When P_3 has been adjusted as required,connect a resistor of 10 kΩ in parallel with the 100 nF capacitors. Then adjust P_1 to return the voltage at D to 2 V. This arranges the phase difference between sinusoidal and square-wave signals at 90°.

Next, remove the 10 kΩ resistor, but not the capacitors, from the input terminals. Ideally, P_2 should be set with its wiper at the output of IC_{2b}. This would, however, create a positive feedback loop with a gain of ×1: not exactly conditions for oscillation, but very nearly so. It is, therefore, necessary to connect an oscilloscope to the output of IC_{2b} and adjust P_2 so that oscillation just does not set in. If an oscilloscope is not available, set P_2 to about ¾ of its travel, that is, 750 Ω between wiper and earth.

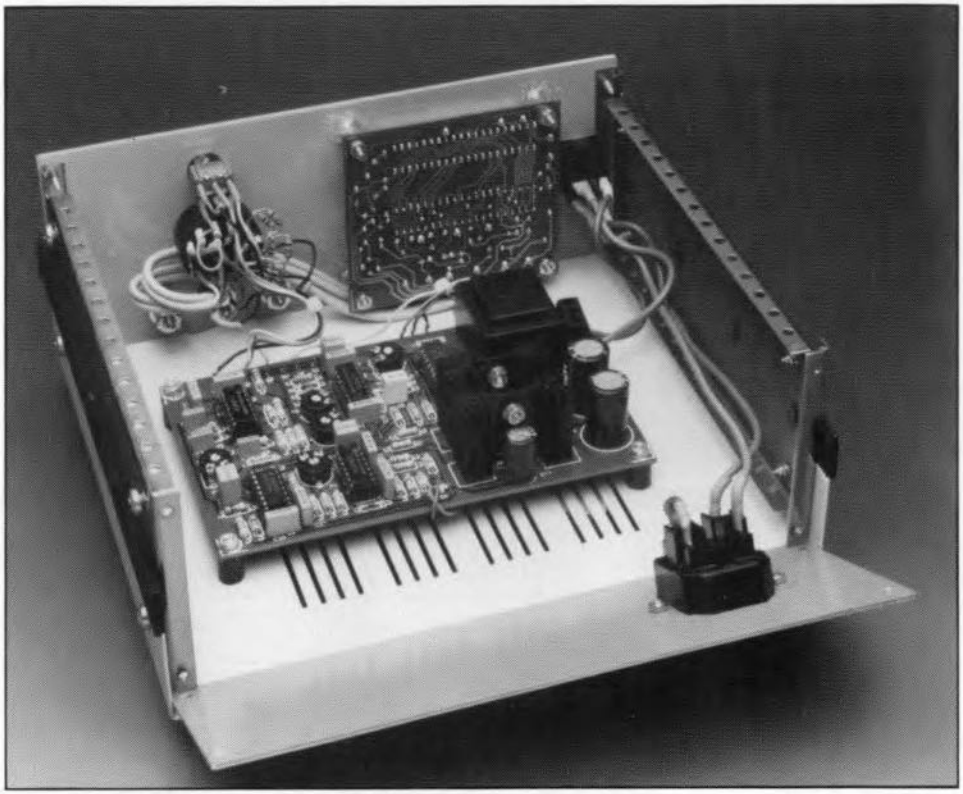


Fig. 8. Inside view of meter with top panel removed and rear panel hinged down.

If, apart from an oscilloscope, a function generator that provides a triangular output is available, P_2 can be adjusted even more accurately. To that end, R_{13} must be unsoldered from IC_{1c} and a 3-V, 1 kHz triangular signal applied across it. An oscilloscope connected to the output of IC_{2b} will then show a square wave-form (because of the integrating action of the capacitors at the input). Adjust P_2 so that this wave-form is 'clean', that is, shows no overshoot.

Connect two 100 nF, 1%, capacitors (if a moving coil meter is used) or an 180 nF, 1%, capacitor (if a digital display is used) to the input terminals and adjust P_6 (moving-coil meter) or P_3 (digital display) until the correct value is read. ■

Mains (power line) voltages are not listed in the articles. It is assumed that our readers know what voltage is standard in their part of the world.

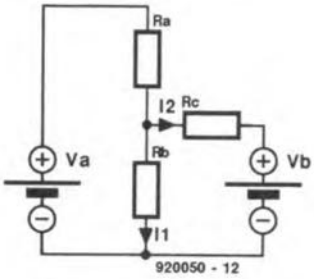
Readers in countries that use 60 Hz supplies, should note that our circuits are usually designed for 50 Hz. This will not normally cause problems, although if the mains frequency is used for synchronization, some modification may be required.

The international letter symbol '*U*' is used for voltage instead of the ambiguous '*V*'. The letter V is reserved for 'volts'.

CORRECTIONS

Plant warmer (June 1992)

Resistor R_c was omitted from Fig. 2. The correct diagram is shown below.



Inductance-capacitance meter (March 1992)

The value of R_{16} and R_{17} should be 39 Ω, not 30 Ω as shown in the parts list.

8751 Emulator (March 1992)

The features list in the first column on page 53 should read:

- download, modify, and upload 8751 programs without having to erase and program an 8751.
- put breakpoints in programs.
- display register and memory contents.
- ...

  etc.

FM tuner – Part 3 (May 1992)

In the PSU parts list on page 54, R_{301} should be 150 Ω, 1%, not 150 kΩ, 1%.

Video enhancer (July 1992)

Preset P_2 is best adjusted for a signal level of 2 V_{pp} at the collector of T_2. Output transistor T_3 may run fairly hot: this is normal.

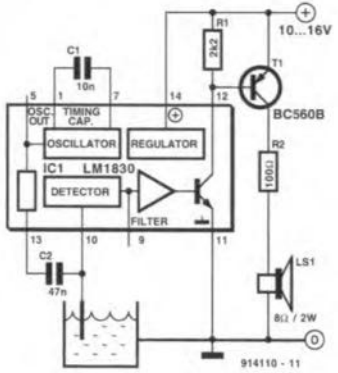
The third paragraph of the text on page 73 should read: The frequency characteristic of the signal at the base of T_3 is shaped by P_1, R_6 and C_8, and is, therefore, to a certain extent under the control of the user (with P_1).

Mark 2 QTC 80/40 loop antenna (July 1992)

The frequency '3800 kHz' mentioned twice under **2. 40-metre band** (page 90) should have read '7300 kHz'.

Audible fluid level indicator (July 1992)

Owing to a printing error, the diagram in this article is incorrect. The right diagram is shown below.



CORRECTIONS

4-Megabyte printer buffer

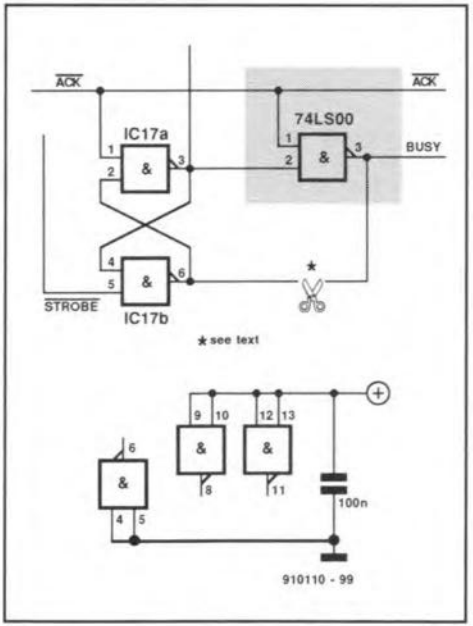
June 1992

Two points regarding this project.

(1) The input of the buffer is designed to be Centronics compatible. Problems may occur when this standard is not respected by the computer or the software. A number of 'fast' PCs (in particular 386 and 486 based machines) appear to have printer interfaces derived from the Epson standard. These interfaces in general do not wait for the ACKNOWLEDGE signal, but instead process the BUSY signal.

Handshaking problems that may occur between these PCs and the printer buffer may be solved by combining the BUSY and ACKNOWLEDGE signals as shown in the diagram opposite. The result of the modification is that the printer buffer behaves like an Epson-compatible peripheral device.

(2) An updated version of the control software (in EPROM) is available that enables 1-Megabyte (1M × 8 and 1M × 9) SIP/SIM modules with three ICs to be used in the printer buffer.



Inductance-capacitance meter

March 1992

Terminals 'A' and 'B' should be transposed in the circuit diagram of the meter circuit proper (Fig. 4 on page 32).

Milli-ohm measurement adaptor

April 1992

To prevent its contacts burning out, switch S_1 must not be operated when an inductive component is connected to the adaptor.

Contrary to what is said under the heading 'Extensions', the reference inputs of the DVM are connected to the pole of S_{1b} and ground, while the 'normal' DVM inputs are connected to the resistor to be measured.

MEASUREMENTS ON POWER SUPPLIES

g10148

by our technical staff

How do you know whether your precious laboratory/workshop power supply unit is still working to specification? How do you measure the parameters of the PSU you have just built or purchased for fitting into an electronic apparatus and what do you specifically have to look out for? The answers to these and many other questions connected with the testing of power supplies are given in this practice-based article.

THE requirements of a laboratory/workshop power supply unit are exacting. Not only the output voltage and current, but also the dynamic and static internal resistance, noise, overshoot and thermal stability, to name but a few, are important. *Any electronic apparatus is only as good as its power supply* is an adage that remains true.

The extent to which a power supply can be tested depends primarily on the available test equipment. Normally, the output voltage can be measured with a simple multimeter.

But even this measurement may be more complicated than appears at first sight. Imagine, for instance, that you have obtained a 6 V mains adapter to replace the batteries in a normally battery-operated apparatus, which is not only less expensive in the long run, but also more sensible from an ecological viewpoint. To your surprise, when you measure the output voltage, it is 9–11 V. The first question that pops into your mind is: "Is it safe to connect to the equipment?" Practical considerations show that there is no harm in that whatsoever. The explanation for this statement is that such a simple mains adapter usually consists of a small transformer, rectifier and reservoir capacitor, nothing more. For all sorts of reason, small transformers generally have a fairly high internal resistance—

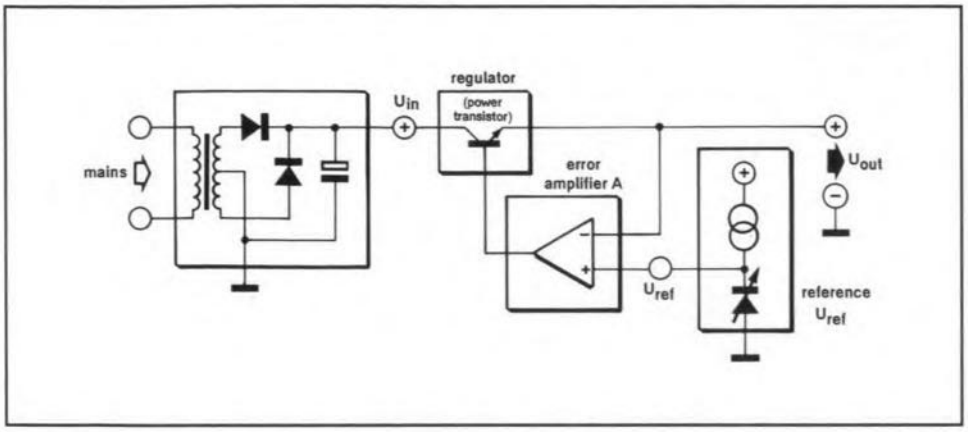


Fig. 1. Basic circuit of a regulated power supply. The quality of the supply is determined primarily by the regulator section.

of the order of a few ohms—and this makes the output voltage highly dependent on the output current. In other words, the e.m.f. is appreciably higher than the nominal (on-load) output voltage: if the load is small, the output voltage is high.That is why the load voltage is normally specified at a certain output current.

It is, therefore, essential to know how a parameter, even one as simple as the output voltage, is measured.

Parameters

In contrast to a simple mains adapter, a regulated power supply is designed to nullify the effect of different loads on the output voltage. In general, the more complex the design, the more the supply will approach the ideal. A perfect power supply has, irrespective of its application, some basic properties: it shall in all circumstances provide a constant output voltage, on which there is no ripple, noise or other spurious signals.

The following list shows which properties determine the quality of the supply.

Load voltage: the voltage that the supply will provide to a load over the nominal range of output currents.

Electro-motive force: the output voltage under no-load conditions; ideally, the e.m.f. and the load voltage should be identical.

Nominal output current: the current that the supply can deliver to the load without becoming overloaded.

Internal resistance: ideally, this should be 0 Ω, but all values in mΩ are good. It is sub-divided into:

Static internal resistance: this is discernible when the input voltage and the load remain constant with time.

Dynamic internal resistance: this is discernible only when the load changes with time.

Load regulation: this gives a measure of the fluctuations in the load voltage as the load current changes; it should ideally be infinitely large. The smaller the internal resistance, the better the load regulation.

Line regulation: this should ideally be infinitely large. It is a measure of the effect changes in the input voltage have on the nominal output voltage.

Ripple: this should ideally be fully suppressed. When rectification is full-wave its frequency is twice the mains frequency. The larger the regulating factor, the smaller the ripple at the output.

Noise: ideally, there should not be any. It originates primarily in the reference voltage source and in components in the regulator section.

Overshoot and undershoot: the regulating process causes small (mV range), short-duration deviations from the load voltage. Ideally, these should not occur.

Long-term stability: affected primarily by ageing processes in the reference voltage source; ideally, the load voltage should not change with time.

Thermal stability: dependent mainly on the quality of the voltage reference source; the load voltage should ideally not vary with changes in ambient temperature.

Power dissipation: this should ideally be small; it is the product of the voltage drop across the regulator and the load current plus losses in the transformer and rectifier.

Overcurrent protection: this becomes active when the load current starts to exceed its nominal value. It is required not only to guard the load from excessive currents under fault conditions, but also to protect the power supply from damage.

Short-circuit protection: ideally, the supply should be able to withstand a short-circuit indefinitely; the protection is often combined with overcurrent protection .

Power supply operation

The basic circuit diagram of a regulated power supply is shown in Fig. 1. The input section consists of the mains transformer, rectifier and filter capacitor. The remainder, regulator, error amplifier and reference voltage source, is required for regulating the load voltage. The entire regulating circuit can be housed on an integrated chip, such as those in the 78xx series.

The quality of the power supply depends primarily on the excellence of the regulating section. Nevertheless, although the internal resistance of the supply, and thus its load regulation, is highly dependent on the gain of the error amplifier, the internal resistance of the transformer, rectifier and reservoir capacitor also play a role.

If the total (static) internal resistance of the input section is, say, 2 Ω, and the amplification of the error amplifier is $\alpha = 1000$, the total (static) internal resistance of the supply is 2 mΩ. This ignores, of course, the resistance of the wiring, the PCB tracks, and so on. The amplification available for regulation consists of the open-loop gain and the closed-loop gain. The latter corresponds to the line regulation (≈ change in input voltage/resulting variation in output voltage).

Setting the amplification very high to reduce the internal resistance to an absolute minimum is not a practical proposition, because, since the error amplifier and power transistor require a finite time to react to changes, the build-up or decay transients increase in proportion to the amplification.

When top quality is required, close attention should be paid to the design of the mains transformer, particularly its (static) internal resistance. Above all, it should be designed so as to meet its requirements handsomely. C-type and toroidal cores, because of smaller stray losses, generally result in smaller internal resistances than the conventional laminated cores.

The capacitance of the reservoir capaci-

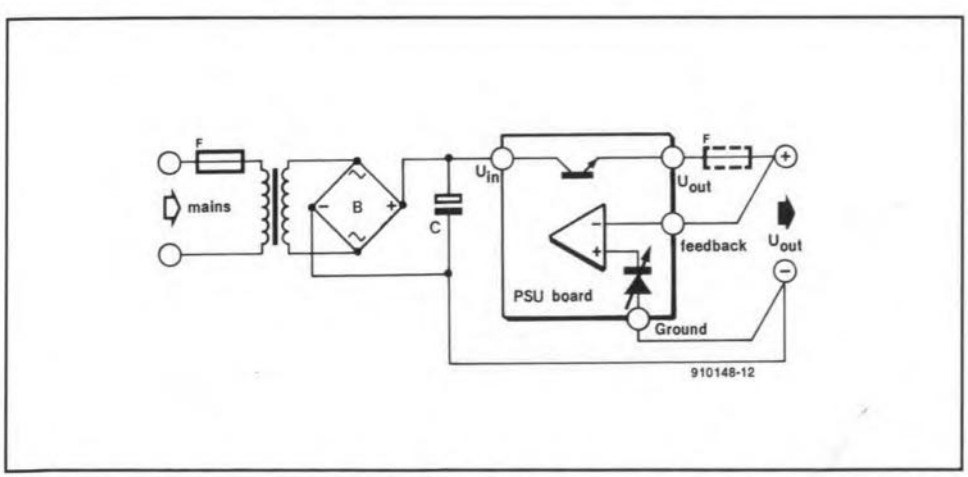


Fig. 2. Wiring diagram of a regulated power supply showing how the unit should be wired up. Note the location of the fuse(s).

tor affects not only the dynamic internal resistance, but also the ripple on the load voltage.

The thermal stability and noise are determined primarily by the reference voltage source. Three-terminal voltage regulators normally have this source on board, which therefore gets as hot as the power transistor—not an ideal situation.

Noise and other spurious signals can normally be reduced appreciably by shunting the voltage source with a small, foil-type decoupling capacitor.

Apart from the quality of the reference source itself, the power supplied to it is also important and should, therefore, be regulated.

It is, of course, essential that a power supply is wired correctly. If the general diagram in Fig. 2 is followed, and heavy-duty wire is used, the internal resistance and ripple will be a minimum.

Fuses should, in general, be located in the +ve input (UK: 'live') line to the mains transformer. Added security is obtained by a fuse between the power transistor and the feedback take-off for the error amplifier (as shown in dashed lines in Fig. 2). The voltage drop across the fuse is compensated by the regulating process. The fuse must be located on the PCB.

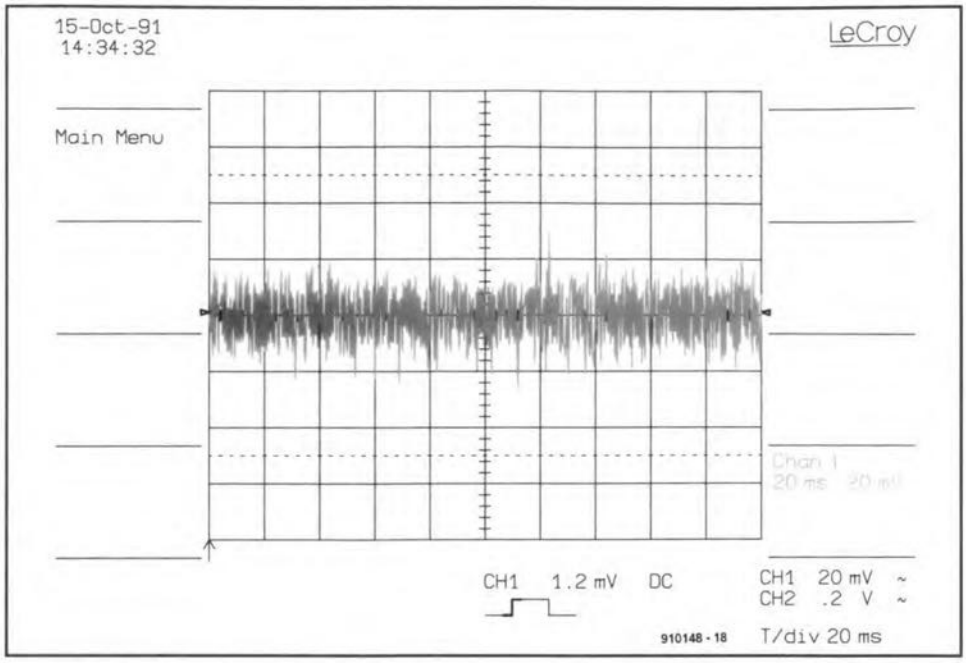


Fig. 3. Representation of noise output of a power supply as seen on an oscilloscope. Noise can be defined as random-frequency signals that extend over a considerable frequency spectrum.

Measurement methods

The most important parameter of a power supply is its static internal resistance. Fortunately, this can be measured fairly easily with a multimeter and a suitable load.

Because of the greater accuracy of its read-out, a digital multimeter is preferred. Moreover, the measurement accuracy of a digital multimeter, even of economy types, is generally better (error <1% on d.c. ranges) than that of an analogue meter in the same price range.

During current measurements, the voltage drop across the meter is important: it should be small and even with large output currents not exceed 200 mV. Note that many 3 ½ digit multimeters have no 200 mV range.

For a 12 V, 2 A power supply, a 6 Ω, 24 W load is needed. This can, for instance, be made from five 33 Ω, 5 W resistors in parallel. The total resistance is then 6.6 Ω, but that is more an advantage than disadvantage, because the load current will then be 1.8 A, a value that can be read very accurately on most digital multimeters. Note that the dissipated heat can easily burn the surface of a table or your fingers.

A better load is provided by a so-called resistor box containing, for instance, 20 or more 0.47 Ω, 5 W resistors that can be interconnected in various ways. Such a box (there are several varieties) can provide a variable load of 0.47–10 Ω rated at 3 A. It is invaluable if a number of power supplies are to be tested.

First, measure the open-circuit output (electro-motive force—e.m.f.), which is, say, 12.08 V. Next, connect the 6 Ω load and measure the current through it, which is, say, 1.836 A. Then, measure the voltage across the load, which is, say, 11.98 V. The difference between the e.m.f. and the load voltage is thus 10 mV. Since the load current is 1.836 A, the internal resistance is $10 \times 10^{-3} / 1.836 \approx 5.5$ mΩ, a reasonably good value.

If the internal resistance of the multimeter is not taken into account during the current measurement (when the meter is in series with the load) a small error results. If, in the example discussed, the voltage drop across the meter was 186 mV (R_i = 100 mΩ), the calculated value of the internal resistance was 1.5% too large. This error can be ignored, because the tolerance of the load causes a larger error (do not forget the increase in resistance caused by heating).

To measure the dynamic internal resistance, and determine noise and ripple, an oscilloscope is indispensable. The scope, connected across the output terminals, is set to its lowest a.c. range, normally 5 mV per screen division, and the time base to 10 ms per division. Both noise, that is, random-frequency signals extending over a considerable frequency spectrum, and ripple, the unavoidable by-product of rectification, here with a period of 10 ms, are displayed—see Fig. 3 and Fig. 4 respectively. The ripple will increase slightly when a load is connected to the supply. As long as the peak-to-peak amplitudes do not exceed a few mV, all is well. If, however, on load, the ripple has a period of 10 ms and a peak-to-peak amplitude of sev-

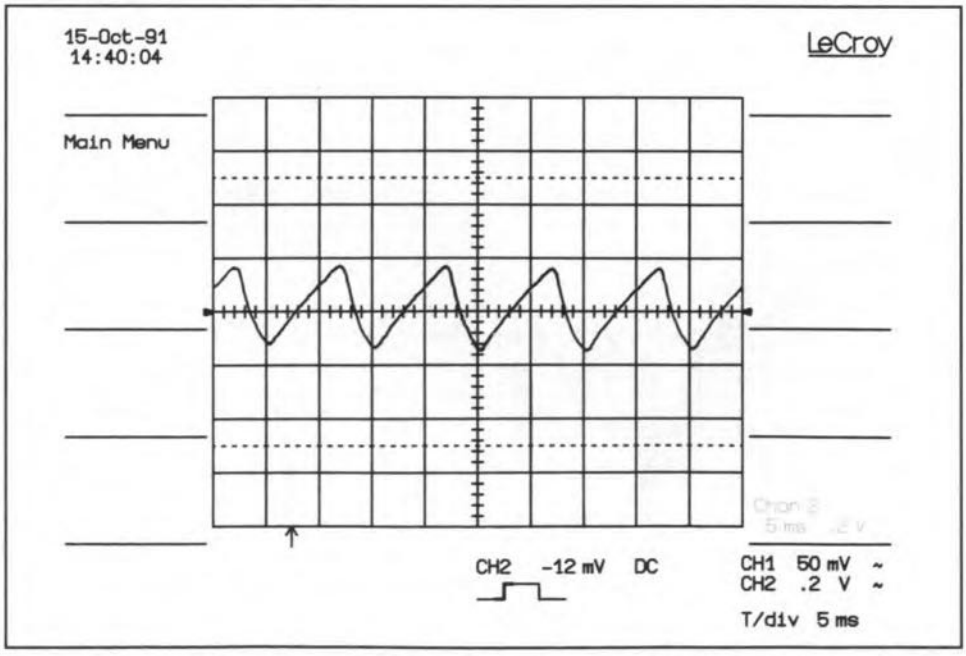


Fig. 4. Representation of a typical 100 mV ripple on the output of a power supply as seen on an oscilloscope.

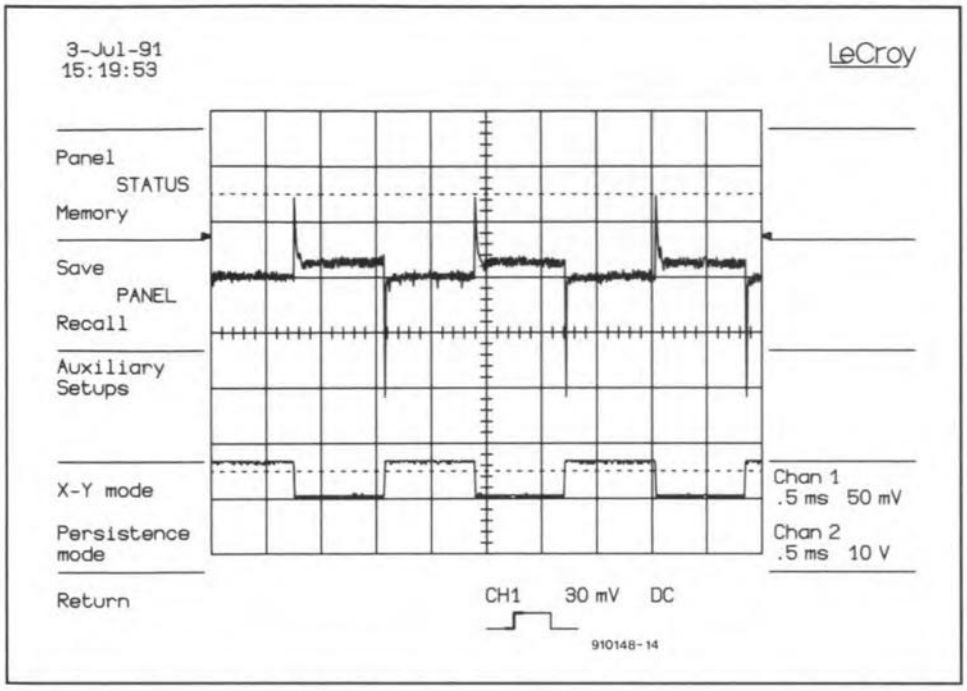


Fig. 5. Representation of the dynamic behaviour of the output voltage of a power supply (upper trace) loaded with the set-up of Fig. 6. The lower trace shows the drive (base signal) to T_1.

eral hundred mV, the input voltage to the regulating section is too small. That means that either the current rating or the secondary voltage rating of the mains transformer is too low. The current rating should be some 1.5× the peak d.c. output current of the supply. The secondary voltage depends to some extent on the design of the regulator and on the capacitance of the reservoir capacitor. For instance, a rating of 12 V~ for a 12 V power supply is clearly too low and should have been 15 V. It is, however, also possible, provided the ripple on load is small, to increase the value of the reservoir capacitor from, say, 4700 µF to 10000 µF.

To ascertain the behaviour of the power supply with rapidly changing load values,

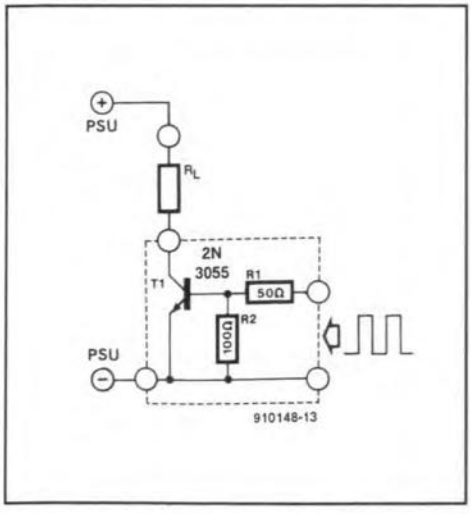


Fig. 6. Rapidly changing loads may be simulated by a power transistor and a rectangular-wave generator. Such a load enables the dynamic behaviour of a power supply to be determined.

its dynamic internal resistance must be determined and the load voltage observed on an oscilloscope. For this purpose, the rapidly changing load can be simulated by the set-up shown in Fig. 6. The function generator should be able to provide rectangular signals from a low-impedance (<50 Ω) output at a level of not less than 5 V p-p. This ensures full drive for T_1 which then draws a current of about 2 A. If a larger current is required, T_1 must be replaced by an appropriate darlington power transistor.

If a function generator is not available, a rectangular-signal generator can be built with the aid of the well-known Type 555, which is ideal for this purpose.

The transistor should be fitted on a small heat sink, since, in spite of the switching operation, it dissipates 2–4 W when the current is 2 A. If the power supply is rated above 45 V, it is advisable to use a sturdier type of transistor, for instance, the Type 2N3055.

The circuit in Fig. 6 is especially suitable for drive frequencies of up to about 2 kHz; note that 1 kHz is the typical frequency at which the dynamic behaviour of a power supply is usually determined.

With the function generator, set to 1 kHz, connected to the power supply via the circuit in Fig. 6 and an oscilloscope (time base set to 0.5 ms per division; amplification set to 10 mV per division) connected across the load, the screen display should be roughly as shown in Fig. 5. The upper trace shows that the regulator cannot follow the rapid changes. When the load is switched on, the load voltage initially drops sharply; only when the power transistor has resumed full drive does the load voltage return to its nominal value. The process on switch-off is similar: the regulator allows the power transistor to remain on for just a little too long. The duration of the voltage peaks in the upper trace gives an idea of how fast the regulator works.

The amplitude of the spikes can be reduced to some extent by a 100 nF capacitor across the output terminals or, preferably, directly across the load.

Apart from the overshoot and undershoot in Fig. 6, the trace also shows another, much smaller, variation with time when the load is constant. That tiny rectangular signal, superimposed on the load voltage, is caused by the dynamic internal resistance of the current source. Its magnitude is determined by reading the value of the rectangular signal on the oscilloscope screen (this is, say, 15 mV p-p) and divide this by the current through the load (measured with the multimeter in series with the load). To ensure that the current flows uninterruptedly during the measurement, the input of the circuit in Fig. 6 (R_1) is connected to, say, 5 V d.c. If the load current is, say, 1.77 A, the dynamic internal resistance is $15\times10^{-3}/1.77 = 8.5$ mΩ.

What quality is required?

Now it has been shown what parameters of a power supply can be measured, and how, the question remains "what quality should a power supply have for a given application?"

For a.f. output amplifiers, a regulated power is normally not needed, but in the a.f. pre-amplifier(s) the suppression of noise and ripple are of paramount importance.

For small digital circuits, the quality provided by a three-wire regulator is normally more than adequate. Care should be taken with 5 V power supplies for complex digital circuits that contain TLL ICs (computers, for instance). Here, the 5 V load voltage should be set accurately to 5.15 V, since at lower values, because of the potential drop across the PCB tracks, the supply to some TTL ICs may become too low for reliable operation.

Power supplies for use in a laboratory or workshop are, as might be expected, the most demanding as regards noise, ripple, static/dynamic internal resistance and dynamic behaviour. Moreover, they should have a variable voltage/current output. All these facilities cost money, of course, and this cost should be considered in relation to the applications for which the supply is, or may be, needed. ■

Useful literature:

Power Electronics Handbook by F.F. Mazda, Butterworths (1990), ISBN 0 408 03004 6.

Electronic Instruments and Measurement Techniques, by F.F. Mazda, Cambridge University Press (1987), ISBN 0 521 26873 7.

Design & Build Electronic Power Supplies, by Irving M. Gottlieb, Tab Books (McGraw-Hill) (1991), ISBN 0 8306 6540 4.

High-frequency Switching Power Supplies, by George C. Chryssis, McGraw-Hill (1989), ISBN 0 07 010951 6

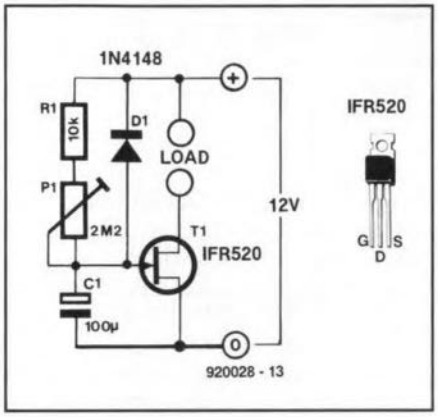
DESIGN IDEAS

The contents of this column are based solely on information supplied by the author and do not imply practical experience by *Elektor Electronics*

Simple timer

by K. R. Kirwan

THE circuit shown below is a simple, yet versatile, timer. It allows loads drawing up to 5 A, for instance, a low-voltage power supply, to warm up slowly. With values as shown, the warm-up time will be 2 minutes.



The main element is a power FET, T_1, which has an impedance of only 300 mΩ and is capable of sinking or sourcing 5 A if it is fitted on a suitable heat sink.

On switch-on, C_1 is charged slowly through P_1, whereupon T_1 begins to conduct. When the FET is fully conducting, the voltage drop across it is only 600 mV.

If P_1 and C_1 are swopped around, the opposite will happen: full voltage across the load on switch-on, which gradually drops to zero.

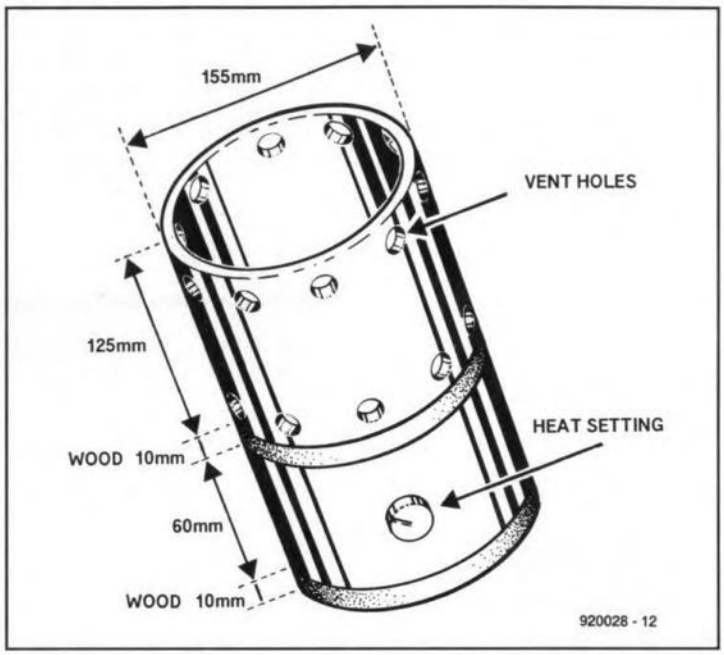
The load can be placed in series with either the drain or the source. A good starting point for further experimentation . . . ■

Make light work of wok cooking

by K. R. Kirwan

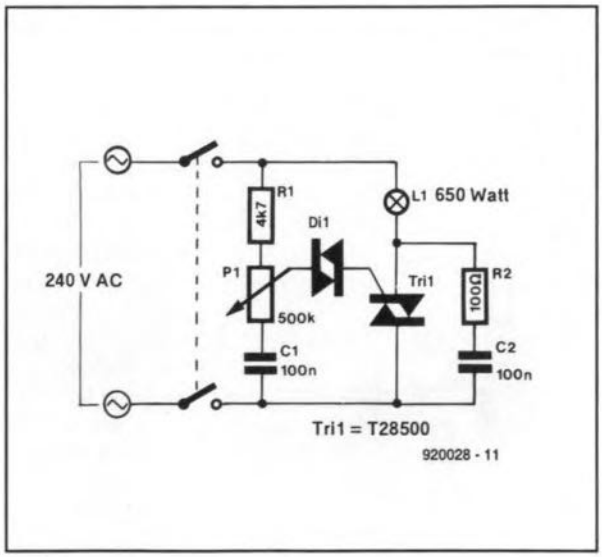
MANY people nowadays do a lot of cooking in their wok, usually on a gas or electric stove, but the idea outlined below, which I have been using for some time and find really good and portable, is based on light. I have used as a container a large catering tin of Nescafe, empty of course, with the lamp mounted in the top tin, with another tin cut into half and a piece of wood insulating the two tins from the heat bolted together. The electronics are mounted in the bottom half, which is finished off with another piece of wood—see first diagram.

In the top tin, which houses the lamp, I have drilled 13 holes of ½ in diameter 1 in down from the top and 13 holes of ½ in diameter 1 in up from the bottom of the top tin for ventilation of the lamp.



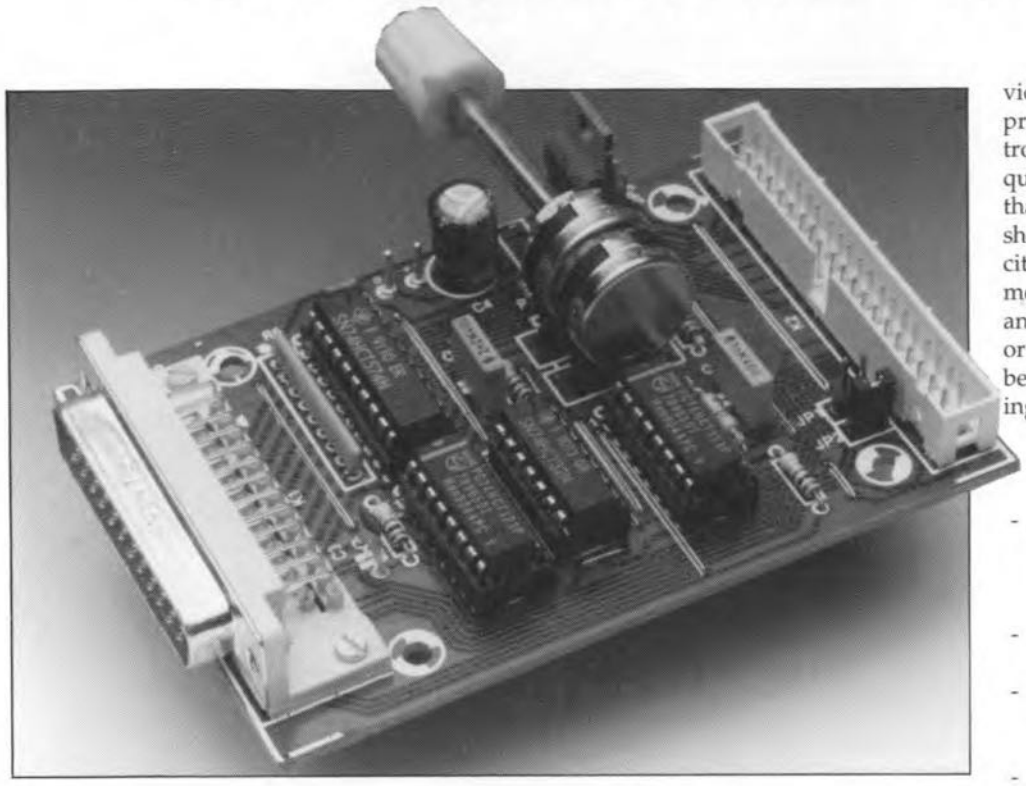
The centre piece of wood has a hole drilled in it to pass the heat resistant cable connecting the electronics to the lamp.

I have used a 650 W Atlas P2/123 projector lamp, left in its original base with reflector and adjuster and a triac that controls the 240 V, 50 Hz mains, from 2% to 98% of full power. This arrangement ensures that the wok cooker is fully controllable from just keeping food warm to stir frying within minutes.



The lamp holder is mounted on a M3 screwed rod so that the lamp can be adjusted to centre the focal point on the bottom of the wok. ■

CENTRONICS LINE BOOSTER



Put your printer a little further away from the PC, connect it with a ready-made 5-metre long Centronics cable, and you may be in for a surprise. Missing characters and error beeps all around you. The problem is obvious: not enough drive power on the Centronics port!

Design by A. Rietjens

TODAY no PC is sold without one or more parallel printer ports. Interestingly, these ports are often referred to as 'Centronics compatible' when in fact they are simply TTL buffers, whose specifications certainly do not meet the Centronics standards as regards signal timing and drive capacity. Consequently, these 'stripped down' versions of the Centronics port can be used with relatively short printer cables only, and often result in erratic behaviour of an otherwise perfectly operating printer. The circuit described here overcomes this problem by boosting the signals on the parallel printer port, allowing long cables to be used between the PC and the printer.

On handshaking

It should be simple, really: only three lines arrange the handshaking necessary for unidirectional data transfer via eight parallel datalines. The Centronics standard further specifies the use of a couple of printer status lines, but these should not cause problems either. To reduce the cost of their products, most PC and printer manufacturers implement only one or two of the available printer status lines: Paper End, Auto Feed, Printer Error, Printer Select and Printer Init.

When the PC starts a printer output job, the BUSY input on its parallel printer port is usually low, which indicates that the printer is waiting for data. Next, the PC puts the data on the eight datalines, D0-D7, and informs the printer that valid data is available by pulling the $\overline{\text{STROBE}}$ line low briefly. To indicate that it has received the databyte, the printer responds to the PC by making the BUSY line high on the negative edge of the $\overline{\text{STROBE}}$ pulse. Once the printer has processed the byte—which means that it has been either printed or stored in a buffer—it pulls BUSY low again, and in addition supplies a short pulse on the $\overline{\text{ACKNLG}}$ line to the PC.

As shown in Fig. 2, the time difference between the active $\overline{\text{ACKNLG}}$ and the BUSY signals is specific to the type of printer, and may differ by a few microseconds. With Centronics compatible printers, the $\overline{\text{ACKNLG}}$ pulse starts on the negative edge of the BUSY pulse, while with Epson compatible printers it is ended by that time.

Requirements

The Centronics standard specifies that each dataline and handshaking line must be individually screened in the cable between the printer port and the printer. Not all 'Centronics' cables on the market meet this requirement, however, whence the problems that may occur when an inexpensive cable as short as, say, 3 m is used. The parasitic capacitances introduced by such a cable make a mess of the relatively short control signals, and the printer either produces error signals, or garbles the characters. This problem can be solved by a circuit that meets the following requirements:

- data must be held stable for a certain time;
- the length of the $\overline{\text{STROBE}}$ signal supplied by the PC must be adapted depending on the length of the printer cable;
- the BUSY signal must be available sufficiently long for the PC to process;
- the $\overline{\text{ACKNLG}}$ signal must be generated at a well-defined length after the BUSY line is deactuated;
- none of the other control lines should be affected.

Circuit description

The circuit shown in Fig. 1 is designed to meet all of the above requirements. The computer is connected to K1, the printer to K2. The functional description that follows is based on the assumption that the PC is running, and the printer is switched on and 'on line'.

The negative edge of the first strobe pulse supplied by the computer triggers monostable IC1a. The resultant pulse at the Q output of the monostable causes IC5 to latch the byte available on the datalines, D0-D7. The output of the latch is connected to the printer via the printer cable. The $\overline{\text{Q}}$ output of monostable IC1a, pin 4, supplies the $\overline{\text{STRBOUT}}$ pulse, which is a lengthened copy of the $\overline{\text{STRB}}$ (strobe) pulse supplied by the computer. The $\overline{\text{STRBOUT}}$ pulse is fed to the printer (via pin 3 of connector K2) as well as to the trigger input of a second monostable, IC1b, where is it again lengthened before it is combined with the BUSY signal from the printer in OR gate IC4c. The lengthened BUSY signal is fed to the respective port line on the PC. The upshot is that if the printer is still busy when the monotime of IC1b has lapsed, it can continue to keep the computer waiting. When the monotime of IC1b has lapsed, **and** the printer is ready again (i.e., the BUSYIN line has returned to low), the output of IC4c goes low also, and triggers the third monostable in the circuit, IC2a. By generating a short $\overline{\text{ACKNLG}}$ pulse for the computer, IC2a closes off the handshaking protocol for one databyte, and the system is then ready to process the next one when this is applied by the PC.

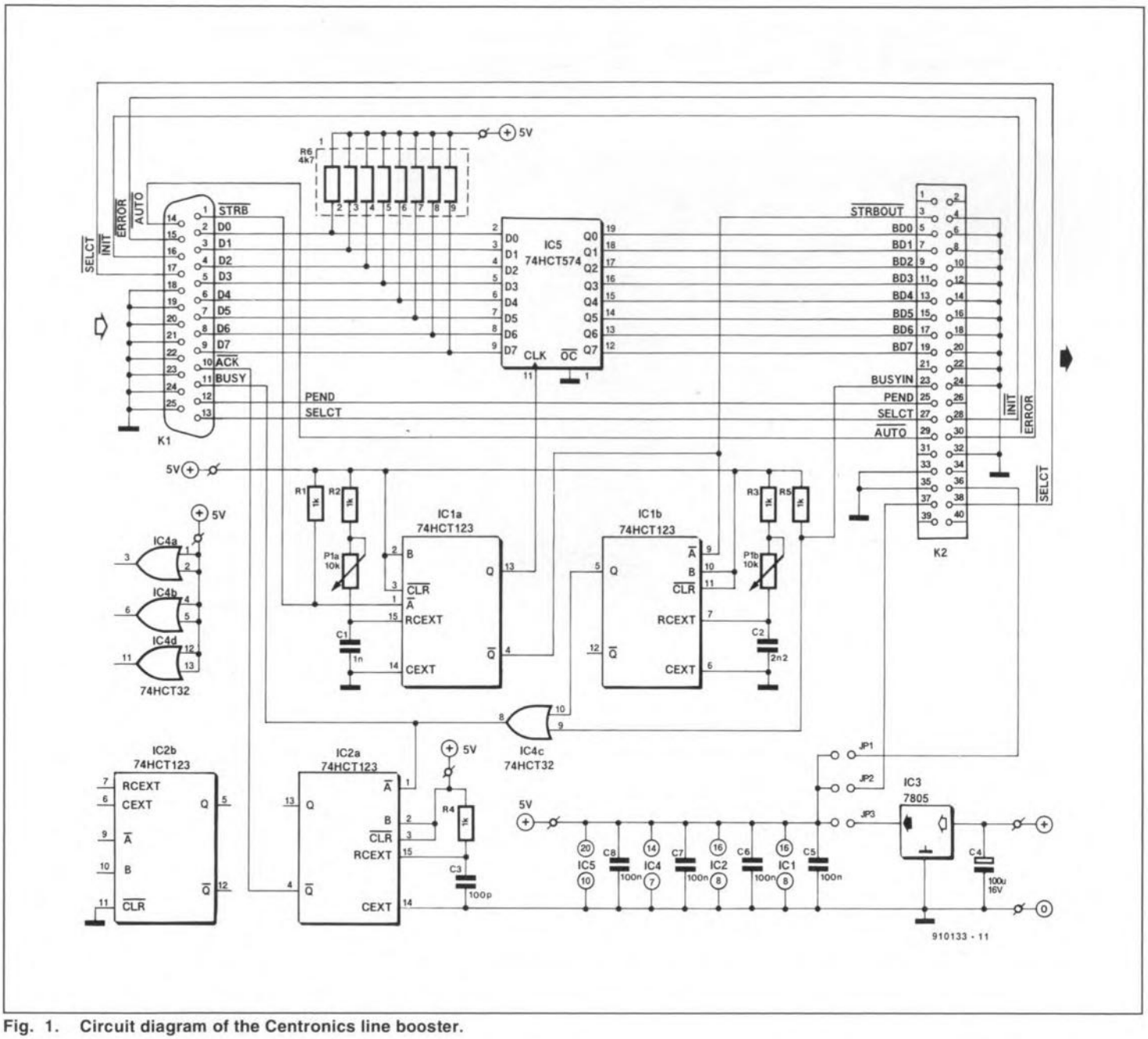


Fig. 1. Circuit diagram of the Centronics line booster.

All other control lines between the PC and the printer, such as AUTO and ERROR, are generally uncritical, and connected straight between the input connector, K1 (a 25-way sub-D type), and the output connector, K2 (a 40-way pin header or box header).

Construction

To keep the line booster as small as possible, the printed circuit board (Fig. 3) is pretty 'crowded'. Start the construction by fitting the ten wire links on the board. Next, fit the IC sockets and the passive components (capacitors, resistors and wire jumpers). Note that the power supply parts, IC3 and C4, are required only if the unit is powered by an external supply, i.e., not by the printer. Most printers supply +5 V at input connector pin 18 or 35. When this voltage is available, fit jumper JP1 or JP2 instead of JP3 on the

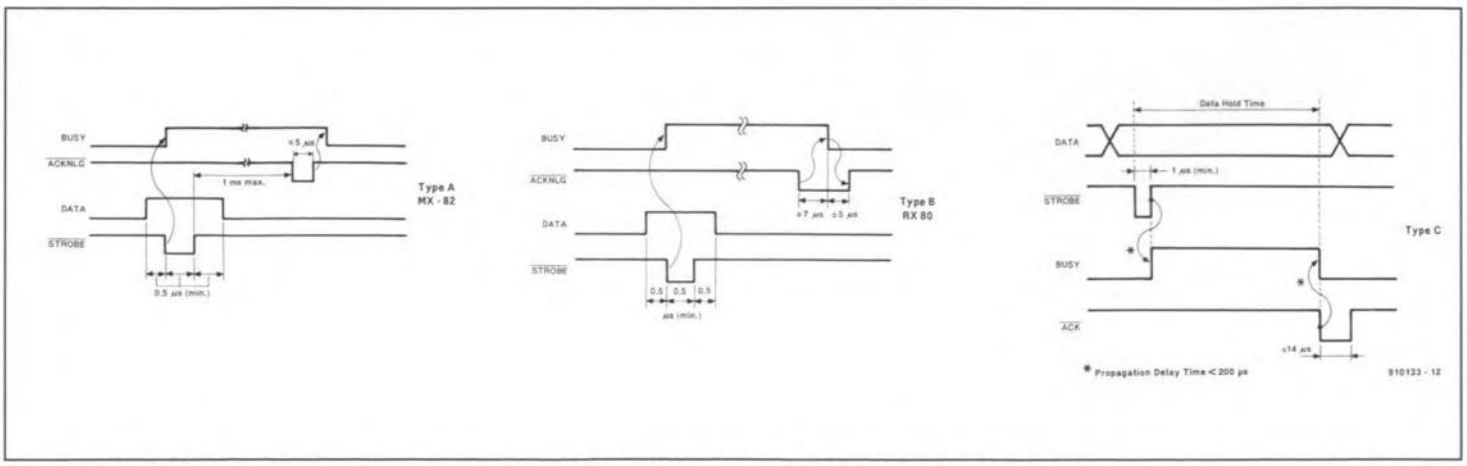


Fig. 2. Printers may differ in respect of the timing of the BUSY/ACKNOWLEDGE handshaking signals.

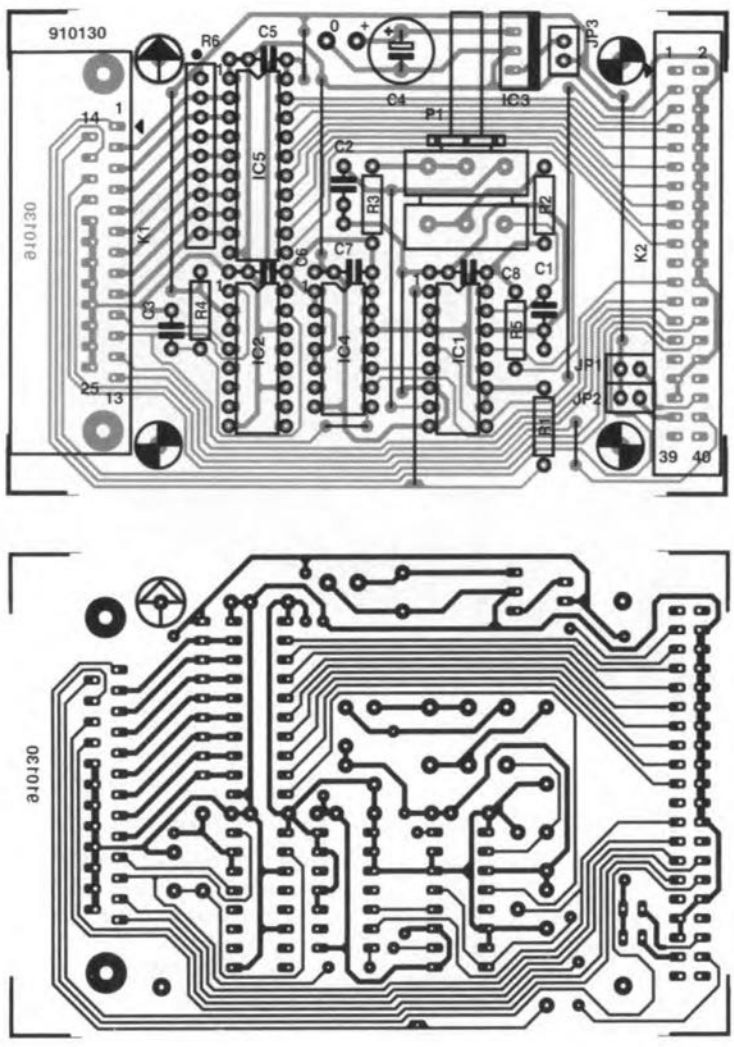


Fig. 3. Single-sided printed circuit board for the project.

COMPONENTS LIST

Resistors:

5	1kΩ	R1-R5
1	8-way 4kΩ7 SIL array	R6
1	10kΩ lin. stereo potentiometer	P1

Capacitors:

1	1nF	C1
1	2nF2	C2
1	100pF	C3
1	100µF 16V radial	C4
4	100nF	C5-C8

Semiconductors:

2	74HCT123	IC1;IC2
1	7805	IC3
1	74HCT32	IC4
1	74HCT574	IC5

Miscellaneous:

1	25-way sub-D plug for PCB mounting	K1
1	40-way box header	K2
1	Printed circuit board	910133

board. The last parts to be fitted before inserting the ICs are the dual-gang (stereo) potentiometer, P1, and the connectors, K1 and K2.

The printer is connected via a short length of 40-way flatcable, one end of which is fitted with an IDC socket (to mate with the pin header on the board), and the other with an IDC-type 36-way Centronics ('blue ribbon') connector. The PC is connected to the booster via an RS232 cable **without** swapped TxD/RxD wires (pins 2 and 3), while the booster is connected to the printer via a Centronics extension cable. The booster should, of course, be located as close as possible to the PC.

The ACK/BUSY timing of the booster is simple to adjust. Initially, turn P1 fully clockwise (maximum resistance). Next, send a fairly long file to your printer, and while the printing is going on turn P1 anti-clockwise until you see the first errors appear. Turn P1 clockwise again until the errors disappear. This is the best setting of the delay, which should not be made larger than strictly necessary to prevent too low a data transfer speed. ■

Inmarsat to develop global paging via satellite

Business executives and professionals on the move will have access to a global satellite paging service using pocket-size receivers, as early as 1994.

Designed to operate via the Inmarsat satellite system, the pagers will enable mobile users on land to receive messages no matter where they are in the world. This will enable travelling executives, journalists and couriers to be contacted by their offices.

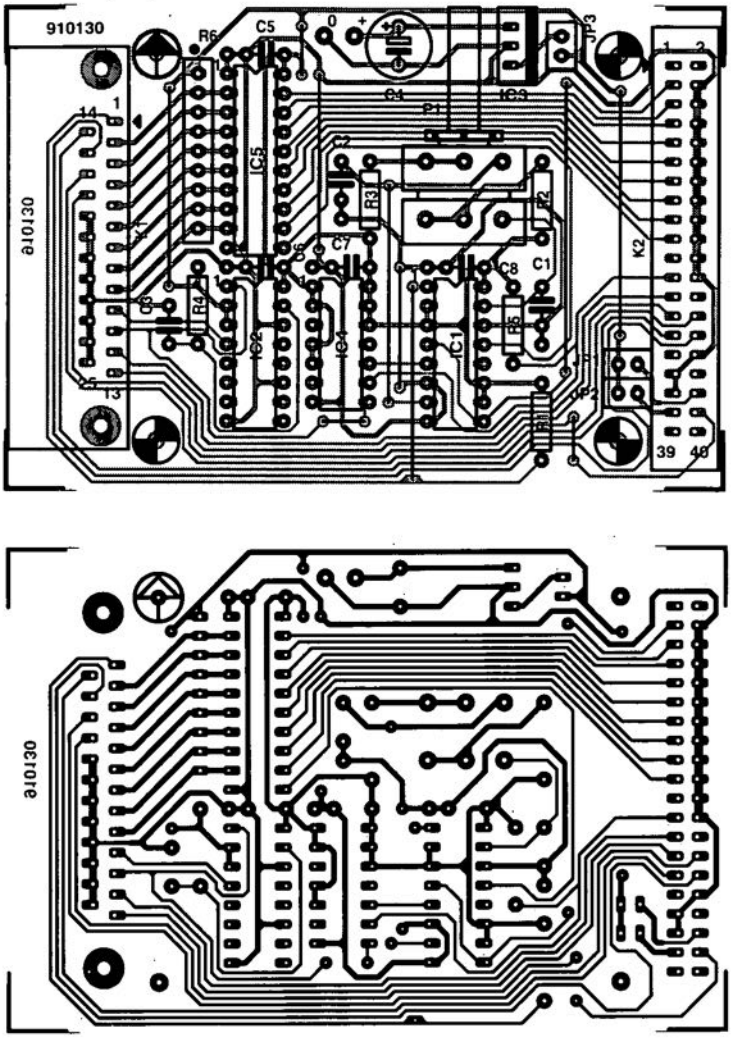
Although wide terrestrial paging services are available in many countries, including some that involve use of satellites for inter-system connections, the Inmarsat satellite paging service will be the first global, direct paging service via satellite, operating to a single worldwide standard. It is designed to provide a higher degree of penetration into urban areas than would normally be achieved by purely line-of-sight mobile satellite services.

Inmarsat, a 64-nation cooperative, operates a system of geostationary satellites to provide global mobile telephone, telex, facsimile and data services to maritime, aeronautical and land mobile users all over the world.

The decision on paging follows a series of technical and commercial studies and experiments over the last couple of years. This new service is designed to complement existing and planned terrestrial paging systems by providing a very wide area of coverage at affordable prices through the Inmarsat global satellite network.

The system will provide for conventional tone paging, as well as alphanumeric messages and various forms of data, to be displayed on a small LCD screen. A variety of receiver models are expected to be available—from pocket-sized stand-alone units, to those integrated into briefcase-sized Inmarsat-C or -M satcom terminals, and receivers designed for installation on commercial vehicles. With satellite pagers integrated into their Inmarsat briefcase satcoms terminals, subscribers can be paged and advised to call their offices, even if their terminals are turned off.

International Maritime Satellite Organization (Inmarsat), 40 Melton Street, London NW1 2EQ. Telephone: (071) 728 1000. Fax: (071) 728 1044.



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1	100µF 16V radial	C4
4	100nF	C5-C8

Semiconductors:

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1	74HCT574	IC5

Miscellaneous:

1	25-way sub-D plug for PCB mounting	K1
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1	Printed circuit board	910133

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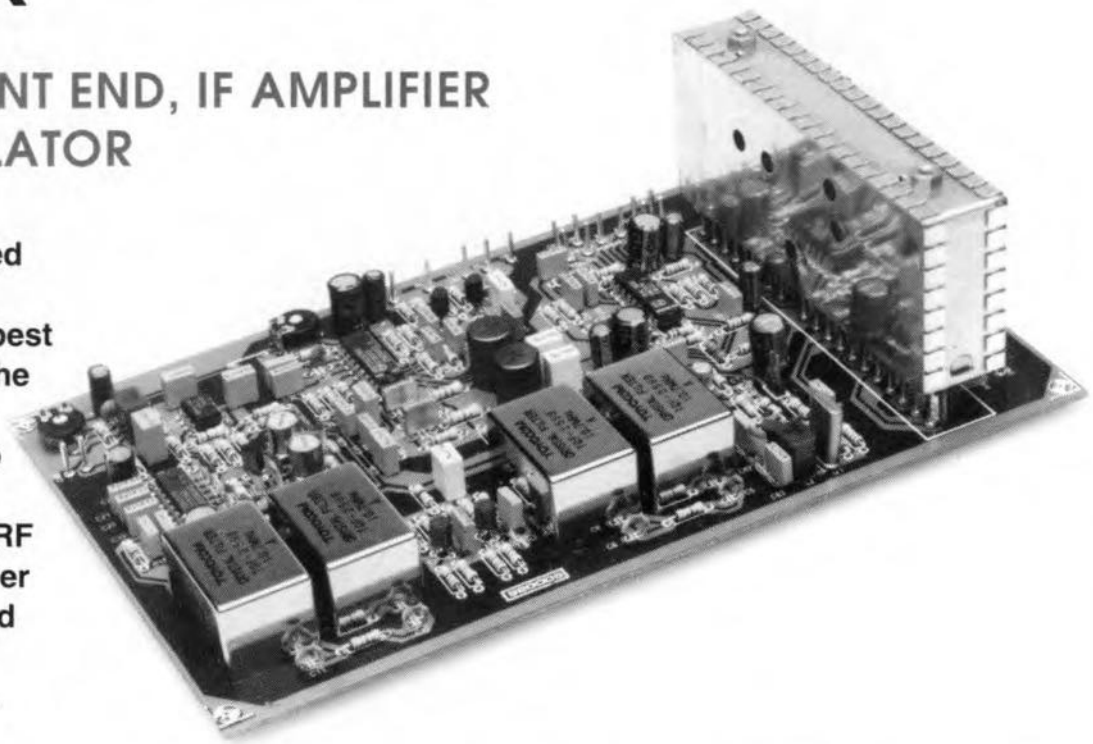
FM TUNER

PART 1: RF FRONT END, IF AMPLIFIER AND DEMODULATOR



An FM tuner is described whose specifications challenge those of the best receivers available on the market. A ready-made tuner module is used to prevent problems with building and adjusting RF circuitry, and the receiver is synthesizer controlled by a 80C32-based microprocessor circuit.

Design by H. Reelsen

SYNTHESIZER control of FM receivers is quire common these days, and even low-priced tuners offer a lot of technology in this respect. Whilst the performance and ease of control of such radios is quite reasonable, their design is almost invariably based on many compromises struck up to keep the price tag attractive. This not only applies to the design, but also to the materials used: plastic enclosures, a single, low-quality, PCB to hold all the components, simple front ends that suffer from cross-modulation, and IF (intermediate frequency) amplifiers based on ceramic filters.

Building your own FM tuner allows high quality components to be used throughout the design, while the total outlay remains within reason. Since synthesizer ICs used in professional communication receivers are now available on the component market, there should be no reason to design a synthesizer with, say, mediocre performance. The synthesizer used in the present FM tuner is controlled by a microcontroller from Intel's MCS51 family, with the program stored in an EPROM. This allows the tuner software to be modified, if necessary.

Overview

In contrast to much mass-produced equipment, home-made electronics can be designed to consist of separate modules (i.e., PCBs), each with its own function. Although this introduces wiring as a potential problem, modular construction is a must where digital and analogue technology meet. In the case of the tuner, it will be obvious that the digital signals produced in the synthesizer must not be allowed to enter the sensitive RF and AF circuits, where they cause interference.

Figure 1 shows an overview of the building blocks that go into the making of the FM tuner. The RF front end is formed by a high-quality, ready-made and pre-aligned tuner Type FD12. The tuning voltage is furnished by a synthesizer with keypad control. The microcontroller used in the synthesizer allows up to 99 preset frequencies to be stored—more than the maximum number of stations that would 'fit' in the VHF FM broadcast band (87 MHz to 108 MHz). A large, bright, LED readout indicates the preset number as well as the station frequency. The FD12 tuner module has a separate, buffered output for the VCO (voltage-controlled oscillator) signal, so that it does not need to be modified for the connection of the synthesizer.

The IF (intermediate frequency) amplifier is marked by excellent high-signal behaviour and selectivity. Four high-quality quartz filters are used in combination with two amplifier stages.

The limiter and demodulator functions are combined in a single IC, the TDA1576 from Philips Components. Interestingly, this IC is also found in many high-end FM receivers, of which some have been designated 'reference receiver' for comparative tests. A

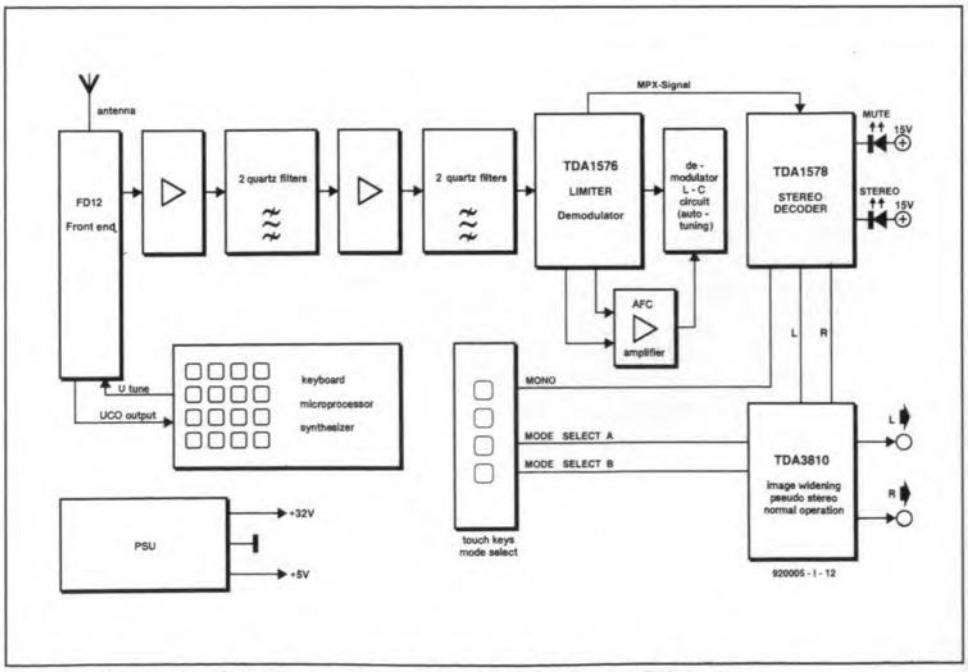


Fig. 1. Overview of the functional blocks that make up the FM tuner.

special feature of the present FM tuner is the automatic tuning of the resonant circuit used in the demodulator. This ensures very low distortion.

The stereo decoder is based on another Philips IC, the TDA1578. A phase correction filter is used to achieve the highest possible channel separation coupled with low distortion.

A TDA3810 is used in the AF output stage. As an option, this IC is capable of widening the stereo image and turning mono into pseudo-stereo. Normally, however, the IC will be used as a straight, high-quality, AF amplifier only that supplies a low-impedance output signal.

No adjustments?

Deciding to use high-quality components to build an FM tuner is one thing, building and adjusting RF circuitry quite another if you lack both experience and suitable test equipment. The FM tuner described here is designed such that adjustment is reduced to a minimum, and possible with simple equipment. First and foremost, a ready-made front end is used to eliminate all problems many of you would face when frequencies up to 150 MHz or so are involved.

The IF amplifier is a potentially bigger

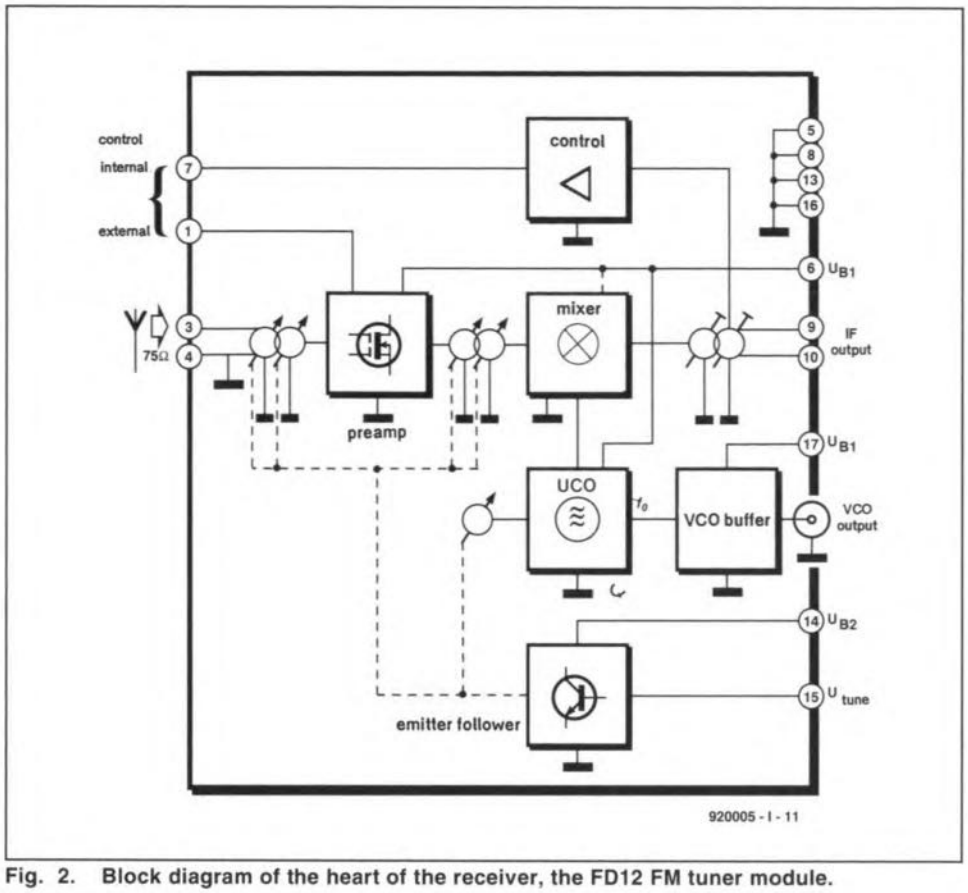


Fig. 2. Block diagram of the heart of the receiver, the FD12 FM tuner module.

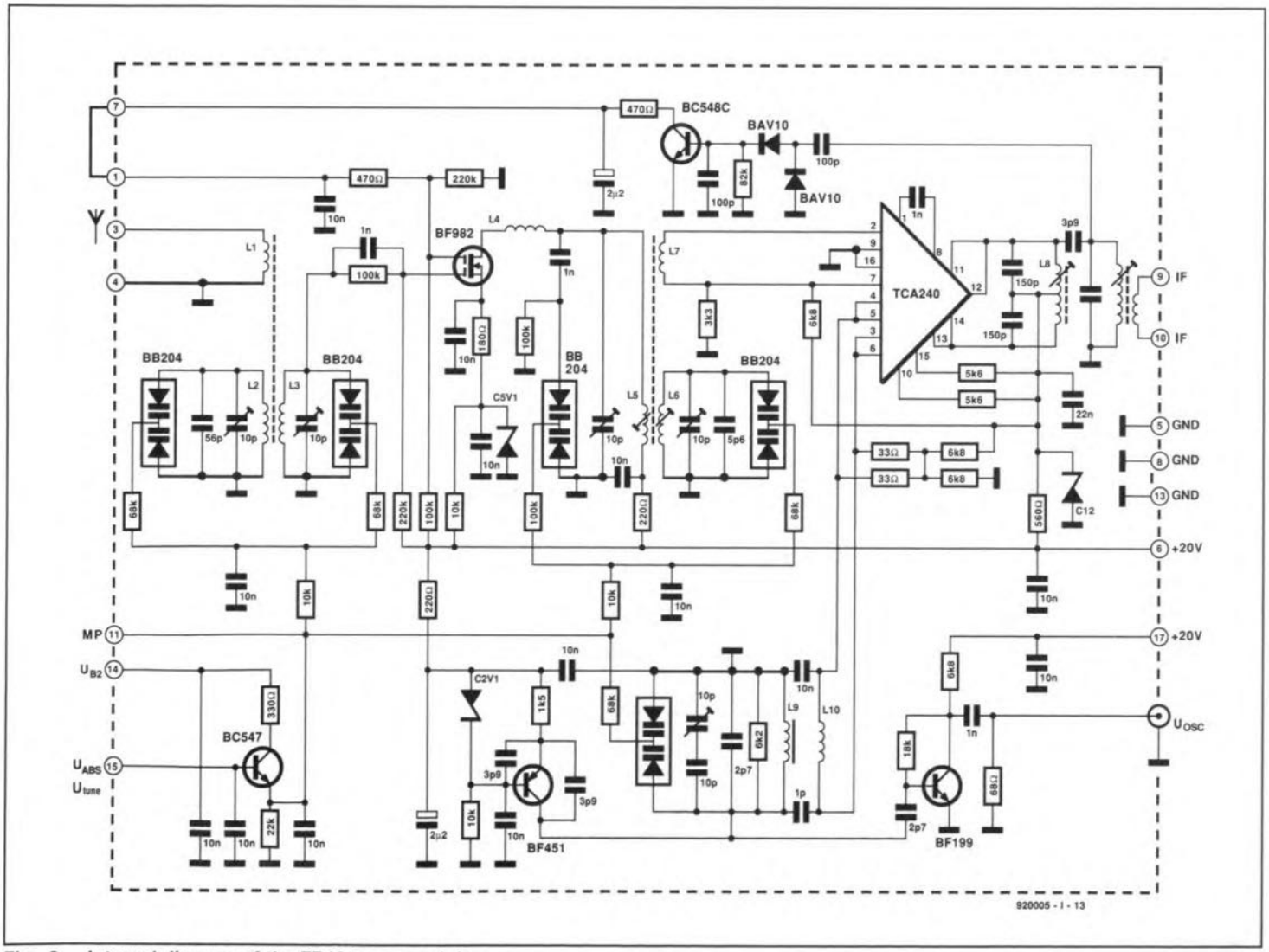


Fig. 3. Internal diagram of the FD12 tuner module.

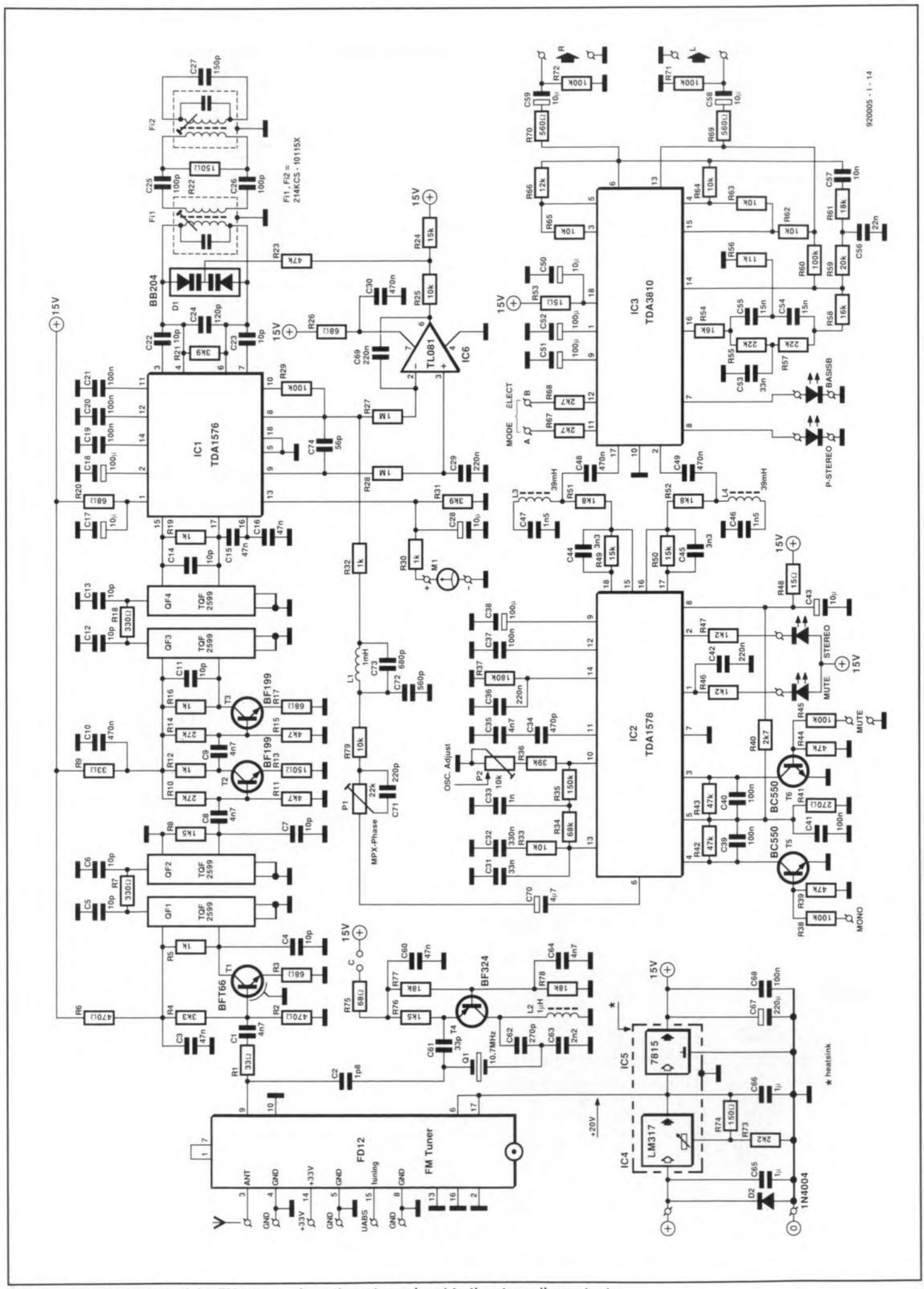


Fig. 4. Circuit diagram of the FM tuner — from the antenna input to the stereo line outputs.

problem, as it is hard to design anything that does not need to be adjusted in some way. Even ceramic filters still require additional tuned circuits to optimize the image rejection and the pass-band characteristic. These adjustments normally call for a swept-frequency generator. Furthermore, ceramic filters are really unsuitable for use in high-quality receivers.

Although four-pole and six-pole *L-C* filters with low ripple and constant group delay times are a certain way to achieve good sound reproduction, their adjustment requires special RF laboratory equipment and a lot of knowhow. Although many designers are enthusiastic about the 6-pole filters produced by Toko, it should ne noted that these devices are difficult to obtain in small quantities, and still require fine tuning. The only remaining alternative is, therefore, the quartz filter, which is generally applied in professional receivers. Quartz filters do not come cheap, but ensure very high selectivity and low pass-band ripple, without the need of adjustment (provided they are terminated correctly). As far as selectivity is concerned, the present tuner could make do with two quartz filters, provided an *L-C* filter is used for the image rejection. This, however, introduces and adjustment point, which was found undesirable.

Fortunately, the required image rejection, selectivity and pass-band characteristics could be achieved by using two pairs of quartz filters with an amplifier in between. This means that the IF amplifier has no tuned circuits at all, and, thus, no adjustment points.

Since the distortion of the demodulator depends mainly on the linearity of the quadrature tuned circuit, adjustment is inevitable at this point (the use of a ceramic resonator in a high-end design like this is out of the question). Here, a two-section *L-C* filter is used to ensure the lowest possible distortion level. Adjustment of this filter is made easy by an on-board 10.7-MHz quartz crystal oscillator which is used as an RF signal generator. Also, there is the previously mentioned automatic tuning facility that takes care of the demodulator fine tuning. This circuit also ensures good long-term stability, and prevents drift caused by temperature changes. The control automatically corrects deviations and tolerances, so that the distortion level remains low even after long periods of use.

FD12 front end

This FM tuner module was originally designed by Valvo (Philips Components Germany) some ten years ago, and marketed for high-quality receiver concepts such as cable head-end stations. Later, the production of the FD12 was taken over by a smaller company, Restek. The block diagram in Fig. 2 shows that the FD12 has a controlled RF prestage based on a dual-gate MOSFET and four tuned circuits with dual varicaps (variable capacitance diodes) Type BB204. The antenna input is 75-Ω unbalanced as customary on FM tuners. The extensive preamplifier and the double balanced mixer give the tuner very good specifications in regard of its noise figure and large signal behaviour. The noise figure is about 4 dB at a voltage gain of 40 dB, while the tuner can handle RF input levels up to 1 V_{rms} (in fact, the oscillator was found to be hardly detuned at an input voltage of 2 V_{rms}).

The tuning voltage for the five tuned circuits is buffered by an internal emitter follower. To make sure that the full tuning range can be covered (3.8 V to 27 V at pin 15 of the module), the supply voltage for the emitter follower must be about 30 V (pin 14). The normal supply voltage of the FD12 is 20 V (pins 6 and 17) at a current consumption of about 26 mA.

The IF signal is filtered at a bandwidth of 300 kHz by a tuned circuit at the output of the FD12. The IF signal is available at pin 9 of the module. The optimum termination impedance of the IF output is 330 Ω.

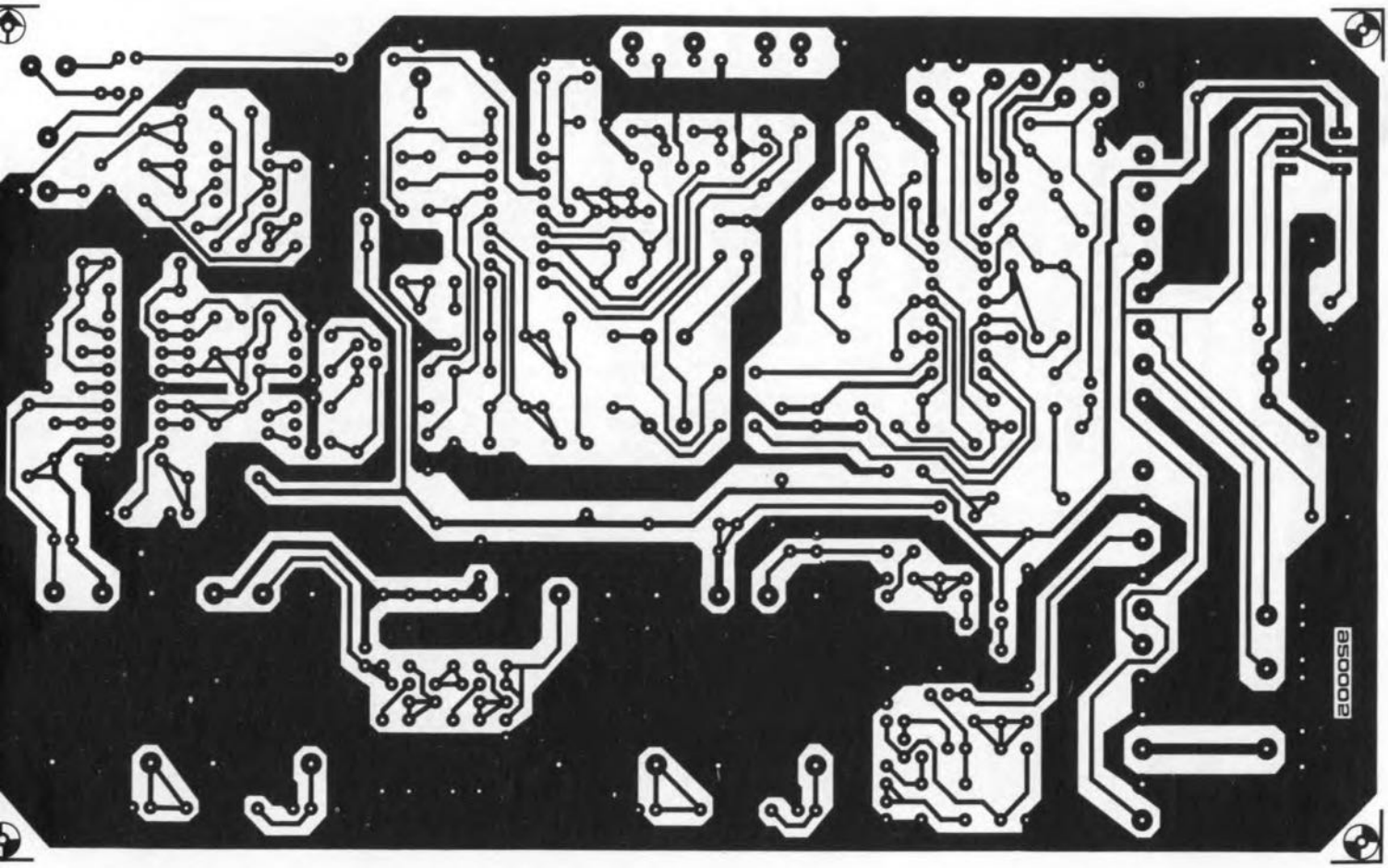


Fig. 5a. Track side copper layout of the PCB for the FM tuner.

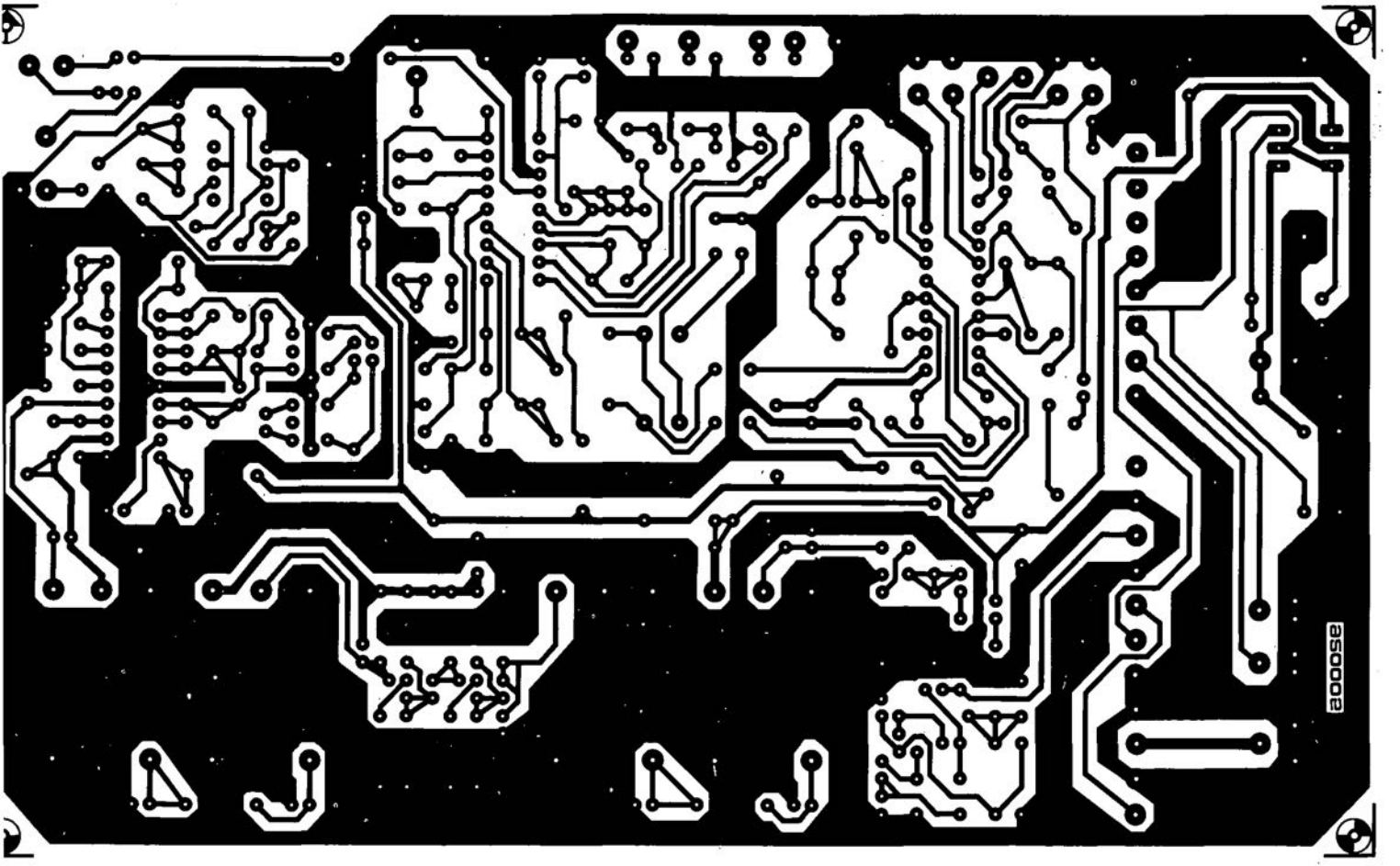


Fig. 5a. Track side copper layout of the PCB for the FM tuner.

Circuit description

The circuit diagram of the RF board is given in Fig. 4. The circuit shown comprises everything from the antenna input to the stereo outputs, and includes a simple regulated power supply with two output voltages.

IF amplifier

The IF output signal at pin 9 of the FD12 tuner module is fed to the first IF amplifier, T1, a bipolar transistor Type BFT66. The BFT66 is a low-noise type normally applied in low-noise antenna amplifiers because of its excellent linearity and large signal behaviour. The output of the previously mentioned 10.7-MHz test signal oscillator is coupled lightly (1.8 pF) to the IF output of the RF module. The test oscillator is enabled by fitting jumper 'C'. When the oscillator is not in use, the IF output signal is hardly loaded because of the light coupling via C2.

The output of the first IF amplifier is matched to the first quartz filter, QF1, a Type TQF2599 from Toyocom. Like the FD12 and the BFT66, this component was originally designed for use in cable head-end stations. QF1 is coupled to QF2 via a matching resistor, R7. Each filter block contains two quartz crystals.

Transistors T2 and T3 form an amplifier that serves to compensate the insertion loss introduced by QF1 and QF2. The two stages are nearly identical, and their input and output impedance is defined accurately by the rather strong feedback created by emitter resistors R13 and R17. After passing through the second pair of quartz filters, QF3 and QF4, the IF signal reaches the

Demodulator

The FM demodulator is based on the TDA1576 limiter/quadrature detector from Philips Components. This IC also provides a field strength meter driver, which is essentially a linear to logarithmic converter. This subcircuit is capable of driving a moving coil meter, M1, directly.

In the design of an FM tuner it is important that signal limiting (clipping as a result of overloading) does not occur at any stage before the limiter proper. This means that both the front end and the IF amplifier must have excellent large signal behaviour. The limiter contained in the TDA1576 works well at small signal levels already, and, more importantly, entirely symmetrically. This is important to achieve good AM suppression (most interference picked up by the antenna or induced in the receiver will be of the AM type).

The phase shifting circuit to complement the quadrature demodulator is formed by two *L-C* filters, Fl1 and Fl2. Since the tuner is synthesizer controlled, the AFC circuit contained in the TDA1576 can be used for a different purpose. When Fl1 is tuned exactly to 10.7 MHz (centre frequency), and when there is no modulation, the difference voltage between pin 8 and pin 9 of IC1 is 0 V. The level and the sign of the difference voltage is proportional to the deviation from the centre frequency. Normally, this is used to implement automatic frequency control (AFC) via the tuning voltage circuit. Here, however, a synthesizer affords the required frequency stability, so that an AFC is not required. This means that a voltage other than 0 V between pins 8 and 9 indicates that the tuned circuit of the quadrature demodulator is detuned. This drift may be caused by ageing, temperature changes, or simply by an incorrect centre frequency setting. In practice, it was found that demodulator detuning, however small, causes an increase in distortion from a very low level (0.05%) to 1 to 2%, which is unacceptable.

Opamp IC6 converts the AFC difference voltage into a tuning voltage for dual varicap D1 (a BB204). This keeps the quadrature inductor centred at 10.7 MHz. As with almost any frequency control system, there are limits to what can be corrected as far as the tuning is concerned. This means that the quadrature inductors, Fl1 and Fl2, have to be adjusted to enable the tuning system to

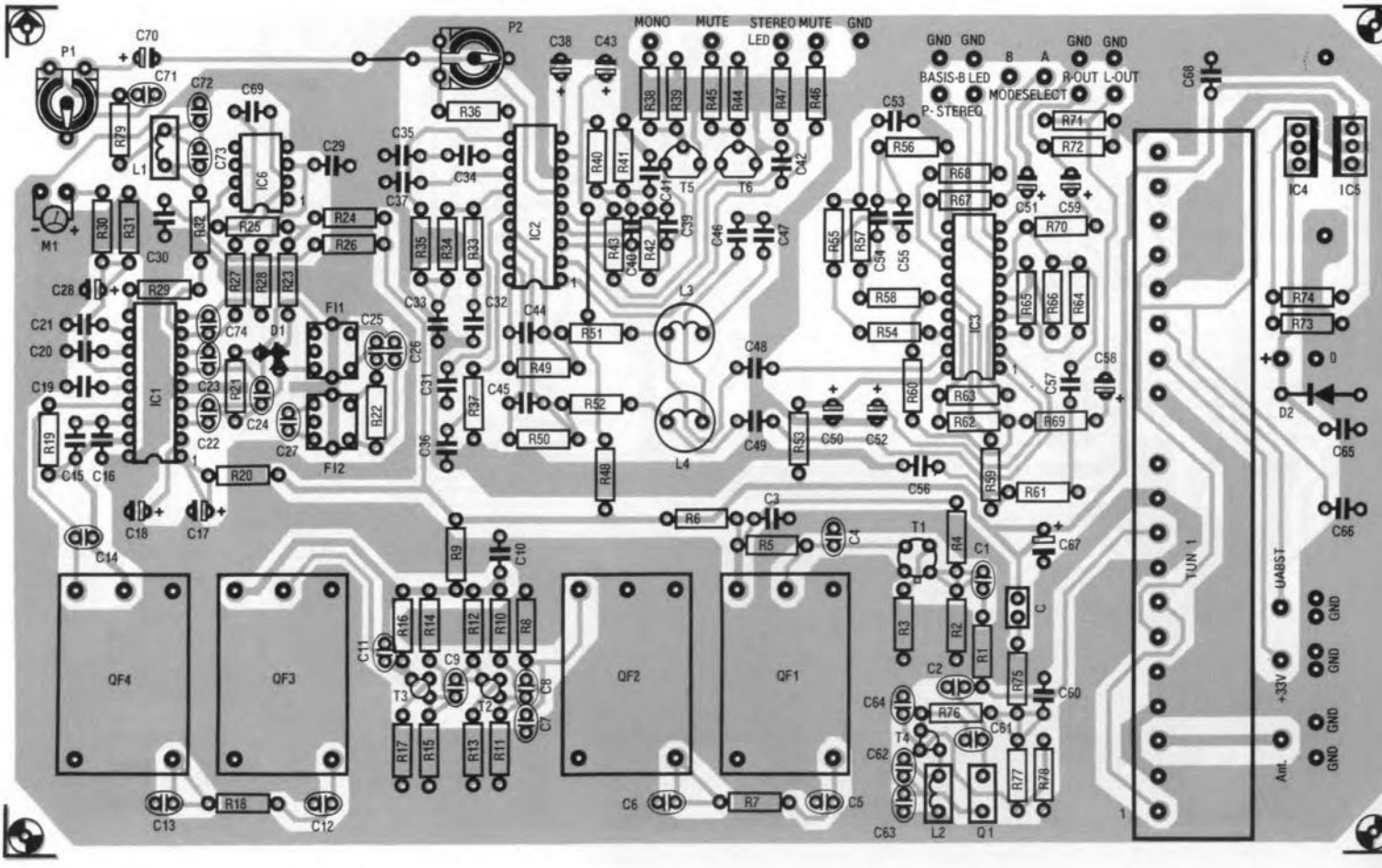


Fig. 5b. Component mounting plan.

COMPONENTS LIST

Resistors:

2	33Ω	R1;R9
2	15Ω	R48;R53
5	68Ω	R3;R17;R20;R26;R75
3	150Ω	R13;R22;R74
1	270Ω	R41
2	330Ω	R7;R18
2	470Ω	R2;R6
2	560Ω	R69;R70
6	1kΩ	R5;R12;R16;R19;R30;R32
2	1kΩ2	R46;R47
2	1kΩ5	R8;R76
2	1kΩ8	R51;R52
1	2kΩ2	R73
3	2kΩ7	R40;R67;R68
1	3kΩ3	R4
2	3kΩ9	R21;R31
2	4kΩ7	R11;R15
7	10kΩ	R25;R33;R62-R65;R79
1	11kΩ 1%	R56
1	12kΩ	R66
3	15kΩ	R24;R49;R50
2	16kΩ 1%	R54;R58
3	18kΩ	R61;R77;R78
1	20kΩ 1%	R59
2	22kΩ	R55;R57
2	27kΩ	R10;R14
1	39kΩ	R36
5	47kΩ	R23;R39;R42;R43;R44
1	68kΩ	R34
6	100kΩ	R29;R38;R45;R60;R71;R72
1	150kΩ	R35
1	180kΩ	R37
2	1 MΩ	R27;R28
1	10kΩ preset H	P2
1	25kΩ preset H	P1

Capacitors:

1	1pF8	C2
10	10pF	C4-C7;C11-C14;C22;C23
1	33pF	C61
1	56pF	C74
2	100pF	C25;C26
1	120pF	C24
1	150pF	C27
1	220pF	C71
1	270pF	C62
1	470pF	C34
1	560pF	C72
1	680pF	C73
1	1nF	C33
2	1nF5	C46;C47
1	2nF2	C63
2	3nF3	C44;C45
5	4nF7	C1;C8;C9;C35;C64
1	10nF	C57
2	15nF	C54;C55
1	22nF	C56
2	33nF	C31;C53
4	47nF	C3;C15;C16;C60
8	100nF	C19;C20;C21;C37;C39;C40;C41;C68
4	220nF	C29;C36;C42;C69
1	330nF	C32
4	470nF	C10;C30;C48;C49
2	1μF solid	C65;C66
1	4μF7 25 V	C70
5	10μF 25 V radial	C28;C43;C50;C58;C59
1	10μF 63 V radial	C17
3	100μF 25 V radial	C38;C51;C52
1	100μF 30 V radial	C18
1	220μF 25 V	C67

Semiconductors:

1	BB204B	D1
1	1N4004	D2
2	BC550	T5;T6
2	BF199	T2;T3
1	BF324	T4
1	BFT66	T1
1	7815	IC5
1	LM317	IC4
1	TDA1576	IC1
1	TDA1578A	IC2
1	TDA3810	IC3
1	TL081	IC6

Inductors:

1	1mH	L1
2	39mH	L3;L4
1	1μH	L2

Miscellaneous:

2	214KCS-10115X (Toko)	FI1;FI2
1	10.7MHz quartz crystal	Q1
4	10.7MHz quartz crystal filter TQF2599 (Toyocom)	QF1-QF4
1	FM tuner FD12	TUN1
1	Heat-sink SK104/40mm	
1	Printed circuit board	920005-1

work. For this, we make use of the on-board quartz-controlled 10.7-MHz test oscillator, which can be enabled (for the adjustment only) by fitting jumper 'C'.

The demodulated MPX (multiplex) signal is superimposed on the AFC difference voltage. It consists of the mono signal (sum of L+R) and everything else contained in the FM baseband spectrum:

the 19-kHz pilot carrier for the demodulation of the stereo difference signal (L®) and the control of the mono/stereo indicator;

the two sidebands of the stereo difference signal, which is modulated on a (suppressed) 38-kHz carrier;

any special service signals in the baseband, like RDS at 57 kHz (suppressed carrier).

An RDS decoder is readily connected to pin 8 of the TDA1576, since this supplies the full baseband spectrum.

Stereo decoder

The stereo decoder, IC2, is driven from pin 8 of the demodulator via a phase shift compensation network that consists of R32, L1, C72-C73, P1 and C71. The channel separation may be optimized by adjusting the preset, P1. A channel separation of 40 dB is achieved with P1 set to the centre of its travel.

Preset P2 serves to set the centre frequency of PLL (phase locked loop) for the recovery of the 38 kHz subcarrier. When more than 3 V is applied to the MONO input of the TDA1578, the decoder switches from stereo to mono. Similarly, it is possible to control the mute function of the IC via a switching voltage applied to the MUTE terminal of the board. The mute function affords noise-free on and off switching of the audio output signal. It may be controlled manually, by the synthesizer, or by a signal strength measurement circuit.

The state of the stereo and mute circuits on board the TDA1578 is indicated by two LEDs connected to the respective open-collector outputs of the IC.

The de-emphasis is implemented in the feedback networks of the output amplifier, R49-C44 and R50-C55. Series resonance tuned circuits L3-C47 and L4-C46 are fitted at outputs of the stereo decoder to provide additional suppression of the 19-kHz pilot signal.

AF output amplifier

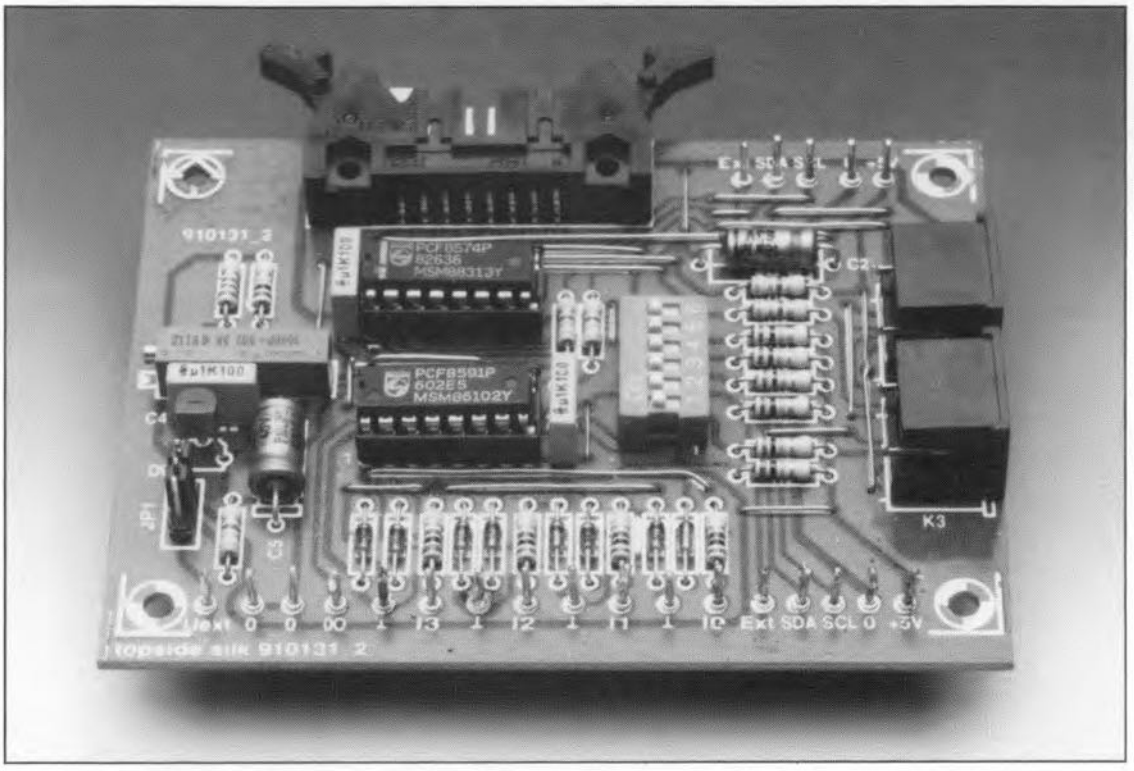
The audio output driver Type TDA3810 has three modes of operation: (1) normal AF amplifier; (2) stereo image widening by adding a 50% inverted version of one channel to the other; (3) pseudo stereo by applying frequency-dependent phase shift to a mono signal and splitting it into two. Mode selection is effected via inputs 'A' and 'B' on the tuner board.

The TDA3810 will normally be used as a straight amplifier with a noise level specification that is to CD player standards. The other two modes, image widening and pseudo stereo, are more fanciful, and not recommended for high-end use. The pseudo stereo mode, however, may be used occasionally to give an interesting 'touch' to pop music. Our advice is to try it out and see if you like the effect. If you don't, there is always the 'straight stereo' mode to return to.

The printed circuit board

Although the construction and adjustment of the tuner board are discussed in part 3 of this article, the track side copper layout and the component mounting plan are already given here (see Fig. 5). The board is single-sided, and easily completed as no 'difficult' RF construction is involved. The tuner is mounted vertically on solder pins. Note that the antenna cable is connected to two solder terminals on the board, i.e, not direct to the tuner. ❑

ADC/DAC AND I/O FOR I²C BUS



This article discusses a compact interface that allows PC users to communicate with I²C compatible ICs and circuits. The interface comprises an I/O port and a combined 8-bit analogue-to-digital and digital-to-analogue converter. Also, system software is described that brings life to the I²C PC insertion card described last month.

Design by J. Ruffell

AS promised last month, this article tackles the software necessary to control the I²C interface for PCs (Ref. 1). This device driver is basically an extension of the disk operating system (DOS) implemented on the PC, and contains all the routines necessary to write and read I²C codes to and from ICs connected to any I²C bus system. The device driver has been written to comply with the protocols drawn up by Philips for the I²C bus.

Device drivers are used at several levels in a PC. Examples of device drivers include 'software handles' for the screen, the printer, the RAM disk, and the keyboard, to mention but a few. There are basically two types of device driver: block drivers and character drivers. Block drivers are used for media such as disk drives, while character drivers are used for the screen, the keyboard and, in this case, the I²C bus. Any device driver is an extension of the DOS, and is invariably called via the DOS. According to the DOS specification, a device driver can contain up to 17 routines (i.e., not all of these need to be implemented). They are:

0* Driver initialisation
1 Media check
2 Build BIOS parameter block
3 I/O control read
4* Read
5 Non-destructive read
6 Input status
7 Erase input buffers
8* Write
9* Write and verify
10 Output status
11 Erase output buffers
12* I/O control write
13* Open device
14* Close device
15 Removable media
16* Output until busy

The routines marked with an asterisk are implemented in the present I²C device driver, which is written in machine language, and available on a diskette (along with the source file) supplied through our Readers Services. A full description of the operation of the device driver is beyond the scope of this article, and readers interested in the programming aspects are advised to print the source file for close analysis. Further information on device drivers for PCs, and machine code programming, may be found in the many books and other publications that have been written on these subjects.

MAIN SPECIFICATIONS

- Controlled via I²C bus
- 4 analogue inputs (256 steps)
- 1 analogue output (256 steps)
- 8 I/O lines (bidirectional)
- Up to 8 boards on one I²C bus
- Adjustable ADC/DAC reference voltage
- Complete with MSDOS compatible device driver
- Source code available in assembler, Pascal and C

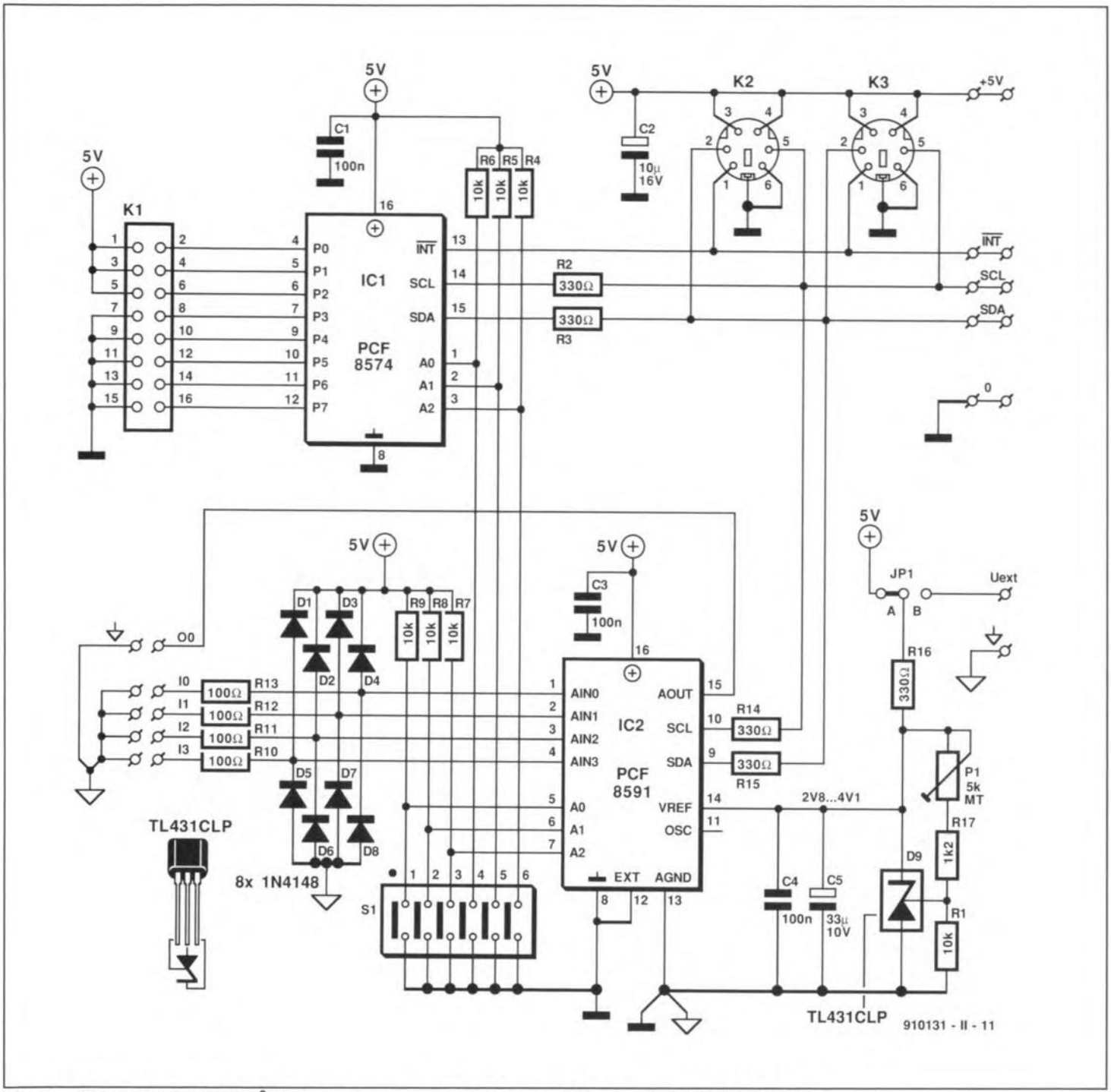


Fig. 1. Circuit diagram of the I²C extension card, which contains an I/O port and an 8-bit ADC/DAC.

Installation

The device driver disk contains the assembled file I2CDRIV.SYS, which may be placed in the root directory of the PC. Next, the CONFIG.SYS file has to modified by adding the line

device = I2CDRIV.SYS

You may type two parameters after 'I2CDRIV.SYS': B:xxxx and/or C:y, where

xxx is the base address of the I²C insertion card. This address is set to a value between 300_H and $3FE_H$ with the aid of DIP switches.

y is a code that selects the clock frequency, SCL, used on the I²C bus. The available clock frequencies deviate slightly from the those mentioned in the datasheets, because a clock of 7.16 MHz is used instead of the more usual 8 MHz. Parameter **y** can take the following values:

0: f_{SCL} = 81 kHz
1: f_{SCL} = 40 kHz
2: f_{SCL} = 9.8 kHz
3: f_{SCL} = 1.3 kHz

The default values for parameters B and C are 300_H and 9.8 kHz respectively.

When the PC is switched on or reset, it reads the new CONFIG.SYS file, and from then on recognizes all routines that support the I²C interface. That is when the real work can begin.

Useful for your own software experiments, the example programs on the diskette illustrate the use of the I²C driver routines in assembler as well as in the higher programming languages C and Pascal.

Hardware

The circuit diagram of the ADC/DAC and I/O card for the I²C bus is shown in Fig. 1. The main components in the circuit are the PCF8574 I/O port and the PCF8591 ADC/DAC. These I²C compatible building blocks prove that interface circuits with I²C control can be kept very simple indeed. The 8-bit I/O port is simplicity itself. Its eight I/O lines may be linked to external digital devices via connector K1. Address lines A0, A1 and A2 are connected to the positive supply line via pull-up resistors. Three switches in DIP switch block S1 are used to set the programmable part of the I/O address of the IC. The DIP switch allows up to eight PCF8574s

to be used simultaneously via the I²C bus.

As with all I²C devices, the addresses are partly fixed in the ICs. The two ICs on the present card are addressed as follows:

PCF8574: 0100 A2 A1 A0 R/$\overline{W}$
PCF8591: 1001 A2 A1 A0 R/$\overline{W}$

In both cases, the first four bits cannot be changed by the user. The next three bits can be set on the DIP switches, and the last bit selects between reading and writing of data. Read operations are enabled when R/$\overline{W}$ is '1', write operations when R/$\overline{W}$ is '0'. As regards the device driver routines found on the diskette, it is assumed that all DIP switches are closed, which means that the I/O port and the ADC/DAC are located at the address pairs 40_H-41_H and 90_H-91_H respectively. If other address pairs are set on the switches, the software requires to be changed accordingly. Given that the example files have a copious amount of comment, this should not cause problems.

The quasi-bidirectional I/O port Type PCF8574, of which the block diagram is shown in Fig. 2, has only one read/write register. Depending on the application, this device allows its output lines to be used as input lines. The output lines have a current sink and source specification of 25 mA and 0.4 mA respectively. If a port line is to be used as an input, it is first made logic '1'. Next, the level of the 'output line' is read back to see if it is still at '1'. If not, it is apparently pulled low (i.e., held at '0') by an external device. Thus, the low level supplied by an external device to the port line overrides the previously programmed '1', and is so recognized by the software. The open-drain outputs allow this to be done with impunity.

The circuit around the PCF8591 ADC/DAC is far more complex than that around the I/O IC. The analogue inputs of the ADC/DAC are protected against overvoltages by resistor-diode combinations R10-R13 and D1-D8. Here, too, the three address inputs are connected to DIP switches that enable the variable part of the address to be set by the user. The external voltage reference is set up around precision zener diode D9, a TLC431CLP. Resistors R1, R16, R17 and P1 are used to set a reference voltage between 2.8 V and 4.1 V. The user may set the value in this range required for the desired A-D/D-A step size. One step corresponds to $U_{ref}/256$. Capacitors C4 and C5 serve to suppress noise on the reference voltage. Jumper JP1 allows the ADC/DAC to be fed with an external reference voltage, which may be useful in certain cases when there is a danger of accurate measurements being spoilt by noise on the 5-V supply. For most applications, however, an external reference will not be required.

Figure 3 shows the block diagram of the I²C compatible ADC/DAC. Because it has many more possibilities, the PCF8591 is more complex to control than the PCF8574. Apart from data bytes, the converter IC requires a control byte to determine a number of settings as shown in Fig. 4. The highest nibble in the control byte determines the configuration of the analogue inputs (either two differential inputs, or four ordinary inputs), and in addition switches the analogue output on and off. The low nibble selects one of four A-D inputs, and may be used to enable the auto-increment flag.

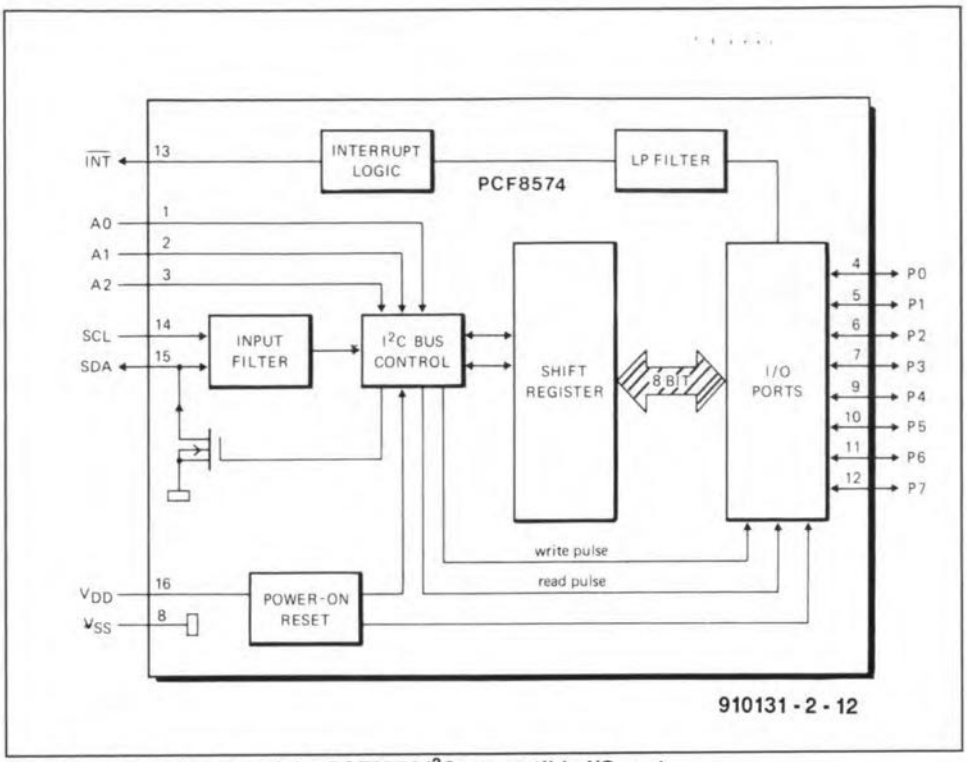


Fig. 2. Block diagram of the PCF8574 I²C compatible I/O port.

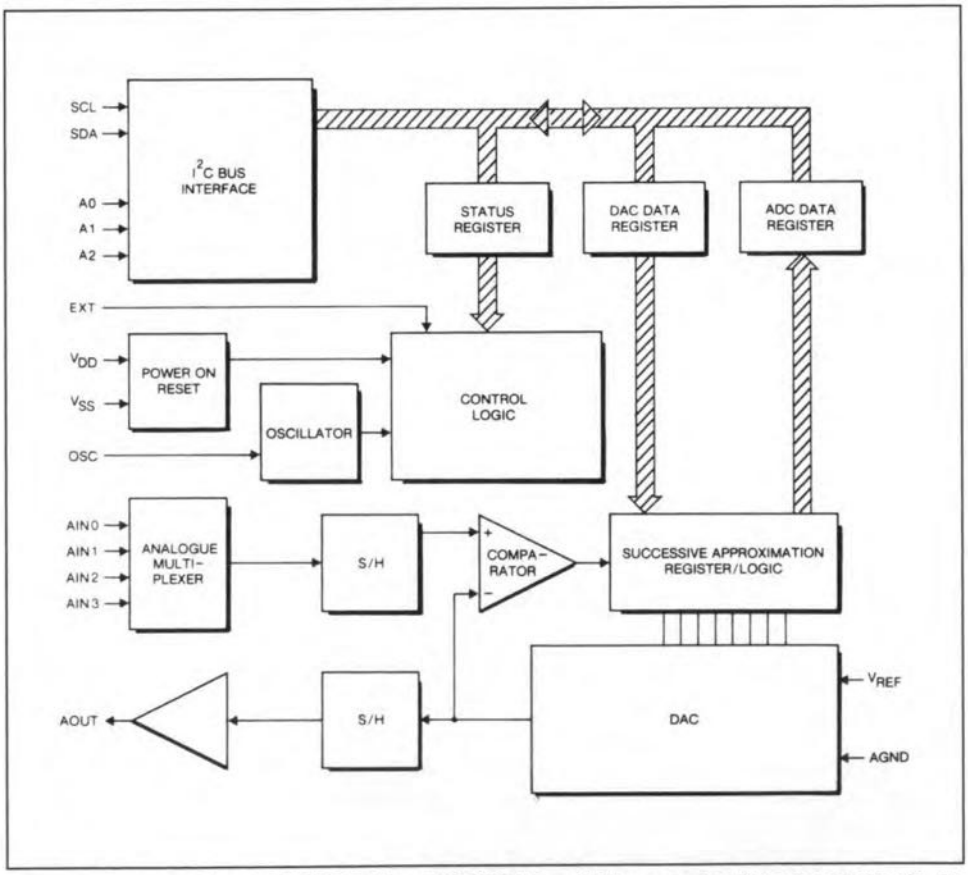


Fig. 3. The combined ADC/DAC Type PCF8591 is a fairly complex integrated circuit. An external voltage reference allows the conversion step size of the ADC and the DAC to be set as required.

The third byte, sent to the IC after the address byte and the control byte, is stored in the DAC register. Next, the previously stored value is converted into an analogue voltage that appears at output of the DAC. The output voltage increment equals $U_{ref}/256$. This means that a value of '00' results in 0 V at the output, and '255' in an output voltage of $255 \times U_{ref}/256$.

The reading back of ADC output values is performed in a slightly different manner. An A-D conversion cycle is started on the positive-going edge of the acknowledge pulse, which is returned to the master device

after the converter has been set to 'read' mode with the aid of a read command. The IC performs another A-to-D conversion cycle while it sends the data resulting from the previous conversion. At the start of the conversion, the voltage level at the selected input is sampled and subsequently converted into an 8-bit binary code. Input voltages supplied by a differential input are converted into an 8-bit two's complement code. The result is stored in the data register of the ADC, from which it can be transmitted. When the auto-increment flag is actuated, the next input is selected. In this manner, all inputs are selected in succession.

Construction

The ADC/DAC and I/O extension is easy to build on the printed circuit board of which the copper side layout and the component mounting plan are shown in Fig. 6. The 6-way miniature DIN-style connectors enable the extension card to be readily connected to the I²C interface in the PC. In principle, only one of the two mini-DIN sockets needs to be fitted on the board. The second socket is required only if further I²C boards are to be connected to form a chain. If a number of I²C extensions are fitted into a common enclosure, there is, of course, no objection against omitting the connectors, and using permanent wiring instead. The +5-V, ground, SCL, SDA and $\overline{INT}$ lines of the units are then connected from board to board.

The pinning of connector K1 is such that it can be linked direct to the 'Measurement amplifier' described last month (Ref. 2). All that is required to implement computer control on this amplifier is a short length of flat cable to link it to the ADC on the present board. By studying the source code of the test program 'ADIO', you will notice that the combination of the ADC and the measurement amplifier is readily turned into an autoranging measurement system.

The reference voltage is set to the required value by adjusting preset P1 and measuring the voltage across C5 with a digital multimeter. Since the program 'ADIO' on the diskette is based on a reference voltage of 4.0 V, it is advisable to set this value initially. Later, other values may be chosen, provided the relevant statements in the program are changed accordingly.

That completes the construction and adjustment of the I²C extension card, which is then ready to be tested. Testing is done in a 'hands-on' way with the aid of a well-documented test program, of which a Turbo Pascal and a C version is available on the diskette. Both versions of the test program cycle through a number of routines, including one that reads the levels at I/O port lines b4 to b7, and copies these to outputs b0 to b3. To run the test, force port lines b4 to b7 logic high with the aid of 10-kΩ pull-up resistors. Connect push-buttons that switch to ground to the same lines. Connect four LEDs between the b0 to b3 output lines and +5 V via 330-Ω series resistors. Run the test program, and check that one of the LEDs lights when the

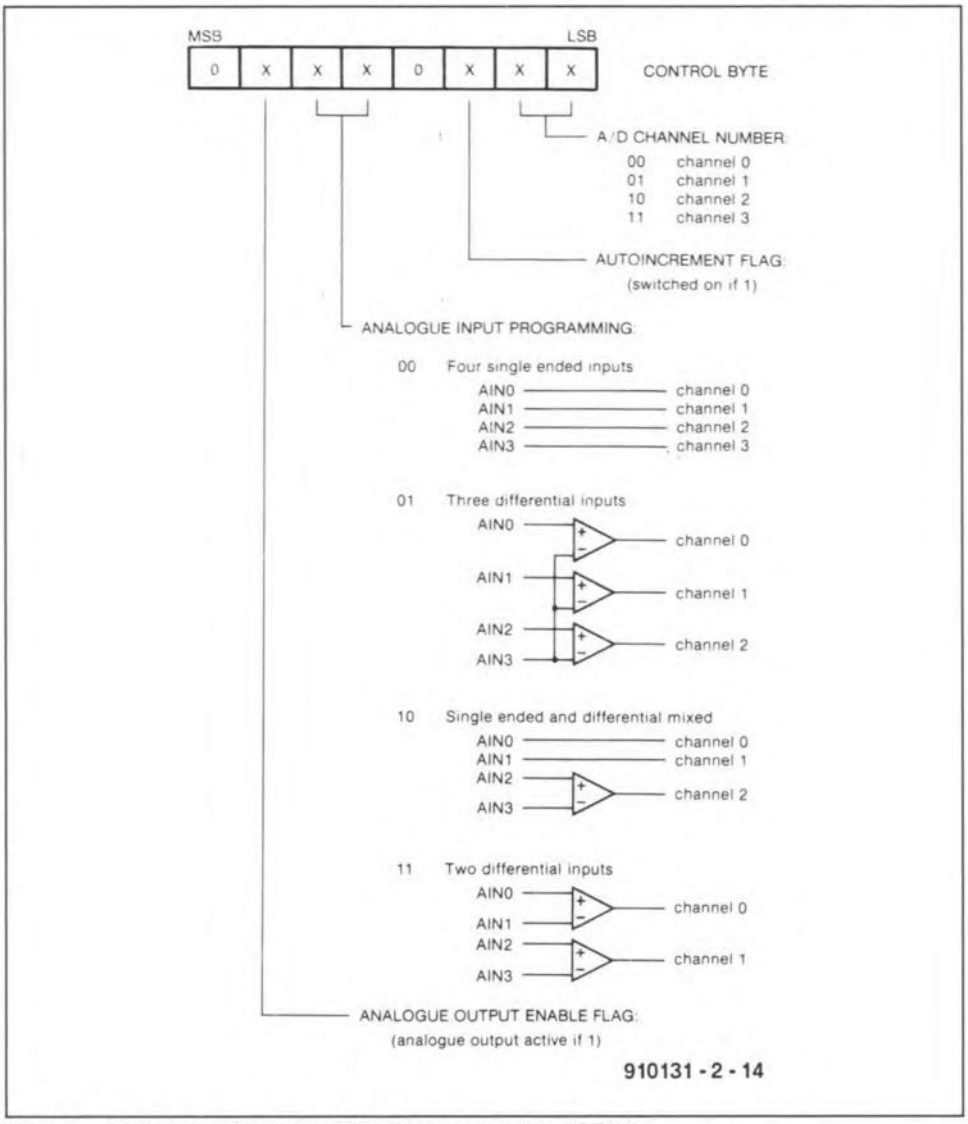


Fig. 4. Bit functions in the control byte sent to the PCF8591.

```
begin (* TestADDA *)
  Ctrl:=GetControlByte(1);          {-Load control byte with option# 1}
  Address(ADA_Addr);                {-Because the R/W_ bit (= LSB ADA_Addr)
                                      equals zero, the PCF8591 enters the
                                      write-mode. Therefore, the next trans-
                                      mitted byte is interpreted as a
                                      control byte,}
  write(bus,Ctrl);                  {-Transmit control byte.}
  with AD do                        {-The next bytes sent to the PCF8591
                                      would be stored in the DAC register.
                                      But at this point, we switch to
                                      read-mode...}
    read(Bus,Dummy,Data[0],Data[1],Data[2],Data[3]); {-I2CDRIV.SYS now
                                      generates a repeated start (same
                                      address, but with R/W_ = 1) and reads
                                      five AD-conversion bytes from the
                                      PCF8591. This is done by using the
                                      channel auto-increment function of
                                      the chip. The first read byte (Dummy)
                                      is the convertion result code of the
                                      previous cycle! We are not interested
                                      in that sample, so it is thrown away.}
  write(bus,Ctrl,AD.Data[Chan3]);   {-I2CDRIV.SYS generates a repeated
                                      start condition; same address, but
                                      with R/W_ = 0. Thus, the PCF8591 is
                                      in write-mode again and expects a
                                      control byte and one or more data-
                                      bytes. All databytes are stored in
                                      the DAC-register, but the analogue
                                      output voltage is always calculated
                                      from the previous DAC-register
                                      contents.}
  for Channel:=Chan0 to Chan3 do
    ShowVoltage(Channel,AD.Data[Channel]);
  ShowVoltage(4,AD.Data[Chan3]);
end;  (* TestADDA *)
```

Fig. 5. Extract from the I²C device driver listing. This source code is written in Turbo Pascal.

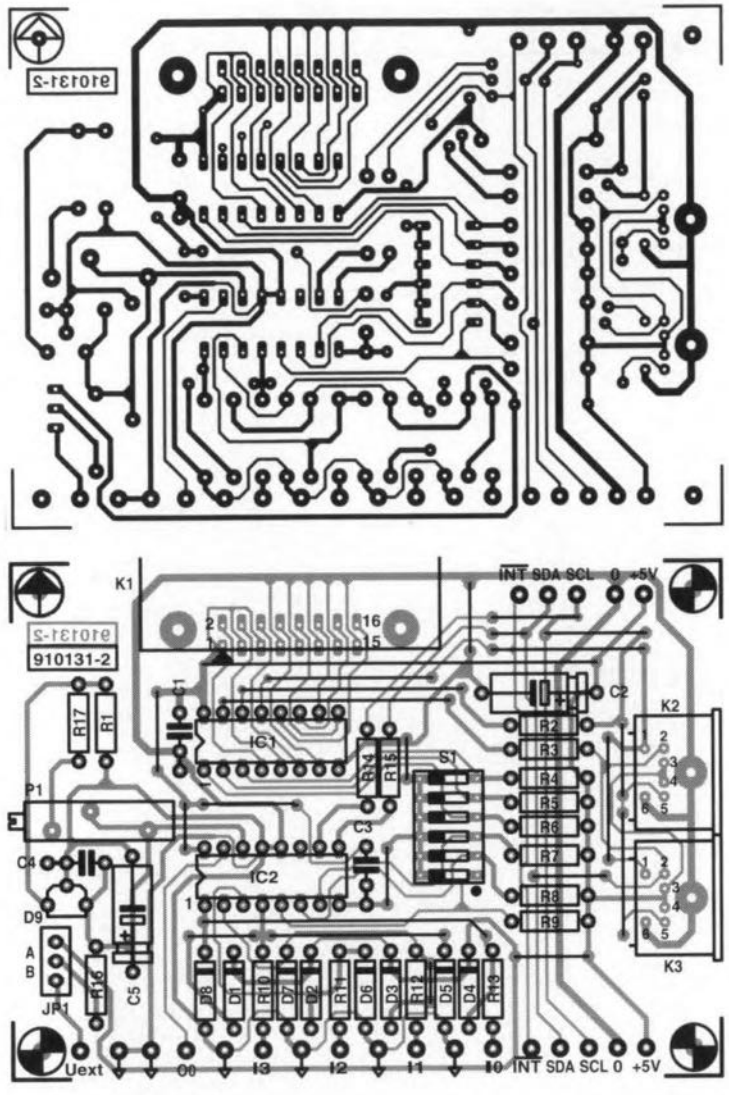


Fig. 6. Track side layout and component mounting plan of the PCB designed for the I²C extension card. Six-way mini-DIN connectors are used to connect I²C boards to the I²C interface fitted in the PC.

COMPONENTS LIST

Resistors:

7	10kΩ	R1;R4-R9
5	330Ω	R2;R3;R14; R15;R16
4	100Ω	R10;R13
1	1kΩ2	R17
1	5kΩ multiturn preset	P1

Capacitors:

3	100nF	C1;C3;C4
1	10µF 16V	C2
1	33µF 10V	C5

Semiconductors:

8	1N4148	D1-D8
1	TL431CLP*	D9
1	PCF8574*	IC1
1	PCF8591*	IC2

Miscellaneous:

1	16-way header, angled, with side latches	K1
2	6-way mini-DIN socket for PCB mounting	K2;K3
2	6-way mini-DIN plug	
2m	(approx.) 6-wire cable	
1	6-way DIP switch	S1
1	Printed circuit board	910131-2
1	Control software on disk (MSDOS)	ESS1671

* Suggested supplier: C-I Electronics, P.O. Box 22089, 6360 AB Nuth, Holland. Fax: +31 45 241877.

corresponding push-button is pressed.

The ADC/DAC is tested similarly. The program reads the voltage levels at the analogue inputs I0, I1, I2 and I3, and puts the level of I3 on output O0.

If the circuit passes the above tests, it is ready for use with your own applications. ■

References:

1. "I²C interface for PCs", *Elektor Electronics* January 1992.

2. "Measurement amplifier", *Elektor Electronics* January 1992.

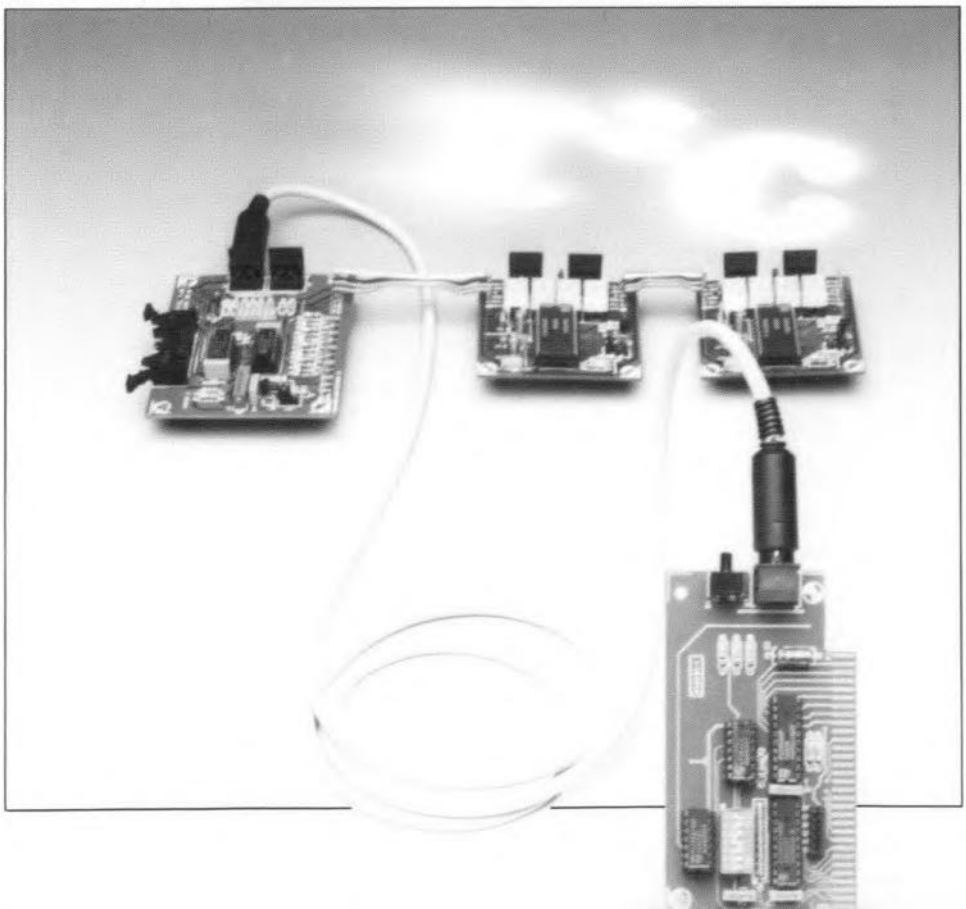
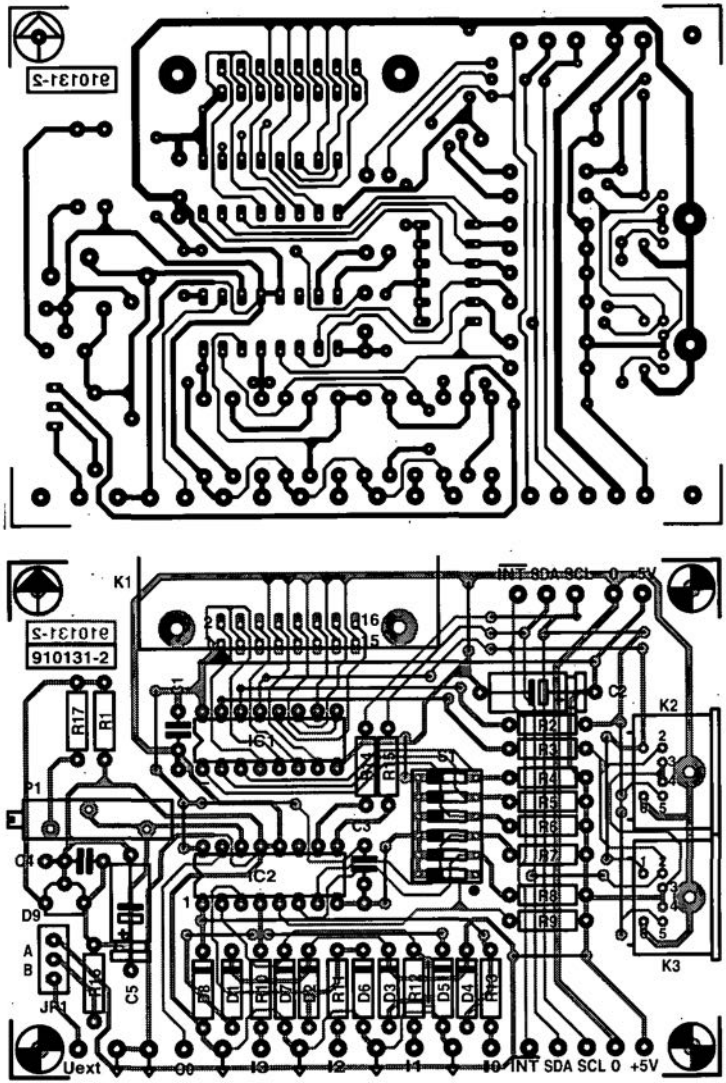


Fig. 7. This demonstration set-up shows how different modules can work with a single interface. The display driver shown will be discussed in a future publication.



COMPONENTS LIST

Resistors:

7	10kΩ	R1;R4-R9
5	330Ω	R2;R3;R14; R15;R16
4	100Ω	R10;R13
1	1kΩ2	R17
1	5kΩ multiturn preset	P1

Capacitors:

3	100nF	C1;C3;C4
1	10µF 16V	C2
1	33µF 10V	C5

Semiconductors:

8	1N4148	D1-D8
1	TL431CLP*	D9
1	PCF8574*	IC1
1	PCF8591*	IC2

Miscellaneous:

1	16-way header, angled, with side latches	K1
2	6-way mini-DIN socket for PCB mounting	K2;K3
2	6-way mini-DIN plug	
2m (approx.) 6-wire cable		
1	6-way DIP switch	S1
1	Printed circuit board	910131-2
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corresponding push-button is pressed.

The ADC/DAC is tested similarly. The program reads the voltage levels at the anal-

8751 EMULATOR

This article describes hardware and software that together form a powerful development system for the popular 8751 microcontroller from Intel.

Design by O. Bailleux

THE microcontroller emulator described here allows you to develop and debug 8751 application circuits with a minimum of effort. The emulator is has two main connections: one to the serial port of a PC, and another to the IC socket reserved for the 8751 in the target system. The combination of the PC, the software that runs on it, and the emulator allows you to

- download, modify, and upload 8751 programs;
- erase and program a 8751;
- put breakpoints in programs;
- display register and memory contents;
- run programs in single step mode;
- modify the contents of certain registers.

Clearly, this makes the emulator a powerful and indispensable tool for all of you who, at a certain stage, are 'confronted' with a 8751 application.

General remarks

This article does not aim at discussing or even introducing all the hardware and software aspects of the 8751 microcontroller, since this field is covered adequately by the *Microcontroller Handbook* from Intel. As regards practical programming of the 8751, the '8051/8032 assembler course' published in this magazine will be very useful to follow (the 8032, 8051 and 8751 are all devices from Intel's MCS52 family of microcontrollers).

None the less, the file READ.ME on the diskette supplied in relation to the present emulator contains some basic information on the 8751.

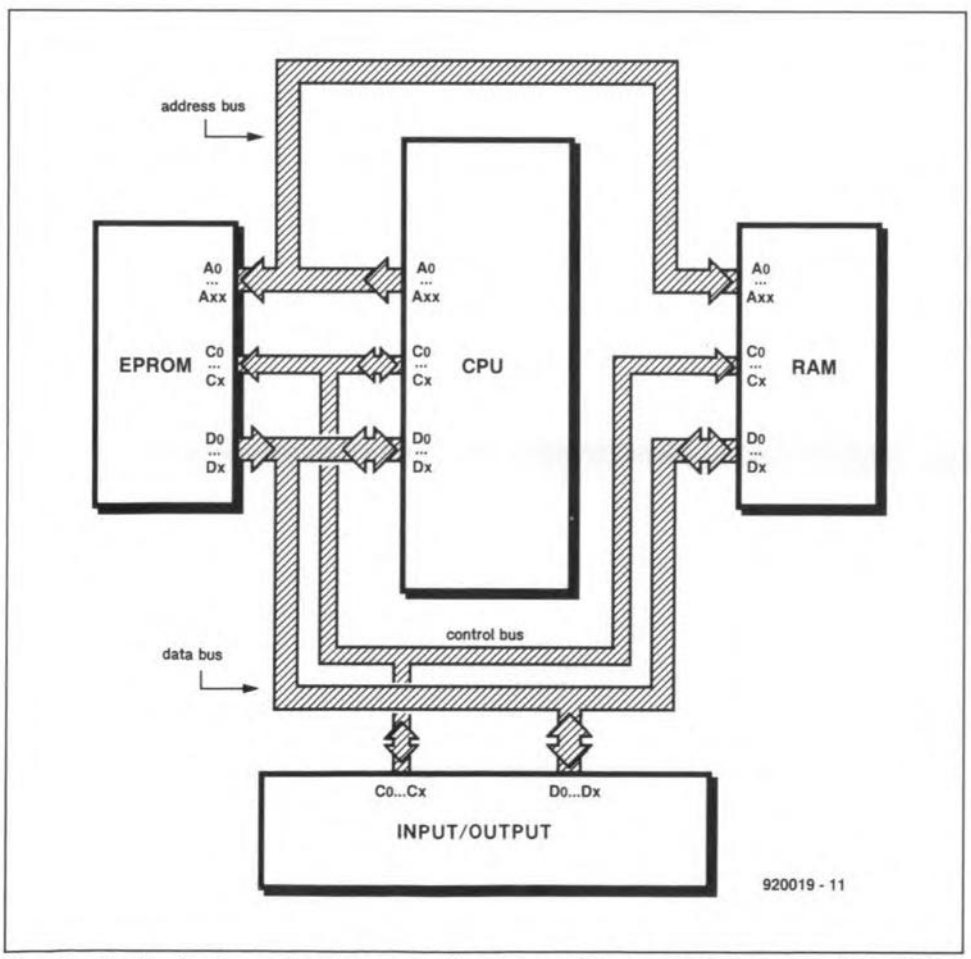


Fig. 1. Basic structure of a microcontroller system. ICs are available that combine all the functions shown here.

MAIN CHARACTERISTICS

- **Real-time 8751 emulator**
- **Clock frequency: 8 MHz**
- **All I/O ports available**
- **All internal interrupt sources available**
- **Powered by target circuit**
- **9,600 baud serial link to PC**
- **Breakpoint analysis and single-step mode**
- **Internal register and internal RAM contents displayed and available for editing**
- **Symbolic assembler for 8751**
- **Full-screen editor with error location facility**
- **Binary or Intel-hex output files**
- **Hard copy of formatted source program**

Limitations:

- **Monochip mode only (internal program memory, no external data memory)**
- **I/O bits P3.6 and P3.7 reserved for system**
- **Register 0 banks only**
- **System software uses 12 stack locations**
- **Masked interrupts during breakpoint processing**

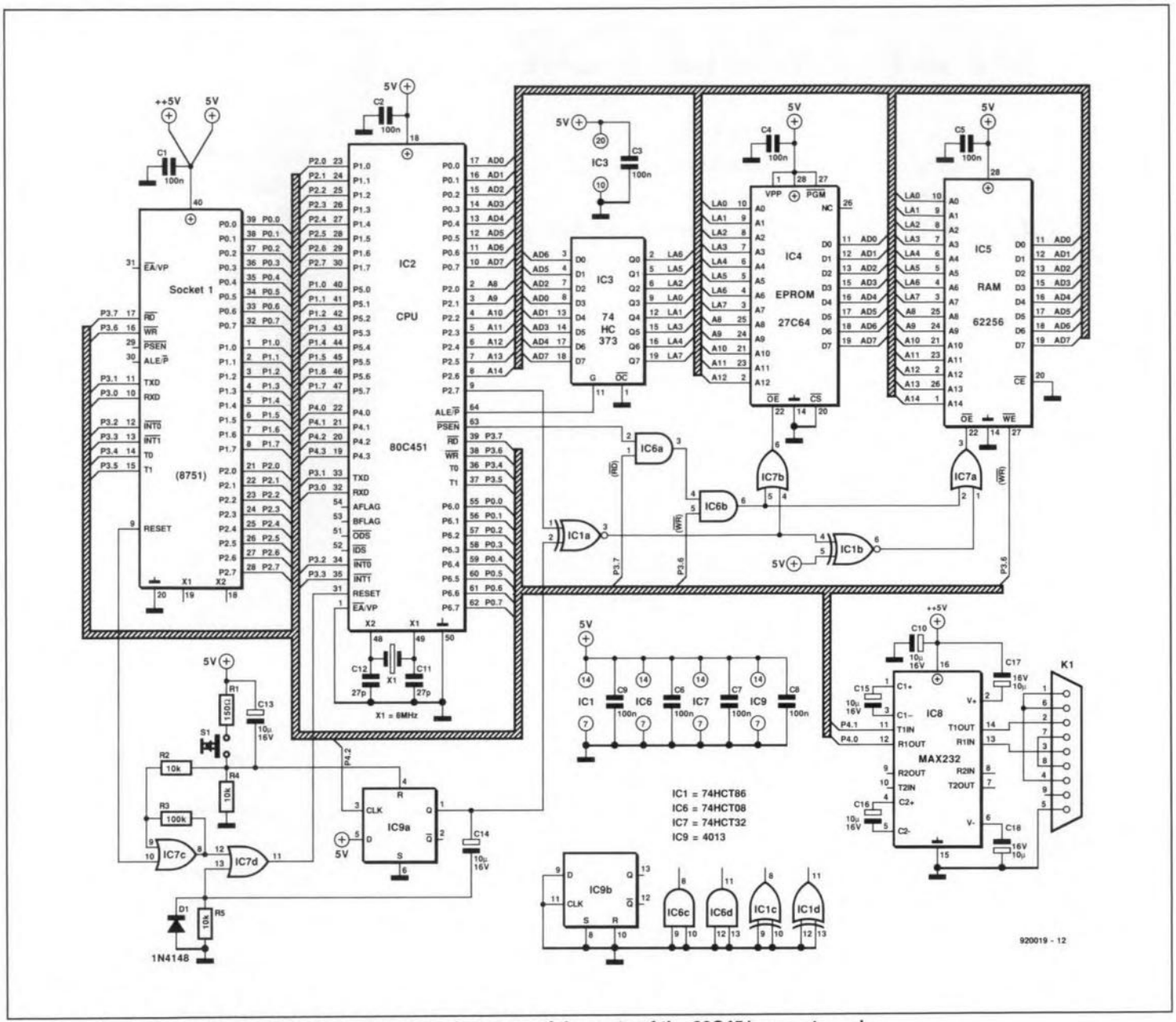


Fig. 2. Circuit diagram of the 8751 emulator. Note that some of the ports of the 80C451 are not used.

The 8751 is a microcontroller that integrates:

- an 8-bit microprocessor;
- a RAM of 128 bytes;
- 4 8-bit parallel I/O ports;
- 1 serial communication port;
- 2 programmable timers;
- 2 external interrupt lines.

The 8-bit (256-byte) addressable range of the 8751 is divided into two parts:

- user RAM between 00H and 7FH: this contains registers R0 to R7 (00H to 07H), and the system stack. A subrange of 16 addresses is bit-addressable.
- control register range between 80H and FFH: this range can be accessed by direct addressing only, and contains the I/O ports, the timer control registers, and a number of other special functions.

Principle of operation

As illustrated by Fig. 1, a microprocessor system generally consists of microprocessor, a program memory, a data memory, and input/output devices. The elements that form the system are interconnected by an address bus, a data bus and a control bus. Since the 8751 microcontroller works in 'monochip' mode, it has all of the above elements internally. Only the four 8-bit ports can be accessed by external devices. Emulating a 8751 thus calls for a device capable of:

- running object code from RAM instead of ROM—this is necessary to allow changes to the program to be made rapidly;
- providing four input/output ports as well as the basic hardware environment of the 8751;
- providing an instruction set that is compatible with that of the 8751.

The Type 80C451 meets all these requirements beautifully, and is used here to emulate a 8751. The pinning of this device is given in Fig. 3.

The emulator based on the 80C451 consists basically of:

- an EPROM with a start-up program;
- a 32-KByte RAM to hold the system routines and the user program being developed;
- a memory switching device with two states:
  start state: the EPROM is located at address 000H, and the RAM at address 8000H
  execute state: the RAM is at 0000H and the EPROM at 8000H;
- a TTL compatible (pseudo-RS232) serial interface for the connection the PC.

The initialization procedure consists of the following steps:

1. Initialization (reset), and start phase. EPROM-based program executed from address 0000H.

2. A routine in the start-up EPROM that sends the system program code from the PC to the emulator RAM. This is done via the serial link, and with the aid a simplified

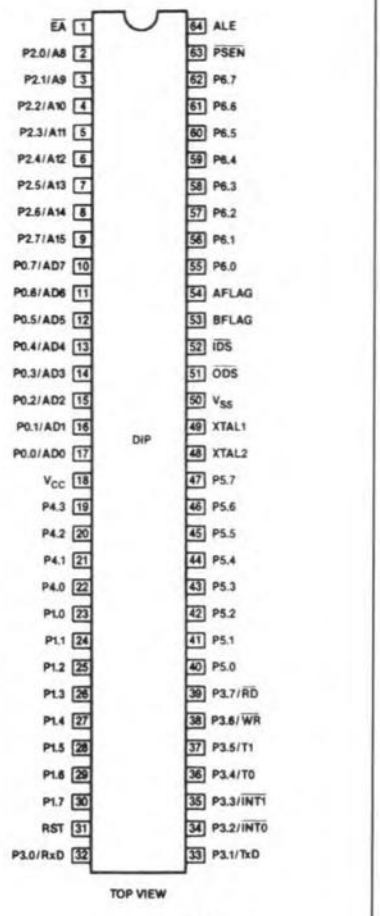


Fig. 3. Pinning of the 80C451 microcontroller (courtesy Signetics).

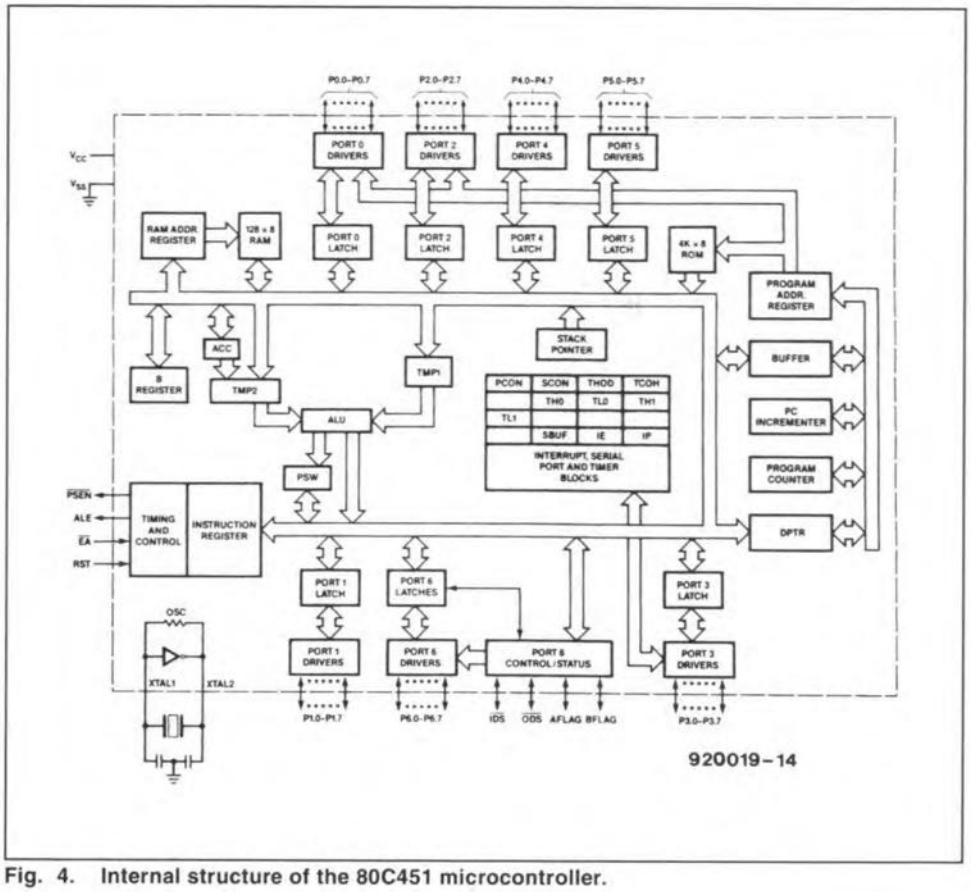


Fig. 4. Internal structure of the 80C451 microcontroller.

transfer protocol.

3. A routine in the start-up EPROM actuates a (reserved) I/O bit, which causes the system to switch to switch to the 'run' (program execution) stage, and in addition generates a reset.

4. The system program starts at address 0000H, it duplicates itself, and runs again from the upper part of the RAM at 7800H. From that location, it arranges the communication with the PC with the aid of a data transfer routine that allows the PC to

- issue a software reset to the microcontroller;
- read the emulator RAM;
- modify the emulator RAM;
- modify the stack pointer;
- upload a new user program;
- start or continue the execution of a user program.

5. The program that runs on the PC arranges the control of the emulator. Initially, it sends the user program object code to the emulator for the purpose of testing. This program will contain at least one breakpoint, which calls up a subroutine in the system software that stops the program execution.

6. The user program is executed until a breakpoint is encountered. At that location, the system software copies the current contents of the registers and the internal RAM of the 8751 into a buffer formed by the external RAM of the emulator, at 7000H. Next, the remote control subroutine is called.

7. The system software switches to the external emulator RAM, and causes the execution of the user program to continue, until the next breakpoint is encountered. At this stage, it is not possible to re-initialize the 8751 via the PC, or run a new user program.

8. The contents of the buffer starting at 7000H (which may have been modified in the mean time by the control program) are reloaded into the internal RAM and the registers, and the breakpoint routine is ended. The user program is continued up to the next breakpoint.

The key of the system is formed by the remote control routine, which enables the control software to modify the user program and the contents of the registers in the 8751. This function makes it possible to set breakpoints (temporarily), which are particularly useful in single-step mode.

Software

The software for the emulator is supplied on a 5¼-inch 360 KByte MSDOS formatted diskette, and consists of the following files:

DEV.EXE	programming environment
CONFIG.EMU	configuration file
SYS8751.C51	initialization file
SYS8751.A51	source code of initialization file
READ.ME	additional information

The user or the control program can access the emulator only while a static or dynamic breakpoint is being processed. The location of a breakpoint is determined by the user by inserting it in the source code. The control program calculates the corresponding address, saves the three bytes of opcode found there, and replaces them with an instruction that calls up the breakpoint handler. After a number of manipulations, the initial conditions are restored, and we can progress to the next breakpoint.

In single-step mode, the control program, while executing the breakpoint routine, automatically places a dynamic breakpoint after the next instruction. In single-step mode you can see exactly what happens to the register contents as the program evolves. A powerful debugging aid!

Hardware

At the heart of the emulator circuit (Fig. 2) is the Type SC80C451 microcontroller from Signetics, the North-American branch of Philips Components. Its internal structure is given in Fig. 4. By taking a close look at the block diagram, it becomes clear that the 80C451 is an extended version of the 80C51, with three additional I/O ports (which gives a total of six), and four additional I/O control lines.

The 80C451 has no internal ROM, and fetches its instructions from an external ROM or EPROM. The microcontroller offers 128 bytes of RAM, and the DIP version used here has no fewer than six 8-bit ports and one 4-bit port. The 80C451 is capable of address-

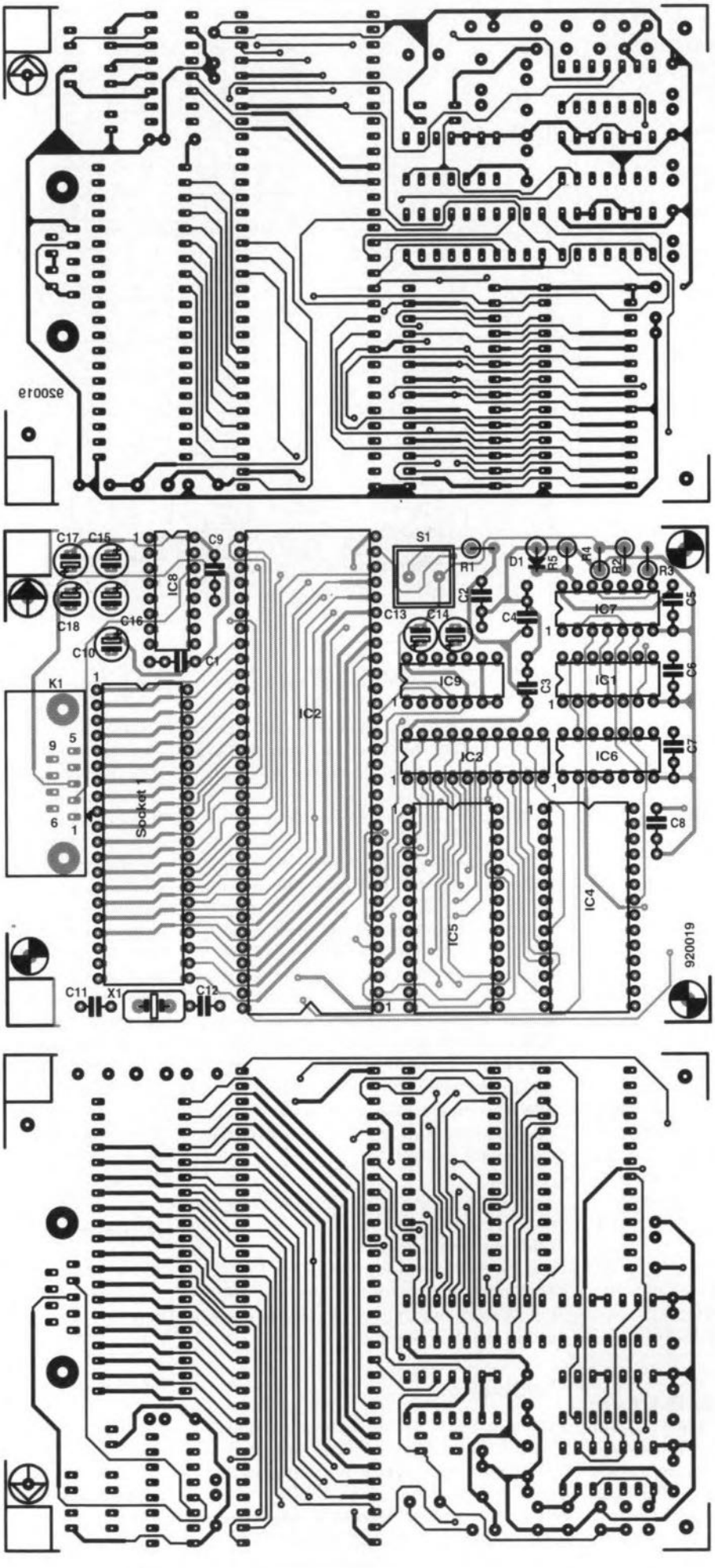


Fig. 5. Track layouts (component side and solder side) and component overlay of the double-sided, through-plated printed circuit board.

COMPONENTS LIST

Resistors:

1	150Ω	R1
3	10kΩ	R2;R4;R5
1	100kΩ	R3

Capacitors:

9	100nF	C1-C9
7	10µF 16V radial	C10;C13-C18
2	27pF	C11;C12

Semiconductors:

1	1N4148	D1
1	74HCT86	IC1
1	SC80C451CCN64 (Signetics)	IC2
1	74HC373	IC3
1	27C64 (ESS6051)	IC4
1	62256	IC5
1	74HCT08	IC6
1	74HCT32	IC7
1	MAX232 (Maxim)	IC8
1	4013	IC9

Miscellaneous:

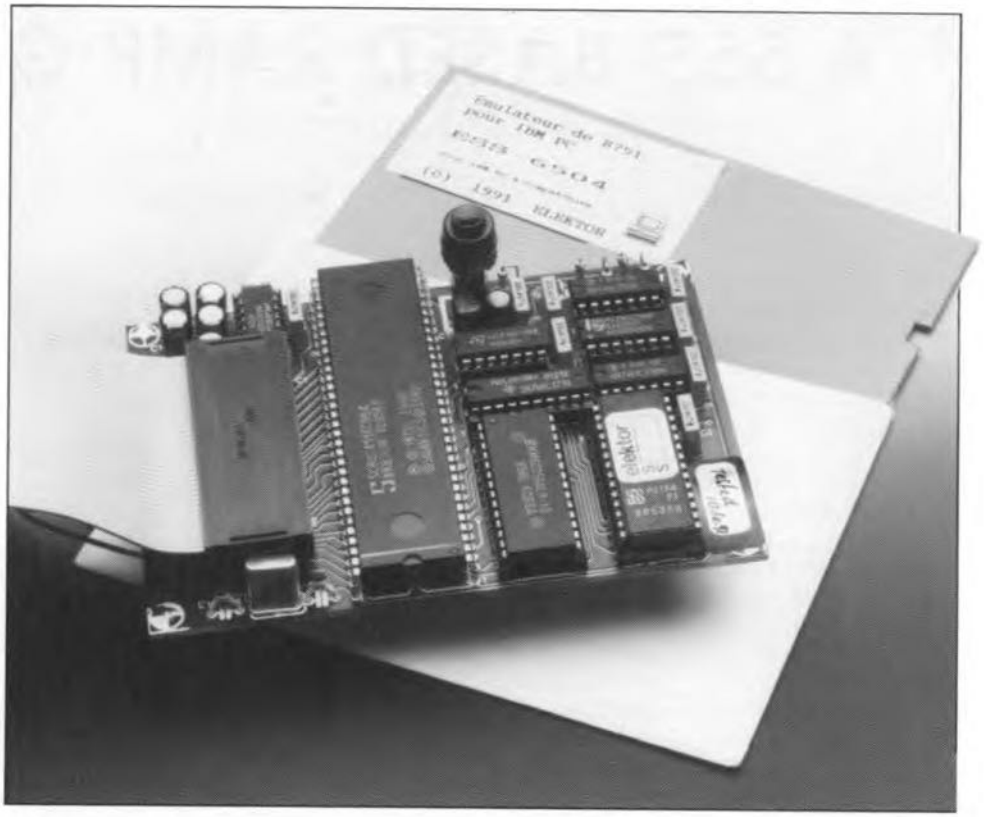
1	9-way female sub-D connector of PCB mounting	K1
1	push-button n.o.	S1
1	8MHz quartz crystal	X1
1	64-pin strip to make IC socket	
1	40-way IC socket with turned pins	H8
2	40-way IDC style DIP header	
1	length of 40-way flatcable	
1	enclosure; approx. dimensions: 92×146×28mm.	
1	printed circuit board	920019
1	control program on disk	ESS6051

ing 64 Kbytes of ROM, and an equal amount of RAM. The current consumption of the device is only about 24 mA at a supply voltage of 5 V and a clock frequency of 12 MHz, 3 mA in stand-by mode, and about 50 µA in the power-down ('sleep') mode.

The mask-programmable ROM version of the 80C451, the SC83C451, has 4 KBytes of ROM. Both the 80C451 and the SC83C451 have two 16-bit timers/counters. Their interrupt structure allows two priority levels to be implemented.

The presence of a serial I/O port in the 80C451 allows a UART (universal asynchronous receiver/transmitter) with true duplex operation to be realized quite easily. Alternatively, the serial I/O port may be used to extend the functions of the I/O lines, or to set up an inter-processor communication system.

The stand-by and the power-down modes can be entered via software. In stand-by mode, the CPU proper is halted, while the RAM, the timers, the serial port and the interrupt system continue to function. In the power-down mode, the clock oscillator is disabled, which causes all functions to be switched off, but the RAM contents to be retained.



Construction

The availability of a ready-made, through-plated printed circuit board (Fig. 5) makes the construction of the 8751 emulator relatively simple. A number of passive components are fitted upright. Due attention should be paid to the orientation of the ICs on the board, since they are not all mounted with the same direction. Naturally, the same goes for the orientation of the electrolytic capacitors and the diode.

The push-button, S1, may be fitted on to the enclosure, and is connected to the appropriate pins on the board.

The SC80C451 is best fitted into a socket made from two 32-pin strips. The RAM and the EPROM are also fitted in IC sockets.

SOCKET1 is best made from a good quality 40-pin IC socket. The connection to the 8751 socket in the target system is then readily made via a short length of flatcable fitted with a 40-way IDC-style DIP header at either end. Unfortunately, the pins of these DIP headers are pretty fragile, so take care not to break one, or the whole header is useless.

The completed printed circuit board is built into a suitable enclosure. A slot is cut in one of the sides to allow the 40-way flatcable to pass.

Practical use

Initially, the application (target) circuit and the PC are switched off. Note that the emulator is normally powered by the target circuit. Connect COM1: or COM2: of the PC to the emulator via an RS232 cable (the serial port selection is made in the file CONFIG.EMU as discussed below).

Do not connect the application circuit as yet. Connect a 5-V supply to the emulator. The + goes to pin 40 (+), and the – to pins 9 and pin 20 of the DIL socket on the emulator board. Next, run the program DEV.EXE on the PC, and check that the error message "Emulator not connected -- PRESS ANY KEY TO CONTINUE" does not appear.

At this stage, it should be possible to emulate the example program (see the syntax requirements mentioned in READ.ME), without the need of inserting the DIP plug into the 8751 socket in the target system. If this works, remove the temporary 5-V supply connections, and plug the 40-way DIP header into the socket on the emulator board. Insert the DIP header at the other end of the cable into the 8751 socket on your target system board. Power up the application before switching on the PC.

Programs may be edited and assembled even when the emulator is not connected or powered. The configuration file, CONFIG.EMU, contains only two characters. The first is an M (for the monochrome Hercules video adapter) or a C (for the colour video adapters CGA, EGA and VGA). The second character selects the serial port, and is either a 1 for COM1:, or a 2 for COM2:. If necessary, edit the configuration file using any ASCII compatible word processor. On the disk supplied through the Readers Services, the configuration is set to colour and COM1:.

The main program, DEV.EXE, is menu-driven, and uses the arrow keys to make selections. If you have the emulator powered up and connected to the target system at this stage, press switch S1 before running DEV.EXE.

Finally, READ.ME contains more information on the operation of the serial data link between the PC and the emulator. ■

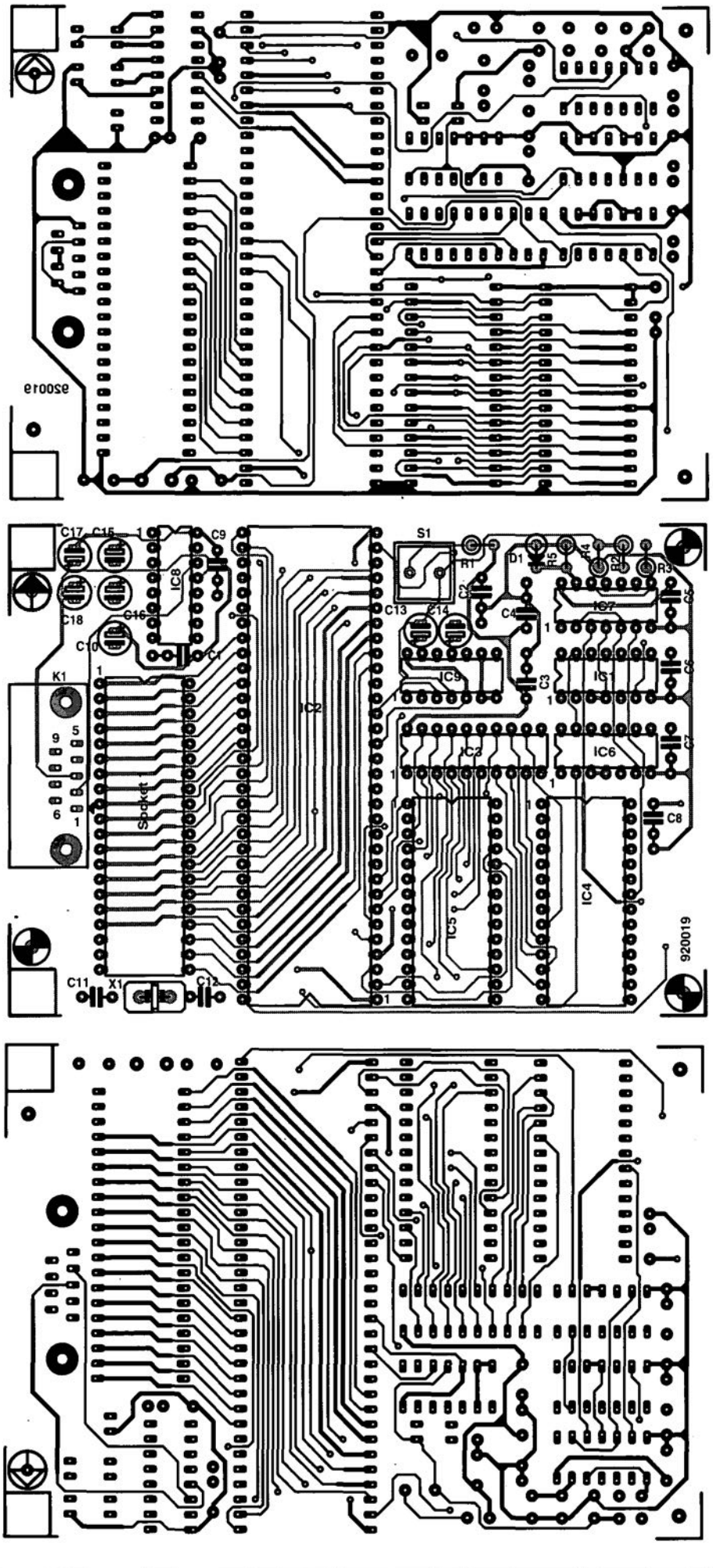


Fig. 5. Track layouts (component side and solder side) and component overlay of the double-sided, through-plated printed circuit board.

Mains (power line) voltages are not listed in the articles. It is assumed that our readers know what voltage is standard in their part of the world.

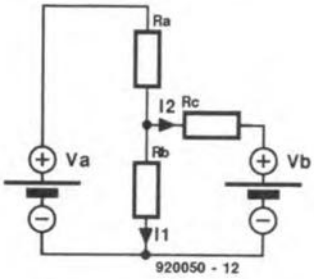
Readers in countries that use 60 Hz supplies, should note that our circuits are usually designed for 50 Hz. This will not normally cause problems, although if the mains frequency is used for synchronization, some modification may be required.

The international letter symbol '*U*' is used for voltage instead of the ambiguous '*V*'. The letter V is reserved for 'volts'.

CORRECTIONS

Plant warmer (June 1992)

Resistor R_c was omitted from Fig. 2. The correct diagram is shown below.



Inductance-capacitance meter (March 1992)

The value of R_{16} and R_{17} should be 39 Ω, not 30 Ω as shown in the parts list.

8751 Emulator (March 1992)

The features list in the first column on page 53 should read:

- download, modify, and upload 8751 programs without having to erase and program an 8751.
- put breakpoints in programs.
- display register and memory contents.
- ...

  etc.

FM tuner – Part 3 (May 1992)

In the PSU parts list on page 54, R_{301} should be 150 Ω, 1%, not 150 kΩ, 1%.

Video enhancer (July 1992)

Preset P_2 is best adjusted for a signal level of 2 V_{pp} at the collector of T_2. Output transistor T_3 may run fairly hot: this is normal.

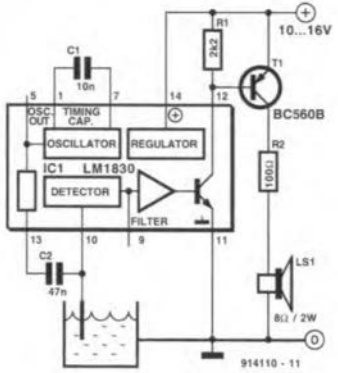
The third paragraph of the text on page 73 should read: The frequency characteristic of the signal at the base of T_3 is shaped by P_1, R_6 and C_8, and is, therefore, to a certain extent under the control of the user (with P_1).

Mark 2 QTC 80/40 loop antenna (July 1992)

The frequency '3800 kHz' mentioned twice under **2. 40-metre band** (page 90) should have read '7300 kHz'.

Audible fluid level indicator (July 1992)

Owing to a printing error, the diagram in this article is incorrect. The right diagram is shown below.



CORRECTIONS AND UPDATES

8751 Emulator

March 1992, p. 53.
(Corrections; component information)
While in emulation mode, the register contents are displayed with an offset of one vertical line from the associated register designations. This error occurs on early releases of the system software, item ESS 1741, and is caused by one superfluous 'space' character in the DEV.EXE program. This 'space' (20H) should be changed into a 'line feed' (0AH). First, make a backup copy of your original diskette. Next, use a hex editor to change the byte at address offset DE0DH from 20H into 0AH. Using the hex editor of PCTools V6, for instance, this byte is found in relative sector 111 (decimal!), at offset 0DH.

Pins 52, 53 and 54 of the SC80C451 must be connected to ground to give proper access to (simulated) Port 0. For no apparent reason, this is not indicated in the Signetics datasheets. Port 0 is actually simulated by Port 6 of the SC80C451. For further information on this compatibility problem with generic 8051 assembler files, consult the SC80C451 (Signetics) or 8xC451 (Intel) datasheets.

In addition to your local Signetics (Philips Semiconductors) distributors, two suggested suppliers of the controller Type SC80C451CCN64 are:

(1) Macro Marketing Ltd., Burnham Lane, Slough SL1 6LN. Telephone (0628) 604383.

(2) C-I Electronics, P.O. Box 22089, 6360 AB Nuth, Holland. Fax: +31 45 241877.

GAL programmer

May 1992, p. 55.
(Update)
The transistors Type BC369 in positions T6 and T7 are apparently difficult to obtain, and may be replaced by BC640s.

The most recent version of the software is V. 6.53dt, June 1992. The README file contains an update note on problems with the programming of certain GAL makes, as well as a suggestion to make GALs with a damaged electronic signature (type identifier) useable again.

8051 Single board computer

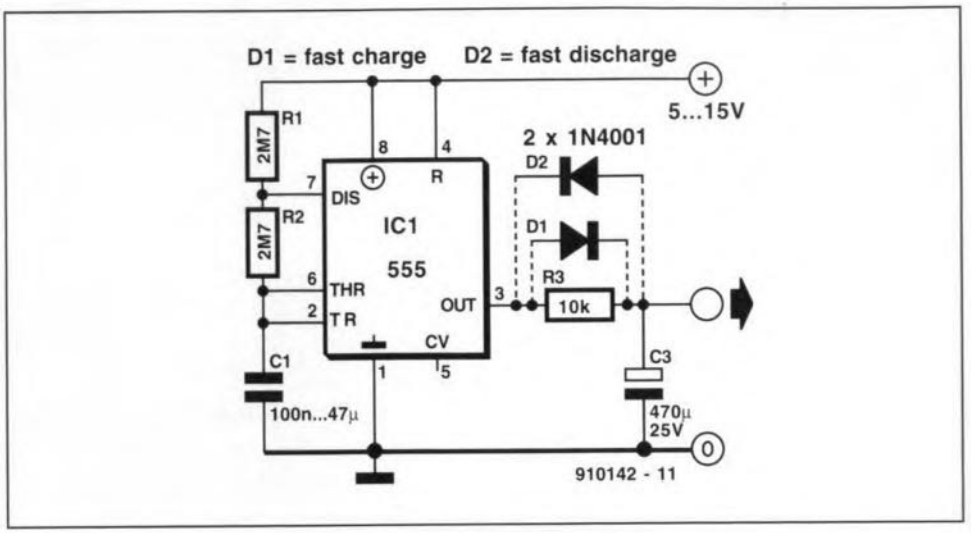
October 1992. p. 40.
(Update)
Since the publication of this article, we have been advised that the telephone number of Suncoast Technologies is +1 (904) 596-7599.

A 555-BASED RAMP GENERATOR

by R.G. Evans

WHILST developing a simple scanning receiver, a need occurred for a ramp generator to provide a varying voltage to apply to the varicap diodes fitted to the variable frequency oscillator (VCO). Referring to various literature suggested that a unijunction transistor (UJT) could be used to produce a reasonable 'sawtooth' waveform that would do the job. The circuit found provided a ramp upwards from about $\frac{1}{2}V_{cc}$ only, and in this case did not provide a sufficient range of voltage (and, therefore, scan) on the receiver. Since all the UJT circuit was doing was allowing a capacitor to charge/discharge (and was, therefore, not linear anyway), thoughts turned to other methods, hopefully cheaper and more flexible.

The ubiquitous 555 integrated circuit was chosen and put to work in a circuit based on an early application note (1976!). This circuit provided a linear charge/time graph, but allowed an output voltage swing between $\frac{1}{3}V_{cc}$ and $\frac{2}{3}V_{cc}$ only. Once again this proved insufficient for the required scan range. Thinking of ways to extend this led to the design shown in Fig. 1. The 555 is connected as an astable with a mark/space ratio of 2:1 (unfortunately 1:1 can not be achieved without additional external components) The frequency of operation can be selected by the user, but in this instance is about 0.1 Hz.



The output on pin 3 is capable of sourcing or sinking 200 mA, and switches nearly to the supply rails under no-load conditions. This alternating high and low voltage is used to charge and discharge a relatively large electrolytic capacitor via a 10-kΩ resistor. The result is a conversion of the rectangular output wave of the 555 into a waveform described by an *e*--function. By careful choice of the resistor and capacitor values, voltage swings almost between the supply rails can be obtained.

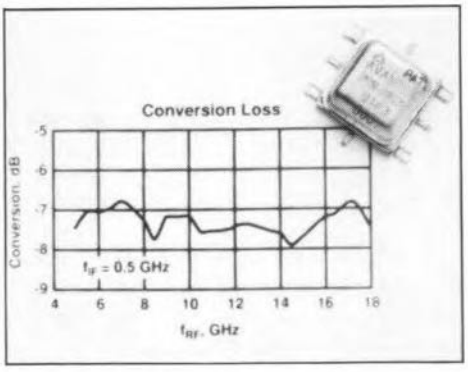
The 555-based circuit was found to provide the required voltage for the varicaps in the scanner. All this for less than the price of a suitable unijunction transistor, I hope many of you will find a use for this handy little circuit. It certainly solved my problems with the scanning receiver. ■

NEWS

GHz surface-mount mixer

Avantek Inc. has introduced the industry's first high-performance, high-frequency broadband double-balanced mixer in a true low-profile surface-mount package. This means that a microwave system engineer can now effectively replace mixers in connectorized packages (typical dimensions of 0.6×0.8 inches)) with a surface-mount component. This mixer is one of the last critical microwave components to become available in a surface-mount package, a major breakthrough in the miniaturization of microwave circuitry.

The PPM-1852L is a double-balanced mixer spanning the frequency range of 5 to 18 GHz on the RF and LO ports, with the DC-coupled IF port covering DC to 1 GHz. The LO power requirement is +10 dBm. Maximum conversion loss is 8 dB, conversion loss vs. frequency is flat to within ±2 dB, and the VSWRs at the LO and RF ports are 3.5:1 and 2.5:1, worst case in the band. This mixer features typical unit-to-unit phase match within 5°, and amplitude match within 0.5 dB. The minimum and maximum



specifications are guaranteed over the –55°C to +85°C temperature range.

Datasheets and additional information on this new device are available through

Avantek Inc., M/S M82, 481 Cottonwood Drive, Milpitas, CA 95035, USA. Telephone: (408) 943-3038. In Europe, call Avantek's UK offices at (0276) 685753.

Computer-assisted electronic logic training programme

LOGIC is the English-language version of a software package from Fitec (France) aimed at perfecting and evaluating your skills in working with logic electronic circuits. The courseware, which consists of a training manual and software for the IBM PC, enables you to master the basic principles behind a wide variety of logic circuits, and check your progress as the various subjects are presented. Each section of the train-yourself course is based on three modules: (1) lesson on theory; (2) explanatory examples taken from everyday applications; (3) tests to check your knowledge. The program that runs on the PC supports the material presented in the training manual, and comes on three 3½-inch diskettes. Among the subjects tackled during the course are decimal and hexadecimal encoding, flip-flops, adders and subtractors, multiplexers and demultiplexers, counters and registers.

Fitec, 52-54 Avenue du 8 mai 1945, F-95200 Sarcelles, France. Telephone: +33 39 923290. Fax: +33 39 921764.