ELEKTOR ELECTRONICS

THE INTERNATIONAL ELECTRONICS MAGAZINE
NOVEMBER 1991 UK £1·90

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Class A amplifier

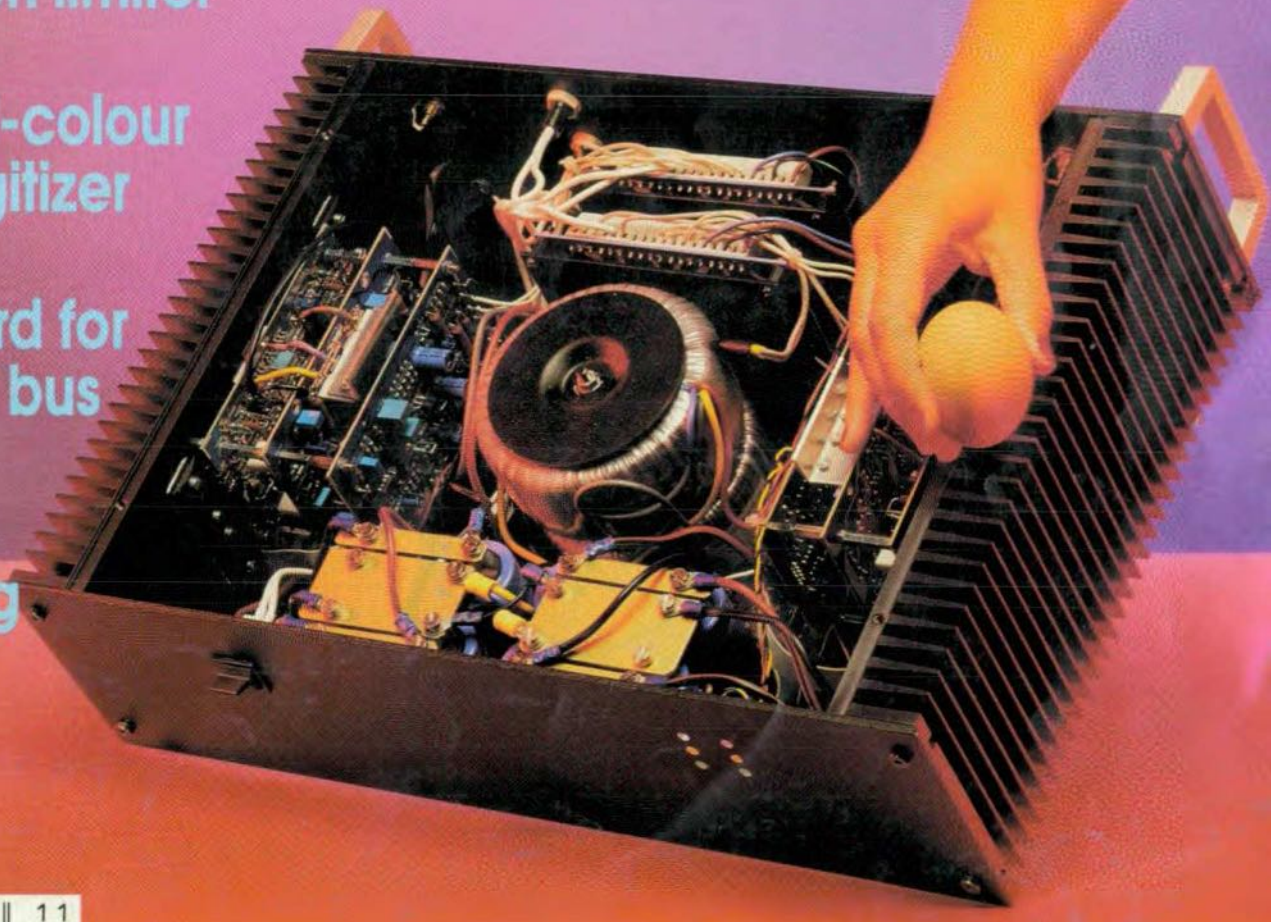
Quadriform ferrite antenna

Dissipation limiter

24-bit full-colour video digitizer

Relay card for universal bus

Product modelling



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ELEKTOR ELECTRONICS

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For many years now, hi-fi equipment has almost exclusively used class AB operation. This method gives acceptable distortion and good efficiency, and the output amplifier remains relatively cool during normal operation. However, many designers and listeners prefer class A operation with its much lower distortion and consequent higher quality of sound reproduction.
To meet their demands, we have revamped the LFA 150 power amplifier we published about three years ago. In the new design, a good compromise has been achieved between class A quality and the high heat dissipation that characterizes this type of operation.

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More than 60 construction projects and informative/ educative articles including

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ABC
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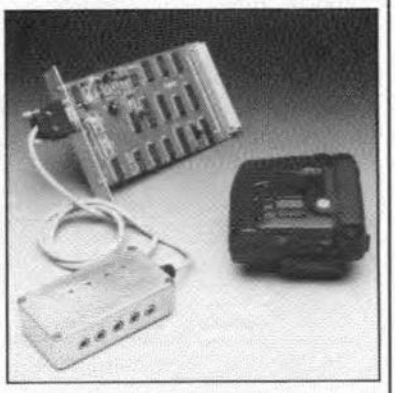

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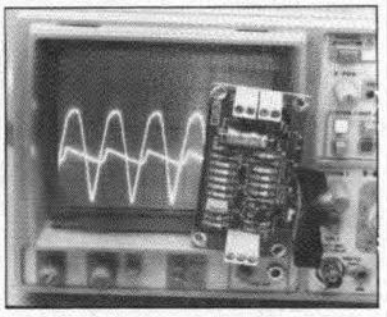

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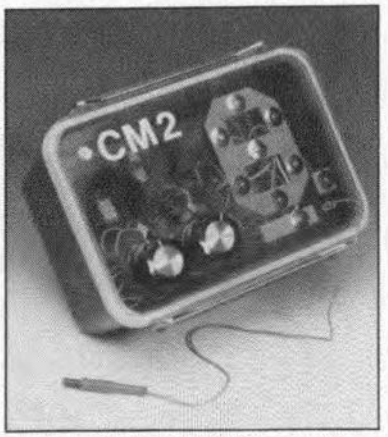

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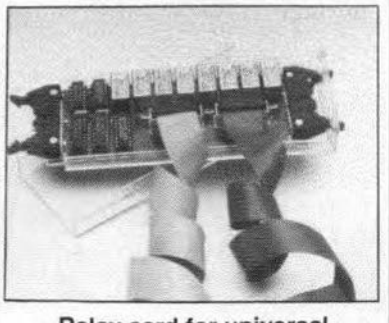

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J17 EQUALIZING NETWORK FOR SATELLITE TV RECEIVERS

While the majority of satellite television channels have sound subcarriers with 50-μs or 75-μs pre-emphasis, certain channels, particularly French and Italian, use an alternative standard called J17. Since most satellite TV receivers sold in Western Europe lack a J17 de-emphasis, and suppliers and retailers do not want to know, the author has come up with a simple add-on filter to solve the problem.

by J.M. Winsor

THE profusion of standards has always been a problem in the radio and television field. To add to the general confusion about picture standards and encryption systems, some French and Italian users of satellite TV transponders have seen fit to use a sound pre-emphasis that differs significantly from the well-established and far more generally used 50-μs or 75-μs standards. The J17 pre-emphasis is used with all channels on the Telecom 1C satellite (orbital position 5° West) and with the RAI Uno and RAI Due channels on the ECS1-F5 satellite (orbital position 10° East). The designation J17 derives from CCITT recommendation J17, published in Geneva in 1972.

Although a small proportion of domestic satellite TV receivers are compatible with J17, the majority are not. In particular, the popular 'Astra' type of receiver is equipped with 50-μs de-emphasis only.

Different curves, different sounds

While listening to a broadcast with J17 pre-emphasis and using a receiver with 50-μs or 75-μs de-emphasis (62-μs is also applied in some cases), the perceived effect is that speech seems excessively sibilant, and music harsh and unnatural. The cause of this effect is illustrated in Fig. 1, where curve 'a' represents the J17 pre-emphasis characteristic, normalized at 0 db at 100 Hz, and curve 'b' the 50-μs de-emphasis characteristic. The net

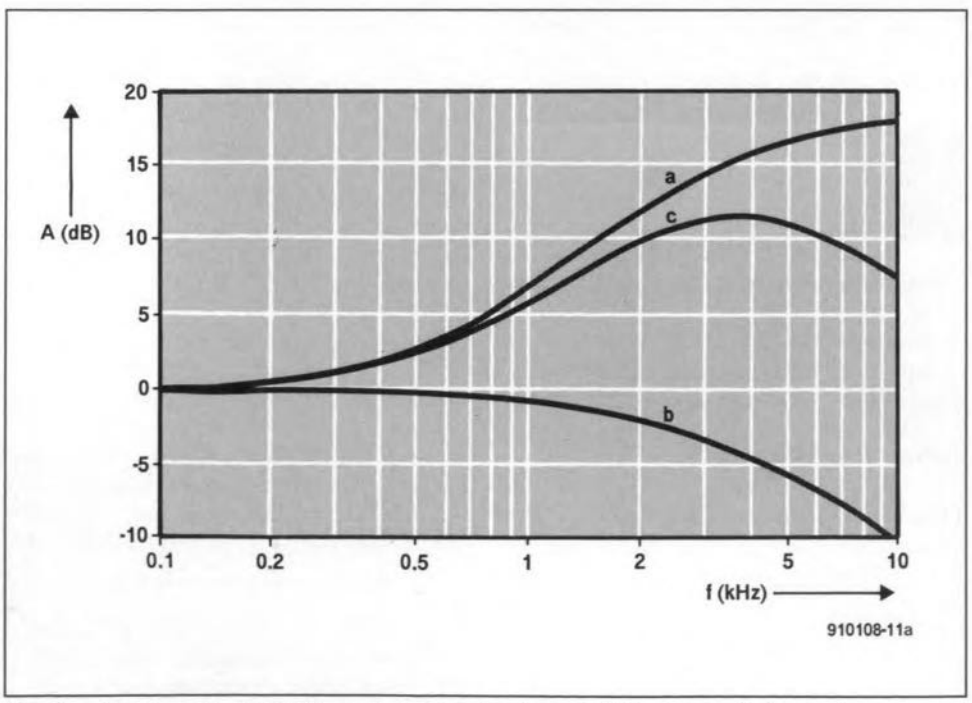


Fig. 1. Using a standard 50-μs de-emphasis characteristic (curve b) to receive a sound channel with J17 pre-emphasis (curve a) yields an undesirable amount of high-boost (curve c).

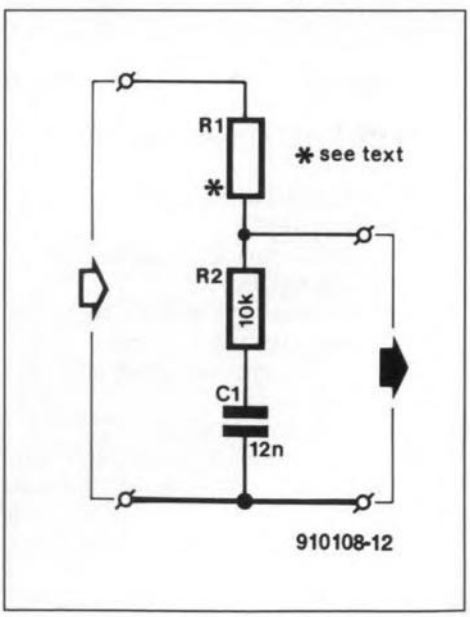


Fig. 2. Depending on the attenuation that can be tolerated, only R1 in this network takes a different value. For 6 dB attenuation: R_1=10 kΩ; for 10 dB attenuation: R_1=22 kΩ. Note that the network is designed for $Z_{in} \leq$ 600 Ω, and $Z_{out} \geq$ 100 kΩ.

result obtained by adding curve 'a' to curve 'b', i.e., receiving a J17 transmission with a 50-µs de-emphasis, is represented by curve 'c'. Clearly, high frequencies are boosted excessively at no less than about 12 dB at 4,000 Hz.

The J17 pre-emphasis characteristic is derived from the equation

$$18.75 - 10\log_{10}\left(\frac{75+(\omega/3{,}000)^2}{1+(\omega/3{,}000)^2}\right) \quad \text{dB}$$

normalized to 0 dB at 100 Hz.

By contrast, the 50-µs de-emphasis characteristic is derived from the equation

$$20\log_{10}\left(\frac{1}{\sqrt{1+(\omega\tau/10^6)^2}}\right)$$

where $\tau = 50$ µs.

A proposed solution

Rather than designing a dedicated J17 de-emphasis circuit, the author set out to reshape the output of the 50-µs de-emphasis such that acceptable sound reproduction is obtained with the French and Italian channels utilizing the J17 standard.

The circuit shown in Fig. 2 is a simple equalizing network developed to improve the poor frequency response that results from applying a 50-µs de-emphasis to a signal with J17 pre-emphasis.

The network is intended for connection between the audio output of the satellite TV receiver and the audio input to the TV. It is designed for a source impedance of 600 Ω or less, and a terminating impedance of 100 kΩ or greater.

The curves in Fig. 3 illustrate the effect of the network. Curve 'a' represents the net result of applying 50-µs de-emphasis to a signal with J17 pre-emphasis (as curve 'c' in Fig. 1), and curve 'b' the frequency response of the equalizing network. The attenuation of the network is selected to be 6 dB. The overall result of adding curves 'a' and 'b' is represented by curve 'c'. A total excursion of amplitude of 6 dB is achieved, which is a great improvement over that in curve 'c' in Fig. 1.

The design of the equalizing network is a matter of compromise. It inevitably introduces attenuation which may be overcome only by increasing the volume setting at the television set, or by the provision of additional gain elsewhere. The greater the attenuation that can be accepted, the flatter will be the overall frequency response.

Figure 4 is similar to Fig. 3, except that curve 'c' shows the overall frequency response that results from an equalizing network having an attenuation of 10 dB. Hence, the output level will be about one third that at the input. It is evident that the overall frequency response as shown by curve 'c' in Fig. 4 is much flatter than that in Fig. 3, showing a total excursion of amplitude of 4 dB (only 2.5 dB up to 7,000 Hz).

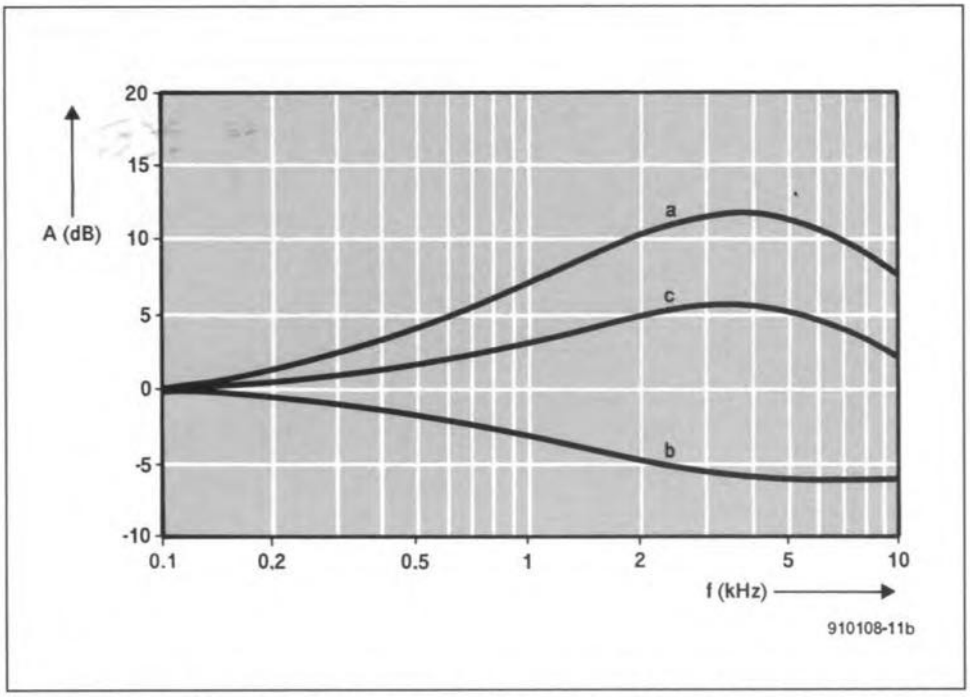


Fig. 3. Output characteristic of a J17 signal after 50-µs de-emphasis (curve a); characteristic of equalizing network (curve b); net result of adding characteristics 'a' and 'b' (curve c). Compare curve 'c' to that in Fig. 1 to see the beneficial effect of the network.

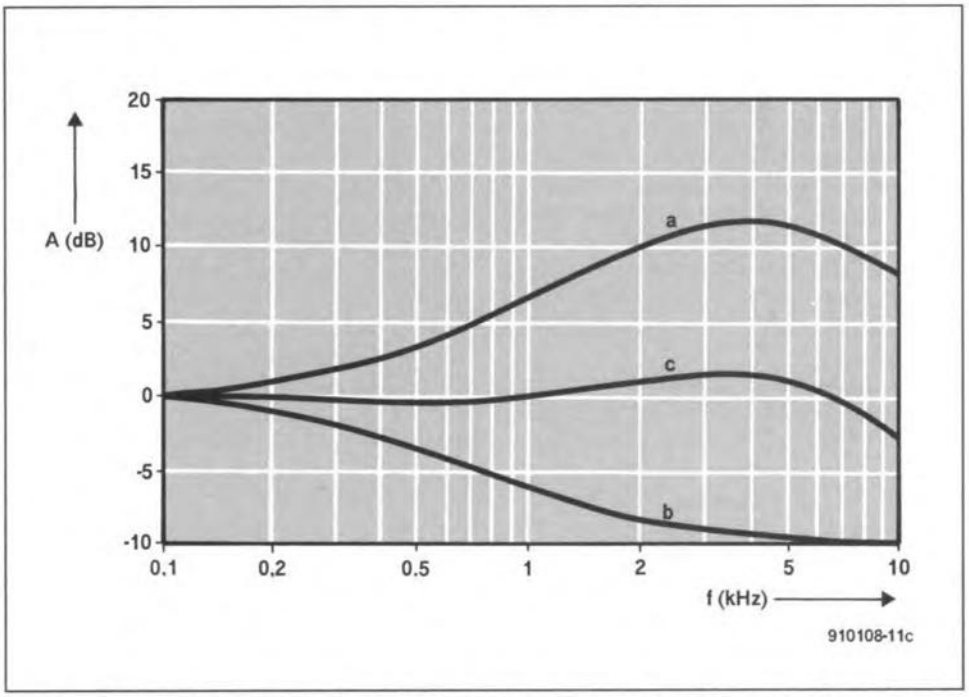


Fig. 4. As Fig. 3, but with network component values to give an attenuation of 10 dB. Despite the higher attenuation, the output characteristic is better than that of the –6 dB version of the network.

The frequency responses of the proposed equalizing network are derived as follows. For the 6-dB attenuation network:

$$10\log_{10}\left(\frac{x+(4{,}167/\omega)^2}{1+(4{,}167/\omega)^2}\right) \quad \text{dB}$$

While for the version with 10 dB attenuation:

$$10\log_{10}\left(\frac{x+(2{,}604/\omega)^2}{1+(2{,}604/\omega)^2}\right) \quad \text{dB}$$

where
$x = 1$ / anti-$\log_{10}$ (dB attenuation / 10).
The time constant $C_1(R_1+R_2)$ equals 240 µs (1/4,167 s) for the 6-dB version, and 384 µs (1/2,604 s) for the 10-dB version. These values are nominal only. ■

24-BIT FULL COLOUR VIDEO DIGITIZER

The circuit presented here enables the Archimedes video digitizer described a few months ago to handle full-colour images at an impressive resolution of 24 bits.

by J. Kortink

THE idea to process colour pictures with the aid of the video digitizer was born shortly after the publication of Ref. 1. Although computer-based colour image processing is far from simple (even a super-VGA card can only show 256 colours at a time), there is a growing demand for digitized colour photographs. This is mainly on account of the widespread use of professional DTP (desk-top publishing) packages capable of supporting 24-bit colour illustrations with the aid of colour separation techniques.

The hardware and software described here was developed with DTP applications (on the Acorn Archimedes) in mind. The performance of the digitizer is quite impressive: it needs only 10 seconds or so to 'read' and display a colour photograph — much faster than many commercial products currently offered.

Colour images

For black and white screen images, only one 'ink' colour is used: usually black. A video image may be reproduced with digital means by scanning the image at a sufficiently high resolution (both as regards the number of pixels and the number of grey levels). The video digitizer has a resolution of 640×512 pixels at 256 grey levels. The reproduction on paper of the image requires the discrete grey levels to be transformed back into ink spots. On a computer screen, intensity modulation is used, while on paper grey levels are reproduced by controlling the size of the ink spots. Hence, the resolution of the printer attached to the computer determines the number of grey levels that can be reproduced. Most 300-dpi (dots per inch) laser printers are capable of reproducing 16 simulated grey levels. Professional image setting machines typically achieve 200 levels when set to a resolution of 2400 dpi. Photographic paper has no such limitations, offering a virtually infinite number of grey levels.

In practice, 64 intensity levels are sufficient to faithfully reproduce a photograph. The 256 grey levels offered by the video digitizer are, therefore, ample for most applications.

Colour images on a computer screen are invariably made by 'building' individual picture elements from three primary colours. In the case of the video digitizer, use is made of the three additive primary colours red, green and blue (RGB model). By contrast, magazine and book printers traditionally use the subtractive primary colours cyan, magenta and yellow, to which is added black (CMYk model).

During the digitizing operation, the saturation of the three primary colours red, green and blue of each picture element is measured. This means that the image is actually scanned three times: once for the red components, once for the blue components, and once for the green components, the saturation of which is stored as a digital value in the computer memory. A digitized colour image is then obtained by combining the three scanned images containing the primary colours. This technique is not unlike that used in the graphics and printing industry, where colour separations are used to produce three or four plates (screens) that each represent a primary colour. The fourth plate represents black, and is used for the brightness information only. During the offset printing process, the images on the plates are printed over one another to give an image with composite colours. Note, however, that the individual picture elements are not printed on top of each other, but side by side with an accurately controlled distance (off-set). In this system, the black plate is theoretically not required, since black can be reproduced with the three primary colours also. In practice, however, black so printed has a brownish hue. Grey levels are, therefore, printed with black ink, which avoids undesirable sub-colours.

Returning to computers, the number of colours is usually determined by the type of video card used. Fortunately, we may avail ourselves of mixing techniques to take the number of colours that can be shown on the screen over the number of colours actually available. This is achieved by dithering, or pixel combination. Unfortunately, dithering has the inherent disadvantage of reducing the overall picture resolution.

Dithering techniques are based on error distribution protocols developed by, among others, R.W. Floyd and L. Steinberg. These protocols allow the difference between the desired colour and that produced on the basis of the actually available colours to be made as small as possible. Unfortunately, we have to leave the subject of dithering at this brief description, since a discussion of the related techniques is beyond the scope of this article. The software developed for the present colour extension of the video digitizer does, however, provide pixel dithering routines.

The hardware

As already mentioned, the black and white video digitizer described in Ref. 1 is taken as the starting point. To be able to process colour images, the video information has to supplied as RGB signals. Lacking an RGB output on your video equipment, existing composite video or S-VHS video signals have to be converted into RGB signals first. This may be done with a special converter — see Ref. 2. Cameras, video recorders, tuners and the like capable of producing RGB signals do not require an additional converter,

and can be connected direct to the input of the present circuit, which is basically an interface between the video source and the input of the video digitizer.

The circuit diagram of the RGB interface is given in Fig. 1. The circuit is really quite simple. Two control signals supplied by the digitizer select one of the four signal inputs via IC1a and four relays. As indicated, three inputs are used for the primary colours, and a fourth for a composite video signal, allowing black and white images to be digitized in a simple manner. The fifth input serves to pass the synchronization signals to the video digitizer. This input is not switched because the sync signals must always be present. Four LEDs are used to indicate which of the four video inputs is connected to the digitizer.

The printed circuit board used to build the interface is shown in Fig. 2. The construction is straightforward, and should not present problems to those of you who have already successfully built the video digitizer.

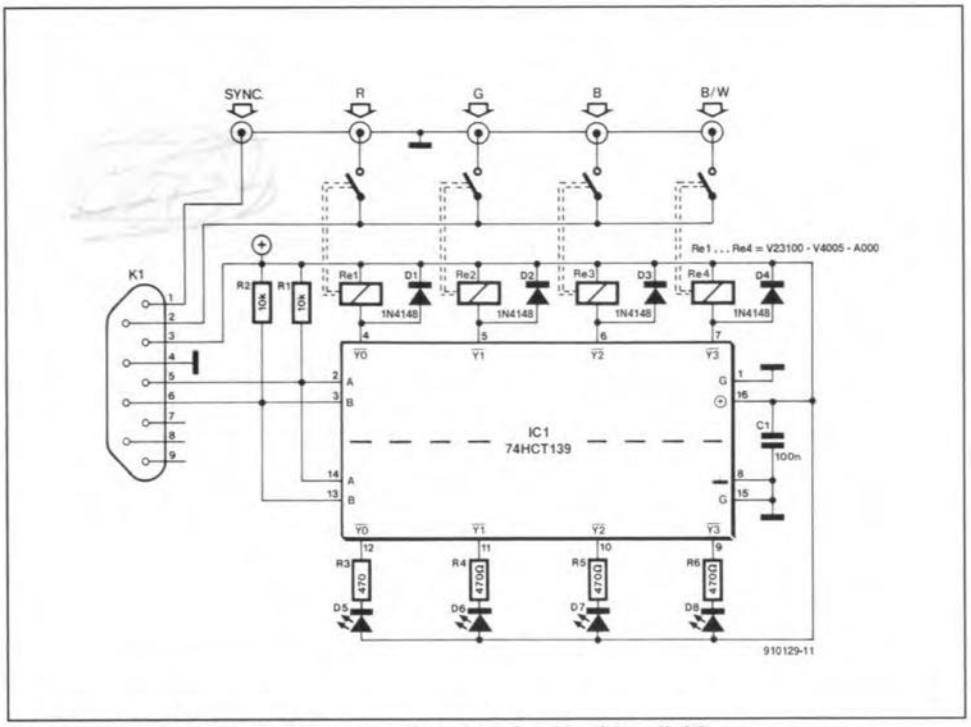


Fig. 1. Circuit diagram of the colour interface for the video digitizer.

A small modification

The circuit of the video digitizer requires a small modification to be made before it can be used for the colour applications we have in mind. First, a 9-pin sub-D connector is fitted on the aluminium support bracket of the podule. This connector takes the place of the existing cinch or BNC socket. For the original black and white application of the digitizer, the video input is fed to the A-D converter (IC10) and the sync separator (IC11) via a buffer stage. Since for colour applications the synchronization and colour signals have to be applied separately, capacitor C18 is removed from the board, and a wire is soldered to pin 2 of IC11. Next, a 100-nF capacitor (C18) is soldered between the free end of the wire and pin 1 of the D9 connector. The video signal is connected to pin 2, the power supply to pin 3, and ground to pin 4.

Finally, we need two control signals. These are supplied by IC15, a PCF8574 — one of the three optional I/O ICs on the podule. Fit this IC and the associated pull-up resistor array, R9, on the podule board. Output lines P0 and P1 (IB0 and IB1) are available on pins 1 and 2 of connector K2. These lines are connected to the D9 connector, for instance, to pins 5 and 6.

The colour interface is connected to the video digitizer via a 6-way cable terminated with D9 connectors at both ends.

The above modification still allows black and white images to be digitized without the interface when a video connector is used with a 9-pin D plug, of which pin 1 is connected to pin 2, i.e., the video signal is connected to these two pins, while ground is connected to pin 4.

Software: !GreyEdit

The control program for the colour version of the video digitizer is called !GreyEdit, and comes on a diskette (Archimedes format) supplied through the Readers Services under order number ESS 1631. All other functions in the program !VidiDigi (see Ref. 1) are also included on this disk.

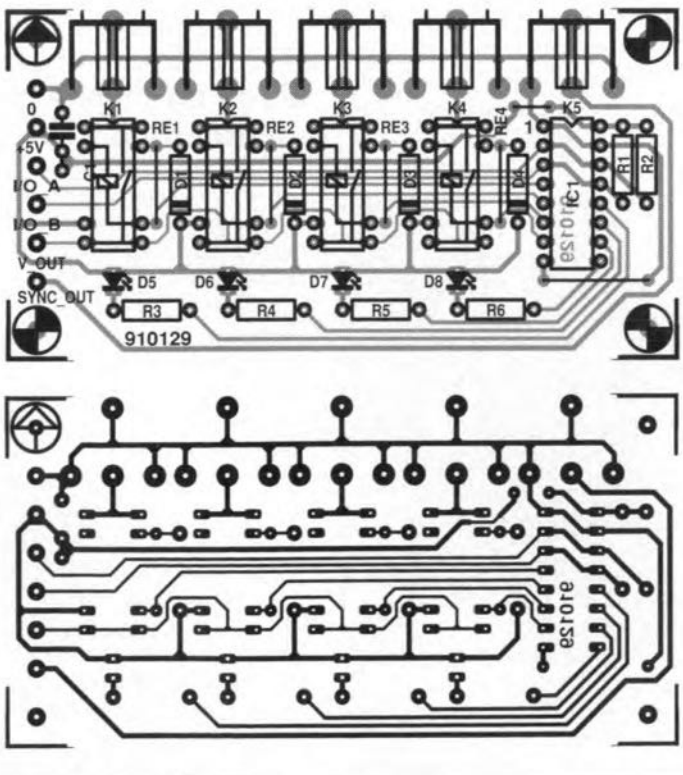


Fig. 2. Printed circuit board for the colour interface.

COMPONENTS LIST

Resistors:

2	10kΩ	R1;R2
4	470Ω	R3-R6

Capacitors:

1	100nF	C1

Semiconductors:

1	74HCT139	IC1
4	1N4148	D1-D4
4	LED	D5-D8

Miscellaneous:

4	V23100-V4005-A000 (Siemens)	Re1-Re4
1	9-way sub-D plug, with hood	
1	9-way sub-D socket	
5	RCA (phono-) socket for PCB mounting	
1	enclosure, aluminium, size approx. 109×58×25 mm (e.g., Hammond 1590)	
1	control software on disk	ESS1631

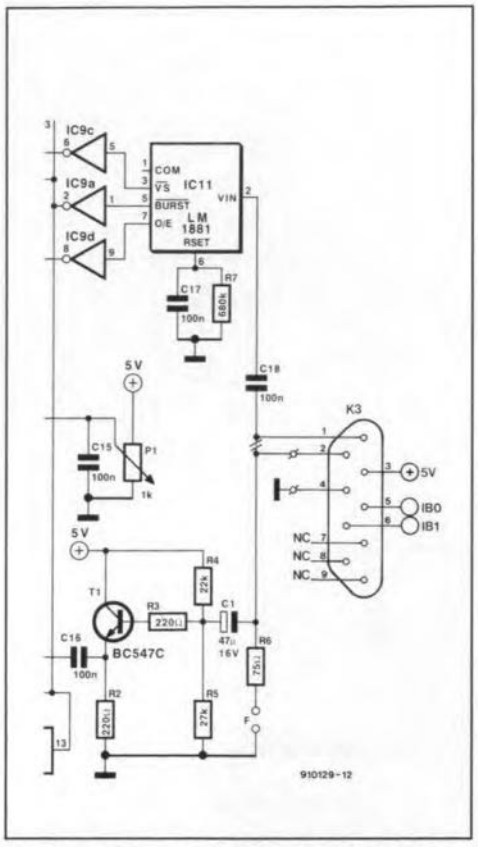


Fig. 3. The modifications to the original video digitizer are simple to make, while all functions are retained.

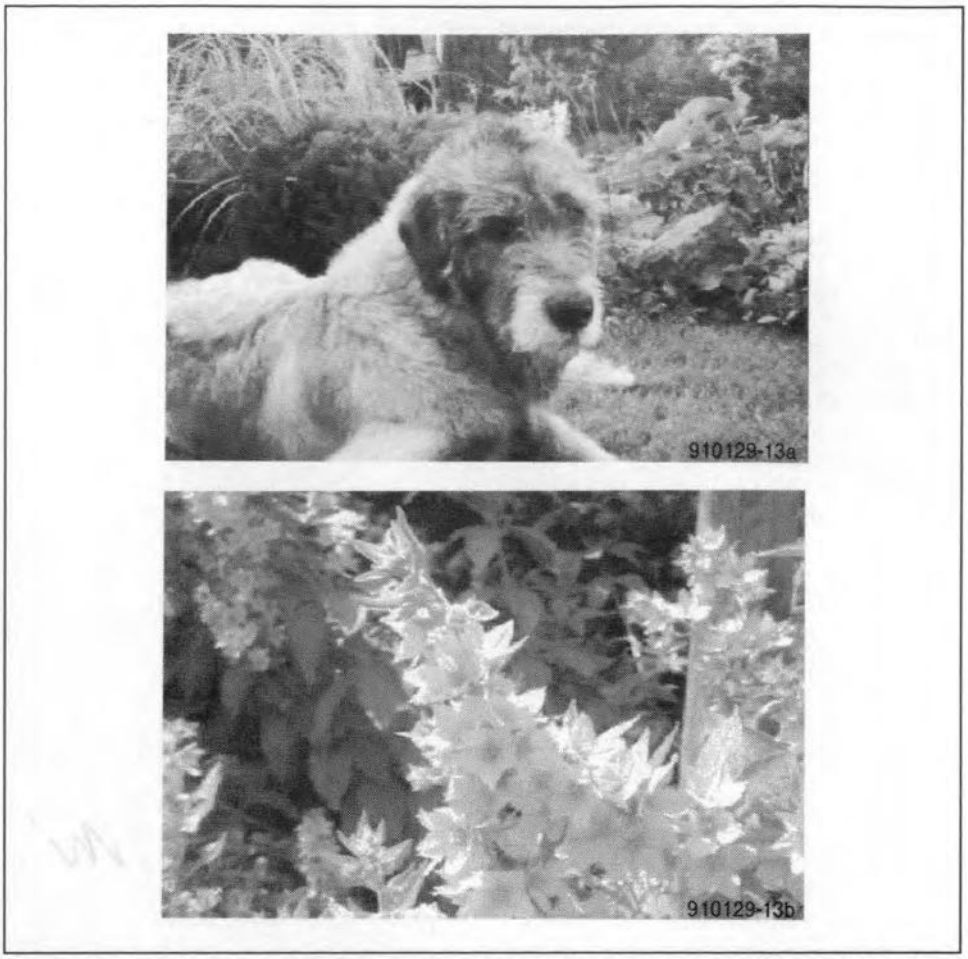


Fig. 4. Digitized photographs taken with a Canon ION. Use was made of the S-VHS output. Also, the picture was improved with the 'sharpen' function provided by the control software developed for the Acorn Archimedes.

The digitizer functions are available via the 'digitizer' sub-menu. The buttons on the screen allow you to select one of the three primary colour signals, or the black and white signal. The selection must be indicated by the LEDs on the interface board. The program also has a utility that allows a colour image to be digitized automatically. On selecting this function, you are prompted to inform the computer where the digitized images are to be stored. Simply drag the icon to a directory on the diskette or hard disk. The digitizing operation starts immediately after this has been done. The files containing the red, green and blue information are stored successively in the indicated directory. The digitizing process is complete after three scans, and the R, G and B information is ready for combining into a new, larger, file. Drag the directory with the three primary colour files to the window marked !GreyEdit. Next, the program asks you where the photograph is to be stored (saved), and under what name. If everything works correctly, the colour photograph will be ready after a few seconds of number crunching activity. The photograph is written in the 'Clear' format and may be converted into a GIF, TIFF or PBM file with the aid of the !Creator utility. Mind you, the current versions of the GIF protocol do not support 24-bit colours. It is, therefore, recommended to use the TIFF format to export files.

The picture may be edited with !Translator, which is supplied on the disk together with !GreyEdit and !Creator. Finally, note that the size of the image files requires a hard disk and a minimum memory of 2 MByte.

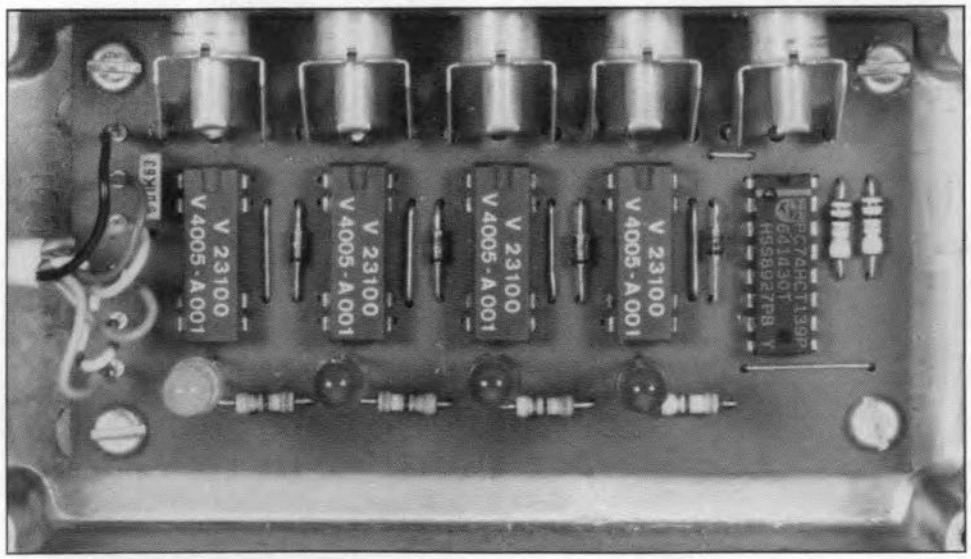


Fig. 5. Interface fitted in a compact enclosure. The unit is connected to the computer via a short flexible cable.

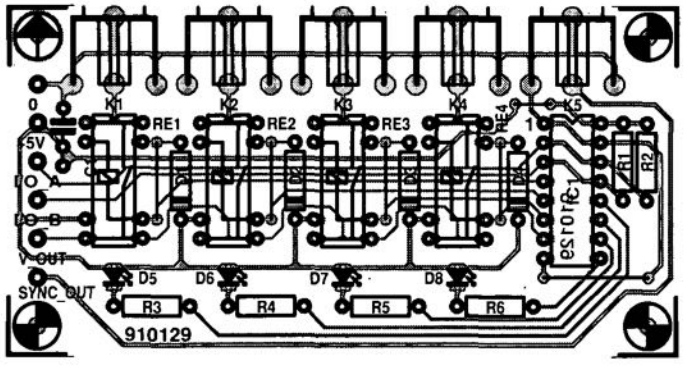
Black and white image enhancement

A couple of experiments with a Canon ION RC-260 camera showed that the quality of digitized black and white pictures can be improved considerably when a video source with an S-VHS (super-VHS) output is used. Where such a source is available, connect its luminance signal (pins 1 and 3) only to the digitizer. Results close to perfection may be obtained in this manner, particularly if the 'sharpen' function of !Greyedit is used. The two photographs in Fig. 4 were produced in this way. After digitizing, they were converted into Postscript, and printed on a Agfa Compugraphic Type 9800 photo typesetter. ■

References:

1. Black-and-white video digitizer (for Acorn Archimedes). *Elektor Electronics* July/August 1991.

2. S-VHS/CVBS-to-RGB converter. *Elektor Electronics* September and October 1990.



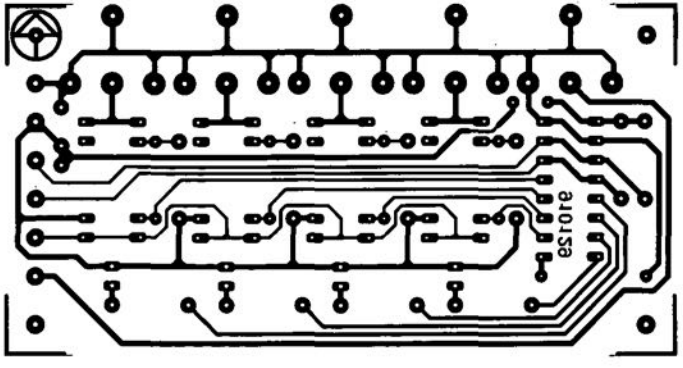


Fig. 2. Printed circuit board for the colour interface.

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5	RCA (phono-) socket for PCB mounting	
1	enclosure, aluminium, size approx. 109×58×25 mm (e.g., Hammond 1590)	
1	control software on disk	ESS1631

DISSIPATION LIMITER

by C. Zschocke

Dissipation in electronically regulated power supplies, manifested by heat, is a problem that is normally tackled by providing external heat sinks. The limiter presented here offers a more intelligent solution. It can be used as an add-on unit with virtually any power supply.

THE secondary alternating voltage in power supplies stabilized with the aid of series regulators is normally calculated to ensure that with maximum output voltage and current the potential across the reservoir capacitor does not drop below the minimum voltage, U_r, required for satisfactory operation of the regulator. When the supply operates below maximum output voltage and current, the power that is then not required is converted into heat. Moreover, the design allows for maximum output voltage and current even when the mains voltage is at its lowest specified level.

The secondary voltage may well be specified too high, with the result that when the mains voltage is at its highest specified level and the power supply is open-circuited, the maximum permissible potential across the reservoir capacitor, and thus that at the input of the regulator, may easily be exceeded.

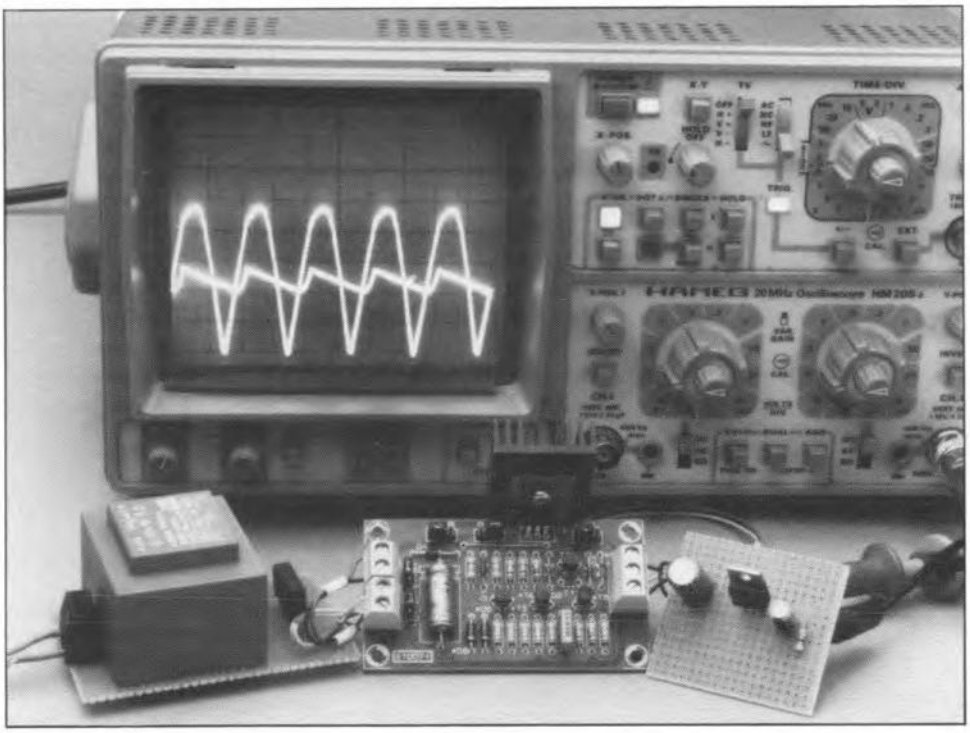
It is clear that in most power supplies, the specified voltage levels for the regulator and reservoir capacitor are needlessly high.

Possible solutions

The uneconomical design outlined above may be improved in several ways. It is, for instance, possible, with the aid of relays, to select secondary alternating voltages according to the load requirement. This is, however, possible only with a very special, and therefore expensive, mains transformer. Another possibility is to use phase gating control. This, however, requires fairly high switching currents and causes noise on the mains supply. Moreover, capacitors that can withstand high current pulses must be used and these are expensive.

A third method is used in the circuit presented here. In this, the charging of the reservoir capacitor is interrupted when a certain potential across the capacitor is reached. The circuit, which can be added to most existing regulated mains power supplies,

- minimizes the power dissipation;
- offers an additional reduction in dissipation during a short-circuit or during current limiting;
- is inexpensive to build;
- uses only standard, readily available components;
- needs only little space;
- is suitable for high-current supplies;
- can be used with positive and negative series regulators.



Principle of operation

In Figure 1, an electronic switch, for instance, a SIPMOS transistor, is inserted between the rectifier and the reservoir capacitor. At the start of each half cycle, the switch is on (U_r>3 V). A charging current flows into the capacitor

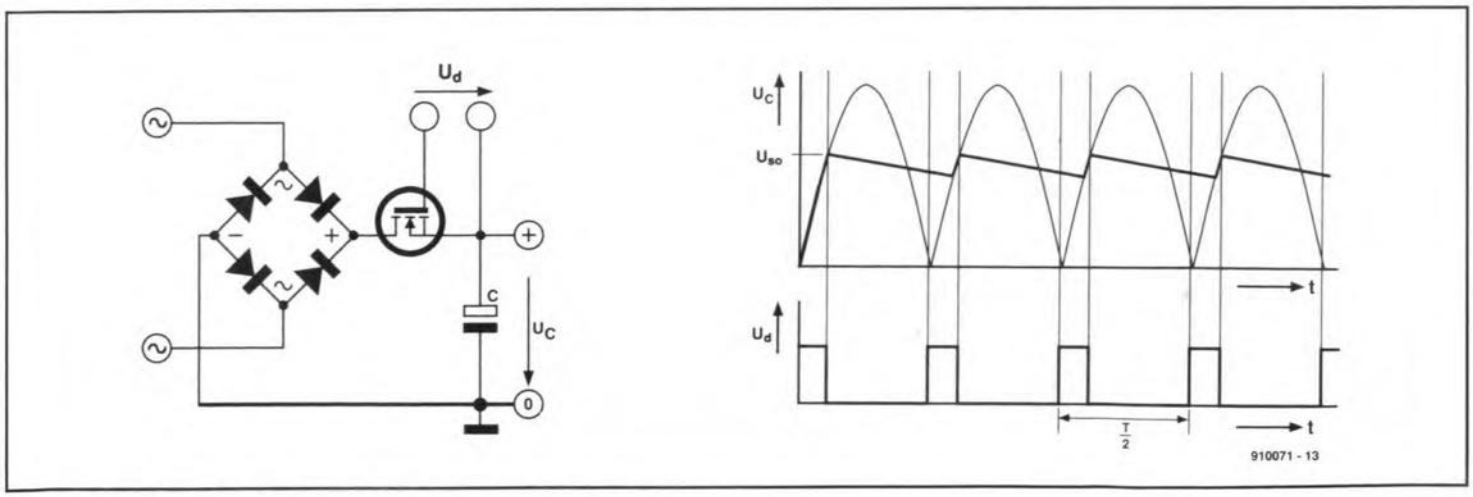


Fig. 1. Principle of operation of the dissipation limiter.

and the potential, U_c, across the capacitor follows the instantaneous level of the half-wave voltage. When U_c has reached the minimum level, U_{so}, required for the wanted output voltage, U_o, the charging current is switched off until the end of the half cycle. The level of U_{so} must be chosen to ensure that U_c does not drop below U_r until charging current begins to flow again at the start of the next half cycle. This voltage is the sum of the wanted output voltage, the drop across the regulator, U_d, and the voltage resulting from the discharging of the capacitor. The difference ΔU that is, the series switch-off voltage, $U_{so(m)}$, between U_r and U_{so} is easily determined, since it is directly proportional to the charging current; in fact, $\Delta U = It/C$, where I is the charging current, t is the time during which charging current flows, and C is the capacitance of the reservoir capacitor. Thus,

$$U_{so} = U_o + U_d + \Delta U$$

$$= U_o + U_d + It/C.$$

The time t is, in full-wave rectification, equal to a half cycle of the mains frequency, that is, $T/2$. Then,

$$U_{so} = U_o + U_d + IT/2C.$$

If now the maximum permissible output current, $I_{o(m)}$ is substituted for I, the highest potential drop across the regulator (at the start of each half cycle) is

$$U_{so(m)} = U_{so} - U_o = U_d + I_{o(m)}T/2C.$$

From this, the instantaneous dissipation, P_r, can be computed:

$$P_r = I_o U_{so(m)} = I_o[U_d + I_{o(m)}T/2C - I_o T/4C].$$

As an example: a power supply with a reservoir capacitor of 3 300 µF is required to provide an output voltage of 0–15 V at a maximum current of 1 A. Since the potential drop across the regulator is 3 V, the voltage across the capacitor, U_c, must be at least 18 V. Without limiting, the maximum power loss, $P_{r(m)}$, in the regulator is 18×1=18 W (which is, for instance, the case when maximum current flows at very low output voltage as in a short-circuit condition).

With limiting, the voltage across the capacitor, U_{so}, needs to be only

$$U_{so} = U_o + U_d + I_o t/C =$$
$$= 0 + 3 + 1 \times 10^{-2}/3300 \times 10^{-6} = 3.03 \text{ V}.$$

The maximum dissipation is reduced to

$$P_{r(m)} = I_o[U_d + I_{o(m)}T/2C - I_o T/4C].$$

Since $I_o = I_{o(m)}$,

$$P_{r(m)} = I_o(U_d + I_{o(m)}T/4C =$$

$$= 1(3 + 1 \times 2 \times 10^{-2}/4 \times 3300 \times 10^{-6} = 4.5 \text{ W},$$

which is an appreciable improvement.

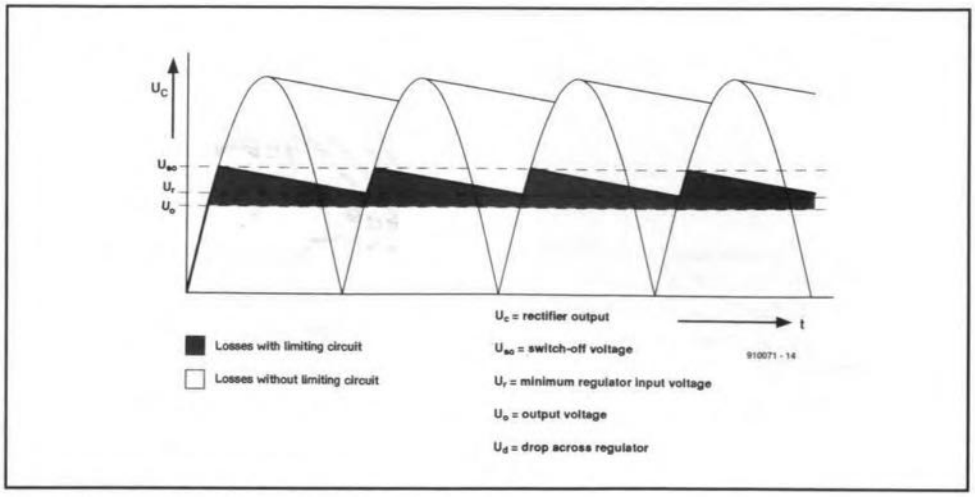


Fig. 2. Dissipation with and without limiter.

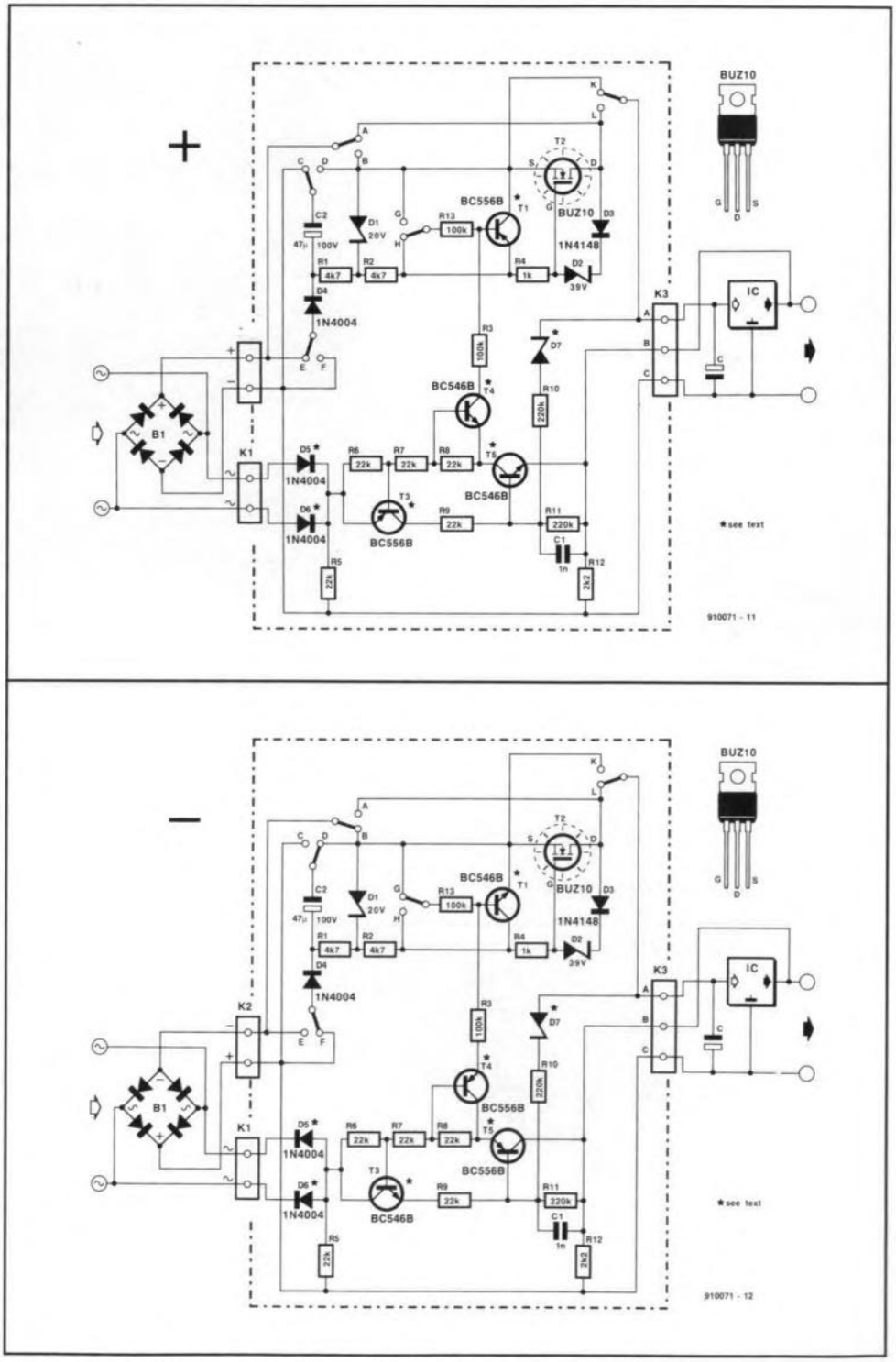


Fig. 3. Circuit diagram for both versions of the dissipation limiter.

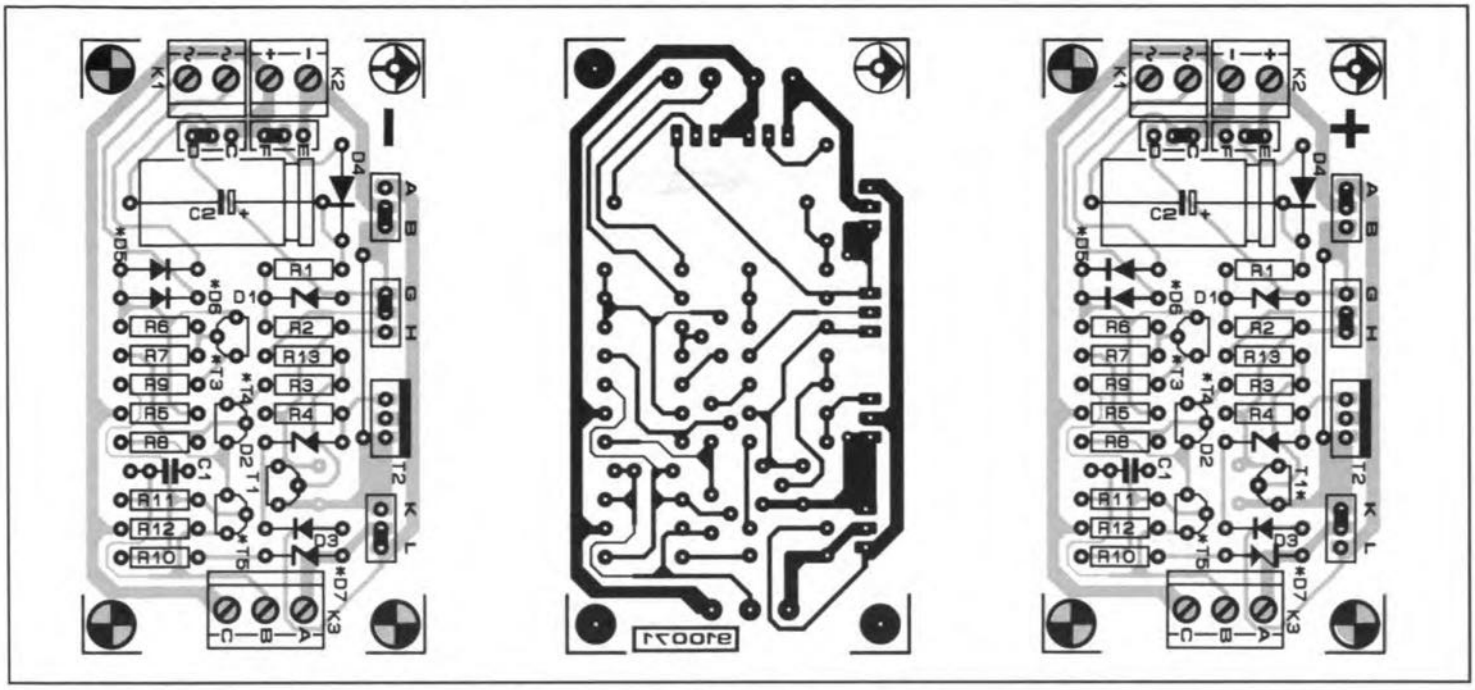


Fig. 4. Printed circuit boards are available for both versions of the dissipation limiter.

PARTS LIST

Resistors:
R1, R2 = 4.7 kΩ
R3 = 100 kΩ
R4 = 1 kΩ
R5–9 = 22 kΩ
R10, R11 = 220 kΩ
R12 = 2.2 kΩ
R13 = 100 kΩ

Capacitors:
C1 = 1 nF
C2 = 47 µF, 100 V

Semiconductors:
D1 = zener diode, 20 V, 400 mW
D2 = zener diode, 39 V, 400 mW
D3 = 1N4148
D4–6 = 1N4004
D7 = see text
T1, T3 = BC556B (pos); BC546B (neg)
T2 = BUZ10 or BUZ11 (see text)
T4, T5 = BC546B (pos); BC556B (neg)

Miscellaneous:
Heat sink for T2
PCB 910071

The practical circuit

The circuit in Fig. 3 may be split into the drive for the current switch, the switch itself (T_2) and a 'thyristor'. The thyristor is formed by transistors T_3 and T_5; its cathode is connected to the output terminal of the series regulator.

The thyristor is switched on via zener diode D_7 as soon as the voltage across the regulator exceeds the level fixed by the zener diode plus the b-e voltage of T_5. It switches itself off just before the next zero crossing. To make certain that it does, it is decoupled from the rectifier and the inverse diode of T_2 via D_4 and D_5, which are loaded by R_5.

When the thyristor is on, T_4 switches T_1 on and this in turn switches T_2 off.

Transistor T_4 also serves, in conjunction with R_3, to decouple the thyristor and the charging-current switch.

Diode D_4 and C_2 provide T_2 with the necessary switching voltage.

Zener diode D_1 protects the gate of T_2 against overvoltage.

The inductance of the mains transformer causes a high back e.m.f. when the charging current is switched off, and this may upset the correct operation of T_2. This is prevented by D_2 and D_3, which switch off T_2 as soon as the back e.m.f. exceeds the permissible reverse bias. A useful effect of the back e.m.f. is that it increases the potential across C_2, which guarantees satisfactory switching of T_2 even when the output voltage is a maximum.

Resistor R_{12} ensures correct switching of T_2 when the output is not loaded (open circuit). It must be rated at $U_{o(m)}^2/R_{12}$ Watt. It may be omitted if the power supply is permanently loaded.

Transistor T_2 must be fitted, *insulated*, on its own heat sink or on that of the regulator.

Depending on the component values, the limiter may be used with secondary alternating voltages of up to 50 V_{peak}. It is not possible to say what the maximum load current can be without knowing the value of the reservoir capacitor and the specification of the mains transformer. What can be said is that the maximum charging current pulses must not exceed the maximum permissible current through T_2, which is 19 A for the BUZ10 and 30 A for the BUZ11.

The limiter can be used without any problem in 5 A power supplies. The prototype operated satisfactorily with an output current of 10 A (reservoir capacitor was 10 000 µF). It is always possible in doubtful cases to connect two or three SIPMOS transistors (T_2) in parallel.

Here are some tips for calculating the values or ratings of a number of components.

- The zener voltage of D_7 must be U_{so}–0.7 V ($U_{b\text{-}e}$ of T_5).
- The maximum reverse bias of T_2 must be greater than the peak value of the potential across the reservoir capacitor.
- The zener voltage of D_2 must be equal to the maximum reverse bias of T_2 minus 5 V.
- Capacitor C_2 must be rated at $U_{so(m)}$ plus 20 V (D_1).
- Transistor T_4 must be able to withstand voltages of $U_{so(m)}$ plus 20 V (D_1).
- Transistors T_3 and T_5 must have a reverse bias rating equal to the peak value of the secondary alternating voltage.
- Resistor R_{12} must be rated at $U_{o(m)}^2/R_{12}$ (watts).
- All connecting wires should be as short as possible and of appropriate thickness.
- The dimensions of the heat sink depend on the transformer, the reservoir capacitor and the maximum permissible short-circuit current.
- In most cases, it is possible to fit T_2 on the heat sink of the regulator.

Construction

The limiter described above is, of course, intended for positive voltages. One for negative voltages operates in a similar manner, but the polarity of some components must be reversed.

Whichever version is needed, it is best constructed on the appropriate printed-circuit board shown in Fig. 4. The differences between the two versions are indicated by an asterisk (*).

It is recommended to 'strengthen' the broad tracks by soldering thick, bare wire on them.

The completed unit is, as shown in Fig. 3, interposed between the rectifier and the reservoir capacitor. Short, heavy-duty wiring should be used. ■

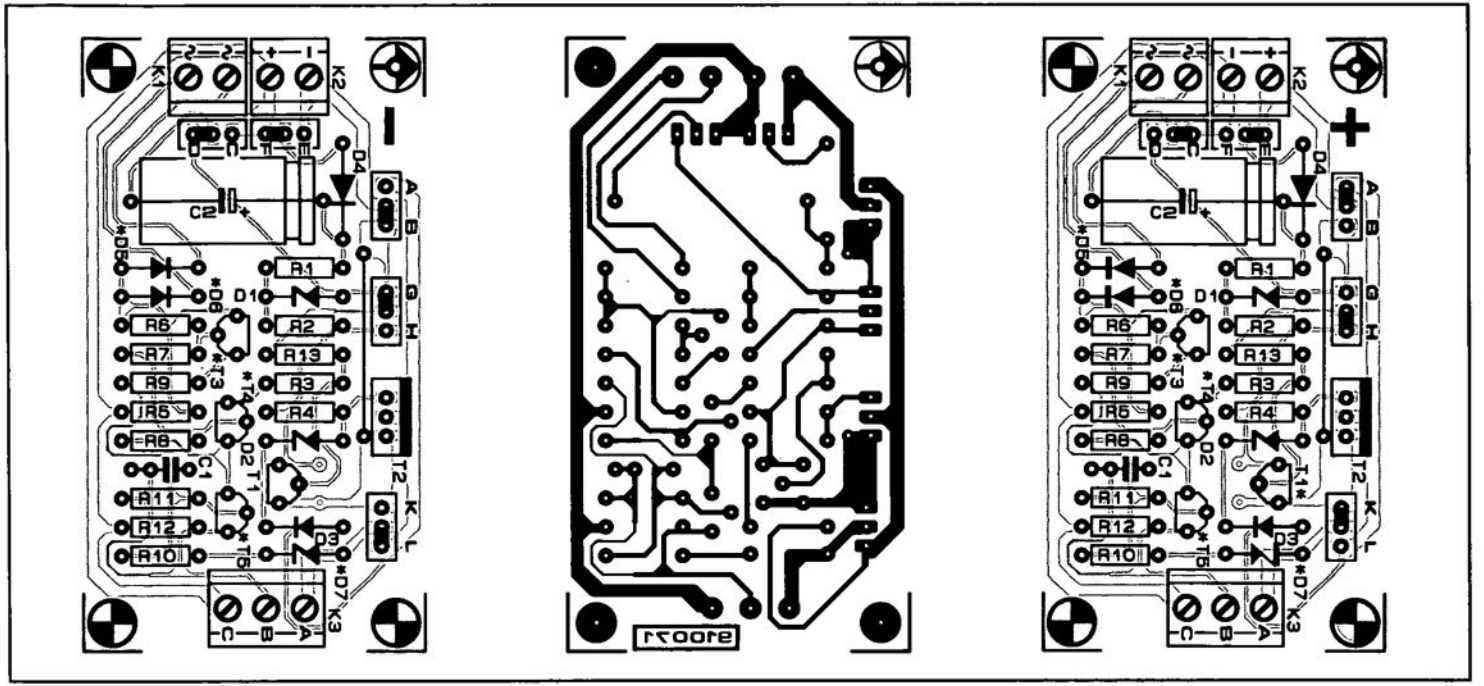


Fig. 4. Printed circuit boards are available for both versions of the dissipation limiter

DIGITAL FUNCTION GENERATOR – PART 2

by T. Giffard

THE ONLY connection between the PLL board and the discretely designed analogue parts of the generator is via plugs and sockets K_2, K_5, and K_8. Pin 1 of these connectors carries the 32 Hz–3.2 MHz clock, which is converted in the various sections to a 1 Hz–100 kHz sinusoidal, rectangular or triangular signal. The other pins carry information about the selected decadic range.

Sine-wave converter

The conversion of the rectangular output signal of the PLL loop into a sinusoidal waveform takes place in three stages—see Fig. 17. The first of these is a digital-to-analogue (D–A) converter with serial input, IC_{26}–IC_{28}; the second, a filter section that removes any unwanted harmonic frequencies; and the third, an output stage based on IC_{40}.

The D–A converter consists of two cascaded 8-bit shift registers, IC_{27} and IC_{28}, whose 16 outputs are fed via a single opamp, IC_{34}, to the filter section.

Before the first pulse arrives at the clock inputs of IC_{27}–IC_{28}, all 16 outputs of the registers are low, whereas inputs B are high. Input A of IC_{28} is low, but input A of IC_{27} is high, since the (low) level at pin 13 (QH) of IC_{28} is inverted by IC_{26d}. Therefore, when the first clock pulse is received, output QA of IC_{27} goes high; on the second clock pulse, QB goes high (while QA remains high) and so on. When, on the eighth pulse, QH goes high, input A of IC_{28} becomes high, so that the outputs of this register also go high consecutively (QA→QH). After 16 clock pulses, all outputs of both registers are high, whereupon input A of IC_{27} goes low, as explained earlier. The outputs then go low in succession until after a further 16 clock pulses the process repeats itself.

The high level at the outputs is 6 V and the low level is 0 V (earth). The values of the series resistors at the outputs have been cho-

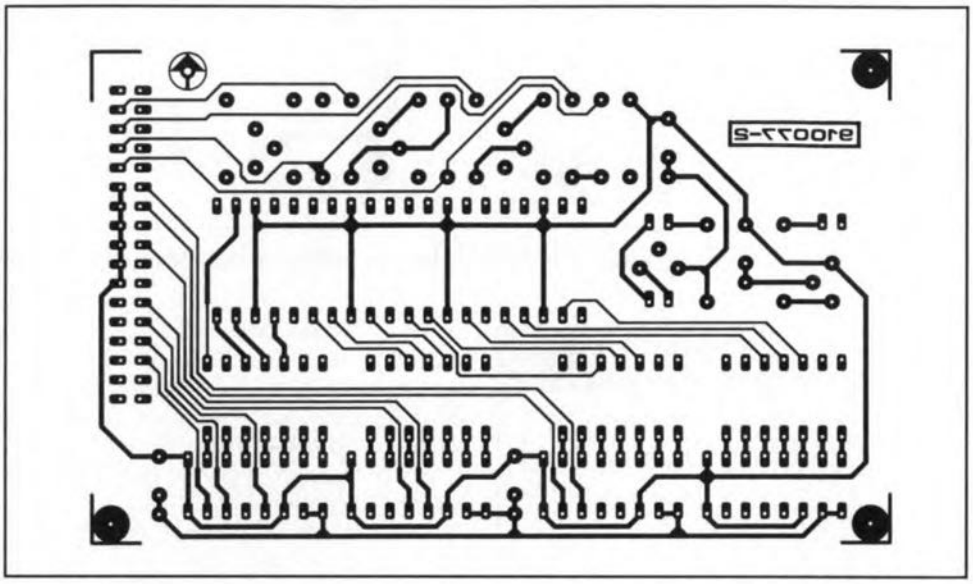


Fig. 13. Third overlay of the PCB for the analogue section of the function generator (belongs to Fig. 10)

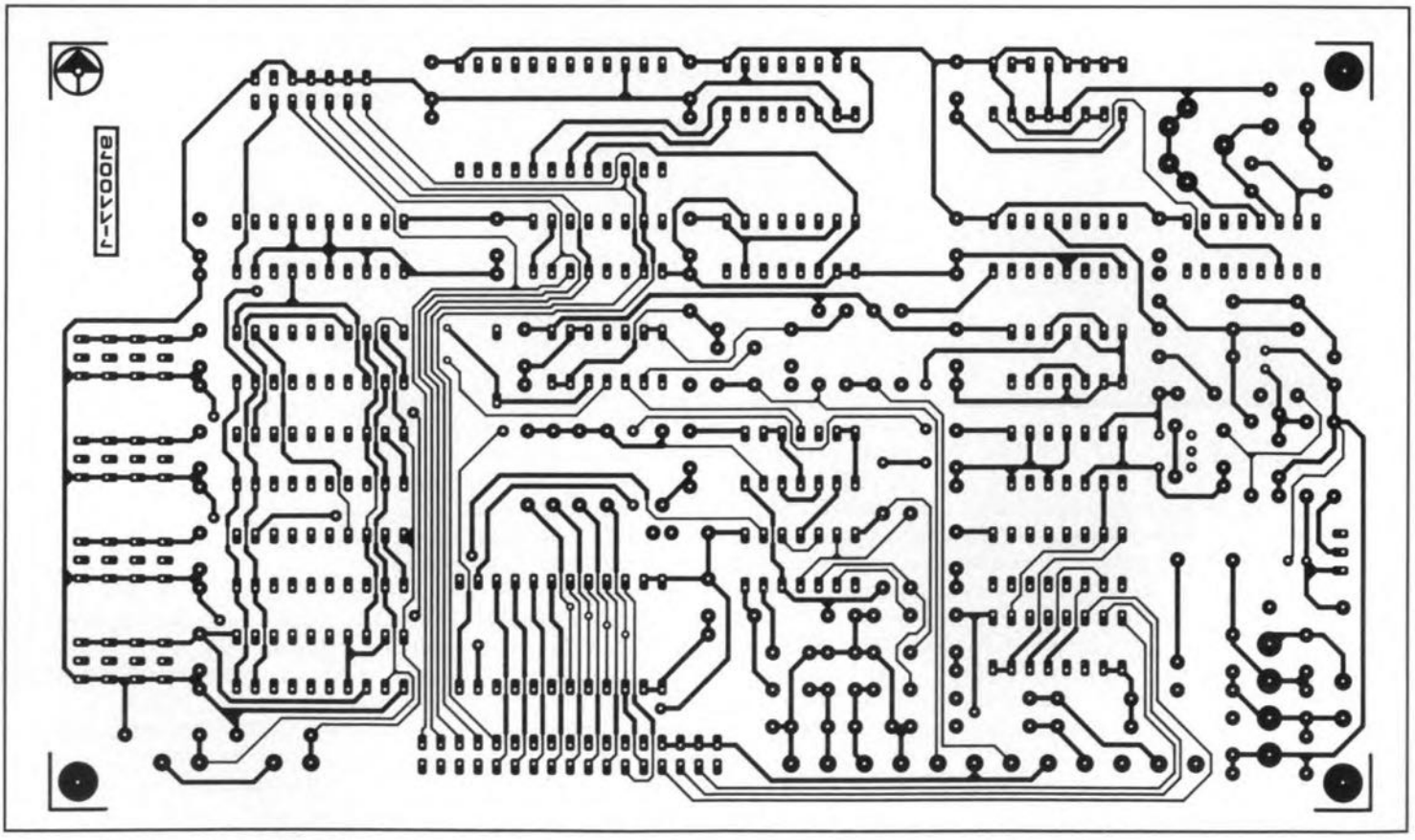


Fig. 14. Third overlay of the PCB for the digital section of the function generator (belongs to Fig. 7)

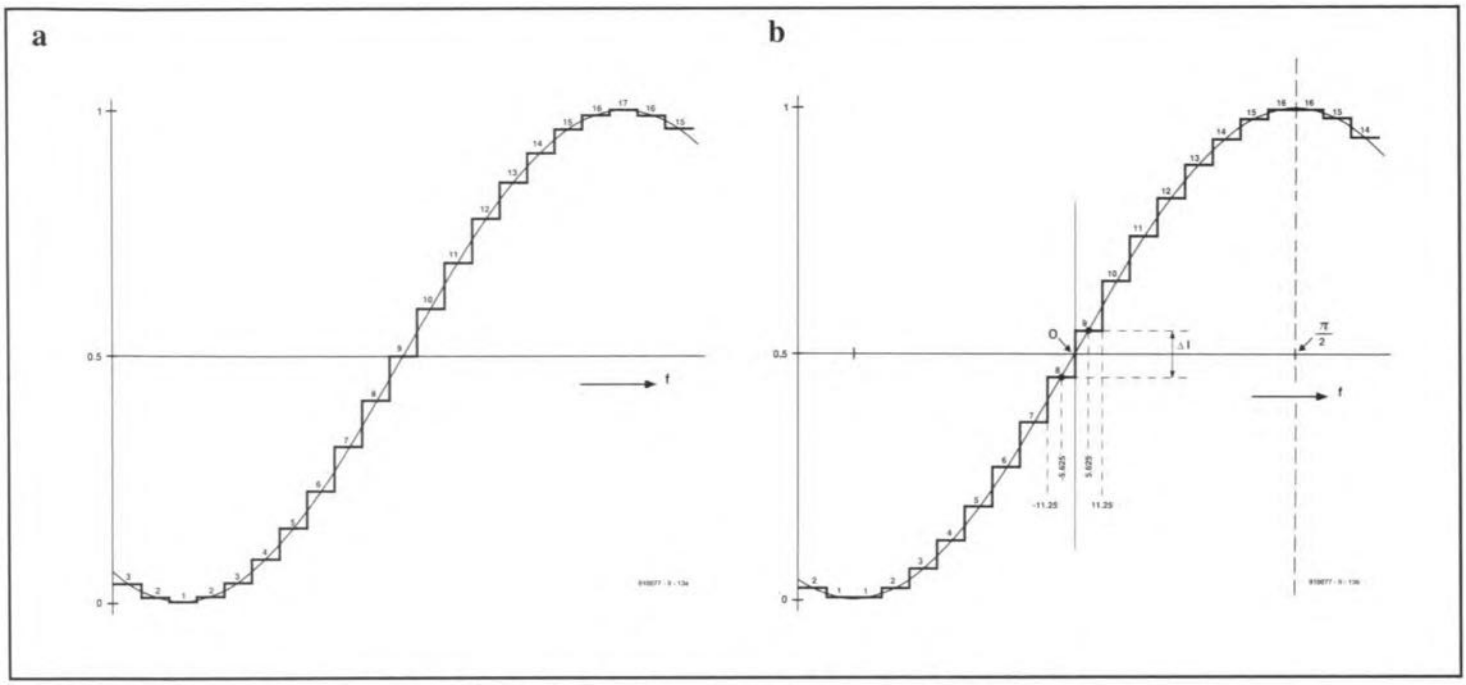


Fig. 15. Illustrating the two methods discussed to build up a sine wave from stepped voltages.

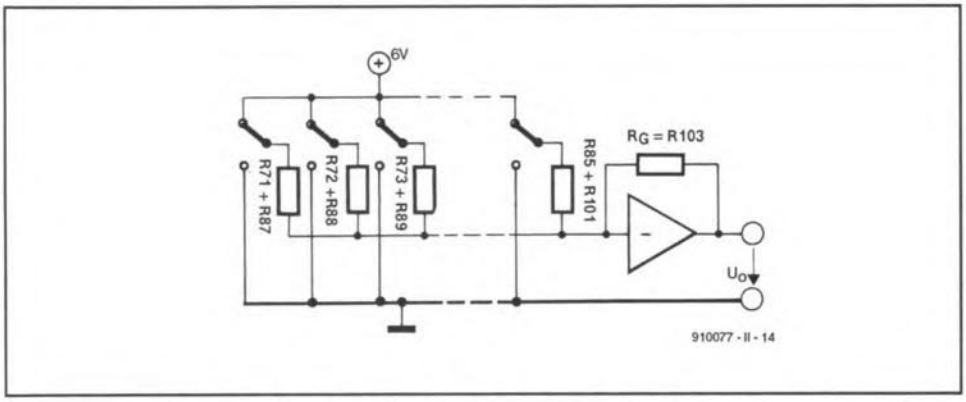


Fig. 16. Illustrating the fundamental operation of the digital-to-analogue converter.

Table 1

Data for computing the resistance networks in the digital-to-analogue converter

n	α_n	$\sin\alpha_n$	$\sin\alpha_n - \sin\alpha_{n-1}$	R_n
8	–5.625	–0.0980		
			0.1960	48 621.23
9	5.625	0.0980		
			0.1923	49 573.78
10	16.875	0.2903		
			0.1811	52 627.25
11	28.125	0.4714		
			0.1630	58 476.26
12	39.375	0.6344		
			0.1386	68 760.81
13	50.625	0.7730		
			0.1089	87 515.91
14	61.875	0.88119		
			0.0750	127 053.40
15	73.125	0.9569		
			0.0382	249 224.20
16	84.375	0.9952		
			0	
17	95.625	0.9952		

sen to ensure that the total current through the resistors is translated into a stepped output voltage as shown in Fig. 15. The computation of the resistance values is not simple, since more than one solution is possible.

The first method is also the most obvious: divide the sine wave into 32 equal parts, so that maximum and minimum values for the harmonic function are obtained. That means that 17 discrete values are required as shown in Fig. 15a. Fourier analysis shows that this method results in relatively high-level second and third harmonics.

An alternative method, used in the present design, is shown diagrammatically in Fig. 15b. It is based on the symmetry of a sine wave around the $\pi/2$ (90°) line. To the left and the right of this line, the corresponding steps are identical. Although the minimum and maximum values of the sine wave are not reached exactly, only a 16-step D–A converter is needed. Moreover, although the 31st and 33rd harmonic have roughly the same amplitude as those arising with the first method, the 2nd and 3rd harmonic are virtually absent.

The fundamental circuit for the second method is shown in Fig. 16. The maximum voltage is present when all resistors are connected to the 6 V source (high) and the minimum when all are at earth potential (low). In this method, resistors R_{86} and R_{102} in Fig. 17 are not used.

The computation of the resistance values is begun at a zero crossing (0°) of the sine wave. Then, one half of the resistors is at 6 V and the other half at 0 V. As an example, resistors R_{78} and R_{94} will be computed. First, the difference between the actual and the next higher value must be ascertained. After that it is only necessary to calculate the *additional* current that flows through the next higher resistance.

First, the period is divided into 32 equal intervals: 360°/32=11.25°. From Fig. 15b, it is evident that the level of the output voltage between 0° and 11.25° must be the same

as the instantaneous value at 5.625°. Next, the sine of the angles α_n=5.625° and α_{n-1}=–5.625° is computed and the difference $\sin\alpha_n - \sin\alpha_{n-1}$ established. That difference is in direct proportion to the value of the resistance, that is, $R_{78}+R_{94}$. In the above, n is the harmonic-number.

The resistance is calculated in the manner used for an inverting opamp:

$$R_n = R_G U_{ref} / (\sin\alpha_n - \sin\alpha_{n-1}).$$

In the denominator, the value 0.196 (as given in Table 1) is substituted and multiplied by 1.4 (to obtain the r.m.s. value). Thus,

$$R_{78}+R_{94} = 2224\times6/0.196\times1.4 = 48\,621.23\ \Omega.$$

This value is roughly equal to preferred (E96) resistors of 47.5 kΩ and 1.1 kΩ in series. The small difference of just over 20 Ω is useful since the output resistance of the shift registers is 20–30 Ω. The higher resistance value (0.1%!) must be just *below* the nearest preferred value in the series. Table 1 gives the resistance values from the zero crossing up to the peak of the sine wave.

Since the sine wave is not only symmetrical around the π/2 line, but also with respect to the x-axis, the steps (1–8) in the negative half of the sine wave are identical to the corresponding ones in the positive half. It is, therefore, only necessary to compute the values for a quarter wave (π/2)—see the values of the appropriate resistors in Fig. 17. Note that the arrangement ensures that the minimum and maximum values of the output voltage remain constant for the duration of two clock pulses.

Operational amplifier IC_{34} not only converts the current into a corresponding voltage, but also ensures that the 'zero' line is 1.2–1.8 V (set with P_1) above earth potential, so that a clean, symmetrical sine wave with an r.m.s. value of about 1 V is obtained.
The amplifier is a BiFET Type AD711, which is characterized by a slew rate of 16 V/µs, low off-set voltage, low drift, good bandwidth-gain product (3 MHz at unity gain) and above all by an excellent transient response of ±0.001% in 1 µs. Capacitors C_{61} and C_{62} remove any residual r.f. components from the signal and so ensure phase stability of the amplifier.

Locked filter

The filter consists of ten fourth-order low-pass sections, of which two are used for each decadic range. The discrete design offers real advantages as far as the harmonic spectrum is concerned over a simple switched filter with direct input of the clock pulses. The *RC* elements are switched on and off by analogue multiplexers Type 74HC4053, which have a very low transfer resistance. Each of the filter sections is buffered by a Type AD712 opamp.

The filter sections are fed with signals D1–D4 and the output of level comparator IC_{17}. It can be seen from Fig. 18 that the relevant section is active only when the corresponding decadic range D1–D4 is selected. The other sections are then short-circuited

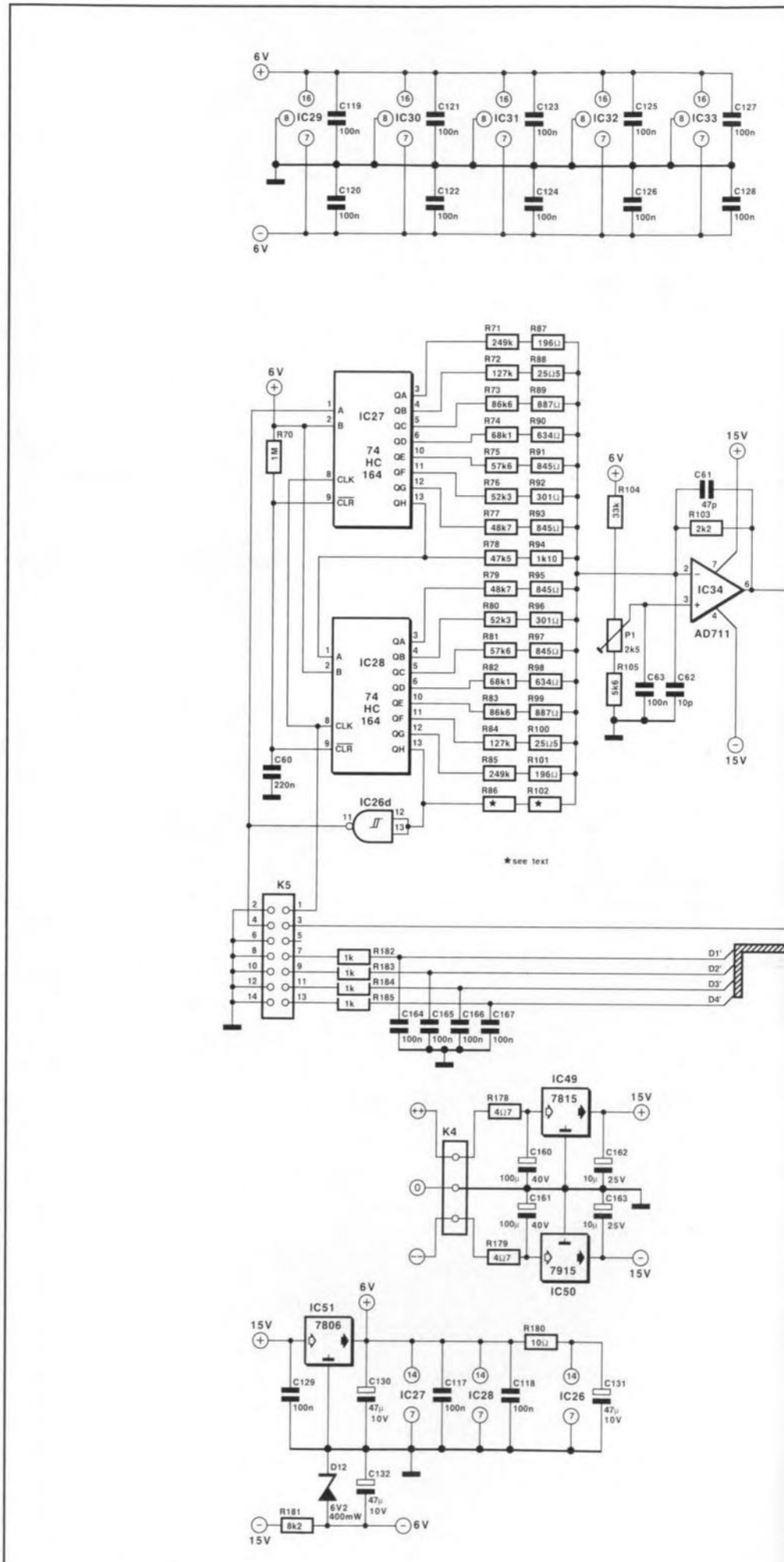
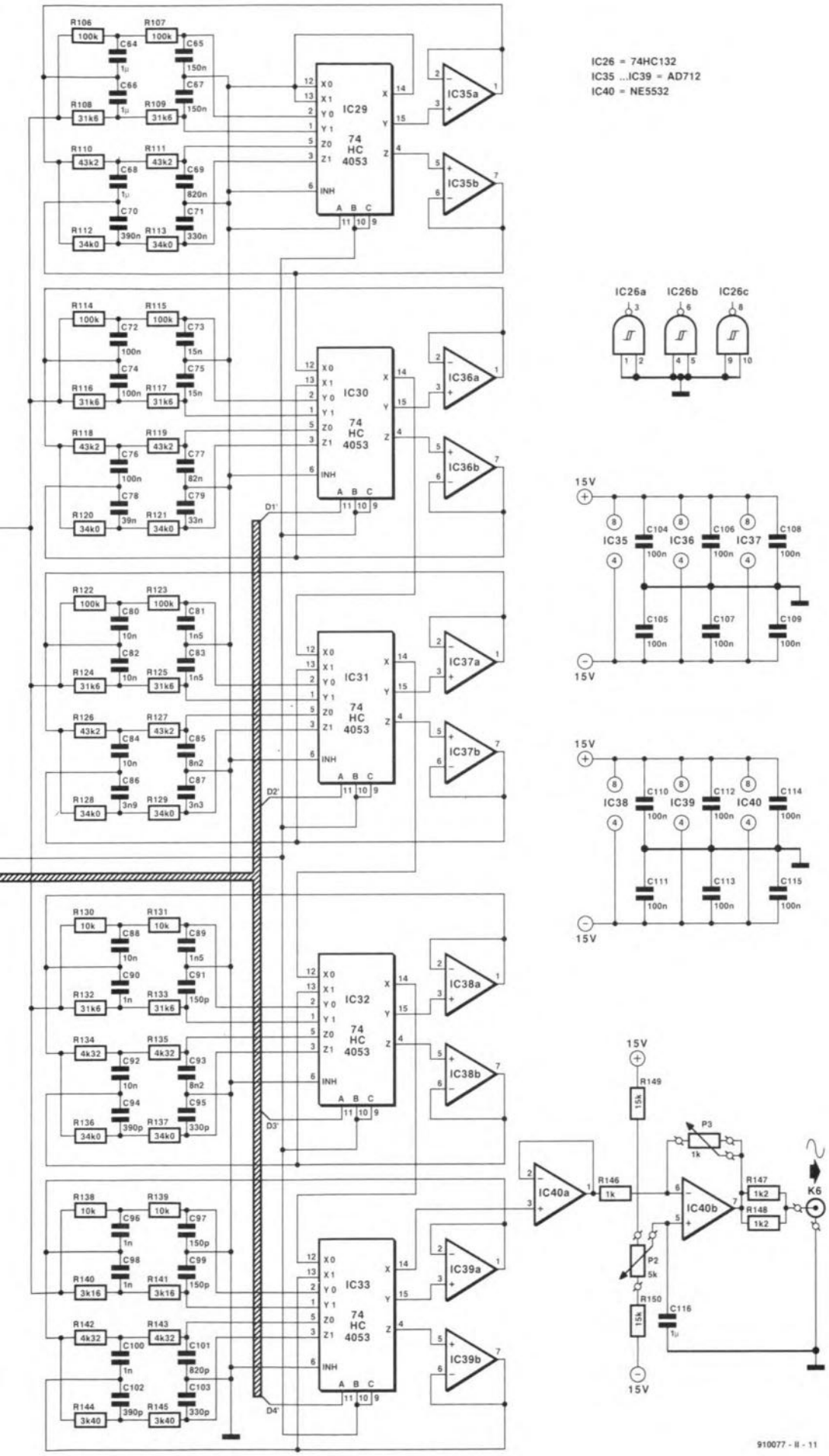


Fig. 17. Circuit diagram of the sine wave converter.


R106 100k
R107 100k
C64 1µ
C65 150n
C66 1µ
C67 150n
R108 31k6
R109 31k6
R110 43k2
R111 43k2
C68 1µ
C69 820n
C70 390n
C71
R112 34k0
R113 34k0
IC29
74 HC 4053
IC35a
IC35b
R114 100k
R115 100k
C72 100n
C73 15n
C74 100n
C75 15n
R116 31k6
R117 31k6
R118 43k2
R119 43k2
C76 100n
C77 82n
C78 39n
C79
R120 34k0
R121 34k0
IC30
74 HC 4053
IC36a
IC36b
D1'
R122 100k
R123 100k
C80 10n
C81 1n5
C82 10n
C83 1n5
R124 31k6
R125 31k6
R126 43k2
R127 43k2
C84 10n
C85 8n2
C86 3n9
C87
R128 34k0
R129 34k0
IC31
74 HC 4053
IC37a
IC37b
D2'
R130 10k
R131 10k
C88 10n
C89 1n5
C90 1n
C91 150p
R132 31k6
R133 31k6
R134 4k32
R135 4k32
C92 10n
C93 8n2
C94 390p
C95
R136 34k0
R137 34k0
IC32
74 HC 4053
IC38a
IC38b
D3'
R138 10k
R139 10k
C96 1n
C97 150p
C98 1n
C99 150p
R140 3k16
R141 3k16
R142 4k32
R143 4k32
C100 1n
C101 820p
C102 390p
C103
R144 3k40
R145 3k40
IC33
74 HC 4053
IC39a
IC39b
D4'
IC26 = 74HC132
IC35 ...IC39 = AD712
IC40 = NE5532
IC26a
IC26b
IC26c
15V
IC35
IC36
IC37
C104 100n
C105 100n
C106 100n
C107 100n
C108 100n
C109 100n
15V
IC38
IC39
IC40
C110 100n
C111 100n
C112 100n
C113 100n
C114 100n
C115 100n
15V
IC40a
R146 1k
R149 15k
P3 1k
IC40b
R147 1k2
R148 1k2
K6
P2 5k
R150 15k
C116 1µ
15V
910077 - II - 11

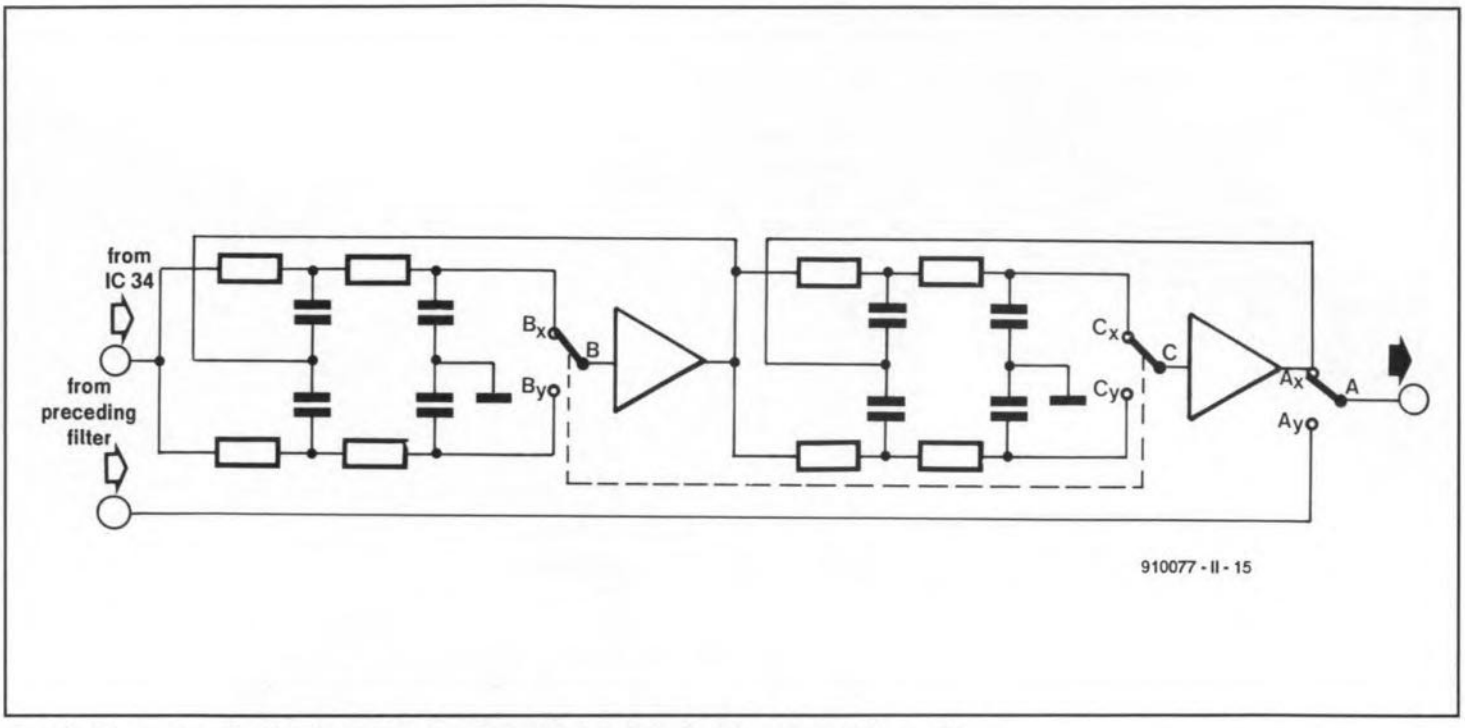


Fig. 18. Illustrating the fundamental operation of one of the five two-stage filter sections.

by switch A. The section for the lowest range is, however, always in circuit and, therefore, does not need signal D0. The other two switched inputs of the analogue circuit are strapped together.

When the ratio is lower than 3 200 (that is, when the frequency of the output signal is at the lower side of the decadic range), *RC* networks with different cut-off frequencies are switched in. In that way, the filter has an own frequency limit for the ranges 1–√10 and √10–10 (√10≈3.2).

The main function of the filter is attenuating the harmonics. Theoretically, only the 31st and 33rd harmonics are significant. The 31st is 30 dB below the fundamental and is attenuated by a further 70 dB by the filter, so that ultimately it is –100 dB with respect to the output sine wave.

Unfortunately, the cut-off frequencies of the filter have to be calculated for the lowest signal frequency of the decadic range. This means that at higher frequencies the fundamental frequency may be attenuated by about 0.7 dB, owing to an inherent property of the Butterworth design used. This attenuation may be accentuated by the tolerances of the components. The top of the filter characteristic, therefore, has a ripple (≥ 0.7 dB). This may be remedied by using higher cut-off frequencies, which increases the distortion, or using a different filter design, for example, Chebishev with 0.1 dB ripple, which requires high-tolerance (that is, more expensive) components. Table 2 gives component values for a Butterworth filter with higher cut-off frequencies, which give an attenuation of the 31st harmonic of only 50 dB instead of 70 dB, but which guarantee a ripple of ≤0.05 dB.

The output stage, IC_{40}, uses the well-known Type NE5532 dual opamp. One part, IC_{40a}, functions as a simple impedance converter to decouple the filter. The other part, IC_{40b}, operates as an inverting amplifier. The off-set voltage can be set between –4.75 V and +4.75 V with P_2.

The amplitude of the sine wave output can be set to 0–1 V with P_3. If a higher output level is required, P_3 can be replaced by a 2.2 kΩ type. The value of R_{146} should not be reduced. Also, at higher amplification, it may be necessary to limit the off-set range by increasing the values of R_{149} and R_{150}.

Rectangular and triangular waveform converter

The rectangular / triangular converter, whose circuit diagram is given in Fig. 19, is controlled by the clock from the sine wave converter that enters the circuit via pin 4 of K_8. That connecter also feeds signals D0–D4 (containing information on the selected decadic range) to the converter.

The clock signal is applied to the non-inverting input of opamp IC_{42b}, which transforms the asymmetrical 0–6 V to a symmetrical rectangular signal (±15 V).

Circuit IC_{42b} is one section of a dual operational amplifier Type OP260. This is a rather special device that operates with negative current feedback—see Fig. 20. The inverting 'input' of this section is, in reality, the low-resistance output of a buffer amplifier, whose input is connected to the non-inverting input of the opamp. If the voltage at this input rises, the current through R_1 increases. Since the current drives an impedance converter, the output voltage also rises (in proportion to the increase in current). Consequently,

Table 2

Component values for higher cut-off frequencies

R106 = 100 kΩ	R107 = 113 kΩ	C64 = 680 nF	C65 = 100 nF
R108 = 31.6 kΩ	R109 = 35.7 kΩ	C66 = 680 nF	C67 = 100 nF
R110 = 37.4 kΩ	R111 = 38.3 kΩ	C68 = 820 nF	C69 = 680 nF
R112 = 14.3 kΩ	R113 = 14.7 kΩ	C70 = 680 nF	C71 = 560 nF
R114 = 100 kΩ	R115 = 113 kΩ	C72 = 68 nF	C73 = 10 nF
R116 = 31.6 kΩ	R117 = 35.7 kΩ	C74 = 68 nF	C75 = 10 nF
R118 = 37.4 kΩ	R119 = 38.3 kΩ	C76 = 82 nF	C77 = 68 nF
R120 = 14.3 kΩ	R121 = 14.7 kΩ	C78 = 68 nF	C79 = 56 nF
R122 = 100 kΩ	R123 = 113 kΩ	C80 = 6.8 nF	C81 = 1 nF
R124 = 31.6 kΩ	R125 = 35.7 kΩ	C82 = 6.8 nF	C83 = 1 nF
R126 = 37.4 kΩ	R127 = 38.3 kΩ	C84 = 8.2 nF	C85 = 6.8 nF
R128 = 14.3 kΩ	R129 = 14.7 kΩ	C86 = 6.8 nF	C87 = 5.6 nF
R130 = 10.0 kΩ	R131 = 11.3 kΩ	C88 = 6.8 nF	C89 = 1 nF
R132 = 31.6 kΩ	R133 = 35.7 kΩ	C90 = 680 nF	C91 = 100 pF
R134 = 3.74 kΩ	R135 = 3.83 kΩ	C92 = 8.2 nF	C93 = 6.8 nF
R136 = 14.3 kΩ	R137 = 14.7 kΩ	C94 = 680 pF	C95 = 560 pF
R138 = 10.0 kΩ	R139 = 11.3 kΩ	C96 = 680 pF	C97 = 100 pF
R140 = 3.09 kΩ	R141 = 3.40 kΩ	C98 = 680 pF	C99 = 100 pF
R142 = 3.74 kΩ	R143 = 3.83 kΩ	C100 = 820 pF	C101 = 680 pF
R144 = 1.43 kΩ	R145 = 1.50 kΩ	C102 = 680 pF	C103 = 560 pF

the current through feedback resistor R_2 also increases and this will result in an equilibrium in the current through the buffer amplifier. The OP260 thus operates with a very small buffer current. The design has the important advantage over conventional opamps of a very fast slew rate: >1000 V/µs!

However, the operation is not entirely symmetrical as far as slope and amplitude are concerned. This is remedied by P_4–R_{152}, which make the signal symmetrical, and R_{167} in conjunction with D_{18}–D_{21} which equalizes the negative and positive halves of the signal. This arrangement ensures that the high slew rate is retained at very low signal levels.

The rectangular signal is available at relay contact re_1.

The rectangular signal at the output of IC_{42b} is applied to operational transconductance amplifier (OTA) IC_{41a} via R_{154}. This amplifier has a slew rate of 125 V/µs; its operating point is set with P_6. Because of the current source at its output (which sets an OTA apart from a 'normal' opamp), the OTA functions as a variable resistance. This means that in conjunction with a capacitor, C_{146}–C_{149}, it is readily made into an integrator. The four capacitors each belong to a different decadic range; they are selected by two analogue integrated switches, IC_{45} and IC_{46}. Capacitor C_{146} is connected between the OTA and buffer amplifier IC_{42a} when the D0 or D1 line is active; C_{147} when D2 is active; C_{148} when D3 is active; and C_{149} when D4 is active.

The use of a switch at either end of the capacitors is necessary, since the transfer resistance of the closed switch is not linear, but dependent on the supply voltage and the current through the switch. Switch IC_{45} is in

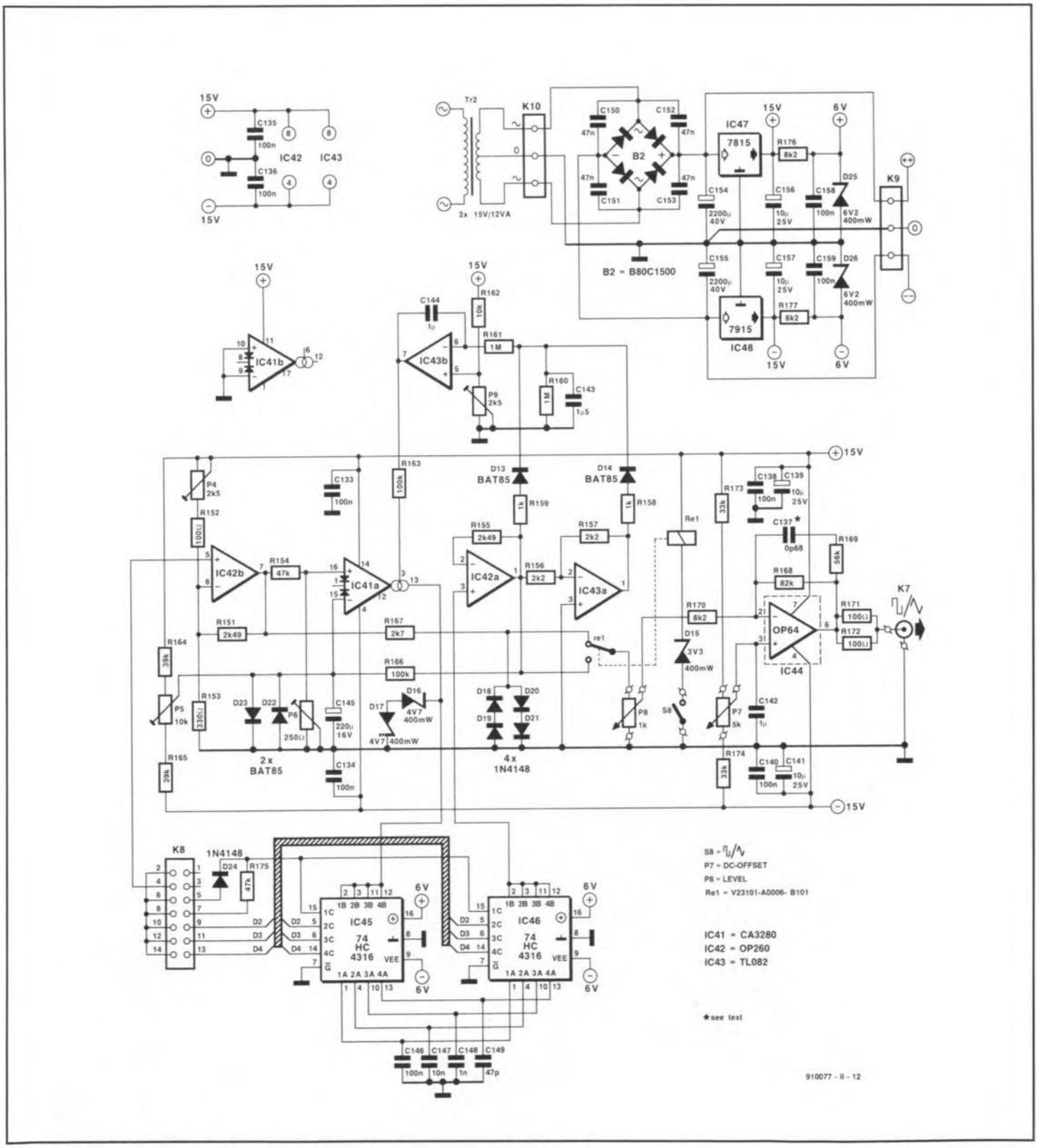


Fig. 19. Circuit diagram of the rectangular/triangular waveform converter.

series with the relevant capacitor and the current cource in the OTA. The current into the capacitor is independent of the transfer resistance of the switch. As far as the following opamp is concerned, only the *potential* across the capacitor is important. The transfer resistance of IC_{46} is in series with the very high input resistance of IC_{42a} and, therefore, has no relevance.

The signal at the output of IC_{42a} has a virtually perfect triangular waveform.

The two zener diodes, D_{16} and D_{17}, limit the output level of the OTA to 5.3 V (4.7 V zener voltage plus 0.6 V forward bias), so that the signal level at the switches cannot exceed the supply voltage to the ICs. The zener voltage can, if required, be chosen lower so as to reduce the regulating time of the OTA even further. An additional effect of the diodes is that, in combination with parasitic capacitances, they make necessary a reduction in the value of C_{149} from the calculated 100 pF to 47 pF.

A frequent problem with integrators is their inability to work with very small d.c. component. This is obviated by the d.c. feedback loop, R_{166}–C_{145}, between IC_{42a} and the OTA. This has the disadvantage, however, that there is no triangular signal available in the lowest decadic range of 1–10 Hz. (Our prototype delivered a triangular signal down to 3 Hz, but it was neither stable nor clean).

The level at the inverting input of IC_{41a} may be increased by a d.c. component derived from R_{164}–P_5–R_{165} to minimize an off-set voltage (of the order of a few millivolts), which, owing to the input current's dependence on the control current, may arise, particularly at the inverting input.

Amplitude control is provided by dual opamp IC_{43}, which is connected as a simple inverter. Its input and output signals (in antiphase!) are combined by D_{13} and D_{14} and the rectified output is smoothed by C_{143}. This capacitor is charged via R_{158} and R_{159} to the peak value of the triangular signal. The higher

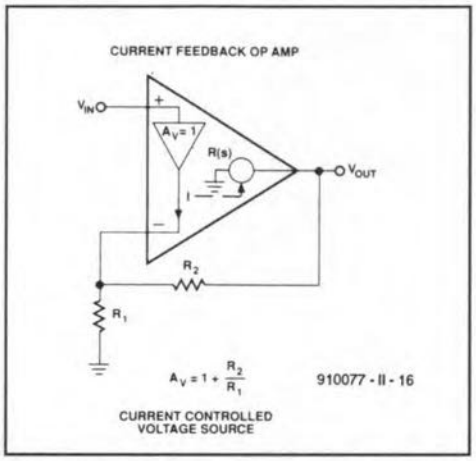


Fig. 20. Basic circuit of an opamp with current feedback.

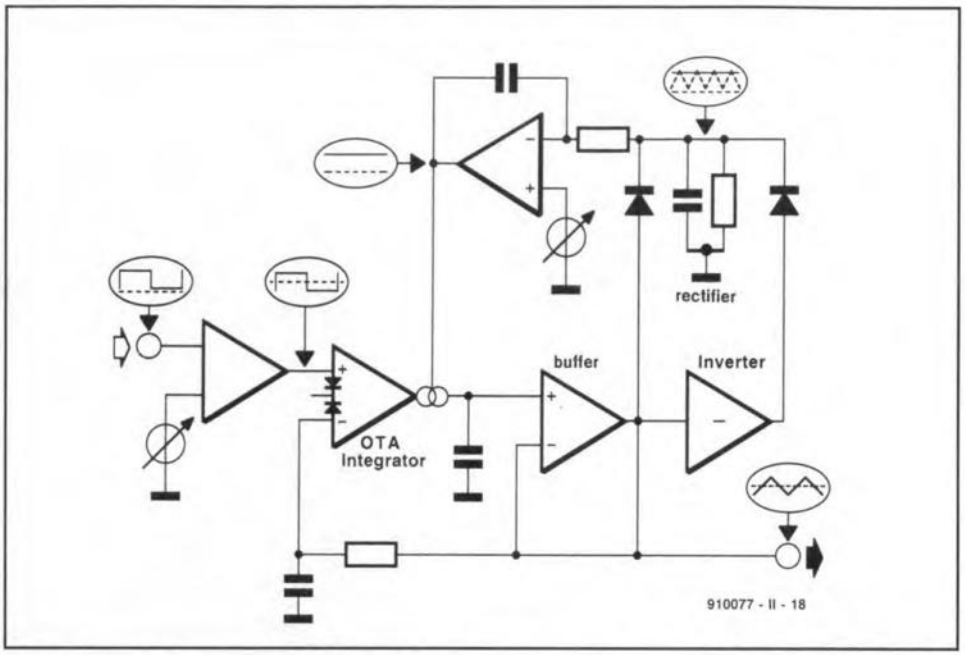


Fig. 21. Block schematic of the triangular-wave shaper, integrator and amplitude regulation.

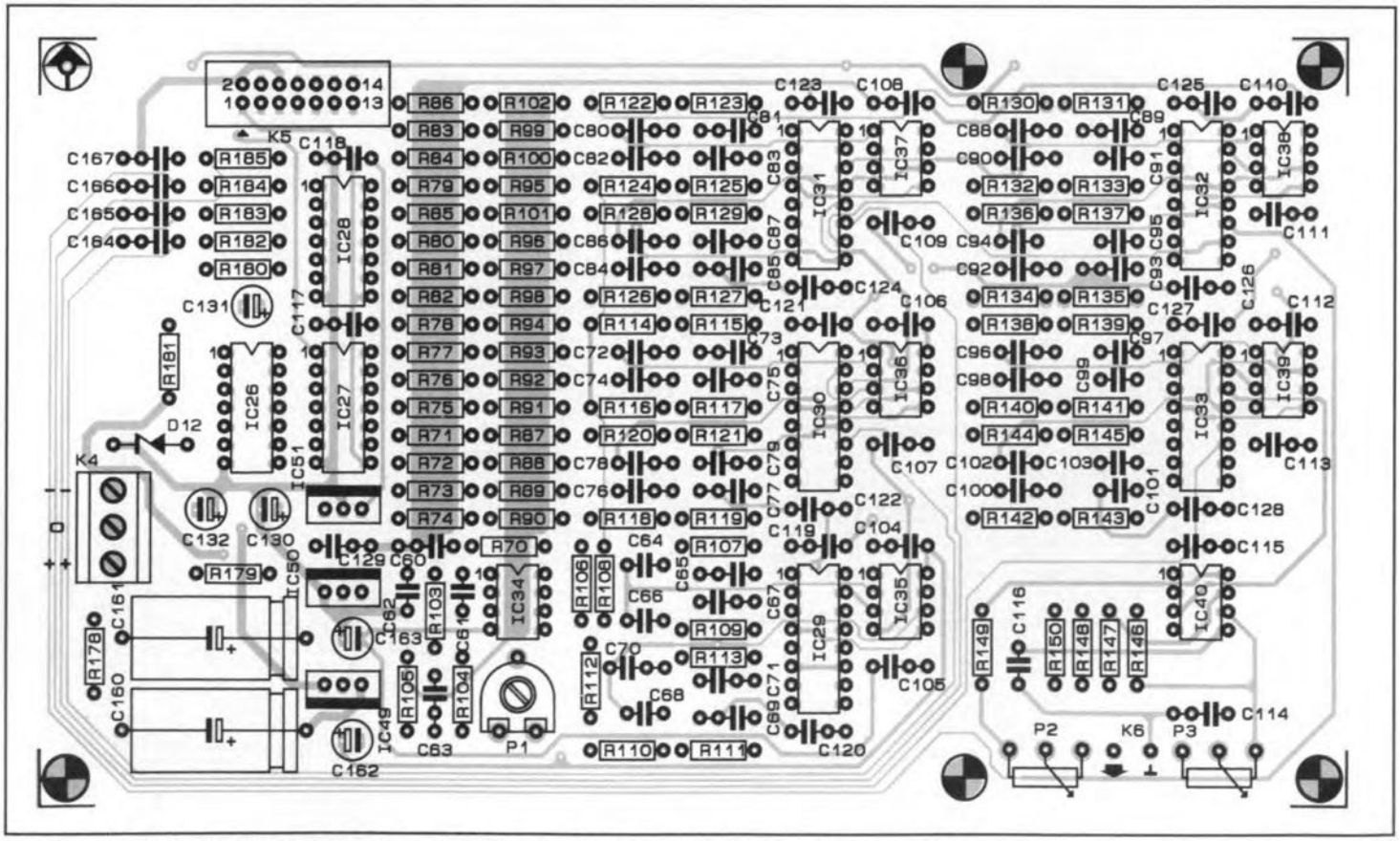


Fig. 22a. Printed-circuit board (component side) for the rectangular/triangular converter.

the potential across C_{143}, the smaller the output voltage (=control voltage for the OTA). Since IC_{43b} tends to keep the voltage at its inverting input, and thus that across C_{143}, equal to that at its non-inverting input, the setting of P_9 will ultimately determine the peak value of the triangular signal.

A disadvantage of this design is that the regulating time, that is, the time span before the amplitude control operates correctly again after a frequency change, is relatively long, because the time constant of the rectifier circuit has to be sufficiently long even at the lowest frequency. Since the regulating time also depends, to some degree, on the setting of P_6, calibrating the two controls properly takes a little practice. This will be reverted to in the next instalment of the article.

The output of buffer IC_{42a}, like that of amplifier IC_{42b}, is applied to relay Re_1. Which of the two signals, rectangular or triangular, is fed to output stage IC_{40}, depends on the setting of switch S_8.

The use of a relay obviates any problems with feedback of the rectangular/triangular signal to the sine wave signal (since both may be connected via one cable to the change-over switch on the front panel). One cable can, therefore, be used to take the signal to and from preset P_8, which sets the peak value of

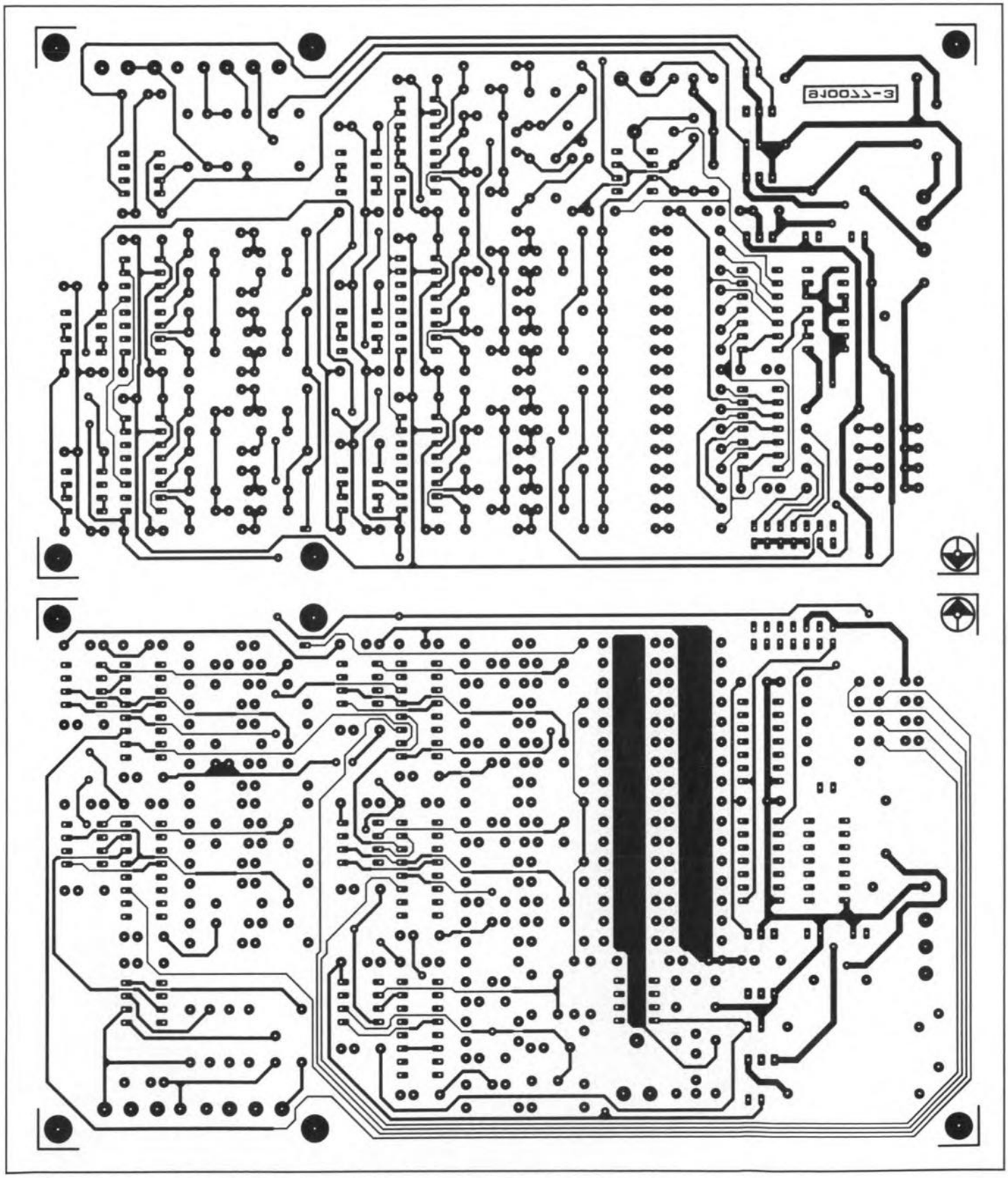


Fig. 22b. Printed-circuit board (track side and third overlay) for the rectangular/triangular converter.

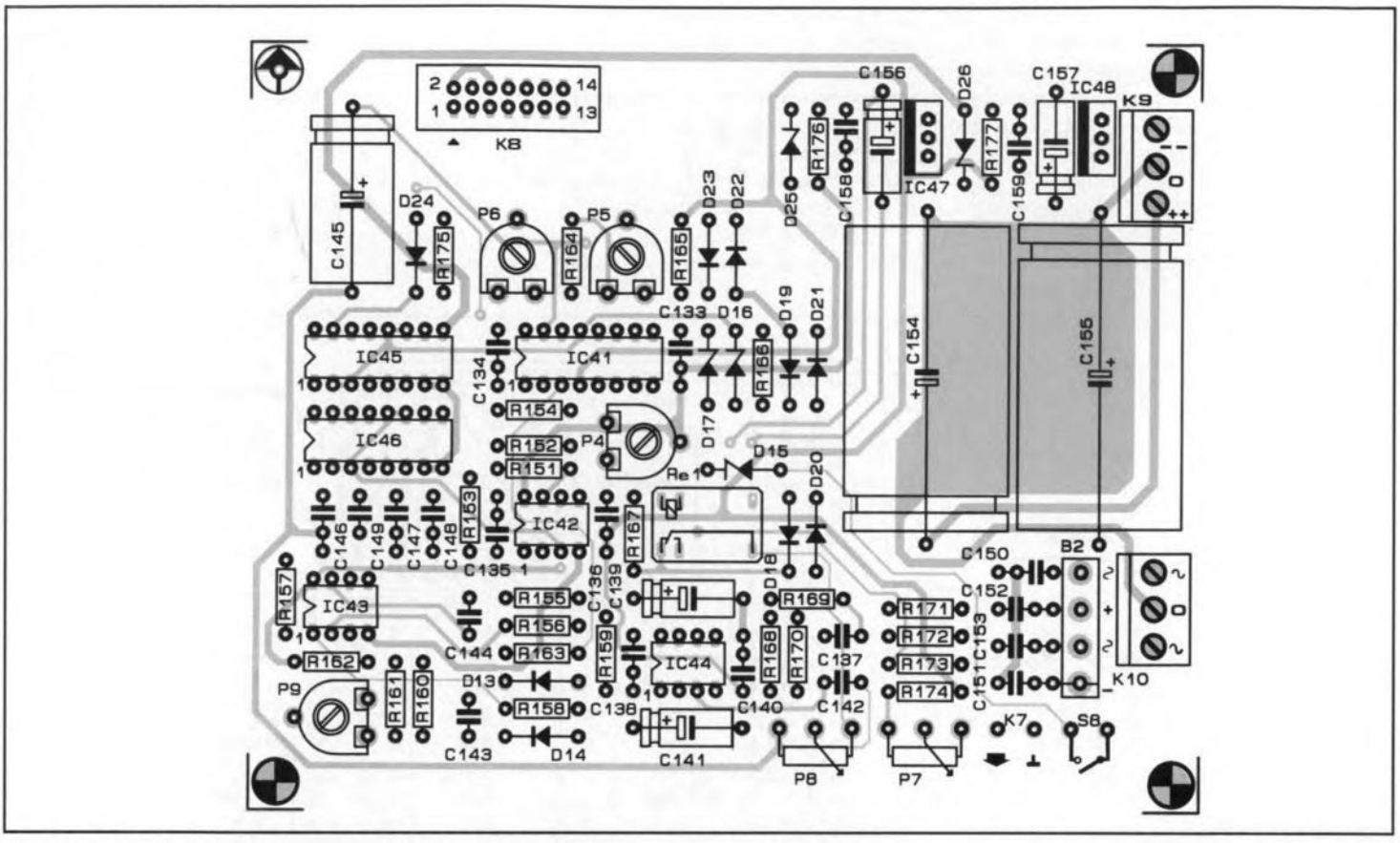


Fig. 23a. Printed-circuit board (component layout) for the sine wave converter.

PARTS LIST

Resistors:
R70, R160, R161 = 1 MΩ
R71, R85 = 249 kΩ, 0.1%
R72, R84 = 127 kΩ, 0.1%
R73, R83 = 86.6 kΩ, 0.1%
R74, R82 = 68.1 kΩ, 0.1%
R75, R81 = 57.6 kΩ, 0.1%
R76, R80 = 52.3 kΩ, 0.1%
R77, R79 = 48.7 kΩ, 0.1%
R78 = 47.5 kΩ, 0.1%
R86, R102 = see text
R87, R101 = 196 Ω, 1%
R88, R100 = 25.5 Ω, 1%
R89, R99 = 887 Ω, 1%
R90, R98 = 634 Ω, 1%
R91, R93, R95, R97 = 845 Ω, 1%
R92, R96 = 301 Ω, 1%
R94 = 1.1 kΩ, 1%
R103, R156, R157 = 2.2 kΩ
R104 = 33 kΩ
R105 = 5.6 kΩ
R106, R107, R114, R115, R122, R123 = 100 kΩ, 1%
R108, R109, R116, R117, R124, 125, R132, R133 = 31.6 kΩ, 1%
R110, R11, R118, R119, R126, R127 = 43.2 kΩ, 1%
R112, R113, R120, R121, R128, R129, R136, R137 = 34 kΩ, 1%
R130, R131, R138, R139 = 10 kΩ, 1%
R134, R135, R142, R143 = 4.32 kΩ, 1%
R140, R141 = 3.16 kΩ, 1%
R144, R145 = 3.4 kΩ, 1%
R146, R158, R159, R182–185 = 1 kΩ
R147, R148 = 1.2 kΩ
R149, R150 = 15 kΩ
R151, R155 = 2.49 kΩ, 1%
R152, R171, R172 = 100 Ω
R153 = 330 Ω
R154, R175 = 47 kΩ
R162 = 10 kΩ
R163, R166 = 100 kΩ
R164, R165 = 39 kΩ
R167 = 2.7 kΩ
R168 = 82 kΩ
R169 = 56 kΩ
R170, R176, R177, R181 = 8.2 kΩ
R173, R174 = 33 kΩ
R178, R179 = 4.7 Ω
R180 = 10 Ω
P1, P4, P9 = preset, 2.7 kΩ
P2, P7 = potentiometer, 5 kΩ, linear
P3 = potentiometer, 1 kΩ, log.
P5 = preset, 10 kΩ
P6 = preset, 250 kΩ
P8 = potentiometer, 1 kΩ, linear

Capacitors:
C60 = 220 nF
C61, C149 = 47 pF, polyester
C62 = 10 pF, polyester
C63, C72, C74, C76, C104–115, C119–129, C146 = 100 nF
C64, C66, C68, C116, C142, C144 = 1 µF
C65, C67 = 150 nF
C69 = 820 nF
C70 = 390 nF
C71 = 330 nF
C73, C75 = 15 nF
C77 = 82 nF
C78 = 39 nF
C79 = 33 nF
C80, C82, C84, C88, C92, C147 = 10 nF
C81, C83, C89 = 1.5 nF
C85, C93 = 8.2 nF
C86 = 3.9 nF
C87 = 3.3 nF
C90, C96, C98, C100, C148 = 1 nF
C91, C97, C99 = 150 pF, polyster
C94, C102 = 390 pF, polyester
C95, C103 = 330 pF, polyester
C101 = 820 pF, polyester
C117, C118, C133–136, C138, C140, C158, C159, C164–167 = 100 nF, ceramic
C130, C131 = 47 µF, 10 V, tantalum
C132 = 47 µF, 10 V, radial
C137 = see text
C139, C141, C156, C157 = 10 µF, 25 V
C143 = 1.5 µF
C145 = 220 µF, 16 V
C150–153 = 47 nF, ceramic
C154, C155 = 2200 µF, 40 V
C160, C161 = 100 µF, 40 V
C162, C163 = 10 µF, 25 V, radial

Semiconductors:
D12, D25, D26 = zener, 6.2 V, 400 mW
D13, D14, D22, D23 = BAT85
D15 = zener, 3.3 V, 400 mW
D16, D17 = zener, 4.7 V, 400 mW
D18–21, D24 = 1N4148
B2 = B80C1500
IC26 = 74HC132
IC27, IC28 = 74HC164
IC29–33 = 74HC4053
IC34 = AD711
IC35–39 = AD712
IC40 = NE5532
IC41 = CA3280
IC42 = OP260
IC43 = TL082 or TL072
IC44 = OP64
IC45, IC46 = 74HC4316
IC47, IC49 = 7815
IC48, IC50 = 7915
IC51 = 7806

Miscellaneous:
K4, K9, K10 = 3-way PCB connectors
K5, K8 = 14-way D-type plug
K6, K7 = BNC socket, insulated
Re1 = 12 V relay, 1 change-over contact
S8 = miniature on/off switch
Tr2 = mains transformer, 2×15 V, 12 VA
Heat sink for IC44 (e.g., Fischer ICK14/16B) [Dau UK Ltd, phone (0243) 553 031]
Enclosure, Telet LC970 (C-I Electronics, p.5)
PCB 910077-3
PCB 910077-4

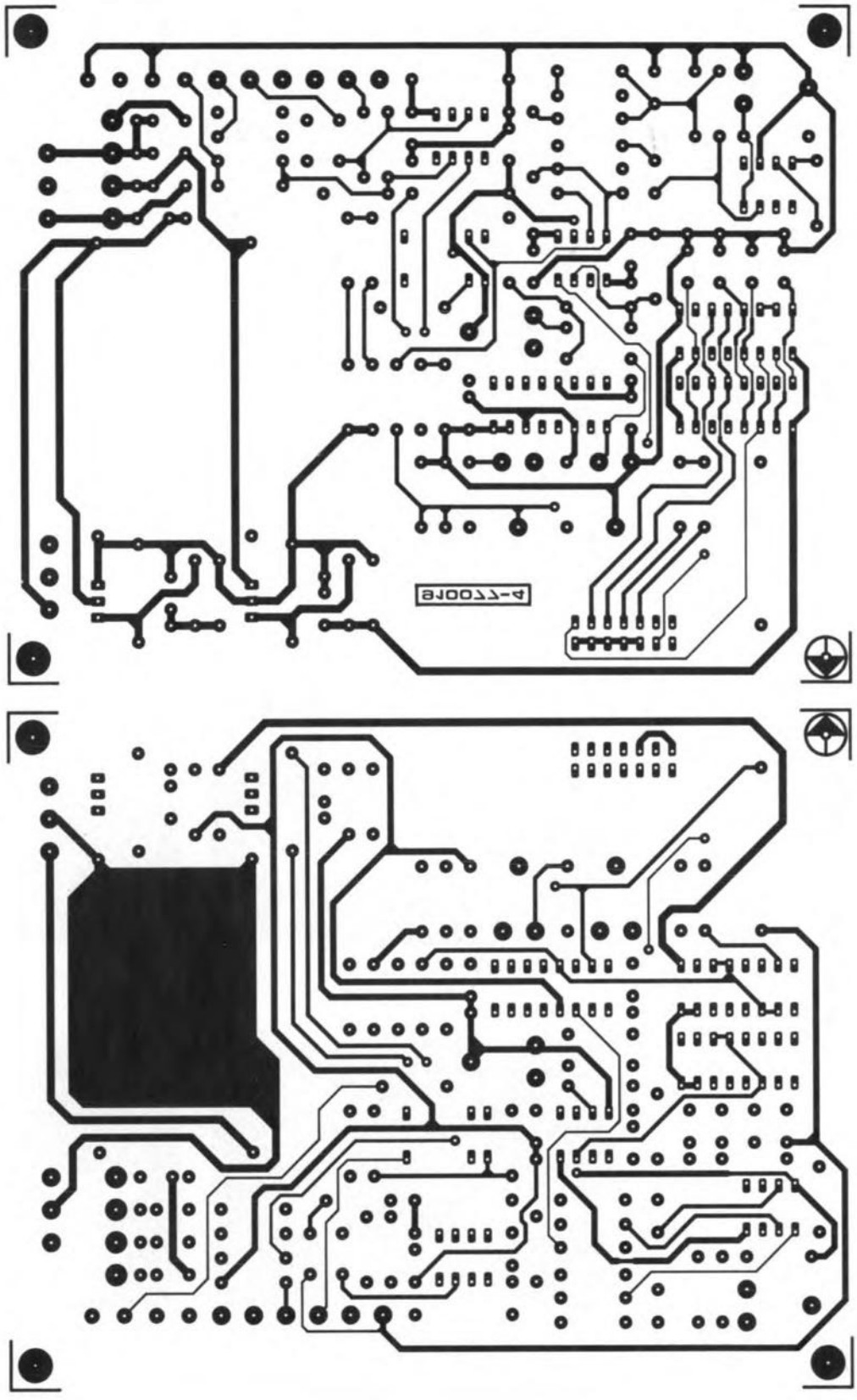


Fig. 23b. Printed-circuit board (track side and third overlay) for the sine wave converter.

the output.

The signal is amplified once more in IC_{44}. This opamp can provide a relatively high output current of ±80 mA at a slew rate of 130 V/µs, so that no difficulties arise with loads down to about 150 Ω. Since R_{171} and R_{172} fix the output resistance at 50 Ω, the minimum load resistance may be as low as 100 Ω. Note that the OP64 is *not* protected against short circuits and must be fitted on to a special heat sink (see parts list).

The OP64 tends to be overdriven by a rectangular signal. Network R_{169}–C_{137} in the feedback loop, therefore, reduces the amplification at high frequencies (that is, the 'corners' of the rectangular signal) slightly.

Capacitor C_{137} consists of two pieces of enamelled copper wire twisted together and cut to size as required.

The d.c. component of the output voltage, ±12 V, is set with P_7. ■

The third and final instalment of this article will appear in our Special Large Christmas issue.

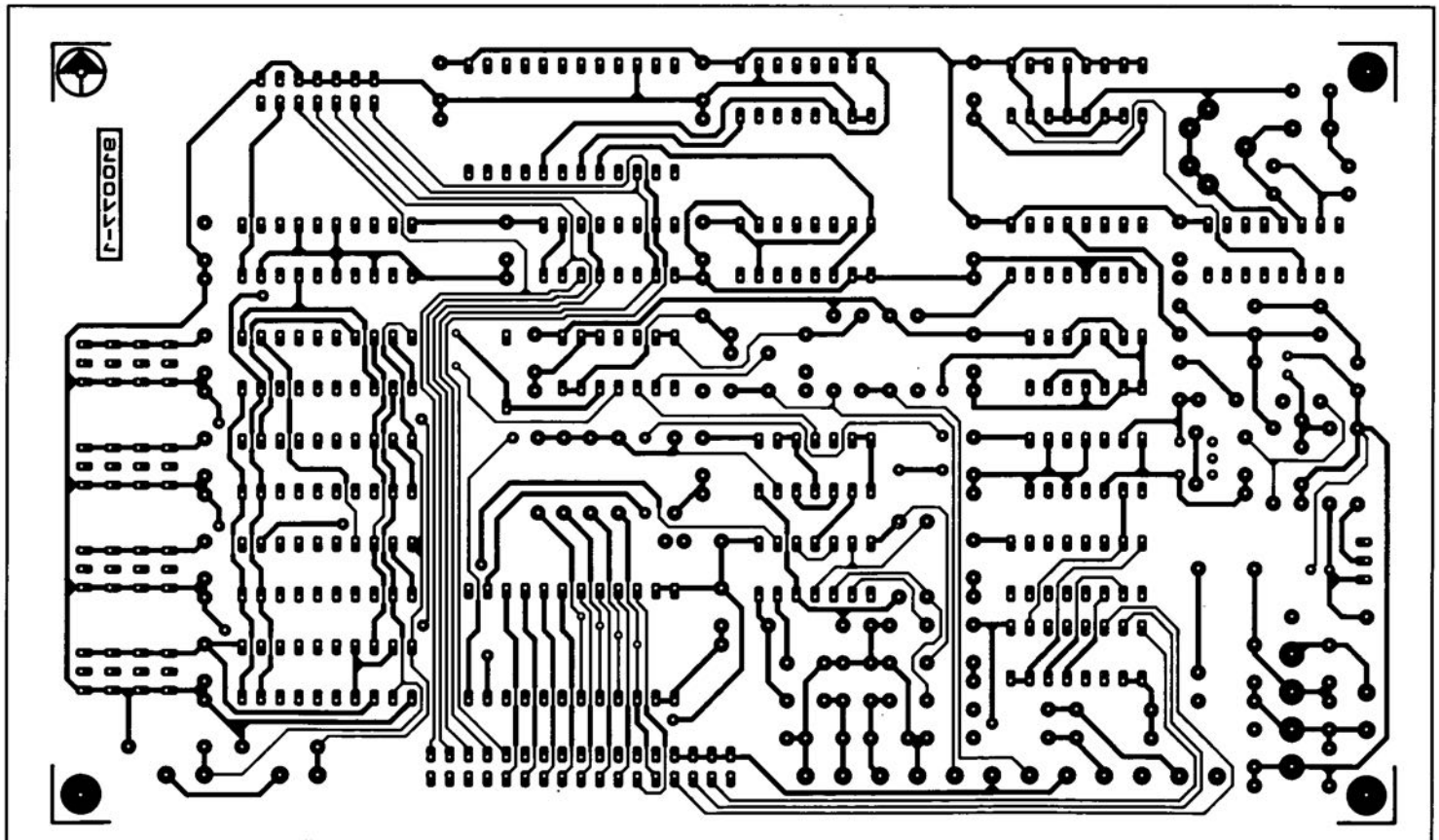


Fig. 14. Third overlay of the PCB for the digital section of the function generator (belongs to Fig. 7)

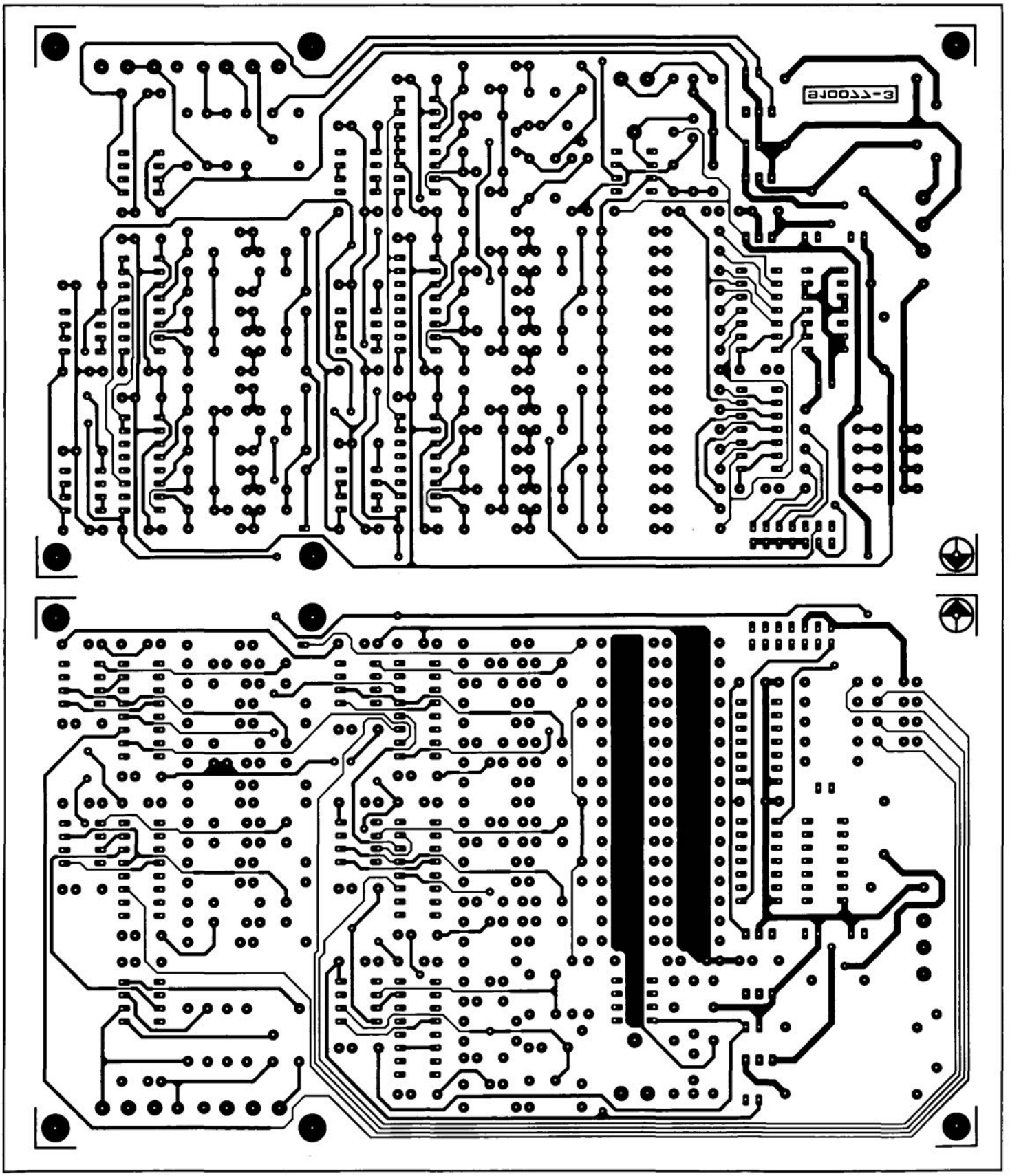


Fig. 22b. Printed-circuit board (track side and third overlay) for the rectangular/triangular converter.

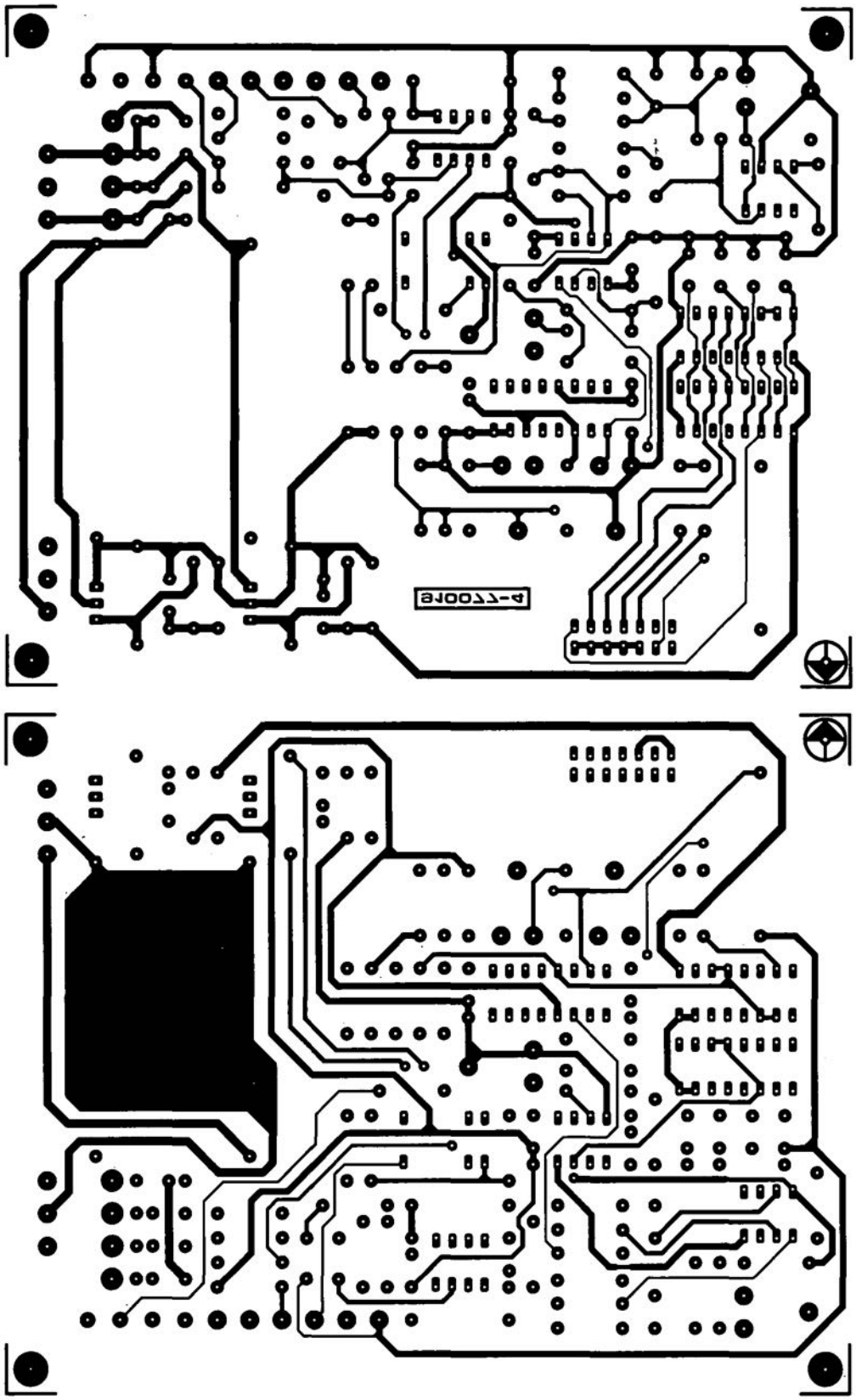


Fig. 23b. Printed-circuit board (track side and third overlay) for the sine wave converter.

PRODUCT MODELLING

by R.G. Evans

EVER since I made my first circuit (a crystal radio) some twenty years ago, I have faced the problem of packaging the finished circuit. The methods I will describe can sensibly replace the aluminium or diecast boxes, the 'project boxes' sold by many of the mail order outlets, and at the same time provide very realistic cases tailor-made to your projects requirements, looking just like (or sometimes better) than the 'real thing'. It is perhaps worth mentioning that I teach Design & Technology in a secondary school (ages 11-18), and that my colleagues and I use this technique with our pupils aged 14 and above. The outstanding results obtained by these beginners should spur many of the readers of this magazine on to have a go themselves.

Basic tools and materials

I mentioned that I work in a school which has workshops and power tools, but these facilities are by no means necessary. Most electronics enthusiasts will have the tools required for making their own project box:

- A 'stanley' type knife with a scoring blade (or grind your own from a blunt ordinary knife). If this is not available, a suitable tool can be a made from an old hacksaw blade suitably shaped and given a simple handle.
- A try square of any shape or size.
- A sanding board — any material that is flat will do, e.g., a piece of kitchen worktop, blockboard etc. It must be **flat**. To this glue a whole sheet of 120 grit 'wet or dry' silicon carbide paper, and leave it weighted down to dry.
- A workbench (kitchen table??) and, if possible, some form of vice,. e.g., a Workmate or a wood or metal vice.
- A selection of files, or at least **one** (fairly coarse and fairly fine will do).
- A tenon-saw, although with care an ordinary hacksaw will suffice.

Useful, but by no means essential:

- A wood plane of any type, a small bandsaw and a sanding wheel (photo 1 shows a useful assemblage of the above).

Hopefully, the reader will have at least some of the above in his or her possession. The next thing to do is to acquire the essentials from which to make the boxes. Polystyrene is the type of plastic to get hold of (not the expanded ceiling tile stuff) Any colour will do, and two thicknesses are needed: 1.0 mm and 3.0 mm. Combinations of these thicknesses will cover most of our needs. The other main requirement is a suitable solvent with the name **dichloromethane**, also known as **methylene chloride**. This is available from laboratory chemical suppliers, some model shops (under the name of Plastic Weld), and from EMA

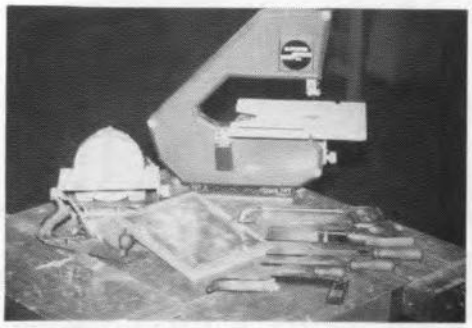


Fig. 1. Some of the basic tools you will need.

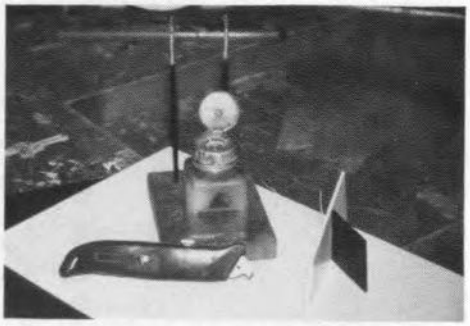


Fig. 2. The pump dispenser, a scoring knife and some plastic sheet.

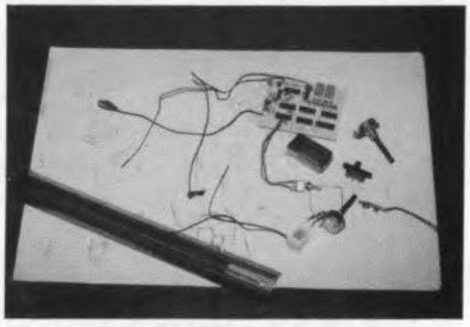


Fig. 3. Showing sensible planning of your work before you start.

Fig. 4. Showing correct use of a safety ruler, scoring knife and the plastic sheet.

Fig. 5. Showing how to 'snap' the plastic cleanly over the edge of a bench.

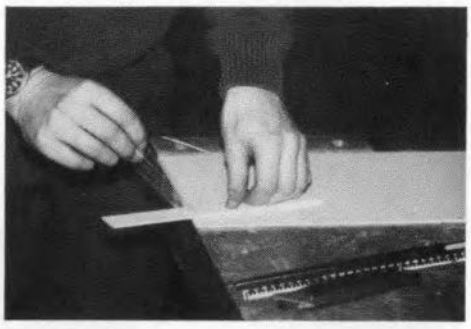


Fig. 6. Showing the removal of the protective plastic film before gluing.

Fig. 7. Edges may be squared up using a conventional wood plane.

Fig. 8. Edges may be squared up on a sanding board with equal ease.

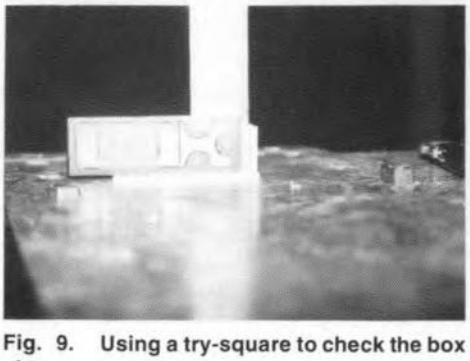


Fig. 9. Using a try-square to check the box shape.

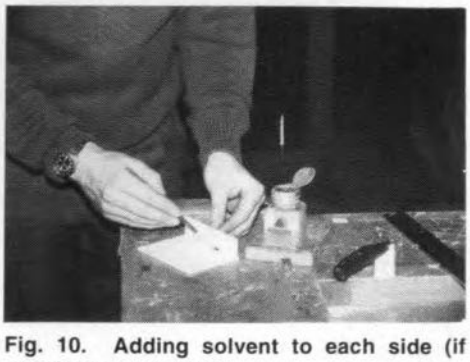


Fig. 10. Adding solvent to each side (if possible) of the joint.

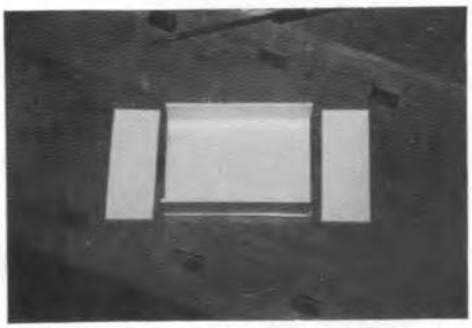


Fig. 11. Box with two sides, also showing slightly oversized end pieces.

Fig. 12. Using a sanding board to square up the box ends.

Fig. 13. A sanding wheel provides a quick alternative, but check its angle first!

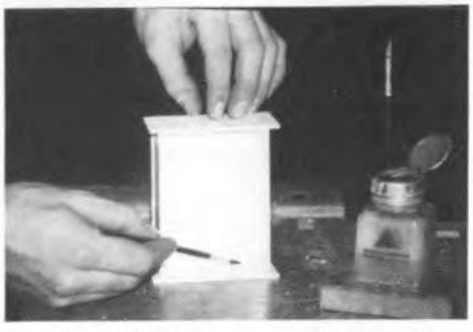


Fig. 14. Gluing the ends on to the box.

Fig. 15. Sanding the top of the box ready for the lid (shown upside down).

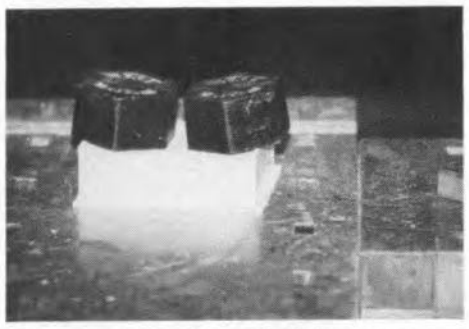


Fig. 16. After gluing the lid on, use some weights to keep it there for half an hour.

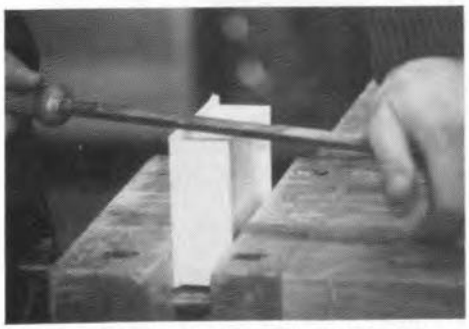


Fig. 17. Reducing the edges with a file — always work into the joint.

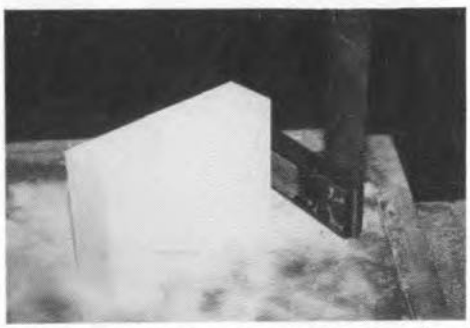


Fig. 18. A finished box, sanded smooth on all sides.

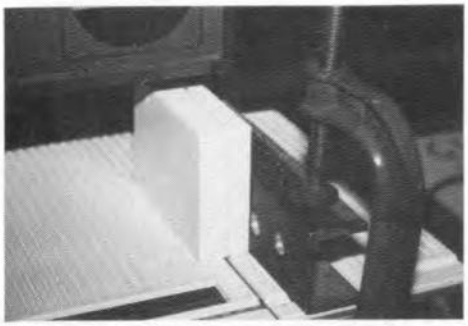


Fig. 19. Cutting the box on a band saw. Always use a fence!

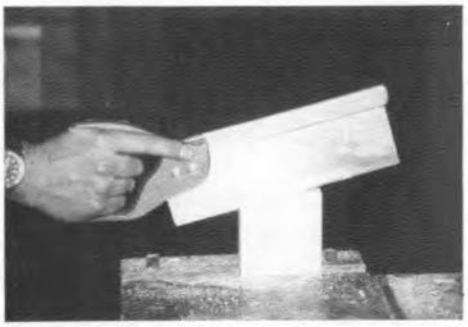


Fig. 20. With care, a tenon-saw can be used for the same task.

Model Supplies. The latter also supply a very neat pump dispenser which makes the use of the solvent much easier (see photo 2).

Planning

Having assembled the tools and materials, it is time to plan your box a little. I teach my students 'design based problem solving' which simply means that as much research and investigation should go into the generation of initial ideas as possible. There are several ways of packaging your circuit, and your first idea is unlikely to be the best. There are several things to consider, such as serviceability, replacement of battery, position and accessibility of the controls such as on/off switches, sensitivity adjustment and range switches. It is worth jotting down a few vital measurements at this stage (remember to leave plenty of room inside — I once had to squeeze a battery in a vice to get the lid on! Never again!), and to sketch a few ideas of the product (photo 3).

Box assembly

Once a few dimensions have been decided, construction can start. Mark out the base of the box (biro or pencil will suffice) on the 3-mm sheet of polystyrene. Cut it by using a ruler and a scoring knife (score to about ½ the plastic's thickness — photo 4). Place the scored line over the edge of a bench or table, and apply sharp downward pressure to both sides. The plastic will snap cleanly along the scored line (photo 5).

The secret of making these boxes lies in making good butt joints, for which a square edge is essential, and a little time spent here will make your job easier later on. Note that some polystyrene sheets have a protective layer of polythene on one or both sides. For our application, this layer should be peeled off (photo 6). Next, cut a strip of the required height, and twice the length of the box. Leave a few millimetres extra for squaring up. At this stage, only one long side of each piece will need squaring. Use a wood plane if one is available, or sand on the sanding board, taking care to keep it at 90° to the board as you do so (photos 7 and 8). Keep sanding until a uniform square edge is obtained.

Next, place this edge on top of the base in the required position, and hold it up to a set square (photo 9). Using a small paint brush (maximum size 5 mm), dip the bristles into the solvent (photo 10), and then run the brush along the inside of the joint. If it is a long joint, replenish the brush as necessary. Once the solvent has been applied, capillary action will put it into the joint area, and there is little to be gained by continued application of the solvent. If both sides of the joint are accessible, the solvent may be applied to both sides. Hold the two pieces together while ensuring that the joint is at 90° to the base.

After some 15 to 30 seconds, the joint will be capable of supporting itself, and the other side can be glued in a similar manner. Although there are several proprietary polystyrene cements on the market, none have the ease of use and speed of bonding offered by dichloromethane. Unlike other cements, however, dichloromethane is purely a solvent, and as such it does not have any gap filling properties. It is therefore well worth making sure that your butt joints are good fits for

best results. Gaps can be filled at a later stage, but it is a lot quicker and easier to get it right first time.

Leave the two sides and base to dry while you prepare the ends and lid of the box. This is where some planning will have paid off. For ease and speed of construction, it is a lot easier to overlap joints, and sand down after construction, than to get it all to fit first. The two ends need to overlap both sides and base (photo 11), so cut out some suitable pieces. As they will be glued onto the **end** of the sides and base, there is no need to give them square edges. Cut a lid out on the same basis, that is, overlap on both sides and ends.

By now the base and sides will be workable, and now is the time to square up the ends. Those of you with a disc sander will find this easy, although the plastic does tend to melt more than sand. Those with sanding boards only will have to carefully sand the ends square, taking care to avoid 'rocking', and consequent rounding of the box ends. This process can be made easier if (a) you did not leave that much spare in the first place (careful marking out!), and (b) if you drag the box across the board towards you, rather than attempting to work both ways (photos 12 and 13).

Once each end is square, the end pieces can be glued on as per the sides (photo 14). Here, no set square will be needed, and pressure can be applied by hand until the solvent 'bites'. Give both ends a chance to dry as the next stage will put them under strain!

Gripping the box firmly upside down, sand it backwards and forwards (and circular) on your sanding board, until an even top surface is obtained (full width of 3 mm all the way round — photo 15). At this point, the lid can be glued on with liberal application of solvent, as the inside will not be accessible.

Leave the box weighted down (photo 16), and forget about it for 12 hours or so. Whilst the solvent is drying completely, it is worth mentioning why the box needs leaving. Although the solvent sticks the plastic very quickly, and allows work to proceed, it does nevertheless cause softening of the plastic in joint areas, and if fine finishing of the box is attempted, 'plucking out' of this softened material will result, and there will be a depression left to fill later. Be patient!

Once the box is dry, it can be externally tidied up. Large amounts of plastic hanging over edges can be removed by using a sanding wheel, if available, or simply filed away (photo 17). People used to working with harder materials will find this plastic quick to file and shape. With only small lips remaining (less than 1 mm), the whole box can be sanded on the sanding board until each and every surface has been 'sanded' (including the middle of plain sheets, photo 18). This may seem a long process, but better results are obtained this way.

Back to the planning stage, and how the box will be divided. Thought needs to be given to fitting the controls, switches, displays, etc. It is preferable, but not essential, that they are all mounted in one half of the box, but for mains powered projects it may be preferable to fit the transformer and circuitry in the base, and have flying leads to the front panel controls. Plan ahead now to avoid disasters later!

Most project boxes can be cut around their height anywhere between ⅓ and ⅔ the total

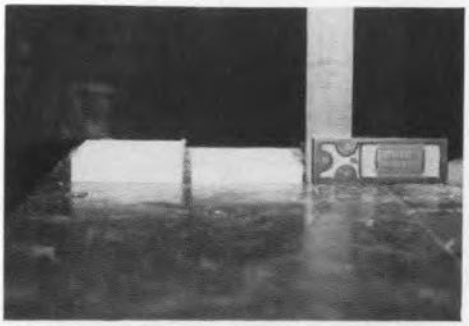


Fig. 21. You should now have two similar pieces of box. The heights can differ.

Fig. 22. Carefully sand the cut edges until they are free of saw marks.

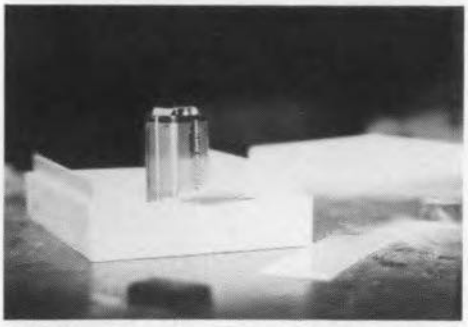


Fig. 23. The thin (1-mm) 'joining sheets' are shown resting in a box.

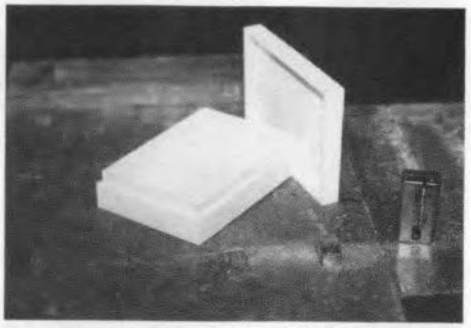


Fig. 24. All four thin strips fitted and glued.

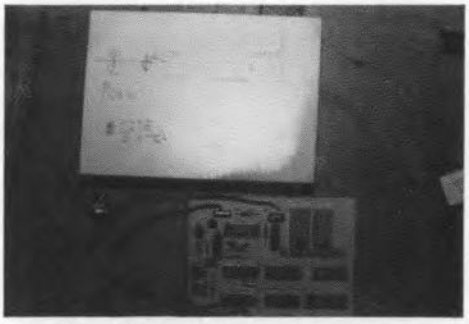


Fig. 25. Plan and mark out where your controls are going to be.

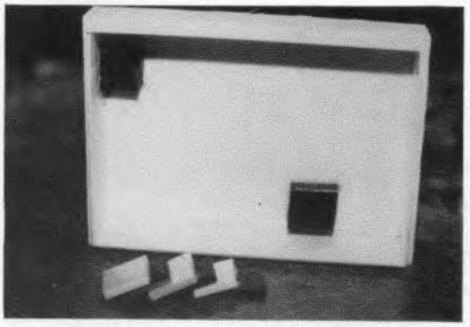


Fig. 26. Mounting pillars for PCBs are made by stacking up small squares.

Fig. 27. Radius the box edges, starting with a file, then with wet and dry paper.

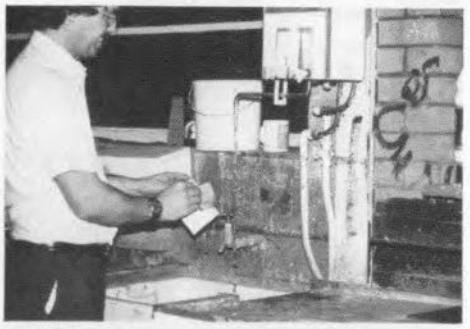


Fig. 28. Surface preparation is vital — use soap, water and wet or dry paper.

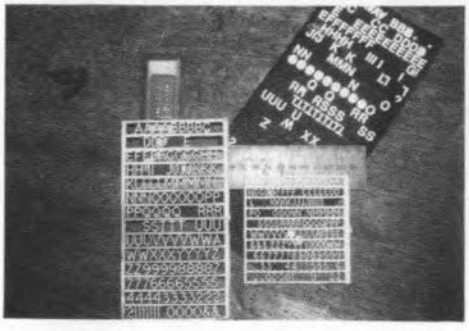


Fig. 29. There are two main types of lettering for surface detailing.

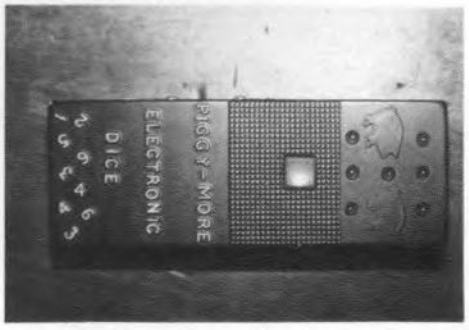


Fig. 30. A variety of effects can be achieved with relative ease.

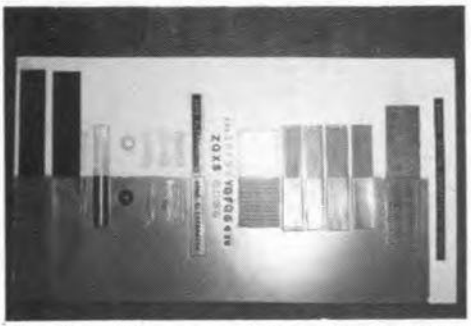


Fig. 31. All manner of 'things' will provide extra surface detail.

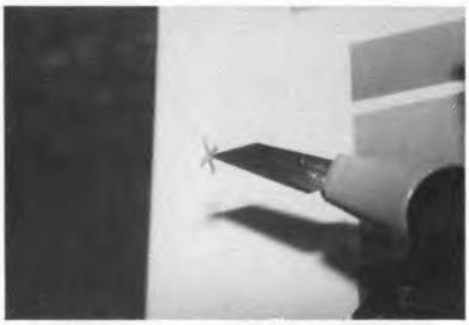


Fig. 32. Plasticard letters are easily picked up using the tip of a knife.

Fig. 33. A wide range of paper stickers are available.

Fig. 34. A range of suitable products to help finish your product.

Fig. 35. Small patches showing through are not a problem — smooth finish is vital.

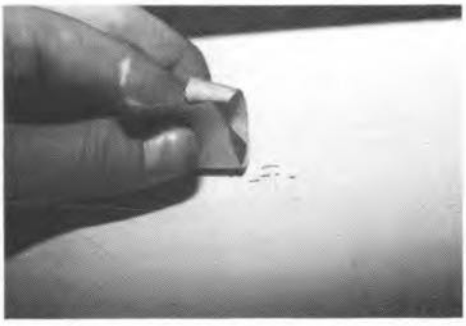


Fig. 36. Removing errant Letraset with a piece of masking tape.

height of the box. This is easily done with a small bandsaw, but take care and use a substantial fence to hold the box against (photo 19). Many boxes have been spoilt by the saw wandering off, so be careful! Those of you without a bandsaw will find that a tenon-saw (fairly fine toothed — see photo 20) will suffice, or failing that, a conventional hacksaw will work but may prove difficult to control directionally.

Assuming your box has now been cut into two (photo 21), the cut surfaces are sanded smooth on the sanding board once again, until any marks from the sawing have gone (photo 22). Take care to sand as evenly as possible, otherwise your box may develop a list. Using the 1-mm polystyrene sheet, cut a strip, or strips, of sufficient length and width to fit around the inside of the box, from the base up to nearly the full interior height. Using the solvent again, secure the two long sides first in the deeper part of the box, and then the two ends (photo 23). Squareness and close fits are not so important inside, and gaps for things like switches can be left in the thin strip. Leave all these to dry for 10 minutes or so. Then reassemble your box, and hopefully you should still have a reasonably square 'shape' (photo 24). If there are small discrepancies between the top and the bottom of the box, these can be sanded out on the sanding board before the next stage.

Fitting up

With the basic box finished, the fitting up can begin. Holes for switches, dials, controls, cables and the like should be added (photo 25). Inside the box, battery compartments can be fabricated quickly by using suitable pieces of plastic and solvent, as can PCB pillars made from small 'piles' of 3-mm plastic glued on top of each other (photo 26). The PCB and the pillars can then be drilled to suit suitable self-tappers which happily cut their own thread in the core diameter pilot holes. Please note that unlike acrylic (perspex), polystyrene does not take fine threads particularly well, so it is best to stick with self-tappers.

These pillars of material can also be used to good effect if you wish to 'sink' securing screws below the surface. In this way, results very similar to commercial injection moulding can be achieved. Simply build up a suitable thickness of material in the area that you wish the screw to be sunk (probably around 12 mm). Drill a hole of sufficient depth and diameter to clear the screw head (allowing for paint and perhaps screwdriver size). Drill a clearance hole right through to allow the self-tapper to sit in the recess so created.

Next, build up a suitable pilar on the opposite side of the box, to the required height for the self-tapper to screw into. Take care to get the pillar height correct, or box distortion can occur. Whilst this provides a secure method of holding your box together, you will often find that the thin strips inside provide more than enough force to hold things together, especially non-critical items like small battery-powered test equipment, torches, etc. If all this sounds too much, countersunk self-tappers may be used.

Appearance!

With all the fitting and bracketry finished, the exterior of the box can now be finally prepared. Radiusing the edges and corners of the box will help its appearance, and, if it is hand-held, its 'touchability'. Use a fine file with caution, and aim for an even radius all over the box, just to take the sharp edges off (photo 27).

The next stage requires warm soapy water and several grades of wet-and-dry silicon carbide paper. Starting with 220 grit, rub the box all over, using plenty of water to avoid clogging the paper. This is the time to finally blend in the radiusing work that you may have done earlier. When you are sure that the whole of the box has been covered by this grade, move on to 320 grit and repeat the process. At this stage, you will probably be able to 'feel' the surface through your finger tips better than by visual inspection.

When you are sure the whole box has been covered by the 320 grit, move on to 400 grit and repeat the process. Finally, go over the whole box with 600 grit, feeling and looking for any scratches left over from coarser papers. If any are found, remove them gently with the appropriate grade, and then move on to 600 grit (photo 28).

With care you will have got this far, and have a very smooth box. If, however, there are some large holes, these can be filled with ordinary P38 car body filler or cellulose putty. It is much easier, however, to avoid them in the first place, which is not as difficult as it may sound. Give the box a final rinse inside and out in warm to hot water, pat it dry with a lint free cloth, and leave it somewhere warm and dry for a few hours.

Lettering

While the box is drying out (especially in the joint areas), some thought needs to be given to any surface detailing that you may wish to add. Simple things will help make your product look more convincing, and can make all the difference. Raised lettering can be added to give the impression of embossed or moulded-on letters. There are two main types, Plasticard polystyrene letters (usually sold to model railway enthusiasts) in several sizes, and Edding self-adhesive vinyl letters. Of the two, the latter are fairly low-profile, but are useful to give a 'makers name' to the product, as they will be painted over later, and so will form part of the product. The Plasticard letters are high-profile, and can be painted over also. The

tops of the letters can be carefully sanded clear of paint to create an additional effect should you so desire (photos 29 and 30), but their higher profile means that they are ideal for identifying important controls such as on/off switches, without being as obvious as, say, the devices' 'names' which can be added later in Letraset.

Other features that you can add include 'grips' made by gluing (with liberal amounts of solvent) strips or pieces of 180/220 wet or dry paper, and spraying over them later. This creates very effectively the 'moulded-on' appearance. Using coarser grades of paper spoils the effect. Embossed self-adhesive metal film is also available from EMA (details further on), and 'pinstripe' tape as sold in motor accessory shops can provide a useful way of breaking up large flat surfaces. This can either be sprayed over, or added later as a colour feature. It does not need much to make the product look real, so take care not to get carried away! (photo 31).

To get perfect edging on some of the items mentioned may necessitate going back to a **fine** file and the range of wet-and-dry papers, just to blend in an overhanging edge. This usually produces better results than just cutting a piece out and sticking it on.

The Plasticard polystyrene letters can be cut out and trimmed with a suitable craft knife. The tip of this knife is the best tool to pick the letters up and put them in place (photo 32). A dab of solvent on their rear immediately prior to placing each letter produces good results. Positioning the letters dry, and then applying solvent tends to leave a mark, so be careful. Getting all the letters in a neat line is also important, and a pre-drawn faint pencil line at 90° to an edge will help a lot here. The vinyl letters mentioned are self-adhesive and may be positioned similarly. If you are making a 'novelty' product for perhaps a child, it may be worth a visit to your local craft and stationary shop. These often have rolls and rolls of small paper stickers that can also be added to the surface of your product, and then sprayed over (photo 33). In this way, a variety of themes could be imparted on your model.

Painting

After the surface detailing is complete, the next stage is to paint the object. For this, aerosol paints as sold by car accessory shops are ideal (photo 34). The two halves of the box should be separated, and can then be given the first coat of grey cellulose primer. A reasonable covering should be given by starting the spray to, say, the left of the object, moving across it and clear to the right before returning. If you wish, you can stop spraying at either end, although some brands of aerosol tend to 'spit' a little when used in this fashion. Spraying this way helps prevent uneven paint buildup and runs! Leave the primer to dry overnight, and then **very carefully** rub down the surface with 800 grit wet-and-dry paper used with lots of soapy water. It is not necessary to re-expose the plastic underneath, just to achieve a silky smooth surface ready for the top coat (use your finger tips). If small areas of plastic re-appear, don't worry. So long as the preparation was good, the primer does not have a lot to do, and the small gaps in the coverage are not a problem (photo 35). When the box has been 'flatted' all over, a final rinse in water is needed (inside and out), and then the box can be dried.

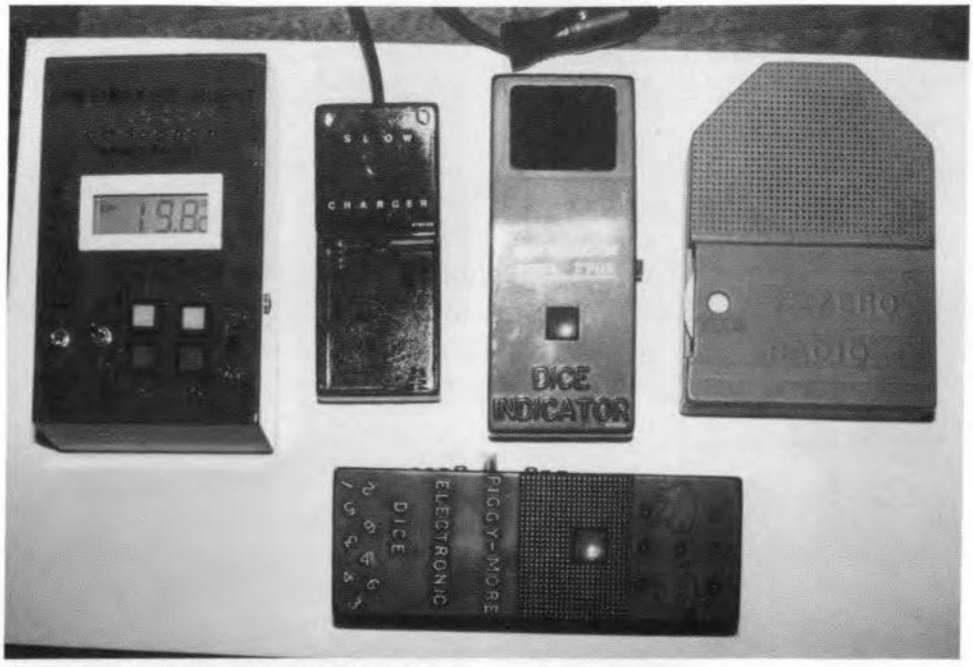


Fig. 37. A selection of finished articles.

The top coat of paint is also aerosol cellulose car paint, and so there is an almost endless variety of colours. If you want black, choose Satin black, which shows fingerprints less than either gloss or matt. Metallic colours are also very effective, but choose carefully after looking at commercial products. Probably the best is Ford 'Graphite', Ford 'Pearl Grey', and one or two others, notably the blues.

A useful tip to improve the spray power of aerosols is to place them in hot water (max. 50°) for a few minutes. This raises the internal pressure, and helps them spray better for longer. Make sure that the whole aerosol is completely dry, as a single drop of water will play havoc with your smooth mirror-like surface!.

If you want an ordinary colour, try and stick with primary colours rather than sickly mixes. Some aerosols (especially the metallics) are what is known as '2-pack', which means that they need a coat of lacquer to give them the final gloss. If you intend to use any Letraset, then this will be needed anyway, and should not be feared.

After the paint has had time to dry, Letraset or similar dry transfer lettering can be added. Given that these dry transfer letters sometimes transfer themselves at the wrong time to the wrong place, the following may be useful. Take a piece of ordinary masking tape, and rub the sticky side against a cotton T-shirt or similar. This will help reduce its stickiness. Use this treated piece of masking tape to provide the baseline for your rub-down lettering. If any do come unstuck, they will probably be on the masking tape, which can be **carefully** removed after you have finished. Do take great care not to press it down too hard, or pull it off too briskly — you may find it brings the paint with it! If, despite this precaution, the odd letter does appear in the wrong place, or you make a mistake, do not despair, as individual letters can usually be removed by the careful application of a small piece of masking tape (untreated), wrapped around a finger tip, and 'dabbed' at the offending letter (photo 36). If this fails, it should be possible to remove it with the aid of a scalpel or craft knife, and a scraping motion, although this method is likely to leave a mark.

If you have used a dark colour to spray your box, then white or red lettering can be used to great effect. Controls can be labelled, and some form of product name added. Very often code numbers at the bottom of the Letraset sheets provide convincing model numbers. It all adds to the realism of the finished article, and will make people look twice or even thrice in their attempt at determining the origin of the 'device' they see.

Finally, a coat of clear lacquer needs to be applied. Car accessory shops sell this as clear cellulose lacquer. Be careful how much you spray on in one coat. Sometimes the solvent attacks the Letraset, causing it to wrinkle up, and destroy all your hard work. Apply just enough to 'flow' into a gloss (allow it to stand a few seconds before adding more!), and spray it somewhere warm to help the solvent evaporate quickly.

Add extra coats as needed until you are happy with the appearance of the finished object (photo 37). All this paint will take quite a while to harden, depending on the number of layers present. I have known some objects (admittedly heavily laden with lacquer) to take up to a week to dry sufficiently to not take fingerprint impressions when handled. If you get the odd fingerprint, it can usually be polished out by using 'T-cut' colour restorer (also from your car accessory shop). That concludes the description of the process — it probably takes as long to read it as it does to make a box! ■

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CLASS-A POWER AMPLIFIER – PART 1

by T. Giffard

The power amplifier presented is a revamped version of the LFA-150 we published in late 1988. It provides rather less power than its popular predecessor, but retains its class A quiescent-current setting up to –3 dB below its clipping limit. The aim of the design was to find a good compromise between class A quality and the dimensions of the necessary heat sinks.

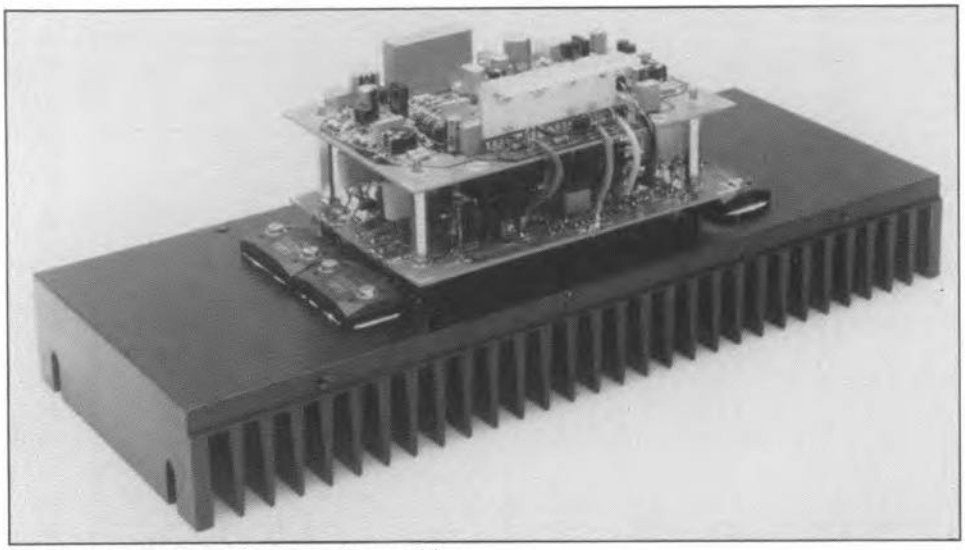


Fig. 1. Prototype of the class A amplifier.

TECHNICAL DATA

Power output (at 1 kHz)	48 W into 8 Ω 83 W into 4 Ω 122 W into 2 Ω
Music power (500 Hz burst, 5 periods on, 5 periods off)	50 W into 8 Ω 90 W into 4 Ω 150 W into 2 Ω
Power bandwidth (48 W into 8 Ω)	1 Hz–270 kHz (+0 dB, –3 dB)
Slew rate	>45 V/µs
Signal-to-noise ratio (1 W into 8 Ω)	>105 dB (A-weighted)
Harmonic distortion (25 W into 8 Ω)	<0.005% (1 kHz0 <0.02% (20 Hz–20 kHz)
Intermodulation distortion (50 Hz: 7 kHz; 4:1)	<0.03% (25 W into 8 Ω) ≤0.005% (1 W into 8 Ω)
Dynamic IM distortion (rectangular wave 3.15 kHz; sine wave 15 kHz)	<0.015% (25 W into 8 Ω)
Input sensitivity	1.1 V r.m.s.
Input impedance	25 kΩ
Quiescent current	1.25 A

ALTHOUGH most of our readers will know what is meant by class A, AB or B, it may be useful for others to recapitulate the properties of these classes of operation.

Most modern a.f. output amplifiers are designed as a push-pull configuration. In this, two power transistors (or valves) are connected in series between the positive and negative power supply lines, and the loudspeakers are connected to their junction. The transistors are driven by opposing signals, that is, when one conducts, the other is switched off.

The transfer characteristic (I_b/I_c curve) of a transistor is, unfortunately, not a straight line: particularly at its lower end, when the currents are low, it is very curved. In principle, the characteristics of two transistors in push-pull complement one another nicely, but the base-emitter transfer voltage puts a spanner in the works.

To prevent distortion, therefore, use is made of a bias that causes a small constant current to flow through the transistors. The result of this is that the curved part of the characteristic is not used. If virtually no current flows through the transistors, class B amplification is obtained, which is characterized by cross-over distortion. Nowadays, this method is used only in inexpensive, portable equipment where economy of battery usage is the prime requirement.

For many years now, class AB operation has been used in hi-fi equipment. In this, a small quiescent current flows through the output transistors, which makes them work in class A when the drive is small (say, 0.1 W) and in class B at higher drives. This method is characterized by acceptable low distortion and good efficiency (about 75%). Moreover, heat dissipation depends on the energy of the drive signal, so that the amplifier remains fairly cool during normal operation.

Many designers and listeners do not find AB operation good enough and prefer class A. In this, such a large quiescent current flows through the transistors, that even at maximum drive neither of the transistors switches off (as happens in class AB). The disadvantages of class A operation are its low efficiency (<50%) and large heat dissipation. Even during quiescent operation, a class A amplifier uses about twice its nominal power.

Naturally, commercial class A amplifiers are

available at many hi-fi retailers, but, although their superior quality cannot be denied, they are very expensive, have very large heat sinks or fans to get rid of the dissipated heat, and provide only a modest power output. These factors make it easy to understand why a 25–50 W class A amplifier is not exactly the most popular item in the hi-fi trade.

In the present design, we have tried to combine class A operation with an acceptable heat dissipation. Output power was specified at 50 W into 8 Ω. In true class A, that would mean a dissipation of rather more than 100 W per channel. To get rid of more than 200 W of heat in normal enclosures without the use of fans is virtually impossible. Fans are, however, anathema, because even the best ones can be heard, particularly during soft music passages.

The design is, therefore, near-class A, that is, the quiescent current is set to a level that ensures that the amplifier can deliver half its nominal power to the loudspeakers. The class A range is thus 25 W, which means that in actual use the amplifier operates in class A up to –3 dB below full drive. The dissipation then amounts to about 140 W and that can be got rid of with 'normal' heat sinks (based on an ambient temperature of not more than 35 °C and a maximum heat sink temperature of 75 °C).

It should be noted that a class A amplifier operates in its class only into its specified load impedance, normally 8 Ω. It is, of course, possible to provide more power into 4 Ω or 2 Ω, but that will not be in class A. This points to a serious disadvantage of class A amplifiers that is hardly ever highlighted: *into a lower than specified load, it operates in class AB*. Since the input impedance of virtually all modern loudspeakers varies between 4 Ω and 10 Ω, amplifier manufacturers have the near impossible task of designing an amplifier that remains in class A over this range of impedances. The power required to operate a class A output stage into a 4 Ω load is twice that for operating it into an 8 Ω load. A 25 W class A amplifier designed to operate into 8 Ω dissipates more than 100 W, but to enable it to operate in class A into 4 Ω, the quiescent current would have to be increased to a level where the dissipation would exceed 200 W.

The real requirement of a top-quality a.f. output amplifier is that it can deliver a reasonable power, say, not less than 10 W, into an impedance varying between 4 Ω and 10 Ω. That will meet the demands of all hi-fi listeners in 95% of the time. The present design provides 25 W into 8 Ω; 12.5 W into 4 Ω and rather more than 6 W into 2 Ω, all in class A. At the other 5% of the time, in class AB, it gives 48 W into 8 Ω, 83 W into 4 Ω and 122 W into 2 Ω.

The revamped circuit

The renovating of the LFA-150 started with a lowering of the supply voltage from ±56 V to ±29 V to ensure an appreciable lowering of the dissipation.

Next, a number of transistor were replaced, partly because some of them were no longer

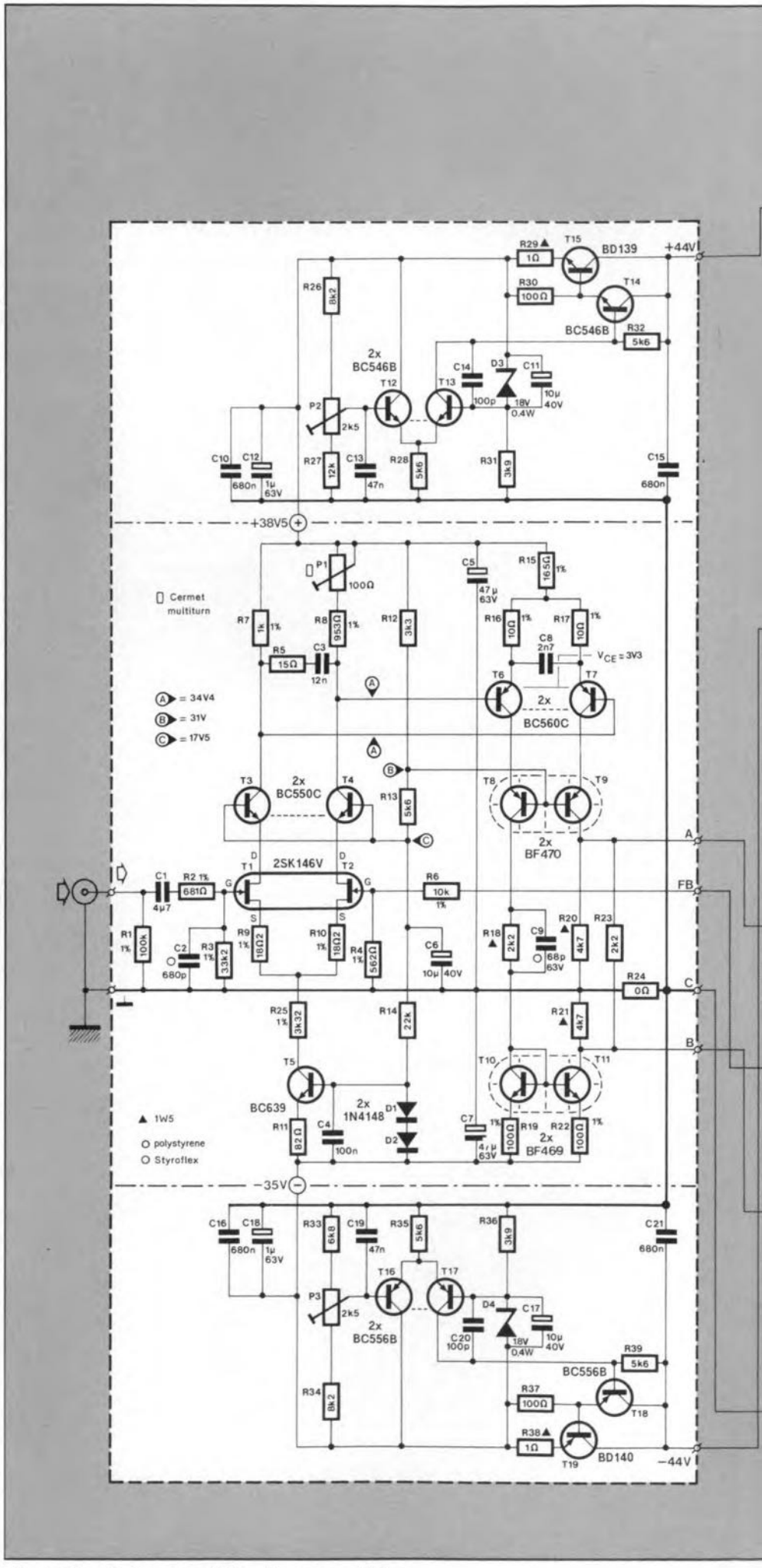
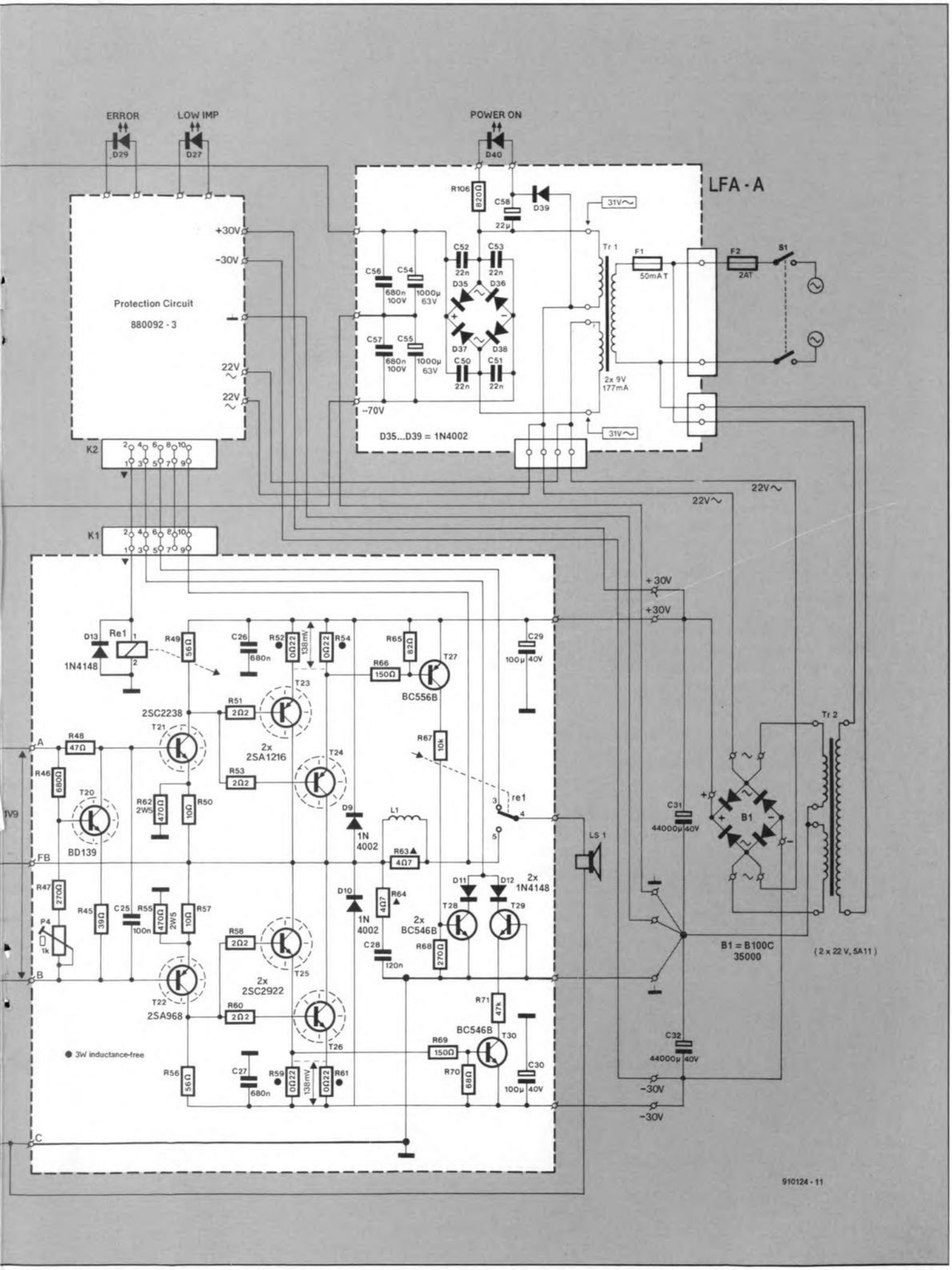


Fig. 2. Circuit diagram of the class A amplifier.


ERROR
LOW IMP
POWER ON
D29
D27
D40
LFA - A
Protection Circuit
880092 - 3
+30V
-30V
22V
22V
K2
K1
R106 820Ω
C58 22µ
D39
31V~
C52 22n
C53 22n
C56 680n 100V
C54 1000µ 63V
C57 680n 100V
C55 1000µ 63V
D35
D36
D37
D38
C50 22n
C51 22n
Tr 1
F1 50mA T
F2 2AT
S1
2x 9V 177mA
-70V
D35...D39 = 1N4002
31V~
22V~
22V~
+30V
+30V
D13 1N4148
Re1
R49 56Ω
C26 680n
R52 0Ω22
138mV
R54 0Ω22
R65 82Ω
R66 150Ω
T27 BC556B
C29 100µ 40V
T23 2SC2238
R51 2Ω2
T21
2x 2SA1216
T24
R53 2Ω2
R67 10k
A
R48 47Ω
R46 680Ω
T20 BD139
R62 2W5 470Ω
R50 10Ω
D9 1N 4002
L1
re1
LS 1
FB
R63 4Ω7
R47 270Ω
R45 39Ω
C25 100n
R55 2W5 470Ω
R57 10Ω
P4 1k
D10 1N 4002
R64 4Ω7
D11
D12
2x 1N4148
T28
T29
2x BC546B
R68 270Ω
C28 120n
R58 2Ω2
T25
2x 2SC2922
T22
2SA968
R60 2Ω2
T26
B
R71 47k
BC546B T30
R69 150Ω
R70 68Ω
C30 100µ 40V
C32 44000µ 40V
-30V
-30V
C31 44000µ 40V
B1
Tr 2
B1 = B100C 35000
(2 x 22 V, 5A11)
3W inductance-free
R56 56Ω
C27 680n
R59 0Ω22
138mV
R61 0Ω22
C
910124 - 11

available. Motorola's BF762 and BF759 have been replaced by the BF470 and BF469 respectively, while Sanken's Types 2SC2922 and 2SA1216 have been substituted for Toshiba's 2SC2565 and 2SA1095 output transistors.

Third, the amplification of some stages has been altered. The gain of the first differential amplifier is now 19 dB instead of 11 dB, while that of the second differential amplifier has been reduced by 6 dB. This results in the open-loop amplification rising from 2 300 to 3 000, which lowers the distortion to even lower levels than in the LFA–150.

Finally, the compensation and d.c. operating points have been changed at a number of places.

Because of all these alterations, the values of many components in the original LFA–150 have had to be changed. The amplifier is constructed on four PCBs: two for the output stages, one for the protection circuit, and one

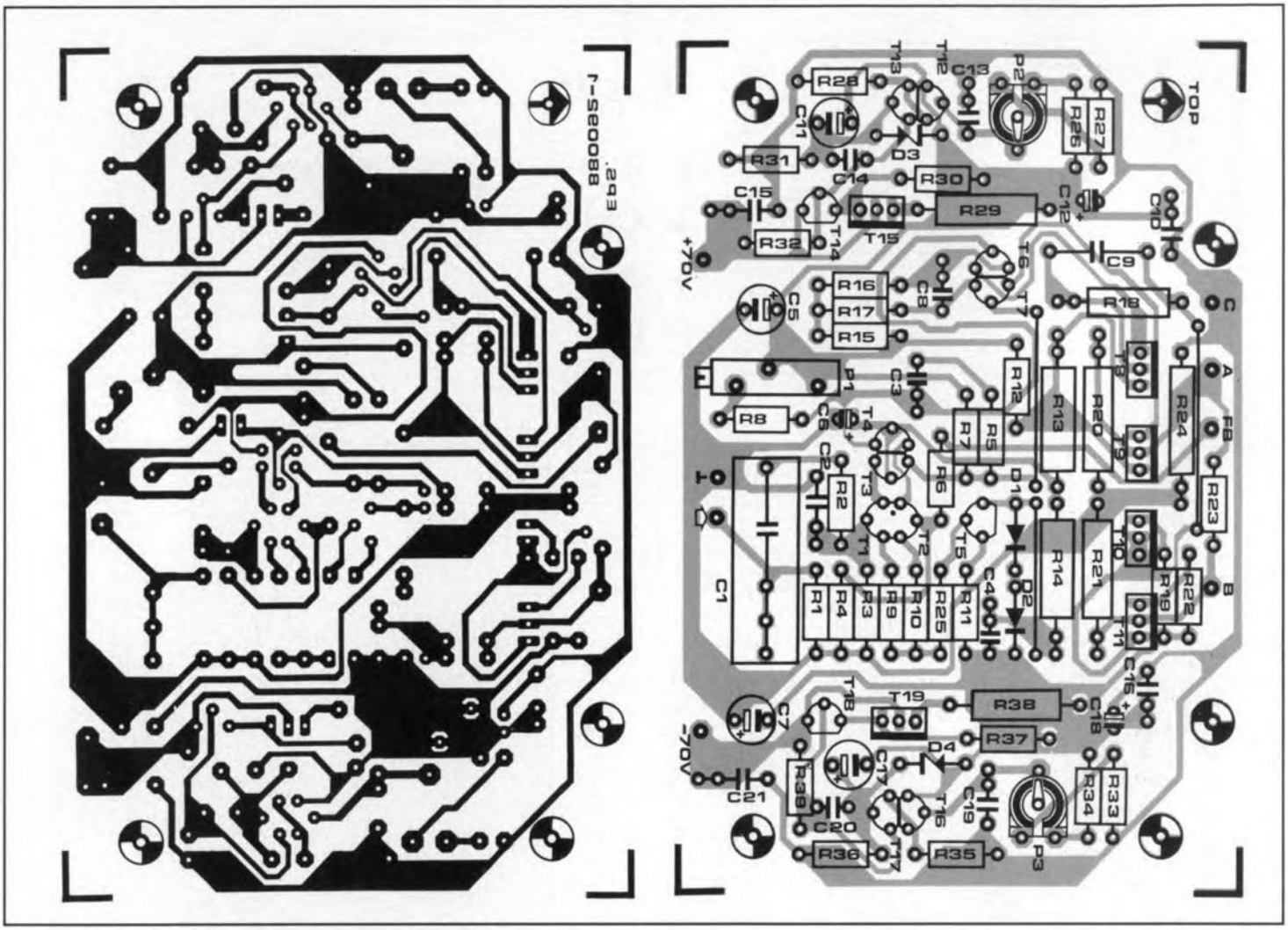


Fig. 3. Printed circuit board for the voltage amplifier.

PARTS LIST

Resistors:
R1 = 100 kΩ, 1%
R2 = 681 Ω, 1%
R3 = 33.2 kΩ, 1%
R4 = 562 Ω, 1%
R5 = 15 Ω
R6 = 10 kΩ, 1%
R7 = 1 kΩ, 1%
R8 = 953 Ω, 1%
R9, R10 = 18.2 Ω, 1%
R11, R65 = 82 Ω
R12 = 3.3 kΩ
R13 = 5.6 kΩ
R14 = 22 kΩ
R15 = 165 Ω, 1%
R16, R17 = 10 Ω, 1%
R18 = 2.2 kΩ, 1.5 W
R19, R22 = 100 Ω, 1%
R20, R21 = 4.7 kΩ, 1.5 W
R23 = 2,2 kΩ
R24 = wire bridge
R25 = 3.32 kΩ, 1%
R26, R34 = 8.2 kΩ
R27 = 12 kΩ
R28, R32, R35, R39 = 5.6 kΩ
R29, R38 = 1 Ω, 1.5 W
R30, R37 = 100 Ω
R31, R36 = 3.9 kΩ
R33 = 6.8 kΩ
R45 = 39 Ω
R46 = 680 Ω
R47 = 270 Ω
R48 = 47 Ω
R49, R56 = 56 Ω
R50, R57 = 10 Ω
R51, R53, R58, R60 = 2.2 Ω
R52, R54, R59, R61 = 0.22 Ω, 3 W, inductance-free
R55, R62 = 470 Ω, 2.5 W
R63, R64 = 4.7 Ω, 1.5 W
R65 = 82 Ω
R66 = 150 Ω
R67 = 10 kΩ
R68 = 270 Ω
R69 = 150 Ω
R70 = 68 Ω
R71 = 47 kΩ
P1 = 100 Ω multiturn preset
P2, P3 = 2.5 kΩ preset
P4 = 1 kΩ, multiturn preset

Capacitors:
C1 = 4.7 µF, MKT
C2 = 680 pF, polyester
C3 = 12 nF
C4, C25 = 100 nF
C5, C7 = 47 µF, 63 V
C6, C11, C17 = 10 µF, 40 V
C8 = 2.7 nF
C9 = 68 pF, 63 V, polyester
C10, C15, C16, C21, C26, C27 = 680 nF
C12, C18 = 1 µF, 63 V
C13, C19 = 47 nF
C14, C20 = 100 pF
C28 = 120 nF
C29, C30 = 100 µF, 40 V

Semiconductors:
D1, D2, D11–13 = 1N4148
D3, D4 = zener, 18 V, 400 mW
D9, D10 = 1N4002
T1, T2 = 2SK146V
T3, T4 = BC550C
T5 = BC639
T6, T7 = BC560C (match!)
T8, T9 = BF470
T10, T11 = BF469 (match!)
T12–14 = BC546B
T15, T20 = BD139
T16–18 = BC556B
T19 = BD140
T21 = 2SC2238
T22 = 2SA968
T23, T24 = 2SA1216
T25, T26 = 2SC2922

Miscellaneous:
Re1 = 24 V for PCB mounting with 1 change-over contact
L1 = 6 turns, I/D 15 mm, of 1.5 mm enamelled copper wire
K1 = 10-way straight header
Heat sink, 0.4 K/W (see Part 2)
PCB 880092-1
PCB 880092-2

for the auxiliary power supply,

Only an outline description of the circuit in Fig. 2 will be given—for more details, see Ref. 1.

The input signal is applied to differential amplifier T_1-T_2 via C_1 (the only capacitor in the signal path) and low-pass filter R_2-C_2. The filter has a cut-off frequency of 340 kHz to prevent transient intermodulation distortion (TIM). The d.c. operating point of the two FETs is set by a constant-current source based on T_5.

Transistors T_3 and T_4 and the FETs form a cascode circuit that has an amplification of about 9.2 (=gain of about 19 dB). Preset P_1 serves to eliminate any inequalities (off-set) in the d.c. operating points.

Lag compensation is provided by R_5-C_3.

The amplified signal is fed to differential amplifier T_6-T_7 that together with T_8 and T_9 form a second cascode circuit to keep the bandwidth as large as possible. The amplification of this section is 308 (nearly 50 dB).

The output of T_8 is fed to the current amplifier via current mirror T_{10}-T_{11}.

The power supply for the voltage amplifier is taken from discrete voltage regulators T_{12}-T_{15} (positive) and T_{16}-T_{19} (negative). The supply voltage for this section is higher than that for the current amplifier, so that the voltage drop across the output transistors remains small, even at maximum drive levels.

The current amplifier consists of a quiescent-current control based on T_{20}, and drivers T_{21} and T_{22}, followed by power transistors T_{23}, T_{24}, T_{25} and T_{26}, which are connected in a compound configuration. In contrast to the usual emitter-follower, this design provides some voltage amplification and combines very low distortion with a low output impedance. The output signal is fed to the loudspeakers via an inductor and a protection relay.

When the load current exceeds 15 A (peak), transistors T_{27} and T_{30} switch on and actuate the protection circuit via T_{28} and T_{29}. That circuit then de-energizes the relay.

The power supply uses two mains transformers in series, Tr_1 and Tr_2. Note that Fig. 2 shows the power supply for a mono amplifier; two (housed in one enclosure) need to be built for a stereo amplifier. The supply for the current amplifier is around ±30 V, and that for the voltage amplifier, ±44 V. The voltage amplifier, however, operates from +38.5 V and –35 V, because its voltage drop on the positive line is about 3.5 V higher than that on the negative line. This supply arrangement ensures that the positive and negative drive levels are exactly equal. ■

Reference.

"LFA-150: a fast power amplifier", *Elektor Electronics*, November 1988, pp. 20–26; December 1988, pp. 42–46.

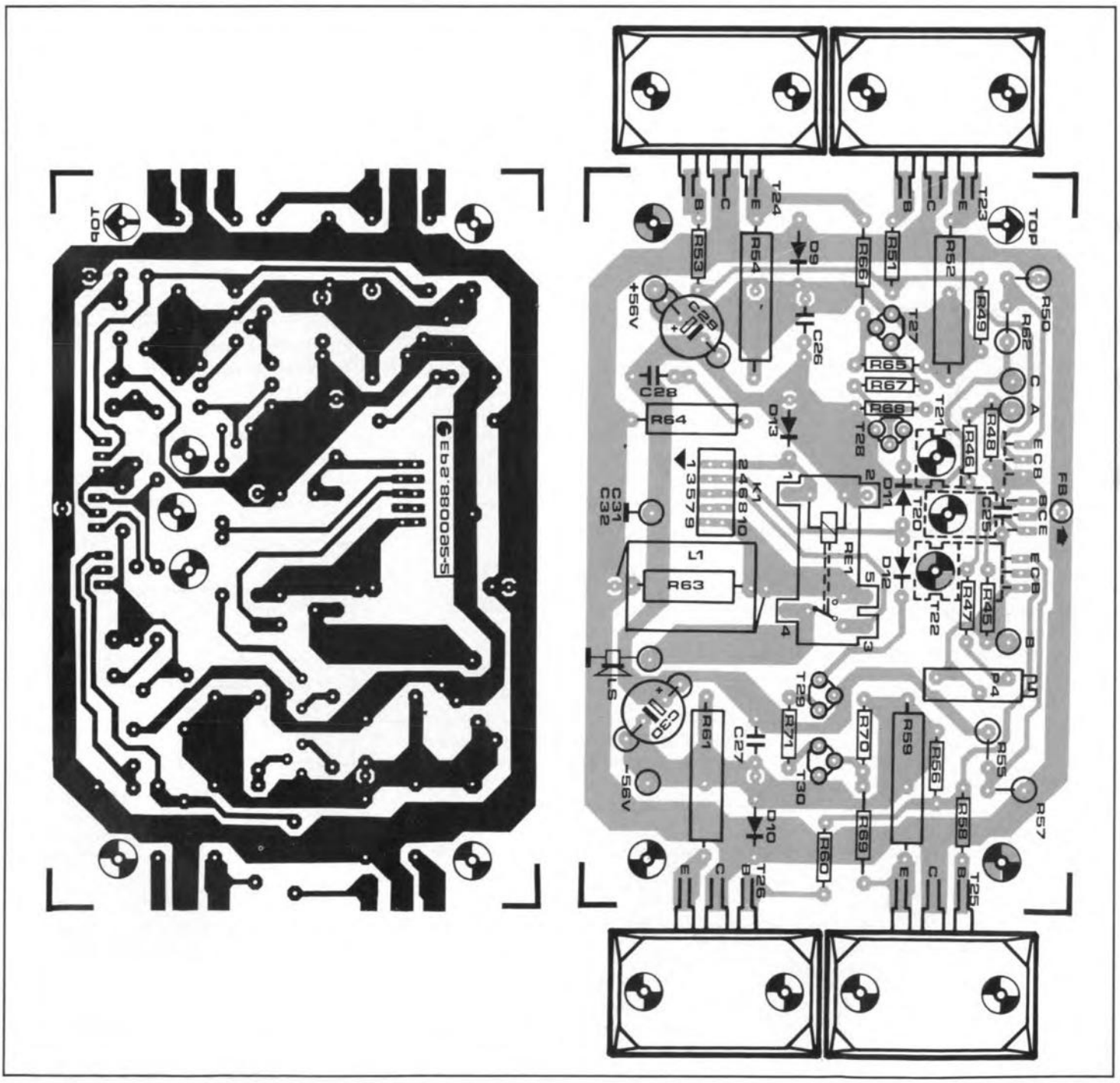


Fig. 4. Printed circuit board for the current amplifier.

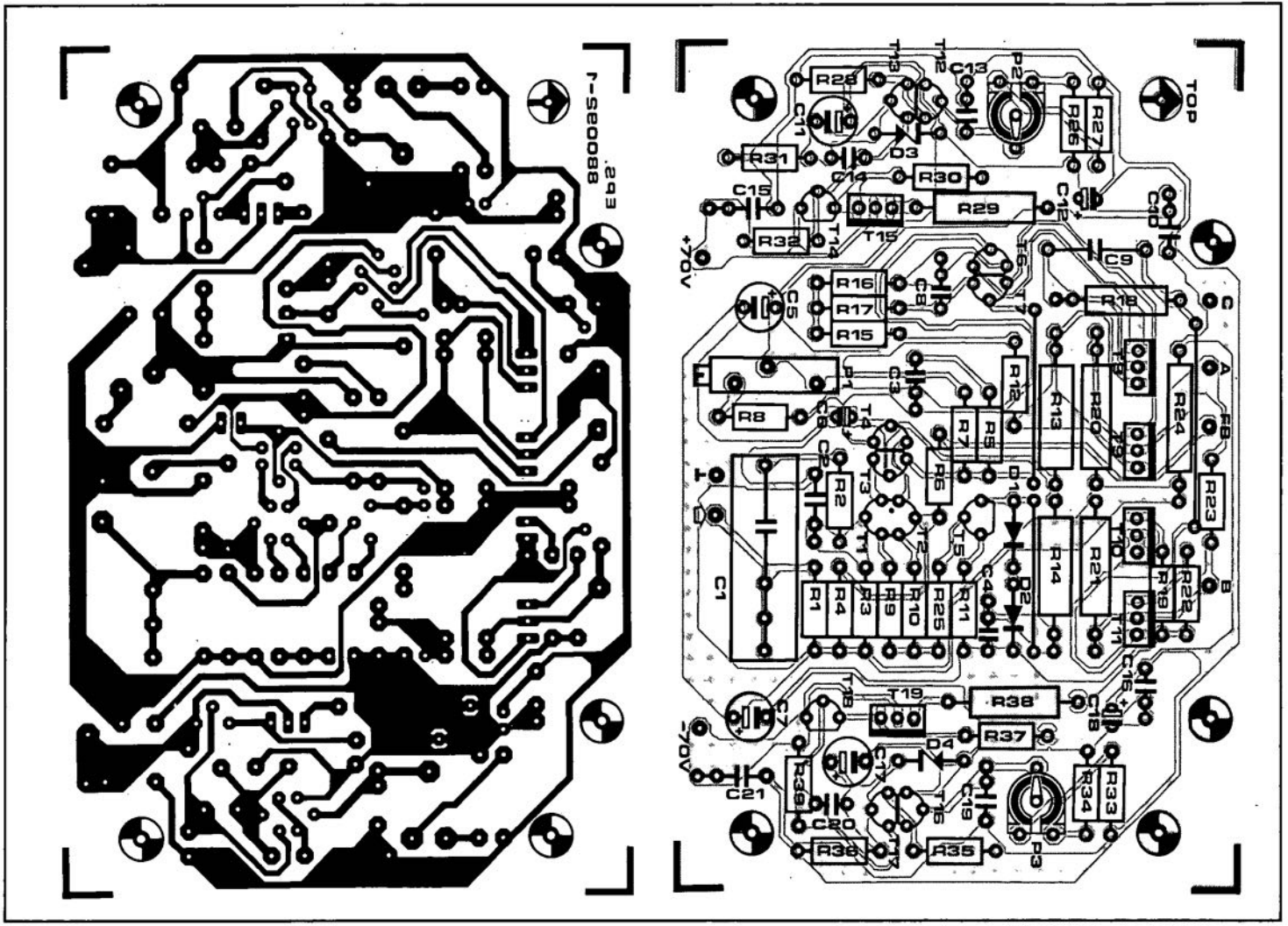


Fig. 3. Printed circuit board for the voltage amplifier.

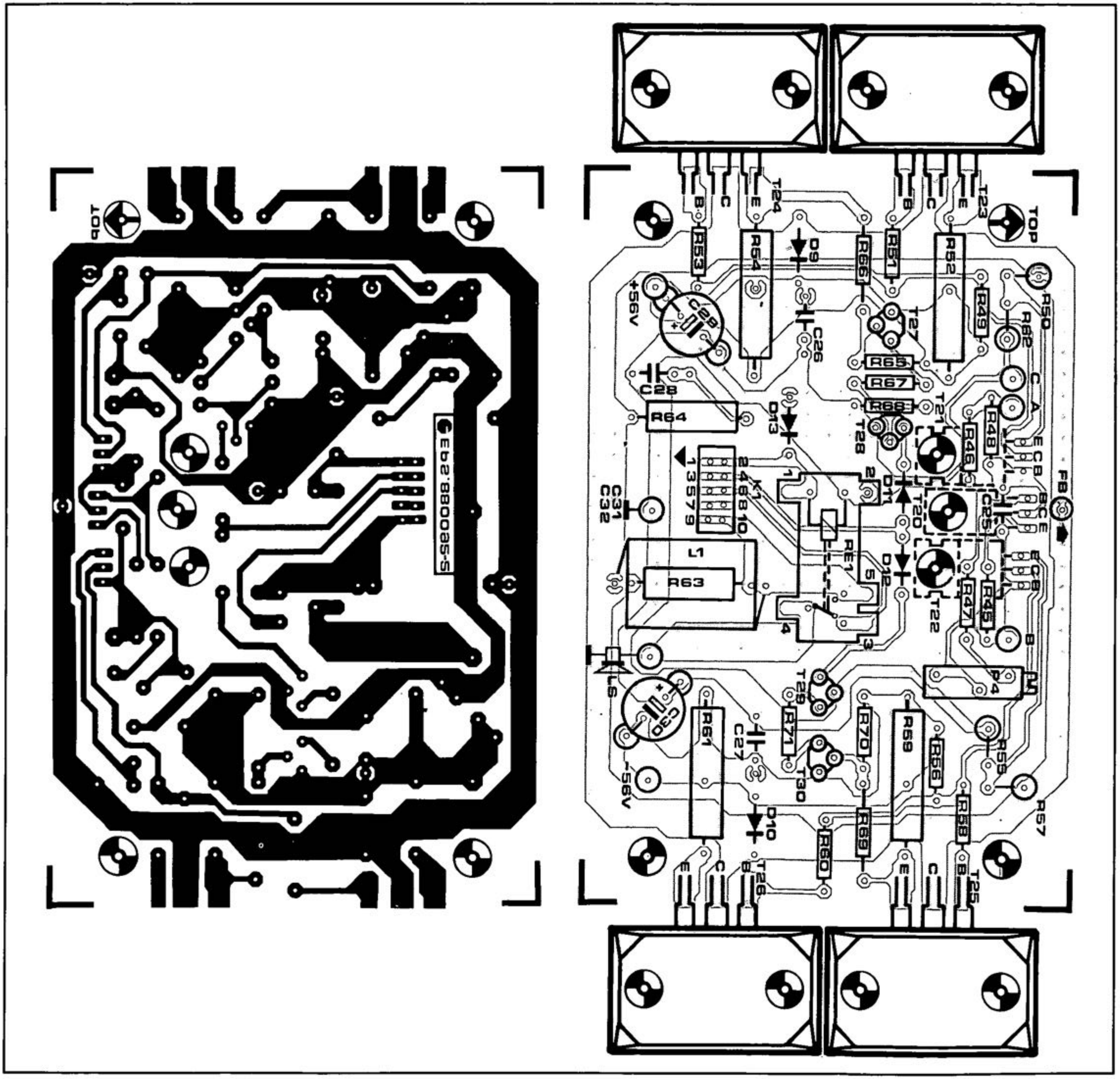


Fig. 4. Printed circuit board for the current amplifier.

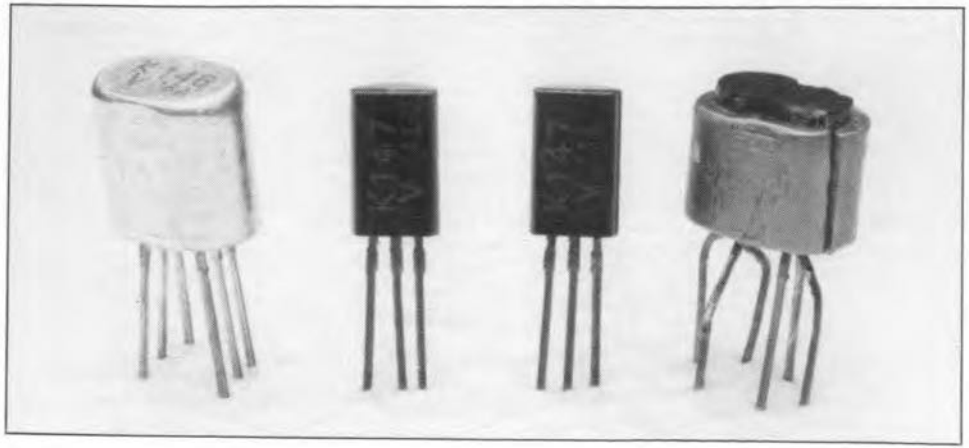
CORRECTIONS AND UPDATES

LFA150-A Class-A amplifier

November and December 1991

Replacement for 2SK146V.

We have recently been informed by Toshiba that the dual FET Type 2SK146V used in the LFA150-A design is no longer manufactured. The 2SK146V is not a dual FET in the true sense of the word, i.e., there are no two FETs on a single chip. Rather, it consists of two FETs, each in its own enclosure, which are held together by a metal ring. Such a construction is readily reproduced by clamping two 2SK147V FETs together, using a small piece of metal (e.g., copper or brass).



The photograph illustrates the construction of the replacement dual FET. In practice, the 'imitation' works perfectly. Note, however, that the pin connections of the replacement FET are different from the original 2SK146, which has facing identical pins. By contrast, the dual 2SK147V construction has identical pins in mirrored positions. Fortunately, this is simple to resolve by bending the outer pins (drain and source) of one FET such that the pin positions are swapped. (920163)

Sound sampler for Amiga

November 1991.

Capacitor C9 is mising from the parts list and the circuit diagram. C9 is a 100-nF decoupling capacitor fitted near IC7 (see component overlay).

LEDs D2 and D4 should be transposed, both in the circuit diagram and the parts list. D2 is the ERROR LED, and D4 the LEFT LED. (920074)

FOUR-TERMINAL NETWORKS - PART 2

The design of attenuators

by Steve Knight, BSc

In this second and final part of our investigation into the design and uses of four-terminal attenuator systems, we shall first of all derive some simple relationships between the characteristic resistance of an attenuator T-section and the degree of attenuation provided by the section in terms of the resistive elements that make up the section.

THE calculations are not difficult, and those readers with an arithmetical bent might like to confirm some of the answers. We will relate our results with those of the π–section, consider insertion loss, and have a look at the practical design of attenuators.

Finding values

For the properly terminated symmetrical T-section shown in Fig. 8, we let the attenuation be expressed as $N=U_1/U_2$, in which numbered subscripts are used for convenience. Since the input resistance is R_o, the input current, I_1, must be U_1/R_o and the voltage, U, across the centre shunt arm will be

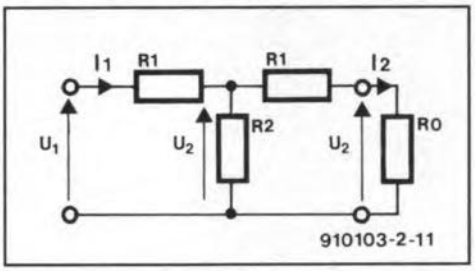


Fig. 8. Deriving the attenuation factor of a section.

$$U=U_1-I_1R_1.$$

Hence,

$$U=U_1-U_1R_1/R_o=U_1[1-R_1/R_o].$$

But the output voltage, U_2, is clearly the proportion of U developed across R_o, given by

$$U_2=U[R_o/(R_1+R_o)],$$

whence

$$U_2=U_1[1-(R_1/R_o)][R_o/(R_1+R_o)].$$

From this, the ratio

$$U_1/U_2=N=(R_o+R_1)/(R_o-R_1).$$

This gives the attenuation factor in terms of R_o and R_1. What we need now is a relationship involving R_1 and R_2 in terms of R_o and N. Working from this last result, we find that

$$R_1=R_o[(N-1)/(N+1)].$$

Using the earlier result that

$$R_o=\sqrt{(R_1^2+2R_1R_2)},$$

we get

$$R_2=R_0[2N/(N^2-1)].$$

When R_o and N are known, these simple expressions enable an attenuator to be designed that gives a desired signal reduction and the proper matching conditions for the circuit system concerned. Figure 9 illustrates the meaning of the two formulae.

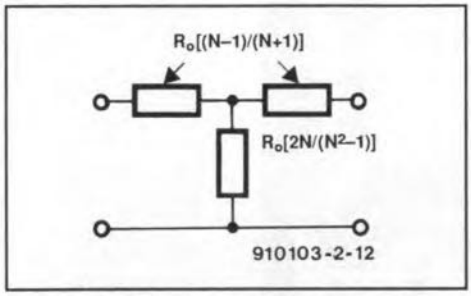


Fig. 9. Relationships to determine the elements in terms of R_o and N.

Trying things out

A couple of examples will show how we can apply these results to solve some elementary design problems.

First, suppose we want a symmetrical T–section network to match into a 300 Ω line and have a voltage attenuation of 14 dB; what values of resistors do we want?

Well, the attenuation factor N=antilog 14/20 =antilog 0.7=5. In other words, the output will be one fifth of the input. We thus get

$$R_1=300[(5-1)/(5+1)]=300\times{}^4/_6=200\ \Omega;$$

and

$$R_2=300[(2\times5)/(25-1)]=300\times{}^{10}/_{24}=125\ \Omega.$$

Figure 10 shows the completed section.

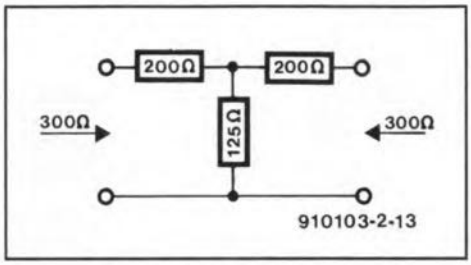


Fig. 10. Example of en elementary T-section design.

Suppose now that the output stage of a small transmitter has an internal resistance of 600 Ω and is intended to supply current to a 600 Ω load. We need to design a T-section which, when inserted into the line connecting generator and load, will reduce the load current to one third of its initial value.

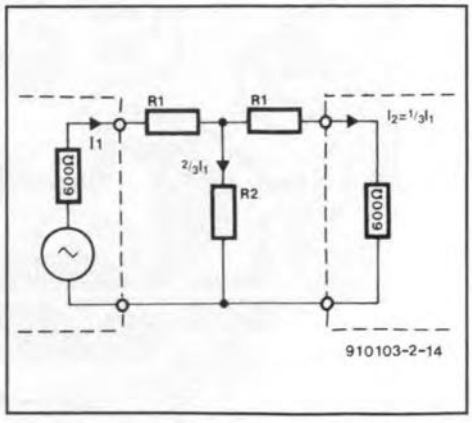


Fig. 11. A further design example relating to correct matching procedures.

This situation can be illustrated after the manner of Fig. 11. The section matches between equal impedances of 600 Ω and should, therefore, have R_o=600 Ω also. The attenuation factor, N, is 3, so that

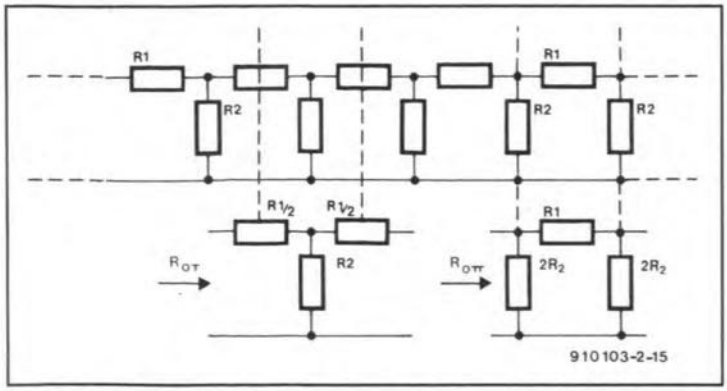


Fig. 12. These attenuator sections have the same total series and shunt resistances; then, $Z_{oT}Z_{o\pi}=R_1R_2$.

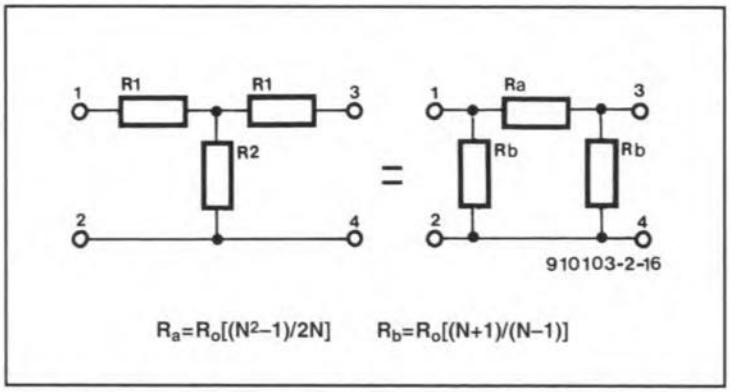


Fig. 13. Finding the element relationships between the T- and π–sections.

$R_1=600[(3-1)/(3+1)]=600\times{}^2/_4=300\ \Omega$

and

$R_2=600[(2\times3)/(9-1)]=600\times{}^6/_8=450\ \Omega.$

In a case like this, it is important to notice that current I_1 supplied by the generator is the *same* whether the section is in circuit or not. In both cases, the generator sees a resistive load of 600 Ω. With the section connected, the 'unwanted' current ($^2/_3 I_1$) flows along the shunt arm, as an application of Ohm's law will immediately verify.

The π-section

It might appear that the π-section has been rather neglected, but there is a circuit relationship between the T-section and π-sections that makes an analysis of the π-section quite easy. Figure 12 shows a ladder network of series and shunt resistances; from an examination of this network, is it a chain of T-sections or π-sections? The answer is that it depends how you look at it. For, either a T-section can be taken from the network by considering the line division AA, or a π–section taken by considering the line division BB. The T-section cuts through the centre of each of the series elements R_1, while the π-section effectually splits the shunt element into two parallel parts, each of value $2R_2$. Hence, the ladder can be viewed as a string of T-sections or π-sections.

We might expect, therefore, that there would be little difference between the relationships derived for the two types of section, but for the matter of *equivalence* it isn't just a job of halving the series arms and doubling up the shunts as this last analysis might have led us to believe.

We can make an exact comparison between the sections by looking at Fig. 13. Here, we use letter subscripts for the π-section resistors to avoid confusion.

For the two networks to be equivalent in their characteristics, the resistance seen between terminals 1 and 2 of both networks must be equal, as must the resistance between terminals 1 and 3 of both networks, with the output on open circuit. This means that R_1+R_2 on the T-section must equal $R_b(R_a+R_b)/(R_a+2R_b)$ on the π-section. Also,

$$2R_1=2R_aR_b/(R_a+2R_b)$$

or

$$R_1=R_aR_b/(R_a+2R_b).$$

Substituting back for R_1 in the first expression then gives us

$$R_2=R_b{}^2/(R_a+2R_b).$$

These relationships provide us with the elements of the T-network such that this will correspond to a given π-network.

It is also not too hard to demonstrate that for the basic π-section shown in Fig. 13

$$R_o=R_aR_b/\sqrt{(R_a{}^2+2R_aR_b)}=\sqrt{R_{oc}R_{sc}}$$

and that

$$R_a=R_o[(N^2-1)/2N]$$

and

$$R_b=R_o[(N+1)/(N-1)]$$

where the bracketed term is simply inverted from that of the T-section and R_a and R_b are themselves swapped over.

A useful relationship follows from the first of these: since $\sqrt{(R_1{}^2+2R_1R_2)}$ is the R_o of a T-section (R_{oT}), we can deduce that for sections having the *same total series and shunt resistances* (see Fig. 12 again)

$$R_{o\pi}R_{oT}=R_1R_2=R_aR_b.$$

Don't confuse this with the equivalence relationships.

So, fundamentally there is no difference in the functions of these alternative forms of the sections and either may be used in a particular situation. The actual choice depends upon which form, given a particular value of characteristic resistance R_o, yields the more readily obtainable values of resistance for the elements.

In general design work, where stringent conditions are not of vital importance, the use of 5% resistors is quite acceptable; the resulting variation in attenuation will normally be no more than 0.5 dB and the mismatch in the characteristic resistance itself of the order of 5%. We will return to these points a little later on.

Insertion loss

The important thing in designing attenuators for general bench use is not to bother too much about getting exact answers to the calculations. It is no use working out a resistance to three or four decimal places and

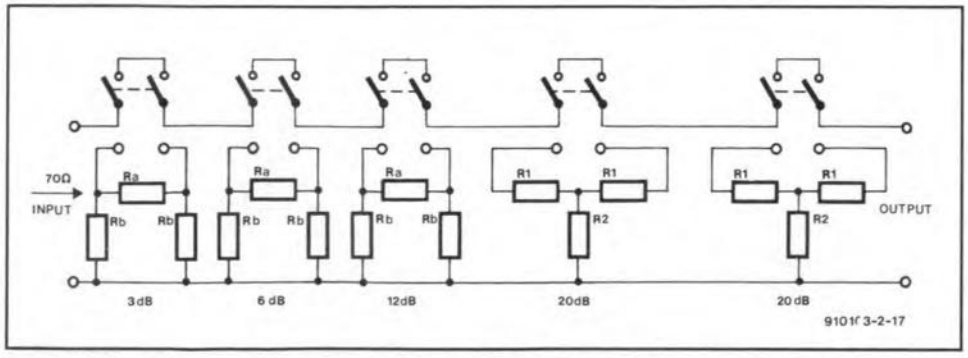


Fig. 14. Designing an attenuator knowing R_o and the required attenuation.

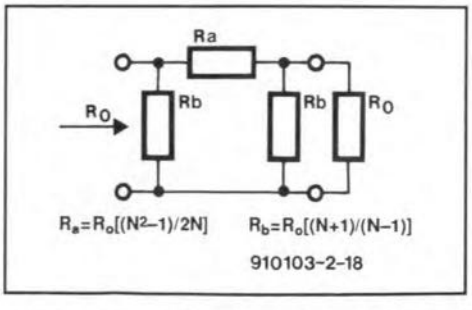


Fig. 15. The relationships should be compared with those for the T-section given earlier.

then discover that you've got to use a preferred value anyway. The attenuation factor can often be rounded off in the same way; 6 dB, for instance, is a voltage ratio of 1.9953... but we wouldn't put this into a formula: we use the nice round figure of 2. Of course, things don't always work out quite so conveniently, but anything beyond two decimal places is a waste of effort.

Let us now design a 5-section attenuator for a 70-Ω line giving switched positions of 3 dB, 6 dB, 12dB and two 20 dB reductions. For interest, let the first three stages be derived from π-sections and the last two from T-sections. The job will look like Fig. 14, which also shows the appropriate switching.

Look first at the 3-dB section; the required attenuation is 3 dB for which attenuation factor N is found to be antilog $^3/_{20}$ or 1.41. Using the relationships shown for convenience in Fig. 15, and with R_o=70 Ω, we find that R_a=24.8 Ω and R_b=410 Ω. The last value is a bit of a problem, since it falls between 390 Ω and 430 Ω in the E24 range. One way out is to parallel 9.1 kΩ with a 430 Ω or get hold of a 412 Ω from the E96 precision range. Otherwise, use 24 Ω and 390 Ω in series; the mismatch is not very serious: R_o then works out at 66 Ω.

Going through the same procedure for the 6 dB (N=2) and the 12 dB (N=4) π–sections, we find for the elements the respective values: R_a=52 Ω; R_b=210 Ω; R_a=131 Ω; R_b=116 Ω. Practical values here would be 51 Ω; 220 Ω; 130 Ω; and 120 Ω. Amuse yourself by calculating the above three ranges in terms of T-sections; do the resistance values fit any better?

For the two T-sections, we require an attenuation of 20 dB (N=10); hence, for R_o=70 Ω, we find

$$R_1=R_o[(N-1)/(N+1)]=70\times{}^9/_{11}=57\ \Omega$$

and

$$R_2=R_o[2N/(N^2-1)]=70\times{}^{20}/_{99}=14\ \Omega.$$

Practical values here would be 56 Ω and 13 Ω. The completed attenuator is shown in Fig. 16.

Now, try designing a series of five T-sections with switched ranges of 1 dB, 2 dB, 4 dB, 8 dB and 16 dB; this enables a maximum attenuation of 31 dB to be achieved in 1 dB steps. The R_o should suit your own particular fancy. As a help, the respective N values are 1.12; 1.26; 1.58; 2.45 and 6.30.

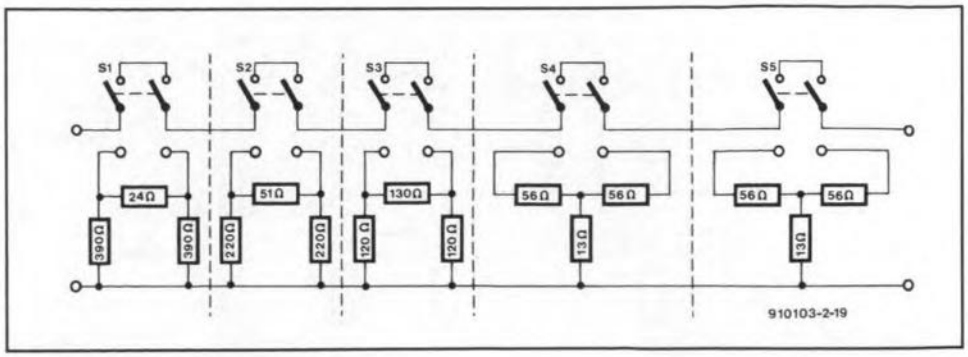


Fig. 16. The completed design.

Practical considerations

When we talk about purely resistive attenuators, we are, of course, in the realms of fantasy; it is not possible to make up an attenuator system having a number of sections in tandem without introducing some inductive and capacitive elements. The object of any design is to keep these to their absolute minimum, just as in filters, where inductance and capacitance are the necessary elements, we try to eliminate resistance.

It is necessary, then, to keep all interconnecting leads as short as possible and to avoid the proximity of these leads, as well as the resistances themselves, to any surrounding metal parts. Further, there must be no capacitive coupling between the sections or certain frequency components of the signal will sneak through without the desired attenuation, but with definite phase shifts. The resistances should not, for obvious reasons, be wirewound, though types with a non-inductive construction might be used.

Simple aluminium boxes are available nowadays that can be used to house bench-type attenuators. Types measuring some 120–150 mm in length with perhaps 50 mm width and a depth of about the same are ideal. Figure 17 shows the general method of assembling such attenuators.

The box is divided up into the required number of compartments by cross screens that can be made of thin aluminium or tinplate. If aluminium is used, the screen will have to be flanged and screwed to the side walls of the box, but with an all tinplate construction, soldering is the best approach.

Small holes are drilled centrally in each screen (before fitting!) to permit the series-arm resistors to feed through, and the shunt-arm resistors are returned either directly to each screen or to a convenient position on the box floor itself. A relatively heavy common wire running through the screens sometimes makes dependence on the box metal unnecessary.

Slide or miniature toggle switches are used for the attenuation selection, though it is possible, with certain forms of construction—see Fig. 18—to use rotary switches. It is often easier to use the base of the box to carry the terminals and switching, the actual lid being fitted last and becoming the working base. This avoids having long leads to connect the switches which would then be separated from the rest of the network in the body of the box.

Attenuators that are to be housed inside equipment, such as a signal generator for example, can be built into the general internal design method, but a divided-compartment assembly is still necessary if the best results are to be obtained. For less stringent work, the resistances can often be simply mounted directly to the tags on a rotary switch wafer or wafers as they could for the system shown in Fig. 18. Most simple 'dividers' are assembled this way.

The power ratings of the resistors used in attenuators must, of course, be such as to ensure that no appreciable temperature rise can occur in normal use. ■

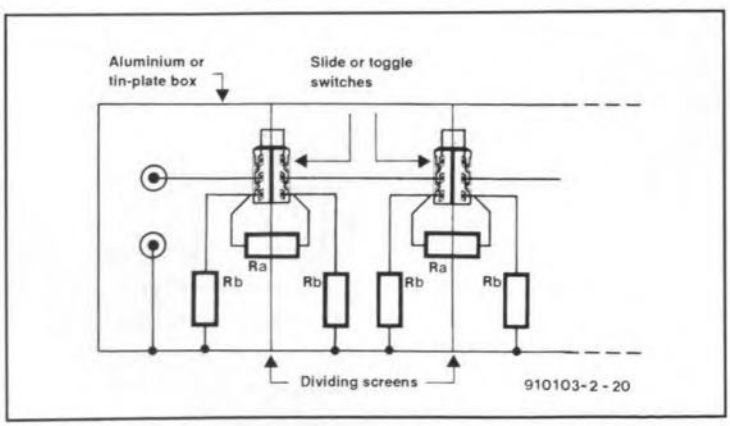


Fig. 17. Practical method of assembly.

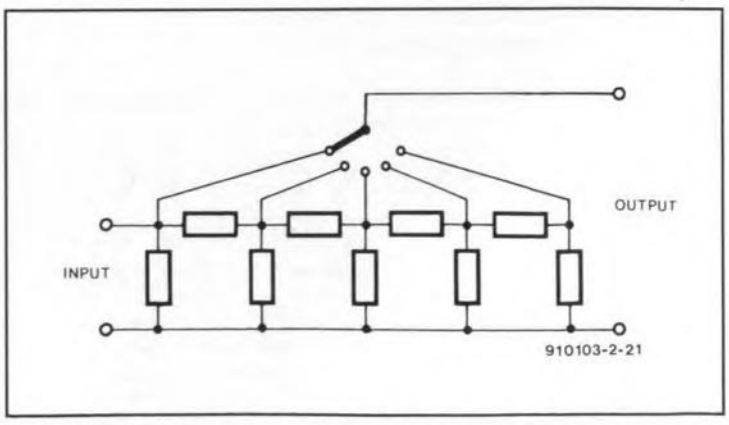


Fig. 18. An alternative switching system—more difficult to screen adequately.

A SIMPLE WATCHDOG CIRCUIT

by Akbar Afsoos

SINGLE-CHIP microcontrollers have been designed and optimized for specific applications such as industrial control and automotive applications. The Intel MCS-51 family of microcontrollers is a popular and typical example.

The presence of various types of electrical noise and interference in the above mentioned applications is by no means taken for granted, but generally accepted as hard to avoid. By virtue of some special features, such as powerful Boolean processing capabilities, single-chip microcontrollers are mostly used in industrial control applications which are known as electrically noisy environments.

In spite of a well-designed power supply, a shielded enclosure, and adequate decoupling provisions, noise may still enter a microcontroller system, upsetting the normal operation, or even causing a system crash. These situations are usually marked by the microprocessor going into its static state, or performing unpredictable operations. In such a case, normal operation can be restored only by a hardware reset (PC users know this as BRST — Big Red Switch Time).

A problem occurs when the microprocessor system operates unattended, which is usually the case in industrial applications. A total lockup of the system can then disrupt a production line, or cause expensive 'down time'. In such applications, hardware resetting must be performed automatically on detection of a software malfunction. The circuit described here (Fig. 1) provides a simple method to accomplish this.

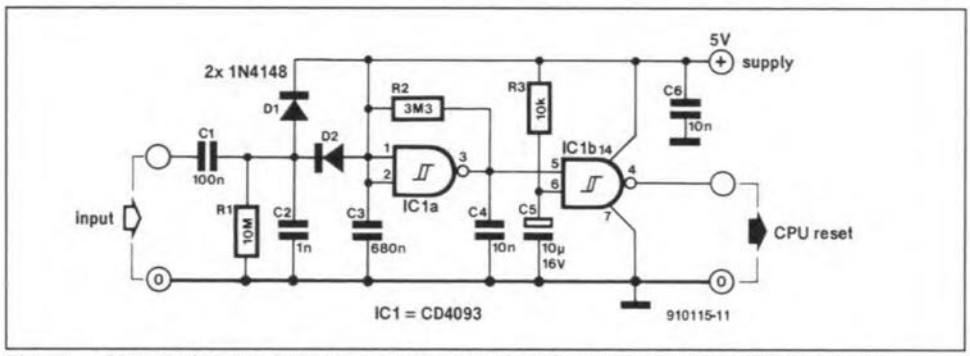


Fig. 1. Circuit diagram of the watchdog. The input is connected to a CPU port line.

Circuit description

The watchdog circuit consists of a power-up reset, a gated astable multivibrator, and a failure detector circuit. In fact, the total circuit simulates a retriggerable monostable multivibrator, which detects a software upset whenever it is not triggered at a proper rate.

In the MCS-52 family of microcontrollers, PX.X can be any pin (bit) of the ports 1, 2 or 3. Ports 2 and 3 may not be used when performing their secondary functions. Components R3 and C5 form a power-up reset circuit that applies a reset pulse to the CPU via gate IC1b, whenever power is applied.

During normal operation, and in the main loop of the program, a periodic pulse must appear on port line PX.X. The frequency of this signal must be at least 10 Hz. The software determines which port line is used to keep the watchdog triggered. In 8051 assembler code, this is simple to implement by the instruction CPL PX.X, where X.X is the port line identification, e.g. 1.0 (bit 0 of port 1).

The software failure detector consists of C1, R1, D1 and D2. The pulse train applied to the PX.X input of the circuit continuously discharges C3 via D2 and C1. As a result, the gated bistable around gate IC1a is disabled, and its output goes high. Hence, during normal program execution, the two inputs of IC1b are high, so that the CPU reset line is held low.

As soon as a software upset occurs, the CPU very likely leaves the main loop of the program. This means that the pulses on PX.X fail, so that the port line takes on a static level. This enables the astable circuit which consists of IC1a, R2 and C3. After C3 has been fully charged by R2, the output of IC1a goes low. Consequently, a logic high reset pulse appears at the output of IC1b.

Because IC1a functions as an astable multivibrator, C3 is discharged again after about one second, so that the output of IC1a goes high. This causes the CPU reset line to revert to logic low, and the control program is executed starting at the reset address. The CPU has enough time (about one second) to restart the pulse train on PX.X, and resume its normal operation.

The reaction time of the watchdog may be shortened by using a smaller capacitor in position C3. Capacitors C2 and C4 reduce the effect of noise on the operation of the circuit. If a reset key is required, you can connect a pushbutton in parallel with capacitor C5.

This circuit may also be used with any of the devices in the Intel MCS-48 family of single-chip microcontrollers. This, however, requires an inverter gate to be inserted between the output of IC1b and the CPU reset line, because these controllers have active-low reset inputs. ■

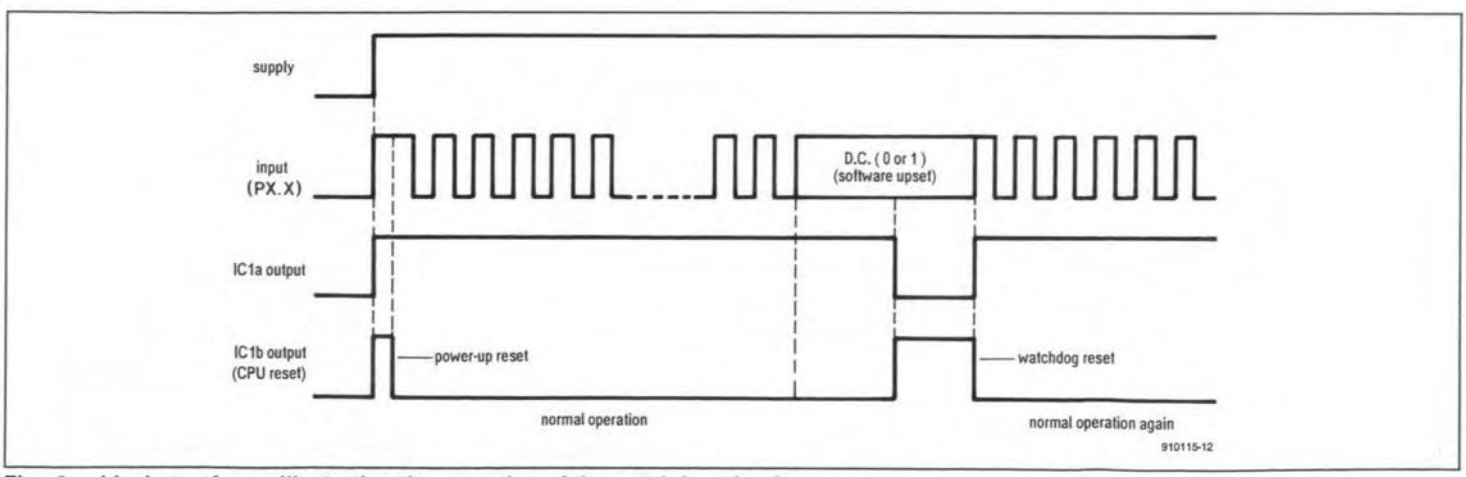


Fig. 2. Ideal waveforms illustrating the operation of the watchdog circuit.

THE CIPHER MACHINE

This project is a playful introduction into message scrambling, intended as a mind-teaser or a toy for the junior members of the family.

by Owen and Audrey Bishop

SINCE antiquity, the scrambling of the letters in a message has been a popular though elementary method of encryption. One of the earliest techniques was to write out the message in the rows of a square, or rectangular array of prearranged shape and size:

```
THISIS
ISNOTA
HIGHLY
SECURE
SYSTEM
```

The message is then written out by columns:

```
TIHSSHSIEYINGCSSOHUTITLRESAYEM
```

Needless to say, anyone who knows anything at all about ciphers will have no difficulty in breaking such a simple scrambled message. Another well-established method is to group the letters of the alphabet into pairs, and then exchange one member of a pair for the other when writing out the message. The pairs are usually determined by beginning with an agreed key-word, followed by the remaining letters in order:

```
MACHINEBDFGJK
LOPQRSTUVWXYZ
```

To encrypt the message, letters in the top row are exchanged for those in the bottom row, and the other way about.

Fig.1. Representing letters and numerals on a 7-segment LED display.

Message:
```
ALSO FAIRLY EASY TO BREAK
```
Cipher:
```
OMNA WORIMJ TONJ EA UITOZ
```

In this project we carry the idea of transposition into the letters themselves. We take the strokes used to write the letter, and scramble them by swapping them in pairs. The result is either a different letter or a weird and unrecognizable symbol. Most alphabetic and numeric characters can be written using the 7-segment matrix commonly employed in pocket calculators and digital clocks. Unfortunately, there are some problems in representing certain letters such as 'M', 'W' and 'X'. For these and a few others, a 16-segment 'starburst' matrix gives a better image, but such devices are expensive. This is intended to be a cheap, easy-to-wire, project for you to build for the youngsters. You may even want to build two, so that they can exchange messages.

So we have settled for a 7-segment display, even though there are difficulties with a few of the more 'awkward' letters. The scheme works better if we use a lower-case alphabet (Fig. 1). We make use of the eighth segment of the display, the decimal point, to distinguish 'm', 'u', 'w' and 'x'. This is used to represent a central vertical segment in the bottom half of the array.

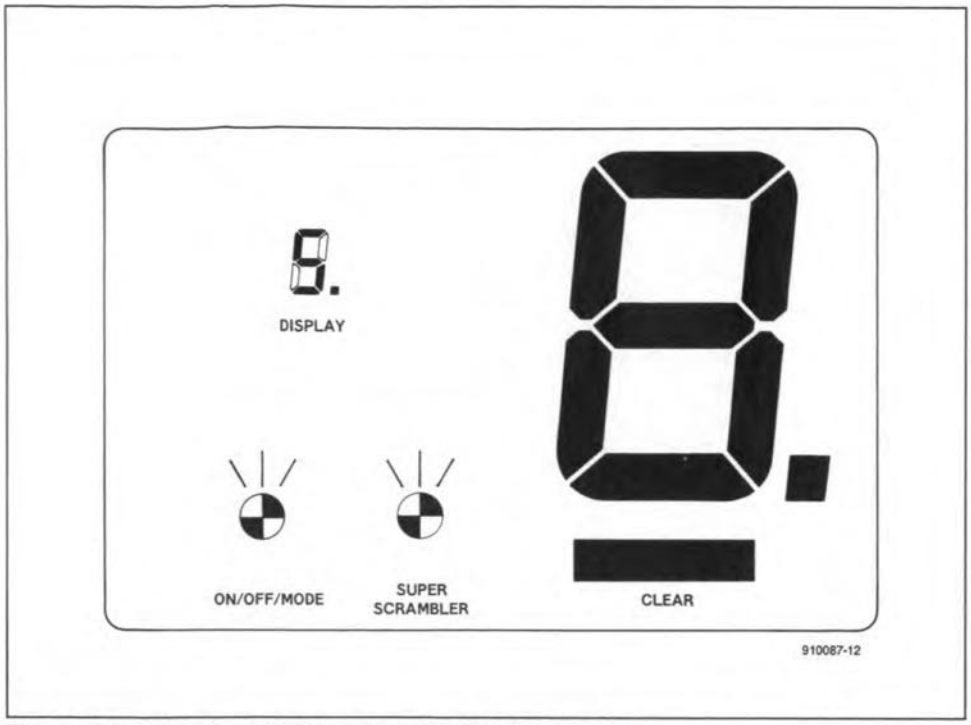


Fig. 2. Suggested layout of the panel of the Cipher machine.

Practical use

The Cipher machine is used as follows. The letters or numerals of the message are entered one at a time by touching the appropriate segments of a 7-segment key-panel with a stylus (See Fig. 2.). The scrambled version of the character appears on a 7-segment LED display, and this is copied down onto paper. The receiver of the message has a Cipher Machine with identical wiring (or uses the same machine), and enters the symbols on to the key-plate. The machine unscrambles the segments, reproducing the original letter or numeral on the 7-segment display.

Choice of display

The original version of this project simply scrambled the segments, producing characters such as those in Fig. 3. The weakness of this technique lies in the fact that the scrambled character has the same number of segments as the regular character. This is a clue to the identity of the letter. For example, a 3-segment symbol obviously comes from a 3-segment letter, either 'c', 'n' or 'v'. It is usually easy to decide, for other reasons, which one of these it must be. Worse still, if the letter has only a few segments (for example, 'c' in Fig. 3), when the symbol tends to end up as a number of disconnected strokes. Such symbols are difficult to write convincingly. They also further advertise the fact that the system depends on interchanging segments.

To make unauthorized deciphering more difficult, the Cipher Machine logically inverts the scrambled segments when there are fewer than four. For example, the letter 'l' (or figure '1'), has only 2 segments, but is displayed as a 5-segment symbol (Fig. 4). This procedure has the advantage of increasing the average number of segments making up the symbols, giving them a more 'connected' appearance. There are a few exceptions to this inversion routine, for reasons which will be explained later.

Table 1. Ciphering rules

Case	Original character	Ciphered symbol	*b* lit?
A	1, 2 or 3 segments, not including *h*	All segments inverted	Yes
B	1, 2 or 3 segments, plus *h*	*h* inverted, rest not inverted	No
C	4 to 7 segments, not including *h*	None inverted	No

Table 2. Deciphering rules

Case	Ciphered symbol	Deciphered character	*h* lit?
A	4 to 7 segments, including *b*	All segments inverted	No
B	1, 2 or 3 segments, not including *b*	*b* inverted, rest not	Yes
C	4 to 7 segments, not including *b*	None inverted	No

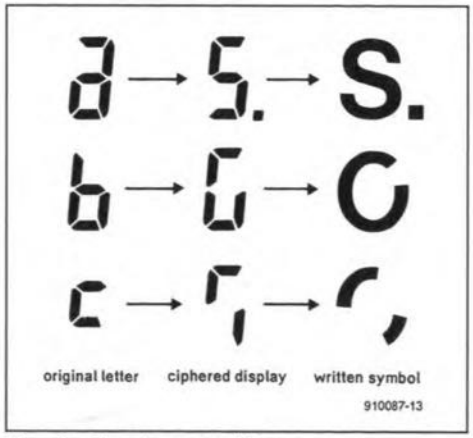


Fig. 3. Simple scrambling.

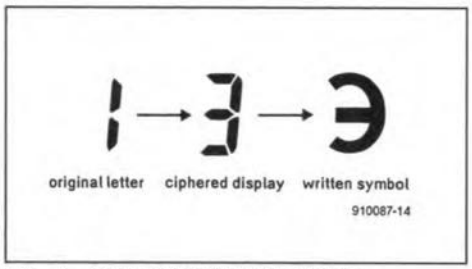


Fig. 4. Scrambling with inversion.

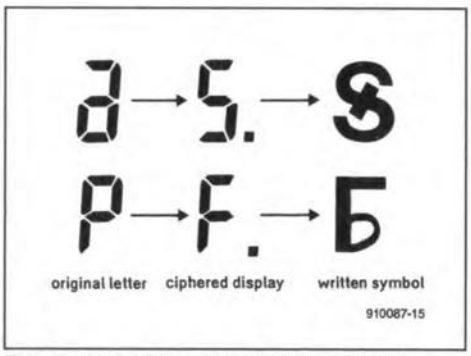


Fig. 5. Use of the 'wild card' segment.

Scrambling twists

Another twist to confuse the snooper is the way we use the decimal point (segment *h* of the display), when this comes up as one of the scrambled segments. We think of this as a 'wild card' which can be added to the symbol anywhere that is not part of the 7-segment matrix, as in Fig. 5. You can add the 'wild card' in different places each time it occurs, producing a confusing set of variations that all represent the same letter.

Finally, there is the super-scrambler option. This consists of a 3-position switch that varies the scrambling of four pairs of segments. This switch is set to a given position before ciphering begins. The authorized recipient knows the setting, and uses this when deciphering. All sorts of routines can be used by prior agreement, such as to alter the switch at the start of each paragraph, or even for each word or letter, according to a regular system.

Circuit details

The eight segments of the key-panel are connected to the SET input of a set-reset bistable (flip-flop) (Fig. 6). The SET input is normally held logic high by a pull-up resistor, R1-R8.

When a segment is touched by grounded stylus, the low input to the corresponding bistable causes its Q output to go high. The RESET inputs of these bistables are all connected to a single CLEAR pad on the keypanel, and are held logic high by R9. Touching the CLEAR pad with the stylus resets all the bistables, and their outputs go low. Thus, the bistables store the segments that make up the character.

The output of each bistable goes to one input of an XOR (exclusive-OR) gate. When the inputs of the gates are low, the output of each gate has the same state as the corresponding bistable. If the other inputs are high, the output of each gate is the inverse of the bistable outputs. For example, if pad *a* is touched, the first bistable in IC1 is set, and its output, pin 13, goes high. If pin 2 of IC3 is low, pin 3 of IC2 goes high, and the LED segment *g* is lit. If pin 2 is high, the segment is not lit. The pads and the LED segments are in exchanged pairs so that, for example, touching pad *a* lights (or turns off) segment *g* on the display. Conversely, touching pad *g* lights (or turns off) LED segment *a*.

The circuit diagram shows just one permutation for scrambling. The super scrambler switch, S1, gives a variable pairing between segments *c* to *f*. This part of the circuit is open to modification. Many different combinations of any four of segments *a* to *g* can be wired to the super scrambler switch, and those four segments not so wired can be paired in three different ways. Th only restriction is that *h* and its partner may not be wired to the super scrambler switch. If you want to be able to use one machine for ciphering, and another for deciphering, both machines must be wired exactly alike.

The lower part of the circuit diagram shows the logic switch that decides when segments are to be inverted. The logic is summarized in Table 1.

In case 'A' we obtain a symbol with five to seven lit segments, plus *b* (assuming that *h* has been scrambled with *b*, as in the schematic). The letters included in case 'B' are the 'm', 'u', 'w' and 'x', all of which require the use of the *h* segment. Since we rely on the state of *h* (scrambled to *b*) when deciphering, we have no compromise by not inverting the segments of these few letters. Case 'C' includes all other letters with three or fewer

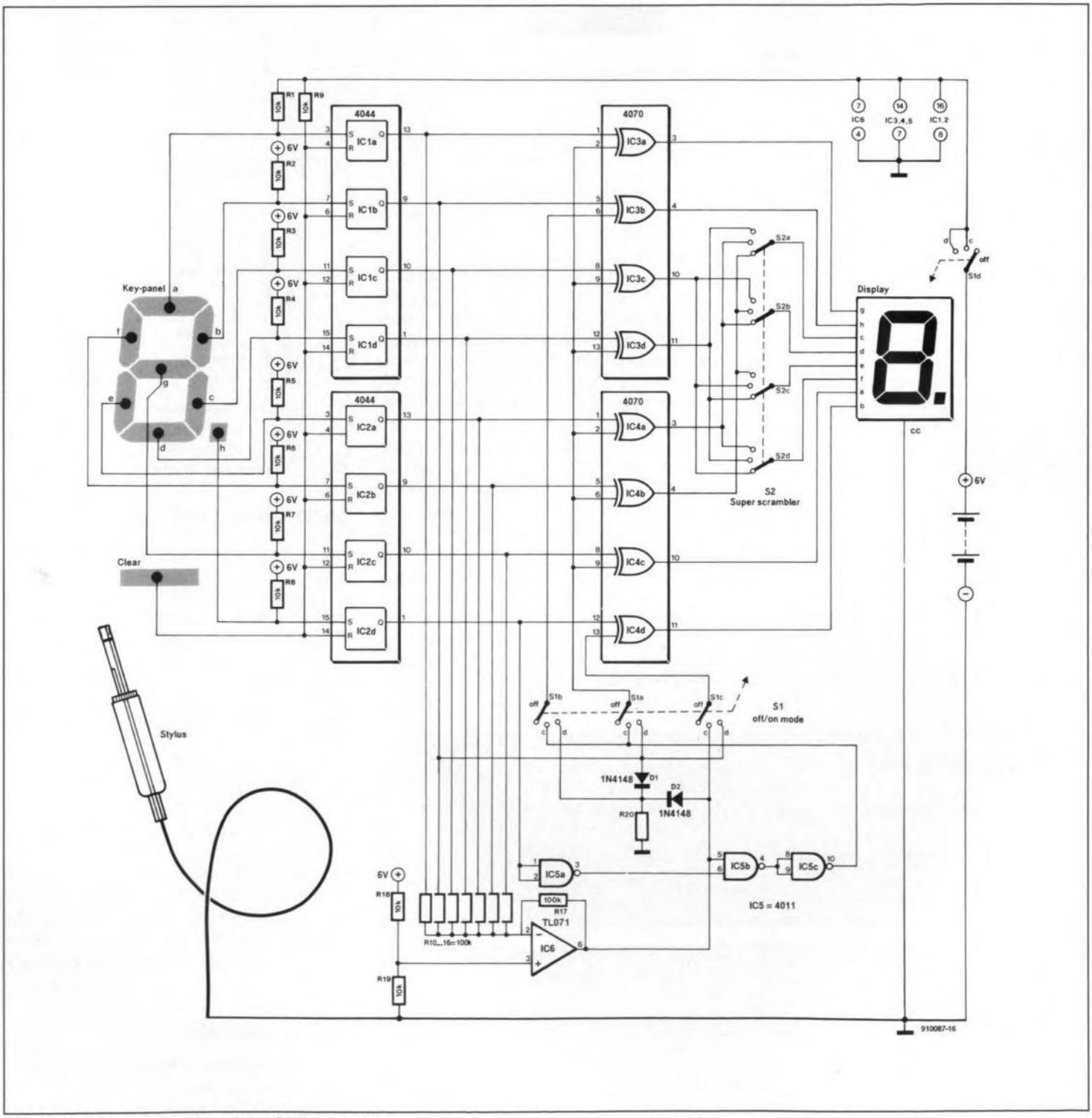


Fig. 6. Schematic diagram of the Cipher machine.

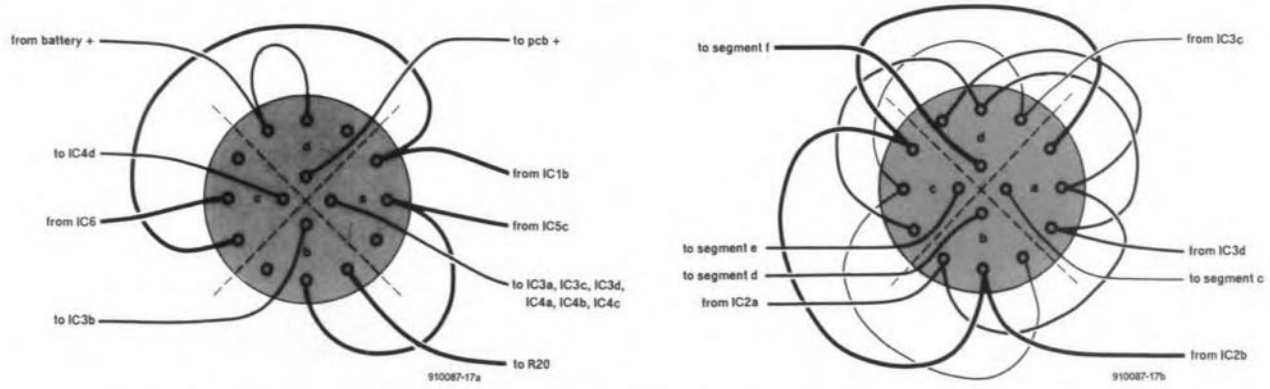


Fig.7. (a) Wiring of S1, as seen from the rear. (b) Wiring of S2, as seen from the rear.

segments. There are no characters that have four to seven segments **and** *h*.

From Table 1, we establish three rules for ciphering:

1. Invert *a* and *c* to *g* if there are one to three segments of *a* to *g* set, **and** *h* is not set (case 'A');

2. Invert *b* for the same conditions as in Rule 1 (Case 'A');

3. Invert *h* if there are one to three segments of *a* and *c* to *g* set (case 'B').

The number of segments set is 'counted' by an operational amplifier, IC6, wired as a summing amplifier. We could have used a digital equivalent, but no 7-input gate is available 'off-the-shelf'. This substitute is considerably less complex to wire up than a digital version made of discrete gates. The summing action is also accompanied by inversion. When three or fewer bistables have a high output, the output of the operational amplifier swings fully high. When four or more have a high output, the amplifier swings fully low.

When there are one to three segments lit, the output of IC6 is high; this is fed by way of S1c to IC4d, the XOR gate for segment *h*, which is thus inverted, causing segment *b* to remain off. This complies with Rule 3 above. The output of the *h* bistable is inverted by IC5a, so its output is high when *h* is not set. The output of IC6 is high when one to three segments are set. The two high inputs to the NAND gate, IC5b, make its output go low, and this is inverted by IC5c. Through switches S1a and S1b, this causes high levels at the inputs of the XOR gates, inverting segments *a* to *g*, and conforming to Rules 1 and 2.

The rules for deciphering are slightly different, which is why we need S1 to switch between ciphering (C) and deciphering (D) modes. The conditions for deciphering are given in Table 2. The logic for Rules 4 and 6 is effected by S1a and S1c connecting the output of the *b* bistable to the inputs of the XOR gates *a* and *c* to *g*. The outputs of IC6 and the *b* bistable need to be ORed together to perform deciphering Rule 5. Instead of installing an extra IC to provide an OR gate, we have used 'Mickey-Mouse' logic: the two diodes D1 and D2, and a 10-kΩ pull-down resistor, R20.

Construction

Since the Cipher Machine was intended as a not-too-serious toy for the junior members of the family, the prototype was built in a brightly-coloured novelty form (see the introductory photograph). The enclosure is a food storage box with a clear snap-on lid. This exposes the 'works' for all to see, so the battery holder, PCB, switches, ICs and other components are painted in red, blue and yellow. We also bought plastic knobs for S1 and S2.

There is no limit to the variety of the colour schemes you can employ but, if you prefer a rather different image, the project could be realized as a rugged all-black 'military-look' device. Alternatively, you could disguise it as a radio set, or even as a bound volume to hide away on the bookshelf.

The circuit should not be too difficult to build on a piece of Veroboard or stripboard. The battery holder is glued to the bottom of the enclosure, and special self-adhesive PCB mounting strip is used for the circuit board. The area around the display is shielded from direct light by a cylinder painted matt black inside, and a bright tint outside. The cap from a spray can makes a suitable shield.

The key-pads are laid out as an array of strips of coloured PVC insulating tape. A narrow hole is drilled at the centre of each strip, and through the lid below. A brass thumb-tack is pushed into each hole to form the contact for the stylus. Wire is wrapped around the pin of each tack, and soldered to it. The lid of our enclosure was made of high-impact polystyrene or similar plastic, so care was needed not to shatter it by over-enthusiastic drilling. The two switches are also mounted on the lid. Their decorative effect is enhanced by looping out the connecting wires in the shape of flower petals, as shown in Fig. 7. A hole is drilled in one side of the enclosure for the lead to the stylus.

There are no alignment problems: if correctly assembled, the Cipher Machine should work first time. The detailed description given above should help you iron out any discrepancies. ■

OPERATING INSTRUCTIONS

Ciphering

1. Switch on and turn to cipher mode (C).

2. Set the super-scramble switch to any one of the positions you have agreed with your correspondent.

3. Touch the stylus to the CLEAR pad.

4. To encipher the first letter or numeral of the message, touch the stylus to the segments that contain it (Fig. 1).

5. Copy on to paper the symbol that appears on the display. If possible, make it more 'rounded' like a hand-written character. If the decimal point on the display is lit, add a stroke anywhere you like, but not where the seven segments of the display are located.

6. Repeat steps 3 to 5 for each character of the message. Leave a space between words, or devise a special 'space' symbol, making sure it is not one that deciphers into a regular letter or numeral.

Deciphering

1. Switch on and turn to decipher mode (D).

2. Set the super-scramble switch to the position that you have agreed with the sender of the message.

3. Touch the stylus to the CLEAR pad.

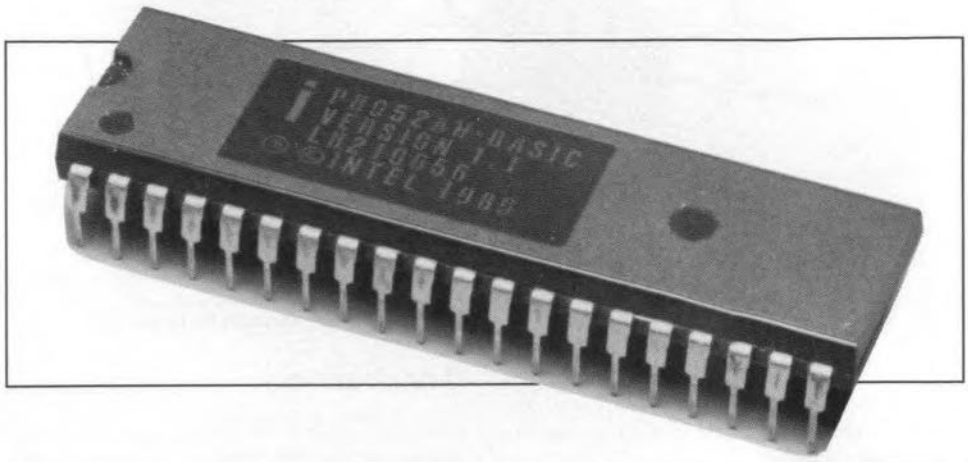
4. To decipher the first symbol, touch the stylus to the segments that it contains. If it includes a 'wild card' stroke, touch the decimal point.

5. Copy on to paper the character that appears on the display. If the decimal point is lit, it indicates one of the letters 'm', 'u', 'w' or 'x', depending on which other segments are lit.

6. Repeat steps 3 to 6 for each symbol of the message.

UPGRADE FOR MCS BASIC-52 V.1.1 (Part 2)

Following last month's dealings with the floating-point nucleus and the hex-to-BCD conversion routine in the MCS-52 BASIC interpreter, the authors now tackle some problems with multiplications.



by Z. Stojsavljevic and D. Mudric

Continued from the October 1991 issue.

INCONSISTENCIES in the multiplication of two numbers as performed by version 1.1 of Intel's MCS BASIC-52 interpreter can be demonstrated by running the following three small programs, all of which produce wrong results.

```
10    a=1.E-65
20    b=1.E-65
30    ?a*b          (result: 1.0E+126)

10    a=1.E-65
20    b=1.E-64
30    ?a*b          (result: 0)

10    a=1.E-64
20    b=1.E-64
30    ?a*b          (result: 1.0E-0)
```

In all three cases, the interpreter should have produced

ERROR: ARITH. UNDERFLOW - IN LINE 30

The above examples point to inconsistencies in limit cases when two numbers are multiplied. On investigating the operation of Intel's BASIC interpreter, a multiplication algorithm of the type shown in Fig. 1 was found. Apparently, the inconsistencies brought to our attention by the above example programs were caused by the exponent adjustment routine, which is listed in Fig. 2. Unfortunately, the errors found in this routine cannot be corrected in BASIC-52 machine code, because some expansion of the machine code is in order. This means that a number of lines should be added to the assembler source file for compensation.

A problem occurs when the result of the instruction SUBB A,#81H is 0FFH, which equals exponent E+127. If the program part for mantissa multiplication includes a result that begins with a 0 after the decimal point, the exponent is not incremented but remains

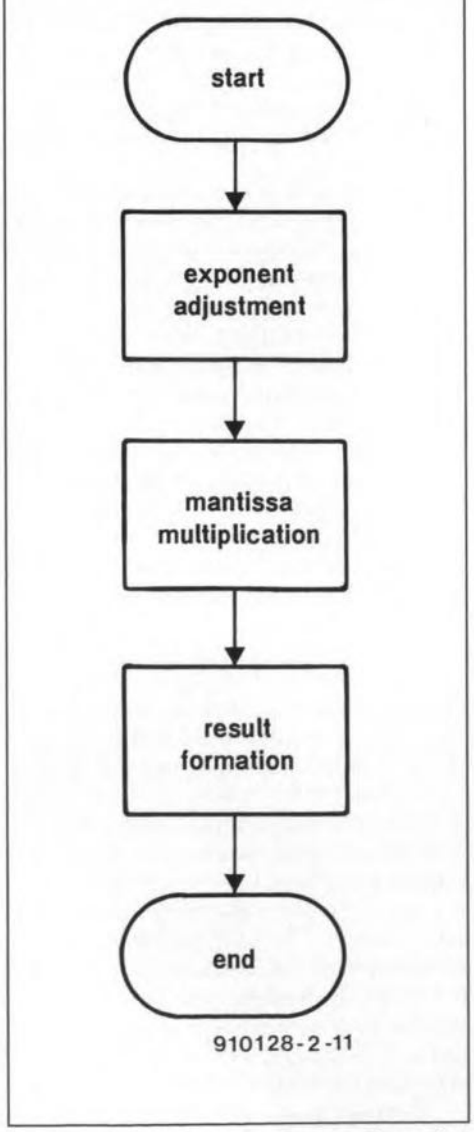


Fig. 1. Flowchart of the routine that handles multiplication of two numbers.

```
1A9AH 9175      ACALL   1C75H
1A9CH BE0002    CJNE    R6,#00H,1AA1H
1A9FH 61B8      AJMP    1BB8H
1AA1H 8D2F      MOV     2FH,R5
1AA3H EF        MOV     A,R7
1AA4H 60F9      JZ      1A9FH
1AA6H 2E        ADD     A,R6
1AA7H 20E705    JB      ACC.7,1AAFH
1AAAH 10D706    JBC     CY,1AB3H
1AADH 61B2      AJMP    1BB2H
1AAFH 5002      JNC     1AB3H
1AB1H 61A1      AJMP    1BA1H
1AB3H 9481      SUBB    A,#81H
1AB5H FE        MOV     R6,A
1AB6H 718B      ACALL   1B8BH
1AB8H 7B04      MOV     R3,#04H
1ABAH AC01      MOV     R4,01H
1ABCH 8C01      MOV     01H,R4
1ABEH E3        MOVX    A,@R1
1ABFH FA        MOV     R2,A
1B30H 7834      MOV     R0,#34H
1B32H E6        MOV     A,@R0
1B33H FE        MOV     R6,A
1B34H 6003      JZ      1B39H
1B36H 717F      ACALL   1B7FH
1B38H 18        DEC     R0
1B39H 08        INC     R0
1B3AH 7408      MOV     A,#08H
1B3CH F9        MOV     R1,A
1B3DH 28        ADD     A,R0
1B3EH F8        MOV     R0,A
1B3FH B60500    CJNE    @R0,#05H,1B42H
1B42H 4013      JC      1B57H
1B44H D3        SETB    C
1B45H E4        CLR     A
1B46H 18        DEC     R0
1B47H 36        ADDC    A,@R0
1B48H D4        DA      A
1B49H D6        XCHD    A,@R0
1B4AH 30E409    JNB     ACC.4,1B56H
1B4DH D9F5      DJNZ    R1,1B44H
1B4FH 18        DEC     R0
1B50H 7601      MOV     @R0,#01H
1B52H 717F      ACALL   1B7FH
1B54H 8006      SJMP    1B5CH
1B56H 19        DEC     R1
1B57H E9        MOV     A,R1
1B58H C3        CLR     C
1B59H C8        XCH     A,R0
1B5AH 98        SUBB    A,R0
1B5BH F8        MOV     R0,A
1B5CH 792B      MOV     R1,#2BH
1B5EH E6        MOV     A,@R0
1B5FH C4        SWAP    A
1B60H 08        INC     R0
1B61H D6        XCHD    A,@R0
1B62H 4206      ORL     06H,A
1B64H F7        MOV     @R1,A
1B65H 08        INC     R0
1B66H 09        INC     R1
1B67H B92FF4    CJNE    R1,#2FH,1B5EH
1B6AH EE        MOV     A,R6
1B6BH 7003      JNZ     1B70H
1B6DH 753000    MOV     30H,#00H
1B7FH 0530      INC     30H
1B81H E530      MOV     A,30H
1B83H 70F9      JNZ     1B7EH
1B85H D0E0      POP     ACC
1B87H D0E0      POP     ACC
1B89H 61A1      AJMP    1BA1H
```

910128-2-12

Fig. 2. Original program part for exponent adjustment.

```
        ORG     1A9AH

        ; TOS   - Top Of arithmetic Stack
        ; NXTOS - NeXt TOS (position behind)

        ; TOS_MUL1
        ; routine for multiplication of two FP numbers, one of which
        ; is located on TOS and the other on NXTOS (NXTOS*TOS)

TOS_MUL1:ACALL  PREP_MUL; clearing of FP working space and reg. prep.
         CJNE   R6,#0,NXTNM_0   ; is NXTOS equal 0?
TOSM_0:  AJMP   ZERO_MANTISSA   ; in case TOS or NXTOS are 0
NXTNM_0: MOV    SIGN,R5         ; result mark in SIGN
         MOV    A,R7    ; is TOS equal 0?
         JZ     TOSM_0
         ADD    A,R6    ; addition of exponent degree (exp. multipl.)
         JB     ACC.7,CMPM_EXP  ; exp. with different mark or overflow?
         JBC    CY,CORM_EXP     ; result is bigger than 0.1
         AJMP   UNDERFLOW       ; in this case exp. sum is < -127
CMPM_EXP:JNC    CORM_EXP; in this case result is smaller than 0.1
OVER_MD: AJMP   OVERFLOW; in this case exp. sum is > 127
CORM_EXP:CLR    MUL_LIMIT_CASE  ; flag of multiplication limit case
         SUBB   A,#82H  ; exp. multipl. results are within the limits
         INC    A       ;  deduction  with  82H  because  of  reduced
         JNC    NMARK_L ;  conditions
         SETB   MUL_LIMIT_CASE  ; limit case
NMARK_L: MOV    R6,A    ; exp. adjustment to real value
         ACALL  BCD2_1  ; disassembl. of TOS mantissa in LEN_MANTISSA
         MOV    R3,#LEN_BYTE    ; acc. (one number in each byte)
         MOV    R4,AR1  ; R1 is pointer of NXTOS
MUL_NOOV:MOV    AR1,R4  ; @R1 contains few numbers and disassembled
         MOVX   A,@R1   ; mantissa is successively multiplied by each
         MOV    R2,A    ; of  them  in  argument  accumulator  (R2  is
                        ; auxilliary register)

-----------------------------------------

        ; TRANSFER
        ; routine  for  adjustment  of  multiplication  and  division
        ; results of  FP  numbers  in  argument  stack  and  mantissa
        ; conversion in BCD packed  format  in  argument  accumulator

TRANSFER:MOV    R0,#ASCII_DEC   ; pointer to MSB result number
         MOV    A,@R0   ; MSB result number is in acc.
         MOV    R6,A
         JZ     MSB_EQ_0; is MSB result number equal 0?
         ACALL  INC_EXP ; exp=exp+1 because from the start it was
         DEC    R0      ; taken that MSB result number is equal 0
MSB_EQ_0:INC    R0      ; pointer to MSB-1 number
         MOV    A,#LEN_MANTISSA ; positioning to LSB-1 number
         MOV    R1,A    ; R1 is counter
         ADD    A,R0
         MOV    R0,A    ; R0 contains the address of LSB-1 number
         CJNE   @R0,#05,ROUND1  ; test of remainder to rounding
ROUND1:  JC     NO_ROUND; in case remainder is smaller than 5 there
C_BCD:   SETB   C       ; is no rounding
         CLR    A       ; carry takes one because of rounding
         DEC    R0      ; transfer of carry into higher byte
         ADDC   A,@R0   ; addition of 1 to higher byte
         DA     A       ; adjustment to BCD format
         XCHD   A,@R0   ; result storing in higher byte
         JNB    ACC.4,NO_C_BCD  ; transfer in higher BCD nibble?
         DJNZ   R1,C_BCD; is @R0 the address of MSB number?
         DEC    R0      ; transfer memorizing in the place MSB+1
         MOV    @R0,#01
         ACALL  INC_EXP ; transfer is outside decimal point frame
         SJMP   BCD1_2
NO_C_BCD:DEC    R1
NO_ROUND:MOV    A,R1    ; address return in R0 to the first bigger BCD
         CLR    C       ; number which is not equal 0
         XCH    A,R0
         SUBB   A,R0
         MOV    R0,A
BCD1_2:  MOV    A,EXPONENT      ; test of exceeding in limit case
         JNB    MUL_LIMIT_CASE,N_LCASE
         JZ     UNDER_MD; message about underflow
         INC    A
         JZ     UNDER_MD; message about underflow
N_LCASE: MOV    R1,#ARGUMENT_ACC; repacking of BCD number in one byte
XFER_1:  MOV    A,@R0   ; in two BCD numbers in one byte
         SWAP   A       ; higher number in BCD packed  format is in
         INC    R0      ; upper nibble
         XCHD   A,@R0   ; BCD packed format is in ACC
         ORL    AR6,A   ; the indication if mantissa is 0 is in R6
         MOV    @R1,A   ; packing in argument accumulator mantissa
         INC    R0      ; two BCD packed numbers in one byte
         INC    R1
         CJNE   R1,#SIGN,XFER_1
         MOV    A,R6
         JNZ    RESULT_MAT_OP_TOS       ; is mantissa equal 0?
         MOV    EXPONENT,#0

-----------------------------------------

INC_EXP: INC    EXPONENT; exp. adjustment by 1 (consequence of
         MOV    A,EXPONENT      ; transfer after addition)
         JNZ    EXP_OK  ; test of exponent exceeding
         POP    ACC     ; removal from return address stack
         POP    ACC
         JBC    MUL_LIMIT_CASE,UNDER_MD ; in limit case it is
         AJMP   OVERFLOW; underflow
UNDER_MD:AJMP   UNDERFLOW
```

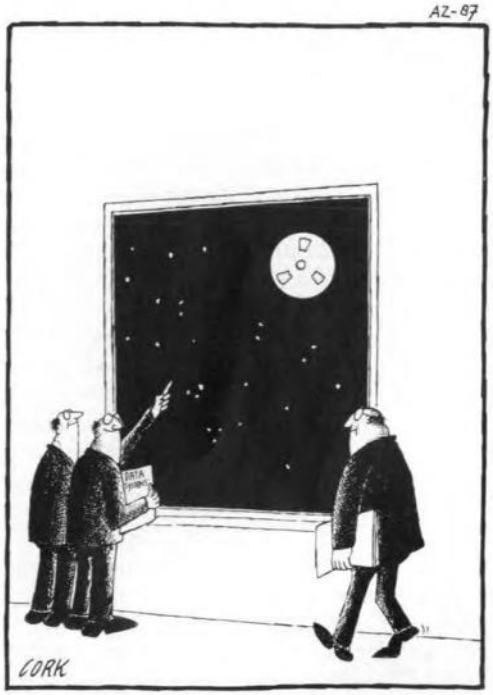
910128-2-13

Fig. 3. Source code of the improved multiplication routine. The vertical bars indicate lines that correct the limit case multiplication errors mentioned in this article.

0FFH. After the result formation (see Fig. 1) and the serial output (display) routine, this gives an exponent E+126.

To avoid inconsistencies, and eliminate errors in limit case multiplications, the program listed in Fig. 3 was developed. The lines marked by vertical bars in particular correct the limit case multiplication errors.

On the basis of the information contained in this and last month's instalment, the authors developed an improved, error-free floating-point (FP) arithmetic for the 8051, on the basis of the FP nucleus extracted from the 8052AH-BASIC. The new FP nucleus uses a modified way of accessing the arithmetic stack, and has faster, shorter code for a number of algorithms. It allows the length of the mantissa of a FP number to range from 2 to 16 digits, while the entire memory map of the FP arithmetic variables is located in the internal memory space of the 8051 microcontroller. ■

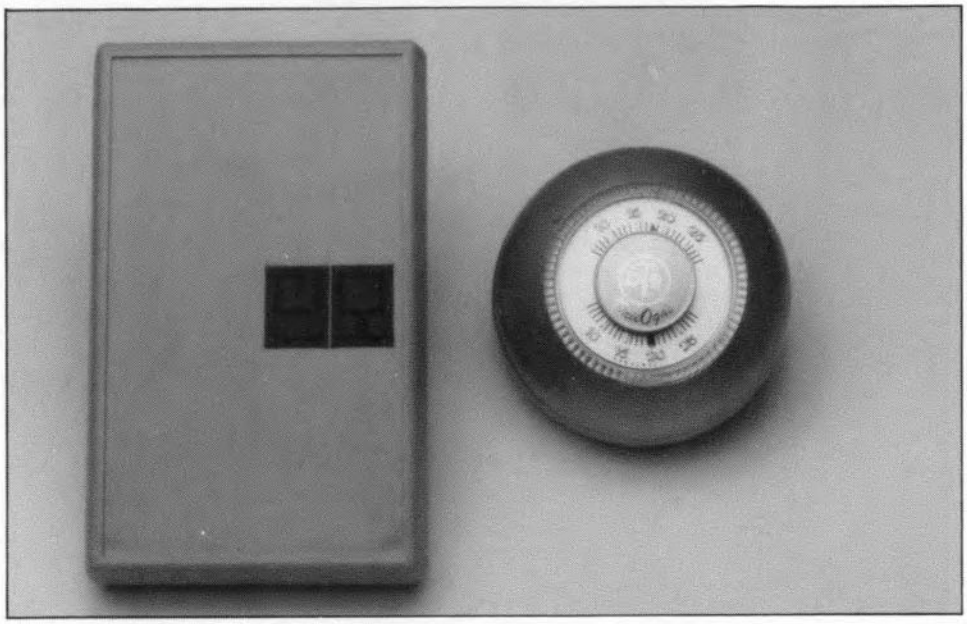


INTERMEDIATE PROJECT

A series of projects for the not-so-experienced constructor. Although each article will describe in detail the operation, use, construction and, where relevant, the underlying theory of the project, constructors will, none the less, require an elementary knowledge of electronic engineering. Each project in the series will be based on inexpensive and commonly available parts.

TIMER FOR CENTRAL HEATING SYSTEMS

To achieve a comfortable room temperature quickly it is often required to switch on the central heating (CH) boiler for ten minutes or so, for instance, in the morning, or when you get home from work. Unfortunately, most CH systems can be switched on only by turning up one of the room thermostats. This works, but if you forget to turn it down again, the resultant hothouse is not only unhealthy but also a waste of energy.



by J. Ruffell

THE circuit described here is a timer that can be connected to most types of CH room thermostats, including the well-known Honeywell types and look-alikes (see the above photograph). Its function is to actuate the CH boiler (and pump) for a certain period, overriding the thermostat output. Unlike you, it is not in the habit of forgetting to turn the boiler off again — all you have to do is press a button to start the timer. The circuit is simple to build, and conveniently fitted next to the room thermostat.

How it works

The timer is actually a monostable multivibrator with an adjustable on-time. The circuit diagram in Fig. 1 shows that a 4060 ripple counter IC is used as the timing device. The 4060 has an on-board oscillator,

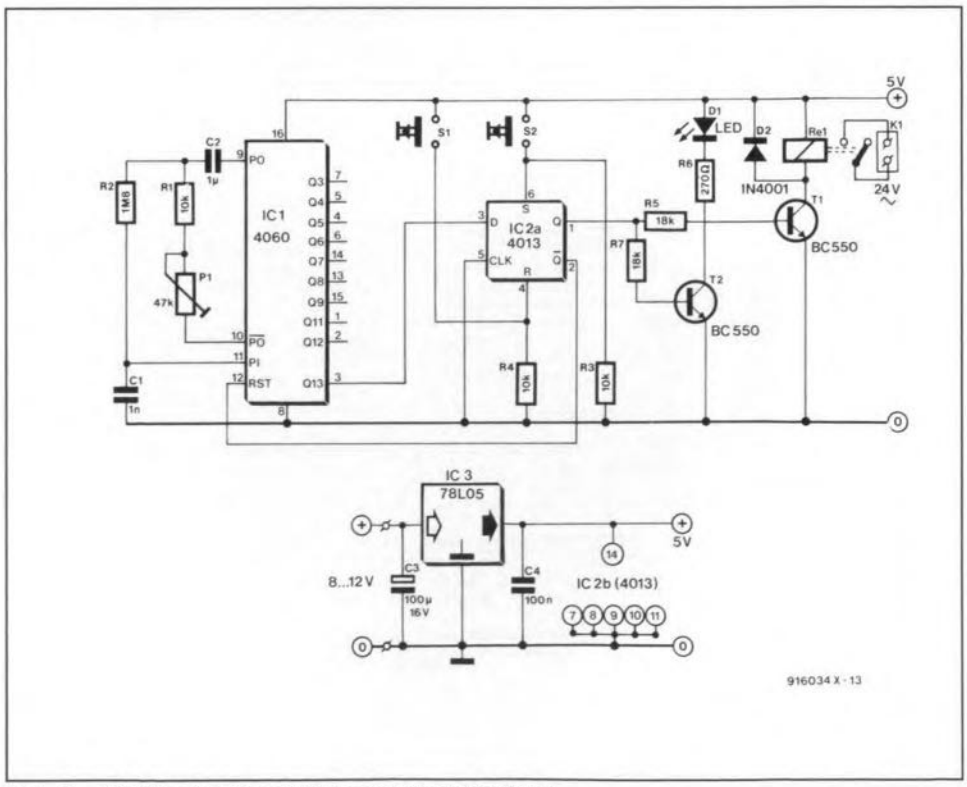


Fig. 1. Circuit diagram of the central heating timer.

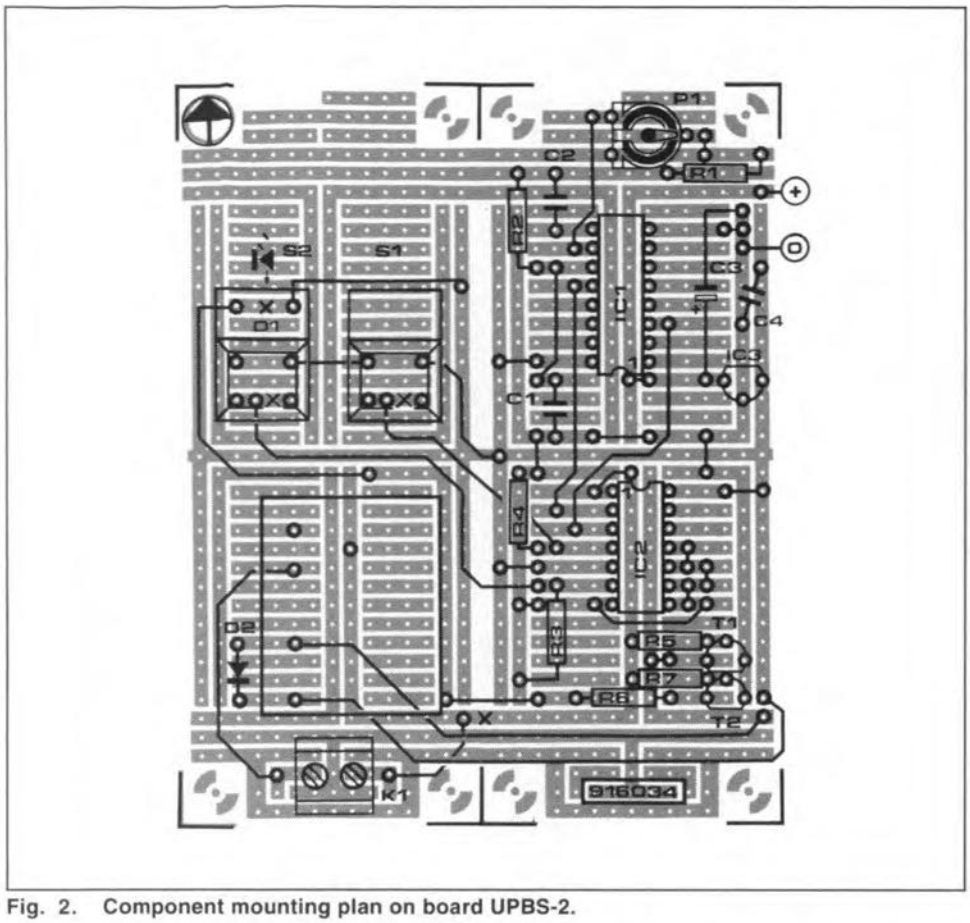


Fig. 2. Component mounting plan on board UPBS-2.

COMPONENTS LIST

Resistors:

3	10kΩ	R1;R3;R4
1	1MΩ8	R2
2	18kΩ	R5;R7
1	270Ω	R6
1	50kΩ preset H	P1

Capacitors:

1	1nF	C1
1	1µF solid MKT	C2
1	100µF 16V axial	C3
1	100nF	C4

Semiconductors:

1	4060	IC1
1	4013	IC2
1	78L05	IC3
2	BC550	T1;T2
1	LED	D1
1	1N4148	D2

Miscellaneous:

1	V23127-A0001-A101 (Siemens) or similar 5-V PCB-mount relay	Re1
1	push-button with LED hole	S1
1	push-button	S2
1	2-way terminal block	K1
1	printed circuit board	UPBS-2

which is connected here to a resistor-capacitor network, R1-P1-R2-C1-C2. These components, connected to the PO (phase out), $\overline{PO}$ (phase out inverted) and PI (phase in) pins of the 4060 determine the oscillator frequency. Preset P1 gives the oscillator a frequency range of about 6 Hz to 27 Hz. The Q13 output of the 4060 goes high after 2^{13} (8,192) oscillator clock pulses, that is, after 5 to 20 minutes depending on the setting of P1.

The ripple counter in the 4060 operates only if the reset input of the IC is held logic low, which is the case when bistable IC2a is set. This happens when push-button S2 is pressed. When the Q13 output of the counter goes high, the logic level at the data (D) input of the bistable is clocked ('latched'). Since the D input is permanently connected to ground, a logic low is clocked, which has the same effect as resetting the bistable (note that resetting is also possible by pressing push-button S2).

The resetting of the bistable halts the counter. This happens either when the preset time has lapsed, or when the user presses S2 while the timer is still counting down. If the Q output of the bistable is high (i.e., when the counter is active), transistors T1 and T2 are switched on via R5 and R7 respectively. T1 in turn switches on a relay whose contacts are connected in parallel with the room thermostat contacts. The closed contact causes the CH boiler (and pump) to be switched on. At the same time, T2 turns on a LED that indicates the activity of the CH timer.

The timer has an internal 5-V supply based on a 100-mA 5-V regulator Type 78L05. The direct input voltage of between 8 V and 12 V may be supplied by a mains adaptor.

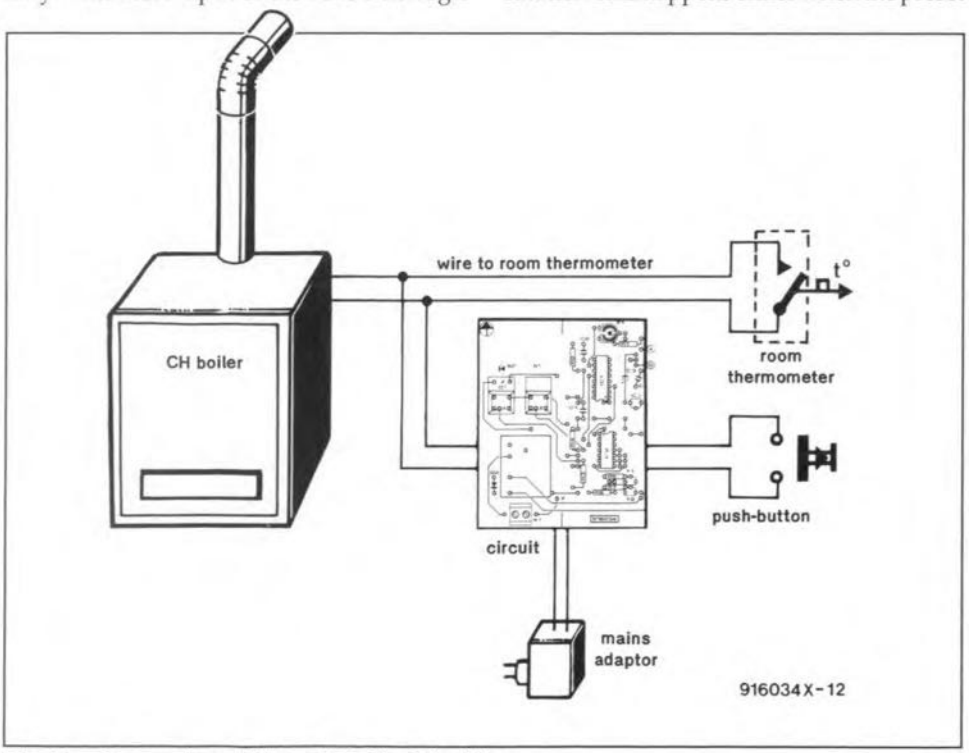
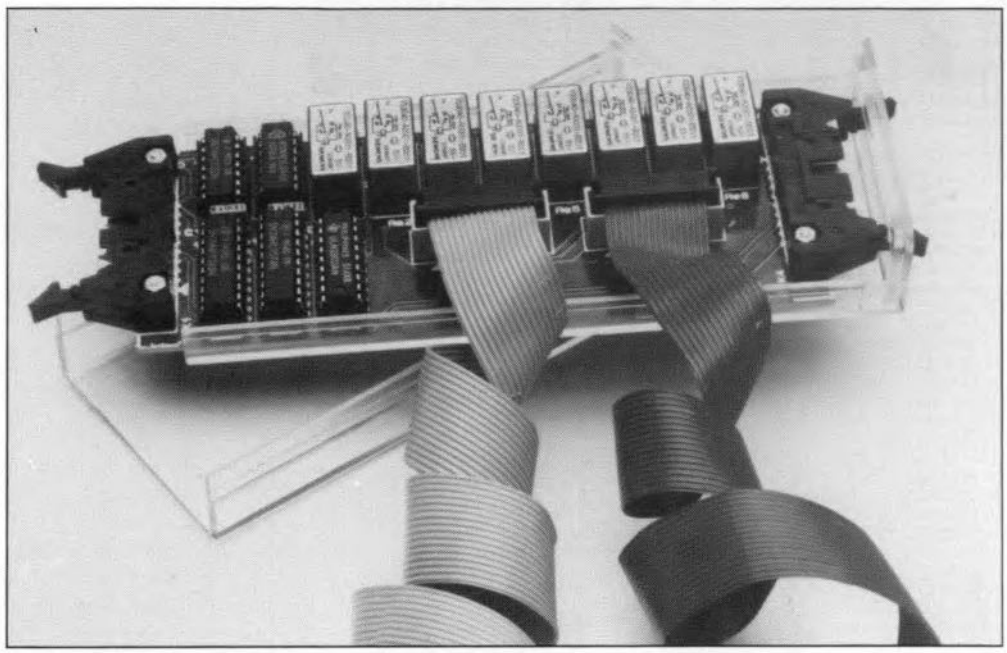


Fig. 3. Connection of the unit to the CH wiring.

Construction and connection

The CH timer is built on a universal prototyping board size-2 (UPBS-2), which may be obtained through our Readers Services. A suggested component mounting plan is shown in Fig. 2. The two ICs are best fitted in sockets. Do not forget any of the wire links, and observe the polarity of the diodes and the electrolytic capacitors. Make sure connector K1 is soldered securely to the board to prevent it coming loose when the connecting wires cause strain. If you want a front panel control instead of the preset on the board, simply replace P1 by a 47-kΩ linear potentiometer. A simple timing scale may be provided around the pot by measuring the on-time of the relay at a few settings. Finally, the timer is connected to the CH system wiring as shown in Fig. 3 ■

RELAY CARD FOR UNIVERSAL I/O INTERFACE



This relay card connects to the universal I/0 interface for IBM PCs described in the May 1991 issue. Simple to build and program, it offers a safe and easy way of controlling all sorts of equipment by means of a PC.

by A. Rigby

ALTHOUGH the relay card described here is designed specifically as an extension for the PC I/O interface (Ref. 1), its input control signals are readily found, or made, in non-IBM (PC) computers.

The circuit diagram of the relay card, Fig. 1, shows that it is linked to the I/O card via connector K1. It is also seen that the I/O card signals are buffered and fed to connector K4, which allows up to four extension circuits to be connected in series. Only two signals 'change' between K1 and K4: address lines A0 and A1 are interchanged on K4 (with respect to K1), and A0 is inverted. This allows all extension cards connected to the PC I/O interface to make use of a single, simple, address decoder. All cards connected in this way respond internally to address 00 (binary), but the successive interchanging of A0 and A1 causes their actual address to be determined by the order in which they are connected. Table 1 shows the address assignments.

Table 1. Address overview

Address	Relay card
base address + 0	1
base address + 1	2
base address + 2	3
base address + 3	4

More relays than ICs

The data flow between the PC I/O card and the relay extension is controlled by a bidirectional buffer, IC2. Although a unidirectional buffer would have been in order for the relay card (which functions as a write-only extension), bidirectional buffering is applied because two-way data flow may be required by other cards in the system.

The actual relay interface starts at register IC4, which is used to latch data when the relay card is addressed. The addressing is accomplished via the $\overline{\text{ENABLE}}$ and $\overline{\text{WR}}$ lines. When both are low, the output of IC1b is low also. To ensure that the data are stable at the input of the register, they are latched when the output of IC1b reverts to logic high. The logic pattern stored in IC4 is fed to driver IC5, which controls the relay coils. The relays are actuated by a logic high data bit written to IC4, so data inverting is not required.

The relay contacts are brought out to pins on connectors K2 and K3. Connector K2 carries the mother contacts and the normally open (NO) contacts of the relays, and K3 the mother contacts and the normally closed (NC) contacts.

Table 2. Relay specifications

Siemens V23040-A0001-B201
Contact specifications

Max. switching voltage:	150 V d.c. 125 V a.c.
Max. switching current:	2 A
Max. continuous current:	2 A
Max. switching power:	35 W d.c. 60 W a.c.
Max. switching frequency:	100 Hz
Mechanical lifetime:	10^8 s.o.
Mechanical lifetime with contacts loaded:	10^3 - 10^8 s.o.

s.o. = switching operations

Building and testing

The relay extension is built on a double-sided, through-plated printed circuit board, of which the track layouts and the component overlay are given in Fig. 2. The construction is mostly straightforward soldering work. The completed card is connected to the PC I/O interface via a 20-way flatcable with IDC connectors at both ends.

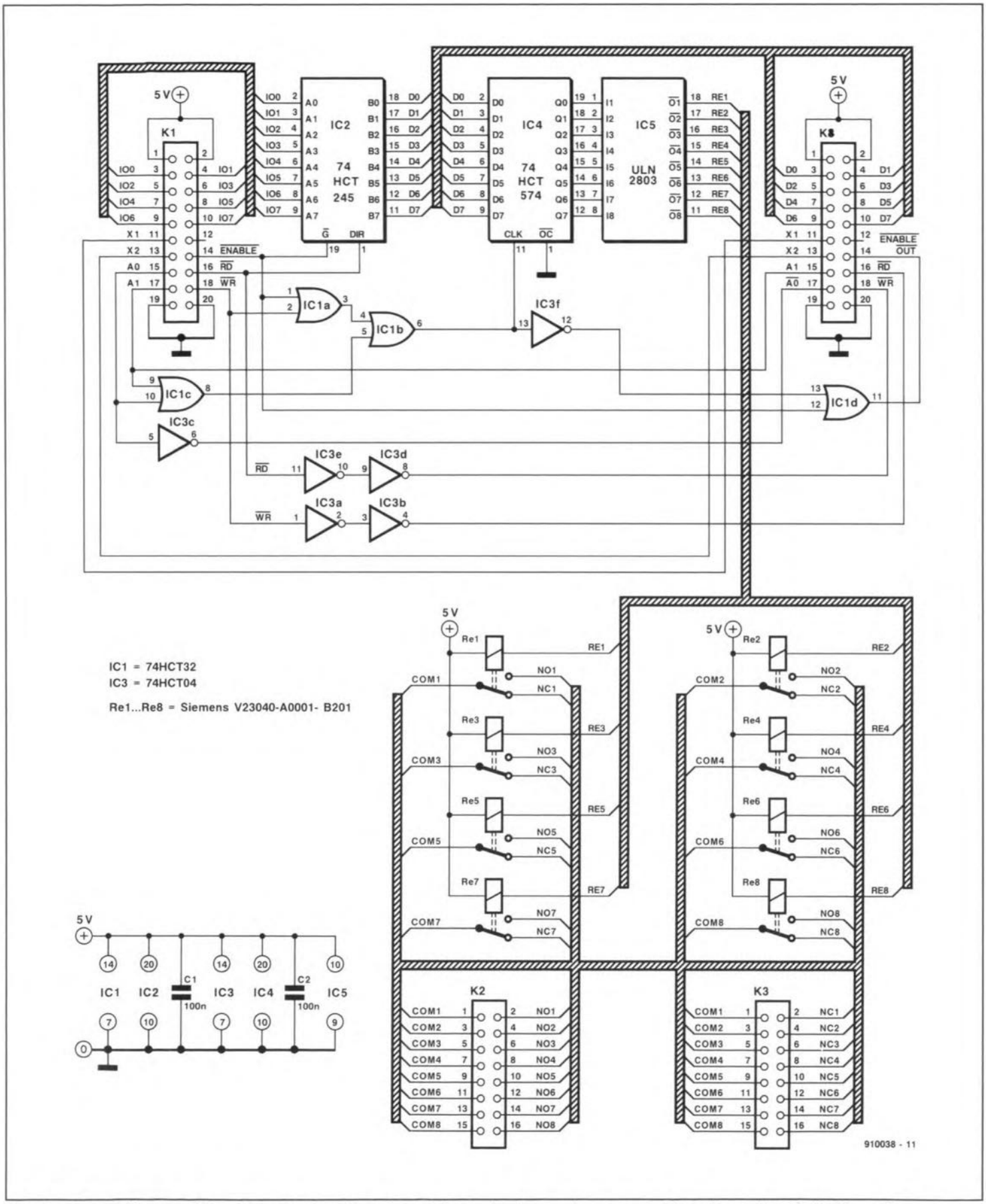


Fig. 1. Circuit diagram of the relay extension. Up to four of these circuits may be connected in series and controlled by a PC.

The current consumption of the relay card is determined by the number of actuated relays. When all relays are actuated, the current consumption is a little below 150 mA.

The switching functions of the relay card may be tested with the aid of the program listed in Fig. 3. When run, this program causes the relays to be actuated and deactuated in succession. The program may be used to test up to four relay cards connected in series.

Because of the track layout of the printed circuit board, the maximum voltage that may be switched by the relays is 42 V a.c. or 60 V d.c. This means that the relay card may **not** be used to switch mains loads directly.■

Reference:

1. Universal I/O card for IBM PCs. *Elektor Electronics* May 1991.

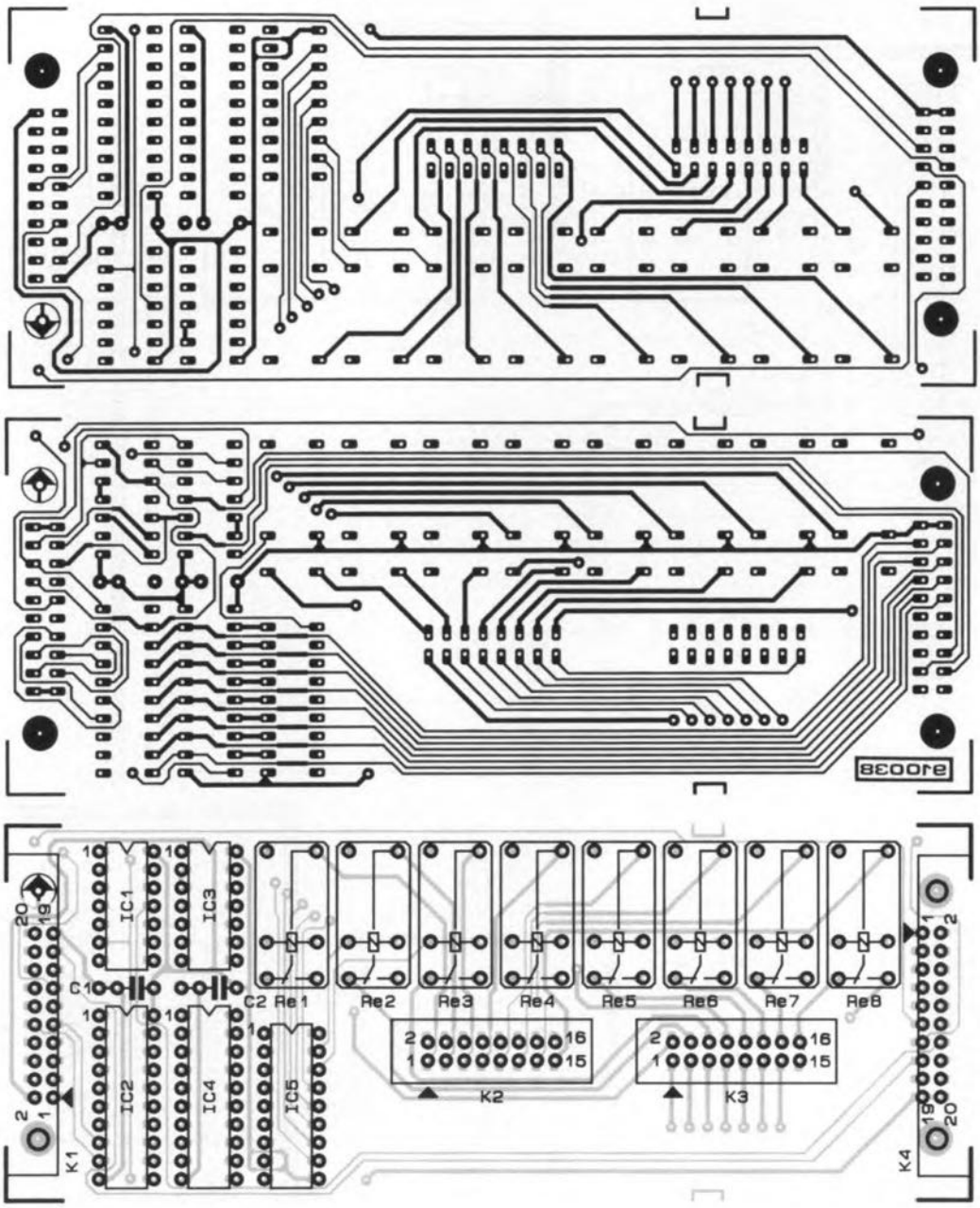


Fig. 2. Printed-circuit board for the relay card. Note that this board is double-sided and through-plated.

```
10 CLS
20 ' ..................................................... ibmio interface test
30 X=0 ' ..................................................... address definition
40 ' ..... X=0: &H300-&H303 X=1: &H304-307 X=2: &H308-&H30B X=3: &H30C-30F
50 ' ..... X=4: &H310-&H313 X=5: &H314-317 X=6: &H318-&H31B X=7: &H31C-31F
60 X=&H300+X*&H4
70 ' ..................................................................addresses
80 A1=X+0: A2=X+1: A3=X+3: A4=X+2: ' ..................... I/O addresses
90 ' ..................................A1 - A4 = relay card 1  to  relay card 4
100 ' ..................................................... test of I/O ports
110 CLS
120 PRINT "Testing I/O"
130 FOR I=0 TO 7
140 OUT A1,2^I ' ..................... close relay number i of card 1
150 OUT A2,2^I ' ..................... close relay number i of card 2
160 OUT A3,2^I ' ..................... close relay number i of card 3
170 OUT A4,2^I ' ..................... close relay number i of card 4
180 GOSUB 280  ' ..................................................... wait
190 NEXT I
200 FOR I=0 TO 7
210 OUT A1,255-2^I ' ................. open relay number i of card 1
220 OUT A2,255-2^I ' ................. open relay number i of card 1
230 OUT A3,255-2^I ' ................. open relay number i of card 1
240 OUT A4,255-2^I ' ................. open relay number i of card 1
250 GOSUB 280      ' ..................................................... wait
260 NEXT I
270 GOTO 130 ' ....................................... return for next cycle
280 ' ..................................... subroutine to execute a wait period
290 FOR J=0 TO 1000:NEXT
300 RETURN
```

Fig. 3. Run this little BASIC program to test one to four relay cards.

COMPONENTS LIST

Capacitors:

2	100nF	C1;C2

Semiconductors:

1	74HCT32	IC1
1	74HCT245	IC2
1	74HCT04	IC3
1	74HCT574	IC4
1	ULN2803	IC5

Miscellaneous:

2	20-way pin header with side latches	K1;K4
2	16-way pin header	K2;K3
8	PCB mount relay V23040-A0001-B201 (Siemens)	Re1-Re8
1	enclosure (e.g., Heddic 222)	
1	Printed circuit board	910038

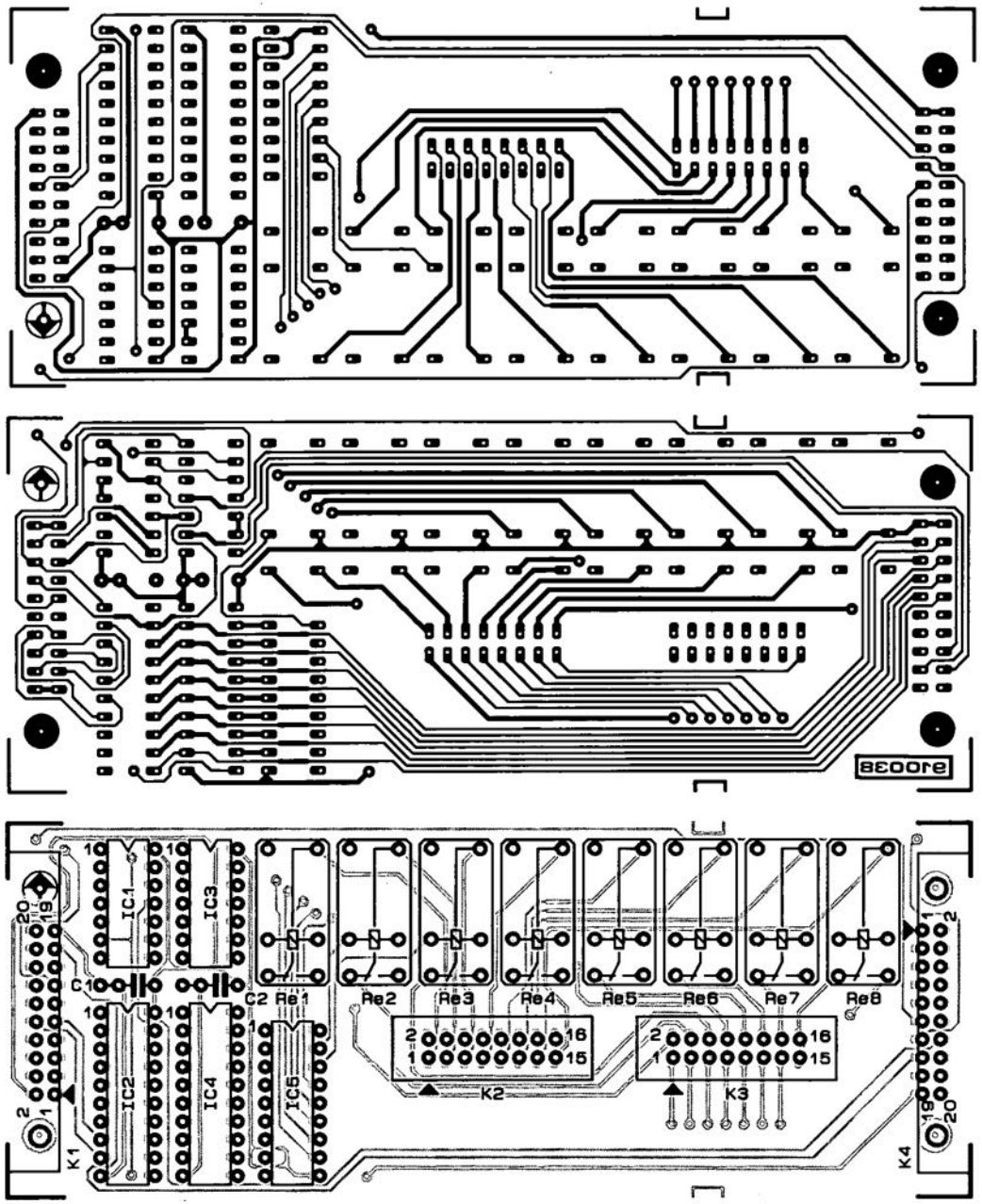


Fig. 2. Printed-circuit board for the relay card. Note that this board is double-sided and through-plated.

EXPERIMENTAL QUADRIFORM FERRITE TRANSMIT/RECEIVE ANTENNA

by Richard Q. Marris, G2BZQ

The quadriform is an experimental 3.5 MHz transmit/receive antenna of mini dimensions, consisting of four high-grade robust ferrite rods in a 9 in × 9 in (230×230 mm) loop configuration. Chambers 20th Century Dictionary defines quadriform as "fourfold; having four forms or aspects".

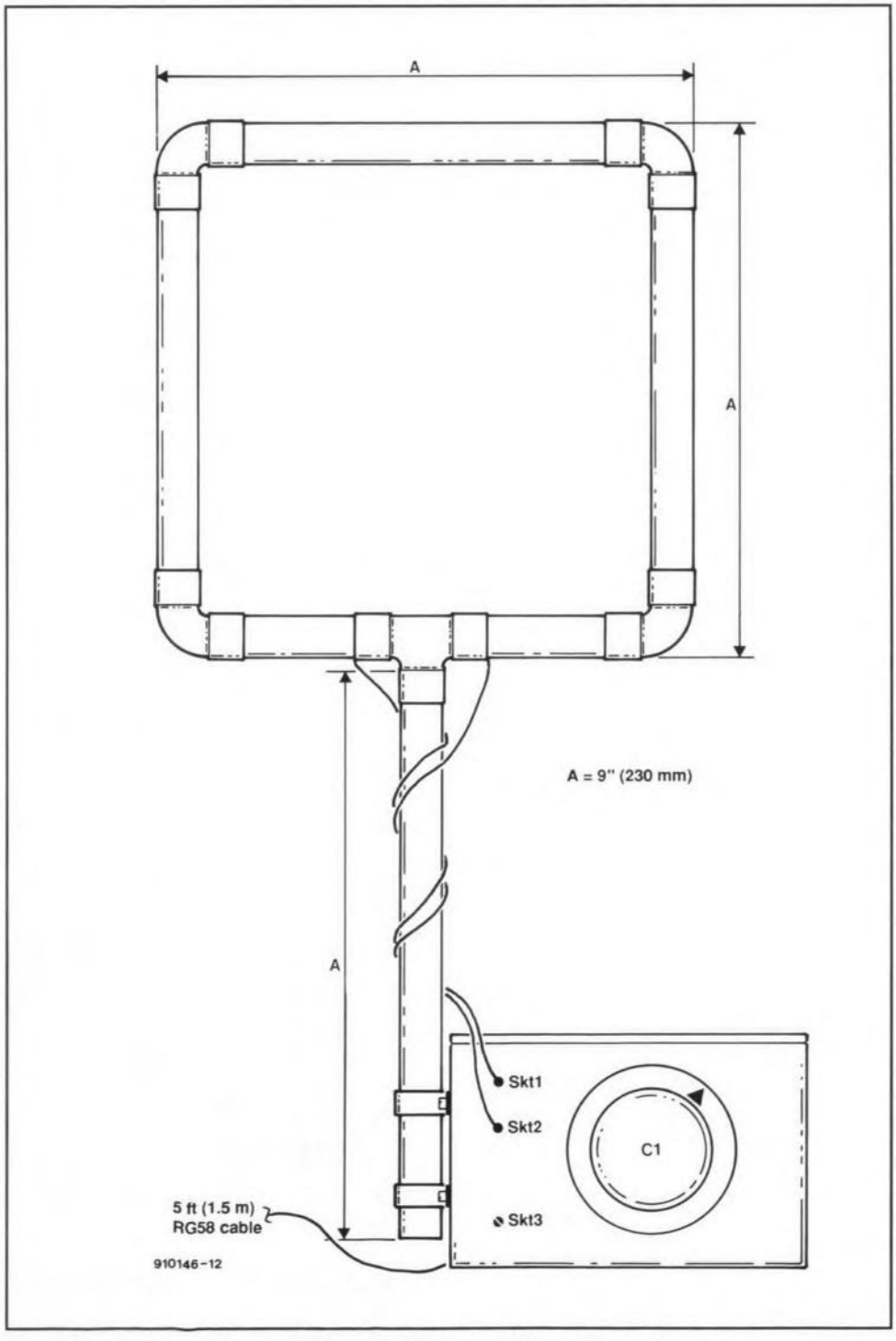


Fig. 1. Assembly of the quadriform ferrite transmit/receive antenna.

WHEN, a decade or so after the end of World War II, the transistor and ferrite rod antenna made their entry on the market, they quite revolutionized the domestic LW/MW radio scene with the arrival of small portable receivers with built-in aerials. One might have expected that ferrite antennas would also be used extensively for transmission, but this was not to be for various reasons. Obviously, however, experiments were taking place, especially in the American defence industry, but little or nothing has been published on the subject.

Nowadays, ferrite rod materials can be divided broadly into manganese-zinc mixtures and nickel-zinc mixtures. The former are used invariably for VLF and LF receiving applications between 1 kHz and 1 MHz, and there are several different mixtures. Nickel-zinc rods, again in several mixtures, have appeared with permeabilities between 40 and 850. In the latter types, apart from their use in domestic LW/MW radios, it has become possible over the years to obtain rods that can be used as HF band receiving antennas. An excellent booklet [1] is available from Amidon Associates (USA), which gives the full characteristics and sizes of many types of manganese-zinc and nickel-zinc rod. It may well enlighten the reader as regards ferrite rods for reception, but the contents are not geared to use of the rods for transmission.

Of particular interest are the Amidon Type 61 nickel-zinc rods, which are quoted as being suitable for use in receiving antennas for frequencies of 0.2–15 MHz. However, I have used these rods experimentally for reception in the VHF bands with acceptable results. I have also made several experimental single rod transmitting antennas from Type 61 ferrite material which gave widely varying results. A brief report on a small part of earlier experiments was published in Ref. 2. For convenience, all ferrite transmitting antennas used in my 'on the air' experiments have been designed for the 3.5 MHz (80 metres) amateur band.

Some of the problems that revealed themselves as the experiments progressed during the design of ferrite rod transmit antennas are listed here.

1. The difficulty of locating small supplies of suffciently large and robust rods suitable for high frequencies and, most importantly, for transmission.
2. How to couple the transmitter to the ferrite antenna: to feed RF power into the antenna? And then how to persuade the antenna to radiate that power over satisfactory distances to other stations?
3. Solving the serious problem of saturation of the core. As power into such an antenna is increased, a point is reached quickly where core saturation occurs. This saturation manifests itself by the heating up of the core, which appears to produce the following effects:
   (a) de-resonating the antenna from the selected frequency;
   (b) harmonics that cause intereference and TVI;
   (c) general instability, similar to (b).

It must be stressed that these findings are based entirely on the results of my own experiments.

Assuming that these problems can be solved, a tremendous advantage appears in that we have a tiny antenna—only a few inches long—compared with a traditional wire antenna: on 3.5 MHz, a wire dipole is about 140 ft (almost 43 metres) long!

It has been discovered that the main difficulty is that of core saturation, even when a suitable rod for h.f. transmission has been found. Experiments have shown, however, that this problem can be overcome to a large extent by leaving a large gap between the ferrite rod and the wire turns and distributing the turns over the entire length of the rod. From these findings, it was decided to try to produce a realistic unidirectional ferrite transmitting antenna with reasonable gain. The result is the Quadriform Ferrite Antenna.

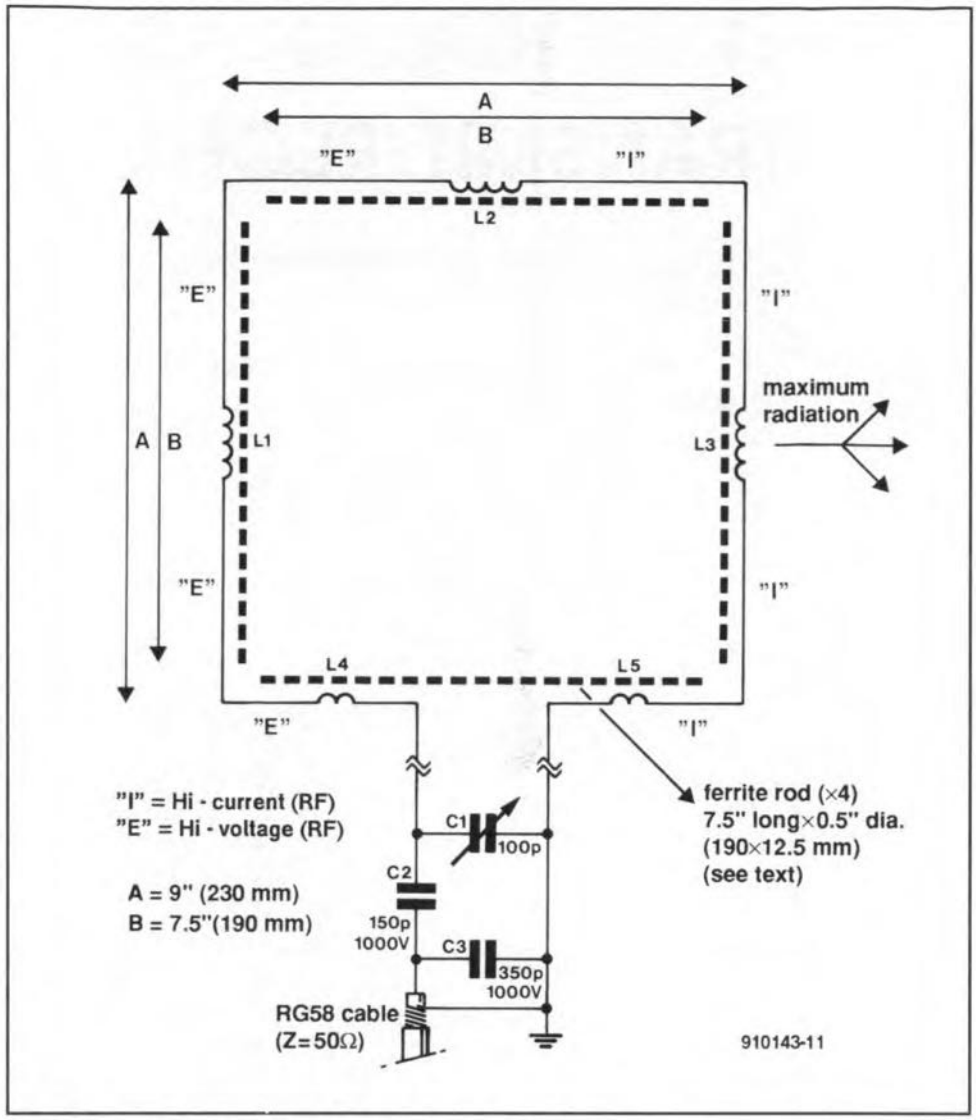


Fig. 2. Circuit diagram of the quadriform antenna.

Description

From Fig. 2, it is seen that the antenna consists of a 9×9 in. (230×230 mm) loop with small inductances, L_1–L_5, in each side. The wire sides are formed around a 7.5×0.5 in. dia. (190×12.5 mm) high-grade nickel-zinc (Type 61 material) rod enclosed in a plastic tube as shown in Fig. 3. It is fed at the bottom, between L_4 and L_5, with leads to plugs Pl_1 and Pl_2 that mate with appropriate sockets, Skt_1 and Skt_2.

The loop is resonated by a 100 pF ceramic, insulated, variable capacitor, C_1. The feed to and from the transmitter/receiver is a Type RG58 coaxial line via C_2 (a 150 pF ceramic, high-voltage disc type). Capacitors C_2 and C_3 form the actual coupling and impedance matching element to match the loop to a 50 Ω impedance. Socket Skt_3 is an optional earthing connection. The antenna is unidirectional.

The general layout is shown in Fig. 1. The loop is supported vertically by a 9 in (230 mm) long piece of plastic tube fastened with wall clips to the front vertical edge of the side of a 6×4×4 in (150×100×100 mm)aluminium box that houses the variable capacitor and some other components. The box is large and heavy enough to act as a base that stops the loop tilting. Sockets Skt_1–Skt_3, together with C_1, are mounted on the front panel; the RG58 cable exits through a grommet at the rear. The box is a two-piece interlocking double 'U'; the loop is clipped to the removable lid.

Care is needed in winding the inductors. First, cut three 7.5 in (190 mm) lengths of the $^{11}/_{16}$ in (17.5 mm) dia. tubing and two pieces of about 2.5 in (63 mm). The two shorter lengths, when fastened together with a standard T junction, form the bottom side that should also be 7.5 in long. The 9×9 in square is completed with four standard 90° plastic elbows. All plastic tubing and junctions are readily obtainable from most DIY stores (in the UK under the name POLY-YORC). A 7.5 in (190 mm) long, 0.5 in (12.5 mm) dia., ferrite rod is inserted into each side before the corner elbows and T junction are fitted. It is necessary to wind a couple of turns of masking tape round the ends of each rod to ensure rigidity in the tube—see Fig. 3. The loop windings are made from PVC covered, single-strand, 1/0.6 mm wire, 1.2 mm o.d., rated at 1 kV, 1.8 A. They are wound as shown in Fig. 3. The wire linking inductors L_1 and L_5 is taped close along the outside of each of the tubes; over the 90° elbows it is held in place by a small 'V' filed in the outside radius of each elbow. Black tubing, black PVC wire and black PVC tapes were used throughout.

The whole wire length, including the small coils, forms part of the ferrite-cored loop. Inductors L_1–L_5 are close wound, clockwise throughout.

Variable capacitor C_1 is mounted at dead centre of the front panel of the base box and it and the other few components are hard wired. A 9 in (230 mm) length of tube is inserted into the T junction of the finished loop; the bottom end of this is clipped to the front edge of the side of the lid of the box with two standard plastic wall clips—see Fig. 2.

CAUTION! It is essential that the specified ferrite rods are used—see parts list. They should be treated with great care. If they are dropped on to a hard surface, they may break, chip or suffer from core destabilization. They are expensive! At the time of writing, they cost $15.00 (about £8.50) each plus $8.00 for airmail shipping direct from Amidon. Delivery is by return mail and is usually within three weeks from airmailing the order to Amidon. Master Card and Visa are accepted.

Testing, operation and results

Initial testing of the antenna is carried out with a receiver tuned to 3600 kHz. Capacitor C_1 is

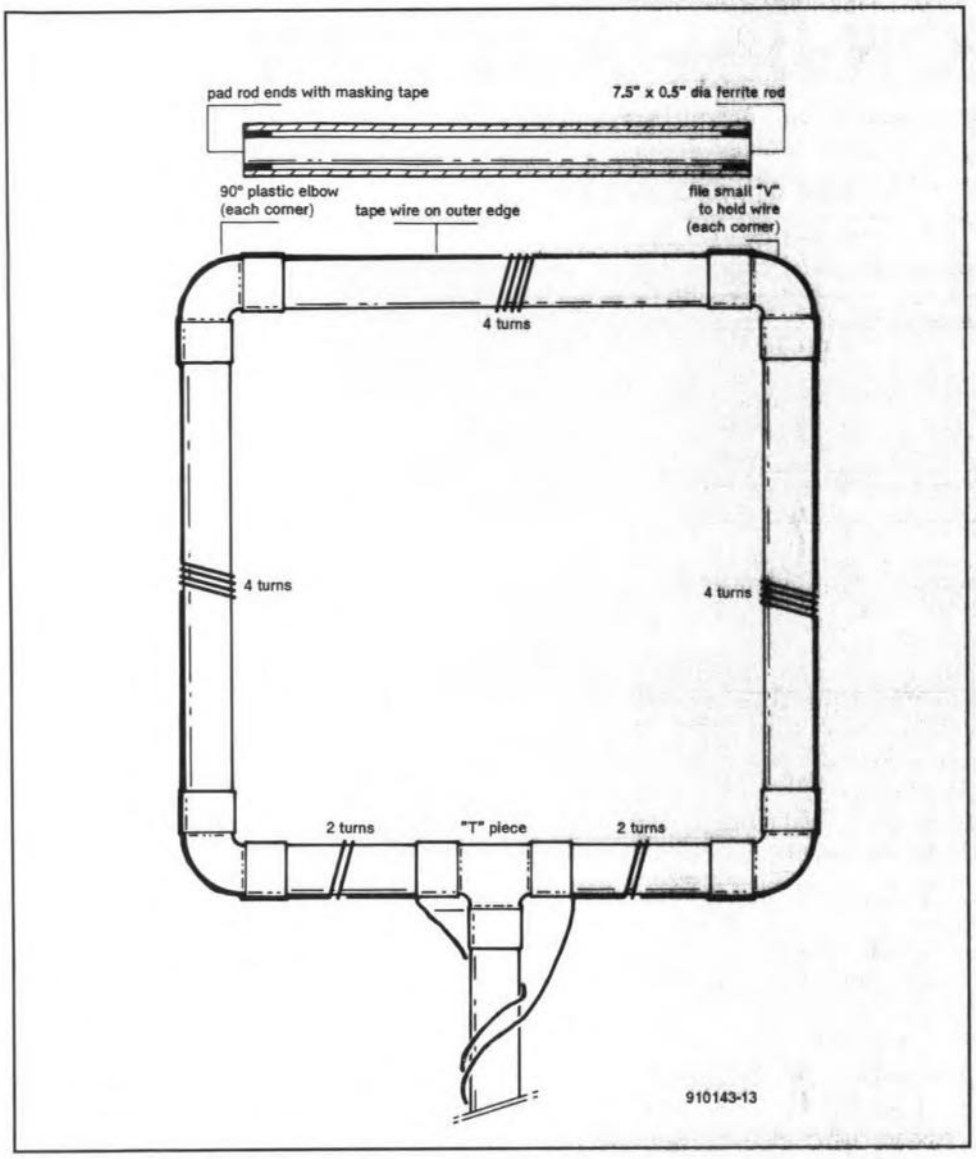


Fig. 3. Assembly details.

rotated for resonance, which is indicated by an increase in signal strength. The plates of the capacitor should then be enmeshed about 50%. The 3500–3800 (or 4000) kHz band is accommodated without any problem.

The polar diagram of a single horizontal ferrite rod antenna is a figure 8 off the two long sides. The polar diagram of the Quadriform is rather more complex and not easy to establish indoors, possibly owing to reflections off walls, and so on. However, it is, to all intents and purposes, unidirectional with one very large lobe off one end, which reduces interference appreciably. This lobe can be moved through 180° by reversing Pl_1 and Pl_2 in sockets Skt_1 and Skt_2, which is a simple way of achieving all-round operation. If necessary, further small adjustments can be made by a small rotation of the antenna. This radiation pattern holds good on transmit and receive.

Before the antenna can be tested for transmission, it is necessary to first set up the transmitter into a 50 Ω dummy load at the desired frequency. The antenna is then resonated with the receiver, at the same frequency, and subsequently substituted for the dummy load. It should be fully loaded by the transmitter on low power, after possible minor adjustments of C_1. The usual bandwidth on transmit, without readjusting C_1, is about 25 kHz.

The antenna is essentially a low-power device. In my experiments, it has been driven by over 20 watts RF without detectable core saturation. However, it is intended for use indoors near the transmitter/receiver, where a transmitter power of <10 watts has been used 'on the air' with very satisfactory results. There was no detectable harmonic or TVI radiated. The use of an RF earth connection made no apparent difference.

WARNING!
IN THE INTERESTS OF DOMESTIC SAFETY, THE TRANSMITTER OUTPUT SHOULD NOT EXCEED 10 WATTS.

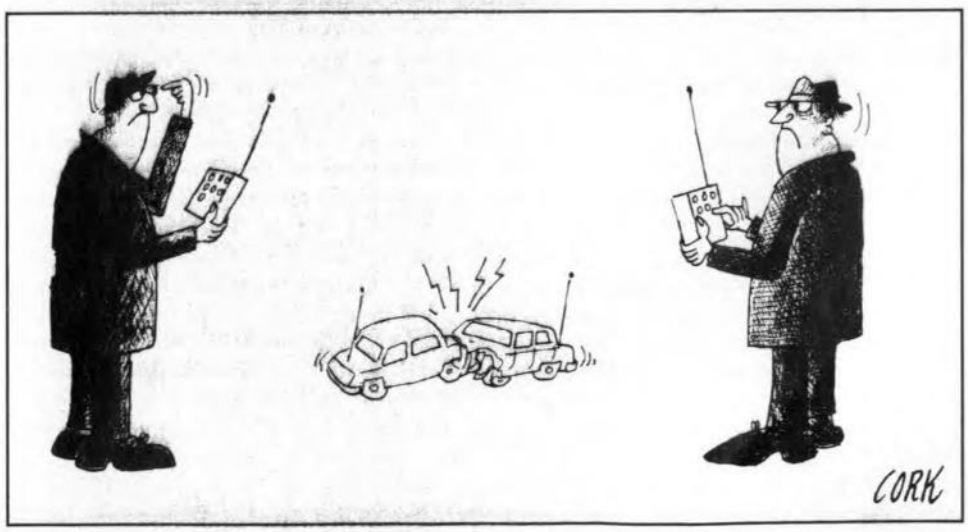
References

Iron-powder and Ferrite Coil Forms, published by Amidon Associates, P.O. Box 956, Torrance, California 90508, USA.

"Fe-ONE Experimental Transmitting Antenna" by Richard Q. Marris, *Practical Wireless*, January 1989.

PARTS LIST

4	nickel-zinc rods, 7.5 in long by 0.5 in. dia. (190×12.5 mm), available from Amidon Associates Inc. P.O. Box 956, Torrance, Ca. 90508, USA; Tel. +1 213 763 5770; Fax +1 213 763 2250.
1	aluminium box 6×4×4 in. (153×102×102 mm) order code Box/J10 from Marco Trading.
1	variable capacitor, 100 pF, Jackson Bros Type 11 or equivalent style and quality plus knob to suit.
1	ceramic disc capacitor, 150 pF, ≥1 kV.
1	ceramic disc capacitor, 350 pF, ≥1 kV.
2	4 mm banana plugs
3	4 mm banana sockets
1 m	Poly-Yorc (or similar) black tubing, o.d. 0.7 in (18 mm), i.d. 0.6 in (13 mm); available from many DIY stores.
4	90° elbows to match the black tubing.
1	T junction to match the black tubing.
2	wall clips for fitting the black tubing.
5 ft	RG58 coaxial feed line; Z=50 Ω, plus coaxial plug to suit transmitter/receiver. PVC covered, single strand 1/0.6 mm wire (black), 1.2 mm o.d., rated at 1 kV and 1.8 A. Order code CBL/EW1/black from Marco Trading. Black PVC tape and masking tape as required.



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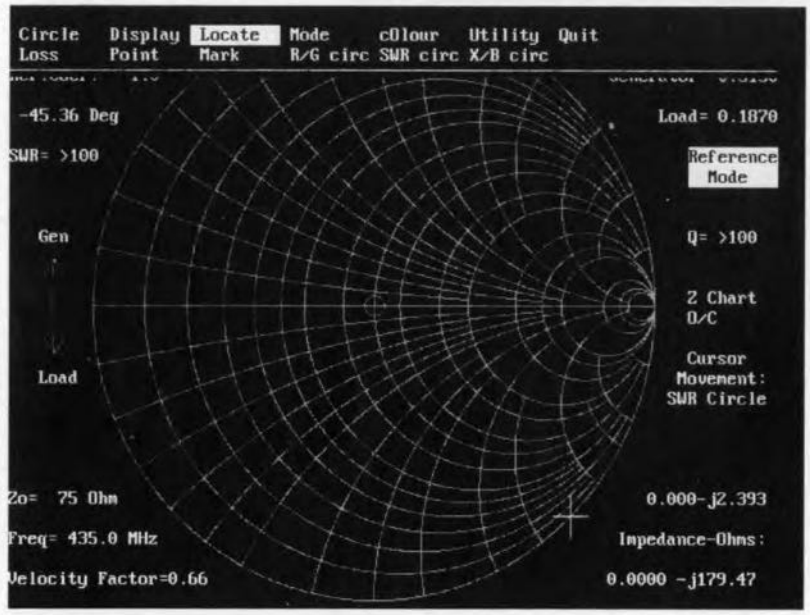
Z-MATCH II — A REVIEW

by Mike Wooding G6IQM

Z-MATCH II is a Smith chart RF design software package. Quoting from the supplier, Number One Systems: '*In spite of the availability of modern design aids, such as the hand-held programmable calculator, sophisticated circuit simulation and Computer Aided Design (CAD) software, the Smith chart is still widely used as a radio frequency circuit design tool. The Z-MATCH II program enables the Smith chart design process to be performed easily and accurately on a personal computer.*'



For those of you who have never seen a Smith chart, the following is going to seem like white man's magic! However, I shall attempt a short explanation of what a Smith chart is, and how one is used. This is not going to be the easiest thing for me to do, as it is a very long time since I learnt how to use them. Therefore, with the kind permission of Number One Systems Limited, I am going to reproduce, in part, the introductory explanations of Smith charts and their uses from the Z-MATCH II instruction manual.

Smith chart circles

The Smith chart is made up of two sets of circles; one set represents the resistive part, R, of a complex impedance, the other set represents the reactive part, X.

Normalised resistance and reactance

In order to avoid the need for a different chart for each characteristic impedance, Z_0, the paper Smith chart uses normalised values of resistance and reactance circles. The normalised impedance, Z_n, is given by:

$$Z_n = Z/Z_0 = (R/Z_0) + j(X/Z_0)$$

Where Z, R and X are the actual values of impedance, resistance and reactance respectively.

Series impedance values

The impedance of any point on a transmission line can be represented by a point on a Smith chart.

The series impedance value of a point on the chart is found by reading the values of the intersecting resistance and reactance circles. The Z-MATCH II program displays the series impedance value corresponding to the cursor position on the chart.

Parallel admittance values

An admittance value (Y-) Smith chart can also be drawn. The circles on this chart represent values of constant conductance ($1/R$) and constant susceptance ($1/X$). By using a Y-chart overlay on an impedance chart, it is possible to convert from series impedance to equivalent parallel admittance.

Standing wave ratio (SWR)

A circle that is concentric with the centre of a Smith chart has a fixed value SWR. The SWR of such a circle is equal to the value of R/Z_0 at the point where the circle crosses the horizontal axis on the right-hand side of the chart.

Intersections of the SWR circle with the horizontal axis on the left of the circle represent points of voltage minimum, intersections on the right represent voltage maxima. Moving round a constant SWR circle is equivalent to travelling along a lossless transmission line; successive values of impedance indicated on the chart correspond to the impedances seen along a lossless line with the same SWR.

Wavelengths towards generator and load

The distance moved on a transmission line is directly proportional to the angle of rotation around a constant SWR circle; one revolution is equal to a half wavelength movement.

Moving around an SWR circle in a clockwise direction is equivalent to travelling towards the generator, whereas moving anti-clockwise is the same as travelling towards the load. The wavelengths towards the generator and load (backwards and forwards respectively) are shown on the periphery of the standard paper Smith chart. These peripheral scales on the paper chart are used by drawing a straight line from the centre of the chart through the point of interest. The Z-MATCH II chart indicates directly the wavelength (or length in metres) corresponding to the cursor position.

By convention, the starting point for the wavelength scales is the left-hand minimum position; this is because in practice it is easier to accurately locate a voltage minimum than a voltage maximum on a line. The angle of the reflection coefficient is zero at the opposite, voltage maximum, point. Since the Smith chart repeats itself every half wavelength around a constant SWR circle, lines longer than half a wavelength are dealt with by subtracting multiples of a half wavelength from the actual line length.

Lumped L and C circuits

The Smith chart can also be used for the design and analysis of discrete L and C circuits. When a single component L, C or R is added to a network then either the resistance (R), reactance (X), conductance (G) or susceptance (B) parameter of that network will not change. The point representing the network impedance, or admittance, on the Smith chart will therefore move on a particular chart circle when a single component is added.

By switching between the Y and Z charts and moving the cursor on constant reactance or constant susceptance circles, it is possible to move from any one point on a chart to any other. Moving on a Y chart susceptance circle is equivalent to adding parallel inductance or capacitance to a network; moving on a Z chart reactance circle is equivalent to adding series inductance or capacitance. Using the Z and Y charts in this way, it is possible to build up networks to impedance match from any source impedance to any given impedance load.

The reference mode facility provided by the Z-MATCH II (see below) program is particularly useful in this type of process; the reference mode enables the value of inductance or capacitance required to move between any two points on a circle to be read directly.

With the conventional paper Smith chart the rules for the correct direction of movement on the constant parameter circle need to be known. Z-MATCH II simplifies the procedures involved considerably, by displaying directly the equivalent value of R, L and C at the operating frequency chosen. The change in L, C or R can therefore be seen as the cursor moves round any of the constant parameter circles.

Z-MATCH II

Z-MATCH II is a CAD package for designing and calculating Smith charts. The basic requirements to run the package are an IBM PC/XT/AT/386 or PS2 computer, or compatible clone, running under MS-DOS 2.0 or later; a col-

our graphics adaptor (CGA, EGA or VGA) and a colour monitor, and a minimum of 256k of free RAM. For hard copy of the output an IBM Graphics printer, or compatible, and adaptor card are required. Z-MATCH II does not require a maths co-processor to be installed, but it will increase the speed of operations substantially. A mouse may be used with the software, but, as will be seen later, owing to the necessity of precision locating of the cursor, this method is not wholly satisfactory.

User manual

The presentation of the package is very good. The user manual comes in an A4 ring binder, allowing for updates to be added easily. The software is supplied on one 5.25-inch 360k disk or one 3.5-inch 720k disc, both being supplied with the package.

The user manual begins with the usual software and copyright licence conditions and agreement, followed by the introduction, installation, running and basic operating instructions. The manual then continues with a brief description of what a Smith chart is and what it can be used for. This is, as is explained in the manual, by no means meant to be able to teach you the whats, whys and wherefores of Smith chart use, but is a general guide for those already conversant with the subject. For those less used to working with Smith charts, a tutorial section of worked examples is included later in the manual.

Following the initial section of the user manual is a comprehensive detailing of all the features of the package and explanations of all the features, menus and command key functions.

Cursor control

There are four methods of manipulating the cursor around the chart:

- in straight lines using the numeric keypad keys (2, 4, 6 & 8). The speed of movement can be changed by holding down the 'SHIFT' key simultaneously;
- if your keyboard is an enhanced version with separate cursor control keys, then these can also be used. In this case the shift key will not change the speed of movement with these keys, but the speed will always be opposite to that with the numeric cursor control keys;
- the 1 and 3 keys on the numeric keypad ('End' and 'Pg Dn') move the cursor around selected circles (see below). On the enhanced keyboard the separate 'End' and 'Pg Dn' keys also do this, but at the slower speed;
- using the mouse, by pressing the left-hand button, moving the pointer to the desired position and then releasing the mouse button. However, as previously noted, using the mouse to position the cursor is less accurate than using the cursor keys which is the recommended method.

Features

Although, owing to the complexity of the software, I am unable to give a complete description of all the features available, I hope to briefly describe some of the major functions.

Circles

This function allows the user to draw various circles on the chart:

- a circle centred on the current cursor position;
- a constant conductance circle that passes through the current cursor position when in the impedance mode;
- a constant resistance circle that passes through the current cursor position when in the admittance mode;
- a constant Standing Wave Ratio (SWR) circle that passes through the current cursor position (this circle passes through all the impedance, or admittance, points that would be present on a half-wavelength of transmission line with the same SWR and Z_0 value);
- a unity conductance circle to be drawn on the chart when in the impedance mode.

Displays

This allows the method in which the parameters are displayed on the chart to be changed to suit the user's requirements in the following ways:

- a rectangular or polar coordinate display shown at the bottom of the screen. This process serves the same function as using a Carter chart overlay with a paper Smith chart;
- toggling between a wavelength scale from source and load to a distance in metres scale from source and load, depending on which constants or parameters are already known;
- redraw the entire chart, maintaining the values of frequency, Zo, etc., already entered, but clearing the display of any circles drawn, whilst maintaining the current cursor position;
- the ability to enter the various known parameters, i.e., characteristic impedance (Zo), frequency and dielectric constant or velocity factor.

Locate

This set of functions allows the user to easily manipulate the graphics cursor around the chart:

- the ability to compensate for transmission line loss, by simply entering the loss in dB, which updates the cursor to a new position, taking the loss into account and giving the corresponding SWR, impedance, etc.;
- the ability to move the cursor to a specific point on the chart relative to the prompted input of values for series impedance, parallel admittance, polar impedance or scattering parameter;
- the facility to permanently mark a cursor position on the chart for future reference;
- selection of cursor movement around constant resistance or conductance circles, SWR circles, or the constant reactance or susceptance circles.

Other facilities are available which allow the user to switch the program to reference mode, which enables further calculations to be made with reference to the current cursor position. Also, the display can be switched between series impedance and parallel admittance displays, using a single function key stroke. The background and drawing colours used in the display can also be user selected.

Main features of Z-MATCH II

Z-MATCH II displays a Smith chart which shows:

- Actual Impedance and Admittance
- Normalised Impedance and Admittance
- Polar Impedance
- Distance towards Generator and Load
- Reflection Coefficient
- Standing Wave Ratio
- Equivalent Inductance or Capacitance
- Z_0, Frequency and Dielectric Constant
- Network Q

Z-MATCH II provides these features:

- Conversion between Impedance and Admittance
- Circle drawing
- Determination of the effect of line loss
  Line Transformer calculations
- Location of any given Z, Y, S or Polar parameter
- Movement of the screen cursor on chart circles
- Amplifier design using S-parameters
- Display of ANALYSER II program output files

Note: ANALYSER II is an advanced AC Linear Analysis program that calculates and displays the steady-state AC frequency response of a circuit in terms of gain, phase, group delay and input/output impedances. It is also available from Number One Systems Limited at a cost of £195.00 exclusive of VAT and p&p. This package may also be reviewed at a later date.

Conclusions

I found the package easy to use and the results obtained were as accurate as those that could be obtained by manual charting, but much quicker and easier to obtain! The ability to quickly change parameters and observe the changes on the chart is an absolute boon to a designer.

I agree with the comment in the user manual that a mouse can be used but is not recommended. It is not really possible to place the cursor accurately enough using the mouse. However, moving around the chart with the mouse and then making final precise adjustments with the cursor keys worked fine.

Obviously aimed at the professional RF circuit designer, this package represents excellent value for money, especially when taking into account the time that could be saved using such a utility, instead of the 'Bob Crachett' method using quill and ink. Highly recommended.

I wish to thank Mr. Espin of Number One Systems Limited for his help and advice, and for the review software. ■

Z-MATCH II is priced at £195.00 + £4.75 p&p + VAT and is available from: **Number One Systems Limited, Harding Way, St.Ives, Huntingdon, Cambridgeshire PE17 4WR. Telephone: (0480) 61778. International: +44 480 61778. Fax: (0480) 494042.**

COMPUTER-AIDED ELECTRONICS DESIGN

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It is hard, if not impossible, to think of professional and industrial electronics design without a computer entering at some stage along the long way via concept, design rule checks, electrical checks, PCB design and product modelling, etc., to a working model that can be used for production. In this article we examine some of the software tools (for IBM PCs and compatibles) available commercially for schematics drawing, circuit simulation and PCB design.

ALTHOUGH the Bob Cratchit method (quill, ink, and the back of an envelope) of recording new electronic circuit designs is still widely applied, an increasing number of electronics designers avail themselves of a PC to produce circuit diagrams (schematics) electronically.

The operation of these so-called schematics editors is basically identical. In most cases, components selected from a library are placed on the screen in the desired configuration. On completion of the component placement phase, the individual parts are interconnected by lines, representing electrical connections. The circuit diagram so made may be stored on disk, or on the computer's memory, or it may be sent to a printer or plotter to obtain hard copy.

Once you are used to seeing only a section of your drawing on, say, a 14-inch monitor, drawing a circuit diagram electronically is hardly more difficult than using pen and paper for the same purpose. Virtually all schematic editor packages allow the user to zoom in on a certain section of the diagram, and also to view the complete diagram at a certain reduction factor. During the first attempts at using a schematics editor, the displayed section is nearly always too small to have a good overview, or the complete drawing is shown at a size reduced so far that it is difficult to place a component at the right place. These problems are usually caused by lack of practical experience, hardly ever by faults in the program. Obviously, a larger monitor solves all these difficulties at a stroke, but the cost of, say, a hi-res 19-inch colour display may be prohibitive to many.

Whether or not a schematics editor is a useful tool depends on the size of the components library, and the user interface. While the components library can usually be edited and expanded to your heart's desire, there is very little you can do to improve a less than efficient user interface. Fortunately, the choice of schematics editors is fairly large, so that finding one that meets your personal requirements at a certain outlay should not be too difficult.

Circuit simulation

A circuit diagram is but the start of a long way towards the production of a working model. The second phase is almost always the construction of a prototype on which electrical measurements are carried out to see if the circuit (on paper or on the screen) lives up to its expectation. In most cases, it will not, and some redesigning is in order. Building a prototype from scratch without the least idea whether or not it will work is a problem to many designers because it is time consuming, and requires a basic set of test equipment. Provided you have acquired the skills necessary to work with them, electronics simulation programs are a good way of preparing for prototype construction. These programs allow you to run a (purely theoretical) analysis of the electrical performance of the circuit taken from your schematics drawing package. For instance, an input signal of 100 mV may be simulated, and a frequency sweep of 20 Hz to 20 kHz. The software calculates the resulting voltage response, group delay, phase shift and, in some cases, the distortion, at the output of the circuit, or at a user-defined point (node) in the circuit. In digital circuits, 'analogue' parameters such as the distortion and the phase shift are usually irrelevant, and other parameters, such as signal set-up times, delays and system timing, are called for to see what happens if, for instance, a certain bit pattern is applied to the circuit. In many cases, digital circuit simulation options allow 8 or even 16 outputs to be monitored simultaneously.

Whether analogue or digital, all circuit simulation is based on component parameters available to the program. Like schematics editors, simulation programs use a components library for this purpose. Here, again, the usefulness of the simulation program depends entirely on the accuracy of the component data, and the number of components included. A component store-and-edit function is indispensable for any serious work, and quite some time may have to be spent on entering data on new components, the libraries supplied with most simulation packages being fairly rudimentary. Fortunately, most of the leading semiconductor manufacturers supply data on their components on diskette, in a format that can be recognized by simulation programs.

Circuit simulation is a pretty complex matter, as you will soon find out from the time your PC spends on analysing even basic circuits like a one-transistor amplifier. Unfortunately, it will be found that a standard PC-XT is hardly suitable for this application. Also, you will need quite some experience in numerical circuit analysis before you can use a simulation program in any successful way.

Prototype construction

Even the best simulation program will not tell you if a circuit works reliably. Prototype construction is, therefore, a must after the usual series of corrections and additions to the circuit. Prototype construction should take as little time as possible, whence the immediate need for a printed circuit board. Construction on veroboard or stripboard is not usually considered at this stage because of the high risk of errors, and the time required for assembly and debugging.

There are a number of ways to produce a PCB track layout, and dedicated software is available for this purpose. For instance, there are programs that enable a track layout to be drawn only, while other, more advanced, packages are capable of drawing their own layout on the basis of the circuit diagram. Called autorouters, the latter invariably insist on the user setting certain initial values and parameters related to the PCB layout. Even the most sophisticated autorouters still require components to be

picked up and placed on to the board manually with the aid of the mouse. That is where the problems begin for inexperienced users: even the best autorouter will not produce an acceptable track layout if the component placement is not given sufficient thought.

Schematics entry

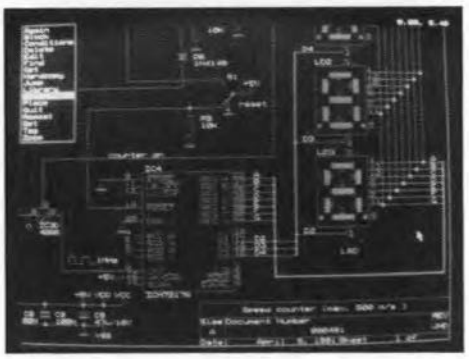
AutoSketch 3.0 plus electronics library is a good example of a schematics drawing package without interfaces to PCB layout software. The program is ideal as a low-cost entry level to schematics edition, and can be run from XT-class computers onwards with a minimum of 512 KByte RAM and a 10-MByte hard disk. A mathematics coprocessor is supported but not strictly required.

AutoSketch is a spin-off of the much more powerful AutoCAD program, and both have been developed by the Swiss company AutoDesk AG. Originally a low-cost CAD program for machine construction and architecture, its library extensions for electrical and electronics applications enable it to be used for drawing circuit schematics.

The program supports a mouse or a graphics tablet as pointing devices, and a plotter, matrix printer or laser printer as output devices. The program installation is straightforward with the aid of the instruction manual. The operation via menus is learned rapidly, which is an advantage if the program is used only occasionally. The finished drawing may be saved in the HPGL (Hewlett Packard Graphics Language) or DXF (Data eXchange Format) format. Although neither of these is of any use for further processing by PCB layout programs, they do allow drawings to be copied to DTP (desk-top publishing) or NC (numerical control) programs.

OrCAD SDT IV (Schematic Design Tools) is a schematics editor with added features such as annotation, back-annotation, netlist and parts list output, and design rule checking. The construction drawing facilities offered by the program are modest, but the electrical circuit drawing capabilities very powerful. Version 4 of the program has no fewer than 20,000 library items, as compared to 6,000 in version 3. Also new is the shell-like user interface, ESP, through which the user has access to the various subprograms and utilities. ESP is a welcome and state-of-the-art improvement to the DOS-based parameter entry implemented in previous versions.

Orcad supports EMS (extended/expanded memory system) of any size, doing away with the dreaded 640-kByte base memory limit in PCs. As to the hardware environment, OrCad can be used cheerfully only when an AT-class PC is used with a hard disk. The package comes with drivers for virtually all of today's graphics adapters. Supplied on four 3½-inch disks and complete with a hefty manual, OrCad is protected against illegal copying and use by a so-called dongle.



Producing circuit diagrams with OrCad is straightforward work. By virtue of the new shell, post-editing, for instance, to generate a parts list, is much simpler than before.

OrCad SDT has a link to OrCad PCB, a separate PCB layout program. SDT is also capable of supplying output to 20 odd standards, including Spice and Calay.

Schema III is a another schematics editor. This program comes on two 1.2-MByte 5¼-inch diskettes, along with two 360-Kbyte disks that contain the library and the utility programs. Schema III is the only schematic editor discussed here to provide a real-time pan (panorama) function, which means that the visible section of the drawing is moved over the screen automatically when the cursor reaches one of the borders. Other programs may offer a similar function, but invariably redraw a section of the screen. By contrast, Schema III ensures that the full section is always visible. As with OrCad, the subprograms that make up Schema III are accessible via a user interface called the Manager.

Schema III supports HP, Calcomp and Houston Instruments plotters, and saves drawings in the TIFF, DXF or Postscript format. It provides the basic schematic editing functions: component replacement, component loading, parts list and netlist generation, and design rule check. According to the manufacturer, it can be run on PC-XT, AT and 386-based computers with a minimum of 640 KByte RAM and 4-MByte of free space on the hard disk. A mathematics coprocessor is not supported.

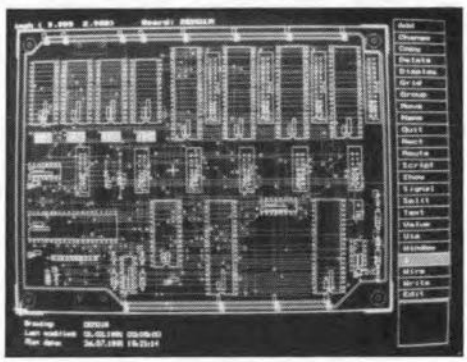
Schematic 3 is a schematic editor in a series of CAD products from the Australian software house Protel. The program is ideal for fast drawing of circuit diagrams and the generation of netlists and parts lists ('bills of material'). Remarkably, the package has an integrated word processor, which allows text to be placed freely in the circuit diagram.

The design rule check is performed as a separate utility, i.e., not during the entry phase (on line), which is more usual. Errors, if found, are written to a file. The package is quite extensive, and requires an AT-class computer (or faster) to run at acceptable speed. EMS is fully supported.

The libraries number a total of 15, and contain over 3,000 components. Among the output devices supported are HPGL and Roland plotters, Epson (compatible) matrix printers and HP (compatible) laser printers. Postscript output is not supported. The program, which is supplied on 5 diskettes, is not protected by a dongle or any other means.

Combination packages

Combination packages avoid problems that may occur in standards exchange and file conversions, by integrating the functions of a schematic editor and a PCB design program. Almost all combination packages offer an autorouter.



Eagle 2.05 is a combination package with extensive libraries and an autorouter capable of handling double-sided board of 10×16 cm (Eurocard size) either automatically or interactively. The PCB layout program offers 1/1000-inch resolution, and various grids on a PCB surface of 1.6 m^2 maximum (approx. 64×64 in.). Each PCB track can have its own width. The operation of the autorouter can be followed on the screen, and may be interrupted and continued at any time. The router has been optimized for two-sided boards, and has a preference for taking directions at an angle of 90°. The current version of Eagle can not be called state-of-the-art with its 50-mil grid and its inability to handle SMA (surface-mount assembly) components. However, the manufacturer has promised that a smaller grid and SMA support will be included in a future release of the program. The new router, to be released towards the end of this

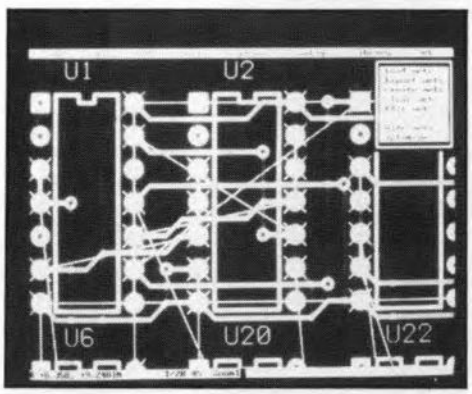
year, is said to offer a resolution of 4 mils at no fewer than 12 layers. SMA should also be supported.

The Eagle package supports all current printer and plotter formats, as well as Postscript. A converter supplied with the program allows netlists and libraries made with Orcad to be loaded.

Eagle is simple to install on an XT or AT computer running under DOS 3.30 or later. The program comes on three disks, and is protected by a dongle plugged into the printer port of the computer. While testing the Eagle package, this caused a problem because on our computer the port happened to be in use for an NEC P2200 printer.

Eagle distributors should be able to supply a demonstration disk at nominal cost.

Boardmaker 1 is an inexpensive program that combines a PCB design program and a schematic drawing program. PCB layouts can be edited, and the program comes with a component library and a library editor.

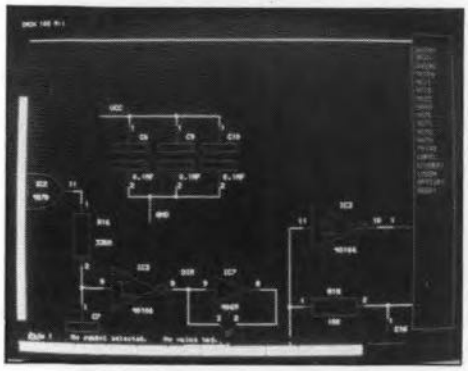


Boardmaker supports Excellon NC drill, Gerber photoplotter and Postscript output formats, but unfortunately lacks a netlist output. The upgraded version, Boardmaker 2, does include a netlist output, but is considerably more expensive than the standard version.

Boardmaker 2 version 2.30 comes on two 5¼-inch diskettes, and is complete with a ring-bound instruction manual. The program is capable of accepting and processing netlists produced by Schema II, Schema III, Protel, Tango Schematic and OrCad.

Tailor-made for Boardmaker 2 is Tsien Laboratories' **Boardrouter**, an interactive autorouter. A number of different parameters included in the command string that calls up the program enable either sections of the board, or the entire board, to be routed. The router can be interrupted and restarted at any time. Boardrouter is protected by a dongle.

The **Ranger 1** package offers a schematic editor and a PCB layout editor with autorouter. Ranger 1 has no on-line design rule



checker. It requires an AT or 386-based PC with a 40 MByte (or larger) hard disk, 640 KByte of RAM, and DOS version 3.30 or later. The package includes two 5¼-inch diskettes, a manual, and a dongle for copy protection.

The schematic drawing program can handle up to eight pages. Components taken from the library can be placed, rotated and mirrored. It is also possible to design new components and add them to the library.

A small word processor enables netlists to be imported, that is, circuit diagrams can, in principle, be made without any drawing activity on part of the user.

The program uses the schematic to generate the parts list and the netlist. After defining the size of the PCB (max. 32×32 in.), the netlist can be used by the PCB design software. Next, the parts are placed on to the board using the well-known rubber-band technique. The Lee track router can be used in manual, interactive or automatic mode. The track placement is directly visible on the screen. The router uses a 1-mil grid.

The program has an option to check the routed board for short-circuits, missing connections or too close by tracks. Errors found are immediately indicated on the screen.

Challenger is a combination package with an excellent price/performance ratio. Supplied by Ultimate Technology, it uses the Ultishell user interface to integrate the Ulticap schematics editor and the Ultiboard PCB design program. Both Ulticap and Ultiboard are 'small' versions of much more expensive high-end programs. Here, 'small' has nothing to do with the performance — only the maximum PCB size is reduced to about 700 pins, corresponding roughly to two times the Eurocard size.

Challenger supports EMS for schematics entry as well as board design, an on-line design rule check, a library containing about 4,000 components, and interfaces to WorkView, DASH, Orcad and Schema. Apart from the very useful 'force vector' and histogram utilities for component placement, the program offers a 'trace shoving' function in the layout phase. This function allows PCB tracks to be moved to make room for new ones, without having to delete and reposition the ones that had been drawn already.

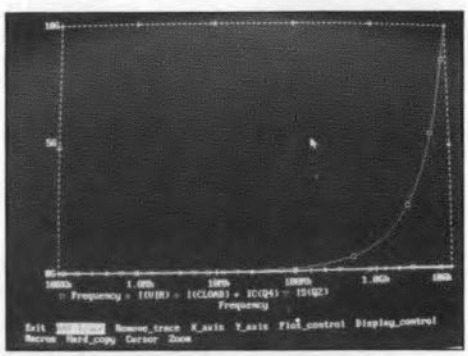
The integrated autorouter, Ultiroute, can handle up to 32 PCB layers simultaneously. Two remarkable features of the Challenger package are the automatic re-wiring after component repositioning in the schematics editor, and the 'hardware zoom' support for certain graphics adapters. In additions to these, Challenger offers the usual functions of auto-panning, parts list and netlist generation, and data output to several plotter and NC standards, as well as to two different Postscript formats.

The Challenger package is not copy protected, and comes with two extensive, well-organized user manuals.

Circuit simulation software

Electronic circuit simulation on a shoestring does not exist, and is marked by huge amounts of data and a high calculation load on the processor. Professional simulation programs such as Accusim require a 400-MByte hard disk, 16 MBytes of main RAM memory, and a Sun-SPARC Workstation Type 2 to work comfortably.

Two simulation packages that can be used on PC-AT computers have found their way to the advanced hobbyist and the laboratory worker. One of these, **Microcap III**, is



supplied in several versions, each with a specific maximum number of nodes (component junctions). The student version, for instance, can handle up to 30 nodes, however does not include a graphics editor or a Monte-Carlo analyser function, and has a relatively small, but extendable, components library.

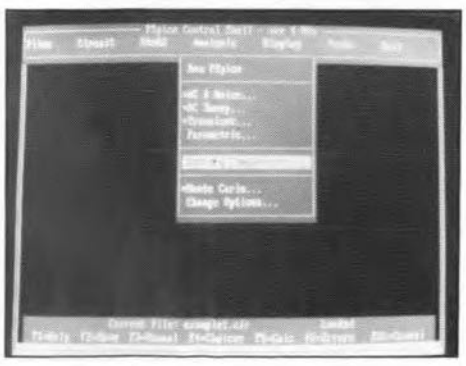
Microcap III offers four ways of examining an electronic circuit: a.c., d.c., transient or Fourier analysis. Initially, the program is used to draw the circuit, which is achieved by loading components from the library, and placing them on the screen. Next, the parameters to be examined are entered, and a

predefined signal source is 'connected' to the input. The program calculates the response of the circuit, and shows the results in the form of a high-resolution graph. The library editor is, of course, much more extensive than that of a schematics drawing program, since the number of characteristics related to a new component is much higher. Consider, for instance, the following basic parameters of a transistor: current gain, current gain in an inverting circuit, temperature coefficient of the current gain, junction resistance, saturation current, etc.

The Monte-Carlo analysis is particularly useful to check the reliability of the circuit in regard of component tolerance. With the aid of this option, the program creates component deviations (within the specified tolerance) in a quasi-random manner, after which a new analysis is run. The Monte-Carlo analysis thus produces a very useful insight into the performance distribution of a particular circuit intended for larger-scale production.

Microcap runs on MS-DOS compatible computers of the AT class and higher, supports expansion memory, and makes use of a coprocessor, if installed. The program comes on four 5¼-inch floppy disks, and is complete with a user manual. The installation should be carried out with care, as it is recorded on one of the disks as a means of copy protection.

The other widely used simulation program for IBM PCs is **Pspice** from Microsim Corp. Pspice requires an AT, 386 or 486 computer equipped with a maths coprocessor. Pspice is available in three versions, ranging from Pspice Evaluation to Pspice DeLuxe.

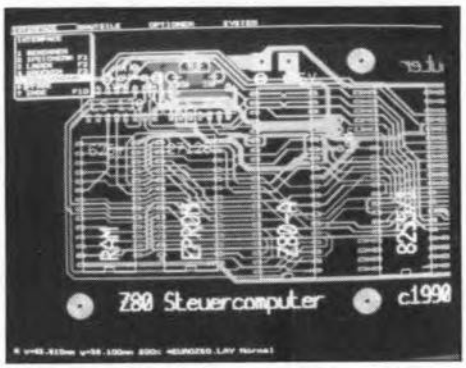


Pspice consists of several parts: a schematics editor, an analyser, a signal source editor, a graphics output function (called Probe), and a utility to establish component parameters (called Parts). In addition to these, the package offers Monte-Carlo and digital simulation utilities. All program function are accessed via a user interface called the Control Shell.

Pspice supports direct circuit entry with the aid of the mouse, as well as entry via parts lists or netlists supplied by the Orcad schematics editor.

PCB design packages

These are basically drawing programs tailored to meet the often exacting demands of PCB (printed circuit board) designers.



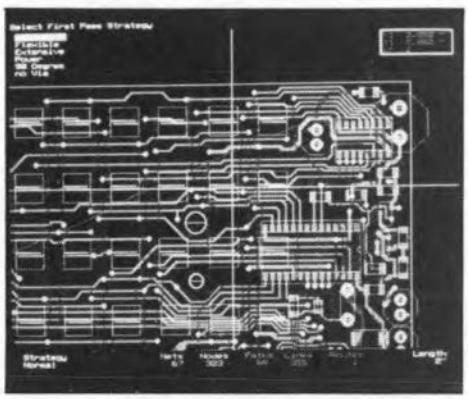
Rule is a simple and inexpensive program capable of producing PCB layouts that meet relatively high standards. Offering the best price/performance ratio in its class, Rule has but one major disadvantage: practically all design work has to be done manually.

Rule can be used on any PC/XT/AT with 640 Kbyte of RAM, one floppy disk drive and MS-DOS, PC-DOS or DR-DOS 2.0 or higher. The program supports Hercules, CGA, EGA and VGA display adapters, which are automatically recognized. The installation is simple and without problems, and may be done on a hard disk. The software is not copy protected. The 5¼-inch floppy disk contains the main program, drivers for Epson compatible printers (8-, 9- and 24-pin types) and HP-LaserJet compatible printers, a components library and a few sample PCB layouts. A 20-page user manual (in English) completes the package.

Rule handles up to 16 layers in a PCB with a maximum size of 23×23 cm. The program is capable of generating the artwork for the component overlay, the drilling template and the solder resist mask. The PC keyboard is used for the basic program functions: select, delete, move, rotate, mirror and copy. These functions may also be selected with the mouse. Lacking an autorouter, Rule forces you to draw tracks from solder pad to solder pad. Fortunately, this is simple to learn, and can be done quite quickly after a while. Output drivers for Postscript, Gerber and Excellon, as well as an extended components library are available separately as upgrades. A HPGL plotter driver is in preparation.

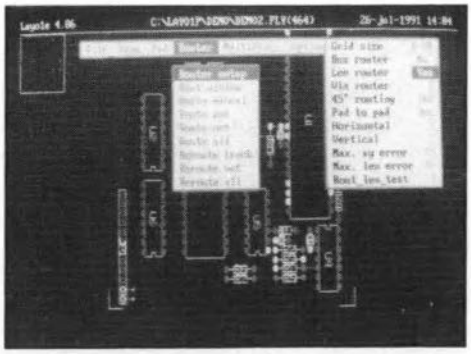
Easytrax from Protel is a PCB design program with an autorouter, offering an excellent price/performance ratio. The current version is 2.06, supplied on four 5¼-inch 360-KByte floppy disks. The program handles PCBs with a maximum size of 32×32 inch, and up to 10 layers (6 of which are for tracks). Easytrax has an integral library which, unfortunately, does not include SMA components. Simple automatic panning is supported, as well as variable zoom factor setting.

The copper track width can be set to between 12 and 100 mils, while solder pads can have any diameter between 40 and 250 mils. On completion of the layout work, the utility Easyplot is used to export the artwork in the HPGL, Calcomp or Roland plotter format, complete with Gerber or Excellon photoplot or drill files. Postscript output is also supported. The autorouter in the Easytrax package is a simple pad-to-pad router that draws a track between two solder pads selected with the mouse.



Another Protel product, **Autotrax**, is an extended, much more powerful, version of Easytrax. Not surprisingly, it is also much more expensive. Although the maximum PCB size is 32×32 inch, Autotrax handles up to 13 layers, of which 6 are used for signals. The use of SMA components is fully supported. The program allows track widths between 1 and 255 mils, and offers 6 different solder pad shapes of a diameter between 1 and 1,000 mils.

The autorouter can be used with any predefined track width and design grid, which is of great importance when working with SMA components. Unlike Easytrax, Autotrax has a netlist importing function, which widens the application range considerably. The program reads netlists produced by Schematic, Tango Schematic, Orcad SDT and Schema. After having the program read the netlist, you can run the Auto-Placer. This utility places the components on to the PCB in a manner that results in the shortest possible tracks and the lowest possible number of through contacts. The decisions of the Auto-Placer can be overridden manually, although this is slightly cumbersome. Autotrax is copy protected by a dongle attached to the printer port of the computer.



Layo 1 Plus is offered in two versions, a Junior version (Layo Plus Junior) and a full-blown version (Layo Plus). The two versions differ only in regard of the maximum PCB complexity. Version 4.8 of Layo Plus is an extremely powerful, all-round PCB design program offering flexible editing features, schematic capture, netlist import (from, among others, OrCad SDT III), an extensive components library containing nearly 500 components (shapes), SMA support, forward annotation, design rule check, project management, real-time rubberbanding, macros and high-speed auto-routing. Layo Plus is capable of working with 16 layers in a PCB of 650×650 mm^2 maximum size. Remarkably, every layer can be shown individually as well as in combination with any other layer(s). The resolution is 1/1280 inch, or about 0.0019 mm. The minimum system requirements to run the Plus version are MS-DOS version 3.3x, an EGA card and monitor, a hard disk with 5 MBytes of free space, and an 8-pin matrix printer. A more comfortable system configuration would, however, look something like this: MS-DOS 4.xx, a VGA card and monitor (resolution up to 1,024× 768), a 40-MByte hard disk, EMS 4.0 with a minimum of 2 Mbytes of extended memory, and a laser printer and/or a plotter.

Input to the program is via a mouse and/or keyboard. A wide variety of output formats (Postscript, DXF and others) and output devices is provided, including printers, plotters, photoplotters and drilling machines. Layo. Finally, Layo is copy-protected by a dongle. ■

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Note: further CAD software for schematics drawing and PCB design is available from **Number One Systems** (0480) 61778, and **Labcenter Electronics** (0274) 542868. For basic product information, please refer to the relevant advertisements in this and previous issues of *Elektor Electronics*.