THE INTERNATIONAL MAGAZINE FOR ELECTRONICS ENTHUSIASTS


I/O interface for IBM PCs Laser - Part 1 Battery tester Conductance meter Video A-D and D-A Augmented A-matrices

# 8032/8052 single-board computer 



The international magazine for clectronics enthusiasts

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- Video A-D/D-A converter Part 2


## Front cover

Seen here is the Mark II version of the popular BASIC computer we published in November 1987. The Mark II is a more powerful system with more RAM, more ROM, an on-board EPROM programmer, and several other additional facilities on a single-sided Euro-size PCB. The computer is ideally suitable for small control applications and software development. It can work with Intel's powerful
8032, 80C32 or
8052AH-BASIC processor. The latter has an on-chip interpreter that allows you to program in BASIC with full access to machine code.

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May 1991
Volume 17
Number 189

# SPEED CONTROL OF LARGE DC MOTORS 

by K.A. Nigim, B.Sc., Ph.D., MIEE


#### Abstract

The power circuit described in this article is used for obtaining a variable direct voltage source from the 50 Hz a.c. mains supply. The variable direct voltage is used, among other applications, for controlling the speed of large d.c. motors.


ALTHOUGH d.c. motors are more expensive than asynchronous a.c. motors, their simplicity and controllability of speed over a wide range puts them in a strong, competitive position for use as electrical drive units in a variety of industrial processing plants.

There are several types of d.c. motor, depending on how the motor windings are connected and excited. The most popular and easiest to handle is the separately excited type. In this, the magnetic field circuit is powered by a separate d.c. power source. This establishes the necessary magnetic flux, $\Phi$, in the windings. When d.c. power is supplied to the armature windings (the coils are embedded in the rotating part of the motor), torque is developed and the motor starts to rotate.

To fully understand the behaviour of the motor when it is powered by different levels of direct voltage, the relationship between the produced torque, current and speed is simplified in the following way. The torque, $T$, developed by the armature windings when the supply is switched on is given by:

$$
T=K_{\mathrm{b}} \Phi I_{\mathrm{a}} \quad[\mathrm{~N}]
$$

where $K_{\mathrm{b}}$ is a motor speed constant that depends on the number of turns the armature windings consist of, how the windings are wound, and the number of magnetic poles; $\Phi$ is the flux per magnetic pole produced by the field windings; $I_{\mathrm{a}}$ is the current (in amperes) flowing in the armature windings and N is the symbol for newton.

The current $I_{\mathrm{a}}$ produces a back electromotive force, $E_{\mathrm{b}}$, which is given by:

$$
E_{\mathrm{b}}=K_{\mathrm{b}} \Phi N
$$

in which $N$ is the steady-state motor speed.

The performance of a motor may be analysed with the aid of its equivalent circuit shown in

Fig. 1. Note that the armature resistance, $R_{\mathrm{a}}$, is in series with $E_{\mathrm{b}}$, because, although the motor has a high inductance, this is ignored during steady-state motor operations.

The field voltage, $V_{\mathrm{a}}$, applied to the ar-


Figure 1.
mature windings is balanced by the sum of the voltage drop $I_{\mathrm{a}} R_{\mathrm{a}}$ and $E_{\mathrm{b}}$ :

$$
\begin{aligned}
V_{\mathrm{a}} & =I_{\mathrm{a}} R_{\mathrm{a}}+E_{\mathrm{b}} \\
& =I_{\mathrm{a}} R_{\mathrm{a}}+K_{\mathrm{b}} \Phi N
\end{aligned}
$$

from which

$$
N=\left(V_{\mathrm{a}}-I_{\mathrm{a}} R_{\mathrm{a}}\right) / K_{\mathrm{b}} \Phi
$$

This is the motor speed which, when ohmic losses are small, may be approximated for practical purposes to

$$
N=V_{\mathrm{a}} / K_{\mathrm{b}} \Phi .
$$



Figure 2

From this equation, it is seen that two methods of speed control are possible. The first one is to alter the supply voltage, $V_{\mathrm{a}}$. The speed may then varied from zero to its maximum rating. The second method is to vary the
magnetic flux, $\Phi$, produced by the magnetic circuit. This method is restricted since the speed range will always be above the specified rated speed, because the magnetic field can not be made any stronger, only weaker. Furthermore, failure of the control circuit would cause very high speeds which might be catastrophic. Generally, therefore, the first method is used to maintain a constant output torque over the entire speed range, while the second method is used where constant shaft power with speed is required.

## Variable d.c. power source

Variable d.c. power may be derived from single-phase or three-phase a.c. mains supplies: in this article only single-phase sources are considered.

There are various ways of converting alternating voltage to direct voltage; the simplest one that can be adopted successfully to vary the speed of a d.c. motor rated at up to 10 kW is shown in Fig. 2. The circuit uses a full-wave rectifier bridge, a freewheeling diode and a thyristor. Each half cycle of the input alternating voltage is rectified by bridge $B_{1}$. The rectified voltage is controlled by thyristor Thy ${ }_{1}$. The thyristor is triggered by phase-controlled signals at its gate. The firing signals are synchronized with the waveform of the mains voltage to provide the required firing delay angle, $\alpha$. The thyristor is switched off every time the supply voltage goes through its zero crossing point.

The various levels of the average direct voltage across a resistive load and the motor are shown in Fig. 3. Two sets of delay angles are shown; one for high power or speed with a short delay angle and the second for low power or speed with a long delay angle. The relation between the produced voltage and the delay firing angle is given by

$$
V_{\mathrm{avg}}=E_{\mathrm{s}(\text { peak })}(1+\cos \alpha) \pi
$$

In practice, the motor can not be represented by a resistive load. As the motor rotates faster, a back e.m.f. is produced for constant magnetic flux. The armature wind-


Figure 3.
ings also possess a large inductance and some resistance: the motor will thus truly behave as a complex load.

The reason for the motor current continuing to flow in spite of the supply voltage dropping below the back e.m.f., point A , is the presence of the armature inductance. This forces the voltage across the armature windings to follow the supply voltage until it becomes negative at point B . At that point, freewheeling diode $\mathrm{D}_{1}$ diverts the current
away from the thyristor which then switches off. When the inductive current flowing through the armature windings and $D_{1}$ has decayed to zero, point C , the freewheeling diode ceases to conduct and the voltage across the armature windings returns to the level of $E_{\mathrm{b}}$. From this, it is clear that $\mathrm{D}_{1}$ allows the circulation of stored energy and maintains a continuous load current. This is a healthy process, since a continuous flow of current through the load is essential for proper control of a


Figure 4.
d.c. motor.

## Thyristor synchronized firing logic

The diagram of the electronic circuit that provides the required phase control (delay angles) over the range $0-180^{\circ}$ is shown in Fig. 4. It may be divided into three sections: that producing the synchronizing signal, the comparator, and the gate drive. It is powered by a 12 V regulated power source based on a Type 7812 regulator $\left(\mathrm{IC}_{3}\right)$.

A portion of the rectified, and as yet unsmoothed, voltage at points A and B is applied to the base of transistor $\mathrm{T}_{1}$. The waveform of these voltages is shown in Fig. 5. A pulse is produced at the collector of $\mathrm{T}_{1}$, point C, every time the base voltage drops below a certain level. This pulse is integrated by the combination of amplifier $\mathrm{IC}_{\mathrm{la}}$, capacitor $\mathrm{C}_{1}$, and variable resistor $\mathrm{P}_{1}$.

Transistor $\mathrm{T}_{2}$ is switched on at the onset of each cyle and then short-circuits $C_{1}$ and $\mathrm{IC}_{\text {la }}$. This results in a sawtooth voltage at point $D$. This voltage is compared with a variable d.c. control signal in comparator $\mathrm{IC}_{1 \mathrm{~b}}$. The intersection of these two voltages determines the pulse at the output of the comparator, point F . The variable width of this pulse is, therefore, in step with the waveform of the mains voltage.

The controlled pulse is applied to monostable $\mathrm{IC}_{2}$, which produces a narrow pulse (point G ) at the leading edge of the pulse at the comparator output. The width of the pulse, $t$, at point G is determined by $\mathrm{R}_{10}$ and $C_{3}$ and is kept wide enough to sustain gate drive. The width is given by

$$
\begin{equation*}
t=0.5 \mathrm{R}_{10} \mathrm{C}_{3} . \tag{s}
\end{equation*}
$$

An emitter follower, $\mathrm{T}_{3}$, interfaces the output of the monostable and the gate of the thyristor. To avoid gate isolation, the zero voltage rail is tied to the negative rail of the power circuit shown in Fig. 2. Therefore, the cathode of the thyristor must be tied to the negative rail.


Figure 5.

## Construction and testing

## Firing control circuit.

The firing control circuit, including the 12 V regulated power supply, should be assembled preferably on a printed-circuit board (for which no design is offered) or on a suitable prototyping board.

Owing to the sensitive nature of the circuit, an oscilloscope is needed to check the relative position of the synchronized pulse with respect to the mains voltage.

Connect the channel X probe of the oscilloscope to test point $A$ and the ground clip to the negative supply rail. With reference to Fig. 5, check the waveforms at points A, B, and C, with the channel Y probe. When the d.c. level at point E is changed, a rectangular wave with variable width should be obtained at point F. At point G, a 2 ms wide pulse should be produced at the leading edge of the pulse at F . Changing the d.c. level with $\mathrm{P}_{2}$ should shift the pulse over the range $0-180^{\circ}$ with respect to the waveform at $A$.

Network $\mathrm{R}_{7}-\mathrm{C}_{2}$ across $\mathrm{P}_{2}-\mathrm{R}_{8}-\mathrm{R}_{9}$ ensures a soft start of the control voltage applied to $\mathrm{IC}_{\mathrm{lb}}$, and sets the minimum and maximum delay angles, thus determining the minimum and maximum speeds of the motor.

Connect a $100-500 \Omega$ resistor between the emitter of $T_{3}$ and the negative rail to check that an output pulse is produced.

Network $\mathrm{R}_{12}-\mathrm{C}_{8}$ provides current and $\mathrm{d} v / \mathrm{d} t$ gate protection.

Power circuit and motor.
The ratings of bridge $B_{1}$, diode $D_{1}$ and the thyristor depend on the load current. If, for instance, it is required to control a 3.75 kW d.c. motor, the current rating for a mains voltage of 240 V is close to 16 A . Both the diode and thyristor, mounted on a suitable heat sink, should then be rated at 35 A .

To test the power circuit, connect the cathode of the thyristor to the negative rail of the bridge rectifier. To play safe, first connect a 100 W light bulb instead of the motor windings across $D_{1}$. Connect the output of the control circuit to the thyristor gate and the cathode of the thyristor to the negative rail. When the delay angle is varied from minimum to maximum, the light bulb should behave exactly as if it were controlled by a light dimmer.

Next, connect the armature windings of the motor (low resistance on a multimeter) across $\mathrm{D}_{1}$. Before switching the supply to the motor, make sure that there is a voltage supply to the field windings (high resistance on a multimeter). Refer to the motor name plate for the rating of the field circuit. When the supply to the motor is switched on and the motor rotates in the wrong direction, switch off and swap the connections to the armature windings.

Finally, protect the thyristor by connecting a series $R C$ network between its anode and cathode. Suitable values are $R=30 \Omega$ $(3 \mathrm{~W})$ and $C=0.1 \mu \mathrm{~F}(1000 \mathrm{~V})$.

## COMPONENTS LIST (FIG. 4)

## Resistors:

R1, R4 $=10 \mathrm{k} \Omega$
$\mathrm{R} 2=470 \Omega, 0.5 \mathrm{~W}$
R3, R5, R14 $=1 \mathrm{k} \Omega$
$R 6=22 \mathrm{k} \Omega$
$R 7=47 \mathrm{k} \Omega$
$R 8=3.3 \mathrm{k} \Omega$
$R 9=2.7 \mathrm{k} \Omega$
$\mathrm{R} 10=15 \mathrm{k} \Omega$
R11, R13 $=6.8 \mathrm{k} \Omega$
$\mathrm{R} 12=100 \Omega$
$\mathrm{P} 1=10 \mathrm{k} \Omega$ cermet potentiometer
$\mathrm{P} 2=5 \mathrm{k} \Omega$ multiturn potentiometer

## Capacitors:

$\mathrm{C} 1=1 \mu \mathrm{~F}, 63 \mathrm{~V}$
$\mathrm{C} 2, \mathrm{C} 8=0.1 \mu \mathrm{~F}, 100 \mathrm{~V}$ polypropylene
$\mathrm{C} 3=0.15 \mu \mathrm{~F}$ polypropylene
$\mathrm{C} 4=2200 \mu \mathrm{~F}, 25 \mathrm{~V}$, electrolytic
C5, C6 = 22 nF , ceramic
$\mathrm{C} 7=10 \mu \mathrm{~F}, 35 \mathrm{~V}$, tantalum

## Semiconductors:

$\mathrm{B} 1=$ bridge rectifier, $200 \mathrm{~V}, 0.5 \mathrm{~A}$
D1, D2 = 1N4001
D3 = LED, green
$\mathrm{D} 4=$ zener diode, 4.7 V
$\mathrm{T} 1, \mathrm{~T} 2=\mathrm{BC} 107$
$\mathrm{T} 3=\mathrm{BFY} 51$
$\mathrm{IC} 1=\mathrm{LM} 358$
$I C 2=C D 4098$
$\mathrm{IC} 3=7812$

## 8032/8052 SINGLE-BOARD COMPUTER



## H. Reelsen

MICROCONTROLLERS these days are silent workers in many apparatus, ranging from the washing machine to the video recorder, to mention but two examples in the home. Nearly all of these controllers are mask-programmed and therefore of very little use for hobby applications since the
program they execute can not be altered. And even if we could alter the program, the information necessary to do so - an instruction set, an assembler language description and some basic hardware information - is often not available or very difficult to obtain. Also, the last resort of many programmers, a cross-assembler, is long sought but never found. In short, many microcontrollers, powerful as they may be, are not accessible
(but bear in mind that they were not designed to be so).

An marked exception to the above 'misery' is the 8052AH-BASIC from Intel. This microcontroller has features that seem to make it more accessible than any other single-chip microcontroller with a reasonable price tag. Consider, for instance, its bit manipulation instructions, its internal BASIC interpreter, its ability to program

EPROMs, or load a BASIC program into memory via a three-wire RS-232C link.

In 1987 we published a single-board computer based on the 8052AH-BASIC (Ref. 1), and it has been a popular project ever since. The computer was not only built and programmed by vast numbers of computer enthusiasts, its design concept was also taken up commercially, witness the sudden influx of 8052-based controller boards and development systems following our publication.

The single-board computer described here is an upgraded version of the 8052AHBASIC computer. The improvements are basically a larger RAM and ROM space of 32 KByte each, a memory backup circuit with $2 \mu \mathrm{~A}$ RAM data retention current, a $12.5-\mathrm{V}$ EPROM programming voltage supply, and, last but not least, the possibility to use the ROM-less (inexpensive) 8032 or 80C32 microcontroller. A further boon for the home constructor is that the printed-circuit board for the present computer is singlesided and designed with $0.4-\mathrm{mm}$ wide copper tracks for easy reproduction. This allows the cost of the computer to be kept to a minimum. If a double-sided board had been used, it would probably have cost more than all the components on it to build the 8032 version of the computer.

## The circuit

The heart of the circuit shown in Fig. 1 is either the ROM-less $80(\mathrm{C}) 32 \mathrm{CPU}$ or the 8052AH-BASIC processor. The LS (least-significant) group of address lines, A0-A7, is multiplexed with the data, and extracted with the aid of octal latch IC8 when the ALE (address latch enable) signal is logic high. The latched databits are fed direct to the data inputs of the system RAM and ROM, as well as to buffer IC9. The MS (most-significant) group of address lines, A8-A15, is not multiplexed and connected direct to the memories and the address decoders, $\mathrm{IC}_{1}, \mathrm{IC}_{2}$ and IC3.

The memory map of the system has the following structure:

- two ROM ranges, one from $0000_{\mathrm{H}}$ to $3 \mathrm{FFF}_{\mathrm{H}}$ and one from $8000_{\mathrm{H}}$ to BFFFH; $^{2}$
- one RAM range from $0000_{\mathrm{H}}$ to $7 \mathrm{FFFH}_{\mathrm{H}}$.
- An I/O range mapped between addresses $\mathrm{C} 000_{\mathrm{H}}$ and $\mathrm{COFFH}_{\mathrm{H}}$.

The structure of the memory map is illustrated in Fig. 2. Wire jumper Br 1 when fitted allocates the range from $0000_{\mathrm{H}}$ to $1 \mathrm{FFF}_{\mathrm{H}}$ (a part of the ROM range) to the internal BASIC interpreter ROM in the 8052AH-BASIC processor. The wire jumper is removed when an external ROM (or EPROM) is used, as required in most cases with the $80(\mathrm{C}) 32$.

The ROM and RAM ranges have an overlapping area between $0000_{\mathrm{H}}$ and $1 \mathrm{FFF}_{\mathrm{H}}$. The PSEN signal allows the processor to use this 'shared' area either as program memory or data memory. This means that the memory structure of the 80(C) 32 and 8052 is not based on the 'classic' Von Neumann model in which the memory areas allocated to program and data are arranged as contiguous blocks in the address space. Fortunately, the


Fig. 1. Circuit diagram of the single-board computer. Note that although a 80 C 32 CPU is sh

present system does allow for a 'classic' address division. This is achieved as follows: access to the lower 16 Kbytes in the ROM (EPROM) area is only allowed when the CPU supplies the appropriate address, and actuates the PSEN line. The upper 16 KByte range can be selected with the appropriate address and the $\overline{R D}$ (read) or the PSEN signal. This means that the upper 16 KByte range may function as a data memory or a program memory, which is a requirement for the storage of BASIC programs. The memory division is realized by a 74 HC 00 (IC2) whose gates are combined to form a kind of decoder.

The lower 16 KByte block in the RAM range between $0000_{\mathrm{H}}$ and $7 \mathrm{FFF}_{\mathrm{H}}$ can only be used as data memory, while the upper 16 KByte block can be used as data memory or program memory because it does not overlap the ROM range. The upper block is therefore suitable for writing and debugging programs written in machine code.

The address decoding of the RAMs is arranged by IC3. Gate IC 1 b combines address lines A14 and A15 to provide an input/output address strobe, $\overline{\mathrm{IOAD}}$, required for the signalling of access to the address range above $\mathrm{C} 000_{\mathrm{H}}$, i.e., the range reserved for $\mathrm{I} / \mathrm{O}$ operations.

Although IC9 latches the lower address byte like IC8, it is controlled differently via its $\overline{\mathrm{OE}}$ input which is connected to the previously mentioned $\overline{\mathrm{IOAD}}$ line. This means that the 8 -bit address is latched only when $\overline{\mathrm{IOAD}}$ is actuated. Otherwise, the de-actuated IC outputs are held at +5 V by a resistor array and so represent a value $\mathrm{FF}_{\mathrm{H}}$.

The datalines are buffered by an octal three-state bus driver, IC10. The $\overline{\mathrm{RD}}$ signal supplied by the controller is inverted by IC2c and determines the data direction (read/write) of IC10. To keep the external bus free from all of the data transfer oper-
ations performed by the processor, IC 10 is enabled by $\overline{\mathrm{IOAD}}$ via its $\overline{\mathrm{G}}$ input.

Port 1 is freely available and may be used to convey outgoing as well as incoming data. A bidirectional bus driver Type 74HC245 protects the controller and increases the drive capacity when the port is used as an output. The logic level applied to the P1DIR connection determines the direction of the data. When P1DIR is not connected, or connected to ground, the port functions as an output (write). The input function (read) is selected by making P1DIR logic high. The $2.7 \mathrm{k} \Omega$ resistors between IC11 and the controller prevent overloading when port 1 is programmed as an output while IC11 supplies data as a result of incorrect programming. The resistors limit the processor output current to a safe 2 mA or so in this output-against-output conflict.

A memory backup circuit retains the RAM data when the power is removed from the computer. A PCB-mount 3-V lithium cell supplies the required data retention current to RAM IC6 via resistor R10 and diode D3. When the computer is in normal use, diode D4 conducts and D3 isolates the backup battery. If you have a sensitive voltmeter, the data retention current may be measured indirectly as the voltage across resistor R10: 1 mV corresponds to about $1 \mu \mathrm{~A}$ of RAM current.

The RAM is automatically switched to its low-power standby state when the power is removed. This function is effected by a MOSFET, T2. As long as the computer is powered by the mains supply, the FET takes the $\overline{\mathrm{CE}}$ input of the RAM low. When the power is removed, the FET arranges the $\overline{\mathrm{CE}}$ input to be effectively connected to the retention voltage via resistor R9. In this manner, the RAM is never allowed to be in a non-defined state (i.e., $\overline{\mathrm{CE}}$ 'floating' while a voltage exists across the supply terminals) which results in


Fig. 2. Parts of the memory space in the system are shared by ROM and RAM. A special kind of memory addressing is therefore required to access the right data or program.
a relatively high current drawn from the battery.

## Interfaces

Programming the board in BASIC essentially requires a serial keyboard as an input device, and a serial display as an output device. The two functions are probably best combined into a terminal or a PC running a terminal emulation or general-purpose communication program (see Refs. 2 and 3).

The SBC has an on-board serial interface that works with TTL levels. The RX (received data) and TX (transmitted data) terminals of this interface are available on the DIN-VG64 connector, K1. Although the serial interface of the SBC works basically with TTL levels, there should be no problem in hooking it up to a terminal or PC with an RS232C-compatible input/output. Designed to work with $\pm 12-\mathrm{V}$ signals, most of these interfaces work happily with TTL $(0 \mathrm{~V} /+5 \mathrm{~V})$ signals, although it must be noted that the noise immunity suffers considerably when a relatively long cable is used between the SBC and the PC or terminal.

At the side of the SBC, the signal received at terminal $R X$ of connector $K_{1}$ is made positive only and limited to a swing of 5 V by R20, a resistors in 8-way array R21, and diode D5. The RS232C signal is inverted as required by that standard by IC12. The serial signal at the TX output of the SBC has a swing of 5 V , and is connected to the RxD input of the terminal. The RX input of the SBC is connected to the TxD output of the terminal or PC.

The two interrupt inputs of the board, INT0 and INT1 (pins c3 and c5 respectively on K1) enable the processor to respond quickly to external events. The use of interrupts is of particular interest when the SBC is at the heart of a computer-controlled system. A software interrupt is acknowledged by the processor with an appropriate servicing routine written by the user.

The SBC may be reset with an external signal via the $\overline{\text { RES }}$ terminal, pin c11 on K1. Since IC12 contains inverting buffers, the write (WR), read (RD) and I/O address (IOAD) signals are active-high on connector K 1 . An example of the use of these signals for a data input/output decoder is shown in Fig. 4.

## On-board EPROM programmer

The 8052AH-BASIC processor is capable of storing a BASIC program in EPROM starting from address 8000 H . The hardware to do so consists of opamp IC5, transistor T1 and a handful of passive parts. The non-inverting input of the opamp is held at +5 V , while the inverting input is connected to pin a12 (PRG) of connector K1 via a $2.2 \mathrm{k} \Omega$ resistor. A low level on PRG takes the opamp output high. Transistor $\mathrm{T}_{1}$ then supplies a programming voltage of about 12.5 V to the Vpp pin of the system EPROM, IC7. When the PRG line is at +5 V , the V pp pin is at 5 V also.


Fig. 4. Illustrating byte-wide input/output for the SBC. Shown here are two suggested external circuits to effect memory-mapped input/output operations with the single-board computer. Both circuits are wired to the system extension connector. The left-hand circuit reads an array of eight push-buttons in a keyboard, while the right-hand circuit is a basic output device that controls eight LEDs.

The ALE signal must be disabled while the EPROM is being programmed. This is achieved by the processor making the ALDIS line logic low. To program an EPROM, connect the PRG terminal to port line P1.4, and the ALDIS line to port line P1.3. The P1DIR terminal is not connected, and jumper Br 2 is best removed.

The programming sequence is indicated by LED D6, which lights only when the programming voltage is higher than about 6.5 V. Wire jumper Br 2 must not be fitted while D6 lights.

## Which processor?

The choice between a 8052 AH-BASIC, a 80 C 32 or a 80 C 32 processor is up to you. The latter two do not have an on-chip BASIC interpreter, and can only be programmed in machine code. It is, however, possible to unload the BASIC interpreter from the 8052AH-BASIC, transfer it to EPROM, and run it with a $80(\mathrm{C}) 32$. How this can be achieved is detailed in Refs. 2 and 3. In addition to the information provided in these earlier publications we print another EPROM downloader - see Fig. 4.

The 80C32 can work with much faster clocks than the 8052AH-BASIC: according to the manufacturer, it is capable of operating at a clock of 16 MHz . A couple of our prototypes however worked fine at a clock of 24 MHz . By contrast, the HMOS 8052AHBASIC threw in the towel at about 15 MHz .

## Power supply

The unregulated power supply voltage to the SBC should normally lie between 8 V and 12 V . To enable the $12.5-\mathrm{V}$ stabilizer around $\mathrm{IC}_{1}$ and $\mathrm{T}_{5}$ to operate correctly, a minimum supply voltage of about 16 V is required when an EPROM is to be programmed. Provided IC4 is adequately cooled, the SBC may be powered permanently with 16 V obtained from a simple mains supply: a $12-\mathrm{V}$ transformer, a bridge rectifier and a $1,000 \mu \mathrm{~F}$ capacitor should do the job.

The current consumption of the SBC depends on the ICs fitted. When the CMOS 80 C 32 is used, you can expect a current consumption between 50 mA and 150 mA . The HMOS CPUs (8032 and 8052AH-BASIC) will require the power supply to deliver more
than 300 mA . Depending on the type of EPROM installed (CMOS or non-CMOS), add another 100 mA or so to the current requirement.

## Practical use

The microcontroller has its own clock generator which operates in conjunction with a quartz crystal. Remove inductor L1 when a quartz crystal specified for fundamental frequency resonance is used, as with the 8052AH-BASIC, which will not go faster than 15 MHz or so. Since most crystals of 20 MHz and higher are overtone types, L1 must be fitted when a $24-\mathrm{MHz}$ type is used with a 80 C 32 processor. A $1.5-\mu \mathrm{H}$ inductor then prevents the crystal resonating at its fundamental frequency of 8 MHz .

In case the computer does not function spot on, the power-on reset capacitor, C 9 , may have to be changed from 220 nF into a $4.7 \mu \mathrm{~F}$ tantalum type. This may be necessary when the supply voltage rises too slow at power on.

You will need software to program the computer, and to use the computer in conjunction with a terminal. MCS-52 assemblers


Fig. 5. Track layout (mirror image) and component mounting plan of the single-sided printed circuit board for the computer.
and cross-assemblers are available for use on a PC, and the object code may be transferred to the SBC by means of an EPROM. If you want to avoid the hassle of burning EPROMs, debugging the program, erasing the EPROM and programming it again, consider the use of an EPROM emulator which forms a direct link between the PC used to develop the program and the target system,
in this case, the SBC.
By virtue of its internal BASIC interpreter, the 8052AH-BASIC is much simpler to get going than the 80C32: connect the terminal or PC to the SBC via RX, TX and ground, set a baud rate of anything between 300 and 19,200, reset the SBC and press the space bar to initiate the automatic baud rate timing. The message

## *MCS-51 (tm) BASIC V1.1 READY

should appear on the console display, and you are ready to start entering or downloading a BASIC program.

One final note: when the 8052AH-BASIC is used, do not suspect a malfunction of the memory backup circuit if you find that your program has disappeared. The BASIC inter-

## COMPONENTS LIST



```
1 FOR \(I=0\) TO 8191 : XBY (I+8192)=CBY(I) : NEXT I
10 PRINT "UNIVERSAL PROM PROGRAMMER" : PRINT "WHAT TYPE OF DEVICE ?"
PRINT : PRINT "1 = EEPROM" : PRINT "2 = INTELLIGENT EPROM"
    PRINT "3 = NORMAL ( 50 MS ) EPROM" : PRINT : \(\operatorname{INPUT}\) "TYPE \((1,2,3)\) - ",T
    ON (T-1) GOSUB \(340,350,360\)
    REM this sets up intelligent programming if needed
    \(\operatorname{IF} \mathrm{W}=.001\) THEN \(\operatorname{DBY}(26)=\operatorname{DBY}(26)\). OR. \(8 \operatorname{ELSE} \operatorname{DBY}(26)=\operatorname{DBY}(26)\). AND. OF7H
    REM calculate pulse width and save it
    PUSH (65536-(W*XTAL/12)) : GOSUB 380
    POP G1 : \(\operatorname{DBY}(40 H)=G 1: P O P\) G1 : DBY \((41 \mathrm{H})=\mathrm{G} 1\) : PRINT
    INPUT " STARTING DATA ADDRESS - ",S : IF S<512.OR.S \(>\) OFFFFH THEN 100
    PRINT : INPUT " ENDING DATA ADDRESS - ",E
    IF E<S.OR. E>OFFFFH THEN 110
    PRINT : INPUT " PROM ADDRESS - ",P : IF P<8000H.OR.P>OFFFFH THEN 130
    REM calculate the number of bytes to program
    PUSH (E-S)+1 : GOSUB \(380:\) POP G1 : DBY (31)=G1: POP G1: DBY(30) = G1
    REM set up the eprom address
    PUSH (P-1): GOSUB 380 : POP G1 : DBY ( 26 ) \(=\mathrm{G} 1:\) POP G1: DBY \((24)=\mathrm{G} 1\)
    REM set up the source address
    PUSH S : GOSUB 380 : POP G1 : DBY (27)=G1 : POP G1: DBY (25)=G1
    PRINT : PRINT "TYPE A 'CR' ON THE KEYBOARD WHEN READY TO PROGRAM"
    REM wait for a 'cr' then program the eprom
    \(\mathrm{X}=\mathrm{GET}\) : IF \(\mathrm{X}<>\) ODH THEN 220
    REM program the eprom
    PGM
    REM see if any errors
    IF (DBY (30).OR.DBY (31)) =0 THEN PRINT "PROGRAMMING COMPLETE" : END
    PRINT : PRINT "***ERROR***ERROR***ERROR***" : PRINT
    REM these routines calculate the address of the source and
    REM eprom location that failed to program
    \(\mathrm{S} 1=\operatorname{DBY}(25)+256 * \operatorname{DBY}(27): \mathrm{S} 1=\mathrm{S} 1-1: \mathrm{D} 1=\operatorname{DBY}(24)+256 * \operatorname{DBY}(26)\)
    PHO. "THE VALUE ", XBY (S1), : PH1. " WAS READ AT LOCATION ", S1 : PRINT
    PHO. "THE EPROM READ ",XBY(D1), : PH1. " AT LOCATION ",D1 : END
    REM these subroutines set up the pulse width
\(\mathrm{W}=.0005\) : RETURN
\(W=.001\) : RETURN
\(W=.05\) : RETURN
    REM this routine takes the top of stack and returns high, low bytes
    POP G1 : PUSH (G1.AND.OFFH) : PUSH (INT(G1/256)) : RETURN
```

Fig. 6. Type in this listing if you want to unload the BASIC interpreter from the 8052AH-BASIC CPU, transfer it to EPROM and run it with a 8032 or 80 C 32 . The advantages: lower cost and higher speed. The pulse timing in this program is based on a clock of 11.0592 MHz .
preter on reset runs a memory test that clears all of the RAM content. When the program is transferred to EPROM, you have the option to use the programming mode PROG3, which forces the interpreter to clear the memory up to the value indicated by MTOP. All data above MTOP is retained.

## References:

1. "BASIC computer". Elektor Electronics November 1987.
2. "CMOS replacement for 8052 AH -BASIC" Elektor Electronics January 1990.
3. "ROM-copy for 8052-BASIC computer". Elektor Electronics September 1990.

For further reading:

1. Microcontroller Handbook, Intel Corp 1984.
2. MCS® BASIC-52 users manual, Inte Corp. 1984, order no. 270010-001.
3. "LCD for 8052 microcontroller". Elektor Electrontics Supplement July / August 1990.


## CORRECTIONS

## Wattmeter

April 1991, p. 32-35
With reference the circuit diagram, Fig. 1, the right-hand terminal of the lower section of switch S2 should be connected to the circuit ground. This point is indicated by a dot.

In the adjustment procedure given on page 35 , the references to presets $\mathrm{P}_{4}$ and P 5 have been transposed. Contrary to what is stated, P4 sets the vY offset, and P5 the vx offset. The functions of the presets are shown correctly in the circuit diagram, Fig. 1.

To improve the accuracy of the instrument, connect R5 direct to the circuit ground instead of junction R6-R7. Finally, all circuit board tracks carrying mains current must be strengthened with $2.5-\mathrm{mm}^{2}$ cross-sectional area solid copper wire if currents higher than about 5 A are measured.

## 80C32/8052 Single-board computer

May 1991, p. 17-23
When a CPU type 8031 or 8052AH-BASIC is used, $\mathrm{IC}_{1}, \mathrm{IC}_{2}, \mathrm{IC}_{3}$, and $\mathrm{IC}_{8}-\mathrm{IC}_{12}$ must be 74 HCT types. Jumper B is erroneously reffered to as Br 2 in the text under "On-board EPROM programmer". Contrary to what is stated, this jumper must be fitted only when an EPROM is to be programmed - for all other use of the SBC, it must be removed. Also note that jumper B may only be fitted when the programming LED is out.

## Sequential control

July/August 1991, p. 61
Motor M should be a d.c. type, not an a.c. type as shown in the circuit diagram.

## Digital phase meter

June 1991, p. 32-39
In Fig. 5, the switch between input ' $A$ ' and IC 1 should be identified ' Sl ', and that between input 'B' and IC2 'S2'. Switch S4 is an on/off type, not a push-button as shown in the diagram. Capacitors C3 and C6 are shown with the wrong polarity. The component overlay of the relevant printed-circuit board (Fig. 8) is all right.

## Universal NiCd battery charger

## June 1991, p. 14-19

The parts list on page 19 should be corrected to read

$$
\mathrm{C} 7=2200 \mu \mathrm{~F} 25 \mathrm{~V}
$$

When difficult to obtain, the BYW29/100 (D5) may be replaced by the BY229, which is rated at 6 A .

The text under the heading 'Calibration'
should be replaced by:
4. Connect a multimeter between points G and H on the board, and adjust P 4 until the measured voltage is 1 V lower than the voltage on the battery terminals.

## MIDI program changer

April 1991, p. 14-17
The contents of the EPROM should be modified as follows:

| address | data |
| :--- | :--- |
| OOBC | E5 |
| 00 C 7 | 80 |
| 00 C 8 | CB |
| 00 C 9 | F 5 |
| 00 CA | 7 B |
| 00CB | 12 |
| 00 CC | 00 |
| 00 CD | D 2 |
| 00 CE | C 2 |
| 00 CF | 02 |
| 00 D 0 | 80 |
| 00 D 1 | C 2 |

Readers who have obtained the EPROM readyprogrammed through the Readers Services may return it to obtain an update.

## Electronic exposure timer

March 1991, p. 31-35
Please add to the parts list on page 32:
$\mathrm{C} 16=33 \mathrm{pF}$

## Augmented A-matrices

May 1991, p. 42-43
The drawing below was erroneously omitted in the left-hand bottom corner of page 43.


## UNIVERSAL I/O INTERFACE FOR IBM PCs


#### Abstract

Those were the days when you could use your Commodore C64, Acorn Atom or ZX81 computer to control hardware intelligently. Model train systems, robots, greenhouse watering and temperature control systems - all within easy reach of the keen programmer with little or no knowledge of computer hardware. Alas, the coming of the IBM PC, the compatibles, the ATs and the 386-based systems, seems to have banished simple hardware interfacing, the PC being an expensive 'box' harnessing a lot of computing power, but restricted to use in an office environment. We do not agree that a PC is unsuitable for control applications: all it needs is the circuit described here: a low-cost fully buffered insertion card that forms a versatile, simple and safe link between the PC (whether an XT, AT or 386-based machine) and your own hardware.


USING a computer and some home-brew software to control apparatus is sheer fun. A few lines of program code allow lamps to light, motors to start turning, and model trains to find their way on a complex track system. Sensors and other types of recorder device enable a computer to measure and store physical quantities from the 'real world' around us.

Unfortunately, an IBM PC or compatible appears to be less suitable for the above control applications as it is very much a closed system designed for office use. Does that imply that we have to say goodbye to the model train system and the computer-controlled hobby lathe? No! Many of you will have noted that PC interface cards are being offered for industrial control applications. Unfortunately, these cards are pretty expensive, so it's time for a low-cost solution.

## Count the components

The circuit shown in Fig. 1 may well be the simplest PC I/O interface you have ever seen, having only three ICs, three resistors and three capacitors. The interface is suitable for all types of IBM PC and compatibles, i.e, XTs, ATs and 386-based systems.

The circuit acts as a buffer between the computer and the external hardware, and is set to operate at a unique address in a small area in the PC's I/O range.

As shown in the circuit diagram, the connector between the computer and the interface card is a type with 31 connections at each side. This is the well-known IBM PC expansion slot connector. A small number of signals available on this connector are used

for the present interface and/or the hardware controlled by it. The external hardware is connected to K 1 , a 20-way PCB header that provides the 8 -bit wide databus, two address lines, an enable signal and the read and write signals. The computer's $5-\mathrm{V}$ supply rail is also available on K 1 , allowing small (experimental) digital circuits to be powered without the need of an external supply.

The address decoding logic ensures that interface card occupies four addresses in the I/O range reserved for prototyping cards. The actual address setting is accomplished with three switches in DIP switch block S1. In all cases, a free base address must be used, i.e., the interface card must not share an I/O address with any other card in the PC. The four addresses in the block are selected individually by A0 and A1. For convenience the DIP switch settings are printed on the component overlay of the interface card (see the component mounting plan in Fig. 2b).

The three switches determine the logic level at inputs P0, P1, P2 and P3 of IC1. The pull-up resistors connected to these inputs provide a logic high level when a switch is opened. When a switch is closed, the relevant IC input is logic low. All other P inputs of IC1 are held at fixed logic levels.

Address lines A2 to A9 on the expansion bus are connected to inputs Q0 to Q6 of address comparator IC1. An AND gate, IC3d, combines address lines A8 and A9 at input Q6. This frees input Q7 for use by AEN, the address enable signal that indicates DMA (direct memory access) activity without an I/O address being decoded. Gate IC3c ensures that IC 1 is enabled during a read or write operation only. When the binary code at the P inputs equals that at the Q inputs, output $\mathrm{P}=\mathrm{Q}$ goes low. This signals the selection of the user hardware hooked up to connector K1. The $\overline{\mathrm{P}=\mathrm{Q}}$ output also actuates the $\overline{\mathrm{G}}$ input of IC2, which enables the PC's databus to be connected to the databus on K 1 . The direction of the dataflow between the PC and the external hardware is determined by the level of the $\overline{\mathrm{RD}}$ (read) signal. A low level means that data is transferred from K1 to the PC, while a high level means data transfer from the PC to K1. Both the $\overline{R D}$ and the WR (write) signal on connector K 1 are provided by the PC and buffered by a gate, IC 3 a and IC 3 b respectively. The PC's databus is buffered by IC2. Since all PC signals are buffered, the risk of cross-effects between the PC and the external hardware is reduced to a minimum.

## Construction

The compact printed-circuit board designed for the PC interface is shown in Fig. 2. Ready-made boards supplied through our Readers Services are provided with goldplated bus contact fingers. Connector K 1 is a so-called box header with right-angled PCB pins. It protrudes from a clearance cut in the support bracket attached to the rear side of the circuit board. This arrangement allows ready connection of a flatcable with an IDC connector.


Fig. 1. Circuit diagram of the interface card for IBM PCs and compatibles. This ultra-simple circuit forms the ideal link between a PC and your own hardware developments.


Fig. 2a. Mirror-image track layouts of the PCB component side and solder side.

After mounting all components, set the DIP switches to the desired I/O address. To avoid an address conflict, consult the manuals of other cards inserted in the PC to



Fig. 3. Pinning and signal assignment on connector K1.


Fig. 2b. Component mounting plan.

## Floppy disk emulator for PCs

The recently introduced EDISK insertion card from DSS innovative electronics is capable of emulating a floppy disk drive in a PC. The maximum storage capacity of the EDISK is 4 MBytes with EPROMs fitted, or 1 MBytes with static RAMs fitted. The following EPROM types may be used: $27(\mathrm{C}) 512$ ( 64 KBytes); 27(C)010 (128 kBytes); $27(\mathrm{C}) 020 \quad$ (256 kBytes); 27(C)040 ( 512 kBytes). The card supports two 32 kByte SRAM types, the 62256 and the 621000 .

The EDISK card enables you to replace the mechanical floppy disk drive A: by an all solid-state equivalent, which will be faster as well as more reliable, offering a speed of the order of a RAM disk. The main difference between the EDISK and a RAM disk, however, is that the contents can be stored in non-volatile EPROMs, or stored in static RAM. When the computer is switched off, the pro-

## NEW PRODUCTS

grams contained in the EDISK will be retained in static RAM by virtue of a back-up battery. Another difference is that the EDISK is automatically writeprotected if EPROMs are used. The EPROMs are loaded with the aid of a programmer; their content can not be changed or erased by the PC user.

Since the EDISK is based on non-volatile memory, it is possible to boot the computer without a floppy disk, or even without a disk controller card.

The EDISK allows a combination of EPROMs and RAMs to be fitted, which effectively emulates two drives, drive A: containing EPROMs and drive $B$ : SRAMs.

Applications of the EDISK include a 'stripped' XT computer that can be connected to a network as a diskless station.

Alternatively, a motherboard fitted with an EDISK and a special I/O card can form a powerful control system. The use of SRAMs allow system parameters to be stored and altered as required.

For more information on the EDISK contact
DSS innovative electronics - Accustrat $25 \cdot 3903$ LX Veenendaal $\cdot$ Holland. Tel. +318385 41301. Fax: +31 838526751.

nector K1. The $\overline{\mathrm{P}=\mathrm{Q}}$ output also actuates the $\bar{G}$ input of $I C 2$, which enables the PC's databus to be connected to the databus on $\mathrm{K}_{1}$. The direction of the dataflow between the PC and the external hardware is determined by the level of the $\overline{\mathrm{RD}}$ (read) signal. A low level means that data is transferred from K 1 to the PC, while a high level means data transfer from the PC to K1. Both the $\overline{R D}$ and the $\overline{W R}$ (write) signal on connector K 1 are provided by the PC and buffered by a gate, IC3a and IC 3 b respectively. The $\mathrm{PC}^{\prime} \mathrm{s}$ databus is buffered by IC2. Since all PC signals are buffered, the risk of cross-effects between the PC and the external hardware is reduced to a minimum.

## Construction

The compact printed-circuit board designed for the PC interface is shown in Fig. 2. Ready-made boards supplied through our Readers Services are provided with goldplated bus contact fingers. Connector $K_{1}$ is a so-called box header with right-angled PCB pins. It protrudes from a clearance cut in the support bracket attached to the rear side of the circuit board. This arrangement allows ready connection of a flatcable with an IDC connector.


Fig. 2a. Mirror-image track layouts of the PCB component side and solder side.

## PART 1: POWER SUPPLY AND MIRROR GALVANOMETERS

Over the past few years, a variety of low-power Helium-Neon (MeNe) laser tubes has found its way into the electronics surplus trade circuit. Unfortunately, these laser tubes are nearly always sold without a suitable power supply, which, being a high-voltage unit, is not so simple to construct. In this two-instalment article we describe a power supply for the popular 2-mW class of laser tubes, a beam steering system based on mirror galvanometers and last but not least a state-of-the-art modulator that enables laser patterns to be created with the aid of a music signal. The circuits described are designed and marketed as kits by ELV.

MOST power supplies for laser exciters are fairly conventional circuits based on a cascade-type voltage multiplier. Unfortunately, these circuits exhibit very low efficiency and have the further disadvantage of being powered from the mains, which makes them dangerous units in many respect. Having a low-power laser tube complate with a suitable casing is one thing, actually making it work is quite another. The stumbling block is nearly always the power supply with its special transformer and high-voltage components.

The good news is that all owners of a twomilliwatt MeNe laser unit can now build a compact, high-efficiency switch-mode power supply: all the parts required to do so are contained in a kit supplied by ELV. The mirror galvanometers and associated control interface are also available in kit form. Many home-made lasers use conventional mirrors fitted on bulky loudspeaker drive units. The mirror galvanometer system discussed here achieves far better beam positioning accuracy, and is much smaller and more sensitive than any loudspeaker-based system. In addition, the mirror control system (to be described in Part 2) is an advanced circuit capable of absolute beam positioning, li-
nearizing a part of the mirrors' frequency response, supplying a number of Lissajous patterns, and much more.

## Mirror galvanometers

A mirror galvanometer is basically a measuring instrument based on a small mirroo attached to a suspension system. The position of the mirror is determined by the level of electrical current sent through a coil in a permanent magnet assembly. A beam of light is reflected by the mirror and the spot of light moves, in principle, across a linear scale. In the present application, a miniature mirror galvanometer is fitted where the laser beam leaves the exciter tube, allowing the beam to be steered to give patterns. The mirfor is positioned by a suitable drive signal, which may be supplied by an audio amplifier. By using two mirror galvanometers fitted at right angles, we are capable of deflecting the laser beam in two directions, horizontal $(\mathrm{X})$ and vertical $(\mathrm{Y})$.

From a constructional point of view, a mirror galvanometer is almost identical to a moving coil meter. The galvanometers used here, however, reverse the operating primciple by using a coil as the stator and a sus-

pended magnet instead of the other way around. The practical realization is shown in Fig. 1. The magnet is divided into two parts suspended from a glass carrier. The carrier is fixed to a flexible silicone pivot, and forms the base for about 40 deposited layers of glass that form a high-precision interference mirror. The irregularities on this surface are smaller than 60 nanometre, or about one tenth of the wavelength of the laser light. The reflection efficiency of the mirror is very high: $99.7 \%$ for light incident at an angle of $45^{\circ}$. This means that the mirror hardly contributes to the attenuation or divergence of the laser beam. Since the mirrors are precision instruments, the glass surface must never be touched - a fingerprint degrades the reflecting performance considerably.

The mirror is positioned with the aid of a coil wound around the moving parts. The


Fig. 1. Basic construction of a mirror galvanometer.


Fig. 2. Laser beam deflection as a function of coil voltage and frequency.

soft iron core around the coil concentrates the magnetic field in the direction of the magnets attached to the mirror. The resultant magnetic force makes the mirror tilt. The silicone suspension system provides a small counterforce that stops the mirror at a certain position, preventing it from tilting completely. The amount of deflection is determined by the magnetic field strength, the inertia of the mirror, and the counterforce of the pivot. Since the magnetic force depends on the level of current that flows through the coil, the deflection of the laser beam incident on the mirror can be controlled fairly accurately by controlling the current through the coil. In practice, however, it is easier to use a voltage rather than a current to control the mirror. Fortunately, this is not a problem since the coil represents a certain resistance. This resistance, albeit reactive, enables voltage drive of the coil.

The deflection of the mirror is not linear but dependent on the frequency of the signal applied to the coil - see Fig. 2. The curves show the correlation between the voltage and the frequency of the coil signal for mirror deflections of $7.5^{\circ}$ and $15^{\circ}$. Fortunately, the actual response of the mirrors is a little better than suggested by the two curves. In practice, the deflection of the mirrors will be almost linear for single frequencies in the range from 0 to about 60 Hz . Serious deviations are, however, caused when more than one frequency is applied to the coil. This happens when the galvanometer coils are driven directly by a music signal. In most cases, however, accuracy is then not a point - what counts is an attractive pattern.

Electrically, the mirror system behaves not unlike an $8-\Omega$ loudspeaker. This means that the deflection system can be connected to almost any AF power amplifier, provided the drive power is limited to about 1 W . Also, the frequency spectrum of the drive signal is limited to about 120 Hz as the mirrors are not capable of following 'faster' signals. When they are not removed or suppressed, signal components of 120 Hz and higher cause additional unnecessary heating of the mirror system.

## High-voltage laser supply

As already mentioned, the present laser supply is somewhat different from most earlier designs because it is off the beaten track formed by mains transformers, cascades and series resistors. The high-voltage supply presented here has an input requirement of 10 to 16 V , and thus can be used independently of the mains. The current consumption is modest at about 1 A , allowing the unit to be powered from a car battery, a set of NiCd batteries, or a suitably rated mains adapter. The proposed PSU is a switch-mode DC-DC converter with current stabilisation to ensure that the laser tube supplies the maximum light intensity without having its lifetime degraded.

The circuit diagram of the power supply is given in Fig. 3. The input voltage is connected to reservoir capacitor C 5 via a polarity


Fig. 3. Circuit diagram of the high-voltage laser power supply.

reversal protection, D1. The positive terminal of $\mathrm{C}_{5}$ is connected to the primary winding of a ferrite-core transformer, Tri. The current through this winding is switched by transistor T 1 . The transistor is driven by a pulse-width modulated (PWM) rectangular signal that allows the voltage induced in the secondary winding of Tr 1 to be controlled. The transformer secondary is connected to a special rectifier/voltage multiplier. First, the secondary voltage is rectified by diodes $D_{2}$ and D3 for the negative and positive halfcycles respectively. This means that the total voltage across reservoir capacitors C 7 and C 8 is about two times the peak value of the alternating voltage supplied by the secondary winding of Tr1. Since D4 conducts and C9 is relatively small, the high voltage is maintained even after ignition of the laser. The laser operating voltage is then 1,400 to $1,500 \mathrm{~V}$. When ignition has not yet taken place, i.e., when the tube draws no current as yet, D4 and C9 plus D3 and C7 form a voltage doubler. This arrangement gives a total voltage multiplication of six times. Since the laser does not draw current at this stage, the voltage control system enables the maximum output voltage of about 10 kV to be achieved briefly. Immediately after ignition of the laser, the output voltage drops to the nominal operating value. This happens because of the small value of C 9 , and the action of the voltage control system.

Unfortunately, the voltage control circuit does not obviate a current limit resistor in the HV output line. However, the resistor used here has half the value of the one used in a conventional cascade-based laser supply, and introduces a power loss of only 0.75 W instead of the more usual 1.5 W or more.

## COMPONENTS LIST

| Resistors: |  |  |
| :---: | :---: | :---: |
|  | $6 \mathrm{k} \Omega 8$ | R1 |
| 1 | 470, | R2 |
| 1 | 6851 W | R3 |
| 3 | $1 \mathrm{k} \Omega$ | R4;R8;R9 |
| 3 | 10 kS | R5; $\mathrm{R} 6 ; \mathrm{R} 7$ |
| Capacitors: |  |  |
| 1 | $10 \mu \mathrm{~F} 25 \mathrm{~V}$ | C1 |
| 1 | $4 \mathrm{nF7}$ | C2 |
| 2 | $1 \mu \mathrm{~F} 100 \mathrm{~V}$ | C3:C4 |
| 1 | 220uF 16 V | C5 |
| 1 | 1 nF | C6 |
| 2 | 10 nF 1.600 V | C7:C8 |
| Semiconductors: |  |  |
| 1 | 1N5400 | D1 |
| 3 | BY509 | D2;D3;D4 |
| 1 | BU406 | T1 |
| 1 | SG3525 | IC1 |
| Miscellaneous: |  |  |
| 1 ferrite-core HSP transformer Tr1 |  |  |
| 2 PCB terminal block |  |  |
| 1 ABS enclosure |  |  |
| 40 cc epoxy resin (compound) |  |  |

Fig. 4. Double-sided printed circuit board for the laser power supply.

The power supply has a stabilized output current of 5.1 mA to keep the laser beam intensity at the maximum level without shortening the tube life. The regulation circuit to achieve this is contained in IC1. The current consumption of the laser is measured by means of the voltage across R 8 . This voltage is passed to pin 1 of IC1 via R9. Pin 2 of the same IC is held at a constant voltage of 5.1 V . The two input voltages are compared, and the difference is used to control a rectangular wave generator with a variable duty factor (pulse/pause ratio). When R8 measures no current, i.e., when the laser has not yet ignited, the duty factor of the PWM signal is 1 (i.e., a square wave is produced). Hence, the transformer supplies the maximum secondary voltage. The frequency of the PWM signal is fixed at about 25 kHz , allowing a transformer to be used of a size much smaller than a mains transformer with an equal power rating.

It is well known that laser exciters have a very low efficiency. The laser tube used here is no exception: it requires about 10 watts of
input power to supply about 2 milliwatt of laser light. That's an efficiency of $0.02 \%$, and you will like to hear that the PSU used to power the laser is at least reasonably efficient.

## Construction of the PSU

Although the laser PSU supplies only small currents, every possible care must be taken to prevent that any part of the circuit can be touched while it is operational. Remember: the maximum output voltage is about 10 kV , and the normal output voltage about $1,500 \mathrm{~V}$. Both voltages can cause nasty and possibly harmful electrical shocks, so be careful.

Another source of danger is the light produced by the laser proper. Never look direct into the laser beam; your eyes may be permanently damaged. Never point the laser beam at a person. At some distance of the exciter, the beam is less harmful, but still, never look into it. During laser shows in discotheques and the like, the beam moves continuously and is unlikely to be harmful as the

eye is 'hit' very briefly and at a considerable distance from the exciter.

The design of the printed-circuit board for the high-voltage PSU is given in Fig. 4. Remarkably, the board has only one, round copper area at the component side. This area forms one 'plate' of high-voltage capacitor C9, which is etched on the board. The single copper area at the component side is connected to the circuit by soldering the anode terminal of diode D3 at both sides of the PCB. The layout of the solder side of the PCB (Fig. 4) shows three grey areas that must be cut out with the aid of a jig-saw (fret-saw) to prevent arcing.

The construction of the PSU board is straightforward - simply follow the components list and the component overlay printed on the board. To prevent arcing, cut all soldered component terminals to a length of 1.5 mm or less. Do not cut its terminals and fit transistor T 1 as high as possible above the PCB surface, but at the same time make sure its terminals are soldered securely. This leaves the metal tab of the transistor in contact with air after the supply is cast in a moulding compound.

The low-voltage connections, ST1 and ST2, are made either via solder terminals or via wires soldered direct to the copper pads. A wire length of 10 cm is sufficient when the PSU is to be built into the exciter cabinet. Use wire of a cross-sectional area of $0.4 \mathrm{~mm}^{2}$ or greater. If you use stranded wire, make sure all individual wires pass through the PCB hole. One wire, however thin, may cause a short-circuit!

The last part to be fitted onto the PCB is the ferrite transformer (note: you must have fitted D2 and D3 beforehand, since they are located underneath the transformer). First, however, cut off the transformer terminals that are not connected to a winding. These terminals are easily identified.

Once the transformer has been fitted on the board, the PSU is ready for testing. Note, however, that this must never be done without a load connected. So, before switching on, connect either the laser exciter unit or a $250 \mathrm{k} \Omega$ resistor made from 25 series-connected $10 \mathrm{k} \Omega$ resistors with a minimum power rating of 0.33 W . When the laser ex-
the internal resistor) to the upper pin on the PSU board (ST3), and the cathode wire to the lower pin (ST4). To ensure the greatest distance between the connections, solder the anode wire to the top side of ST3, and the cathode wire to the lower side of ST4.

The mirror galvanometer assembly is fitted to the laser cabinet with the aid of four screws that are inserted from the inside of the cabinet into the mirror unit. The photograph in Fig. 6 shows the mirror assembly attached to the laser cabinet, with the cover plate removed. The mirror assembly has two screws that enable the rest position of the mirrors to be adjusted.

## Power supply and cooling

Any power supply with an output of 12 V d.c. at a nominal current of 1 A can in principle be used to power the laser. The safest and cheapest power supply is probably a ready-made mains adapter. In many cases, however, mains adapters do not meet the specifications as regards output current. The typical symptoms of an overloaded mains adapter are extreme heating and a slowly falling output voltage. Obviously, the mains adapter used to power the laser must be capable of supplying 1 A at 12 V for extensive periods. If you have doubts about the performance of your mains adapter, use a more powerful type, or build a separate 12 V supply.

Given its very low efficiency we can safely say that all of the input power of the laser (approx. 10 W ) is dissipated as heat. To keep the operating temperature of the laser tube within safe limits, there should be ample airflow around the device. The laser cabinet shown in the photographs has slots in the side panels to prevent heat building up inside.

Continued next month.

Nu layl

A complete kit of parts for the laser is available from the designers' exclusive worldwide distributors:

## ELV France

B.P. 40

F-57480 Sierck-les-Bains
FRANCE
Telephone: +3382837213
Facsimile: +3382838180
The type code of the kit that contains the laser power supply, the laser exciter tube and the metal cabinet is LPS12. The type code of the kit that contains the mirror galvanometer assembly is LA90.

dou doubler. This arrangement gives a total voltage multiplication of six times. Since the laser does not draw current at this stage, the voltage control system enables the maximum output voltage of about 10 kV to be achieved briefly. Immediately after ignition of the laser, the output voltage drops to the nominal operating value. This happens because of the small value of C 9 , and the action of the voltage control system.

Unfortunately, the voltage control circuit does not obviate a current limit resistor in the HV output line. However, the resistor used here has half the value of the one used in a conventional cascade-based laser supply, and introduces a power loss of only 0.75 W instead of the more usual 1.5 W or more.


Fig. 4. Double-sided printed circuit board for the laser power supply.

## INTERMEDIATE PROJECT


#### Abstract

A series of projects for the not-so-experienced constructor. Although each article will describe in detail the operation, use, construction and, where relevant, the underlying theory of the project, constructors will, none the less, require an elementary knowledge of electronic engineering. Each project in the series will be based on inexpensive and commonly available parts.


## BATTERY TESTER


#### Abstract

This month we describe a useful little instrument that gives a clear condition indication for the most popular types of dry battery. Based on one integrated circuit and a coloured LED bar that functions as a readout, the tester is both inexpensive and simple to build.


RUNNING a quick condition check on the batteries before using portable equipment can help prevent a lot of frustration. The professional photographer, for instance, can not rely on his good fortune when he starts to use his flasher to make, say, a series of wedding photographs. He knows that there can be no excuses for mishaps: the flasher must work under all conditions, and

## L. Lemon


must have fresh, tested, batteries. Similarly, if rechargeable batteries are used, they must be fully topped up and known to have their full capacity.

There are, however, instances where a partly exhausted battery can be used without problems. But then again, it is useful to have at least an indication of how long we can rely on the battery to supply its nominal
voltage. For this purpose we can use the present tester. It has a number of ranges with different test currents for popular dry batteries of $1.5 \mathrm{~V}, 4.5 \mathrm{~V}$ and 9 V . On pressing the TEST button on the instrument, a VU-meterlike read-out gives an unambiguous full/usable/flat indication. No difficult-toread scales or expensive moving coil meters here: just three colours: red for 'flat', orange for 'usable' and green for 'full'.

## Loading, e.m.f. and measuring

If you have ever attempted to test a battery simply by measuring its voltage with a multimeter, you may have noted that the battery in question may be virtually exhausted even though its voltage is, say, less than $10 \%$ below the nominal value. The explanation for this is that degradation of battery capacitance is a matter of increasing internal resistance rather than decreasing cell voltage.

A multimeter with a very high internal resistance gives a corresponding indication of the e.m.f. (electromotive force) of the battery. We must hasten to add, however, that the term e.m.f. applies strictly to an unloaded source of electrical energy but is sometimes erroneously used as being equivalent to a potential difference. The e.m.f., $E$, of a battery will supply a current $I$ to an external resistance $R$ :
$E=I(R+r)$
[volt]
where $r$ is the internal resistance of the battery. From this equation it is simple to see


Fig. 1. The circuit diagram of the battery tester is basically a standard application of National Semiconductor's LM3914 LED bargraph driver IC.
that $E$ may correspond closely to the nominal battery voltage as long as $r$ is small with respect to $R$. Returning to the above battery test using a voltmeter, a digital multimeter will have a typical input resistance of several megohms, so $r$ is bound to be small in any case, even it is, say, five times the value specified for a 'fresh' battery. The upshot is that the capacity (not the e.m.f.) of a dry battery can only be measured when the load resistance equals, say, ten times the internal resistance of the battery. If the battery is capable of supplying its nominal voltage at the resultant load current, its internal resistance is still relatively small. If the battery is exhausted, the internal resistance will have risen to a value that is no longer small with respect to the load resistance.

## The circuit: a single-chip voltmeter

The circuit in Fig. 1 is a kind of VU (volumeunit) meter based on a single IC and LEDs $\mathrm{D}_{1}-\mathrm{D}_{10}$. The load resistors that set the battery test current, R7-R12, are selected with a rotary switch. The battery is effectively loaded when push-button $\mathrm{S}_{2}$ is pressed.

The dual-pole rotary switch in the circuit, S 1 , enables one of six load resistors to be selected. Each load resistor has a value geared to a particular type of battery, of which the capacity, as you probably know, depends on size, construction and chemical composition. The first four ranges are for 1.5 V batteries. The load currents are for button cells, penlight batteries (IEC-R6), IEC-R14 ('baby') batteries and IEC-20 ('mono') batteries. The
selected load resistor is connected across the battery terminals when $S_{2}$ is pressed. Assuming that the relevant battery is full, it supplies 0.7 mA (button cell), 10 mA ('pen-
light'), 45 mA ('baby') or 100 mA ('mono'). The test current for 4.5 V 'power pack' batteries is 66 mA , and 27 mA for $9-\mathrm{V}$ (PP3 or IEC 6 F22) batteries. Since the battery is connected permanently to the voltmeter, you can instantly see the difference between the open-circuit voltage (virtually the e.m.f.) and the loaded voltage, which is indicated when S 2 is pressed. The larger the difference between the open-circuit voltage and the loaded voltage, the smaller the battery capacitance. Note that the term open-circuit voltage is strictly incorrect here since the battery is connected to the RLO and SIG pins of IC1. However, the LM3914 has such a high resistance between these pins that it is safe to say that the battery is not loaded. Hence, the test current flows only when $\mathrm{S}_{2}$ is pressed.

It should be noted that the tester can only be used with batteries or cells that exhibit a gradually falling voltage curve, as shown in Fig. 2. These batteries include carbon-zinc and alkali-manganese types, as well as nickel-cadmium types (which are rechargeable). The tester is not suitable for battery types whose voltage remains almost constant over the hours of service, and drops suddenly at the end. This type of voltage characteristic is illustrated in Fig. 2 for lithium, silver-oxide and mercury batteries.

## Circuit description: introducing the LM3914

As shown in the block diagram in Fig. 3, the LM3914 from National Semiconductor has

| Range | LED |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | D10 |  |
|  | red | orange |  | green |  |  |  |  |  |  |  |
| 1.5 V | 0.86 | 0.96 | 1.04 | 1.13 | 1.21 | 1.29 | 1.38 | 1.46 | 1.55 | 1.63 |  |
| 4.5 V | 2.58 | 2.83 | 3.05 | 3.31 | 3.57 | 3.82 | 4.07 | 4.33 | 4.57 | 4.82 |  |
| 9.0 V | 5.3 | 5.8 | 6.3 | 6.9 | 7.4 | 7.9 | 8.5 | 9.0 | 9.5 | 10.2 |  |

Table 1. Switch-on voltage levels for the LEDs on the battery tester.


Fig. 2. Typical discharge curves for a number of dry battery types.
an internal network of series resistors connected between the RLO and RHI terminals (pins 4 and 6 of the IC). In the present application, the RLO terminal is connected to ground via R5, while the RHI input is held at a fixed voltage derived from the $I^{\prime}$ 's onboard $1.25-\mathrm{V}$ reference voltage source. The output of the reference is connected to IC pin 7, marked ref out. Hence, the internal resistor network is supplied with an accurately defined voltage. This, in turn, means that there are fixed voltages at the taps on the series network (i.e., at the junctions of the resistors that form the ladder network). There are 10 taps on the ladder, and each of these is internally connected to the +input of an associated comparator. The other inputs of the 10 comparators are connected to the output of an internal buffer opamp, whose input is connected to IC pin 5, marked SIG (for signal). The main function of this opamp is to protect the 10 comparators against reversed or too high input voltages.

Because of the ladder network in the LM1914, the comparator which is closest to the RLO input will toggle at the lowest input voltage. As the input voltage rises, more comparators toggle, until the 'highest' one, i.e., the one associated with the top of the ladder at the RHI input, changes state. The comparator outputs are connected to an internal decoder (not shown in the block diagram) with active-low outputs marked L1 to L10 in the circuit diagram. Here, the decoder is set to operate in the 'dot' mode, which means that only one LED lights at a time, depending on the input voltage applied to the tester.

The stabilized voltage at pin 7 of the LM3914 can be changed within certain limits by connecting pin 8 to a voltage divider. Note, however, that the voltage between pins 8 and $6-7$ is fixed at 1.25 V . Thus, the indication range of the voltage meter can be changed by giving resistors R1 to R4 appropriate values. In the present circuit, this is achieved with the aid of a rotary switch which creates the three voltage ranges, 1.5 V , 4.5 V and 9 V . Table 1 shows the voltages at which the LEDs of the VU-meter light. The red LED lights when the battery is flat, one of the orange LEDs when the battery is usable, and one of the green LEDs when the battery is full, covering a range from usable to fully topped.

## Building the battery tester

The track layout and the component mounting plan shown in Fig. 4 are used to produce a printed-circuit board for the battery tester (ready-made PCBs are unfortunately not available for this project). The internal construction of the prototype of the battery tester is shown in the Fig. 5. The 'test' button, S 2 , is connected to the board via two short wires before it is secured to the front panel of the ABS enclosure. Do not cut the terminals of the 10 LEDs before you solder them onto the board. The distance between the PCB and the front panel of the enclosure is determined by the mounting height of the LEDs. As shown in Fig. 5, the PCB is secured to the


Fig. 3. Internal circuit of the LM3914 bargraph driver (illustration reproduced here by courtesy of National Semiconductor).



Fig. 4. Printed-circuit board for the battery tester.


Fig. 5. As shown here, the PCB is secured to the front panel of the enclosure with the aid of four long M3 screws and plastic PCB spacers.

COMPONENTS LIST

| Resistors: |  |  |
| :--- | :--- | :--- |
| 1 | $180 \Omega$ | $R 1$ |
| 1 | $1 \mathrm{k} \Omega 8$ | $R 2$ |
| 2 | $10 \mathrm{k} \Omega$ | $R 3 ; R 5$ |
| 1 | $8 \mathrm{k} \Omega 2$ | $R 4$ |
| 1 | $680 \Omega$ | $R 6$ |
| 1 | $2 \mathrm{k} \Omega 2$ | $R 7$ |
| 1 | $150 \Omega$ | $R 8$ |
| 1 | $33 \Omega$ | $R 9$ |
| 1 | $15 \Omega$ | $R 10$ |
| 1 | $68 \Omega$ | $R 11$ |
| 1 | $330 \Omega$ | $R 12$ |
| Capacitors: |  |  |
| 1 | $10 \mu \mathrm{~F} 25 \mathrm{~V}$ | C 1 |

## Semiconductors:

| 7 | green rectangular |  |
| :--- | :--- | :--- |
|  | LED e.g., LGB480F | D1-D7 |
| 2 | orange rectangular |  |
|  | LED e.g., LYB480H | D8;D9 |
| 1 | red rectangular LED |  |
|  | e.g. LSB480H | D10 |
| 1 | LM3914 | IC1 |

## Miscellaneous:

1 two-pole six-way rotery switch for PCB mounting S1
1 push-to-make button
1 ABS enclosure approx. dimensions: $110 \times 45 \times 55 \mathrm{~mm}$
front panel of the box by four plastic spacers. Cut a slot in the front panel, and adjust the position of the LEDs such that their tops are just flush with the front panel surface.

The rotary switch used is a double-pole six-way type with solder pins for PCB mounting. The range and test current indications on the front panel are made with the aid of rub-down symbols as shown in Fig. 6. The tester is powered by a small mains adapter with a $12-\mathrm{V}$ d.c. output which need not be regulated. This adapter is connected to the circuit via a small socket of the type used on portable cassette recorders and pocket calculators - see Fig. 5.

Finally, LED D1 lights when the tester is powered but not connected to a battery. It is, therefore, a perfect on/off indicator!


Fig. 4. Printed-circuit board for the battery tester.


# VIDEO A-D/D-A CONVERTER 

## PART 1: INTRODUCING THE ICs


#### Abstract

Although fast 8 -bit video converters are available from a variety of manufacturers, their practical application has so far been over the head of the average electronics hobbyist with an interest in video signal processing. Fortunately, that situation has come to an end with the introduction of a number of simple to use A-D and D-A converter ICs from Philips Components. Two of these ICs, the TDA8708 ADC and the TDA8702 DAC, form the heart of an advanced video converter described in this two-instalment article. This month we discuss the basic operation of ADC and the DAC, followed next month by a constructional project intended to get you going with video encoding/decoding experiments, digital video processing, sync locking techniques, etc.


## P. Godon (Philips Components, Paris)

## TDA8708 <br> analogue-to-digital converter

The TDA8708 contains more than just a fast ADC - in fact, it should be referred to as a 'video analogue input interface'. The internal diagram of the TDA8708, which is also available in a surface-mount assembly package (suffix -T), is given in Fig. 1. Clearly, the ADC is but one of a number of functional blocks contained in the IC. Each of the three analogue video inputs, VIN0, VIN1 and VIN2 may be driven by a CVBS (chrominance-video-blanking-synchronization) signal of an average level between 0.45 V and 1.6 V measured with respect to the analogue ground, AGND. The typical input capacitance of the vinx inputs is about 1 pF , while the input impedance lies between $10 \mathrm{k} \Omega$ and $20 \mathrm{k} \Omega$ (input capacitance and input impedance values without external components). The video input selection is effected by applying logic levels to the 10 and 11 inputs of the chip as shown below:

## Table 1. Input channel selection

| I1 | IO | VINX |
| :--- | :--- | :--- |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 2 |
| 1 | 1 | 2 |



Fig. 1. Internal diagram of the TDA8708 analogue-to-digital converter.

The video amplifier features switchable AGC (automatic gain control) and clamping circuits. The AGC sets the upper video level (peak white); the clamping, the lower video level (base of sync pulse). As illustrated in Fig. 2, the peak white level produces the highest digital value, and the base of the sync pulse, the lowest digital value. The AGC and clamping sections receive information on the instantaneous drive level of the ADC via three comparators: one for the white level, one for the black level and one for the sync level. The AGC and the clamping logic each drive a pulsating direct current source that controls the video amplifier gain. The control current causes a voltage drop on the AGC capacitor connected to pin 25 of the TDA8708. The minimum and maximum video amplifier gains are 0.5 and 2.3 times respectively, corresponding to control voltage levels of 2.8 V and 4.0 V . As an option, the gain may be determined externally by omitting the AGC capacitor and applying a direct voltage instead. This, however, requires a fairly accurate temperature compensation circuit.

The gain of the internal amplifier is also controlled as a function of the lower video level: here, the voltage across the clamp capacitor at pin 24 is subtracted from the instantaneous video input voltage. A current limiting resistor, $\mathrm{R}_{\text {PEAK }}$ at pin 28 , determines the level of the current diverted when the instantaneous level of the video signal exceeds the set limits. With $R_{\text {PEAK }}=0 \Omega$, the diverted current has a maximum level of $80 \mu \mathrm{~A}$.

Table 2 lists the various possibilities of controlling the upper and lower video levels with the aid of logic levels applied to the GATE A and GATE B inputs of the chip.
In mode 1 (GATE $A=$ GATE $B=1$ ), the ADC output values are 255 for peak white and 0 for the base of the sync pulse. Mode 2 by contrast affords greater control over the conversion output values. As shown in Fig. 2, a positive pulse at the GATE A pin links the sync level to a value of 0 . A positive pulse applied to the GATE B pin during the back porch sets the digital value of the top of the sync pulse to 64 . The white level comparator is active all the time. Nominal levels of the video input signal produce a digital value of 213 . This creates a safety margin of between 213 and 240 . When the output value exceeds 240 , the white level comparator reduces the gain of the video amplifier. This is done to reduce the risk of $A D C$ overdrive to a minimum.

The analogue output, AN OUT (pin 19), of the video amplifier is connected to an external anti-aliasing low-pass filter. The maximum amplifier output current is limited to 2.5 mA , while the maximum output voltage is set to $1 \mathrm{~V}_{\mathrm{pp}}$ at a nominal video input level of $1 \mathrm{~V}_{\mathrm{pp}}$. Table 3 lists a few additional characteristics relevant to the input circuit in the TDA8708.

The output signal of the external filter is fed back into the IC via the ADC IN pin. The ADC input may also be driven direct, provided the applied video signal has a voltage range of ( $\mathrm{V}_{\mathrm{CCA}}-1.6$ ) V to $\left(\mathrm{V}_{\mathrm{CCA}}-1.1\right) \mathrm{V}$. The input impedance of the ADC is about $50 \mathrm{M} \Omega$,


Fig. 2. Digital output value as a function of the analogue video input level in mode-1 (top drawing) and mode-2 (lower drawing).

Table 2. TDA8708 Mode Selection

| AB |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  | $<0$ | $-2.5 \mu \mathrm{~A}$ | IPEAK |  |
| 11 | 0-255 | $-2.5 \mu \mathrm{~A}$ | $-2.5 \mu \mathrm{~A}$ | 1 |
|  | $>255$ | lpeak | $-2.5 \mu \mathrm{~A}$ |  |
| 00 | <240 | 0 | 0 |  |
| 00 | $>240$ | 0 | IPEAK |  |
| 10 | $<0$ | $+2.5 \mu \mathrm{~A}$ | 0 |  |
| 10 | 0-240 | $-2.5 \mu \mathrm{~A}$ | 0 | 2 |
| 10 | $>240$ | IPEAK | 0 |  |
| 01 | $<64$ | $+50 \mu \mathrm{~A}$ | 0 |  |
| 01 | 64-240 | $-50 \mu \mathrm{~A}$ | 0 |  |
| 01 | $>240$ | $-50 \mu \mathrm{~A}$ | IPEAK |  |

Table 3. TDA8708 main technical characteristics

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
| :--- | :--- | :---: | :---: | :---: | :---: |
| VCCA | analogue supply voltage | 4.5 | 5.0 | 5.5 | V |
| ICCA | analogue supply current | - | 37 | 45 | mA |
| - | VINx crosstalk | - | -60 | -55 | dB |
| G $_{d}$ | Gain error | - | 2 | - | $\%$ |
| $\Phi_{\mathrm{d}}$ | phase error | - | 2 | - | 0 |
| B | -3dB bandwidth | 12 | - | - | MHz |
| S/N | noise distance | 60 | - | - | dB |
| SVRR | supply voltage rejection | - | 45 | - | dB |
| G | Gain | -4.5 | - | 6.0 | dB |

## Table 4. TDA8708 pin function description

| Pin | Symbol | Description |
| :--- | :--- | :--- |
| $1-4$ | D7 (MSB) - D4 | Digital outputs, bit 7 (MSB) through bit 4 |
| 5 | CL | Clock input |
| 6 | VCCD | Digital supply voltage +5 V |
| 7 | VCCO | TTL output supply voltage +5 V |
| 8 | DGND | Digital ground |
| 9 | OF | Output format and chip enable (3-state) |
| $10-13$ | D3 - DO (LSB) | Digital outputs, bit 3 through bit 0 (LSB) |
| 14,15 | IO, I1 | Video input channel selection |
| $16-18$ | VINO - VIN2 | Analogue video inputs $1,2,3$ |
| 19 | ANOUT | Analogue voltage output |
| 20 | ADCIN | ADC input |
| 21 | DEC | Decoupling capacitor for ADC |
| 22 | VCCA | Analogue supply voltage +5 V |
| 23 | AGND | Analogue ground |
| 24 | CLAMP | clamp capacitor |
| 25 | AGC | AGC capacitor |
| 26,27 | GATEB, GATEA | clamping and sync level control |
| 28 | RPEAK | current limit for AGC |

the DAC output level for load impedances of $10 \mathrm{k} \Omega$ and $75 \Omega$.

While the output voltage (w.r.t. $\mathrm{V}_{\mathrm{CCA}}$ ) at the vout pin is proportional to the digital input value, the voutn pin supplies an inverted output signal. The signals at vout and voutn are typically coupled out via an electrolytic capacitor of $68 \mu \mathrm{~F}$ to $100 \mu \mathrm{~F}$. Each of these introduces a voltage drop,

$$
V_{c}=\frac{V_{\text {Out }} \times R_{L}}{R_{L}+75 \Omega}
$$

where $R_{\mathrm{L}}$ is the load impedance.
The circuit in Fig. 6 shows the two video outputs connected to a differential amplifier. This may be done to increase the suppression of hum and noise on the ADC supply voltage. A suggestion for a simple transistorbased buffer amplifier is given in Fig. 6.

Finally, a few notes on the timing of the TDA8702. As shown in Fig. 7, the DAC is transparent whilecl (clock) is held logic low. Transparent means that the DAC follows the changes of the digital input signal. The
and the input capacitance is as low as 1 pF .
The maximum clock rate of the ADC inside the TDA8708 is 30 MHz . The timing is illustrated in Fig. 4: the analogue input voltage is measured $2 \mathrm{~ns}\left(\mathrm{t}_{\mathrm{su}}\right)$ after the leading edge of the clock signal has exceeded the reference level of 1.5 V . The previous digital word remains on the outputs for another four to six nanoseconds, and is replaced by the new value after a delay $\mathrm{t}_{\mathrm{d}}$ ( 16 to 20 ns ).

The digital outputs of the ADC, Do through D7, have a $20 \mu \mathrm{~A}$ current sinking or sourcing capability. The digital word is supplied either in binary form (with pin of not connected) or as a two's complement value (with pin of at logic 0 ). The ADC outputs are switched to high-impedance when the OF input is made logic high. Finally on the ADC, Table 4 provides the descriptions of the signals associated with the IC pins.

## TDA8702 <br> digital-to-analogue converter

This IC is of a much simpler layout than its counterpart - see the block diagram in Fig. 3. The pinning of the DAC is given in Table 5.

The digital data applied to the TDA8702 is accepted at the D0 through D7 inputs, which are TTL-compatible. The data are buffered by an input interface before they are loaded into a register. As shown in the block diagram, the register drives eight constantcurrent sources that translate the digital value into a corresponding analogue quantity, in this case, a current. Each digital output causes a current of about $85 \mu \mathrm{~A}$ to flow through the $75-\Omega$ resistor. This in turn causes a voltage drop of about 6.3 mV with respect to the positive analogue supply voltage, $\mathrm{V}_{\mathrm{CCA}}$, provided the load impedance is relatively high. Table 6 provides information on


Fig. 3. Block diagram of the TDA8702 digital-to-analogue converter.

## Table 5. TDA8702 pin function description

| Pin | Symbol | Description |
| :--- | :--- | :--- |
| 1 | REF | Reference voltage source decoupling |
| 2 | AGND | Analogue ground |
| 3,4 | D2,D3 | Digital video inputs bits 2,3 |
| 5 | CL | Clock input |
| 6 | DGND | Digital ground |
| $7-10$ | D7-D4 | Digital video inputs bit 7 (MSB) through 4 |
| 11,12 | D1,DO | Digital inputs bit 1 , bit 0 (LSB) |
| 13 | VCCD | Digital supply voltage +5 V |
| 14 | VOUT | Analogue video output |
| 15 | VOUTN | Inverted analogue video output |
| 16 | VCCA | Analogue supply voltage +5 V |

TDA8702 latches the current digital value when the clock signal reaches a value of 1.3 V on the leading edge. To ensure that the output voltage is stable until the trailing edge of the clock signal, the input data must be stable at least 0.3 ns before, and 2 ns after, the threshold is reached. Table 7 lists the main technical characteristics of the TDA8702.

Next month's final instalment of this article will describe a construction project based on the TDA8708 and TDA8702.


Fig. 4. TDA8708 data conversion timing.


Fig. 5. Video output buffer based on a differential amplifier.


Fig. 6. Transistor-based video output buffer for the TDA8702.


Fig. 7. Transparent and latching modes of the TDA8702 DAC.

## Table 7. TDA8702 main technical characteristics

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Symbol | Parameter | Min. |  | Max. | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| VCCA | Analogue supply voltage | 4.5 | 5.0 | 5.5 | V | Zout(N) | Output impedance |  | 75 |  | $\Omega$ |
| Icga | Analogue supply current | - | 26 | 32 | mA | DLE | Differential linearity error |  |  | $\pm 0.5$ | LSB |
| VCCD | Digital supply voltage | 4.5 | 5.0 | 5.5 | $\checkmark$ | ILE | Internal linearity error |  |  | $\pm 0.5$ | LSB |
| ICCD | Digital supply current | - | 23 | 30 | mA | $\mathrm{t}_{\text {su }}$ | Data setup time | 0.3 |  |  | ns |
| Vout(N) | Output voltage ( $\mathrm{Z}_{\mathrm{L}}=10 \mathrm{k} \Omega$ ) | -1.45 | -1.6 | -1.75 | $V$ | thi | Data hold time | 2.0 |  |  | ns |
|  | $\left(Z_{L}=75 \Omega\right)$ | -0.72 | -0.8 | -0.88 | V | $t_{\text {pd }}$ | Propagation delay |  |  | 1.0 | ns |
| Voff | Output offset | - | -3 | -25 | mV | $\mathrm{ts}_{51}$ | Settling time 10-90\% |  | 1.1 | 1.5 | ns |
| $\Delta V_{\text {out }}(\mathrm{N} /$ / $\Delta$ T | Temperature co-eff. Vout |  |  | 200 | $\mu \mathrm{V} / \mathrm{K}$ | ts2 | Settling time $\pm 1$ LSB |  | 6.5 | 8.0 | ns |
| $\triangle V_{\text {OFF/ }} /$ T | Temperature co-eff. Voff |  |  | 20 | $\mu \mathrm{V} / \mathrm{K}$ |  |  |  |  |  |  |
| B3वB | 3 -dB bandwidth of analogue output |  | 150 |  | MHz |  |  |  |  |  |  |

# RECTIFIER CALCULATIONS 


#### Abstract

What is the ripple voltage across the buffer capacitor? What is the level of the peak current through the rectifier diodes? The values of these and many other quantities are often obtained by rule of thumb, but what is the basis of that? This article aims to answer that question.


ATYPICAL, fundamental mains power supply is shown in Fig. 1. In this, $U_{\mathrm{p}}$ is the primary voltage; $R_{\mathrm{p}}$ represents the total losses at the primary side; $U_{\mathrm{s}}$ is the secondary voltage; $R_{\mathrm{S}}$ represents the total losses at the secondary side; $U_{\mathrm{C}}$ is the open-circuit output voltage (e.m.f.).


It is advantageous in most calculations to combine $R_{\mathrm{p}}$ and $R_{\mathrm{s}}$ into a single loss representation at the secondary side and call this $R$. The value of $R$ (in $\Omega$ ) is given by

$$
\begin{equation*}
R=\left(U_{\mathrm{s}} / U_{\mathrm{p}}\right)^{2} R_{\mathrm{p}}+R_{\mathrm{s}} . \tag{1}
\end{equation*}
$$

This means, in effect, that the transformer need no longer be a part of any calculation; the circuit is fed by a source that provides a voltage $U_{\mathrm{s}}$, has an internal resistance $R$ and, for nominal loads, has negligible inductance.

Unfortunately, $R$ can not be calculated readily owing to lack of data, and measuring it is also not possible. An ohmmeter will not do, because that does not take into account the losses caused by stray magnetism. Similarly, the resistance offered by the diodes can not be measured realistically.

For a proper measurement to be made, a variac is needed at the primary side of the transformer (begin with $U_{\mathrm{p}}=0$ ). The buffer capacitor, $C$, is short-circuited by an ammeter (whence the variac).

Start by adjusting the variac until the secondary winding provides the nominal level of current specified by the manufacturer. The primary voltage needed for this depends on the variac, the transformer, the rectifier diode(s), and the ammeter. The current indicated by the ammeter is the r.m.s. value of the short-circuit current, $I_{\mathrm{sc}}$. Now, $R$ (in $\Omega$ ) may be calculated from

$$
\begin{equation*}
R=U_{\mathrm{s}} / I_{\mathrm{sc}} \tag{2}
\end{equation*}
$$

## Draw first, calculate later

Figure 2 shows a few voltages that are involved in the calculations. If rectifiers were ideal components, the waveform of $U_{\mathrm{s}}$ would indeed be as drawn. Since, however, ideal components do not exist, the voltage that is available to charge the buffer capacitor is lower than $U_{\mathrm{s}}$ by the knee voltage of the diodes, $U_{\mathrm{d}}$. The level of that knee voltage depends on the number of diodes and on the forward voltage of each diode. The bridge rectifier in Fig. 1 will lower $U_{\mathrm{s}}$ by about 2 V . The voltage, $U$, after the rectifiers is thus

$$
\begin{equation*}
U=U_{\mathrm{s}}-U_{\mathrm{d}} . \tag{3}
\end{equation*}
$$

In most textbooks, the waveshape of that voltage is shown slightly differently: roughly as the dashed line in Fig. 2 immediately below the peak of $U$. In reality, the voltage will have a shape somewhere between the dashed and solid curves of $U_{C}$, depending on the ratio charging current : discharge current.

The shape of the (solid) curve of $U_{C}$ is explained as follows. From the moment that $U$ becomes larger than $U_{C}$, current flows from the voltage source to the buffer capacitor via resistor $R$. The level of the current is determined by the difference between $U$ and $U_{C}$, which is $U_{R}$, and the value of $R$ across which that difference voltage exists.

At the onset, $U_{R}$ is tiny and the charging current, $I_{\mathrm{ch}}$, is smaller than the discharge
current, $I_{\text {dis }}: U_{c}$ will then drop to $U_{\min }$ (the minimum value of $U_{C}$ ). From there, $U_{C}$ rises and may go on rising after $U$ has begun to drop again (because $I_{\mathrm{ch}}$ is then still larger than $I_{\text {dis }}$ ). However, at a given instant, $U$ becomes too small and the capacitor starts to discharge. How much $U_{C}$ will drop depends on the current, $I_{L}$, that the capacitor must supply to the load and on the duration, $t_{\text {dis }}$, of the discharge current.

The level of load current is known from the specification of the power supply. The duration of the discharge current is equal to the period of the rectified voltage minus the time necessary to charge the capacitor. The charging period is (as yet) unknown, but in general it is much smaller, in fact, negligible, compared with the discharge period. That means that the discharge time is equal to the period, $T_{\mathrm{r}}$, of the rectified voltage. Note that $T_{\mathrm{r}}$ depends on the frequency and the method of rectification. For instance, in full-wave rectification, the capacitor is charged twice as fast as in half-wave rectification. That means that in half-wave rectification $T_{\mathrm{r}}=1 / f$ and in full-wave rectification $T_{\mathrm{r}}=1 / 2 f$.

The charge, $Q$, that the capacitor can supply in that time is given by

$$
\begin{equation*}
Q=I T_{\mathrm{r}} . \tag{4}
\end{equation*}
$$

The ripple voltage, $U_{\mathrm{r}}$, may be calculated from

$$
\begin{equation*}
U_{\mathrm{r}}=Q / C=I / 2 f C . \tag{5}
\end{equation*}
$$



Apart from the ripple voltage, the mean capacitor voltage, $U_{C \mathrm{~m}}$, or, if voltage regulators are used, the minimum capacitor voltage, $U_{C \text { min }}$, is important. The exact computation of these voltages is, unfortunately, fairly complex and, therefore, in this article approximations are used, based on the data that have been found so far. Which of the two approximations given must be used for the mean capacitor voltage depends primarily on the ratio $R: R_{L}$, where $R$ represents the total resistance of the trans-
former and the rectifier and $R_{L}$ is the load through which current $I_{L}$ flows. If $R_{L}$ is large with respect to $R$ (the usual case), $I_{L}$ is small with respect to the maximum current with which the buffer capacitor can be charged. This means that the capacitor can be charged to the peak value, $U_{\mathrm{p}}$, of the available voltage. The mean capacitor voltage is then

$$
\begin{equation*}
U_{C \mathrm{~m}}=U_{\mathrm{p}}-1 / 2 U_{\mathrm{r}} \tag{6}
\end{equation*}
$$

## Some additional mathematics



The buffer capacitor is charged via resistor $R$ for a period $-t_{L}$ to $+t_{L}$. The charge, $Q$, stored in the capacitor in that period depends on the average charging current, $I_{\mathrm{ch}}$ and the length of the period, $t=2 t_{\mathrm{ch}}$ :

$$
\begin{equation*}
Q=I_{\mathrm{ch}} t . \tag{11}
\end{equation*}
$$

The average current depends on the resistance, $R$, in the charging circuit and the average voltage, $U_{R}$, across that resistance:

$$
\begin{equation*}
Q=U_{R} 2 t_{\mathrm{ch}} / R \tag{12}
\end{equation*}
$$

So that

$$
\begin{align*}
U_{R}^{2} t_{\mathrm{ch}} & =2 U_{\mathrm{p}} \int_{0}^{t \mathrm{ch}} \cos (\omega t) \mathrm{d} t= \\
& =2 U_{\mathrm{p}} \sin \left(\omega t_{\mathrm{ch}}\right) \tag{13}
\end{align*}
$$

and

$$
\begin{equation*}
Q=\frac{2 U_{\mathrm{p}} \sin t_{\mathrm{ch}}}{\omega R}=\frac{2 I_{\mathrm{p}} \sin t_{\mathrm{ch}}}{\omega} \tag{14}
\end{equation*}
$$

where $I_{\mathrm{p}}$ is the peak value of the current that the supply can deliver for short periods, that is, $U_{\mathrm{p}} / R$.

To keep the mean value of the capacitor voltage constant, the charge removed from the capacitor must equal the input charge, that is,

$$
\begin{equation*}
I_{\mathrm{ch}} 2 t_{\mathrm{ch}}=I_{\mathrm{dis}} T_{\mathrm{r}}, \tag{15}
\end{equation*}
$$

where $I_{\text {dis }}$ is the discharge current and $T_{\mathrm{r}}$ is the period of the rectified voltage (as explained in the text, $T_{\mathrm{r}}=1 / f$ in half-wave
rectification and $=1 / 2 f$ in full-wave rectification).

Since the incoming and outgoing charges are equal,

$$
\begin{equation*}
\sin \left(\omega t_{\mathrm{ch}}\right)=\omega I_{\mathrm{dis}} T_{\mathrm{r}} / 2 I_{\mathrm{p}} \tag{16}
\end{equation*}
$$

so that,

$$
\begin{equation*}
t_{\mathrm{ch}}=\frac{1}{\omega} \arcsin \left(\frac{\omega I_{\text {dis }} T_{\mathrm{r}}}{2 I_{\mathrm{p}}}\right) \tag{17}
\end{equation*}
$$

Depending on the method of rectification, $\omega T_{\mathrm{r}}=\pi$ (full-wave rectification) or $\omega T_{\mathrm{r}}=2 \pi$ (half-wave rectification). If it is assumed that $I_{\mathrm{p}}$ is several times (or even many times) larger than $I_{\text {dis }}$, the following approximations are obtained:

$$
\begin{equation*}
t_{\mathrm{ch}}=\frac{\pi I_{\mathrm{ch}}}{2 \omega l_{\mathrm{p}}}=\frac{I_{\mathrm{ch}}}{4 f l_{\mathrm{p}}} \tag{18}
\end{equation*}
$$

or

$$
\begin{equation*}
t_{\mathrm{ch}}=\frac{2 \pi I_{\mathrm{ch}}}{2 \omega I_{\mathrm{p}}}=\frac{I_{\mathrm{ch}}}{2 f I_{\mathrm{p}}} \tag{19}
\end{equation*}
$$

where it is assumed that

$$
\arcsin (x) \approx x \text { if } x \leq 0.5
$$

The level of the ripple voltage, $U_{\mathrm{r}}$, is determined by the amount of charge removed during the period that the capacitor is not being charged. The length of that period is $T_{\mathrm{r}}-2 t_{\mathrm{ch}}$, so that

$$
\begin{equation*}
U_{\mathrm{r}}=Q / C=I_{\mathrm{dis}}\left(T_{\mathrm{r}}-2 t_{\mathrm{ch}}\right) / C . \tag{20}
\end{equation*}
$$

In a well-designed power supply, the capacitor is charged rapidly and $t_{\mathrm{ch}}$ « $T_{\mathrm{r}}$, so that a simplification may be made:

$$
\begin{equation*}
U_{\mathrm{r}}=I_{\mathrm{dis}} T_{\mathrm{r}} / C \tag{21}
\end{equation*}
$$

or

$$
\begin{equation*}
U_{\mathrm{r}}=I_{\text {dis }} / 2 f C \text { (full-wave rectification) } \tag{22}
\end{equation*}
$$

or
$U_{\mathrm{r}}=I_{\text {dis }} / f C$ (half-wave rectification).
[23]
and the minimum capacitor voltage is

$$
\begin{equation*}
U_{C \min }=U_{\mathrm{p}}-U_{\mathrm{r}} \tag{7}
\end{equation*}
$$

If $R_{L}$ is not much larger than $R$, the capacitor will not charge to $U_{\mathrm{p}}$ and [6] and [7] are no longer valid. However, $U_{C \mathrm{~m}}$ may then be calculated with the aid of Fig. 3.


The voltage source, which represents the transformer and rectifier, provides a direct voltage that is equal to the mean value of the non-smoothed direct e.m.f., $U$, supplied by the transformer and rectifier. The internal resistance of the source is represented by $R$. If a current $I$ is drawn from the circuit, that is, the circuit is loaded, the output voltage, $U_{C}$, will reduce by the voltage drop across $R$, that is

$$
\begin{equation*}
U_{C}=U-I R \tag{8}
\end{equation*}
$$

The level of $U$ is dependent on the method of rectification: with full-wave rectification it is equal to $2 U_{\mathrm{p}} / \pi$, and with half-wave rectification it is equal to $U_{\mathrm{p}} / \pi$.

The maximum current through the rectifier diode(s), $I_{\mathrm{d}(\mathrm{p})}$ is

$$
\begin{equation*}
I_{\mathrm{d}(\mathrm{p})}=U_{\mathrm{p}} / R \tag{9}
\end{equation*}
$$

This level of current flows normally only when the power supply is switched on, since the capacitor voltage is then zero. It can, however, also flow in conditions of very heavy (over-) loads when the minimum of the ripple voltage is zero. Normally, however, the capacitor voltage is appreciably higher and the current that then flows is equal to the maximum voltage drop across $R$ (roughly $U-U_{C}$ ) divided by $R$, that is

$$
\begin{equation*}
I_{\mathrm{d}}=\left(U-U_{\mathrm{C}}\right) / R \tag{10}
\end{equation*}
$$

The rectifier diodes must be able to cope continuously with this level of current, and should also be able to withstand, for short periods, the maximum current $I_{\mathrm{d}(\mathrm{p})}$.

The considerations in this article allow the practical design and calculation of the rectifier section of a power supply. The formulas given are not one hundred per cent accurate for all theoretical considerations; for instance, no account has been taken of the time constant, $\tau$, presented by resistance $R$ and buffer capacitor $C$.

# SCIENCE \& TECHNOLOGY 

# Augmented A-matrices: <br> a new circuit technique suitable for use with home computers 

by Michael Soper, MA


#### Abstract

Many articles have been written on the use of two-by-two matrices for the representation of two-port or four-terminal networks. Computer design now makes such techniques seem laborious when CAD facilities are available. But many designers still do not have access to such advanced facilities and need powerful techniques to help them analyse their proposed circuits. The advantage of the techniques outlined in this paper is that, unlike standard matrix techniques, they may represent forwardbiased diodes as well as linear active or passive circuits.


To describe the system, we start off with the standard circuit where a shunt impedance $Z$ has these equations:
and

$$
V_{1}=V_{2}
$$

$$
I_{1}=V_{2} / Z-I_{2}
$$

and is represented by the matrix

$$
\left[\begin{array}{ll}
1 & 0 \\
1 / Z & 1
\end{array}\right]
$$

The whole standard system is summarized as follows

$$
\left[\begin{array}{c}
V_{1} \\
I_{1}
\end{array}\right]=[A]\left[\begin{array}{c}
V_{2} \\
-I_{2}
\end{array}\right]
$$

represents this circuit


910058~11
where

$$
A=\left[\begin{array}{ll}
a_{11} & a_{12} \\
a_{21} & a_{22}
\end{array}\right]
$$

and the circuit equations are:

$$
\begin{aligned}
& V_{1}=a_{11} V_{2}-a_{12} I_{2} \\
& I_{1}=a_{21} V_{2}-a_{22} I_{2}
\end{aligned}
$$

The system in use here is a three-by-three matrix system which represents these equations:

$$
\begin{aligned}
& V_{1}=a_{11} V_{2}-a_{12} I_{2}-u .1 \\
& V_{2}=a_{12} V_{2}-a_{22} I_{2}-y .1
\end{aligned}
$$

$$
1=1
$$

The third equation is purely formal and thus the three-by-three matrix has this form:

$$
\left[\begin{array}{lll}
a_{11} & a_{12} & u \\
a_{12} & a_{22} & y \\
0 & 0 & 1
\end{array}\right]
$$

Another notation may be used for this:

$$
\left[\begin{array}{lll}
a & b & u \\
c & d & y \\
0 & 0 & 1
\end{array}\right]
$$

The vectors to use are:

$$
\left[\begin{array}{l}
V \\
I \\
1
\end{array}\right]
$$

This is the standard voltage/current vector used in transmission matrices augmented by the extra column:

$$
\left[\begin{array}{l}
u \\
y \\
1
\end{array}\right]
$$

All this will be explained more fully in the following.

A drawback of $A$-matrix technique is that although linear passive circuits can be rep-
resented adequately for design purposes by two-by-two matrices (called $A$-matrices), these are not adequate for the d.c. design of active circuits. This is because of the necessity of bias components which can not be calculated by what is essentially an incremental method. For example, there is unfortunately no matrix for a forward biased silicon diode.

This restriction has its origin in the mathematical fact that two-by-two matrices can not be used to move the origin to which the

$$
\left[\begin{array}{l}
V \\
I
\end{array}\right]
$$

vectors of the model are referred. This restriction may be removed by an artifice: replace

$$
\left[\begin{array}{l}
V \\
I
\end{array}\right] \text { by }\left[\begin{array}{l}
V \\
I \\
1
\end{array}\right]
$$

and use three-by-three matrices. These may be termed 'augmented' A-matrices and they have the form:

$$
\left[\begin{array}{lll}
a & b & u  \tag{1}\\
c & d & z \\
0 & 0 & 1
\end{array}\right]
$$

where $u, z$ are complex numbers as are, of course, $a, b, c, d$.

## Standard A-matrix technique

We will summarize the standard $A$-matrix technique and then show how the augmented matrices are an improvement.
$A$-matrix technique has its origin in the equations:

$$
\begin{equation*}
V_{1}=a V_{2}-b V_{2} \tag{2a}
\end{equation*}
$$

$$
\begin{equation*}
I_{1}=c V_{2}-d V_{2} \tag{2b}
\end{equation*}
$$


where $V_{1}, I_{1}$ are the input voltage and current, and $V_{2}, I_{2}$ are the output voltage and current. Equations [2a] and [2b] may be summarized neatly in matrix form:

$$
\left[\begin{array}{c}
V_{1}  \tag{3}\\
I_{1}
\end{array}\right]=[A]\left[\begin{array}{c}
V_{2} \\
-I_{2}
\end{array}\right]
$$

The simple series impedance, $Z$, and the parallel admittance, $Y$, have therefore the corresponding $A$-matrices:

$$
\left[\begin{array}{ll}
1 & Z  \tag{4}\\
0 & 1
\end{array}\right] \quad\left[\begin{array}{ll}
1 & 0 \\
Y & 1
\end{array}\right]
$$

A formulation like this is particularly suitable for use in computer programs, but it has a serious limitation: $V$ and $I$ are incremental, not absolute, as may be seen from the fact that a shunted current-source can not be represented by an A-matrix.


## New system

The liberation of the standard technique from this restriction is relatively easy, since the restriction has its root in the fact that two-by-two complex matrices can not be used to represent translations in the $(V, I)$ plane. The solution is to replace each vector

$$
\left[\begin{array}{l}
V \\
I
\end{array}\right] \quad \text { by }\left[\begin{array}{l}
V \\
I \\
1
\end{array}\right]
$$

and each matrix $A$ by:

$$
\left[\begin{array}{ll}
A & u  \tag{5}\\
& Z \\
0 & 0
\end{array}\right]
$$

To give an example: suppose the circuit is
in which the diode is forward biased and has zero forward impedance. The matrix for a silicon diode then summarizes the situation:

$$
\left[\begin{array}{lll}
1 & 0 & 0.7 \\
0 & +1 & 0 \\
0 & 0 & 1
\end{array}\right]
$$

and

$$
\begin{gather*}
V_{1}=V_{2}+0.7 \\
I_{1}=-I_{2}  \tag{6}\\
1=1
\end{gather*}
$$

## Current source

Let us now consider the matrix of a current source

$$
\left[\begin{array}{lll}
1 & 0 & 0  \tag{7}\\
0 & 1 & -i \\
0 & 0 & 1
\end{array}\right]
$$

which provides these equations:

$$
\begin{gathered}
V_{1}=V_{2} \\
I_{1}=-I_{2}-i .
\end{gathered}
$$

The source has infinite impedance and supplies a current $i$. These matrices may be multiplied just as the unaugmented matrices: the result represents two circuits in cascade. The advantage of this system is that it is absolute and can represent absolute levels of voltage and current.

To model a transistor, we must include the knee voltage of the emitter-base junction and an emitter-collector working voltage. A small-signal silicon n-p-n transistor with a 0.7 V e-b voltage in a common-emitter configuration might have a matrix

$$
\left[\begin{array}{lll}
-7 \times 10 \mathrm{E}-4 & -20 & 0.7 \\
-10 \mathrm{E}-6 & -0.24 & 10 \mathrm{E}-6 \\
0 & 0 & 1
\end{array}\right]
$$

When it is known what d.c. voltage offsets are required at input and output, the matrix may be computed as follows:
$M=\left[\begin{array}{lll}1 & 0 & V_{\text {knee }} \\ 0 & 1 & 0 \\ 0 & 0 & 1\end{array}\right]\left[\begin{array}{cc}A & 0 \\ & 0 \\ 0 & 0\end{array}\right]\left[\begin{array}{ccc}1 & 0 & -V_{\mathrm{w}} \\ 0 & 1 & 0 \\ 0 & 0 & 1\end{array}\right]$

If the matrix is to represent a transistor, and $A$ is the usual $A$-matrix for, say, a com-mon-emitter configuration, $A$ may be found from the $h$ parameters, where $h$ is the determinant of the hybrid matrix by choosing

$$
\begin{gathered}
a=-h / h_{21} \\
b=-h_{11} / h_{21} \\
c=-h_{22} / h_{21} \\
d=-1 / h_{21} .
\end{gathered}
$$

Empirical tests may be the best way to obtain optimum parameters for the augmented $A$-matrix.

A related question is: 'Given the augmented $A$-matrix of a transistor, how can the surrounding circuit values be designed?'

In a common-emitter configuration, the emitter resistor, the collector resistor, and the two base bias resistors are the minimum requirement.

This is best shown by an example as follows.

## Design procedure

In the design of a small-signal, single-stage n-p-n bipolar silicon transistor amplifier in a common-emitter configuration, let $A$ be the augmented matrix of the transistor. For convenience, we write the column vectors in rows.

1. Solve $A(Z, 0,1)^{T}=\left(V_{\mathrm{k}}, 0,1\right)^{T}$
for $V_{k}$, where $Z$ is adjusted for zero input current.

Then, let the supply voltage be $V$ and the transistor d.c. current, $I$.
$A\left[\begin{array}{lll}1 & R_{L} & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1\end{array}\right][V,-I, 1]^{T}=\left[0.7, I / \alpha h_{22}, 1\right]^{T}$

## 2. Solvefor $R_{\mathrm{L}}$.

3. Let $j$ be the current in the potential divider and $\mathrm{d} v$ half the peak-to-peak signal value; then:

$$
\begin{gathered}
{\left[\begin{array}{lll}
1+R_{2} / R_{1} & R_{2} & 0 \\
1 / R_{1} & 1 & 0 \\
0 & 0 & 1
\end{array}\right]} \\
{\left[0.7+\mathrm{d} v,-I / \alpha h_{22}, 1\right]=[V, j, 1]}
\end{gathered}
$$

Solve for $R_{2}$ and $R_{1}$.

## System use

The use of this system has been outlined in the foregoing; it allows, with care, circuits containing forward- or reverse-biased diodes and transistors, as well as passive components, to be easily designed.

## References.

"Matrix Algebra-2" by G.H. Olsen, Wireless World, April 1965.
"Useful matrix theorem with applications to electronic circuit theory" by M.C. Soper, Electronics Letters (IEE), 18 July 1985, Vol. 21 No. 15.
"Electromagnetism and Time" by M.C. Soper, Awareness, Vol. 12 No. 2, 1983-84.

Introductory circuit theory by Guillemin, Wiley 1953.
"Metalogic" by M.C. Soper, Awareness, Vol. 16, No. 3, 1989.

## CORRECTIONS

## Wattmeter

April 1991, p. 32-35
With reference the circuit diagram, Fig. 1, the right-hand terminal of the lower section of switch S2 should be connected to the circuit ground. This point is indicated by a dot.

In the adjustment procedure given on page 35 , the references to presets $\mathrm{P}_{4}$ and P 5 have been transposed. Contrary to what is stated, P4 sets the vY offset, and P5 the vx offset. The functions of the presets are shown correctly in the circuit diagram, Fig. 1.

To improve the accuracy of the instrument, connect R5 direct to the circuit ground instead of junction R6-R7. Finally, all circuit board tracks carrying mains current must be strengthened with $2.5-\mathrm{mm}^{2}$ cross-sectional area solid copper wire if currents higher than about 5 A are measured.

## 80C32/8052 Single-board computer

May 1991, p. 17-23
When a CPU type 8031 or 8052AH-BASIC is used, $\mathrm{IC}_{1}, \mathrm{IC}_{2}, \mathrm{IC}_{3}$, and $\mathrm{IC}_{8}-\mathrm{IC}_{12}$ must be 74 HCT types. Jumper B is erroneously reffered to as Br 2 in the text under "On-board EPROM programmer". Contrary to what is stated, this jumper must be fitted only when an EPROM is to be programmed - for all other use of the SBC, it must be removed. Also note that jumper B may only be fitted when the programming LED is out.

## Sequential control

July/August 1991, p. 61
Motor M should be a d.c. type, not an a.c. type as shown in the circuit diagram.

## Digital phase meter

June 1991, p. 32-39
In Fig. 5, the switch between input ' $A$ ' and IC 1 should be identified ' Sl ', and that between input 'B' and IC2 'S2'. Switch S4 is an on/off type, not a push-button as shown in the diagram. Capacitors C3 and C6 are shown with the wrong polarity. The component overlay of the relevant printed-circuit board (Fig. 8) is all right.

## Universal NiCd battery charger

## June 1991, p. 14-19

The parts list on page 19 should be corrected to read

$$
\mathrm{C} 7=2200 \mu \mathrm{~F} 25 \mathrm{~V}
$$

When difficult to obtain, the BYW29/100 (D5) may be replaced by the BY229, which is rated at 6 A .

The text under the heading 'Calibration'
should be replaced by:
4. Connect a multimeter between points G and H on the board, and adjust P 4 until the measured voltage is 1 V lower than the voltage on the battery terminals.

## MIDI program changer

April 1991, p. 14-17
The contents of the EPROM should be modified as follows:

| address | data |
| :--- | :--- |
| OOBC | E5 |
| 00 C 7 | 80 |
| 00 C 8 | CB |
| 00 C 9 | F 5 |
| 00 CA | 7 B |
| 00CB | 12 |
| 00 CC | 00 |
| 00 CD | D 2 |
| 00 CE | C 2 |
| 00 CF | 02 |
| 00 D 0 | 80 |
| 00 D 1 | C 2 |

Readers who have obtained the EPROM readyprogrammed through the Readers Services may return it to obtain an update.

## Electronic exposure timer

March 1991, p. 31-35
Please add to the parts list on page 32:
$\mathrm{C} 16=33 \mathrm{pF}$

## Augmented A-matrices

May 1991, p. 42-43
The drawing below was erroneously omitted in the left-hand bottom corner of page 43.


## APPLICATION NOTES

## The contents of this column are based on information received from manufacturers in the electrical and electronics industries and do not imply practical experience by Elekfor Electronics or its consultants.

## D.C.-TO-D.C. CONVERTER

(SGS-THOMSON MICROELECTRONICS)

DC-TO-DC converters are also known as switching regulators, which, in the opinion of many, is a more appropriate name. The converter described in this article is based on SGS-Thomson's new UCxx84x family of regulators.

The average output voltage of the converter is controlled by varying the pulse-width of a regulator, $\mathrm{IC}_{1}$ in Fig. 2.

The regulator described is a step-up type that converts a direct voltage input of $12-16 \mathrm{~V}$ to one of 18 V . The maximum output current is 3 A at 18 V . The efficiency is $73 \%$.

The new chips all operate according to the pulse-width control technique. In contrast to similar chips, for instance, those from National Semiconductor, the SGS-Thomson devices do not have the power transistor on board. Although this increases the number of external components required, it offers greater freedom in the design of the regulator circuit. The internal circuit of the regulator chip is shown in Fig. 1.

The various members of the UCxx 84 x family differ in ambient temperature range, the difference between on and off voltage, the accuracy of the internal reference voltage source and the maximum duty ratio. The housing is indicated by a single letter: J for ceramic mini-DIP; B and D for DIP-14 and SO-14 respectively. The circuit described here uses the consumer version UC3843N.

The principle of operation is that the countere.m.f. generated in inductor $L_{1}$ is added to the input voltage. When $T_{1}$ is switched on for a time $t_{1}$, the current through $\mathrm{L}_{1}$ rises and energy is stored in the inductor. When $\mathrm{T}_{1}$ is switched off for a time $t_{2}$, the energy stored in the inductor is transferred to the load via diode $\mathrm{D}_{1}$ and the inductor current drops.

When $\mathrm{T}_{1}$ is on, the voltage across $\mathrm{L}_{1}$ is

$$
\begin{equation*}
U_{L}=L(\mathrm{~d} / / \mathrm{d} t) \tag{1}
\end{equation*}
$$

and this gives the peak-to-peak ripple current in the inductor as

$$
\begin{equation*}
\Delta I=\left(U_{\mathrm{i}} / L\right) t_{1}, \tag{2}
\end{equation*}
$$

where $U_{\mathrm{i}}$ is the input voltage.
The instantaneous output voltage, $U_{\mathrm{o}}$, is

$$
\begin{align*}
U_{\mathrm{o}} & =U_{\mathrm{i}}+L\left(\Delta I / t_{2}\right) \\
& =U_{\mathrm{i}}\left(1+t_{1} / t_{2}\right) \\
& =U_{\mathrm{i}}(\Delta I /[1-k]) . \tag{3}
\end{align*}
$$



Fig. 1. Diagram of the internal circuit of the UCxx84x regulator.


Fig. 2. Circuit diagram of the step-up switching regulator controlled by the UCxx84x.
depends on the duty factor, $k$, that is, the ratio of the on and off times, $t_{1} / t_{2}$, of $\mathrm{T}_{1}$. The minimum output voltage occurs when $k=0$. However, $\mathrm{T}_{1}$ can not be switched on continuously such that $k=1$. For values of $k$ tending to unity, $U_{0}$ becomes large and very sensitive to changes in $k$.

## Circuit description

The circuit shown in Fig. 2 is based on regulator $\mathrm{IC}_{1}$. This device controls the on and off times of $\mathrm{T}_{1}$ and thus the on-off switching of the current through $\mathrm{L}_{1}$.

As explained earlier, the voltage across $\mathrm{C}_{5}$ depends on the ratio of the on and off times of $\mathrm{T}_{1}$. The regulator chip (pin 2: error amp) measures the output voltage with the aid of potential divider $\mathrm{P}_{1}-\mathrm{R}_{2}-\mathrm{R}_{5}$ and compares
the part of it that exists across $\mathrm{R}_{5}$ with the internal 2.5 V reference voltage. On the basis of this, it adjusts the duty factor of the pulse at its output (pin 6), which switches $\mathrm{T}_{1}$, in a manner that ensures the required level of output voltage.

The pulse rate is constant and kept at about 50 kHz by the oscillator on board the UC3843N. The duty factor may vary from $0 \%$ to $50 \%$ ( $\mathrm{x} 844 / 5$ ) or from $0 \%$ to $100 \%$ (x842/3).

A peculiarity of the regulator chip is the way the current in the transistor circuit is measured: this is done indirectly by the voltage drop across source resistor $\mathrm{R}_{9}$. This voltage is integrated by $\mathrm{R}_{7}-\mathrm{C}_{2}$ and then applied directly to the input of the current sense comparator on board $\mathrm{IC}_{1}$. This method improves the speed of control appreciably.


## Construction

If the converter is constructed on the PCB shown in Fig. 3 (not available through our Readers' services), no difficulties should be encountered. If the board is mounted on to the metal rear panel of an existing power unit, $\mathrm{T}_{1}$ normally does not require an additional heat sink. It must, however, be insulated with the aid of mica washers and heat conducting paste, since its metal base is NOT at earth potential.

Since $D_{1}$ can get pretty warm, it is advisable to mount it $2-3 \mathrm{~mm}$ above the board.

Inductor $\mathrm{L}_{1}$ consists of 19 turns 1.5 mm dia. enamelled copper wire on a Siemens Type R20/7 ring core. The turns should be distributed more or less evenly across the core, but this is not very critical.

The efficiency of the converter depends greatly on the quality of the components used. Therefore, a fast FET instead of a bipolar transistor is used for $\mathrm{T}_{1}$. Also, a fast diode is used for $\mathrm{D}_{1}$; the circuit would operate with a simple silicon diode, but the transit times would not be short enough.

The converter is calibrated by applying an input of $10-16 \mathrm{~V}$ provided by an accurate power supply and setting the output voltage to $16-20 \mathrm{~V}$ as required with $\mathrm{P}_{1}$.

## References

SGS Application: Industrial and Computer Peripheral ICs.

SGS Power Supply Application Manual.
"Switch-mode power supplies", Elektor Electronics, October 1987.

## COMPONENTS LIST

## Resistors:

R1 $=22 \Omega$
$R 2=62 \mathrm{k} \Omega$
$R 3=100 \mathrm{k} \Omega$
R4-R6 $=10 \mathrm{k} \Omega$
$R 7=1 \mathrm{k} \Omega$
$R 8=15 \mathrm{k} \Omega$
$\mathrm{R} 9=0.1 \Omega ; 5 \mathrm{~W}$
P1 $=10 \mathrm{k} \Omega$ preset

## Capacitors:

C1, C4 $=10 \mathrm{nF}$
C2, C3 $=1 \mathrm{nF}$
$\mathrm{C} 5, \mathrm{C} 6=1000 \mu \mathrm{~F} ; 35 \mathrm{~V}$; upright

## Semiconductors:

IC1 = UC3843N
11 = BUZ11
D1 = FR606 (Taiwan Semiconductors)

## Miscellaneous:

$\mathrm{L} 1=20 \mu \mathrm{H}$ (see text)
Ring core R20/7, K1 (Siemens)
Heat sink for T1 (SK09)
Enamelled copper wire 1.5 mm dia.

Fig. 3. Printed-circuit board for the d.c.-to-d.c. converter.


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Fig. 3. Printed-circuit board for the d.c.-to-d.c. converter.

# CONDUCTANCE METER 

from an idea by $J$. Vaessen


#### Abstract

Conductance, the inverse or reciprocal of resistance, is not a quantity that many of us measure daily: we normally deal with resistance. However, in some instances, for example, in liquids, it is easier to measure conductance than resistance.


GENERALLY speaking, the measurement T of conductance is not any harder than measuring resistance. In fact, in case of an analogue ohmmeter it is sufficient to state the inverse of the printed figure to convert the instrument to a conductance meter. However, most ohmmeters operate from a direct voltage or current. If that were used in a liquid, it would invariably give rise to some sort of electrolysis that would distort the measurement.

To counter the electrolysis, the meter must operate with analternating voltage or current of a sufficiently high frequency. The principle of such a meter is shown in Fig. 1a. Here, a rectangular-wavegenerator provides a voltage that alternates between 0 and a reference voltage, $U_{\text {ref. }}$. That potential is applied to one end of the unknown conductance, $G_{x}$; the other side is kept at $v_{2} u_{\text {ref. }}$. This means that the potential across $G_{x}$ is a rectangular voltage that swings between $\pm 1 / 2 U_{\text {ref }}$, which is a true alternating voltage. To determine the conductance, the potential across one of the resistors $R_{\text {ref }}$ needs to be measured.

The relationship between $G_{x}$ and the output voltage, $U_{\mathrm{o}}$, follows from Thevenin's Theorem and the Superposition Theorem. For convenience, in the following the direct voltage setting of $1 / 2 U_{\text {ref }}$ will be ignored. That being the case, Fig. 1b is the a.c. equivalent


Fig. 1. The principle of measurement is similar to that used in an ohmmeter.
of Fig. 1a. From this,

$$
U_{o}=\frac{1}{2} U_{r e f} \frac{\frac{1}{2} R_{r e f}}{\frac{1}{G_{x}}+\frac{1}{2} R_{r e f}}
$$

If we make the term $1 / 2 U_{\text {ref }}$ in the denominator much smaller than $1 / G_{x}$, the formula may be rewritten as

$$
U_{\mathrm{o}}=1 / 4{ }_{4} U_{\text {ref }} R_{\text {ref }} G_{\mathrm{x}} .
$$

However, this has advantages as well as drawbacks. The advantages are that the meter will have a linear scale and that $R_{\text {ref }}$ will be
small in spite of the fact that conductancemeasurements are normally used in case of high impedances. After all, $R_{\text {ref }}$ would be impractically high for some meter ranges. It is also possible to draw a new scale for the meter, which allows for the assumption. The drawbacks are that the assumption causes some degradation of accuracy and that in this method of measurement the greatest accuracy is obtained when $1 / G_{\mathrm{x}}=R_{\text {ref. }}$.

## The circuit

The circuit diagram of the conductance meter is given in Fig. 2.

The rectangular-wave oscillator is based


Fig. 2. Circuit diagram of the conductance meter.
on the well-known Type 555 ( $\mathrm{IC}_{1}$ ). Its frequency is 10 kHz , which is high enough to prevent electrolysis in a liquid. The output of the oscillator is applied to the measuring circuit as indicated in Fig. $1\left(G_{x}, R_{3}, R_{4}\right)$.

The output of the measuring circuit is buffered by opamp $\mathrm{IC}_{2 \mathrm{a}}$ and amplified about $\times 10$. This figure comes about because both $\mathrm{R}_{3}$ and $\mathrm{R}_{4}$ must have a value of $0.2 / G_{\max }$, where $G_{\max }$ is the value of the conductance at full-scale deflection-f.s.d.

The amplifier is followed by a high-quality rectifier circuit based on $\mathrm{IC}_{2 \mathrm{~b}}$. Buffer capacitor $C_{3}$ is charged via $D_{3}$ regularly, fastand accurately to the peak value of the voltage at the non-inverting input of the opamp, while it discharges slowly via $\mathrm{R}_{8}$.

The potential across $C_{3}$ is applied to the non-inverting input of buffer $\mathrm{IC}_{3 \mathrm{a}}$, which drives the meter. Network $\mathrm{R}_{9}-\mathrm{P}_{1}$ serves to set the full-scale value of the meter. Potential divider $\mathrm{R}_{10}-\mathrm{R}_{11}-\mathrm{P}_{2}$ serves to zero the meter.

The circuit is powered via voltage regulatr $\mathrm{IC}_{4}$. The regulator ensures that the supply voltage may be used to derive the reference potential.

A probe for measuring in liquids is made readily from a print header. Two pins of the
header-preferably gold-plated-formanexcellent probe with fixed distance between the electrodes. The link between the electrodes and the connecting wires should be made waterproof with the aid of two-component epoxy resin or potting compound.

## Calibration

Depending on the application, the meter may be calibrated in two ways. If it is to be used for measuring the conductance of solids only, a high-value resistor may be used as the calibrating conductance. The meter is adjusted with $P_{1}$ and $P_{2}$ as described later.

If the meter is intended for measurements in liquids, the shape of the probe, that is, the distance between the two electrodes, plays a role. The measurand is expressed in $\mu \mathrm{S} \mathrm{cm}^{-1}$, that is, micro-siemens per centimetre. The'per centimetre' emphasizes that the distance between the electrodes is a factor.

To calibrate the meter including probe accurately, a calibrating liquid is required. A saturated calcium-sulphate (anhydrite- $\mathrm{CaSO}_{4}$ ) solution is eminently suitable for this purpose: at $20^{\circ} \mathrm{C}$, this has a conductance of $1976 \mu \mathrm{~S} \mathrm{~cm}^{-1}$. The solution is prepared by mix-
ing calcium-sulphate in distilled water until the liquid accepts no more of the $\mathrm{CaSO}_{4}$. Note, however, that calcium-sulphate is only slowly soluble in water.

By adding an identical volume of distilled water to the solution, the conductance will be halved. Doubling the volume again by adding distilled water will halve the conductance once more. While diluting the solution, make sure that it remains at $20^{\circ} \mathrm{C}$, because the conductance varies with temperature.

Start the calibration before the power is switched on by manually adjusting the mov-ing-coil meter to zero.

Next, switch on the power and let the instrument warm up for a few minutes, after which the microammeter is zeroed by adjusting $P_{2}$ as appropriate. There should be nothing connected to the measuring electrodes or terminals.

Then, connect the calibrating resistor or immerse the probe in to the calibrating liquid and adjust $\mathrm{P}_{1}$ till the microammeter indicates the correct value. Since this affects the setting of $\mathrm{P}_{2}$ slightly, the adjustments of the two potentiometers should be repeated a couple of times.

# The contents of this column are based solely on information supplied by the author and do not imply practical experience by Elektor Electronics 

## Versatile pulse-width modulator

by Dr U. Kunz

THE CIRCUIT shown here generates a pulse train in which the width of each individual pulse is determined by a control voltage. This property makes the circuit suitable for use as a multiplex-decoder in, for instance, a remote control system, but other applications are, of course, also possible.

If the input signals applied to $\mathrm{IC}_{1}$ originate in analogue sources, they can be transmitted in digital form over a two-wire system or via a wireless system. In other words, the circuit can also serve as an analogue-todigital converter with eight channels. Its use in that function is readily accomplished with the aid of a computer.

The constant-current source, based on $\mathrm{T}_{1}, \mathrm{~T}_{2}$ and associated components charges capacitor $\mathrm{C}_{1}$ linearly. When the rising potential at the non-inverting input (pin 3) of $\mathrm{IC}_{3}$ reaches the level of the voltage at the inverting input (pin 2), the output of the opamp becomes $+U_{\mathrm{b}}$.

The consequent leading edge at pin 12 of $\mathrm{IC}_{4}$ starts monoflop $\mathrm{IC}_{4 \mathrm{a}}$, and this results in the output going high. At the same time, $\mathrm{C}_{1}$ discharges via $\mathrm{IC}_{5 \mathrm{~b}}$ and $\mathrm{T}_{4}$.

When $\mathrm{IC}_{4 \mathrm{a}}$ toggles, binary counter $\mathrm{IC}_{2}$ advances one step. Since outputs Q1, Q2 and Q3 of the counter are connected to the digital inputs of multiplexer $\mathrm{IC}_{1}$, this IC applies a different voltage, which is presettable with $\mathrm{P}_{4}-\mathrm{P}_{4}{ }^{\prime}$, to the input of $\mathrm{IC}_{3}$.

Since $C_{1}$ discharges via $T_{4}$, the process just described repeats itself, but with a different input voltage. This ensures that the time lapsed before comparator $\mathrm{IC}_{3}$ toggles is different from that in the previous cycle. The setting of the potentiometers or, if none is used, the voltage level at the inputs of $\mathrm{IC}_{3}$ influences the width of the pulse at pin 10 of $\mathrm{IC}_{4}$. In other words, the input voltages are translated into pulse widths.

At the eighth cycle, pin Q4 of $\mathrm{IC}_{2}$ goes high and this starts monoflop $\mathrm{IC}_{4 \mathrm{~b}}$. The time constant of this stage is much longer than that of $\mathrm{IC}_{4 \mathrm{a}}$. The leading edge at pin 6 of $\mathrm{IC}_{4 \mathrm{~b}}$ is used to reset the counter. Gate $\mathrm{IC}_{5 \mathrm{a}}$ and $T_{3}$ prevent $C_{1}$ from charging until $\mathrm{IC}_{4 \mathrm{~b}}$ toggles. The long pulse so generated, which appears at the outputs of IC5c and $\mathrm{IC}_{5 \mathrm{~d}}$, may be used for time synchronization (for instance, to reset a counter) in the receiver unit. When $\mathrm{IC}_{4 \mathrm{~b}}$ toggles, the whole process

starts afresh.
The values of $\mathrm{C}_{1}, \mathrm{C}_{2}$ and $\mathrm{C}_{3}$, which determine the time constants of the pulse generation, must be chosen to fit the particular application.

## Applications

The circuit was designed as a multiplex encoder for a remote control system, in which potentiometers $\mathrm{P}_{4}-\mathrm{P}_{4}$ are the control joysticks. $\mathrm{P}_{5}-\mathrm{P}_{5}$ ' serve to restrict the control range of $\mathrm{P}_{4}{ }^{-}$ $\mathrm{P}_{4}{ }^{\prime}$. This is advantageous in applications
where great sensitivity of control is needed. Since the time constants for the various cycles can be set independently of one another, and the time lapses are controlled not only by potentiometers, but also by voltage sources, the field of applications is very wide.

The possibility of using the circuit as an A-to-D converter has already been mentioned. Other uses include a weather station, where the sensor output voltages for air pressure, temperature, wind speed, humidity, and so on, are applied to the inputs of $\mathrm{IC}_{1}$.

## WIDEBAND ACTIVE ROD ANTENNA


#### Abstract

The starting point for this design is the well-known 5/8-lambda whip antenna with base coil as used for mobile communications in the 2-m VHF band. Interestingly, this type of antenna is readily tuned to 6 -metres. Add a wideband low-noise preamplifier and you have a wideband rod antenna for a large frequency range ( 20 kHz to 150 MHz ).


Dipl.-Ing. Jo Becker, DJ8IL

Afamiliar sight on cars fitted with a VHF band mobile radio, the $5 / 8$ - $\lambda$ whip aerial offers a gain of 2 to 3 dB over the $1 / 4-\lambda$ rod, known as the Marconi antenna. The coil seen at the base of the $5 / 8-\lambda$ antenna serves to lengthen it electrically and match it to a $50-\Omega$ coax cable. Most $5 / 8-\lambda$ antennas for the $2-\mathrm{m}$ amateur radio band have a length of about 1.25 m , which is about $0.22 \lambda$ in the $6-\mathrm{m}$ band. The additional inductance formed by the base coil gives the antenna an electrical length of a little over $1 / 4 \lambda$, which allows ready connection to a $50-\Omega$ coax cable.

## Active antenna

Long established for maritime radio communications, the active antenna is gaining popularity with users of general coverage receivers ( 100 kHz to 30 MHz ). Compared with the familiar long wire, the active antenna is unobtrusive, small and simple to install (although its final location will have to be given some thought in view of interference). Where a 'full-size' vertical antenna for general coverage reception has a minimum size of about 6 m and a weight of more than 5 kg , the active version presented here weighs a modest 400 g and has a length of only 1.3 m .

In principle, an antenna for the frequency range below 20 MHz or so can be shortened

to about 1 m without degrading reception. This is so because the level of man-made and natural noise is then still higher than the noise level of the receiver. However, the problem with such a short antenna is that it has a relatively high radiation resistance. As a rule of thumb, short antennas for the SW frequency range have a capacitive base impedance, $C_{A}$, of about $10 \mathrm{pF} / \mathrm{m}$. This means that they must be fitted quite close to an amplifying impedance transformer with a $50-\Omega$
output for the coax cable to the receiver input. This assembly of a short rod and a wideband RF amplifier fitted at its base is called an active antenna. The amplifier is provided with its supply voltage via the coax cable and a simple $L-C$ decoupling network at the receiver input.

Transmit/receive operation in the $2-\mathrm{m}$ and $6-\mathrm{m}$ band is enabled by a relay that disconnects the amplifier and connects the antenna to the coax cable when transmitting.

Table 1. Main technical data

- Passive operation; transmitting or receiving:
- VSWR = 1.4-1.6 in $2-\mathrm{m}$ amateur radio band
- $V$ VWR = 1.2-1.7 in 6 -m amateur radio band
- Loss introduced by relay and switching circuit: 0.1 dB (2-m band)
- Permissible transmit power: >50 watt
- Active operation at $U_{\mathrm{b}}=11$ to 15 V ( 13.5 V typ.)
- Current consumption: 60 mA
- Field strength conversion constant $\mathrm{k}_{\mathrm{A}}=U_{0} / E=0.5 \mathrm{~m}$
- Ripple of $\mathrm{kA}: \pm 1 \mathrm{~dB}$ between 150 kHz and 65 MHz
- Noise level $P_{\mathrm{No}} / \Delta \mathrm{ff}=-155 \mathrm{dBm} / \mathrm{Hz} \pm 1.5 \mathrm{~dB}$ between 1 and 60 MHz $U_{\mathrm{NO}} / \sqrt{\Delta f} \equiv 4 \mathrm{nV} / \sqrt{\mathrm{Hz}}$
- Equivalent noise level: $8 \mathrm{nV} / \mathrm{m} \times 1 / \mathrm{JHz}$
- Large-signal behaviour: 2nd-order intercept point $\mathrm{IP}_{2}=48 \mathrm{dBm}$; 3rd-order intercept point $\mathrm{IP}_{3}=30 \mathrm{dBm}$


Fig. 1. Basic schematic and parameters of an active antenna.

The relay is controlled remotely from the receiver or transceiver.

As illustrated in Fig. 2, the active rod antenna supplies a virtually constant voltage relative to the field strength of signals in the range from VLF to VHF. It is precisely this characteristic that makes the active rod suited to relative field strength measurement. Fitted on a car roof, it allows the inband and out-of-band signal levels of SW stations to be monitored. The antenna is also suitable for mobile long-distance SW reception, provided you take the trouble to drive your car as far as possible from large cities, broadcast transmitter sites and industrial sites. At home, the antenna is best fitted to the metal protection parts of the roof (see the introductory photograph). An alternative location is the balcony railing.

Given its small size, the performance of the active antenna is quite impressive, as shown by the measurement data collected in Table 1.

## Background noise and background theory

The field strength conversion factor, $\mathrm{k}_{\mathrm{A}}$, of an antenna of effective length $l_{\mathrm{e}} \cong l / 2$ (for values of $l$ smaller than $\lambda / 8$ ) is determined with the aid of the basic circuit shown in Fig. 1. As an example, the factor is calculated at a frequency of 10 MHz and at the associated gain, G, measured as 1.91 (see Fig. 2):

$$
\begin{aligned}
\mathrm{k}_{\mathrm{A}} & =\frac{U_{o}}{E}=\frac{l}{2} \cdot \frac{C_{A}}{C_{A}+C_{i}} \cdot G \\
& =\frac{1.25 \mathrm{~m}}{2} \cdot 10^{-220}=0.5 \mathrm{~m}
\end{aligned}
$$

Next, the intermodulation-free drive margin of the amplifier, $P_{\max }$, and the dynamic range, $D R$, are calculated with the aid of the second-order and third-order intercept points, $\mathrm{IP}_{2}$ and $\mathrm{IP}_{3}$. The purpose of this calculation is merely to compare the performance of one active antenna with that of another. For the practical construction, it has no significance.

$$
P_{\max }=\frac{1}{3}\left(P_{\mathrm{N} 0}+2 \mathrm{IP}_{3}\right)
$$

[dBm]

$$
D R=P_{\max }-P_{\mathrm{N} 0}=\frac{2}{3}\left(\mathrm{IP}_{3}-P_{\mathrm{N} 0}\right) \quad[\mathrm{dBm}]
$$

All power levels in the above equations are entered in decibel-milliwatts ( dBm ) nor-
malized at $50 \Omega$ for RF; 0 dBm equals 1 mW . For SSB in a bandwidth of 2.5 kHz :
$P_{\text {No }}=-155 \mathrm{dBm}+34 \mathrm{~dB}=-121 \mathrm{dBm}$ hence $P_{\text {max }}=-20 \mathrm{dBm}$, and $D R=101 \mathrm{~dB}$

For CW in a bandwidth of 500 Hz :
$P_{\text {No }}=-155 \mathrm{dBm}+27 \mathrm{~dB}=-128 \mathrm{dBm}$
hence $P_{\text {max }}=-23 \mathrm{dBm}$, and $D R=105 \mathrm{~dB}$

To many of you, voltage levels may be more familiar than the above dBm values. Assuming an antenna impedance of $50 \Omega$, and remembering that

$$
\begin{equation*}
U=\sqrt{P \cdot R} \tag{V}
\end{equation*}
$$

the resultant figures may have more meaning. The result for SSB is a noise voltage, $U_{\mathrm{N} 0}$, of $0.21 \mu \mathrm{~V}$, a maximum antenna voltage, $U_{\text {max }}$, of 22 mV , and a maximum field strength, $E_{\max }$ of $44 \mathrm{mV} / \mathrm{m}$.

For CW we obtain the following values: $U_{\mathrm{N} 0}=0.09 \mu \mathrm{~V}, U_{\max }=16 \mathrm{mV}$, and $E_{\max }=$ $32 \mathrm{mV} / \mathrm{m}$.

In practice, when the field strength of a received station exceeds $E_{\text {max }}$, the intermodulation and interference signals produced by the amplifier will exceed its own noise. The effects of intermodulation cause a number of spurious signals which may be heard in the receiver if they are strong enough to top the level of the background noise produced by man-made, atmospheric and other natural sources.


Fig. 2. Frequency response of the active antenna. The rod was simulated by a capacitor of 15 pF and a resistor of $25 \Omega$.


The active antenna discussed here was tested with a Yeasu FT-757GXII SW transceiver. The noise produced by the active antenna was audible only above 10 MHz . The dynamic range of the receiver with the active antenna switched on is smaller than that of the receiver proper, while the dynamic range
of the receiver alone is greater than that of the preamplifier alone.

The achievable signal-to-noise ratio can only be improved by means of a directional antenna, which, as most radio amateurs know, have a size of at least $\lambda / 2$, and offer a relatively small bandwidth.

From Fig. 2 we could be lead to believe that the active antenna could be used up to nearly 200 MHz . However, when the electrical length of the rod is $\lambda / 4$ or greater, the antenna starts to form a low impedance. This means that the preamplifier (which is essentially an impedance converter) can be omitted, and the rod connected direct to the input of the VHF receiver. Consequently, the VHF receiver will produce a low noise voltage relative to its own noise level. For an impedance of $50 \Omega$, the equivalent input noise voltage of the amplifier is $1 \mathrm{nV} / \sqrt{ } \mathrm{Hz}$.

## Circuit concept

As to the wideband amplifier, if you are after low amplifier noise rather than a high dynamic range, consider the following alternatives:

- a single-stage VMOS-FET based amplifier utilizing, for instance, the VN0808M or the VN66AK from Siliconix;
- a two-stage amplifier with a source follower at the input and an emitter follower with strong feedback at the output.

The second alternative has certain advantages: the input capacitance $C_{i}$ is small; the


Fig. 3. Circuit diagram of the active antenna, consisting of a $5 / 8$-lambda whip with base coil, a wideband RFamplifier and a supply voltage coupling circuit. Relay Re1 is actuated in receive mode only when the amplifier is functional also. During transmit operation, the supply voltage to the amplifier is switched off, so that the whip antenna is connected direct to the transceiver.


Fig. 4. Double-sided printed circuit board for the wideband RF amplifier.
noise level $U_{N}$ is low; the current consumption is modest and, importantly, the amplifier has no adjustments.

The circuit shown in Fig. 3 is a source follower based on a Type J309 n-channel junction FET (T1) from Siliconix or National Semiconductor. This transistor offers a good large signal performance by virtue of the relatively high and constant drain current. To stabilize the drain current, the source resistor, R5, is not connected to ground but in parallel with the base-emitter junction of the output amplifier transistor, T 2 . This is a Type 2N5109 medium-power wideband transistor designed for use in CATV head-end stations. The transistor (manufactured by Motorola) is marked by low noise and excellent linearity. If you can not get hold of the 2N5109, you may use the 2N5943, 2SC1252 or 2SC1253 as a near equivalent.

The linearity of the output stage is ensured by a relatively high degree of feedback. The gain of the stage is set to about 1.9, allowing $\mathrm{k}_{\mathrm{A}}$ factors of between 0.2 and 0.5 to be achieved. The output impedance of the amplifier is $50 \Omega$ to allow conventional coax
to be used. The output signal is fed to the receiver via a diplexer consisting of R8, L3, C7 and the input impedance of the receiver.

The supply voltage arrives at the ampli-

COMPONENTS LIST

| Resistors: |  |  |
| :---: | :---: | :---: |
| 1 | $27 \Omega$ | R7 |
| 2 | 47 0.3W | R1, R8 |
| 1 | $82 \Omega$ | R5 |
| 1 | 120』 0.3W | R6 |
| 2 | $100 \mathrm{k} \Omega$ | R2,R4 |
| 1 | $2 \mathrm{M} \Omega 2$ | R3 |
| Capacitors: |  |  |
| 1 | 470 pF 3 kV ceramic | C1 |
| 1 | 5 nF feedthrough | C9 |
| 1 | 100 nF 10 V ceramic | C5 |
| 2 | 100 nF 35 V ceramic | C3,C4 |
| 1 | 470 nF ceramic | C7 |
| 1 | 470 nF 35 V tantalum | C2 |
| 1 | $4 \mu \mathrm{~F} 710 \mathrm{~V}$ tantalum | C6 |
| 1 | $10 \mu \mathrm{~F} 25 \mathrm{~V}$ tantalum | C8 |
| Semiconductors: |  |  |
| 2 | 1 N 4148 | D1,D2 |
| 1 | 18V 1.3W zener diode | D3 |
| 1 | J309 (Siliconix) | T1 |
| 1 | 2N5109 (Motorola)* | T2 |
| Miscellaneous: |  |  |
| 11 | 12 V relay with $2 \mathrm{c} / 0$ contacts (SDS ${ }^{* *}$ type DS2E-12V) |  |
|  | noble-gas surge arreste 145V@5,000A |  |
| * Cricklewood Electronics. |  |  |
| Farm • Milton Keynes MK11 2HF - Tel. (0908) 567725. |  |  |

fier and the transmit/receive relay via chokes L1 and L2. The chokes must be capable of withstanding the transmit power while not introducing significant losses or resonance at any frequency within the range covered by the active antenna.

Two small gas-filled surge arrester tubes are provided to protect the amplifier against voltage peaks caused by lightning and 'electrostatic rain'. In addition, two diodes, D1 and $D_{2}$, and a series resistor, $R_{1}$, protect the

## Table 2. Inductor winding data

L1: 22 turns of 0.2 mm dia. copper enamelled wire on a ferrite ring core of o.d./i.d. $=16 \mathrm{~mm} / 9.6 \mathrm{~mm} ; \mathrm{h}=6.3 \mathrm{~mm}$; type B64290-K45-X830 from Siemens. L2: 20 turns of 0.2 mm dia. copper enamelled wire on a ferrite ring core of o.d.fi.d. $=14 \mathrm{~mm} / 9 \mathrm{~mm} ; \mathrm{h}=5 \mathrm{~mm}$; type 43220209718 from Philips Components. Alternative type: FT50A-61 (Micrometals/Amidon).
L3: 21 turns of 0.2 mm dia. copper enamelled wire on a ferrite ring core of o.d. $\mathrm{fi} . \mathrm{d} .=16 \mathrm{~mm} / 9.6 \mathrm{~mm} ; \mathrm{h}=6.3 \mathrm{~mm}$; type B64290-K45-X830 from Siemens.

## Main electrical data of the ferrite cores:

L1, L3: material $\mathrm{N} 30, \mu_{i}=4,300 ; \mathrm{A}_{\mathrm{L}}=2.77 \mu \mathrm{H} . \mathrm{L} 1=1.3 \mathrm{mH} ; \mathrm{L} 3=1.2 \mathrm{mH}$.
L2: material 4C6; $\mu_{i}=120 ; A_{L}=53 n H ; L 2=21 \mu H$.
Siemens distributor in the UK is ElectroValue Limited - 28 St Judes Road Englefield Green • Egham • Surrey TW20 OHB. Telephone: (0784) 33603. Telex: 264475. Fax: (0784) 35216. Northern branch: 680 Burnage Lane • Manchester M19 1NA. Telephone: (061 432) 4945.


Fig. 5. Mechanical outline of the active antenna. The whip antenna is bolted to the top part of the base, P.
gate of the J309. The zener diode, D3, has three functions: first, it limits the maximum supply voltage; second, it prevents backe.m.f. from the relay coil; and third, it acts as a protection against polarity reversal of the supply voltage.

## Construction and earthing

Figure 4 shows the double-sided, not through-plated, printed circuit board for the amplifier. The component side is largely unetched to allow it to function as a ground plane. All component terminals that are connected to ground are soldered at both sides of the PCB. Note that all component terminals, whether grounded or not, must be kept as short as possible.

The construction of the board is largely apparent from the photograph of the prototype. Note the orientation of the tab on the case of T 2 . If you use a transistor with a terminal connected to the case (the near equivalents of the 2 N 5109 ), this terminal is soldered to ground.

The FET, T1, is fitted with its flat side facing $D_{2}, R_{2}$ and the relay. The centre terminal of the FET (source) is not indicated on the component overlay. The outer two terminals are the drain (near C3) and the gate (near $\mathrm{D}_{1}$ ).

The frequency response of the amplifier will be a little smoother than shown in Fig. 2 when toroid core $\mathrm{L}_{3}$ is allowed more space than in the 'cramped' prototype shown in the photograph. The supply/coax connection should be sealed to prevent rain or dew entering the coax cable or the amplifier enclosure. An N-type plug and socket may be used because they are waterproof. The disadvantage however is the relatively high

## Table 3. Mechanical parts

```
o.d. = outside diameter
i.d. = inside diameter
A: Metal washer o.d. Ii.d. \(=16 / 11 \mathrm{~mm} ; 4 \mathrm{~mm}\) thick.
B: 6.3 mm dia. jack socket.
E: chrome-plated aluminium support plate.
\(\mathrm{H}, \mathrm{J}\) : Isolating washer o.d./i.d. \(=12 / 4 \mathrm{~mm} ; 2 \mathrm{~mm}\) thick.
K: relay.
N : nylon screw \(\mathrm{M} 4 \times 15 \mathrm{~mm}\).
Q: stainless steel spring washer o.d. \(/ \mathrm{i} . \mathrm{d},=16 / 11 \mathrm{~mm} ; 0.2 \mathrm{~mm}\) thick.
\(\mathrm{S}: 6.3 \mathrm{~mm}\) dia. angled jack plug.
X: isolating washer o.d. \(\mathrm{i} . \mathrm{d} .=16 / 11 \mathrm{~mm} ; 2 \mathrm{~mm}\) thick.
W: water exhaust
G: diecast case \(111 \times 60 \times 27 \mathrm{~mm}\) (Eddystone Radio 27134P).
P: antenna base.
```

cost. The author used a cheaper alternative in the form of a jack socket and a mating plug. After $11 / 2$ years of continuous use on the roof no traces of corrosion could be detected inside the amplifier enclosure.

In the introductory photograph the antenna is seen attached to the zinc rim (of width $w$ ) on the edge of a flat roof. The antenna is secured to a $2-\mathrm{mm}$ thick U-shaped chrome-plated aluminium piece ( E ) that is clamped on to the metal rim of the roof. The size of the aluminium plate is $200(\mathrm{~L}) \times$ $(100+w+100 \mathrm{~mm})(W) \mathrm{mm}$. The zinc rim on the roof is connected to the lightning conductor system. It should be noted that there may exist a up to a few 100 mV of hum between the lightning conductor system (which is earthed) and the protective earth on the mains system, to which the RF equipment is connected. To prevent a stray current flow-
ing via the relay coil and $\mathrm{L}_{1}, \mathrm{~L}_{2}$ and $\mathrm{L}_{3}$ (as a result of the potential difference, which is essentially hum), the two earthing systems are capacitively coupled via C1 The value of $\mathrm{Cl}_{1}$ is 470 pF , which is much greater than $\mathrm{C}_{\mathrm{A}}$. The capacitor effectively prevents harmonics of the hum voltage occurring in the VLF range of the receiver. Finally, use insulating spacers between the PCB and the metal enclosure, as shown in Fig. 5. This is done to ensure that the two earth systems are not interconnected.

## Note:

This article was translated and edited by the staff of Elektor Electronics from an originally German version that appeared in the 2-1990 issue of CQ-DL magazine. We thank the editors of CQ-DL for their permission to reproduce Mr. Becker's article.


Fig. 4. Double-sided printed circuit board for the wideband RF amplifier.

fier and the transmit/receive relay via chokes L1 and L2. The chokes must be capable of withstanding the transmit power while not introducing significant losses or resonance at any frequency within the range covered by the active antenna.

## PREAMPLIFIER FOR MOVING-MAGNET PICK-UP

by T. Giffard


#### Abstract

The basic function of a pick-up element is to translate the motion of the stylus into an electrical signal. The most popular cartridges in use are the moving magnet (fixed coil and tiny magnet) and the moving coil (fixed magnet and tiny coil). In both designs the vibrations of the stylus cause fluctuations in a magnetic field. Last month we published a preamplifier for advocates of the moving coil design; this month we turn our attention to those who favour a moving magnet element.


MOVING magnet carrtridges have a relatively high output and require a load of some $47 \mathrm{k} \Omega$ in parallel with a specified capacitance, normally $200-500 \mathrm{pF}$, for optimum performance.

The output voltage of the cartridge increases with frequency as shown in Fig. 1 following the recording characteristic of LP records in accordance with the IEC recording standard. This is a 1976 adaptation of the well-known RIAA (Recording Industry Association of America) recording standard. The preamplifier is therefore required to have a playback characteristic as shown in Fig. 1 with de-emphasis time constants of 8 ms , $3180 \mu \mathrm{~s}, 318 \mu \mathrm{~s}$ and $75 \mu \mathrm{~s}$, corresponding to roll-off points of $20 \mathrm{~Hz}, 50 \mathrm{~Hz}, 500 \mathrm{~Hz}$ and 2120 Hz respectively. The output level is $0.8-2.0 \mathrm{mV} \mathrm{cm}^{-1} \mathrm{~s}^{-1}$ of groove modulation velocity, resulting in a mean output of some $3-10 \mathrm{mV}$ at 1 kHz .

The RIAA recording characteristics did not specify the 8 ms time constant which, particularly in the present preamplifier, is of importance since it attenuates all kinds of subsonic sound (at 2 Hz by as much as 20 dB compared with the RIAA characteristic). The use of the IEC rather than the RIAA characteristic means that theamplifier reproduces records cut according to the RIAA standard with a greater attenuation of any rumble, while thosecut in conformity with the IEC standard are reproduced correctly. This assumes, of course, that the components in the correction networks are close tolerance types.

## Circuit description

This is the first quality preamplifier designed around opamps that we have ever published. The opamps used have the lowest noise figure currently commercially available-more about this later.

The circuit diagram of the preamplifier is shown in Fig. 2; it will be discussed on the basis of the left-hand channel.

The signal from the pick-up element is applied to the non-inverting input of $\mathrm{IC}_{1}$. The input impedance is formed by the parallel network $\mathrm{R}_{1}-\mathrm{C}_{1}$. The correct value of these components is normally given by the manu-


Fig. 1. Recording (1) and playback (2) characteristics according to the 1976 IEC standard.


Fig. 2. Circuit diagram of the stereo preamplifier and associated power supply.
facturer of the cartridge, although that of the resistor is usually taken as $47 \mathrm{k} \Omega$. The value of the capacitor varies between 200 pF and 500 pF . Note that $\mathrm{C}_{1}$ is shunted by the capacitance of the cable, which is normally $100-200 \mathrm{pF}$ and this must, of course, be deducted from the capacitor value specified by the manufacturer. If no manufacturer specification is available, make $\mathrm{R}_{1}=47 \mathrm{k} \Omega$ and $\mathrm{C}_{1}=100 \mathrm{pF}$.

The feedback of low-noise opamp $\mathrm{IC}_{1}$ has been arranged to ensure that the opamp does not only provide an amplification of $\times 10$, but also the required correction of the low frequency part of the signal. The high-frequency part is corrected by $\mathrm{R}_{7}-\mathrm{R}_{8}-\mathrm{C}_{9}$. Apart from the 20 Hz roll-off point, that completes the frequency response requirement according to the IEC standard.

The output of $\mathrm{IC}_{1}$ is applied to $\mathrm{IC}_{2}$, whose characteristics are virtually identical with those of the well-known OP27. The amplification of the stage is $\times 6.5$.

Although $\mathrm{R}_{11}$ at first sight appears to have no function, it does, in fact, stabilize the opamp if the load is highly capacitive.

The 20 Hz filter is formed by the parallel combination of $\mathrm{C}_{10}$ and $\mathrm{C}_{11}$ and the input impedance of the power amplifier connected to $K_{2}$. The value of the capacitors may be calculated from $\mathrm{C}_{10}+\mathrm{C}_{11}=1 / 40 \pi \mathrm{R}_{\mathrm{i}}$, where $\mathrm{R}_{\mathrm{i}}$ is the input resistance ( $47 \mathrm{k} \Omega$ ). Theold RIAA characteristics may be retained by giving both $\mathrm{C}_{10}$ and $\mathrm{C}_{11}$ a value of 470 nF .

The power supply for the stereo preamplifier contains no fewer than six regulator stages. The transformer rating is about 4.5 VA .

Any spurious noise signals produced by the rectifier diodes are suppressed by capacitors shunting the diodes.

The $\pm 15 \mathrm{~V}$ output of regulators $\mathrm{IC}_{5}$ and $\mathrm{IC}_{6}$ is suitable for powering $\mathrm{IC}_{2}$ and $\mathrm{IC}_{4}$, but for the low-noise opamps it needs further smoothing in $\mathrm{T}_{1}-\mathrm{T}_{4}$. Strictly speaking, since these transistors are not saturated, they function not so much as regulators but more as filters. Their bases are driven via $R C$ networks with a very low cut-off point $(0.7 \mathrm{~Hz})$. This arrangement ensures effective suppression of any residual hum and other noise extant on the output voltage.


Fig. 3. Equivalent circuit of all noise sources associated with the preamplifier.



Fig. 4. Voltage noise and current noise as a function of frequency (Courtesy Linear Technology).

## Noise

Noise figures do not tell the whole story of the noise that an amplifier will produce. The level of noise is determined primarily by the input circuit(s). The equivalent circuit in Fig. 3 shows where the sources of noise are to be found. Sources $\mathrm{E}_{\mathrm{N}}, \mathrm{I}_{\mathrm{N} 1}$ and $\mathrm{I}_{\mathrm{N} 2}$ represent all possible causes of noise in the opamp. Sources $\mathrm{E}_{\mathrm{t} 1}$ and $\mathrm{E}_{\mathrm{t} 2}$ represent the thermal noise level of the source impedances ( $\mathrm{R}_{\mathrm{s} 1}$ and $\mathrm{R}_{\mathrm{s} 2}$ ) that are connected to the opamp. The noise level at $25^{\circ} \mathrm{C}$ is about $0.13 \sqrt{ } \mathrm{R}\left(\mathrm{nV} \sqrt{ } \mathrm{Hz}^{-1}\right)$ where R is expressed in $\Omega$. Although this noise is not under the direct control of the designer, it does have an effect on the amplifier. The extent of its effect can only be assessed once we know more about the noise caused by the opamp.

The noise voltage, $\mathrm{E}_{\mathrm{N}}$, and noise current, $\mathrm{I}_{\mathrm{N}}$, as function of frequency are shown in Fig. 4. In both, the characteristic may be divided into two: a flat part and a part where the amplituderises with decreasing frequency. This comes about because, basically, both voltage noise and current noise consist of two types of noise: white noise and $1 / f$ noise.

White noise is characterized by by its level being the same at all frequencies, whereas the level of $1 / f$ noise is inversely proportional to the frequency. The characteristic curve is therefore a descending line ( $1 / f$ component greater) that slowly becomes horizontal (white noise greater). The frequency at which the levels of the two components are equal is usually called the rolloff frequency.

The effects of these noise sources may be limited by three golden rules:

- Thesourceimpedance mustbekeptas low as possible to keep thermal noise low. This in turn will keep down the level of the noise voltage caused by noise currents $\mathrm{I}_{\mathrm{N} 1}$ and $\mathrm{I}_{\mathrm{N} 2}$ across the source impedances. Note, however, that with the LT1028 the effects of the noise current are already exceeded by those of the thermal noise when the source impedance is smaller than $20 \mathrm{k} \Omega$. Nevertheless, to ensure minimum noise in the LT1028, the source impedance must be less than $400 \Omega$ to ensure that both the noise current and the thermal noise may be ignored: only the noise voltage then still plays a role. In their data book, Linear Technology therefore state that the use of the LT1028 is sensible only when the source impedance $<400 \Omega$.
- The $1 / f$ rolloff frequency must be chosen as low as necessary (and possible). This ensures that the amplifier has a good signal-to-noise ratio at even low frequencies. It does not make sense to use a $1 / f$ rolloff frequency that lies beyond the bandwidth of the amplifier.
- Match the bandwidth of the amplifier to that of the signal. Noise that lies outside the bandwidth of the amplifier is amplified to a lesser degree than noise within it. In other words, the output of an amplifier with a correct bandwidth will contain less noise than that of an amplifier with too large a bandwidth.

With the LT1028 a big step has been taken


Fig. 5. The printed-circuit board for the preamplifier is available through our Readers' services.
towards a low-noise design, but the designer has little control over the source impedance. A moving-magnet cartridge usually has an impedance of $1-2 \mathrm{k} \Omega$ and that means that not the opamp but the pick-up element produces most noise. In other words, the amplifier is too good for a moving-magnet element.

There are, however, high-output movingcoil elements with an impedance of about 200 ת; when these are used, it is the noise voltage of the opamp that will determine the signal-to-noise ratio.

In the latter case, the $1 / f$ frequencyalso becomes important. For the LT1028 that lies at about 10 Hz . That is well below the 20 Hz rolloff frequency designed into the preamplifier: no problem here. In case of a mov-

## PARTS LIST

## Resistors:

All resistors are $1 \%$ metal film types unless otherwise stated
$\mathrm{R} 1, \mathrm{R} 12=47.5 \mathrm{k} \Omega$
$R 2, R 13=20 \mathrm{k} \Omega$
R3, R14 $=2 \mathrm{k} \Omega$
$R 4, R 15=200 \Omega$
$R 5, R 6, R 16, R 17=4.7 \mathrm{k} \Omega^{2}$
R7, R8, R18, R19 $=10 \mathrm{k} \Omega$
$\mathrm{R} 9, \mathrm{R} 20=1.54 \mathrm{k} \Omega$
R10, R21 $=274 \Omega$
R11, R22 $=22 \Omega^{2}$

## Capacitors:

C1, C14 $=100 \mathrm{pF}^{1}$
$\mathrm{C} 2, \mathrm{C} 15=150 \mathrm{nF}$ MKT (match)
С3, C6, C16, C19, C33, C37 =
$=47 \mu \mathrm{~F} ; 25 \mathrm{~V}$; radial
C4, C7, C17, C20, C27-C30, C32,
C34, C36, C38 = 47 nF , ceramic C5, C8, C12, C13, C18, C21, C25,
$\mathrm{C} 26=22 \mu \mathrm{~F} ; 25 \mathrm{~V}$; tantalum
C9, C22 $=15 \mathrm{nF} ; 1 \%$; polystyrene
C10, C23 $=100 \mathrm{nF} ;$ MKT
C11, C24 $=68 \mathrm{nF} ;$ MKT $^{1}$
$\mathrm{C} 31, \mathrm{C} 35=470 \mu \mathrm{~F} ; 40 \mathrm{~V}$; radial
Semiconductors:
D1-D4 = 1N4001
T1, T3 $=\mathrm{BC} 550 \mathrm{C}$
$\mathrm{T} 2, \mathrm{~T} 4=\mathrm{BC} 560 \mathrm{C}$
IC1, IC3 $=$ LT1028CN83
IC2, $\operatorname{IC} 4=$ LT1007CP3

## Miscellaneous:

K1-K4 = gold-plated phono sockets
Mains adapter or transformer, 4.5
VA, with $2 \times 15 \mathrm{~V}$ secondary
PCB Type 900111

[^0]ing-magnet element, the frequency at which the noise of the cartridge is exceeded by the $1 / f$ noise is lower still, so no problem here either.

The question is, however, what are we going to do with the bandwidth? After all, the correcing networks are affected by the bandwidth. To keep the bandwidth as narrow as consistent with the amplifier requirements, the entire IEC correction network should be incorporated in the feedback loop. Only then, no more noise than absolutely unavoidable will be amplified. There is, however, also the requirement of keeping the source impedances small. This means that the value of $\mathrm{R}_{4}\left(\mathrm{R}_{15}\right)$ must be kept low ( $200 \Omega$ in the prototype).

Since the consequent $40 \mu$ Fcapacitor would be very large (it has to be a film type, because an electrolytic one would not do),the 20 Hz high-pass filter can not be accommodated in the feedback loop.

Similarly, the 2122 Hz low-pass filter can not be included in the feedback loop, because an opamp that is used as a non-inverting amplifier has an amplification of not less than $\times 1$. The required attenuation of the highest frequencies can not, therefore, be achieved by the feedback loop.

## Construction

As always, a high-quality amplifier as described here should preferably be constructed on the printed-circuit board shown in Fig. 5. The most conspicuous aspect of this is the earth track that divides the left- and righthand channels.

It is also possible to separate the power supply from the the remainder of the board, at least as far as its part without transistors $\mathrm{T}_{1}-\mathrm{T}_{4}$ is concerned. Those transistors are located as close as possible to $\mathrm{IC}_{1}$ and $\mathrm{IC}_{3}$ for reasons explained earlier.

This arrangement makes it possible for a range of a.c. input voltages to be used: the amplifier works readily from $\pm 7.5-20 \mathrm{~V}$. In all cases, it is essential to keep the mains transformer or adapter well away from the board.

If, for instance, the amplifier is built as a stand-alone unit (in a metal enclosure), it is advisable to house the transformer in its own (metal) enclosure away from the amplifier.

The connecting cables between the amplifier and the pick-up element must be as short as feasible. It is not a bad idea to build the amplifier within the record player.

Populating the board is fairly straightforward, although it requires absolute firstclass soldering. It is necessary to tin the earth track again before any other work is begun. The only components that require extra care are:
$\mathbf{R}_{1}, \mathbf{C}_{1}, \mathbf{R}_{12}, \mathrm{C}_{14}$, which ensure correct termination of the pick-up element. Their value is as indicated in the documentation of the element. Note that the cable capacitance must be deducted from the specified capacitance to arrive at the correct values for $\mathrm{C}_{1}$ and $\mathrm{C}_{14}$ If no data on terminating the element are available, use the values given in the parts list. $C_{2}, C_{15}$ should preferably have been $1 \%$ polystyrene types, but those are so large that the size of the PCB would have to be increased by almost $40 \%$. It was therefore decided to use MKT-metallized polyester (PEPT)-types. These must, however, be carefully selected to ensureaccuracy of the circuit. Apply soldering heat for a short time only, because the value of MKT capacitors changes when they are overheated.
$\mathrm{C}_{11}, \mathrm{C}_{10}, \mathrm{C}_{23}, \mathrm{C}_{24}$ form, together with the input impedance of the amplifier connected to K2 and K4, the 20 Hz high-pass filter. The correct value is calculated from

$$
\mathrm{C}_{10}+\mathrm{C}_{11}=\mathrm{C}_{23}+\mathrm{C}_{24}=1 / 40 \pi \mathrm{R}_{\mathrm{i}} .
$$

Note that the board allows the use of two capacitors in parallel.

It is important that the capacitors just discussed are of exactly the same value in the lefty- and right-hand channels. This means that two capacitors for the $C_{2}$ and $C_{15}$ positions that have the same value are preferred over two values that are not equal but are closer to 150 nF .

types of noise: white noise and $1 / f$ noise.
White noise is characterized by by its level being the same at all frequencies, whereas the level of $1 / f$ noise is inversely proportional to the frequency. The characteristic curve is therefore a descending line ( $1 / f$ component greater) that slowly becomes horizontal (white noise greater). The frequency at which the levels of the two components are equal is usually called the rolloff frequency.

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Fig. 5. The printed-circuit board for the preamplifier is available through our Readers' services.


[^0]:    1 See text
    2 carbon film type
    ${ }^{3}$ Linear Technology

