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Elektor Electronics

All-waveband ferrite rod antenna
Transistor characteristic plotting
Intro-scan for CD players
Image segmentation
Horn loudspeaker
A-D converter

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Elektor Electronics

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Front cover

Data relay satellites play a vital role in the space communications network, but they are so huge and complex that they are in danger of becoming unmanageable. The tiny detector unit shown in the photograph, designed by SIRA, a leading British research and development company, will play a vital role in a project aimed at reducing both size and complexity. Here, it is being aligned and calibrated after manufacture. The detector, developed in collaboration with British Aerospace, is part of a tracking sensor for a project known as SILEX, due to be launched by the European Space Agency in the early 1990s. The object of this is to develop optical inter-satellite communications links (ISL) that will in future be used to transfer data and commands between the data relay satellites and operational satellites in low orbit. ISLs will also be used to link pairs or groups of geo-stationary communications satellites.
Optical communications are more efficient than a conventional microwave beam, which means that satellites will not need to be so large and will be able to carry far smaller antennas than at present.
SIRA LTD, South Hill, Chislehurst BR7 5EH, England; telephone 081 467 2636.

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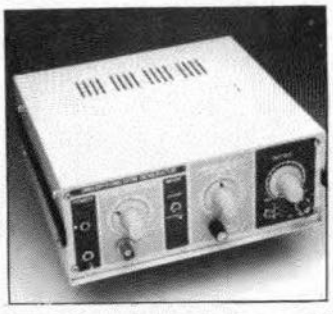

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THE MULTI-MAC CONCEPT

J. Buiting

ITT's Digit-2000 system has been designed to ensure ready integration of new TV and audio standards with existing hardware concepts. This means that a MAC decoder based on the Digit-2000 system is readily installed into an existing TV set as an upgrade. Provided the necessary control software is available, it is, of course, also possible to use the relevant chip set in a stand-alone application, which is of particular interest to the many thousands of viewers who own satellite-TV receiving equipment. This article introduces the main components that go into the making of such a C/D/D2-MAC compatible decoder.

Intermetall/ITT Semiconductors is among the world's largest producers of components for the consumer electronics market. Since 1985, the company has been involved in the development of MAC decoding systems, and it was the first semiconductor manufacturer to introduce a D2-MAC decoder chip, the DMA2270. The planned use of D-MAC on the BSB services, among other factors, prompted ITT Semiconductors to expand the DMA2270 with a multi-MAC decoding feature. The result is the C-, D- and D2-MAC compatible DMA2280, which, together with the DMA2285 MAC descrambler, forms the heart of the multi-MAC decoder for the Digit-2000 system.

An important point must be made at this stage. When we speak of a MAC decoder, we mean a circuit capable of extracting video and audio information from a signal to the MAC standard. As such, the function of the MAC decoder may be compared to that of, say, an FM decoder. Hence, the use of the word 'decoder' has in principle nothing to do with scrambling, and is really a misnomer. Just like PAL TV signals, or, for that matter, FM radio signals, MAC signals may be encrypted. Since that process has basically nothing to do with the standard of the transmission—only with the way in which the input signal is pre-processed—a separate unit, the MAC descrambler, may be used along with the MAC decoder. As already stated, the associated type numbers in this context are DMA2285 and DMA2280 respectively. The use of the DMA2285 is optional. However, bearing in mind that all BSB channels are encrypted, a MAC descrambling chip like the DMA2285 is a must for all BSB receive units.

Digit-2000: ready for the future

The Digit-2000 concept is illustrated in Fig. 1. Signals travel from the left (signal sources) to the right (sound/picture re-

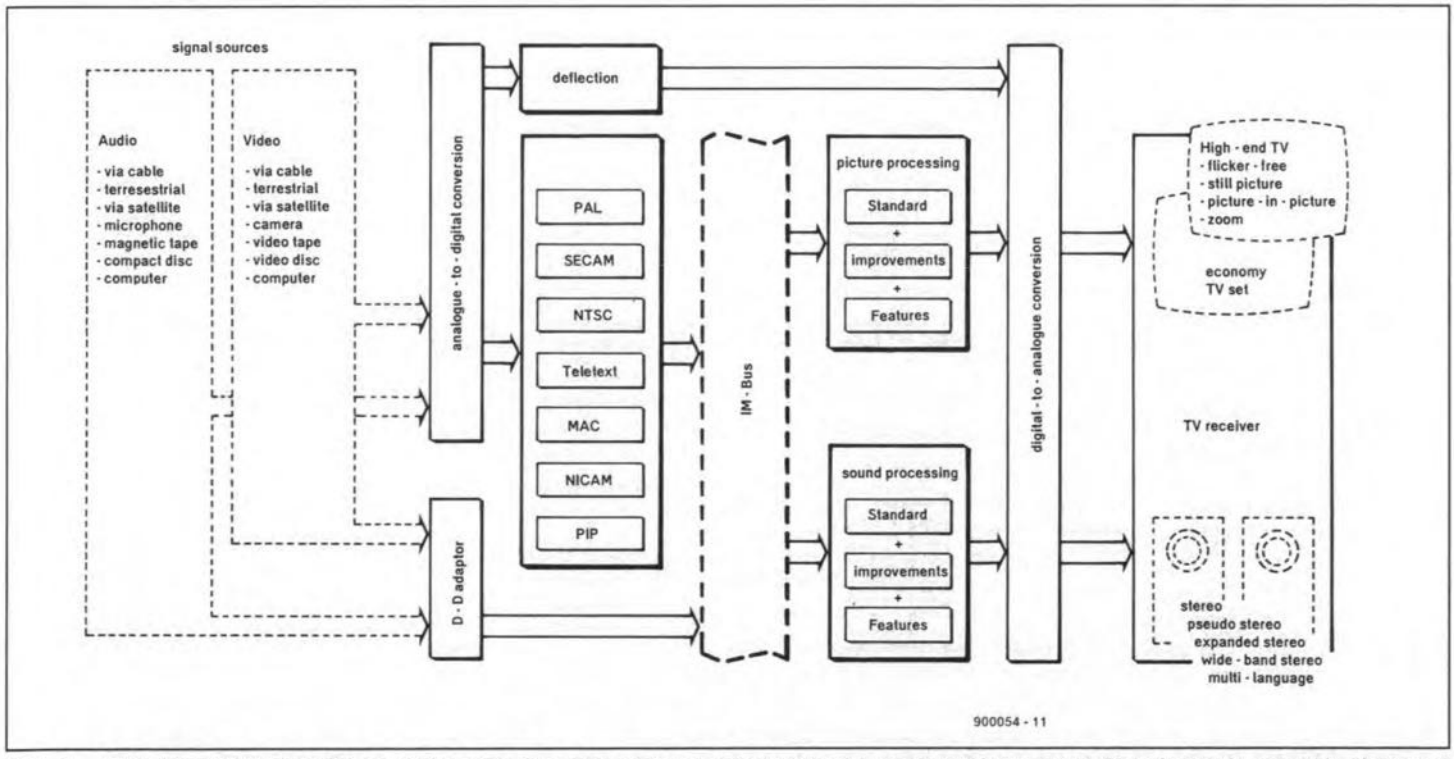

Fig. 1. ITT's Digit-2000 TV/radio system is geared to easy expansion by virtue of a command bus and all-digital signal processing between an ADC and a DAC.

production devices). The intermediate signal processing is entirely digital between an ADC and a DAC. Control signals for the system are conveyed via the IM bus, which is a simple 4-wire network that enables a central or external processor to communicate with the various devices (slaves) connected to the bus. The system is very flexible in that it allows new standards to be implemented readily. Take, for instance, the MAC extension: it is driven by the same ADC, is controlled by the same bus, and uses the same DAC as, say, the PAL circuitry. This means that the system allows both an economy and a top-quality TV set to be produced on the basis of three main building blocks: a fast ADC, a control bus, and a fast DAC. Extensions are always possible in this system: the appropriate unit (say, a NICAM processor) is simply connected in parallel with existing circuits and addressed via the IM bus.

MAC in a nutshell

The PAL, NTSC and SECAM colour TV systems currently in use are based on frequency division, which means that the two video components and the sound component are assigned a particular part of the transmitted spectrum. In this system, it is virtually impossible to ensure perfect separation of the luminance ('brightness') and chrominance ('colour') information. Inevitably, signals of both components will encroach upon each other's part of the frequency spectrum — see Fig. 2a. The effect is the well-known moiré patterning in picture areas with relatively fast luminance transitions. The colour processor in the TV receiver mistakes these fast luminance signals in the cross-colour area between about 2.3 MHz and 3.5 MHz (PAL) for colour information, and actuates colours which are not related to the luminance information in the particular picture area.

MAC relies on time division rather than frequency division and gives near-perfect separation of the picture components. Figures 2b and 2c shows how the luminance (Y) picture components in a PAL video signal may be transferred and compressed at a ratio of 3:2 into a time slot in the MAC signal (Ref. 1). The chrominance component (compression ratio: 3:1) is transferred in a similar manner to the time slot preceding the Y period. MAC lines alternately carry the compressed U (B–Y) and V (R–Y) colour difference signals. Note that both Y and U/V are analogue levels. Compression and expansion are required to fit these signals into the available line time, which is 64 µs just as with PAL.

Each line of MAC consists of serial U/V and Y signals, reference periods and a sound/data burst (packet). The latter is digital and duobinary-encoded (Ref. 2) to reduce the bandwidth of the FM signal produced for D- and D2-MAC transmissions via satellite. D-MAC differs from D2-MAC by its higher data rate in the sound/data burst: 20.25 MHz instead of 12.125 MHz (Fig. 2d), which allows a greater number of high-quality sound channels to be used at the expense of a slightly greater bandwidth.

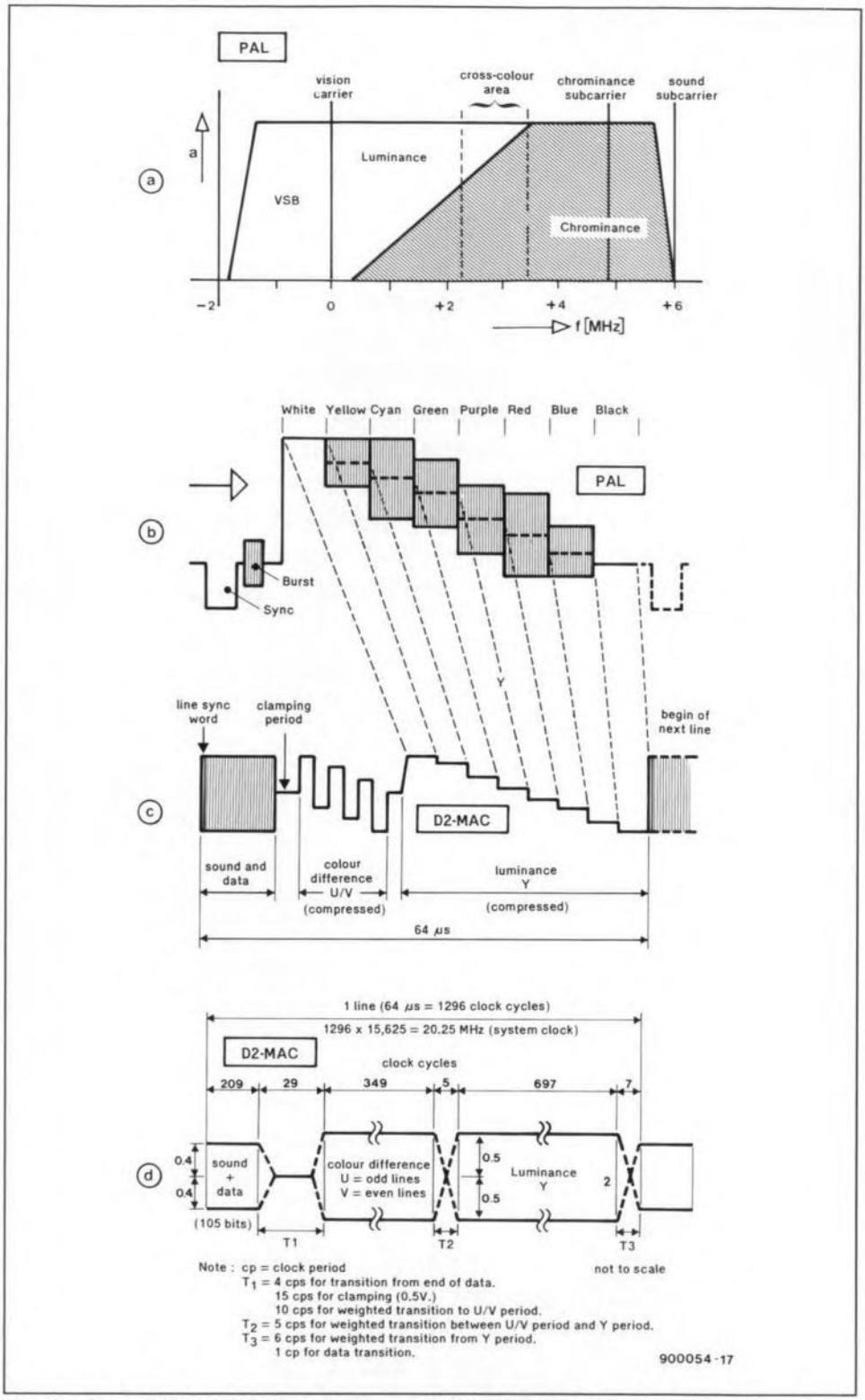

Fig. 2. From PAL to MAC: time-division multiplex of picture components and sound.

Clock generator MCU2600

After a necessarily brief recap on the background of MAC, the components that go into ITT's Multi-MAC concept will be discussed below with reference to block diagrams. Unfortunately, the scope of this article does not allow a full description of each device to be given; this may be found in the relevant datasheets.

Time multiplexing must rely on accurate clocking of various circuits in the MAC decoder. As shown in Fig. 2d, the system clock required for a MAC signal is determined by the number of samples within the line time of 64 µs, and the line frequency: 1,296/15,625 = 20.25 MHz.

The MCU2600 supplies the digital processors, decoders, converters, etc., that form part of the Digit-2000 TV system with the required main clock signal, which is of trapezoidal shape, with rounded corners, to avoid cross-talk and other interference. The MCU2600 may also be used for PAL, SECAM or NTSC: depending on the crystal used, the chip

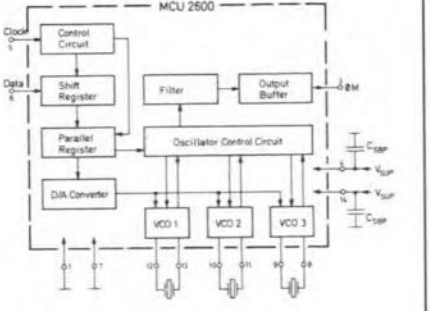

Fig. 3. Block diagram of the MCU2600.

supplies four times the chroma subcarrier frequency needed (PAL/SECAM: 17.734 MHz; NTSC: 14.318 MHz).

All three VCOs on board the MCU2600 may be selected individually, via the clock and data inputs, to form part of a PLL which is controlled by another chip, for instance, the DMA2280 MAC decoder. The PLL control (= error-) signal is applied in digital, serial, form to pin 6 of the MCU2600. The default VCO selection is VCO1.

Video coder/decoder (codec) VCU2133

The VCU2133 contains the ADC and the DAC mentioned above in the introduction of the Digit-2000 concept. The chip is provided with the baseband signal after de-emphasis to the MAC standard (which is not the same as the CCIR standard for PAL). As already noted, all digital signal processors in the Digit-2000 system are located between the ADC and the DAC in the VCU2133, which provides the following functions (see Fig. 4):

- two software-selectable input amplifiers
- one fast A-D converter for the composite video signal
- one noise inverter
- one D-A converter for the luminance signal
- two D-A converters for the colour difference signals
- one RGB matrix for converting the colour difference signals and the luminance signals into RGB signals
- three RGB output amplifiers
- programmable auxiliary circuits for blanking, brightness adjustment, white balance control and picture tube alignment
- additional clamped RGB inputs for text, teletext or other analogue RGB signals
- programmable beam current clamping

The VCU2133 may be used with a variety of video circuits, including the VPU2203 PAL processor, the CVPU2233 NTSC Comb Filter Video Processor, the SPU2220 SECAM Chroma Processor, the DPU2553 Deflection Processor and the DTI2223 Digital Transient Improvement Processor (note: DTI is sometimes referred as CTI: colour transient improvement). The chip contains a large number of registers that are loaded and read by the central processor in the Digit-2000 system via the IM bus.

The A-D converter that follows the two video input amplifiers and the selection switch is of the flash type, which means that it is a circuit that consists of 2^n comparators in parallel. For a slowly varying video signal, 8 bits are required. To achieve 8-bit picture resolution with a 7-bit converter, a special operation known as 'bit enlargement' is used. During every other line, the reference voltage of the A-D converter is changed by an amount corresponding to one half of the least-significant bit (LSB). In this manner, a grey value between two 7-bit steps is converted into the next lower value during one line, and into the next higher value during the next line. The two grey values are averaged by the viewer's eye, producing the impression of grey values with 8-bit resolution. Synchronously with the changing reference voltage of the ADC, a half-bit step is added to the output signal of the Y DAC every second line. The bit enlargement is switched off for D- and D2-MAC signals by appropriate control of the registers in the VCU2133.

The ADC's sampling frequency supplied by the MCU2600 is 17.7 MHz (PAL/SECAM), 14.3 MHz (NTSC) or 20.25 MHz (MAC). The converter's resolution is ½ LSB of 8 bits. Its output signal is Gray-coded to eliminate spikes and glitches resulting from different comparator speeds, or from imperfections in the coder itself.

After having been processed in other circuits, e.g., the DMA2280, the different parts of the digitized video signal are fed back to the VCU2133 for further processing to drive the RGB output amplifiers. The luminance (Y-) signal is routed from the contrast multiplier in the DMA2280 to the Y DAC in the VCU2133 in the form of a parallel 8-bit signal with a resolution of ½ LSB of 9 bits. This range provides enough headroom for large contrast vari-

ABBREVIATIONS

ADC	Analogue-to-Digital Converter
AGC	Automatic Gain Control
ALU	Arithmetic Logic Unit
BER	Bit-Error Rate
BSB	British Satellite Broadcasting
CCIR	Comité Consultatif International de Radio
CCU	Central Control Unit
CLIMB	Command Language for Intermetall Bus
DAC	Digital-to-Analogue Converter
FM	Frequency Modulation
HD-MAC	High-Definition MAC
MAC	Multiplexed Analogue Components
NICAM	Near-Instantaneous Companding Analogue Multiplex
NTSC	National Television Standards Committee
PAL	Phase Alternation Line
PC	Personal Computer
PDM	Pulse Duration Modulation
PLL	Phase-Locked Loop
QPSK	Quadrature Phase Shift Keying
RGB	Red-Green-Blue
ROM	Read-Only Memory
SECAM	Séquentiel Couleur à Mémoire
SEEPROM	Serial Electrically Erasable Programmable Read-Only Memory
VCO	Voltage-Controlled Oscillator

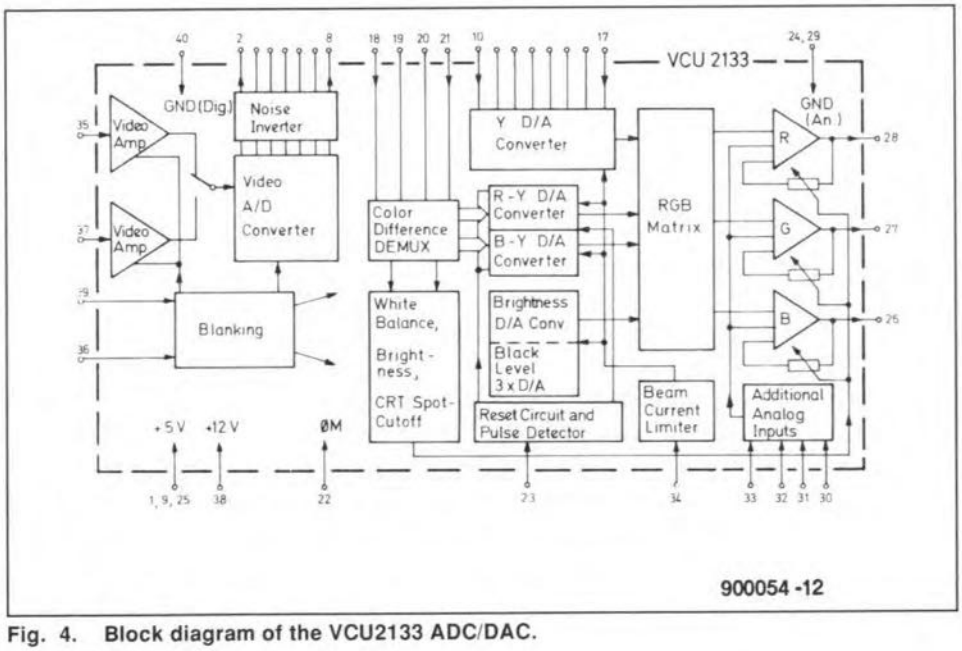

Fig. 4. Block diagram of the VCU2133 ADC/DAC.

ations as well as positive and negative overshoot. The Y DAC is an R-2R ladder network which is provided with the central clock frequency (20.25 MHz for MAC).

The two digital colour difference signals, R–Y and B–Y, are transferred in a time-multiplex arrangement to save on input pins. At a clock of 20.25 MHz and a chrominance bandwidth of between 1 MHz and 2 MHz, this can be done with impunity. Like the Y DAC, the two 8-bit DACs for R–Y and B–Y are implemented as R-2R ladder networks. Although they are clocked at one quarter of the central clock frequency, the multiplex data transfer rate is 20.25 MHz (for MAC). Sixteen (four times four) bits are transferred sequentially under the control of a sync signal that co-ordinates the multiplex operations between the VCU2133 and the video processor (in this case, a DMA2280).

C/D/D2-MAC decoder DMA2280

This chip forms the heart of the multistandard MAC decoder. Its tasks may be summarized as follows:

- to accept the digitized video (baseband) signal and extract from this the time-compressed chrominance and luminance information, and the sound/data packet
- to de-compress (expand) and correlate the luminance and chrominance information
- to extract audio, special data and sync words from the sound/data packet, taking account of the two different data rates (D2-MAC: 10.125 MHz; D-MAC: 20.25 MHz)
- to ensure a central clock of 20.25 MHz by providing a control voltage to the PLL in the MCU2600
- recognition of packet 0 for special purposes
- when required to provide error correction on weak input signals, and allow different slicing levels to be defined for the on-board duobinary decoder
- to provide an AGC signal for (digital) level control of the baseband input signal
- to communicate with the central IM bus processor

The DMA2280 is the multi-MAC version of the (older) DMA2270. Its block diagram is given in Fig. 5. The DMA2280 is a complex chip by almost any standard because it handles many relatively fast digital signals at the same time. It has on-board luminance and chrominance storage circuits which enable the relevant picture components to be de-compressed (expanded) and multiplexed (chrominance only) under the control of the central clock. Furthermore, it is capable of de-interleaving and linking the packets sent in each MAC TV line. A special word recognizer with error correction capabilities ensures the recognition of the field and line syncs, which are complex digital words contained in the sound/data packet. The DMA2280 has a capability for direct interfacing with any of the teletext processors in the Digit-2000 series, such as the TPU2733.

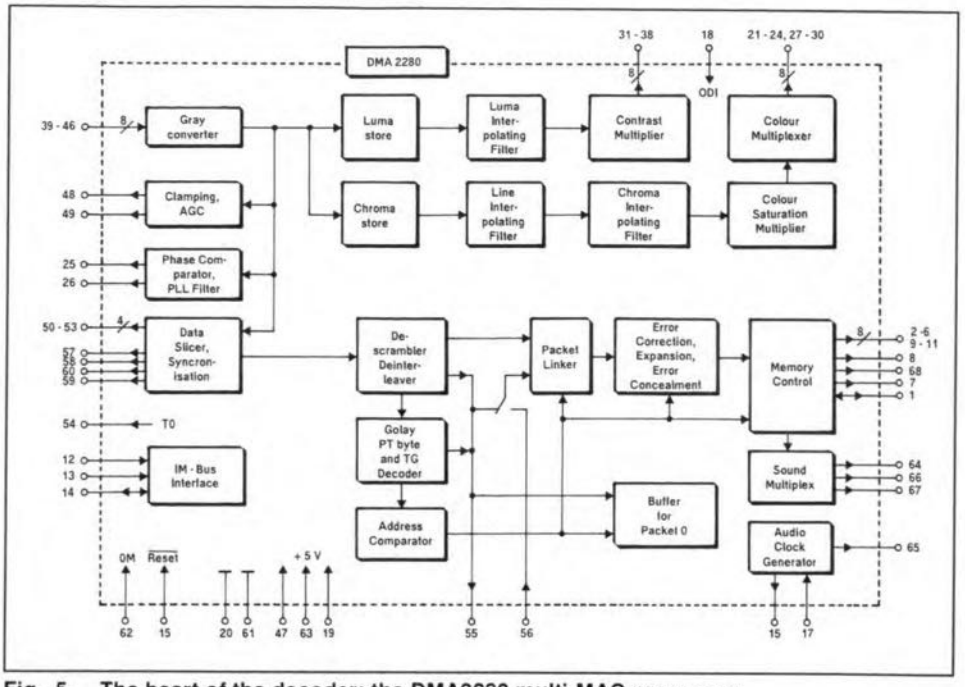

Fig. 5. The heart of the decoder: the DMA2280 multi-MAC processor.

The sound recovered from the data packets is fully decoded by the DMA2280 but left digital for demultiplexing and converting into analogue form by the AMU2485 audio processor.

All functions provided by the DMA2280 are controlled by registers, of which the content is determined by the chip itself (read-only) or the central processor. The bit-error rate (BER) register, for instance, contains a number that represents the sum of the error bits encountered in the 82 packet headers in one frame. This sum is stored in a register that can be read as bits 0–7 at address 206 by the central processor, which can take the necessary actions such as muting the audio signal when the BER parameter exceeds a certain predefined level. The DMA2280 occupies a total of 12 addresses on the IM bus. The bits reserved for these registers control a total of over 30 programmable functions, some of which may be used to select, in turn, up to four different modes of operation. The selection between C-, D- and D2-MAC is not automatic and must therefore be accomplished by the control software.

It should be noted that the DMA2280 requires a separate sound demodulator for C-MAC, since in that case the sound is provided in 2-4 QPSK rather than duobinary FM.

Audio mixer AMU2485

The AMU2485 (Fig. 6) receives the serial audio data supplied by the DMA2280 at its S-bus inputs. The S-bus is unidirectional and consists of three lines: S-clock, S-ident and S-data. The sound information is transmitted in frames of 64 bits, divided into four successive 16-bit sam-

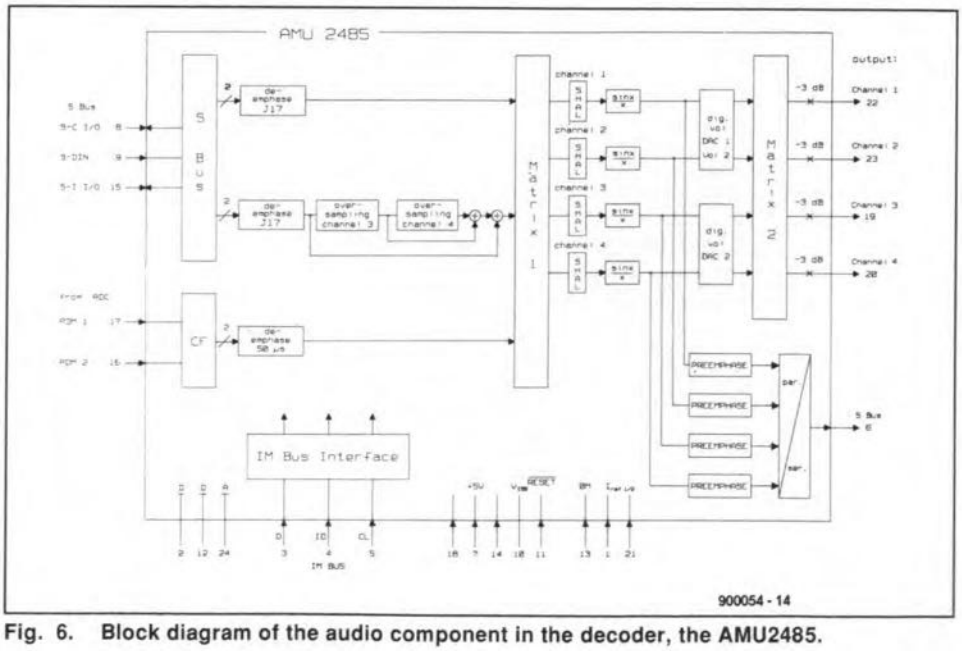

Fig. 6. Block diagram of the audio component in the decoder, the AMU2485.

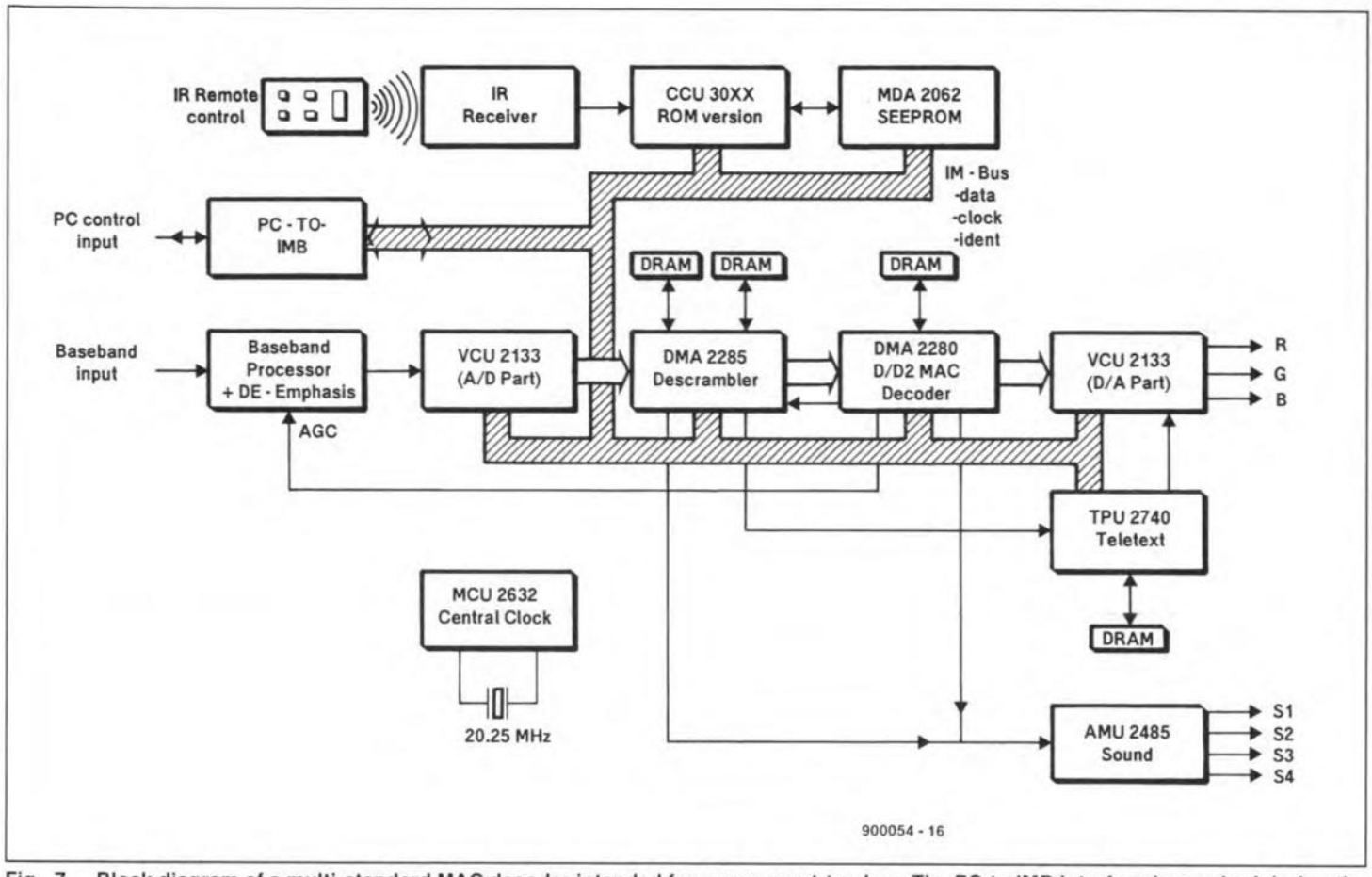

Fig. 7. Block diagram of a multi-standard MAC decoder intended for use as a set-top box. The PC-to-IMB interface is required during the development stages only.

ples. Each sample represents one audio channel. The repetition rate of the samples is equal to the sampling rate of the D- or D2-MAC signal so that up to four sound channels can be transferred simultaneously.

The AMU2485 provides a complete digital signal processor that runs its own control program from an on-chip mask-programmable ROM. Two de-emphasis filters are available: one to the CCIR J17 standard (used for MAC and NICAM transmissions) and one to the 50 µs standard (used for PDM sound broadcasts). Both de-emphasis circuits operate digitally and can be switched off if required by an appropriate register instruction.

The oversampling filters in S-bus channels 3 and 4 allow medium-quality D2-MAC sound signals (16 kHz sampling rate) to be mixed with high-quality signals (32 kHz sampling rate). The filters are third-order Cauer-type low-passes with a stop-band rejection of 40 dB.

The audio mixing feature of the AMU2485 allows any input to be routed to any output and, of course, to mix differently weighted input channels. The mixing and volume control operations on the DACs are entirely digital and run under the control of an internal ALU that receives the appropriate commands via the IM bus.

A multi-MAC decoder

The previously discussed chips all go into the making of the MAC decoder shown in Fig. 7. This concept packs all the signal processing required between the baseband output of the indoor unit and the RGB drivers in the colour monitor or TV set into a single set-top decoder.

The IM bus, which has not been discussed so far, is shown as a shaded path that links the sub-circuits into a small network. The bus consists of three lines: Signal Ident (ID), Clock (CL) and Data (D). The clock frequency range is 50 Hz to 170 kHz. Ident and clock are unidirectional from the CCU to the slave devices; data is bidirectional to allow the CCU to interrogate devices by loading and examining the contents of their registers.

The block diagram in Fig. 7 shows that the decoder can be controlled either by a PC via the PC-to-IMB interface, or by a CCU which uses a SEEPROM for storing and loading user settings such as the MAC standard (C, D, or D2), sound selection or contrast. The PC is required only during the development stages of the decoder; the software that runs on it, CLIMB, allows all registers in the chips that form the decoder to be examined and, if necessary, loaded or reloaded. CLIMB allows individual chips such as the VCU2133 to be programmed in great detail, with the aim of developing machine code for the CCU.

Once debugged and tested, the system control software is burned into a ROM on board the CCU. The CCU, which may be a 65xx or 80xx-like processor, has a direct input for digital data supplied by an infrared receiver.

As shown in the block diagram, the DMA2280 works in conjunction with the DMA2285 descrambler. In addition to its normal function as a low/high level MAC decryption processor, the DMA2285 allows 16:9 format HDMAC pictures to be converted to 4:3 format. Note, however, that this feature makes the decoder described only partly compatible of HD-MAC because of the present resolution of 625 lines. Fortunately, the next generation of MAC chips —which are now being developed — will be capable of meeting the full HD-MAC specification with 1,250 lines and thus deliver virtually flicker-free wide-format pictures. ■

Source:
Datasheets AMU2485; DMA2280; DMA2285; VCU2133; MCU2600/2632; DMA2270; CLIMB V2.1. **ITT Semiconductors.**

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References:
1. The MAC system. *Elektor Electronics* July/August 1987.
2. Introduction to duobinary encoding/decoding. *Elektor Electronics* January 1990.

HORN LOUDSPEAKER

T. Giffard

Horn loudspeakers for domestic hi-fi reproduction are generally large, cumbersome and expensive boxes that are built only by real enthusiasts. It is nevertheless highly satisfying to build them, particularly the one described here which, although producing excellent sound quality, is far less expensive than usual. Because of its high efficiency, it will produce more than enough sound pressure for most domestic purposes, even when it is driven by a low-power amplifier.

The horn loudspeaker is almost certainly the oldest type of loudspeaker, dating back to the days of Edison's wax cylinders. Then, they were the only devices to offer sound amplification, and ever since researchers like Webster, Wilson, Voigt and Klikpsch have applied their skills to the design of horn loudspeakers. Even with today's powerful amplifiers, they remain the only solution for filling large spaces with an adequate volume of sound.

In hi-fi installations, however, the horn has had to give way long ago to different types of loudspeaker construction, such as the bass reflex, the transmission line and the closed box.

Nevertheless, the domestic horn loudspeaker is not dead and for very good reasons: it has a very high efficiency, and consequently a large dynamic range, good impulse behaviour and low distortion. On the other hand, its design is usually highly complex, while the drive units it uses are generally (but not always) quite expensive. Moreover, it takes up a lot of space in the home.

Drive units	McFarlow Type T8-60
	McFarlow Type H25-90
Volume of box	about 100 litres
Efficiency	92 dB (1 W/1 m)
Power output	80 W continuous
	120 W music
Filter attenuation	6 dB/octave (woofer)
	12 dB/octave(tweeter)
Crossover frequency 3800 Hz	

Since it is very difficult to buy a horn speaker, the one described in this article has been designed specially for us by professional designers. The drive units and filter cost something like £60–£70 per box. The construction of the enclosure is, however, not recommended for beginners in woodworking.

The horn

A horn is basically an acoustic transformer. It transforms a small area diaphragm into an effective large area diaphragm without the disadvantages of increased mass, cone resonances, and so on. The radiation resistance of a large-area diaphragm is much greater than that of a small area one and thus more power is radiated for a given velocity of volume of air (sound velocity).

The basic requirements in the design of a horn are maximum acoustic power, wide frequency range, and low distortion. Once these have been determined, the drive units may be specified, after which the throat and mouth diameters and the form and length of the horn may be calculated.

Many horns are of the exponential type (others are conical or hyperbolic). The exponential behaviour of the horn ensures better coupling between drive unit and air and this increases the efficiency to almost 50%, which is an enormous improvement

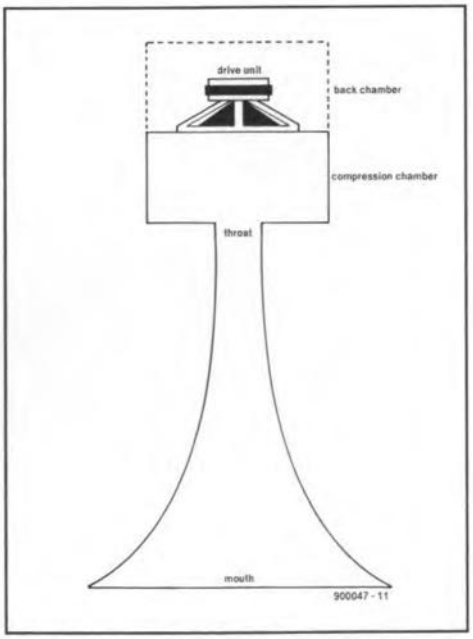


Fig. 1. Basic design of a horn loudspeaker.

Fig. 2. The McFarlow woofer and tweeter.

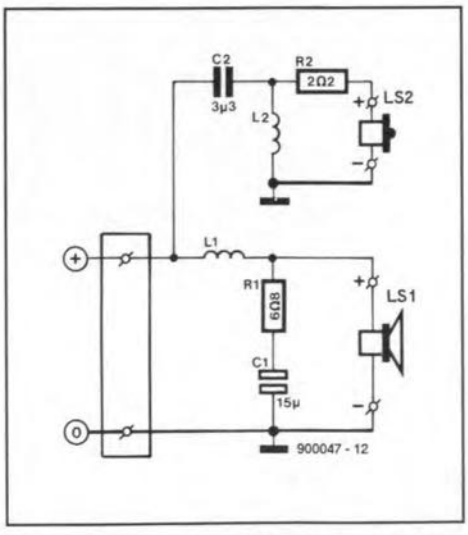


Fig. 3. Circuit diagram of the crossover filter.

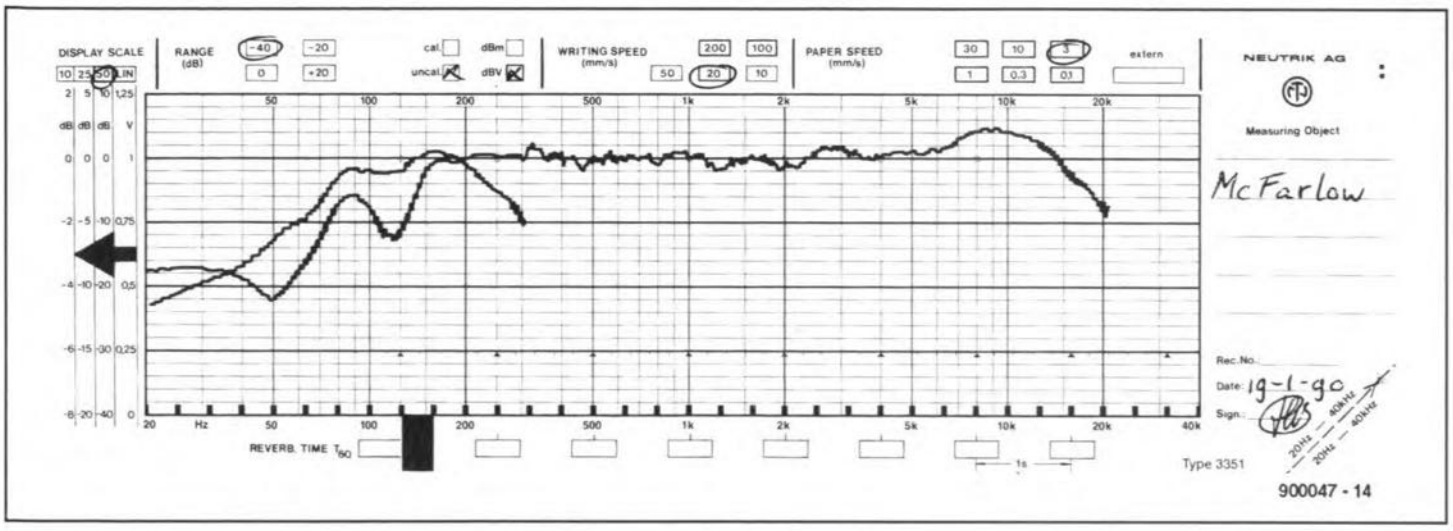


Fig. 4. Frequency characteristic of overall system.

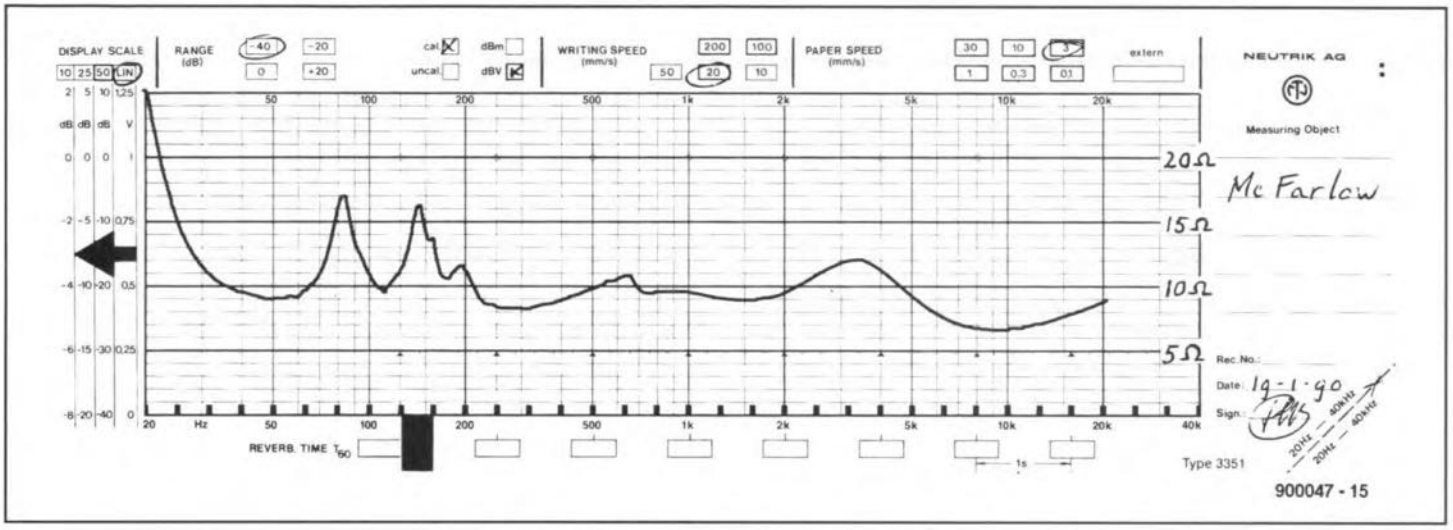


Fig. 5. Impedance characteristic of overall system

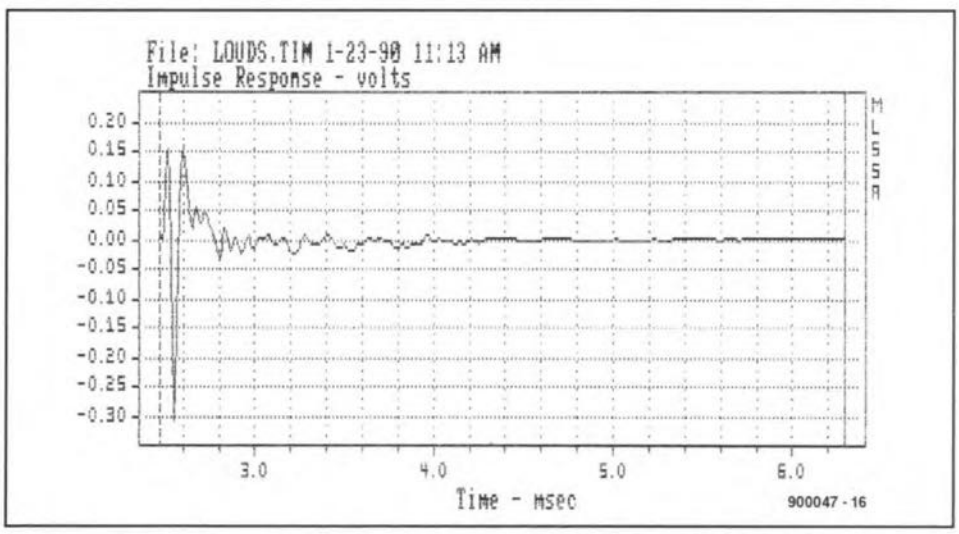


Fig. 6. The impulse behaviour of the overall system is typical of a horn design.

over the 1% of most other types.

The calculations of a horn design are not simple: every one of the many types has to be computed differently. We will not go into all of these, however, and will restrict ourselves to a general description of the operation of a typical horn system.

The modern horn speaker consists of a drive unit and matching horn as shown in Fig. 1. The drive unit is loaded by the volume of air in the compression chamber. Since the acoustic impedance is inversely proportional to the frequency, the compression chamber and the throat effectively form a low-pass filter.

The throat provides the coupling between the drive unit cum compression chamber and the horn. The area of the throat is important for optimum coupling.

The area of the mouth of the horn determines the low cut-off frequency. A good rule of thumb here is that the circumference of the mouth must be at least equal to the wavelength of the lowest frequency to be reproduced. Depending on how many surfaces the horn will be coupled to, the area of the mouth may be reduced by a factor 2 (floor), 4 (floor plus wall) or 8 (corner of room).

The length of the horn depends on a number of factors, particularly the ripple in the frequency curve that is acceptable. Since for good low-frequency reproduction the length is of the order of metres, the horn is normally folded a couple of times. Its total volume will then remain within acceptable limits for domestic use.

Often, the drive unit is also loaded at the back by a horn or closed box so as to ensure equal acoustic loading at both sides of the diaphragm. With back-loaded horns, as used in the present design, that is not possible, because these must then radiate the higher frequencies directly. Such

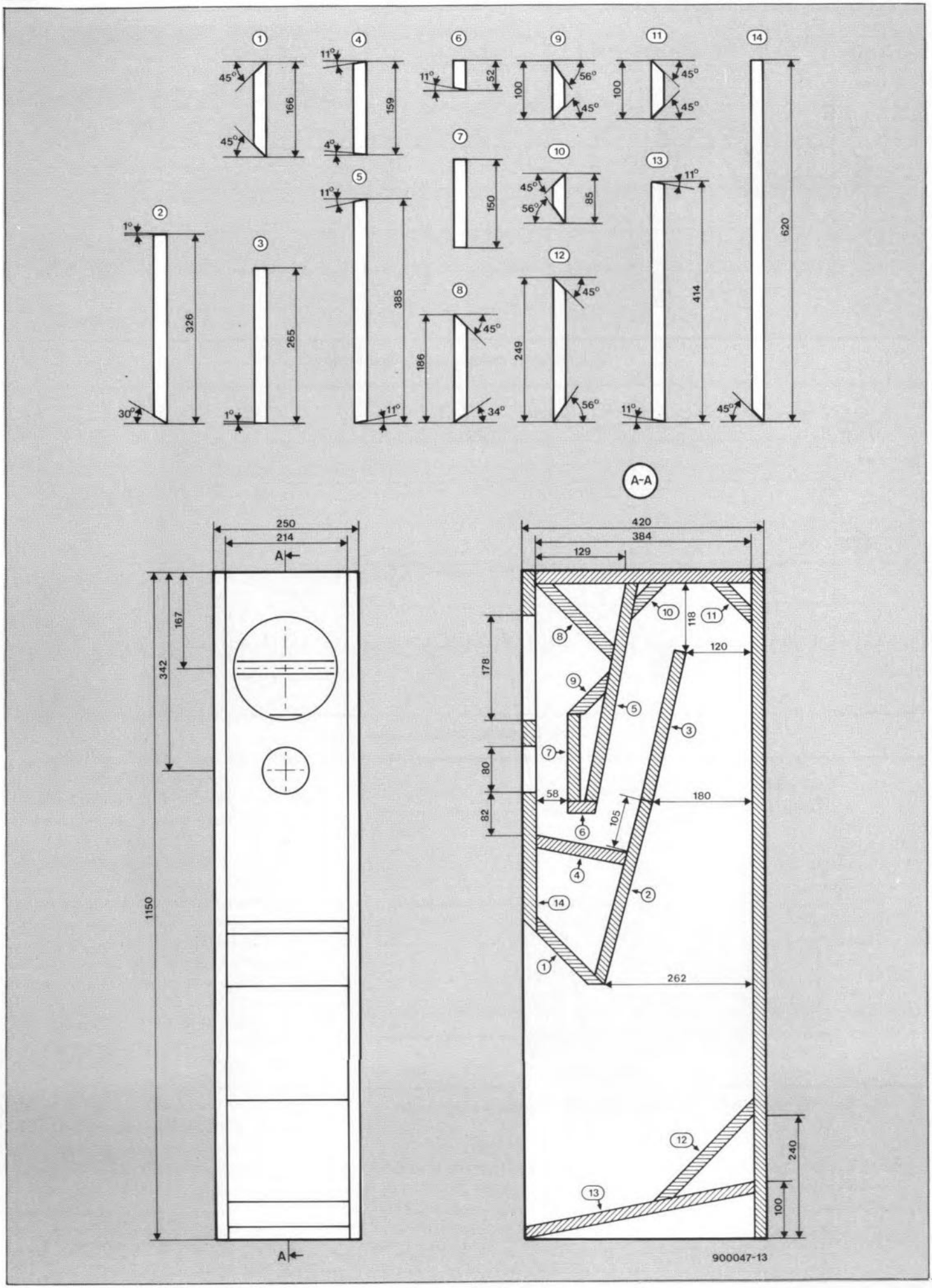


Fig. 7. Construction diagram of the horn enclosure.

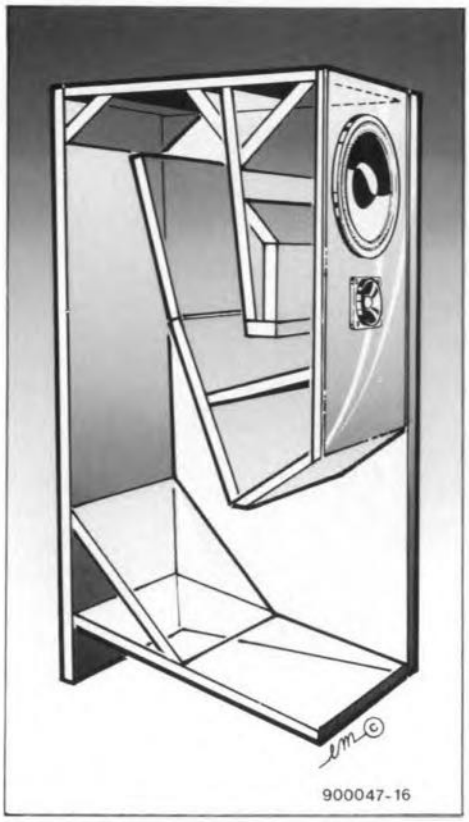


Fig. 8. Artist's impression of partially completed enclosure.

PARTS LIST (ONE ENCLOSURE)

Drive units	McFarlow T8-60 McFarlow H25-90
Filter	
L1	air-core inductor 05 mH wound from 1 mm dia. enamelled copper wire
L2	air-core inductor 0.25 mH wound from 0.71 mm dia. e.c.w.
C1	15 µF, 35 V, bipolar
C2	3µ3 MKT
R1	6Ω8, 5 W
R2	2Ω2, 5 W

18 mm chip board or plywood

rear panel	250×1132 mm
top plate	250×420 mm
front panel	250×602 mm
flank (2×)	420×1150 mm
panel 1	250×166 mm
panel 2	250×326 mm
panel 3	250×265 mm
panel 4	250×159 mm
panel 5	250×385 mm
panel 6	250×52 mm
panel 7	250×150 mm
panel 8	250×186 mm
panel 9	250×65 mm
panel 10	250×85 mm
panel 11	250×100 mm
panel 12	250×249 mm
panel 13	250×414 mm

Miscellaneous

Damping material as required (expanded polystyrene nuggets or rockwool)
glue and screws as required

horns, including the present, are therefore used to reproduce the low-frequency range only.

Design parameters

In the design of the present horn speaker system the most important requirement was that the mouth area should not exceed 0.125 m^2 so as to keep the dimensions of the enclosure within reasonable limits. The throat area and the low cut-off frequency, f_c, must also had to have reasonable values. The throat area is normally given a value between 0.3 A_d and 1.0 A_d, where A_d is the effective cone area of the bass drive unit. Since the throat area and the volume of the compression chamber determine the acoustic load, and thus the bandwidth, of the speaker system, we have chosen a ratio of 0.73 (according to the calculations of W. M. Leach).

It is often thought that in horn systems only drive units with a very low Q_{ts} (that is, with a very large magnet) may be used. This is, however, not always necessary: it depends on what bandwidth the system is required to reproduce. The bandwidth of a back-loaded horn as used in the present design is so small that a drive unit with a Q_{ts} of 0.35 is perfectly suitable.

The low cut-off frequency is that frequency at which the horn is no longer loaded, that is, produces no sound. In the present design it is set at 40 Hz. The real –3 dB point lies somewhere between f_c and the frequency determined by the mouth area. The ratio of these two frequencies must not be too large to avoid irregular behaviour of the radiation impedance between horn and room and a lumpy frequency characteristic.

The cross-sectional area, A_x, of an exponential horn at any distance x from the throat increases according to the following equation:

$$A_x = A_t e^{2mx}$$

where A_t is the throat area, e = 2.718 and m, the flare constant, = $2\pi f_c/c$, where c is the sound velocity (about 345 m/s).

Drive units and filter

In the choice of drive units it was important, since the larger part of the frequency range is radiated direct by the drivers, to find a combination that would match the efficiency of the horn,. The choice fell on the McFarlow Type T8-60 woofer and Type H25-90 tweeter (see Fig. 2).

The woofer is a 20 cm type with a normal pressed steel chassis and a coated paper cone. It has a reasonably sized magnet (dia. = 11 cm) and an efficiency of 92 dB (1 W/1 m). It is provided with a separate aluminium front bezel that gives it a very attractive appearance. Moreover, it costs only about £30 or so.

The tweeter has an even better efficiency than the woofer, which makes some attenuation in the filter necessary. The dome is made from a type of pressed foam and the speech coil is cooled by ferro fluid. Its price is very close to that of the woofer.

The crossover filter, whose circuit is shown in Fig. 3, has been kept fairly simple. The low-pass section has an attenuation of 6 dB/octave and the high-pass section one of 12 dB/octave. Because the crossover point is rather high (3800 Hz), some impedance correction proved necessary and this is provided by R1 and C1. Resistor R2 ensures correct level matching between woofer and tweeter. The filter is easily constructed on a piece of veroboard or even on a small piece of plywood.

Building the enclosure

Most of the work goes into the construction of the enclosure. You can, of course, have it made, but that may increase the cost of the system quite appreciably. The construction plan is shown in Fig. 7, while Fig. 8 gives an artist's impression of a partially completed box.

The enclosure is made of 18 mm chipboard or plywood; thicker board may be used but it will then be necessary (and not easy) to match the horn to the new dimensions. Wherever possible, angles have been kept to 45° or 90°. If possible, have the dealer you buy the board from saw it to size according to the wood list.

Start with gluing the rear panel, top plate, base plate, front panel and one of the side flanks together. Then, one by one, glue the inner wedges, inclines and tails in place. It is important to stick to the correct distances between all these panels. Any gaps where panels are glued together should be filled with a good-quality (silicone) wood filler.

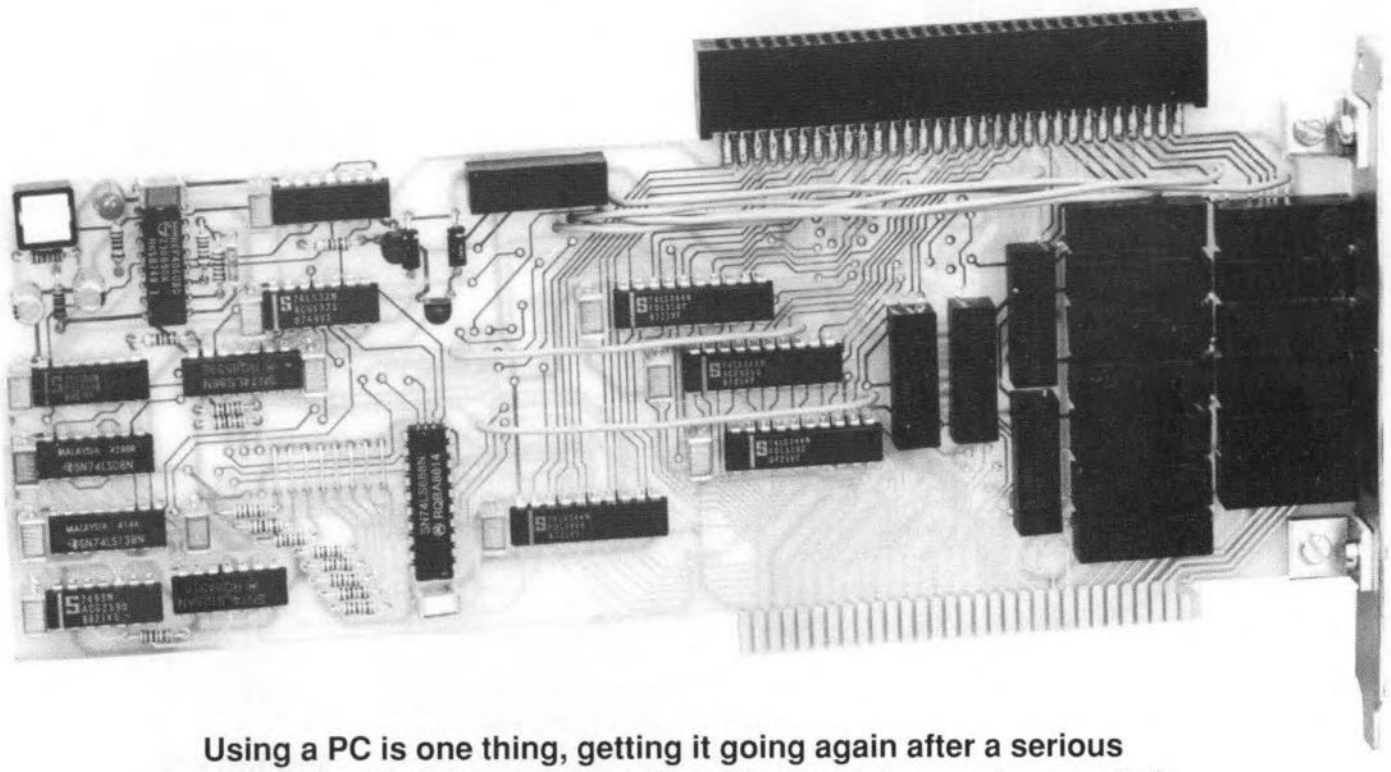
When the glue has set hard, drill holes for the connecting cables. At the same time, fit the crossover filter in the hollow base.

Next, fit the drive units securely in place , after which all the wiring should be completed.

Finally, fill the enclosure with suitable expanded polystyrene chips or rockwool and glue the second side flank in place.

The enclosure can then be finished externally to personal taste. ■

PC SERVICING CARD



Using a PC is one thing, getting it going again after a serious hardware malfunction quite another. The servicing card presented here, a design by ELV, is aimed at two groups of PC-XT/AT users: first, those bold enough to declare war on defective add-on boards, and second, those engaged in developing application-specific hardware. One remarkable feature of the servicing card is that it allows the card under test to be removed and inserted without the need of switching the computer on and off.

The most irritating thing about dealing with suspect or defective PC add-on cards is that they are difficult to get at for measurements with, say, an oscilloscope when they are seated in an expansion slot on the motherboard. The first and foremost requirement of a servicing card is, therefore, that it extends the bus physically, so that the card under examination is accessible from all sides without having to rebuild the inside of the computer.

A further well-known source of annoy-

BASIC TEST PROGRAM

```
100 REM
110 REM *** switch on servicing card ***
130 REM
130 D = INP (&H300)
140 REM
150 REM approx. 0.5 sec delay
160 FOR I = 1 TO 1000:NEXT I
170 REM
180 PRINT "TEST PROGRAM SHOULD END HERE"
190 REM
200 REM *** switch off servicing card ****
210 REM
220 OUT &H300, D
230 END
```

PASCAL TEST PROGRAM

```
PROGRAM service;

USES Crt; {for Turbo4.0}

CONST IOaddress = $0300; {change as r'qd}

VAR Dummy : Byte;

PROCEDURE switch_on;

Begin
  Dummy := Port [IOaddress];
End;

PROCEDURE switch_off;

Begin
  Port [IOaddress] := Dummy;
End

PROCEDURE test_program;
{test program for defective add-on board}

Begin
  Write    ('test program should');
  Writeln  ('end here');
End;

Begin { main program }
  switch_on;
  DELAY (500);
{wait for control to finish}
  test_program;
  switch_off;
End.
```

Table 1. Example BASIC and Pascal programs that enable the servicing card to be controlled by the PC rather than push-button Ta1.

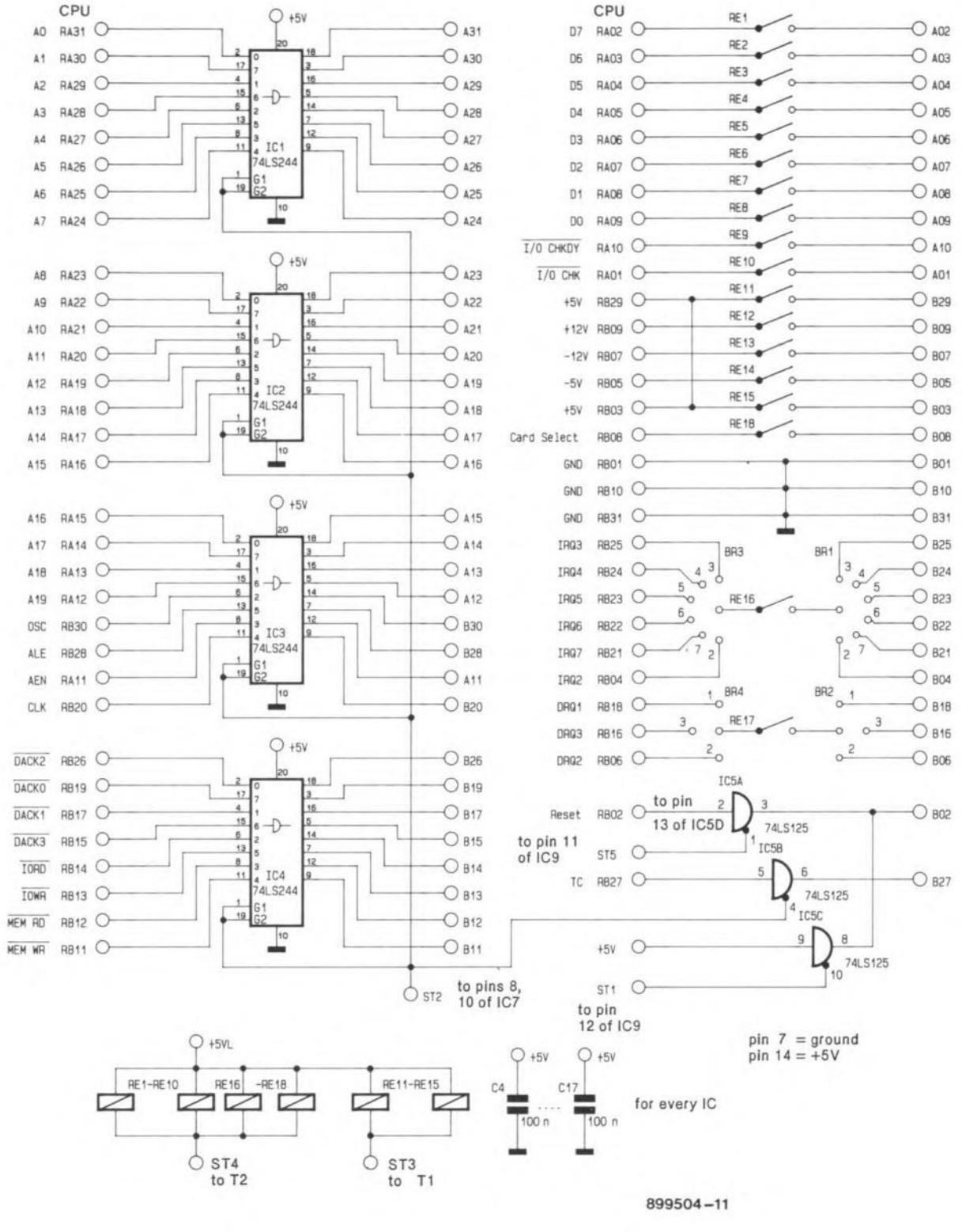


Fig. 1. Circuit diagram of the bus interface on the PC servicing card.

ance is elegantly eliminated by the present servicing card: the add-on board under examination may be removed and inserted without the need of switching the computer off and on again, and without causing hang-ups to the system. This is achieved by the servicing card decoupling the lines for the supply voltage, address-, data- and control- signals between it and the card under test.

Operation and controls

After it has been inserted into one of the bus expansion slots on the PC motherboard, the servicing card allows the user to enable or disable the card under test in two ways.

First, the user may press a button on the servicing card. When the associated red LED lights, the card under test is enabled. Since the push-button controls a toggle function, pressing it again causes the LED to go out and the supply-, ad-

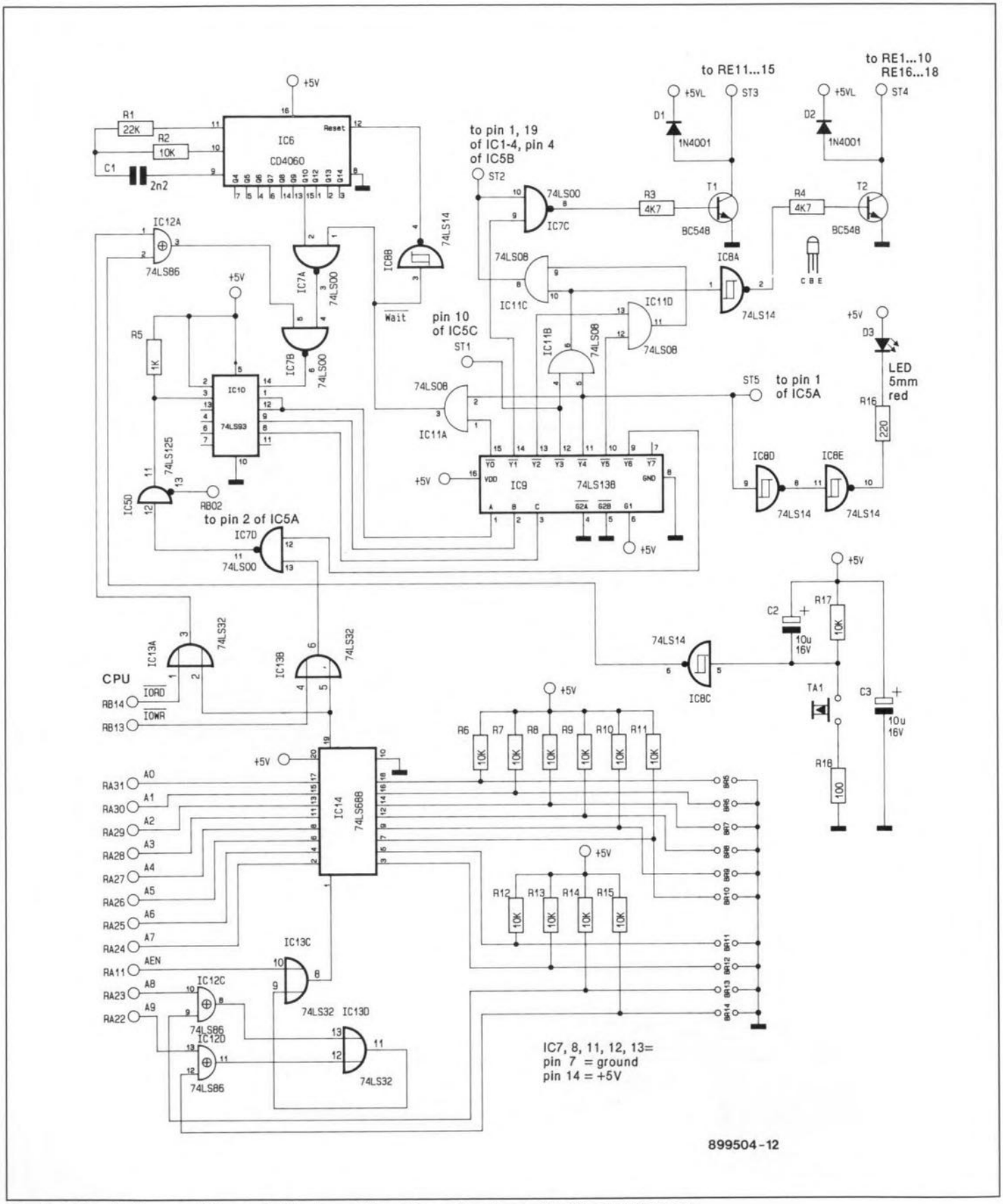


Fig. 2. Circuit diagram of the control logic and the address decoder on the PC servicing card.

dress-, data- and control- lines between the PC motherboard and the card under test to be disconnected.

The second control option lies in the use of software with basically the same function and LED indication as the 'disconnect' button. The servicing card thus allows home-made I/O cards to be tested with the aid of a small program that transfers the test data obtained to the user via the PC. Table 1 gives suggestions for such programs: examples are given in BASIC and Pascal.

Circuit description

The service card consists of three parts: a bus interface circuit, a control circuit and an address decoder circuit. The circuit diagram of the first part, the bus interface, is given in Fig. 1, while that of the control circuit and the address decoder appears in Fig. 2.

Bus interface circuit

The unidirectional control lines in a PC, such as the ones that carry the address and

count	output	WAIT	ST3	ST2	ST4	ST1	ST5 LED
0	$\overline{Y0}$	L	H	H	H	H	H
1	$\overline{Y1}$	H	L	H	H	H	H
2	$\overline{Y2}$	H	L	L	H	H	H
3	$\overline{Y3}$	H	L	L	L	L	H
4	$\overline{Y4}$	L	L	L	L	H	L
5	$\overline{Y5}$	H	L	L	H	H	H

Table 2. Overview of counter functions.

bus control signals, are applied to the circuit via bus drivers Type 74LS244, IC1–IC4. The outputs of these drivers are enabled or switched to three-state via a common control line, ST2. The PC address lines A0–A19 are buffered by IC1, IC2 and one half of IC3. The other half of IC3 buffers control signals OSC, ALE, AEN and CLK. In a standard PC, the frequency of the OSC signal is 14.31818 MHz. The system clock, CLK, runs at 4.77 MHz since it is always one-third of the OSC frequency. Control line ALE (address latch enable) is actuated at every bus cycle, and thus indicates that the CPU is not performing a DMA access operation. A DMA cycle is indicated by a separate control line, AEN.

The terminal count (TC) control line is buffered by three-state driver IC5c.

Circuit IC4 buffers a number of control signals provided by the PC motherboard. Lines $\overline{DACK0}$–$\overline{DACK3}$ (DMA acknowledge) are driven by the DMA controller, which uses them to issue DMA requests. Lines $\overline{IORD}$ and $\overline{IOWR}$ control read and write operations. Their equivalents for memory access operations are $\overline{MEMRD}$ amd $\overline{MEMWR}$ respectively.

Control signals which are either bidirectional or supplied by OC (open-collector) outputs are passed via reed relay contacts. This arrangement obviates the need of complex address decoders and direction control circuits. Datalines D0–D7 are passed via reed contacts RE1–RE8, and control lines $\overline{IOCHRDY}$ and $\overline{I/OCHK}$ via reed contacts RE9 and RE10. The I/O channel check ($\overline{I/OCHCK}$) line serves to signal parity errors in external memory areas. Such errors generate a non-maskable interrupt (NMI).

The $\overline{I/OCHRDY}$ (I/O channel ready) line enables bus cycles to be delayed. This is particularly useful for relatively slow input/output ports or memories which require the bus access time to be lengthened. Control line CARD SELECT is passed via reed relay contact RE18.

Relay contacts RE11–RE15 pass the supply voltages, +5 V, –5 V, +12 V and –12 V to the card under test.

The only fixed connection between the PC and the add-on board under test is the ground line. This ensures the presence of a reference potential the instant the add-on board is inserted, and prevents open-collector outputs being damaged.

One of interrupt request lines IRQ2–IRQ7 is passed via relay contact RE16 and wire jumpers Br1 and Br3, which are fitted in accordance with the IRQ line used. This enables current to flow from, say, RB25 via BR3, and on via RE16 and Br1 to B25, or from RB24 to B24, etc. The type of add-on board to be debugged determines which jumper is to be installed. Line IRQ4 is commonly used by the serial port, line IRQ6 by the floppy controller, and IRQ7 by the parallel port. This leaves IRQ2, IRQ3 and IRQ5 free for special applications and future extensions.

The use of the DMA request lines also differs from card to card. DRQ1 has the highest priority, DRQ3 the lowest.

The reset line forms a special case. Normally, it is buffered by three-state driver IC5a. When the servicing card is actuated, it automatically generates a short reset pulse for the add-on board.

Signal name	Pin designation			Signal name
	track side	↑ rear panel of PC	component side	
GND	B01		A01	$\overline{I/O}$ CHCK
RESET	B02		A02	D7
+5V	B03		A03	D6
IRQ2	B04		A04	D5
–5V	B05		A05	D4
DREQ2	B06		A06	D3
+12V	B07		A07	D2
reserved	B08		A08	D1
+12V	B09		A09	D0
GND	B10		A10	$\overline{I/O}$ CHRDY
$\overline{MEMW}$	B11		A11	AEN
$\overline{MEMR}$	B12		A12	A19
$\overline{IOWC}$	B13		A13	A18
$\overline{IORC}$	B14		A14	A17
$\overline{DACK3}$	B15		A15	A16
DREQ3	B16		A16	A15
$\overline{DACK1}$	B17		A17	A14
DREQ1	B18		A18	A13
$\overline{DACK0}$	B19		A19	A12
CLK	B20		A20	A11
IRQ7	B21		A21	A10
IRQ6	B22		A22	A9
IRQ5	B23		A23	A8
IRQ4	B24		A24	A7
IRQ3	B25		A25	A6
$\overline{DACK2}$	B26		A26	A5
TC	B27		A27	A6
ALE	B28		A28	A3
+5V	B29		A29	A2
OSC	B30		A30	A1
GND	B31		A31	A0

Table 3. Signal assignment on the PC expansion slot.

I/O Address	Function
000H–00FH	DMA-Controller (8237A-5)
020H–021H	Interrupt-Controller (8259-5)
040H–043H	Timer/Counter (8253-5)
060H–063H	System Register (8255A-5)
080H–083H	DMA-Page Register (74LS670)
0A0H–0BFH	NMI-Interrupt Register
0C0H–0FFH	Reserved
100H–1FFH	Front Panel Controller
200H–20FH	For Computer Games (Game Port)
210H–217H	Additional Unit
220H–24FH	Reserved
278H–27FH	Second Printer
2F8H–2FFH	Second Serial Interface
300H–31FH	Prototyping Card
320H–32FH	Hard Disk-Controller
378H–37FH	Printer Interface (parallel)
380H–38FH	SDLC-Interface
3A0H–3AFH	Reserved
3B0H–3BFH	Monochrome Adaptor and printer
3C0H–3CFH	Reserved
3D0H–3DFH	Colour Graphics Card
3E0H–3E7H	Reserved
3F0H–3F7H	Floppy Controller
3F8H–3FFH	Serial Interface

Table 4. PC I/O address map and reserved functions (all addresses in hexadecimal).

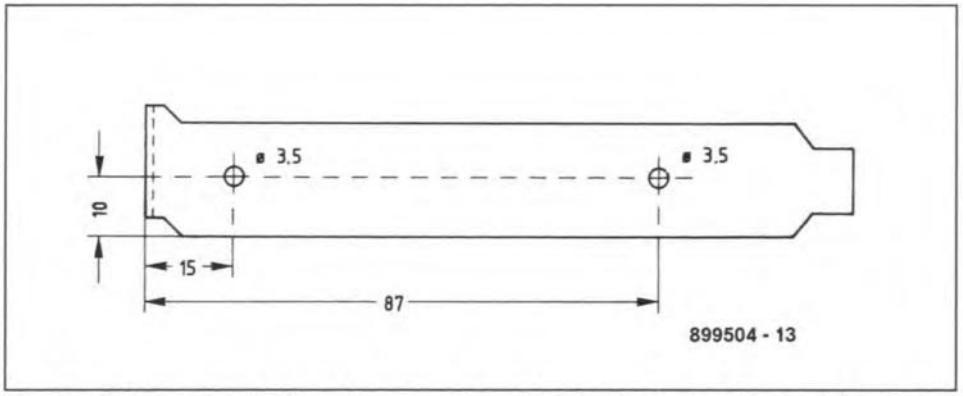


Fig. 3. Construction details of the cover plate which is attached to the circuit board.

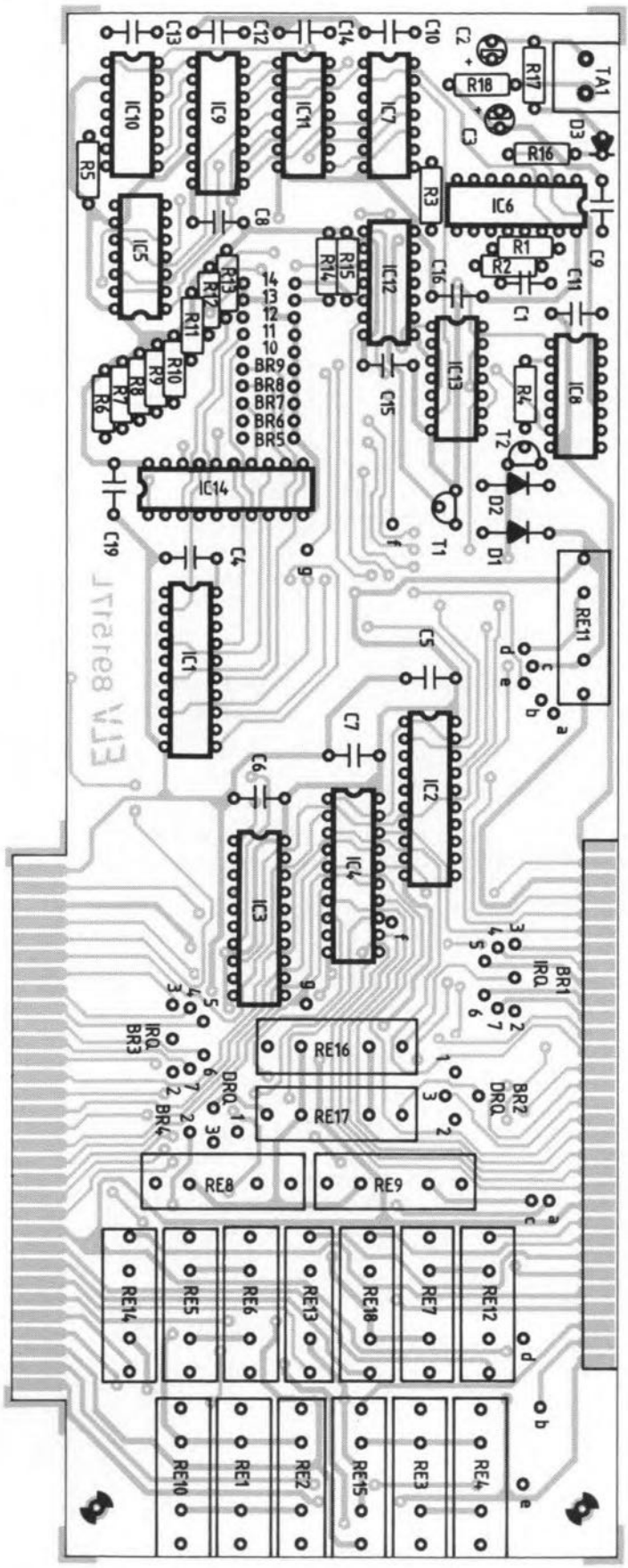


Fig. 4. Component overlay on the double-sided through-plated printed-circuit board.

COMPONENTS LIST

content of kit supplied by ELV

Resistors:

1	100Ω	R18
1	220Ω	R16
1	1k0	R5
2	4k7	R3;R4
12	10k	R2;R6–R15;R17
1	22k	R1

Capacitors:

1	2n2	C1
14	100n	C4–C17
2	10µF 16 V	C2;C3

Semiconductors:

1	74LS00	IC7
1	74LS08	IC11
1	74LS14	IC8
1	74LS32	IC13
1	74LS86	IC12
1	74LS93	IC10
1	74LS125	IC5
1	74LS138	IC9
4	74LS244	IC1–IC4
1	74LS688	IC14
1	CD4060	IC6
2	BC548	T1;T2
2	1N4001	D1;D2
1	LED 5 mm red	D3

Miscellaneous:

18	reed relay	Re1–Re18
1	PCB-mount push-button	Ta1
1	62-way PC expansion socket	
1	printed-circuit board	
100 cm	flexible wire	
20 cm	silvered wire	
1	PC card cover plate	

Control circuit

This consists of a 4-bit binary counter Type 74LS93, IC10, and a binary-to-decimal decoder Type 74LS138, IC9. The oscillator in IC6, a Type CD4060, is set to operate at about 10 kHz. Its Q10 output therefore supplies a clock signal of about 10 Hz. This signal is applied to the clock input of counter IC10 via IC7a and IC7b. When the counter reaches either state 0 or state 4, the output of AND gate IC11a goes low. This freezes the counter state because NAND gate IC7a blocks the clock pulses. Actuation of push-button Ta1 causes IC10 to be provided with a clock pulse via IC8c, IC12a and IC7b. This causes the output of IC11a to change from low to high, re-enabling divider IC6.

A clock pulse may also be provided by an I/O read operation on part of the PC. Further details on this are given in the description of the address decoder. When state 6 is reached, the counter is reset to 0 via IC7d and IC5d. Again, this can also be accomplished by a PC I/O write operation. After the computer has been switched on, the reset pulse causes buffer IC5d is to be switched briefly to three-state. Counter IC10 is subsequently reset to 0000 by pull-up resistor R5 at pin 3. This causes

the servicing card to be disabled when the PC is switched on.

The second part of the control circuitry decodes the individual counter states. This is done to ensure well-defined on/off switching of the address-, data-, control- and supply- lines. Reset line ST_1 is only actuated at counter state 3 and thus provides a reset pulse via IC_{5c}. This pulse resets the servicing card to a default state. The relays that pass the data signals are actuated during counter states 3 and 4 via IC_{11b}, IC_{8a} and R_4-T_2, while the control- and address-lines are passed at counter states 2–5 via gates IC_{11b}, IC_{11c} and IC_{11d}. In addition to these four states, the supply voltage is also actuated during state 1. The function and operation of the counter are summarized in Table 2.

I/O address decoder

The third part of the circuit is formed by the I/O address decoder. The servicing card occupies one address only in the PC's I/O map. All control functions are derived from the PC accessing this I/O address, i.e., data, whether read or written, is ignored.

The I/O addressing function is based on a 10-bit decoder which is set to the desired address with the aid of wire jumpers Br_5–BR_{14}. This arrangement enables the servicing card to be selected only when the I/O address supplied by the PC is equal to the address set with the wire jumpers. The outputs of XOR gates IC_{12c} and IC_{12d} are low simultaneously when the levels on PC address lines A9 and A8 are equal to the levels set with Br_{13} and BR_{14} respectively. Only in this condition does the output of OR gate IC_{13d} supply a low level.

Circuit IC_{14}, an 8-bit comparator, is enabled by a low level on the AEN line. Its output goes low if the levels of address bits A0–A7 match those provided by wire jumpers Br_5–Br_{10}.

PC bus line $\overline{IOR}$ is low when the CPU performs a read operation. This low level enables gate IC_{13a} so that counter IC_{10} is provided with a clock pulse. If the write line, $\overline{IOW}$, is actuated, the output of OR gate IC_{13b} goes low and causes IC_{10} to be reset to 0000.

Construction

The complete circuit is accommodated on a double-sided, through-plated printed-circuit board of dimensions 233×104 mm. Two angled pieces of aluminium are used to secure the card to the usual cover plate required for PC add-on boards. Cutting and drilling details of this plate are given in Fig. 3.

The construction of the servicing card is straightforward. IC sockets are not used so as to eliminate the risk of bad contacts. All parts must be fitted at the lowest possible height to prevent them touching parts on an adjacent board installed in the PC. Use precision pliers to press pin pairs in the horizontal rows of the 62-way bus expansion socket a little closer together so that they can be soldered direct to the copper tracks at the long side of the board as shown in the photograph.

Use two M3×6 mm screws and nuts to secure the support bracket on the board to the cover plate.

Address selection

The input/output address range and the associated functions used in a standard PC are given in Table 4.

The I/O address occupied by the servicing card is set by wire jumpers Br_5–Br_{14}. As an example, suppose the servicing card is to be controlled via I/O address 300. The first digit, 3, is equal to 11_2 and therefore set by leaving Br_{13} and Br_{14} open. Since the all the other digits are 0, Br_5–Br_{12} are closed.

Debugging

Although problems with the practical use of the servicing card should be rare if the construction is carried out with care and precision, a few hints are given to assist in faultfinding.

In case the servicing card causes the PC to crash, remove it from the expansion slot. Connect the card to an external 5-V power supply. The + is connected to bus contact B19 or B03, and ground to B01, B10 or B31. Measure the current consumption: this should be between 200 mA and 300 mA.

Actuate push-button Ta_1 to check that LED D_3 lights after a delay of about 0.5 s. If this does not happen, take a hard look at oscillator/counter IC_6. This is normally disabled via pin 12. Pressing the button should provide IC_{10} with a clock pulse. As a result, pin 3 of IC_{11a} should go high so that the counter starts to count either to state 0 or state 4 at which it disables IC_6. When the counter is not actuated, the bit combination at pins 1, 2 and 3 of IC_9 is either at 000 or 100. The states of outputs ST_1–ST_5 may be checked with reference to Table 2.

In the actuated state, the current consumption of the servicing card rises by about 70 mA. The current consumption then lies between 290 mA (typical) and 360 mA (maximum).

The operation of the I/O address decoder may be checked manually in case the relevant circuitry does not respond to the test program. The card address is assumed to be 300 as in the above example. This means that wire jumpers Br_5–Br_{12} are installed.

Connect inputs RA24–RA31 to ground. Pin RA11 (AEN line) must be made low in any case. Address lines A8 (RA23) and A9 (RA22) are tied to +5 V. Check that pin 1 of the 9-bit comparator, IC_{14}, is low. All other inputs must be low as well. As a result, pin 19 is low also. A brief low level at RB13 ($\overline{IOWR}$) should cause the servicing card to switch to its default state. Make RB13 high again and briefly actuate RB14 ($\overline{IORD}$) by making it low. Apply a couple of pulses in this way and check that they enable and disable the card via IC_{13a} and IC_{13b}.

If the service card does not function correctly after inserting it into the PC, it is recommended to remove it and first check the relay contacts RE_1–RE_{17} after applying 5 V. This is simple to achieve by measuring the contact resistance between the relevant points at the both sides of the board, near the expansion bus socket. The 'on' resistance of the contacts should be of the order of a few ohms. For this test, it is necessary to select the service card and switch on the extension function. Evidently, jumpers Br_1–Br_4 must be closed to be able to check that the IRQ and DRQ lines are connected by the relevant relay contacts.

The correct operation of bus drivers IC_1–IC_4 may be verified by applying high and low levels to the relevant control pins at the reverse side of the board. Provided the card is actuated, measurements may be made at the expansion slot.

Finally, the service card may be left in its PC slot even it is not used. ■

A complete kit of parts for the PC servicing card is available from the designers' exclusive worldwide distributors (regrettably not in the USA and Canada):

ELV France
B.P. 40
F-57480 Sierck-les-Bains
FRANCE
Telephone: +33 82837213
Fax: +33 82838180

Also see ELV France's advertisement elsewhere in this issue.

AN EXPERIMENTAL ALL-WAVEBAND FERRITE ROD ANTENNA

Richard Q. Marris, G2BZQ

The ferrite rod antenna described here is a most unusual conception in as much as it covers the frequency spectrum from 125 kHz to 24 MHz (2400–12.5 metres) with continuous tuning and without wavechange switching. This is in sharp contrast to the ferrite rod assemblies usually found in MW/LW radios

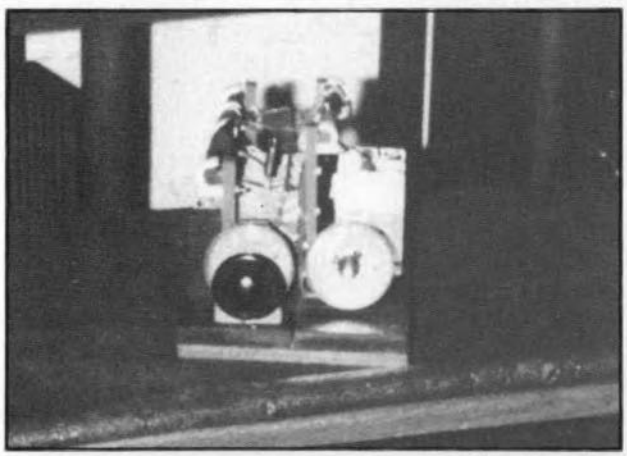
The unit was designed as an external antenna for use with any all-waveband radio with external antenna requirements such as communications receivers, vintage radios, home constructed radios and HF bands of modern transistor radios. A further and novel feature is that it covers the segment between the LW and MW bands, which is now again of much interest to many enthusiasts who have built or purchased receivers covering these frequencies, and that between 2000 and 2400 metres where there is increasing activity.

The unit is coupled to the radio input by either coaxial cable or 300 Ω flat twin feeder, which is of particular interest where end-fed long-wire antennas have to be attached. In the case of older communications and domestic receivers, it was not unusual for a 100 ft long outside wire antenna to be specified. Even if you have the real estate necessary for this, it is not going to be popular with the neighbours and local authorities.

Many successful experiments have been conducted over the entire waveband covered by the unit. The impressive results are in no small measure due to the careful selection of ferrite core material grades and sizes and the use of a 5-gang variable tuning capacitor.

The experimental unit is seen from various angles in the photographs, in one of which (4) it is shown on top of a superb vintage Pye 9-waveband all-wave Export Receiver. This receiver is in everyday domestic use: its audio reproduction outperforms most modern AM radios. Since the unit is experimental, certain imperfections can be seen in the photographs owing to modifications carried out during the final construction, testing and evaluation, but

1



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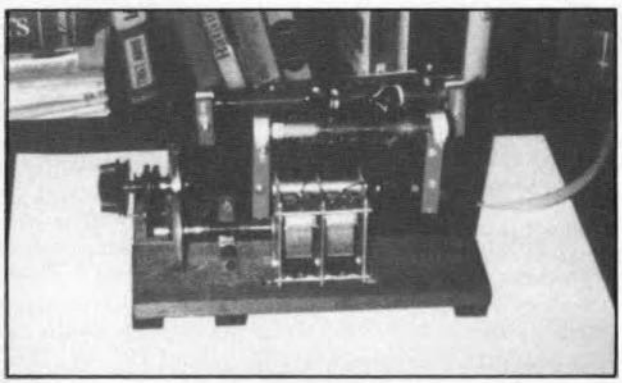

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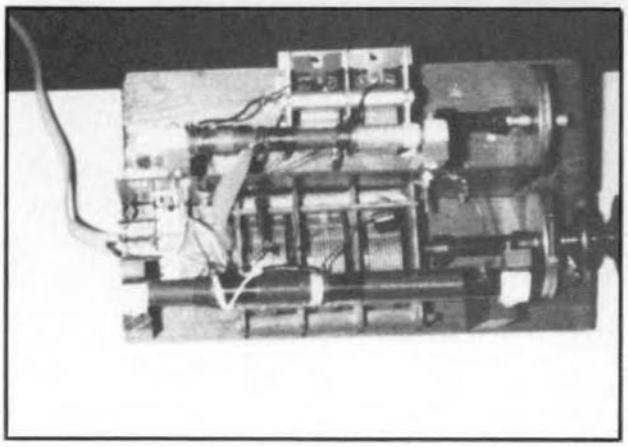

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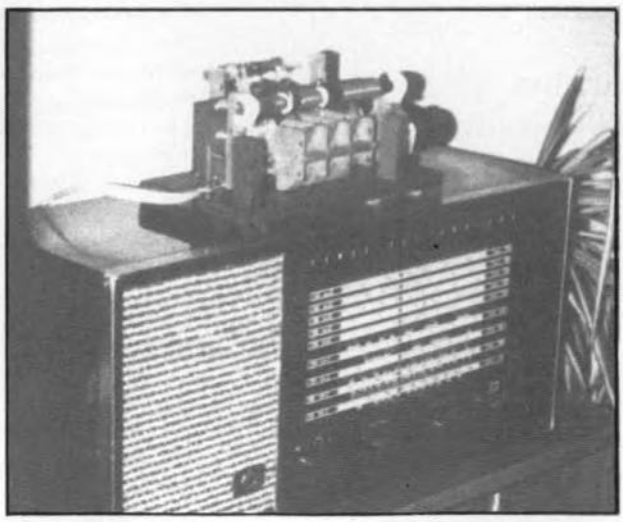

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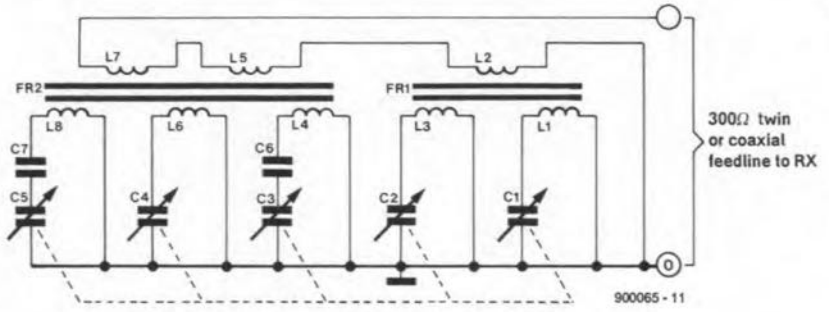

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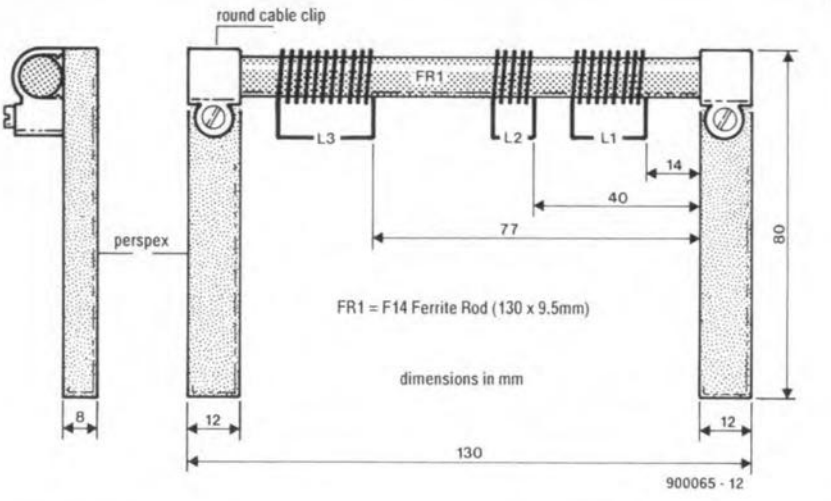

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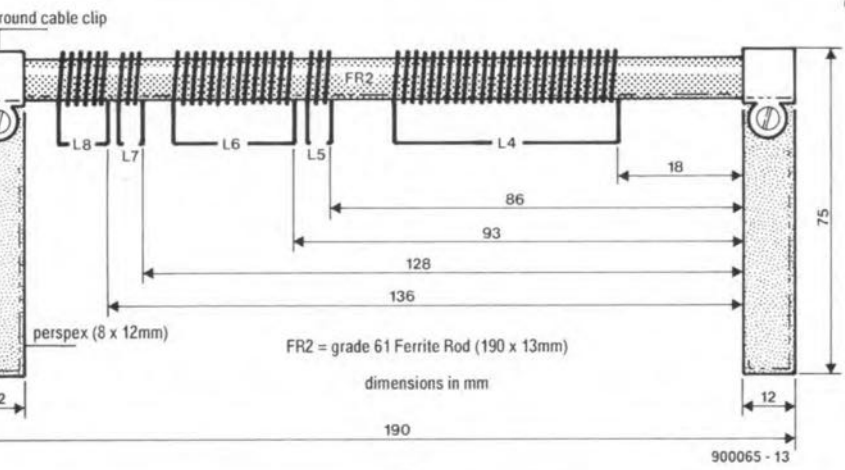

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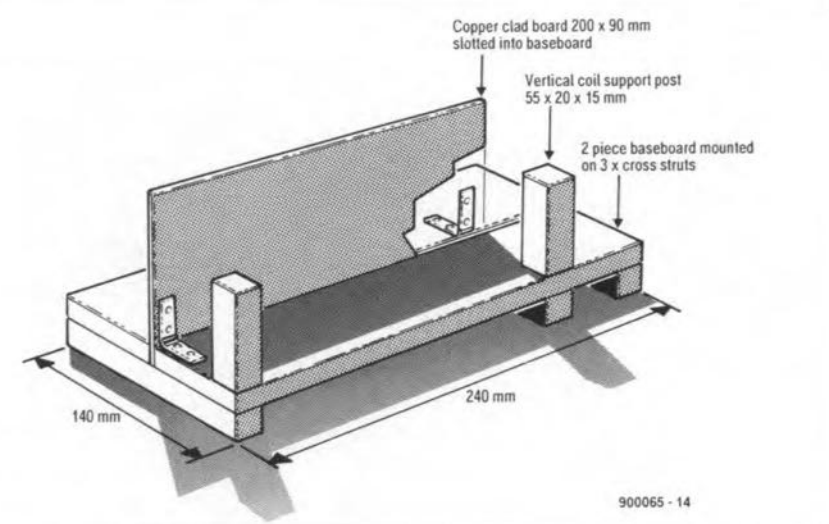


that's experimental work for you!

The circuit

The circuit diagram in Fig. 5 shows five tuned circuits: L1–C1; L3–C2; L4–C3–C6; L6–C4; and L8–C5–C7. A 5-gang, 500 pF per section, variable capacitor is used for C1 to C5. The location of coils L2, L5 and L7, coupling the antenna to the receiver, is critical. All inductors are wound on ferrite rods.

The tuned circuits are adjusted simultaneously and cover different wavebands with small overlaps. The required band is selected automatically by the tuned input circuits in the receiver. There is no interaction between the five tuned circuits during normal operation.

The prototype has been evaluated and tested with several types of communications, domestic and vintage receiver. The wavebands covered by each of the five tuned circuits are:

L1–C1 — 125–450 kHz (2400–667 m)
L3–C2 — 400–1900 kHz (750–158 m)
L4–C3–C8 — 1000–4250 kHz (300–71 m)
L6–C4 — 3500–9500 kHz (85.7–31.6 m)
L8–C5–C7 — 8000–24000 kHz (37.5–12.5 m)

Construction

The baseboard assembly shown in Fig. 8 is made of two pieces of 18–22 mm thick (ply)wood. The vertically mounted copper-clad board is for direct common earthing connections and is trapped between the two halves of the baseboard and secured with two brass angle brackets. All wood parts should be given an application of teak colour wood dye.

The LF-MF coil assembly—see Fig. 6 — uses a 130×9.5 mm Grade F14 ferrite rod, cut down from a standard 140 mm long rod with a Junior hacksaw. Grade F14 is a nickel-zinc material that is usable up to 2 MHz, where performance just begins to fall off. The rod is clamped at either end in a plastic, round cable clip that is secured to a vertical bar of perspex (hardwood would do). The assembly is bolted to the vertical copper-clad board as shown in Fig. 9, side view 'A'.

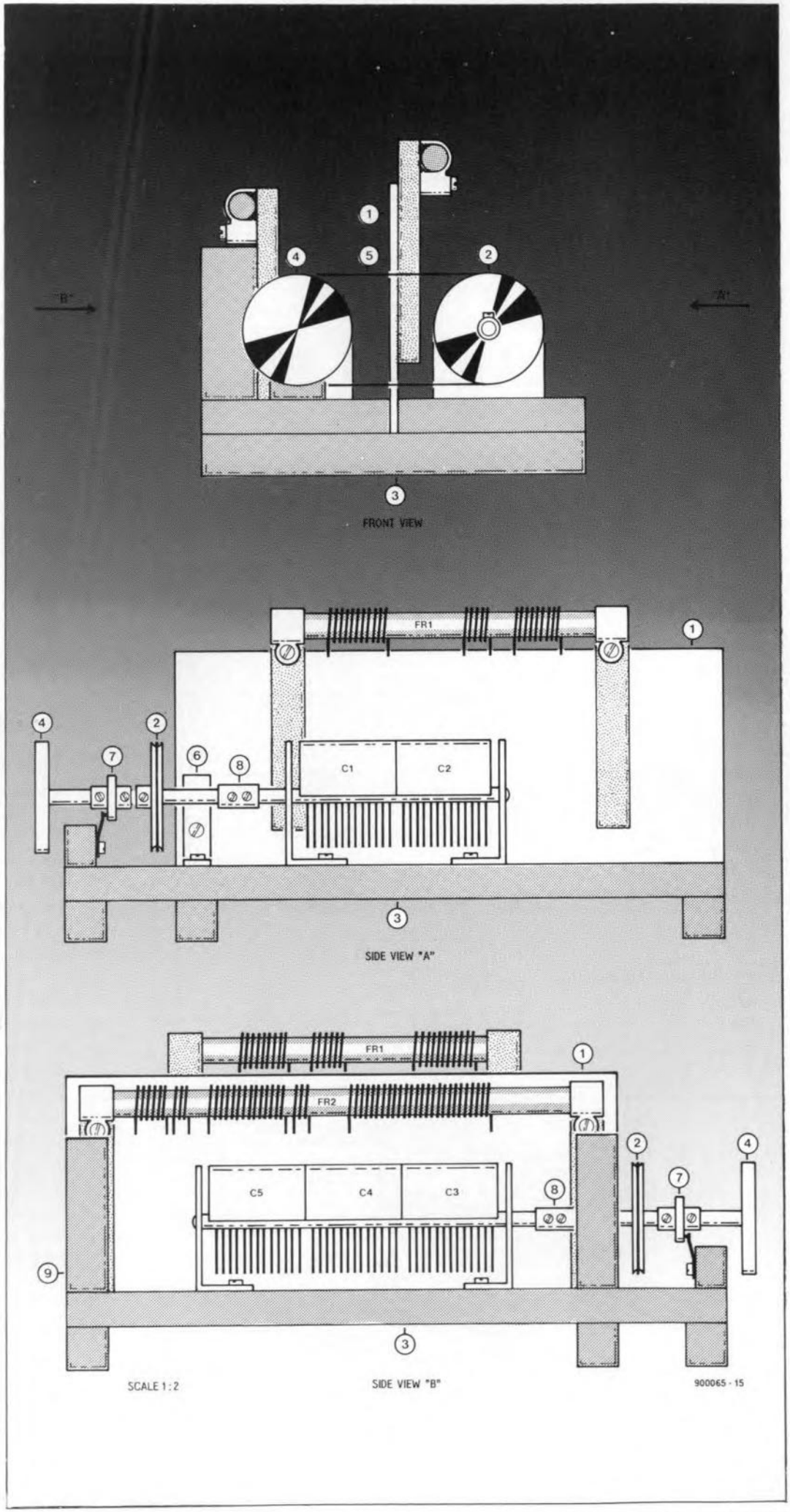
Both L1 and L3 are proprietary inductors; each has a small coupling winding which should be ignored. The coupling coil to the receiver, L2, consists of 22 close-wound turns of 32 SWG enamel copper wire on a small paxolin former. All three should be positioned in the exact positions shown in Fig. 6: deviations will change the overall frequency coverages.

The HF coil assembly—see Fig. 7—is also mounted on two vertical perspex (or

1 = copper-clad board
2 = 2 in. dia. cord drum
3 = wooden base
4 = knob (with cord drum and slow-motion drive behind)
5 = drive cord with tension spring
6 = brass angle bracket
7 = slow-motion drive
8 = shaft coupler
9 = feeder terminal block

PARTS LIST

FR1 = ferrite rod; Grade F14; 140×9.5 mm, cut to 130mm; Type FRA; stock no. 35-14147; Circkit Distribution Ltd
FR2 = ferrite rod; Grade 61; 7.5×0.5 in; Type R61-050-750; Amidon Associates, 12033 Otsego St, Nth Hollywood, California 91607, USA
L1 = antenna coil LWC1; stock no.35-00108; Cirkit Distribution Ltd
L3 = antenna coil MWC2; stock no. 35-00268; Circkit Distribution Ltd
C1, C2 = 2-gang × 500 pF large BC type variable capacitor; J. Birkett
C3, C4, C5 = 3-gang × 500 pF large BC type variable capacitor; J. Birkett
C6 = 470 pF, silver mica or ceramic
C7 = 1000 pF, silver mica or ceramic
slow-motion drive = code RX42V; Maplin
shaft coupler (2 off) =0.25 in. shaft; J. Birkett
dial cord drum (2 off) with spring; 54.5 mm dia.; code RX43W; Maplin
copper-clad circuit board, undrilled; 200×90 mm
cable clip, plastic (4 off) to fit ferrite rods
wire (a) 32 SWG enamel insulated copper
(b) 1/0.6 mm single-strand PVC covered, 1.2 mm outside diameter (NOT 1.0 mm O/D!)



hardwood) columns that are later screwed to the vertical coil support posts shown in Fig. 8. The ferrite rod is 7.5×0.5 inch (the US manufacturer specifies the dimensions only in inches). It is made of Grade 61 nickel-zinc material, specified for use up to 15 MHz, but which here, with special winding techniques, has been stretched to over 40 MHz.

The coils are closewound straight on to the rod from single-strand 1/0.6 mm PVC covered wire, 1.2 mm overall diameter. Similar wire exists with thinner insulation of about 1.0 mm overall diameter, but this MUST NOT be used. The direction of winding should be same for all five coils. They should be positioned exactly as shown in Fig. 7: deviations will result in incorrect frequency ranges and incorrect coupling. After the coils have been tested, they should be held in place with spots of adhesive at the ends. The number of turns for the coils is:

L_4 — 36;
L_5 — 3;
L_6 — 15;
L_7 — 2;
L_8 — 5.

The 5-gang variable capacitor is made by coupling a 2-gang and a 3-gang capacitor together with the aid of two cord-drive drums, a length of dial cord and a spring for tension as shown in Fig. 9 and the photographs. A single epicyclic slow-motion drive operates the two variable capacitors simultaneously.

The variable capacitors are of the 'large broadcast' type that have the advantages of wide-spaced plates, ceramic insulation and a full 500 pF maximum capacitance, while their large size assists in keeping the leads to the coils short. Moreover, the minimum capacitance is smaller than that of most smaller compact types.

In view of possible variations in the dimensions of different makes of capacitor, the exact mounting positions are not shown.

The assembly should be fitted as shown with the aid of shaft couplers and lengths of 0.25 in. dia. rod to align the assembly and drive mechanism. On the prototype, the 2-gang variable capacitor was screwed vertically to the baseboard with the metal frame hardwired to the vertical copper-clad board. The 3-gang was mounted upside down (to reduce lead lengths) and bolted to the copper-clad board.

All earth connections should be soldered direct to the copper-clad board by the shortest possible route.

Coupling coil L_2 is connected to the feeder terminal block—see Fig. 9, side view 'B'—by a short length of 300 Ω twin feeder. Coils L_5 and L_7 are connected in series and also connected to the terminal block via some 300 Ω twin feeder and then wired in series with the feeder from L_3. This means that all three coils are in series, as shown in the circuit diagram.

The feeder to the receiver may be either the usual coaxial cable or 300 Ω flat twin feedline. This gives versatility of connection to all types of receiver input impedance.

It might be thought that the coupling coils should have dissimilar numbers of turns, depending on the feedline impedance. Practical experiments indicated that only a fraction of a turn difference would be necessary on L_5 and L_7, while L_2 was not critical. Because of that, the numbers of coupling turns are a compromise that does not degrade the performance, however.

Testing

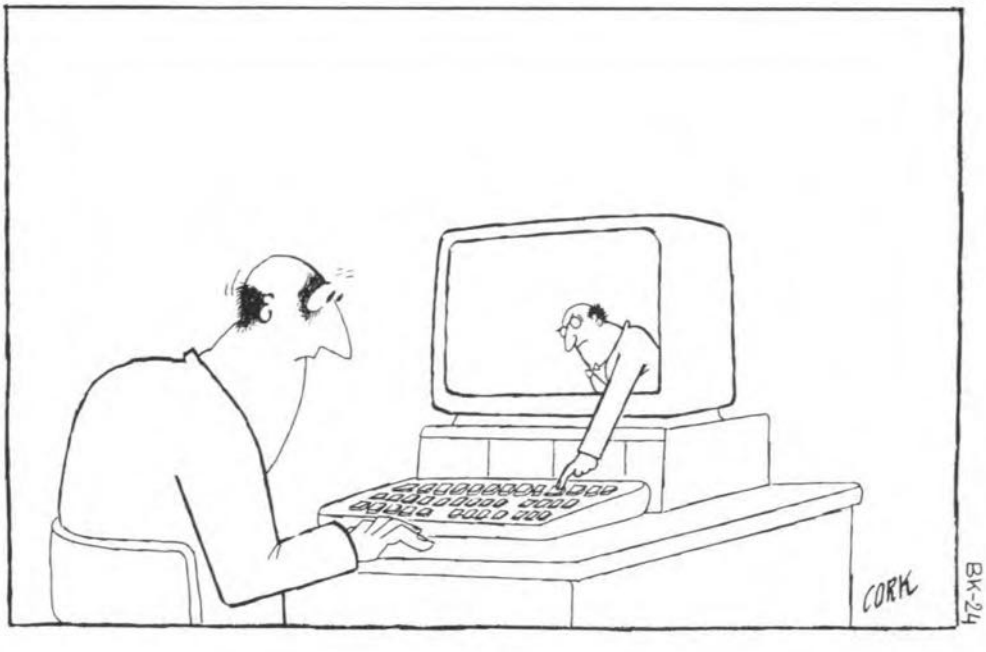
The correct feeder should be connected between the feeder terminal block and the receiver. It will be found that the tuning of the antenna unit is quite sharp, thus improving the selectivity of the receiver. Whatever the selected waveband, the antenna tuning should be brought to resonance as indicated by a significant increase in signal. The antenna is directional, with maximum signal appearing on the 'flat' side of the rod and minimum signal at the ends of the rod. Rotation of the unit will, therefore, increase/decrease the strength of the received signal. If there is interference from other stations, local man-made noise, or static, the antenna should be rotated slightly to either side to reduce/eliminate that interference. In general, it will be noticed that the ambient noise level is far lower than with a long-wire antenna.

It will have been noted that the earlier quoted frequency ranges have small overlaps, so that the whole range of 125 kHz to 24 MHz is covered by five complete sweeps of the 5-gang capacitor to match any preselected receiver frequency range, whether LF, MF or HF. A preamplifier may be needed between the antenna and the receiver in the higher HF ranges if the receiver does not have a high RF gain.

The exact frequency ranges can be checked, if required, with a signal generator and appropriate receiver. If, as is probable, a signal generator is not available, but the receiver is dial calibrated, it is possible to check the ranges with an artificial noise signal. For this, a small battery-operated calculator is placed about 12–18 in. from the antenna. This generates a noise signal that can be resonated by the antenna-receiver combination. By manipulation of the calibrated receiver tuning and the antenna tuning, it is possible to check the frequency ranges of the five antenna ranges and, most importantly, to check that the ranges overlap somewhat to provide continuous frequency coverage.

Conclusion

This compact antenna unit covers all those frequencies, HF, MF and LF, that one may like to receive below 24 MHz. It is directional for elimination or reduction of adjacent station interference, man-made electrical noises and static. It is far smaller than conventional antennas and picks up far less noise. It could be housed in a simple polished or painted wood enclosure or plastic (not metal!) case. ■



INTERMEDIATE PROJECT

A series of projects for the not-so-experienced constructor. Although each article will describe in detail the operation, use, construction and, where relevant, the underlying theory of the project, constructors will, none the less, require an elementary knowledge of electronic engineering. Each project in the series will be based on inexpensive and commonly available parts.

ACOUSTIC TEMPERATURE MONITOR

J. Ruffell

Electronic temperature monitoring need not be complex. This circuit gives an audible indication when a preset temperature is reached. It can be used as a thermal alarm on boilers and heating systems, as a bath water temperature indicator, or in an electronic whistle kettle.

Basically, the temperature alarm consists of three parts: a temperature sensor, a small printed-circuit board which contains the measurement circuit, and a piezo-ceramic buzzer that functions as an indicator. The printed-circuit board and the buzzer are housed in a small ABS enclosure, together with the battery that powers the circuit. The sensor is connected to the circuit via two lengths of flexible wire so that it can be located as close as possible to the object whose temperature is to be measured.

Temperature sensor

The temperature sensor is formed by an integrated circuit rather than the more conventional NTC (negative temperature coefficient) resistor. This choice was made to ensure a wide temperature range with acceptable accuracy. The sensor used is a Type LM235. This device, which looks like an ordinary transistor in a plastic enclosure, contains a fairly complex circuit that provides an output voltage that is a function of ambient temperature. The output voltage is linear over a wide range and accurately defined at 10 mV/K. Since the electrical behaviour of the LM235 is not unlike that of a temperature-sensitive zener diode, a similar circuit symbol is used. A third pin is drawn, however, to indicate that the LM235 has a calibration input (which is not used here).

The sensor is supplied in a number of versions for different temperature ranges. The LM135 is suitable for −55 °C to +150 °C, the LM235 for −40 °C to +125 °C, and the LM335 for −40 °C to +100 °C. In principle, all three may be used in this circuit: the choice depends on the application. Note, however, that the price of the devices rises with the temperature range.

The circuit

The circuit diagram is given in Fig. 1. Apart from the sensor, only one integrated circuit is used. This IC, a TLC272, contains two CMOS operational amplifiers, A_1 and A_2. The first is used for the temperature measurement, the second for the acoustic alarm.

Opamp A_1 is wired as a comparator: it compares the voltage provided by the temperature sensor, D_2, to that provided by an adjustable reference, D_1. The LM336 in that position is a temperature-compensated 5-V zener diode. The reference voltage may be adjusted between 0 V and +5 V with the aid of preset P_1 before it is applied to the +input of comparator A_1.

As long as the temperature measured by D_2 is relatively low, the voltage at the −input of A_1 is lower than the reference voltage at the +input. As a result, the out-

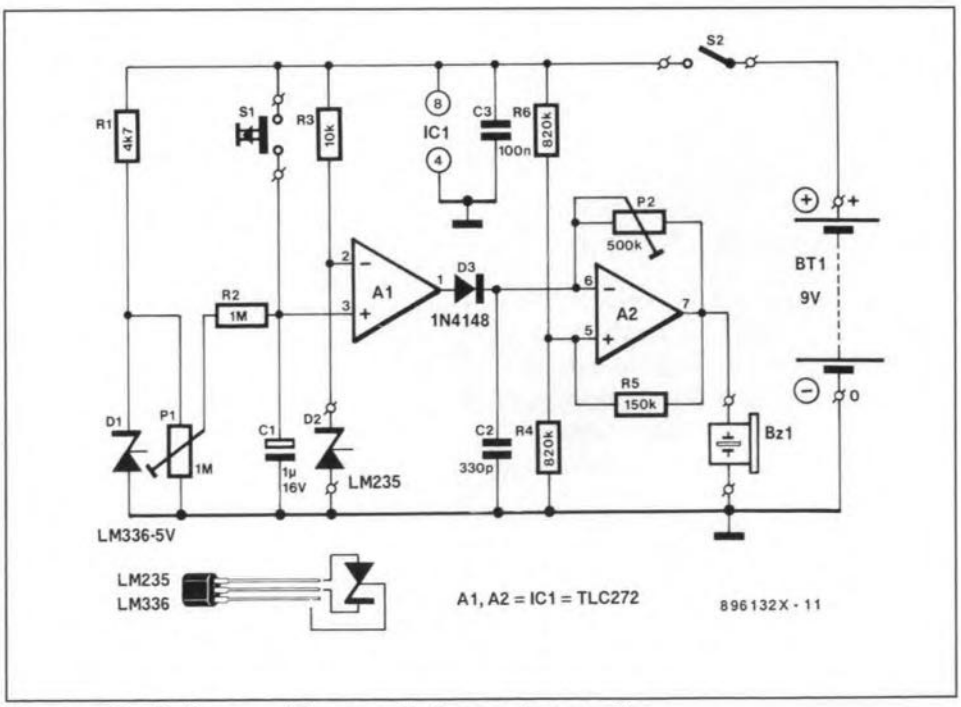


Fig. 1. Circuit diagram of the acoustic temperature monitor.

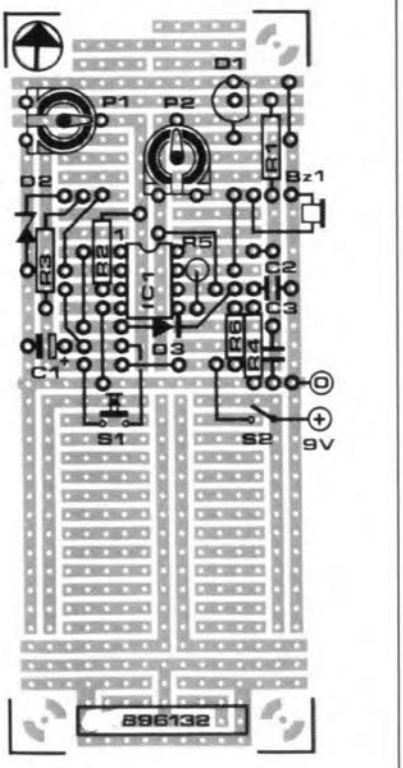


Fig. 2. Suggested construction on universal prototyping board size-1.

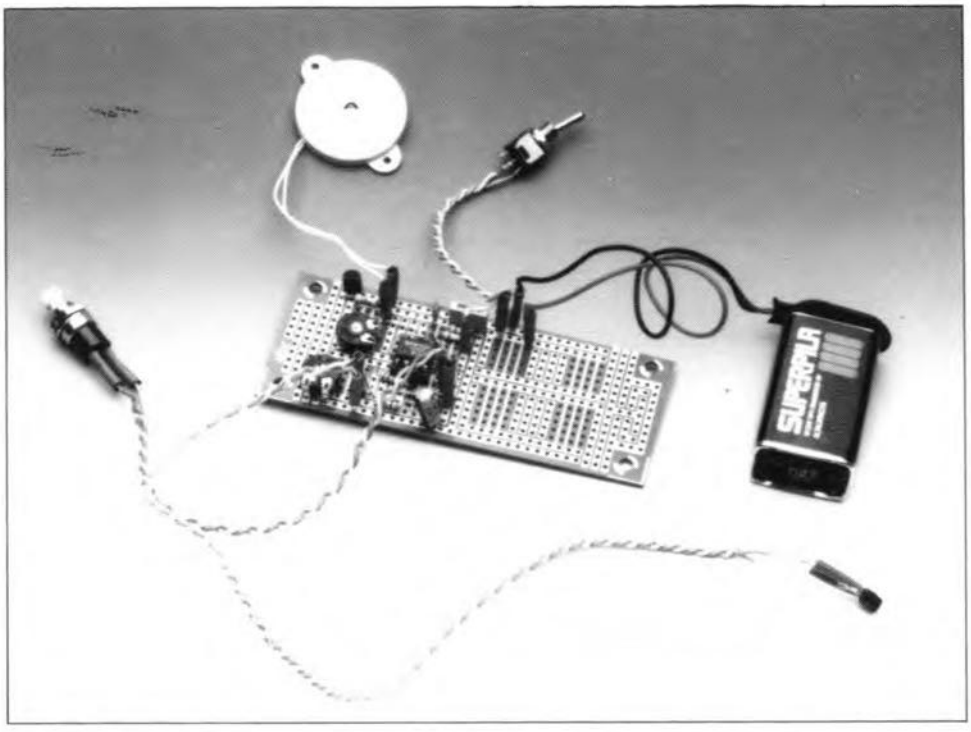


Fig. 3. Completed printed-circuit board with external components connected.

COMPONENTS LIST

Resistors:

1	4k7	R_1
1	1M0	R_2
1	10k	R_3
2	820k	R_4;R_6
1	150k	R_5
1	1M0 preset H	P_1
1	500k preset H	P_2

Capacitors:

1	1µ0 16V	C_1
1	330pF	C_2
1	100nF	C_3

Semiconductors:

1	LM336	D_1
1	LM235	D_2
1	1N4148	D_3
1	TLC272	IC_1

Miscellaneous:

1	push-to-make button	S_1
1	miniature on/off switch	S_2
1	passive buzzer	Bz_1
1	9-V battery	Bt_1
1	printed-circuit board	UPBS-1

put of the comparator is high, i.e., virtually equal to the battery voltage. The oscillator, A_2, is disabled because the junction of its frequency-determining components, P_2-C_2, is held at about +9 V via diode D_3. Hence, buzzer Bz_1 remains silent.

This condition is ended when the measured temperature rises above the set threshold. In electronic terms, this means that the voltage supplied by D_2 is higher than that at the +input, so that A_1 toggles and supplies a low output voltage. Diode D_3 blocks and decouples the output of A_1 from the oscillator, A_2. Buzzer Bz_1 is actuated and supplies an acoustic signal of which the frequency is determined by P_2.

Push-button S_1 allows the circuit to be reset following an alarm condition. When pressed, it causes C_1 to be charged to the supply voltage, so that the voltage at the +input of A_1 is higher than that at the –input, irrespective of the voltage supplied by D_2. Pressing S_1 therefore disables the oscillator. Evidently, C_1 will be discharged slowly via P_2 and R_1. This takes a while, however, because of the relatively high value of the components. The upshot is that D_2 will have cooled down to a temperature below the alarm level well before the voltage at the +input of A_1 has fallen below the reference voltage.

Construction and adjustment

A suggested arrangement of the components on universal prototyping board size-1 (UPBS-1) is shown in Fig. 2. The population of this PCB should not present any problems. The buzzer, the temperature sensor, the battery and the two switches (reset and on/off) are external components, which are connected to the circuit via wires and solder terminals. In most cases, the alarm will be set for a fixed temperature, e.g., approximately 100 °C for boiling water. This allows a preset to be used as shown in the component mounting plan. If a variable temperature setting is required, P_1 is replaced by a potentiometer which is fitted on the front panel of the enclosure.

The way in which the sensor is mounted and connected to the circuit depends on the application. For temperature measurements on fixed objects, the sensor is simply secured with a small clamp or a plastic cable tie. For measurements on hot gases, mount the sensor at the end of a probe and insulate its terminals with shrink sleeving or two-component epoxy resin.

The alarm is simple to adjust with the aid of a thermometer. Immerse the sensor (not its terminals) in water which is heated until the desired alarm temperature is reached. Wait a few seconds, and adjust P_1 until the buzzer just starts to sound. Next, set the frequency of the alarm tone by adjusting P_2.

In cases where the alarm is used continuously, as with a CH boiler, the battery may be replaced by a mains adaptor with 9-VDC output. The current requirement of the alarm is modest at a few milli-amps only, so that a low-power adaptor may be used. ■

CENTRONICS A-D/D-A CONVERTER

J. Ruffell

To the many PC users who would like to interface their computers with the real world we present an analogue-to-digital and digital-to-analogue converter. The low-cost, versatile, unit with accompanying control software is unconventional in that it is connected to the PC's Centronics port, which is normally used for a parallel printer.

The use of standard interfaces for applications they are not intended for is widespread and goes back to the days of the first hobby computers. The advantages are obvious: there is no need to get to grips with the computer hardware, and the function of the peripheral is not dependent on extension connectors peculiar to the system. Thus, the software required to control the 'custom-made' peripheral is often hardware-dependent and obtained by rewriting the system-resident I/O routines, or accessing the relevant circuitry in a non-standard way, e.g., through bypassing the BIOS (basic input/output system).

Many modern PCs contain large gate arrays instead of individual I/O circuits. The A-D/D-A converter described may be used without the need of rewriting the control routines available for parallel I/O operations. Note, however, that this does not imply complete independence of the hardware, since the BIOS routines normally used for controlling the Centronics printer port are not suitable for the controlling the present converter board. Fortunately, the degree of hardware dependency is low and restricted to a few addresses in I/O routines. The control program available for the converter board should not, therefore, give problems on most MS-DOS computers. Note, however, that a number of older PCs have a printer port with incomplete handshaking. The absence of certain lines generally does not cause problems when a standard printer is used. The converter board, however, may require these lines for a number of functions.

Centronics port inputs

The block diagram of the A-D/D-A converter is given in Fig. 1. The operation of the circuit is based on the use of the output as well the input lines of the Centronics port. The latter are normally used to convey 'paper empty', 'busy' and other information from the printer to the computer. The converter, however, uses these inputs to convey digital data, such as the state of two comparators, to the computer. The two comparators enable two analogue input voltages to be compared with an analogue output voltage supplied by the DAC (digital-to-analogue converter). By writing a series of rising values to the DAC and monitoring the relevant comparator output, the computer is able to determine the value of the analogue input voltage applied to the board. Such an operation is generally referred to as successive approximation. In the present case, its advantage lies in the use of a single computer input only instead of a number equal to the conversion resolution in bits (in this case, eight). This is an important consideration since there are few inputs on a Centronics interface. A LED monitor circuit enables, by selection, either the state of the Centronics data lines or those of the digital outputs of the circuit to be indicated.

Circuit description

The actual circuit (see Fig. 2) is just as straightforward as the block diagram, although some details may create an impression of greater complexity. The eight databits on the Centronics port are fed direct to the inputs of the DAC, IC_{12}. Provided the PC port meets the drive specifications set out in Centronics standard, these lines are driven by open-collector (OC) outputs,

MAIN SPECIFICATIONS

- **8-bit D-A converter**
  - output voltage: –5 V to +5 V
  - total settling time: approx. 1 µs
  - three reference options:
    REF-02 (+5 V; very stable)
    TL317 (+5 V; low-cost)
    external source
- **2-channel A-D converter**
  - DAC-based successive approximation
  - attenuators for adjustable input sensitivity
- **4 multi-purpose OC outputs**
  - $I_{C(max)}$=100 mA; $U_{CE(max)}$=30 V
- **3, 4 or 5 digital inputs**
  - switching threshold: approx. 2.5 V
  - CMOS and TTL compatible
- **LED indication for functional checks**
  - monitors either Centronics datalines or digital input/output lines
- **Supply voltage: ±12 V**

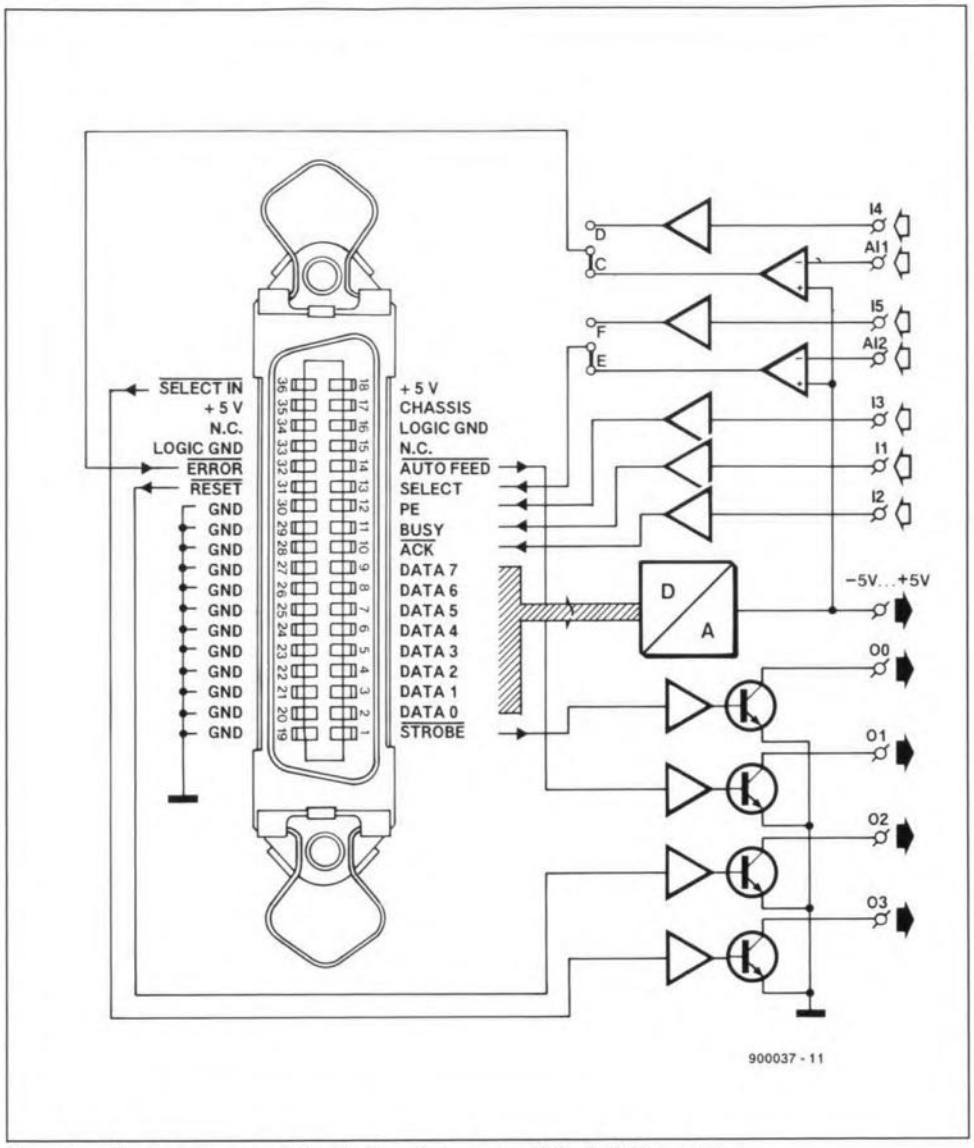


Fig. 1. Block diagram of the Centronics-compatible A-D/D-A card.

whence the use of pull-up network R_3. The output current supplied by the DAC is determined by the value of the dataword supplied by the computer. This current is converted into a voltage with a range of −5 V to +5 V with the aid of IC_9 and IC_{10}. The relation between the applied data and the output voltage, U_o, is expressed by

$$U_o = U_{ref}\,(\text{data}-128)/128 \quad [\text{V}]$$

The reference voltage, U_{ref}, is supplied either by an external source (via jumper B), or by an internal source. The internal source is either a REF-02 or a TL317; the REF-02 provides the highest stability and accuracy, but is more expensive than the TL317. The choice between these two devices is up to you.

Opamps IC_{11a} and IC_{11b} form the previously mentioned comparators. Their inputs are protected against overvoltage by two diodes (D_3-D_4/D_5-D_6) and a resistor (R_{45}/R_{46}). The input sensitivity may be adapted by modifying attenuators R_{47}-R_{48} and R_{49}-R_{50}. The indicated resistor values provide an attenuation of 2 times, which creates an input voltage range of −10 V to +10 V. In case one or both analogue inputs are not used, the associated input on the Centronics interface may be set to function as a digital input. This is achieved by means of a jumper (C–D; E–F).

Each digital input consists of a darlington transistor (T_1–T_5), a collector resistor and two base resistors. The inputs switch at about +2.5 V, which makes them suitable for driving both TTL and CMOS logic. The maximum input voltage is about +30 V.

The digital outputs, T_6–T_9, are of the open-collector type to allow direct connection to small loads, such as LEDS or relays. Note, however, that any relay coil must shunted by a diode to prevent the transistor being damaged by inductive voltage surges. The maximum voltage that can be switched by the output transistors is 30 V.

Two three-state buffers, IC_1 and IC_2, and a LED array, allow the operations of the ADC and the DAC to be checked visually. Depending on the connection made by jumper G–H, the LEDs indicate either the data applied to the DAC, or the state of the digital inputs on the Centronics port. Since the monitor circuit falls short of one line to provide an indication of SEL (select), this is taken over by two inverters, IC_{3a}-IC_{3b}, and LED D_{15}. The function of each LED is shown in Table 1.

LED	jumper G	jumper H
D7	00	D0
D8	01	D1
D9	02	D2
D10	03	D3
D11	I1	D4
D12	I2	D5
D13	I3	D6
D14	I4/AI1	D7
D15	I5/AI2	I5/A12

Table 1. LED function overview.

Construction

The converter is best constructed on the double-sided, through-plated printed-circuit board of which the component mounting plan is shown in Fig. 3 (the track lay-outs are not given because this through-plated board is virtually impossible to make without special equipment).

The construction itself is precision work, but none the less entirely straightforward with reference to the component overlay and the parts list. As already stated, the choice between the REF-02 and the TL317 is up to you: simply fit and omit the relevant components as indicated in the parts list. Connector K_1 is a standard 36-way Centronics socket with angled pins for PCB mounting. This type of connector is often used on matrix printers.

Control software and setting-up

A 360-KByte MS-DOS formatted 5¼-inch diskette is available for this project. The programs on the disk are helpful for adjusting and testing the converter board. A Turbo-Pascal source file is provided that contains the basic routines for the I/O operations with the A-D and the D-A converter. This program uses a set of default I/O register addresses, which may have to be changed depending on the computer used. It should be noted that the logic levels in the status-, data- and control-registers must correspond to those of the inputs and outputs. This point is made because the levels of the active-low lines are inverted either by hardware or software, again, depending on the type of computer. Obviously, the LED indicator array comes in handy here.

Adjustment

The first routine given in the form of a flow-chart is the adjustment procedure (see Fig. 4). All indicated voltages are measured with respect to the analogue ground potential. The relevant connection for the DVM may be found between the two analogue inputs and the analogue output.

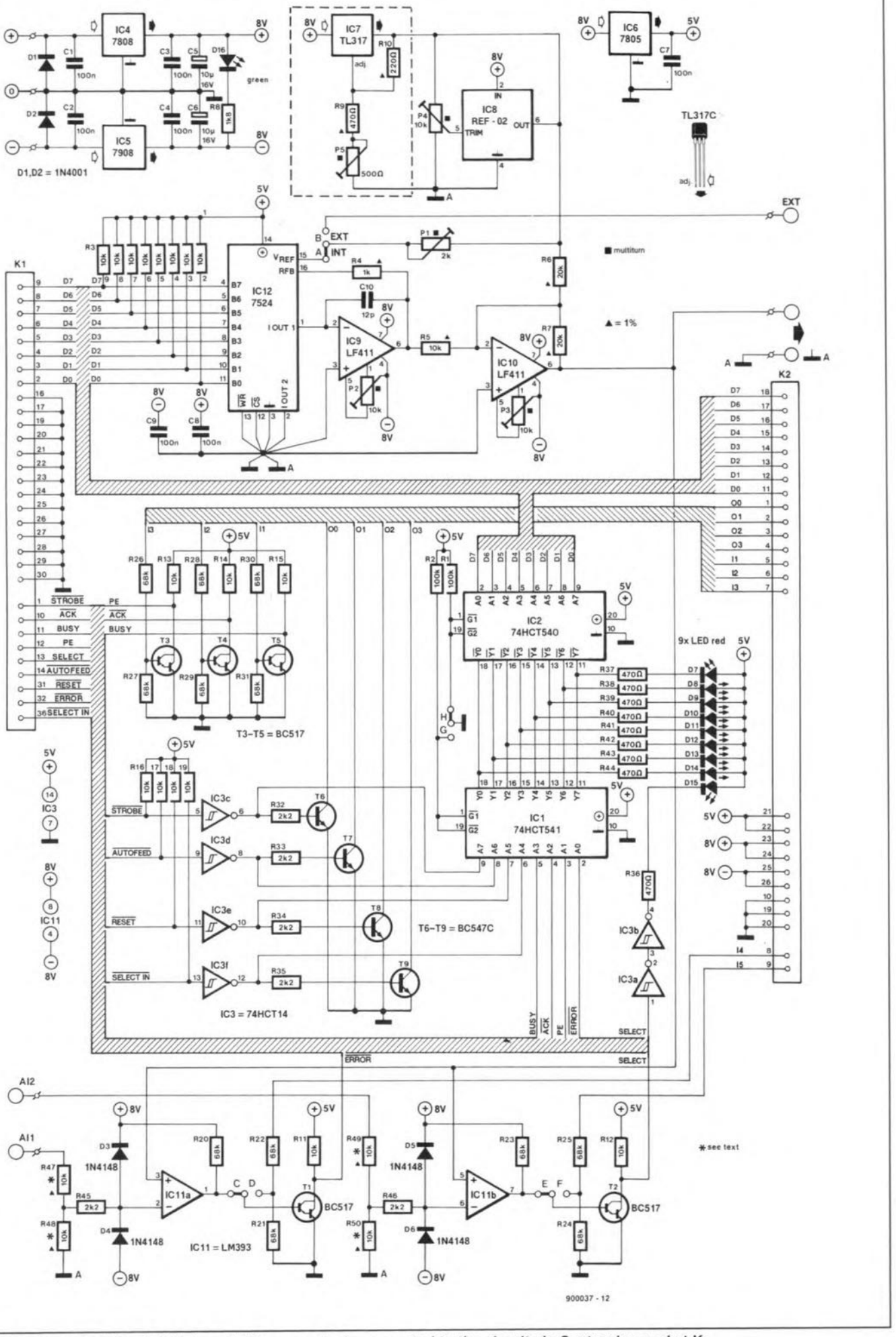


Fig. 2. Circuit diagram of the A-D/D-A card. The computer is connected to the circuit via Centronics socket K1.

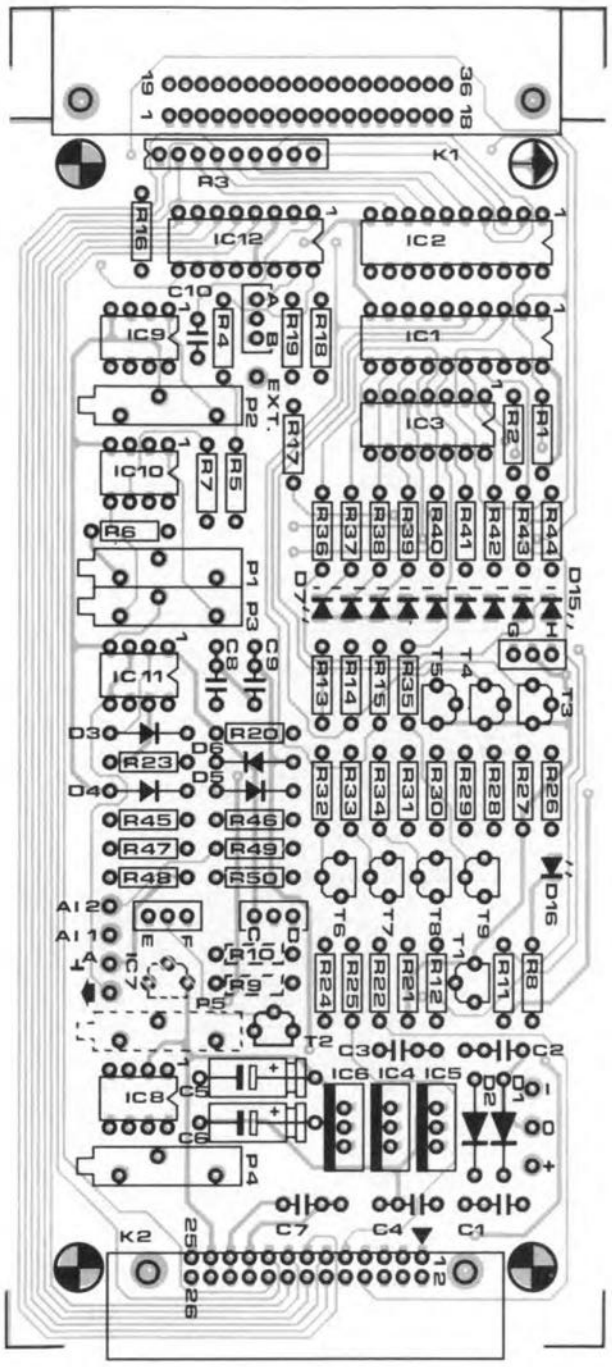


Fig. 3. Component mounting plan of the double-sided, through-plated PCB.

COMPONENTS LIST

Resistors:

2	100k	R_1;R_2
1	10k 8-way SIL	R_3
1	1k0 1%	R_4
5	10k 1%	R_5;R_{47};R_{48};R_{49}; R_{50}
2	20k 1%	R_6;R_7
1	1k8	R_8
1	470Ω 1%	R_9 **
1	220Ω 1%	R_{10} **
9	10k	R_{11} – R_{19}
12	68k	R_{20} – R_{31}
6	2k2	R_{32} – R_{35};R_{45};R_{46}
9	470Ω	R_{36} – R_{44}
1	2k multiturn preset	P_1
3	10k multiturn preset	P_2;P_3
1	10k multiturn preset	P_4 ***
1	500Ω multiturn preset	P_5 **

Capacitors:

6	100n	C_1 – C_4;C_7; C_8;C_9
2	10µF 16 V	C_5;C_6
1	12pF	C_{10}

Semiconductors:

2	1N4001	D_1;D_2
4	1N4148	D_3 – D_6
9	LED 3mm red	D_7 – D_{15}
1	LED 3mm green	D_{16}
5	BC517	T_1 – T_5
4	BC547C	T_6 – T_9
1	74HCT541	IC_1
1	74HCT540	IC_2
1	74HCT14	IC_3
1	7808	IC_4
1	7908	IC_5
1	7805	IC_6
1	TL317	IC_7 **
1	REF-02	IC_8 ***
2	LF411	IC_9;IC_{10}
1	LM393	IC_{11}
1	PM7524 (PMI) or AD7523 (Analog Devices)	IC_{12}

Miscellaneous:

1	36-way Centronics socket for PCB mounting; angled pins	K_1
1	26-way header; angled pins; with eject handles	K_2
1	printed-circuit board	900037
1	control program on disk	1421

** not fitted when IC_8 is used
*** not fitted when IC_7 is used

First, adjust either P_5 (reference: TL317) or P_4 (reference: REF-02) until a reference of 5.00 V is obtained. Next, cancel the off-set voltage of IC_9 by adjusting P_2. Set the current that flows into the V_{ref} input by adjusting P_1. Finally, adjust P_3 to cancel the off-set voltage of IC_{10}.

Writing data to the DAC is simple: in nearly all cases, this involves loading one register with the desired value. One statement,

```
PORT [DATAREG] := DATA;
```

is sufficient in Turbo Pascal. Since U_{ref} = 5 V, the relation between the value of the dataword and the resultant analogue output voltage is expressed by

$$U_o = 5\,(\text{data}-128)/128 \quad [\text{V}]$$

Data '0' therefore produces –5 V; data '80_H' 0 V; and data 'FF_H' +4.961 V. Since the circuit is capable of producing 0 V, the highest output voltage remains 39 mV below +5 V. A slightly different setting-up procedure allows you to reach +5 V, but this in turn makes it impossible to achieve 0 V, which can not be approximated at a difference better than 39 mV or ½LSB at data = 80_H. In practice, it is easier to state a voltage and calculate the corresponding DAC data from

$$\text{data} = 128\,(U_o/5+1)(-5 \le U_o \le 4.961)$$

where 'data' is rounded off to give a whole number. Both the checking of U_o and the required conversion computation to provice the necessary bit combination for the

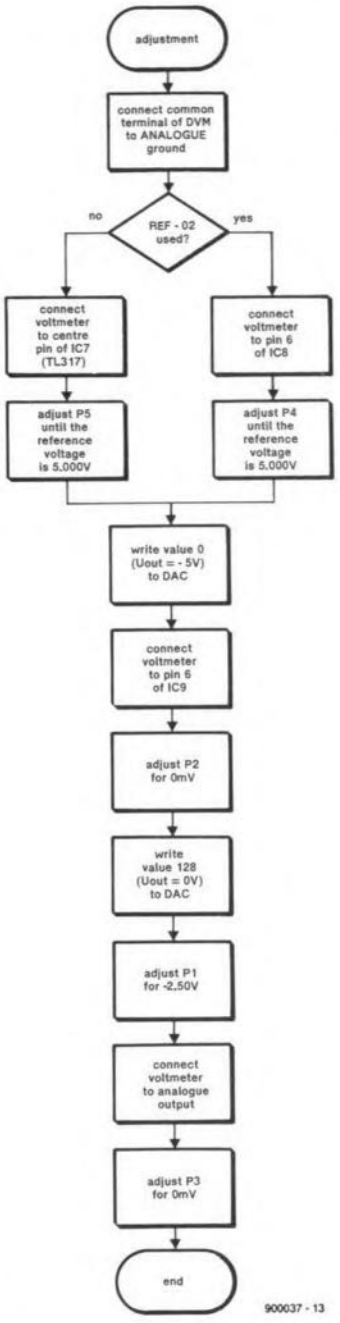


Fig. 4. Flow diagram of the adjustment procedure.

DAC may be included in the routine that controls the voltage setting.

A-D conversion

As already noted, this is effected on the basis of successive approximation. The unknown analogue voltage is approximated by comparing it to analogue voltages generated by the DAC, whose resolution causes the longest (worst-case) approximation to require the maximum number of steps, 2^8 or 256. The use of a different approach may reduce this number to 8, or the width (in bits) of the data input of the DAC. Figure 5 shows the flow-chart of the D-A routine. This procedure is invoked with two variables: the input channel and the attenuation (for which variable K must be greater than 1).

```
external variables:
Ui, input,
K (= input attenuation)
begin procedure A-D conversion
intermediate value := 0
bit position := 7 down to 0
    DAC := intermediate value OR (SHL 1 bit position)
    wait (DAC and comp. settling time)
    comparator number (input) <> 0 (Ui < UDAC)
    no \ / yes
       intermediate value := intermediate value OR (SHL 1
       bit position)
Ui := Uref * K * (intermediate value - 128)/128
end of procedure
```

Fig. 5. Flow diagram of the successive approximation routine

```
 Volume in drive A is ESS_1421
 Directory of  A:\

CENTR&ME EXE     41328   2-12-90    3:06p
CIOPUBLI PAS      4241   3-16-90   10:32a
CIOPUBLI TPU      2816   2-20-90    9:57a
EXAMPLE  EXE      8656   2-20-90    9:59a
CONFIG   DAT       386   3-16-90   10:35a
EXAMPLE  PAS      1697   3-16-90   10:39a
        6 File(s)     300032 bytes free
```

Fig. 6. Directory of the PC-MSDOS program disk, number 1421, for the project.

Variable 'data' is used for intermediate data storage, starting with value 0. Next, a for-next loop is entered. This is passed eight times, during which the A-D conversion is effected. A program within the loop checks for each bit whether this must become 0 or 1. The most significant bit is treated first with an intermediate value of 0 (all bits are 0). The sum of these two is obtained with the aid of an OR function and is subsequently written to the DAC. When the relevant comparator indicates that the voltage is too high, the corresponding bit in the intermediate value must remain at 0. When the voltage is too low, the same bit must become 1. All eight bits are treated in this manner by shifting the 1 to the left (SHL). After the eight steps, the input voltage may be calculated on the basis of the intermediate value.

Short wait times are inserted between the write operation to the DAC and the read operation to the comparator. This is done to allow for the response time of the ICs. This wait time is so short, however, as to make the use of standard time functions in the PC impossible, since their minimum delay of about 1 ms is much too long. Hence, a for-next loop is used. An obvious problem caused by this approach, dependency on the clock speed of the computer, may have to be resolved empirically with different loop repetitions. In many cases, a single repetition is sufficient to establish the required wait time. In that case, the loop may be replaced by one or more useful statements of your own. A statement like 'repeat until true' does effectively nothing but last a number of clock cycles and does not require a previously declared auxiliary variable.

Test program

The diskette supplied for this project contains the basic routines in a Turbo-Pascal unit, both in the form of compiled code and source text. Also on the disk is an auxiliary program for testing and adjusting the card. This program, CENTR&ME.EXE, searches for a file called CONFIG.DAT, which contains five numbers that indicate the printer port number, the attenuation on input channel 1, the attenuation on input channel 2, the reference voltage, and the number of iterations in the wait loop, in that order. This configuration file may be edited to individual requirement with the aid of any ASCII compatible word processor, like EDLIN or the one in SideKick or PCTools. The numbers are separated either by a comma or a space. The file also contains a few lines to explain the meaning of the numbers. These lines are comment and have nothing to do with the actual operation of the test program, which, incidentally, may be run without the A-D/D-A card connected to the computer. This is particularly useful to become acquainted with its structure and commands. ■

SCIENCE & TECHNOLOGY

IMAGE SEGMENTATION

goodby

M.S. Kishore

The aim of this article is to give a basic idea of Image Segmentation techniques and how they are applied to a given image. Several techniques are described: it is shown that the use of each of these depends on the specific requirement.

Segmentation is a technique for splitting an image into regions that hopefully represent the surfaces in the real world where the image originated. Its purpose is to create, by algorithms, a symbolic representation of the scene rather than the pixel grid we normally look at. If, for instance, we want to express a scene consisting of a circle of radius r, centre (a, b), intersecting a square of side s, centred at (x, y), we want the segmentation process to dispense with the usual pixel-based information and give us the parameters of the scene in a more concise and meaningful way.

Segmentation is one of the most important elements in automated image analysis because it enables objects or other aspects of interest to be extracted from an image for subsequent processing, such as description and recognition.

Segmentation algorithms are generally based on one of the two basic properties of grey-level values: *discontinuity* and *similarity*. An image that is based on abrupt changes in grey level is classed in the first category.

The principal areas of interest in this category are the detection of isolated points and the detection of lines and edges in an image.

The main approaches in the second category are based on thresholding, region growing and splitting and merging.

The concept of segmenting an image based on discontinuity or similarity of the grey-level values of its pixels is applicable to both static and dynamic (time-variable) images. In the latter case, however, motion can often be used as a powerful cue to improve the performance of a segmentation algorithm.

Point detection

The problem of detecting and then segmenting isolated points in an image applies in noise removal and particle analysis. The basic mask used for detecting isolated points in an image is

−1	−1	−1
−1	8	−1
−1	−1	−1

At each mask location, we compute the vector product

−×1−×2−×3−×4+8×5−×6−×7−×8−×9.

In an area of constant grey level, the result of this operation would have been zero. Since in the example the image is centred at an isolated point (×**5**), where the intensity is greater than at the other locations, the result is greater than zero.

In practice, where one is interested only in strong responses, we say that an isolated point, whose intensity is significantly different from the background, has been detected if the vector product is greater than some non-negative threshold.

Line detection

The next level of complexity involves the detection of lines in an image. Consider the mask

−1	−1	−1
2	2	2
−1	−1	−1

If this mask were moved around on an image, it would respond more strongly to horizontal lines; with constant-level background, the maximum response would obtain when the line passed through the middle row of the mask.

A similar experiment would reveal that this mask

−1	−1	2
−1	2	−1
2	−1	−1

would respond best to lines at +45°; this mask

−1	2	−1
−1	2	−1
−1	2	−1

to vertical lines; and this mask

2	−1	−1
−1	2	−1
−1	−1	2

to lines at –45°.

The direction of the lines may also be established by noting that the preferred direction of each mask is weighted by a larger coefficient (i.e., 2) than other possible directions.

Edge detection

Although point and line detection certainly are elements of any discussion on segmentation, edge detection is by far the most commonly used approach for detecting meaningful discontinuities in grey level. The reason for this is that isolated points and thin lines are not frequent occurrences in most applications of practical interest.

In this approach, we define an edge on the boundary between two regions with relatively distinct grey-level properties. It is assumed that the two regions are sufficiently homogeneous for the transition from one to the other to be determined on the basis of grey-level discontinuities alone. When this assumption is not valid, line or point techniques are generally more suitable than edge detection.

Most of the edge detection techniques involve the computation of a local derivative operator.

The first derivative of an edge is zero in all regions of constant grey level and assumes a constant value during a grey level transition.

The second derivative is zero in all locations, except at the onset and termination of grey-level transition.

It is evident that the magnitude of the first derivative can be used to detect the presence of an edge, while the sign of the second derivative may be used to determine whether an edge pixel lies at the dark (background) or light (object) side of the edge.

The sign of the second derivative is positive, for instance, for pixels lying at the dark side of both the leading and trailing edges of the object, while the sign is negative for pixels at the light side of these edges.

Similar comments apply to the case of a dark object on a light background.

The direction of the gradient vector is also important.

Gradient operation

As indicated, the gradient of an image $f(x, y)$ at location (x, y) is defined as the two-dimensional vector

$$\mathbf{G}[f(x, y)] = [\mathbf{G}x\ \mathbf{G}y]$$

It is well-known from vector analysis that the vector $\mathbf{G}$ points in the direction of maximum rate of change of f at location (x, y). For edge detection, we are interested in the magnitude of this vector, generally referred to simply as the gradient and denoted by $\mathbf{G}[\mathbf{f}(x, y)]$, where

$$\mathbf{G}[\mathbf{f}(x, y)] = [\mathbf{G}x + \mathbf{G}y].$$

This quantity is equal to the maximum rate of increase $f(x, y)$ per unit distance in the direction of $\mathbf{G}$. The direction of the gradient vector is also an important quantity. If (x, y) represents the direction angle of $\mathbf{G}$ at location (x, y), it follows from vector analysis that

$$\alpha(x, y) = \tan(\mathbf{G}x/\mathbf{G}y),$$

where the angle is measured with respect to the x-axis.

Consider the sub-image area

×1	×2	×3
×4	×5	×6
×7	×8	×9

where ×5 represents the grey level at location (x, y) and the other mask locations represent the grey levels of the neighbours of $f(x, y)$. We define the component of the gradient vector in the x direction as

$$\mathbf{G}x = (\times 7 + 2\times 8 + \times 9) - (\times 1 + 2\times 2 + \times 3);$$

and in the y direction as

$$\mathbf{G}y = (\times 3 + 2\times 6 + \times 9) - (\times 1 + 2\times 4 + \times 7).$$

The use of a 3×3 area in the computation of the gradient has the advantage of increased smoothing over 2×2 operators, tending to make the derivative operations less sensitive to noise.

Weighting the pixels closest to the centre by 2 also produces additional smoothing. It is possible to base gradient computations over larger neighbourhoods (Kirsch), but 3×3 neighbourhoods are by far the most popular because of the advantage in computational speed and modest hardware requirements.

It follows from the discussion in the previous two sections that $\mathbf{G}x$ can be computed by using the mask

$\mathbf{G}x =$

–1	–2	–1
0	0	0
1	2	1

or

$\mathbf{G}y =$

–1	0	1
–2	0	2
–1	0	1

These two masks are commonly referred to as the SOBEL operators.

The responses of these operators at any point (x, y) are combined to obtain the gradient at that point. Convolving these masks with an image $f(x, y)$ yields the gradient at all points in the image: the result is often referred to as a GRADIENT image.

Another useful approximation, called the ROBERTS gradient, makes use of the cross differences given by

$$\mathbf{G}[f(x, y)] \equiv |f(x, y) - f(x + 1, y - 1)| + |f(x + 1, y) - f(x, y - 1)|$$

The LAPLACIAN is a second-order derivative operator, which can be implemented by convolving the mask

0	1	0
1	–4	1
0	1	0

Although the LAPLACIAN responds to transitions in intensity, it is seldom used by itself for edge detection. The reason for this is that, being a second derivative operator, the LAPLACIAN is typically sensitive to noise. It is, therefore, usually relegated to the secondary role of serving as a detect for establishing whether a given pixel is at the dark or the light side of an edge.

The vector formation for the detection of points, lines and edges has the important advantage that it can be used to detect combinations of these features. The technique was developed by Frei and Chen. The nine associated masks are shown on the next page: the first four are suitable for detecting edges, the second set of four represents templates suitable for line detection and the last mask is proportional to the average of the pixels in the region at which the mask is located in an image.

Gradient image threshold

If we take the threshold of a gradient image at a moderately grey level, we find both object and background below threshold and most edge points above threshold.

Kirsch has developed a method that makes use of this phenomenon. In this, the gradient image is first given a moderately low grey level threshold to identify the object and the background, which are separated by bounds of edge points. Then, the threshold is increased gradually, which causes both the object and the background to grow. When they touch, they are not allowed to merge, but the points of contact, which define the boundary, are noted. This method is computationally expensive, but it tends to to produce maximum gradient boundaries while avoiding many of the problems of gradient tracking bugs. For multiple object images, the segmentation is correct if, and only if, it is carried out correctly by the initial thresholding step.

The edge operater developed by Kirsch also detects the presence of edges. It functions as follows. Each 3×3 neighbourhood is convolved with eight kernels. The maximum value over each of the eight orientations is taken as the output value.

−1	√2	1
0	0	0
−1	−√2	−1

1	0	−1
√2	0	−√2
1	0	−1

0	−1	√2
1	0	−1
−√2	1	0

√2	−1	0
−1	0	1
0	1	−√2

0	1	0
−1	0	−1
0	1	0

−1	0	1
0	0	0
1	0	−1

1	−2	1
−2	4	−2
1	−2	1

−2	1	−2
1	4	1
−2	1	−2

1	1	1
1	1	1
1	1	1

Masks used in the Frei-Chen technique.

Segmentation by thresholding

Thresholding is a particularly useful technique for scenes containing solid objects resting on a contrasting background. It is computationally simple and never fails to define disjoint regions with closed connected boundaries. When using this technique for image segmentation, one assigns all pixels at or above the threshold; all those with a grey level below the threshold fall outside the object. The boundary is then a set of interior points, each of which has at least one neigbour outside the object.

Thresholding works well if the grey level of the object is uniform and the object rests on a background of a different, but also uniform, grey level. If the object differs from its background by some property other than grey level (such as texture), one can first use an operation that converts that property to grey level.

In the simplest implementation of boundary location by thresholding, the value of the threshold grey level is held constant throughout the image. If the background grey level is reasonably constant throughout the image, and the object has a roughly equal contrast against the background, a fixed global threshold will usually work well, provided a correct threshold grey level was selected.

Adaptive threshold: in many cases the background grey level is not constant and the object contrast varies with the image. In such cases, a threshold that works well in one area might work poorly in other areas of the image. It is then convenient to use a threshold grey level that is a slowly varying function of the position in the image.

Optimal threshold: unless the object in the image has very steep sides, the exact value of the threshold grey level can have a considerable effect on the boundary position and overall size of the extracted object. For this reason, we need an optimal, or at least consistent, method for establishing the threshold. An image containing an object on a contrasting background has a bimodel grey level histogram. The two peaks correspond to the relatively larger number of points inside and outside the object. The dip between the peaks corresponds to the relatively few points around the edge of the object and is commonly used to establish the threshold grey level.

+5	+5	+5
−3	0	−3
−3	−3	−3

−3	+5	+5
−3	0	+5
−3	−3	−3

−3	−3	+5
−3	0	+5
−3	−3	+5

−3	−3	−3
−3	0	+5
−3	+5	+5

−3	−3	−3
−3	0	−3
+5	+5	+5

−3	−3	−3
+5	0	−3
+5	+5	−3

+5	−3	−3
+5	0	−3
+5	−3	−3

+5	+5	−3
+5	0	−3
−3	−3	−3

Results of convolving a 3×3 neighbourhood with eight kernels.

Region growing by pixel aggregation

Region growing is a process that groups pixels or sub -regions into larger regions. In its simplest form, pixel aggregation, we start with a set of 'seed' points and from these grow regions by appending to each sub-point those neighbouring pixels that have similar properties, such as grey level, texture, and colour.

For instance, in applications of infrared imaging, hot targets appear brighter than the background. Choosing the brightest pixels is then a natural starting point for a region-growing algorithm.

The selection of similar criteria depends not only on the problem under consideration, but also on the type of image data available. For example, the analysis of satellite imagery is dependent mainly on the use of colour. The analysis would be much more difficult if only monochrome images were available.

All boundaries between adjacent regions are examined. A measure of the boundary strength is computed from the differences of the averaged properties of the adjacent regions. A given boundary is strong if the properties differ significantly on either side of the boundary and weak if they do not.

Strong boundaries are allowed to stand, while weak boundaries are dissolved and the adjacent regions merged. The process is repeated by first computing the object membership properties of the enlarged region again and then dissolving the weak boundaries. The process is then continued until a point is reached where the boundaries are weak enough to be dissolved.

Region splitting and merging

The region growing process starts from a set of 'seed' points. An alternative is to sub-divide an image inititally into a set of arbitrary, non-joining regions and then merge or split the region in an attempt to satisfy the requirements discussed earlier.

Given a digital image containing several objects, the pattern process consists of three major phases. The first of these is object isolation, in which each object must be found and its image isolated from the rest of the scene. The second is called feature extraction. The features are formed by a set of measurable properties. The extraction phase measures these properties from which it produces a set of measurements called the feature vector. This drastically reduced amount of information represents all the knowledge on which the subsequent classification must be based. The third phase is object classification, which is merely a decision as to which class the object belongs.

When a human observer views a scene, the neurological process that takes place in the retina and the optic cortex essentially segments the scene for him. This is done so effectively that he sees not a complex scene, but rather something he thinks of as a collection of objects. With digital processing, however, we must isolate the objects in the image by breaking up that image into sets of pixels, each of which is the image of one object. ■

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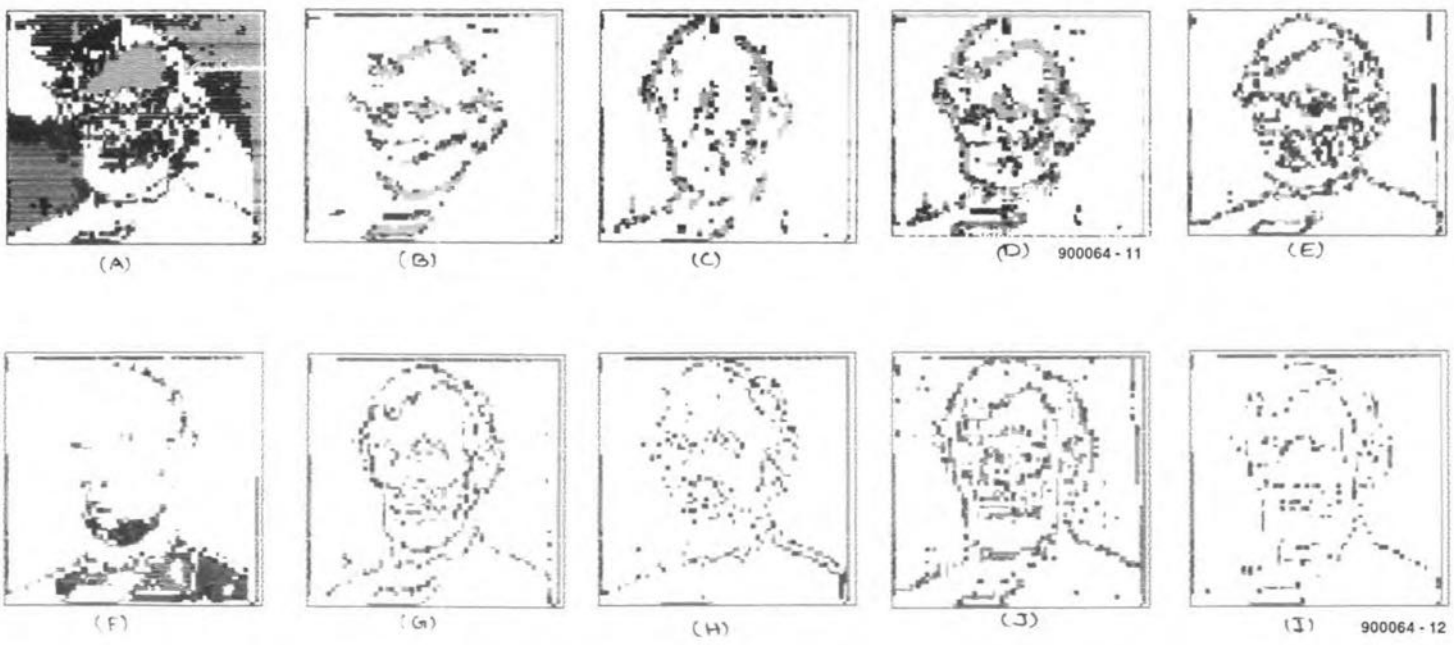


(A) Original 64×64 image; (B) after applying the Sobel operator Gx; (C) after applying the Sobel operator Gy; (D) after applying the Sobel operator G; (E) after applying Roberts gradient operator; (F) after applying horizontal line detection mask; (G) after applying vertical line detection mask; (H) after applying Laplacian operator; (I) and (J) after applying edge detection.

BUDGET SWEEP/FUNCTION GENERATOR

T. Wigmore

This month we add yet another item to our series of budget test instruments. The signal generator described has a built-in sweep function which is ideal for audio measurements. Based on the well-known XR2206 function generator IC with very few external components, the instrument offers a hard-to-beat price/performance ratio.

It is not wise to disregard the XR2206 from Exar when designing an all-round function generator. The device is versatile like no other, and guarantees a fairly simple circuit for the given application. Furthermore, its cost makes any attempt at designing an equivalent circuit based on discrete components a waste of time, while its output signal distortion figures are not spectacular, but none the less low compared to those of a competitive chip like the 8038.

For use as a basic function generator, the XR2206 requires only a handful of passive parts. The frequency adjustment and the sweep function are simple to implement by the addition of one dual opamp and three transistors. The output amplifier of the instrument also follows the general line of comprising of as few components as possible: only one power opamp is required.

The generator

The XR2206 forms the heart of the circuit (see Fig. 1). With the external components configuration used here, the IC supplies a sine-wave and a triangular wave at output pin 2. The d.c. operating point is set to half the supply voltage (6 V at pin 3) by potential divider R_{15}-R_{16}. The resistance at the potential divider junction, 16.5 kΩ, and the voltage at the AM input, pin 1, (0 V) determine the amplitude of the output signal.

The waveform selection is effected by one contact of S_4. In the position shown, resistor R_{17} is connected to pin 14 of the XR2206. The current flow through R_{17} enables the IC to convert the triangular signal into a sine-wave. The value of R_{17} determines to what extent the inflection points of the triangle are rounded to give a sine-wave. For the sake of simplicity, a fixed resistor instead of the expected (multiturn) preset is used to set this current.

When the contact of S_4 is opened, pin 2 supplies a triangular signal whose peak amplitude is twice that of the sine-wave. The rectangular wave is supplied via pin 11. This open-collector output of the XR2206 is pulled to ground at the generator pulse rate by an n-p-n transistor. Voltage divider R_{18}-R_{19}-R_{20} at pin 11 sets the amplitude of the rectangular wave. The maximum and minimum voltage le-

MAIN FEATURES

- Frequency ranges: 3 (10 Hz – 20 kHz) or 4 (10 Hz – 200 kHz)
- Sweep frequency: 0.1 Hz – 100 Hz
- Sweep range: 0 – 1:20
- Sweep output: 5 V_{pp}; sawtooth; Z_o = 1 kΩ
- Waveforms: sine-wave, triangle, rectangle
- Distortion (sine-wave): 0.5% typ. (in AF range)
- AC output: all waveforms; Z_0 = 50 Ω, short-circuit resistant
- Output amplitude (R_L = 50 Ω):
  0.1 mV_{pp} – 1 V_{pp} (sine-wave)
  0.1 mV_{pp} – 2.5 V_{pp} (triangle)
  0.1 mV_{pp} – 1.5 V_{pp} (rectangle)
- Output amplitude (R_L = 600 Ω):
  0.1 mV_{pp} to 1.8 V_{pp} (sine-wave)
  0.1 mV_{pp} – 4.5 V_{pp} (triangle)
  0.1 mV_{pp} – 3 V_{pp} (rectangle)
- Current consumption: approx. 100 mA at 12 V

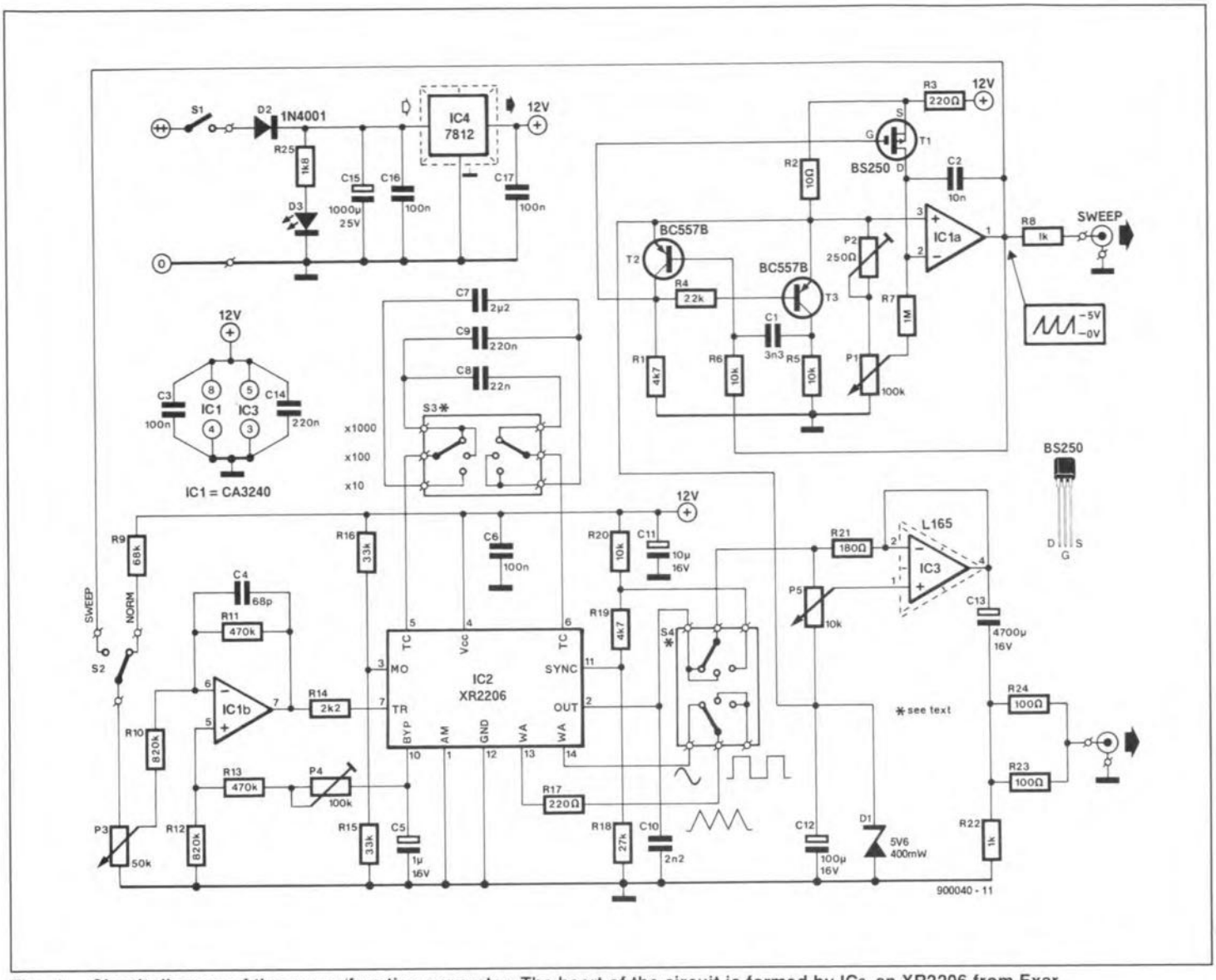


Fig. 1. Circuit diagram of the sweep/function generator. The heart of the circuit is formed by IC2, an XR2206 from Exar.

vels are 9.1 V and 3.8 V respectively. This swing is close to the optimum drive margin of the power opamp that follows the XR2208.

The second contact of S4 selects either of the two IC outputs and passes the relevant waveform to the output amplifier.

Frequency control

The frequency of the signal supplied by the XR2206 is determined by two factors: the capacitance between pin 5 and pin 6, and the current drawn from pin 7.

The capacitance is determined by the three capacitors selected by the frequency range switch, S3. A fourth range (up to 200 kHz) may be added by providing an extra switch position and a capacitor of 2.2 nF (see the section on construction further on).

Pin 7 of the XR2206 supplies a temperature-compensated reference voltage of 3 V, which is also available at pin 10, where it is decoupled by C5. The voltage at pin 3 is loaded by a resistor, R14, and the output of opamp IC1b. Hence, the output voltage of the opamp determines the current through R14 and with it the signal frequency, *f*:

$$f = I_{R14}/3C$$

where I_{R14} is in ampères. Factor *C* is the capacitance (in farads) between pins 5 and 6.

Frequency and frequency sweep adjustment are effected manually by potentiometer P3 at the –input of IC1b. When S2 is set to the 'normal' position, P3 and R9 form a potential divider that limits the voltage at the wiper to a value between 0 V to 5 V. Resistors R10-R11 set the amplification of the inverting opamp to a value that results in output voltages of virtually 0 V and 3 V with P3 set to maximum and minimum (wiper to ground) respectively. The d.c. operating point —and with it the start of the frequency range — is determined by P4-R13 and R12, which ensure that a part of the 3-V reference voltage is applied to the non-inverting input of IC1b.

Sweep function

When the generator frequency is set manually, a fixed resistor, R9, provides the direct voltage to potentiometer P3. When S2 is switched to the other position, however, P3 is supplied with the output voltage of a ramp generator. In this mode, the potentiometer sets the swept frequency range rather than the frequency itself. In other words, it determines to what extent (in Hz/V) the ramp generator can change the set generator frequency.

The ramp generator is formed by opamp IC1a and integrator C2. The integration time is set by the voltage at the wiper of P1: the higher the voltage, the faster the capacitor is charged, and the faster the sawtooth voltage rises. Potentiometer P1 allows the sweep time to be set to a value between 10 ms and 10 s. The maximum time is calibrated by preset P2, which also serves as an off-set compensation for IC1a.

The rise of the sawtooth voltage at the integrator output is ended via T2 and T1. The emitter of T2 is held at a reference potential provided by zener diode D1. The transistor conducts, and T1 and T3 are kept off, as long as its base voltage is below the reference. As soon as the sawtooth reaches a level of about 0.5 V below the reference voltage, T2 is briefly turned off, so that its collector voltage is pulled to about 0 V via R1. As a result, T3 conducts and resets the integrator by making the inverting input of IC1b positive with respect to the non-in-

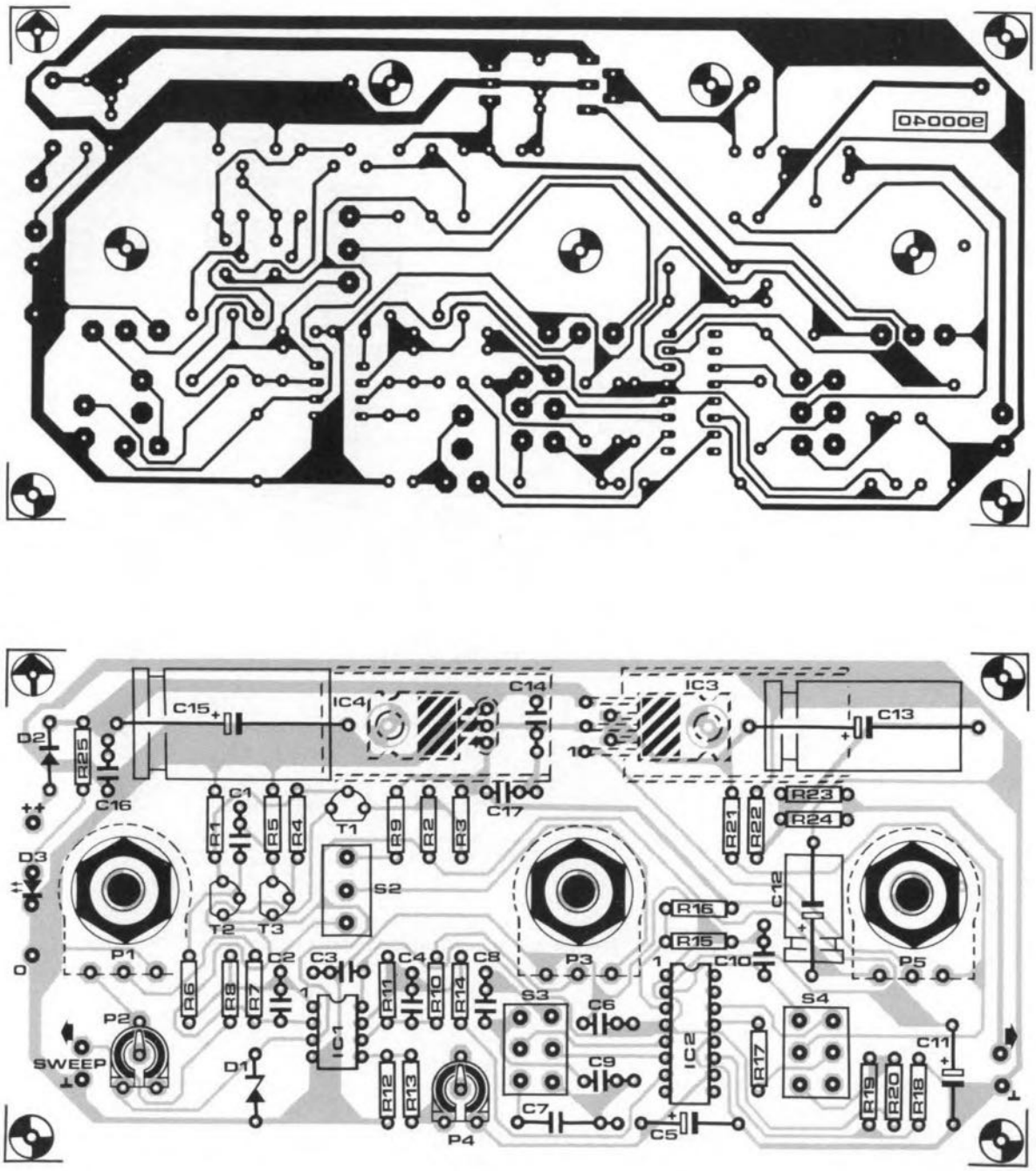


Fig. 2. Track layout (mirror image) and component mounting plan of the single-sided printed circuit board for the generator.

verting input. This is achieved with the aid of T_1. In the monostable formed by T_2-T_3, C_1 ensures that the integration capacitor is discharged rapidly to provide the trailing edge of the sawtooth. The reference voltage provided by D_1 thus determines the amplitude of the sawtooth voltage that sweeps the frequency of the function generator.

The sawtooth voltage is also available at a separate sweep output on the instrument. Resistor R_8 sets the output impedance to about 1 kΩ. The sweep output is short-circuit resistant and may be used for driving the X amplifier of an oscilloscope for swept-frequency measurements.

Output amplifier

The Type L165 opamp used in the output amplifier is capable of providing ample output current at a reasonable price. The IC is used in a conservatively rated configuration and is therefore not likely to actuate its internal overheating protection. The power opamp is wired as an non-inverting buffer (voltage follower), so that the amplitude and phase of the output signal correspond to those of the input signal at the wiper of amplitude control P_5. An electrolytic capacitor, C_{13}, is required to decouple the d.c. component at the output since a non-symmetrical supply is used. The parallel resistor combination at the output is not strictly required for overload protection (which the L165 provides by itself). It does, however, limit the output current to a safe value. At the same time, it sets the generator output impedance to 50 Ω, which is a commonly used value on test equipment.

COMPONENTS LIST

Resistors:

2	4k7	R1;R19
1	10Ω	R2
2	220Ω	R3;R17
1	22k	R4
3	10k	R5;R6;R20
1	1M0	R7
2	1k0	R8;R22
1	68k	R9
2	470k	R11;R13
2	820k	R10;R12
1	2k2	R14
2	33k	R15;R16
1	27k	R18
1	180Ω	R21
2	100Ω	R23;R24
1	1k8	R25
1	100k lin. potentiometer	P1
1	250Ω preset H	P2
1	50k lin. potentiometer	P3
1	100k preset H	P4
1	10k lin. potentiometer	P5

Capacitors:

1	3n3	C1
1	10n	C2
4	100n	C3;C6;C16;C17
1	68p	C4
1	1µ0 16V axial	C5
1	2µ2 MKT	C7
1	22n	C8
2	220n	C9;C14
1	2n2	C10
1	2n2 (optional)	C16
1	10µF 16V axial	C11
1	100µF 16V axial	C12
1	4700µF 16V axial	C13
1	1000µF 25V axial	C15

Semiconductors:

1	5V6 400mW zener diode	D1
1	1N4001	D2
1	LED	D3
1	BS250	T1
2	BC557B	T2;T3
1	CA3240E	IC1
1	XR2206	IC2
1	L165	IC3
1	7812	IC4

Miscellaneous:

1	miniature SPST switch	S1
1	miniature SPDT switch	S2
2	2-pole 3-way switch (Knitter MTA206PA or C&K 7211) (S3 may be replaced by a miniature 1-pole 4-way rotary switch)	S3;S4
2	BNC socket	K1;K2
2	TO-220 style heat-sink	
1	printed-circuit board	900040
1	front-panel foil	900040-F

Construction

The single-sided printed-circuit board on which the generator is constructed is shown in Fig. 2. Population of the PCB is straightforward with the possible exception of the following points:

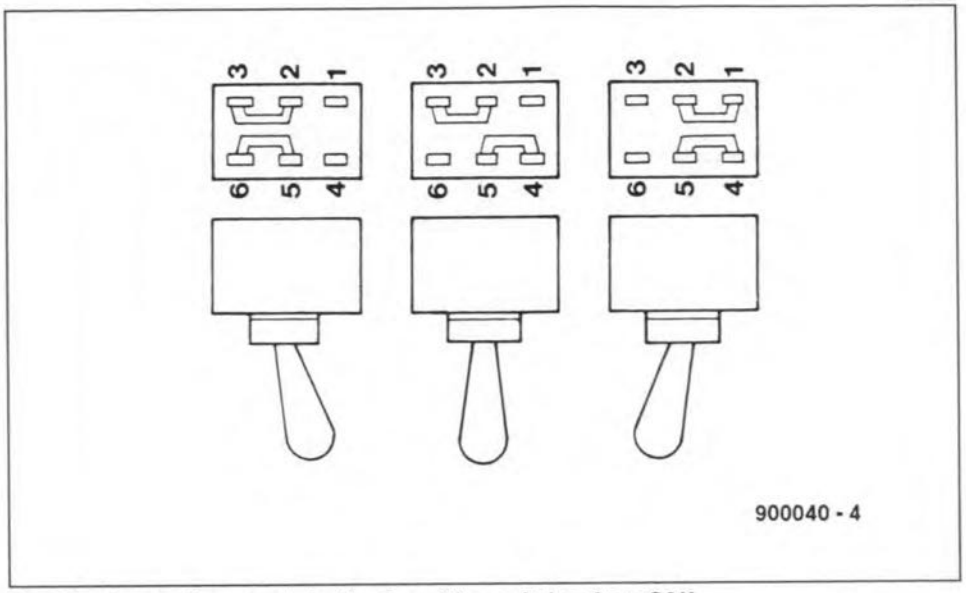


Fig. 3. Connections made in the 3-position switches from C&K.

- The spindles of potentiometers P1, P2 and P3 are inserted from the track side of the PCB to enable the nuts on the shafts to be locked at the component side. Use short wires to connect the potentiometer terminals to the relevant copper tracks.
- As shown in Fig. 5, IC3 and IC4 are fitted at the track side of the board. Do observe their correct orientation and the electrical insulation of the heat-sinks.
- Switches S1, S3 and S4, and the BNC sockets are mounted on the front panel. Their positions correspond to those provided on the overlay printed on the ready-made circuit board. The connections are made in short lengths of light-duty insulated wire.

It is not strictly necessary to use IC sockets, although the small additional investment may prove worth while if a faulty IC is suspected. Since the instrument has its own single-phase rectifier, smoothing capacitor and 12-V voltage regulator, it may be powered from an unregulated AC or DC supply with an output of 15 V to 18 V. If a transformer is used, observe the necessary safety precautions as regards insulation of the mains voltage and the fuse rating.

Setting up

It is recommended to adjust the completed printed-circuit board before it is fitted into the enclosure. This means that the switches and the output sockets have to be connected provisionally.

Apply power and allow a few minutes for the circuit to warm up. Set S2 to NORMAL, and P3 to a frequency roughly at the centre of a range, e.g., 100 Hz. Connect a frequency meter to the signal output and adjust P4 until the measured frequency equals that set on the scale.

If you do not have access to a frequency meter to perform this adjustment, use the beat frequency method instead. Feed the 100 Hz signal obtained with the aid of a small mains transformer, a bridge rectifier and a series network of a 100-Ω resistor and a 100-µF capacitor, to a loudspeaker. Drive another loudspeaker with the generator output signal. Listen to the two signals and adjust P4 for zero frequency difference. This method gives quite accurate results (for use with a 60-Hz mains, set the generator to 120 Hz).

The adjustment of the sweep function is carried out at the greatest sweep time, 10 s. Turn P1 fully counter-clockwise and connect an analogue voltmeter or a LED to the sweep output of the instrument. Adjust P2 until a time period of 10 s is obtained.

Tips and options

In the basic arrangement, the waveform and frequency range selection are effected with 3-position miniature switches from C&K. The switching configurations are shown in Fig. 3. In the case of S3, the use

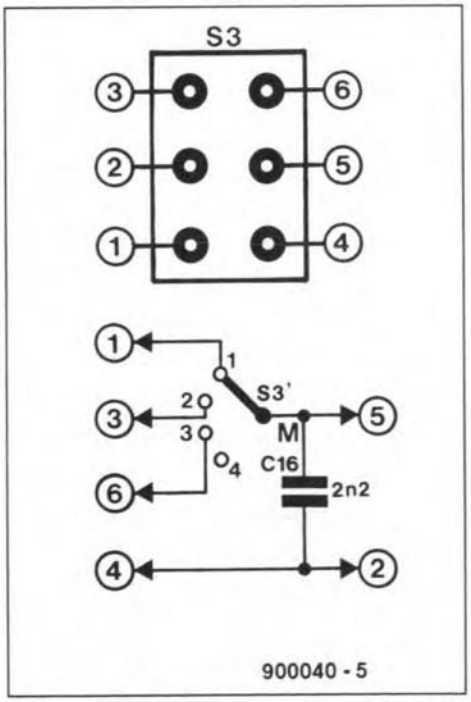


Fig. 4. Alternative switch connection which enables the frequency range of the generator to be extended to about 200 kHz.

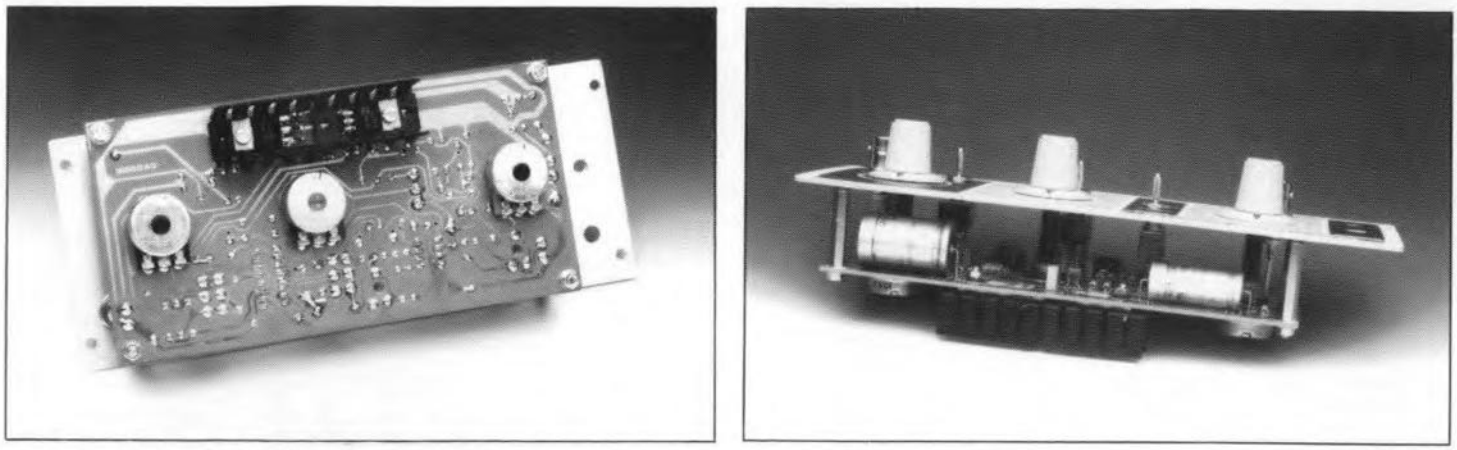


Fig. 5. Completed PCB-front panel assembly seen from the PCB track side (left) and from the side (right).

of a switch that has only three positions limits the frequency range of the instrument to about 20 kHz. A fourth range, which may be desirable in a number of cases, may be added by replacing the toggle switch with a small, four-position, rotary switch, which is wired as shown in Fig. 4. The numbers 1 to 6 on the overlay mark the connections of the terminals of S_3. To create a 200 kHz range, solder an additional 2.2 nF capacitor, C_{16}, to the centre terminals, numbers 2 and 5, and solder a wire between terminals 2 and 4. Next, connect the contacts (1, 2 and 3) and the pole of the rotary switch to the PCB terminals 1, 3, 6 and 5.

As already noted, the value of R_{17} determines the shape of the sine-wave. At relatively high generator frequencies, it may be useful to replace the resistor by a 500-Ω preset to enable the distortion to be minimized. From a number of practical tests, the XR2206 supplies a fairly clean sinusoidal signal up to about 100 kHz. Towards 200 kHz, the sine-wave gradually changes into a triangular waveform.

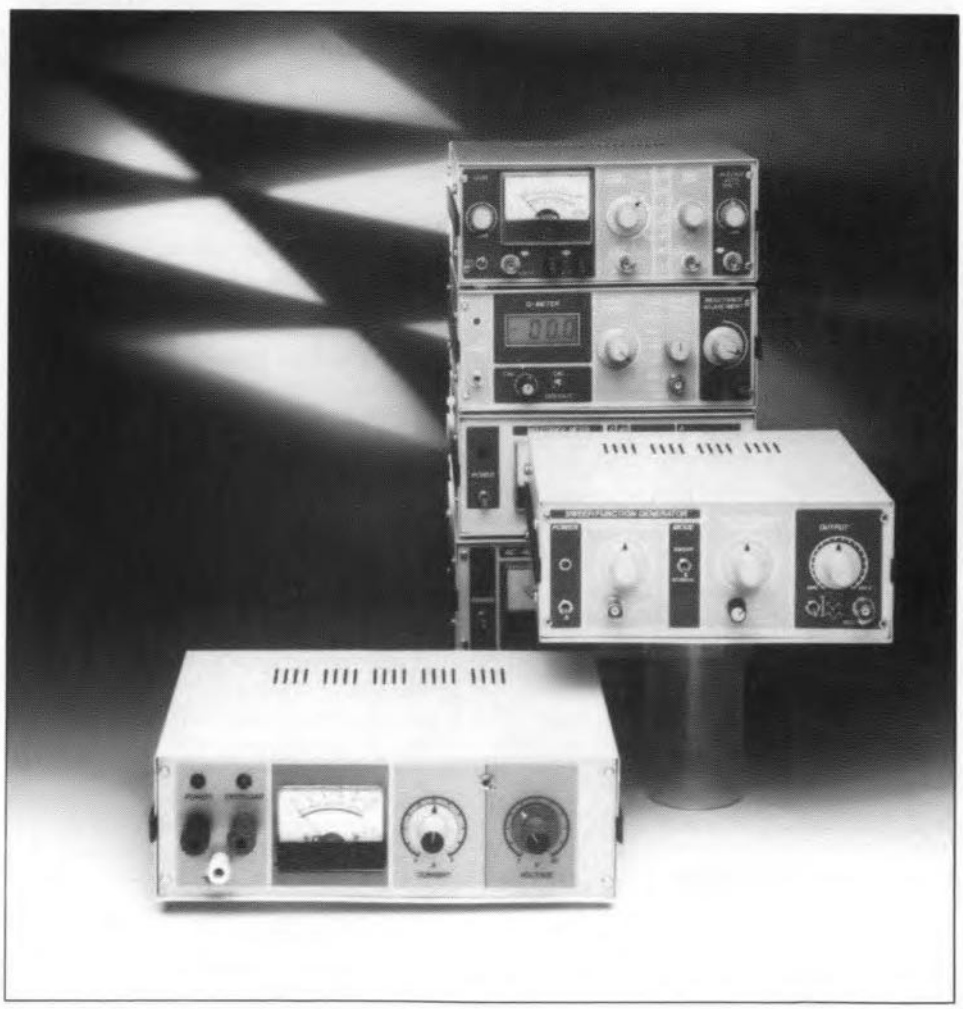
The L165 is capable of providing considerably more output power than it is allowed to by the 50-Ω output. If it is desired to use the generator for swept-frequency measurements on loudspeakers or drive units, a low-impedance output may be provided on the instrument by fitting two binding posts on the rear panel. The signal outlet is connected direct to the negative terminal of C_{13} to negate the effect of the two 100-Ω series resistors. Note, however, that this extension requires a rather larger power supply. In that context, it is recommended to use a mains transformer capable of supplying at least 1 A of secondary current, a bridge rectifier (4×1N4001) and an additional 1000 µF smoothing capacitor. The single-phase rectifier on the board, D_2, is replaced by a wire link. The 1-A power supply enables the function generator to provide ample driving power for 4-Ω and 8-Ω loudspeakers. The use of a bridge rectifier instead of the single-phase rectifier allows a mains transformer with a secondary voltage of 12 V to be used instead of a 15-V type. ■

LOW-BUDGET TEST EQUIPMENT

This is the fifth instalment in a series of articles describing test equipment no serious electronics enthusiast or design engineer can do without. All instruments are housed in an attractive metal cabinet type LC-850 from Telet, which comes with with protective strips at the sides. The switch areas on the front panels are grey, light blue or dark blue with white lettering, and their size is geared to the front panel of the LC-850 enclosure.
Shown in the picture are the instruments described so far in this series. The **power supply** shown in front will be next month's subject.
The pile of four instruments behind the **sweep/function generator** consists of (top to bottom):

- **LF/HF signal tracer (January 1990)**
- **Q meter (May 1990)**
- **RF inductance meter (November 1989)**
- **AC millivoltmeter (February 1990)**

The pointer knobs used on the instruments are made by applying a small arrow or triangle (available as transfer symbols) on to the collet and protecting it with plastic spray.



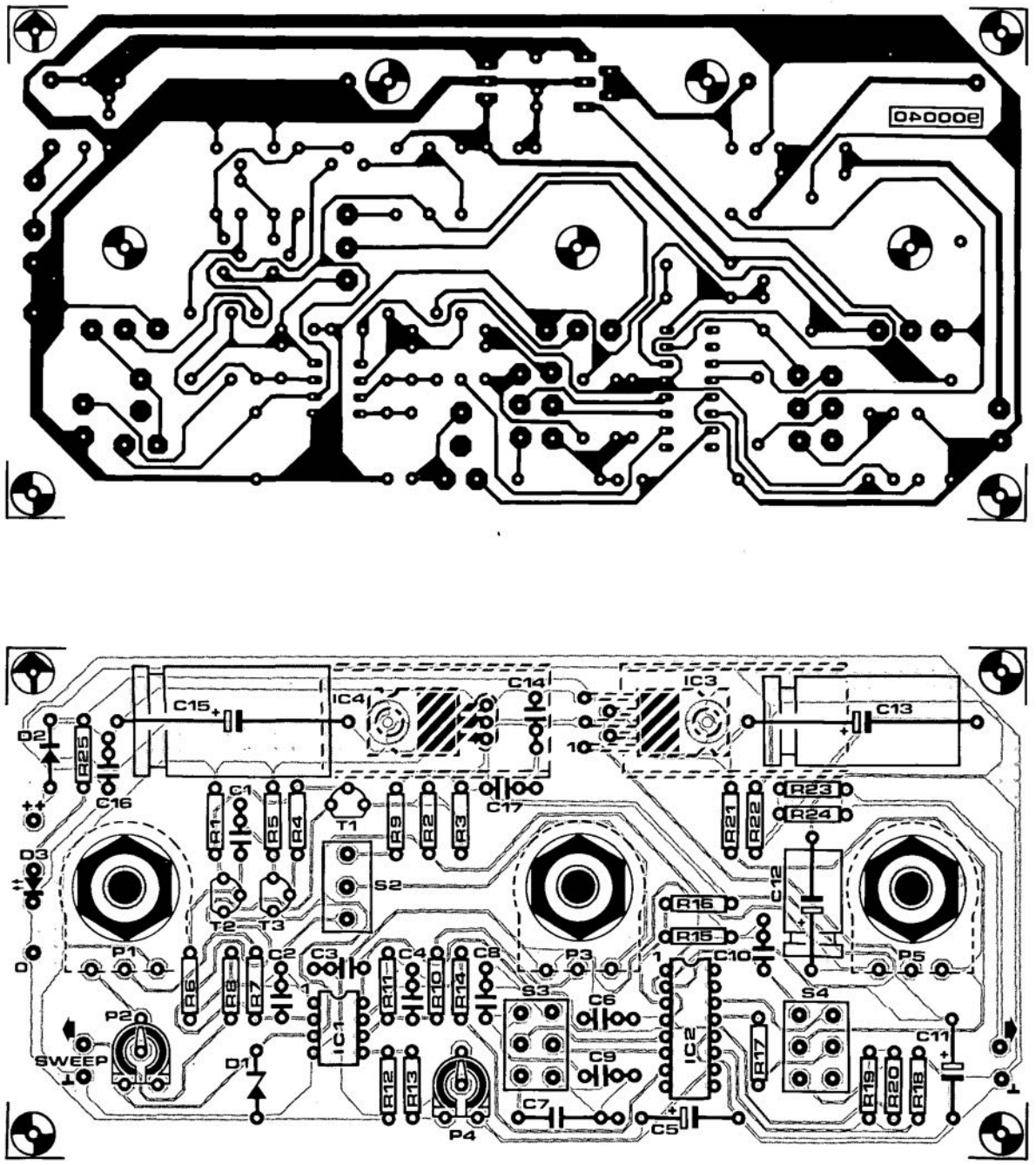


Fig. 2. Track layout (mirror image) and component mounting plan of the single-sided printed circuit board for the generator.

verting input. This is achieved with the aid of T_1. In the monostable formed by T_2-T_3, C_1 ensures that the integration capacitor is discharged rapidly to provide the trailing edge of the sawtooth. The reference voltage provided by D_1 thus determines the amplitude of the sawtooth voltage that sweeps the frequency of the function generator.

The sawtooth voltage is also available at a separate sweep output on the instrument. Resistor R_8 sets the output impedance to about 1 kΩ. The sweep output is short-circuit resistant and may be used for driving the X amplifier of an oscilloscope for swept-frequency measurements.

Output amplifier

The Type L165 opamp used in the output amplifier is capable of providing ample output current at a reasonable price. The IC is used in a conservatively rated configuration and is therefore not likely to actuate its internal overheating protection. The power opamp is wired as an non-inverting buffer (voltage follower), so that the amplitude and phase of the output signal correspond to those of the input signal at the wiper of amplitude control P_5. An electrolytic capacitor, C_{13}, is required to decouple the d.c. component at the output since a non-symmetrical supply is used. The parallel resistor combination at the output is not strictly required for overload protection (which the L165 provides by itself). It does, however, limit the output current to a safe value. At the same time, it sets the generator output impedance to 50 Ω, which is a commonly used value on test equipment.

PROFILE: MAPLIN ELECTRONICS

by Bernard Hubbard

"We're working very hard to improve the service to our customers," said Doug Simmons, Marketing Director of Maplin Electronics PLC in an exclusive interview with *Elektor Electronics*. "In fact, we have assigned one of our directors to concentrate on improving every aspect of our service."

It is this singleness of purpose that has taken Maplin from a back bedroom business to a multi-million pound operation with 400,000 customers and employing 250 people at three locations: Hadleigh and Raleigh (near Southend) and Wombwell near Barnsley.

From the outset the directors had a series of distinct operating principles: the purchasing of new, high-quality, reliable components; competitive prices; and same-day dispatch for orders.

To achieve this, Doug and his fellow directors search the world for sources, new products and new projects. "We often visit the Far East, mainly Japan, Taiwan, Korea, Hong Kong, and China".

From day one the Maplin directors set themselves the ambitious target of growing at a rate of 20 per cent per year and this they have been able to achieve in spite of the ups and downs of the electronics market.

Says Doug: "After several years when hobbyists' interest in electronics seemed to be on the wane, there now appears to be a resurgence of interest. People seem to have overcome the fascination with the computer and want to get on and build electronic projects again".

Doug also believes that this resurgence has come about partly because of the changes in education, particularly since electronics now forms part of design technology, which is a core subject in the national curriculum.

Certainly, many of Maplin's customers are of school age. Says Doug: "From all our evidence so far, our customers are predominantly young—between 15 and 30 years old". However, such is the expertise of Maplin that they are busily engaged in a long study to discover more about their customers.

Studies aside, Maplin do a lot of talking to their customers. Apart from a team of 50 girls engaged in telesales at Hadleigh, two engineers are on stand-by from 2 p.m. to 4 p.m. every afternoon to talk to customers with tricky technical questions. "The trouble is they tend to spend hours talking to our engineers and that makes it difficult to handle all the calls. That is why I implore people who ring up with technical problems to be economical so as to give other people a chance", says Doug.

Maplin would love to set up electronics hobbyist clubs but are concerned that they would not be able to sustain a vigorous organization nationwide. "Being the type of company we are, we would hate to start something that folds after a couple of years".

Despite opening a chain of shops (another is planned), Maplin never lose sight of the fact that theirs is predominantly a mail order business, with its huge catalogue being sent to over 200,000 customers, mainly based in the UK, each year. "It's a never-ending task. The moment you have completed one catalogue, you have to begin the next. This year we plan to bring our catalogue out earlier, possibly in the autumn rather than at the turn of the year". The catalogue is unlikely to grow any thicker because the last one has reached the top end of the Post Office weight band.

Front of the new distribution centre at Wombwell.

Section of the main collection area.

The goods inward department (foreground).

Orders are dispatched at the rate of 13,000 a week from the new £2 million distribution centre that Maplin opened formally last autumn. The distribution centre is linked to Hadleigh by computer so that orders are being processed at the distribution centre within seconds of their documentation being prepared in the south. A far cry indeed from the shop above the launderette where Maplin's retail life began.

Despite the enormous strides made by Maplin, which is 18 years old this year, the company has not lost its happy atmosphere. A bingo game is played every Monday morning to ensure everyone is concentrating. During the game vital messages are communicated to employees who directors know full well will be fully alert.

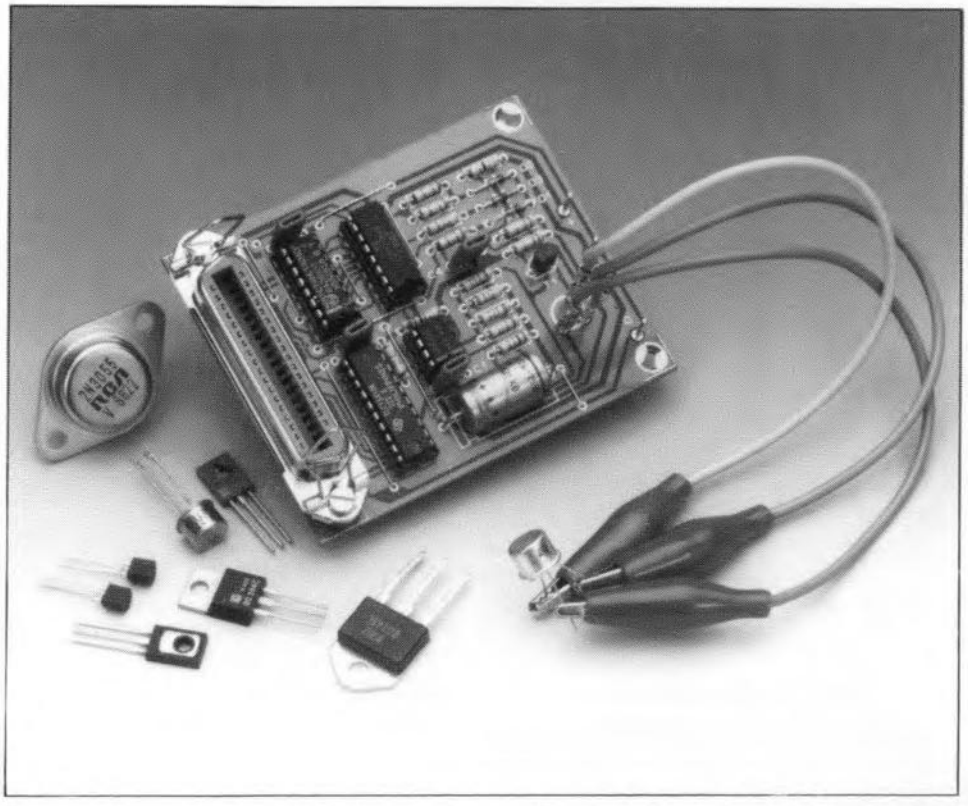
The company is convinced it still has a big job to do in terms of customer service and the enhancement of product quality. It has a quality assurance department that tests components and new products as they enter Maplin and before their inclusion into orders. At the same time, the company is working towards being granted a British Standards certificate on its products.

Although there might be a great opportunity with the creation of the single European market in 1992, Doug Simmons is cautious: "The grass is always greener on the other side of the fence and in countries in the EEC where the disposable income is higher than in the UK there are already highly successful companies such as ours well entrenched. We would have a difficult task penetrating these markets and in doing so might well invite a retaliatory drive into our own home market". ■

TRANSISTOR CHARACTERISTIC PLOTTING

S. Aaltonen

The circuit described here makes use of a computer to plot the so-called output characteristic and determine the small-signal current gain, h_{fe}, of an n-p-n transistor. These two transistor parameters are of great importance for classifying an unmarked transistor, for a reliable good/faulty test, and for selecting matched transistors from an available lot. Although the program that controls the circuit is written for the Atari ST series of home computers, the use of the Centronics port should enable owners of other micros to adapt their own version fairly easily.



The use of a computer and a printer, instead of the more usual oscilloscope, to measure and record transistor parameters is subject to one important proviso: the transistor under test must be located between a digital-to-analogue converter (DAC) and an analogue-to-digital converter (ADC). The circuit presented here has, therefore, a digital input as well as a digital output, both of which are connected to the Centronics (parallel) printer port to convey the necessary data and control levels to and from the computer.

Transistor parameters

Since the basics of transistor characteristic plotting have been covered relatively recently in Ref. 1, only a recap is given here.

Figure 1 shows an ideal transistor in the standard four-pole test circuit in which voltages are applied to the base-emitter junction and the collector-emitter junction.

The first important transistor parameter that may be obtained from this basic test circuit is the so-called output characteristic, which is a curve that describes the relation between the collector-emitter voltage, U_{CE}, and the collector current, I_C, with the base current, I_B, as a parameter. Ideally, such curves are straight lines since the collector current is determined by the base current only, and not by the collector-emitter voltage. In practice, however, the so-called early effect causes the I_C-vs-U_{CE} characteristic to become a curve rather than a straight line,

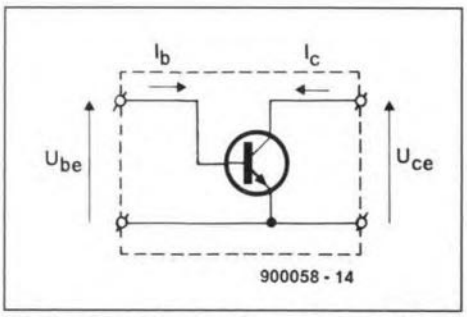


Fig. 1. Transistor in a four-pole test circuit.

particularly at relatively low values of U_{CE}.

The second important characteristic is the small-signal current gain, h_{fe}. This is defined as the ratio of change in collector current, δI_C, to the change in base current, δI_B, that produces it, when the collector-emitter voltage is kept constant:

$h_{fe} = \delta I_C / \delta I_B = I_c / I_b$ when U_{CE} is constant.

Most transistor manufacturers provide this parameter at two or three values of U_{CE} and I_B.

The present circuit plots the output characteristic of n-p-n transistors for eight values of I_B, and in addition automatically calculates a statistically derived h_{fe} value. With these two parameters on the screen and on paper (hard copy from the printer), you are in a position to select matching transistors for critical applications, or find a substitute for an unknown transistor.

Circuit description

As already stated, the transistor under test (TUT) is located between a DAC (IC_2) and an ADC (IC_4) —see Fig. 2. All control and processing of measured values is carried out by the computer.

The circuit uses two supply voltages: 5 V for the DAC, the ADC and counter IC_1, and 15 V for the transistor test circuit and the associated voltage amplifiers. The

higher supply level of 15 V is required to provide the TUT with a maximum collector-emitter voltage of about 9 V.

The measurement is cyclic and controlled by the computer. First, the base current of the TUT is set at a certain value. Next, the collector-emitter voltage is raised gradually from 0 V to about 9 V, and the resulting collector current is measured. This process is repeated with the next higher value of the base current. The step size is 25 µA, and there are eight steps starting at $I_B = 0$ µA. The test cycle is complete at $I_B = 175$ µA.

The control program provides a stream of clock pulses on the D1 (data-1) line of the Centronics port. The clock pulses are counted by IC_1, a Type 74HCT4040. The counter values at the Q0–Q7 outputs are converted to an equivalent analogue voltage between 0 V (value: 0) and 2.5 V (value: 255) by DAC IC_2. The Q8, Q9 and Q10 outputs of IC_1 control the base current of the TUT in 8 steps. The required current step size of 25 µA is obtained with the aid of resistors R_3–R_6. Note that the value or equivalent value of each resistance at the three counter outputs is derived from 180 kΩ, since this value results in a current flow of about 25 µA at a logic high voltage of about +4.8 V at the respective counter outputs.

The clock pulses provided by the computer cause the voltage at the output of IC_2 to be increased from 0 V to the reference voltage of the ZN425 (2.5 V) in 255 steps. Initially, this happens with Q8, Q9 and Q10 of the counter being low so that I_B = 0 µA. The analogue voltage is amplified by a factor of four by opamp IC_{3a}. The resulting voltage range at the collector of the TUT is about 0 V to 9 V. This voltage range is divided by two by R_{15}-R_{16} to prevent the maximum input voltage of ADC IC_4 being exceeded.

The emitter current of the TUT causes a voltage drop across R_{14}. This voltage is amplified by a factor of 48 by opamp IC_{3b} before it is applied to the A0 input of the ADC. Note that the emitter current rather than the collector current of the TUT is measured. This can be done without problems, however, since in the four-pole test circuit the emitter current is the sum of the collector current and the base current. The latter is in the µA range and is, therefore, negligible with respect to the collector current, which is in the mA range.

Every time U_{CE} of the TUT reaches its maximum value of about 9 V, it is reset to 0 V again, and the base current is increased by 25 µA, to start a new curve.

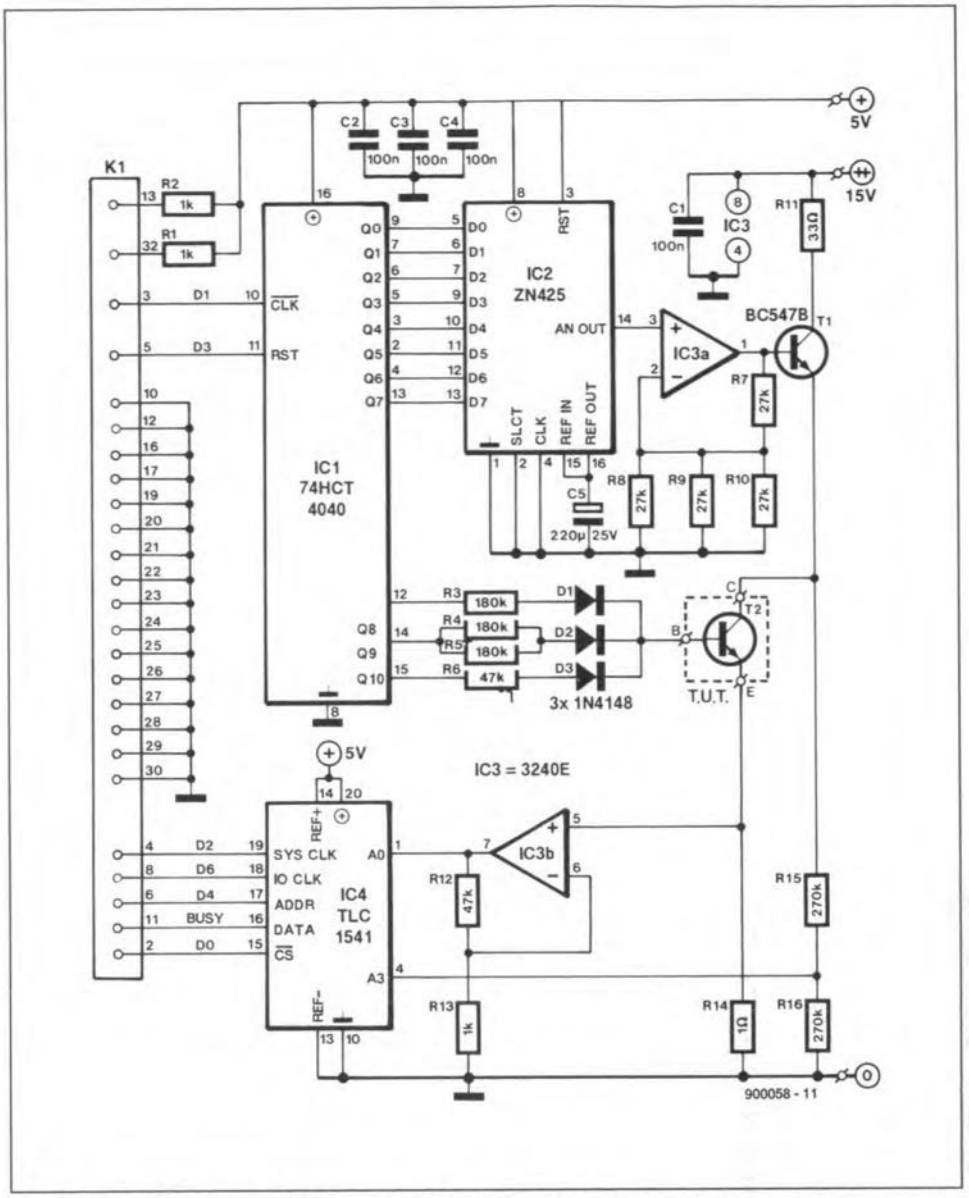


Fig. 2. Circuit diagram of the computer-controlled transistor curve tracer.

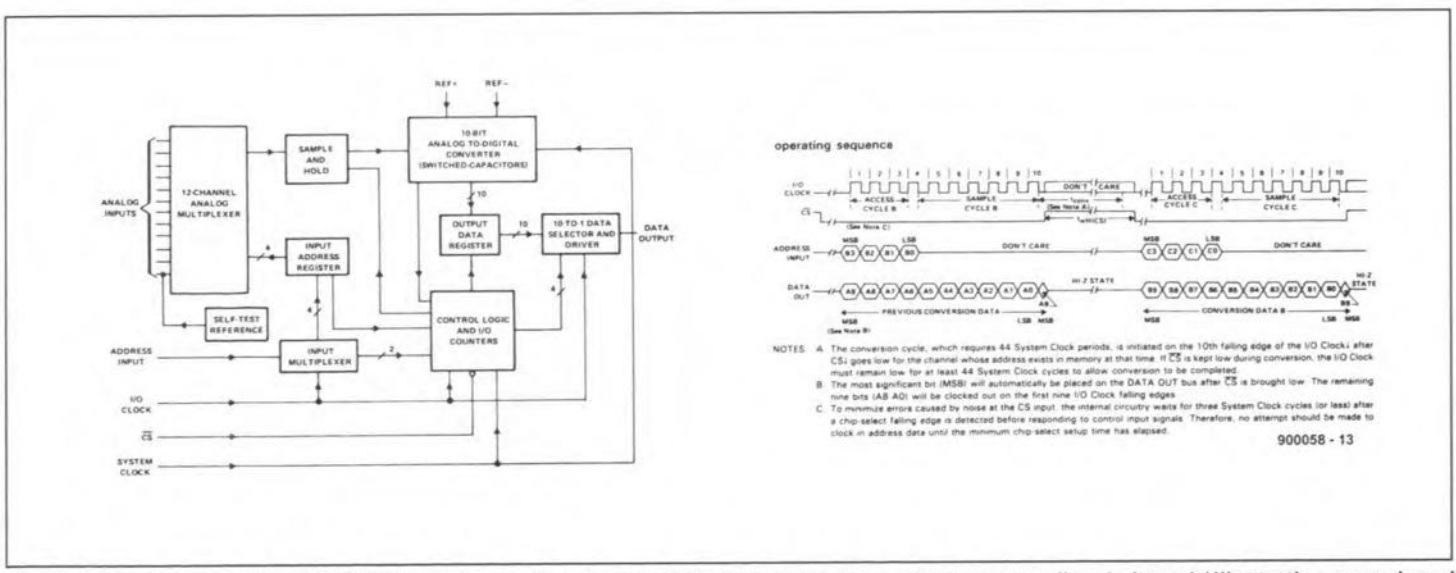
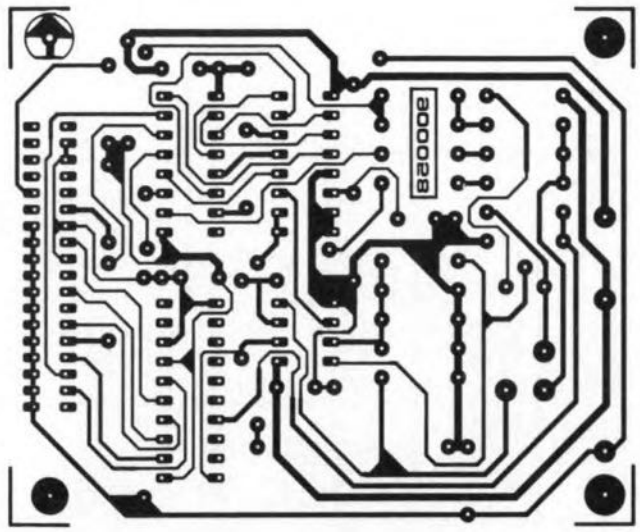


Fig. 3. Block diagram of the TLC1541 and the pertinent pulse timing on which the control program flow is based (*illustration reproduced by kind courtesy of Texas Instruments*).



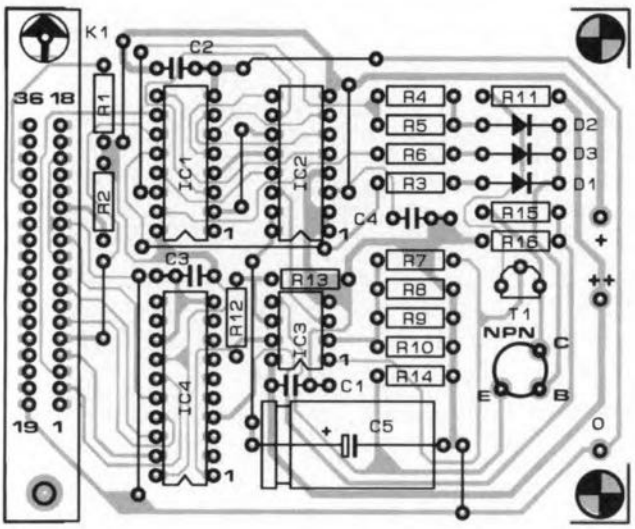


Fig. 4. Track layout and component mounting plan of the single-sided printed-circuit board

COMPONENTS LIST

Resistors:

3	1k0	R_1;R_2;R_{13}
3	180k	R_3;R_4;R_5
2	47k	R_6;R_{12}
4	27k	R_7–R_{10}
1	33Ω	R_{11}
1	1Ω0	R_{14}
2	270k	R_{15};R_{16}

Capacitors:

4	100n	C_1–C_4
1	220µF 25V	C_5

Semiconductors:

1	BC547B	T_1
1	74HCT4040	IC_1
1	ZN425	IC_2
1	CA3240E	IC_3
1	TLC1541	IC_4
3	1N4148	D_1;D_2;D_3

Miscellaneous:

1	36-way PCB-mount Centronics socket	K_1
1	PCB	900058
1	control program	ESS1431

This cycle is repeated eight times until a high pulse on Centronics line D3 resets counter IC_1.

Processing the analogue quantities

The Type TLC1541 (IC_4) from Texas Instruments is a 10-bit, 11-channel analogue-to-digital converter with an internal analogue multiplexer and a serial data output. In the present circuit, only two of the available 11 channels are used. One channel, A0, takes the I_C parameter, the other, A3, the U_{CE} parameter.

Figure 3 shows the block diagram of this interesting LinCMOS chip, along with the pertinent timing sequence.

The computer selects the channel from which it requires the 10-bit data. This selection is accomplished by pulling $\overline{CS}$ of the TLC1541 low via Centronics bit D0 and applying the relevant channel code (0 or 3) serially via Centronics bit D4. All channel selection, timing, conversion, and serial data output operations in the TLC1541 run under the control of SYSCLOCK and IO CLOCK, for which the required pulses are supplied by the computer via Centronics lines D2 and D6 respectively.

The 10-bit output data for processing by the computer is shifted out serially with the MSB first. The conversion error of the TLC1541 is ±1 LSB, or 5 V/1024 = 4.8 mV at a maximum voltage of 5 V at the channel inputs. Hence, the maximum error of U_{CE} is about 10 mV, which is acceptable in the present application. The computer reads the measured value by monitoring the state of the BUSY input line on its Centronics port.

Control program

The control program for the curve tracer must:

- provide clock pulses to the U_{CE}-I_B generators
- arrange the timing sequence of the TLC1541
- read the measured values of U_{CE} and I_C that belong with a particular value of I_B.
- calculate an average h_{fe} value
- plot I_C as a function of U_{CE} with I_B as a parameter
- provide a graphics screen
- allow the graphs on the screen to be dumped to a printer to obtain hard copy

All this is arranged by a program written in C for the Atari ST series of computers. This program, npn.prg, and the source file, npn.c, are available on disk. A few examples of output characteristic plots are shown in Fig. 5.

Construction and use

Construction of the computer-controlled curve tracer is straightforward if the printed-circuit board shown in Fig. 4 is used. Connector K_1 is a standard 36-way Centronics socket for PCB mounting. As shown on the photograph of our prototype, this connector is mounted on two plastic PCB spacers. An alternative that does not require spacers is a similar connector with angled terminals. Both types of connector are often referred to as 'blue-ribbon' and are commonly used on matrix printers.

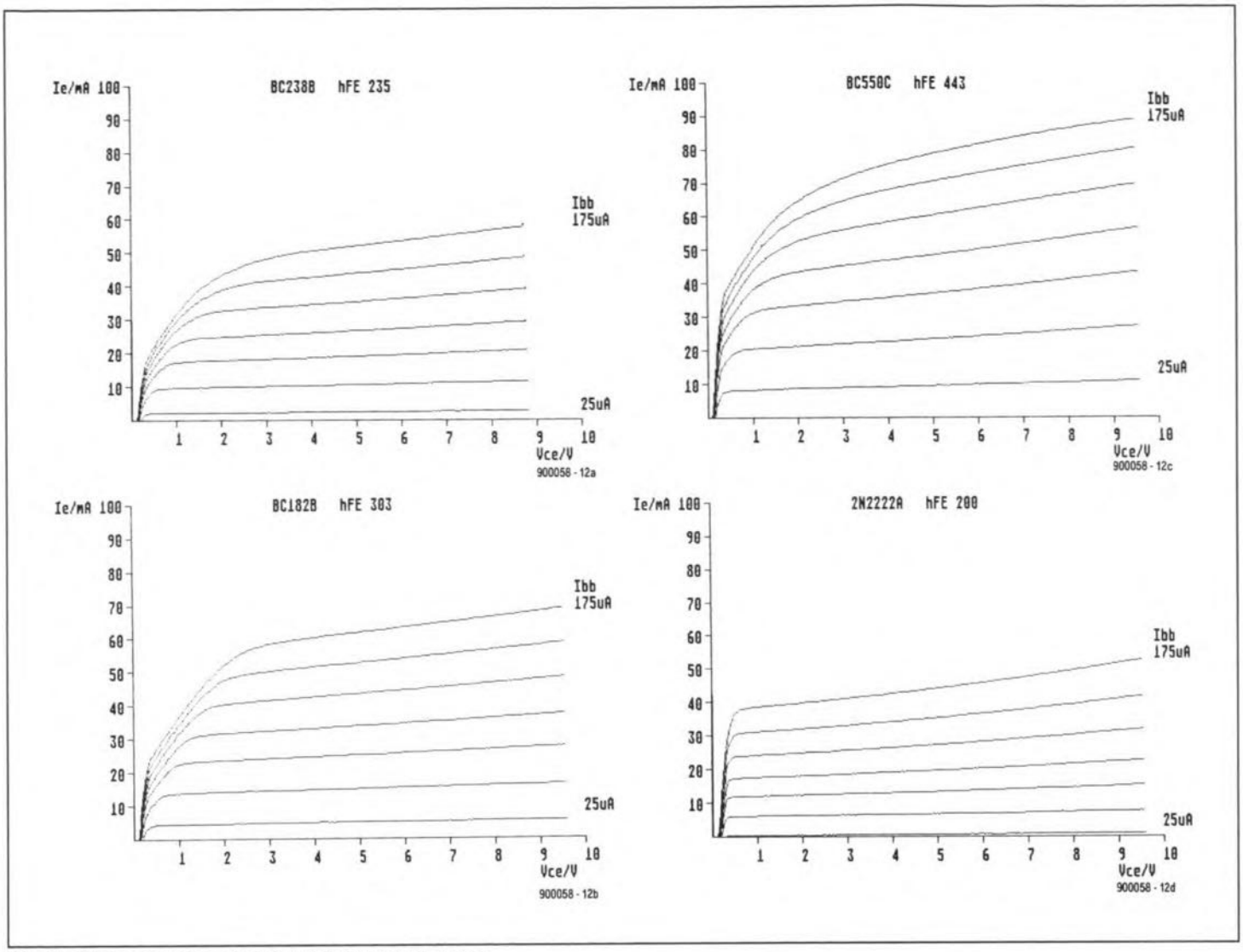


Fig. 5. A few examples of plots made by the program.

Start the construction by fitting the seven wire links, followed by the IC sockets. Next, mount the resistors, the capacitors, diodes and the single transistor.

A transistor test socket may be used for inserting the TUT, but in many cases three light-duty flexible wires with small, plastic covered crocodile clips are perfectly all right.

The ICs are fitted last. Observe their orientations, and be extra careful with the ZN425 and the TLC1541!

The circuit requires a separate power supply that provides regulated output voltages of 5 V (+ terminal) and 15 V (++ terminal). The current requirement for the 5-V supply is only 50 mA or so, while that of the 15 V supply is determined mainly by the collector current of the TUT. In most cases, 200 mA will be adequate. Voltage regulators such as the 7805 and the 7815 are fine for these applications, but do not forget the usual decoupling capacitors to prevent noise and oscillation.

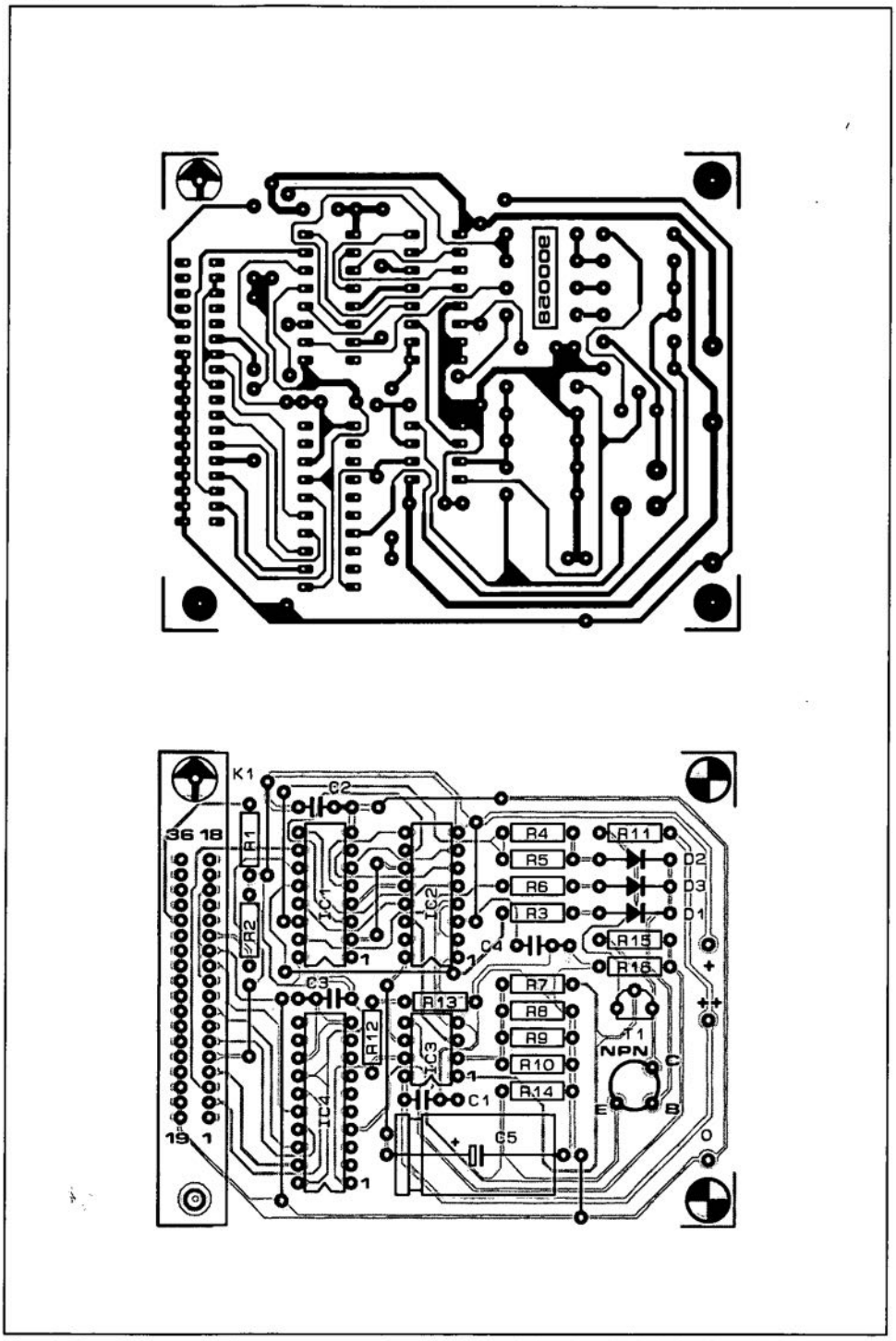
The completed PCB is fitted in a suitable ABS enclosure, the size of which depends on whether the power supply is internal or external. In any case, do not use mains adapters to power the circuit, since these do not in general provide the required output voltage stability.

The curve tracer is connected to the computer by a standard printer cable.

The curve tracer is simple to use: insert or connect the transistor under test (make sure you get the b-c-e terminals right), apply power and run the control program by clicking twice on 'npn.prg' in the file menu. The program, after being loaded, will prompt you to enter the transistor type and type any key to start plotting. Do not worry if nothing appears to happen at first, since the I_B = 0 µA curve is drawn first. Once the output characteristic appears complete on the screen, the program halts and waits for a key to be pressed to take you back to the file menu. Hard copy may be obtained before exiting the program by disconnecting the tracer from the printer port, connecting the printer, switching it on line and pressing the ALTERNATE and HELP keys simultaneously. Finally, the circuit and the program are suitable for testing n-p-n transistors only. The control program supplied on disk is suitable for **monochrome Atari ST** systems only. ■

Reference:

1. Transistor curve tracer. *Elektor Electronics* October 1988.



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1	1Ω0	R14
2	270k	R15;R16

Capacitors:

4	100n	C1–C4
1	220µF 25V	C5

Semiconductors:

1	BC547B	T1
1	74HCT4040	IC1
1	ZN425	IC2
1	CA3240E	IC3
1	TLC1541	IC4
3	1N4148	D1;D2;D3

Miscellaneous:

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1	PCB	900058
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This cycle is repeated eight times until a high pulse on Centronics line D3 resets counter IC1.

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INTRO-SCAN FOR CD PLAYERS

J. Ruffell

Owners of inexpensive, yet reliable, CD players, such as the Philips CD371 or Aristona CD1372, are often frustrated by the limited programming facilities of these machines. This drawback becomes particularly annoying when a CD is to be copied on to a cassette. The programming aid described here can put an end to this irritation.

With most of the popular CD players, it is necessary, when a certain number of tracks of a CD are to be copied in a particular order on to a cassette, to place the track numbers into the memory. This in itself is not a big problem if you have the CD box to hand. This is not always the case and the only solution is then to listen to all the tracks and note down the relevant track numbers. This can, however, be a time-consuming business.

The programming aid presented here makes it possible, with the aid of the "next" key, to listen briefly to all the tracks on the CD during which each track number may be entered into the memory of the programming aid. After all tracks have been scanned, the content of the aid's memory is transferred to the internal memory of the CD player. Provision is made for the CD player to be started auto-

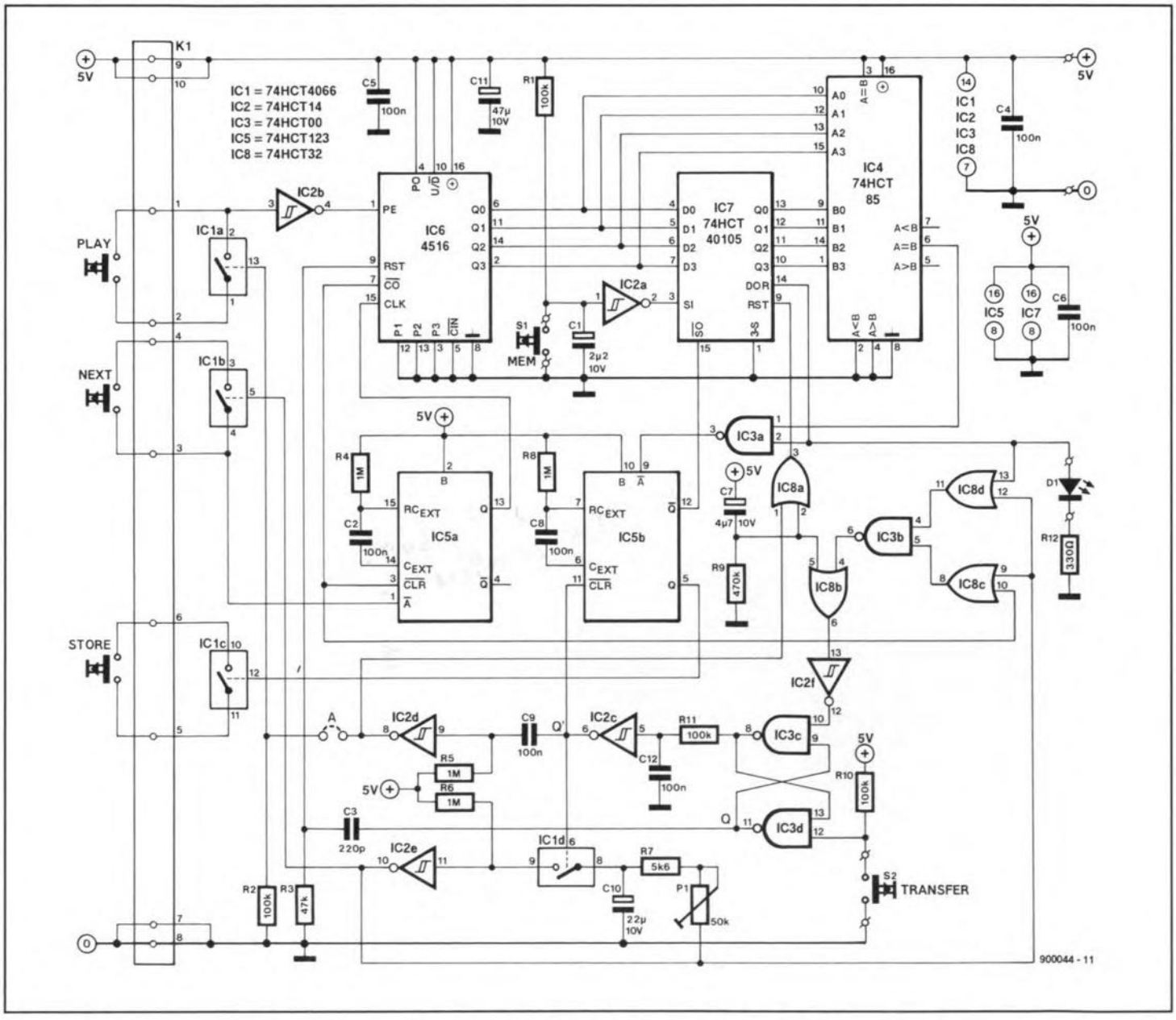


Fig. 1. Circuit diagram of the programming aid.

matically after the memory transfer has taken place.

The board is small enough to be fitted inside the CD player. Connexions between it and the front panel are by a 10-way flat cable. Two key switches and an indicator LED must be added to the player controls.

Circuit description

The circuit of the programming aid—see Fig. 1—is based on IC7, a register with a capacity of 16×4 bits that stores the programmed track numbers.

When the unit is switched on, IC7 is reset via C7, R9 and IC8a, and the SR bistable formed by IC3c and IC3d via C7, R9, IC8b and IC2f. The Q output (pin 8 of IC3) of the bistable then disables the square-wave generator based on IC2e via R11, C12 and IC2c. The frequency of the generator is determined by (P1+R7)-C10.

When in this condition the 'play' key of the CD player is pressed, the first track of the CD is played. At the same time, counter IC6 is increased by 1. Every time the "next" key is pressed briefly, the counter position is increased by 1. Monostable IC5a, connected between the "next" key and the clock input of the counter, ensures that the pulse train emanated by the "next" key is converted into a single pulse.

The keys on most popular CD players operate by tone decoding. This means that continuous pulse trains exist at pins 2 and 4 of K1. Pressing the 'play' or the "next" switch places the pulse train on pin 1 or pin 3. A pulse train at pin 1 does not matter because the pulses are used only for enabling the counter, but that at pin 3 is converted into a single pulse by IC5a.

Each time the MEM switch, S1, is pressed, IC7 receives a clock pulse via IC2a and the position of IC6 is stored in the register. The relevant track number is then programmed. The LED will light when at least one number has been placed into the register.

After all track numbers (up to 15) have been stored, the 'stop' key of the CD player must be pressed. The display then shows the total number of tracks on the CD.

The contents of IC7 are transferred to the player's memory by simulation of the manual programming of the player, a process that is started by pressing TRANSFER switch S2. The bistable is then set, so that the counter receives a reset pulse via R3-C3. After a brief delay caused by R11-C12, the square-wave generator is started. Each pulse emanating from the generator operates the "next" switch; at the same time, the counter receives a clock pulse via IC5a so that it remains synchronous with the track indication on the display.

The position of IC6 is compared by IC4 with the first four-bit word stored in the register. If the data are identical, the A=B output of IC4 emits a pulse that is passed to the programme key of the player via IC5b and pins 5 and 6 of K1. The relevant number is then stored in the player.

The next stored number then appears at the output of the register, after which the generator sends as many clock pulses to the "next" switch and the counter as are necessary to make the counter position coincide with that at outputs Q0–Q3 of IC7. In this manner, the circuit scans all the track numbers of the CD and emits a program pulse at the moment the relevant number appears at the output of IC7. The speed at which this happens depends on the setting of P1. In principle, there are no limits to the speed so long as the copying takes place correctly.

Gates IC2f, IC3b and IC8b–d ensure that the circuit is reset correctly when the highest counter position is reached.

Wire bridge A enables automatic starting of the CD player when the contents of the register have been copied to the player. When copying is complete, a pulse is sent to the 'play' switch. If this facility is not required, the bridge is simply omitted.

Construction

The printed-circuit board shown in Fig. 2 is not available ready-made. It is, however, easy to make and once it has been populated, it is conveniently built into the CD player. The connexions from the board to the player's front panel controls are as shown in Fig. 1. The supply line

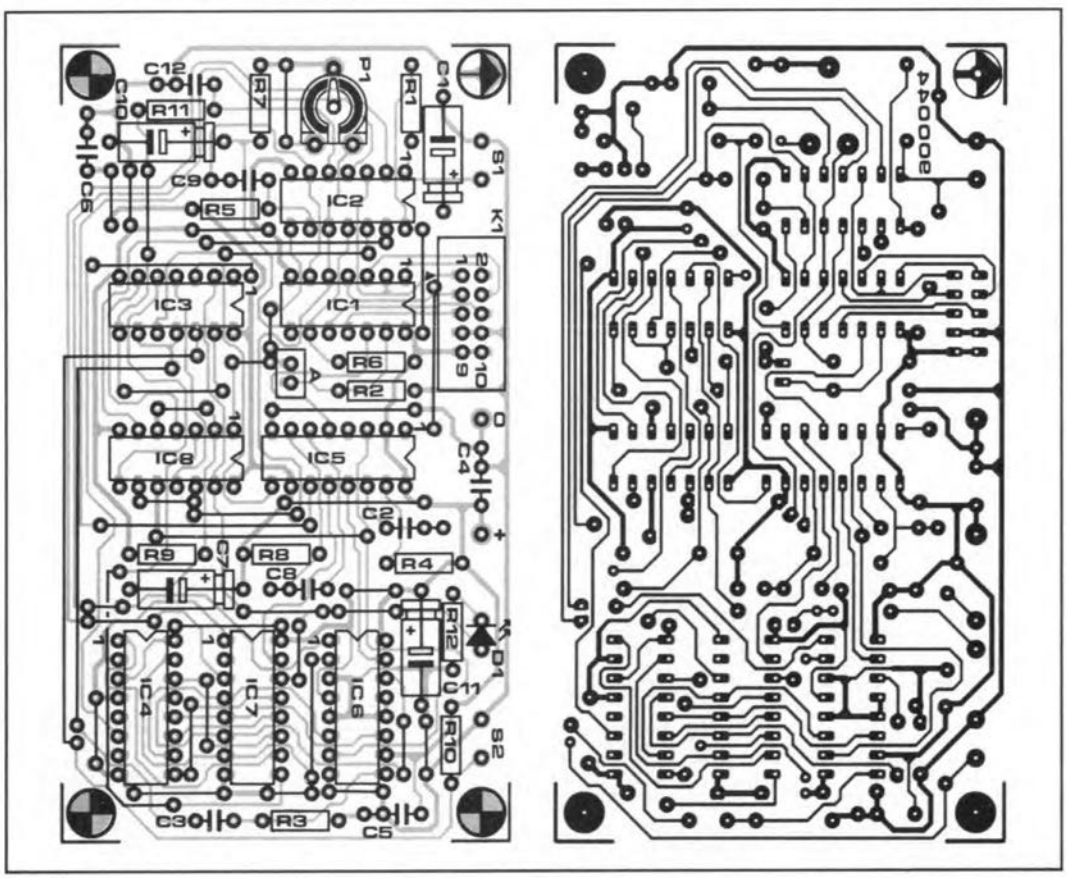


Fig. 2. Printed circuit board of the programming aid.

PARTS LIST

Resistors:
R1,R2,R10,R11 = 100 k
R3 = 47 k
R4,R5,R6,R8 = 1 M
R7 = 5k6
R9 = 470 k
R12 = 330 R
P1 = 50 k preset

Capacitors:
C1 = 2µ2, 10 V
C2,C4,C5,C6,C8,C9,C12 = 100 n
C3 = 220 p
C7 = 4µ7, 10 V
C10 = 22 µ, 10 V
C11 = 47 µ, 10 V

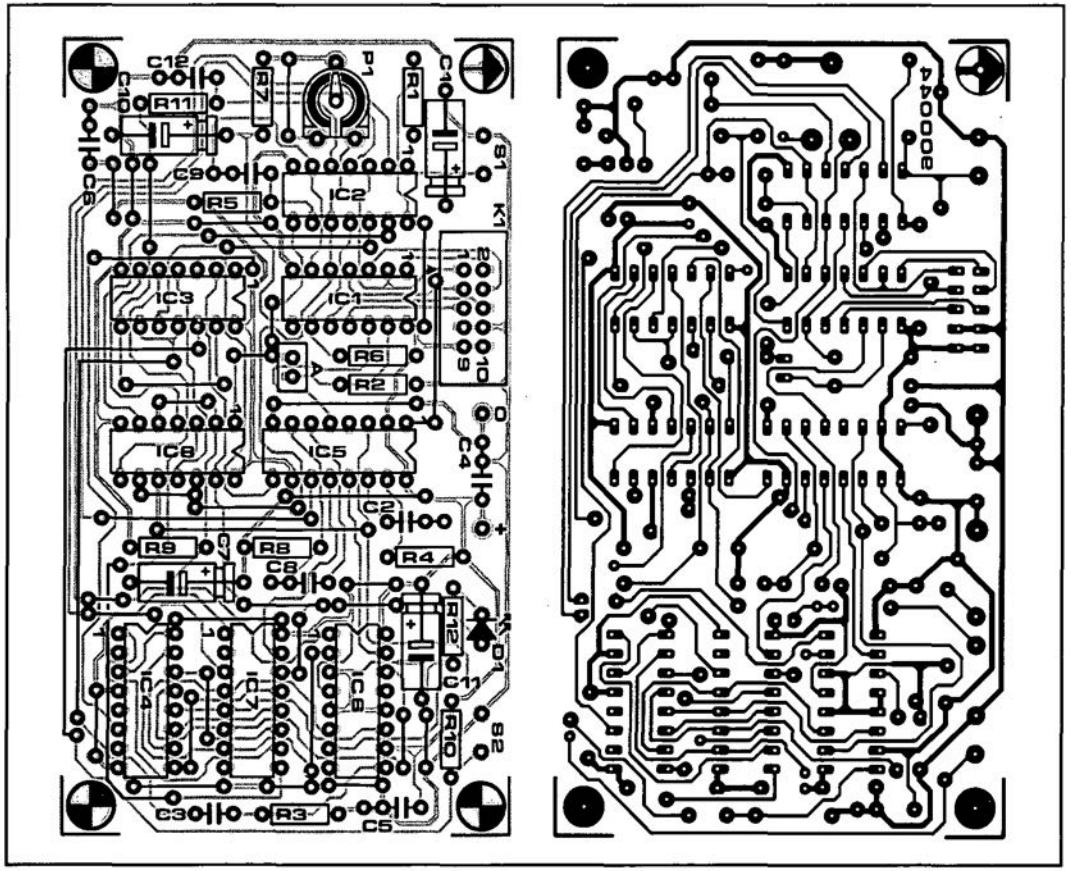
Semiconductors:
D1 = LED, red, 3 mm
IC1 = 74HCT4066
IC2 = 74HCT14
IC3 = 74HCT00
IC4 = 74HCT85
IC5 = 74HCT123
IC6 = 4516 (NOT 74HCT4516!)
IC7 = 74HCT40105
IC8 = 74HCT32

Miscellaneous:
K1 = 10 pole male header
S1,S2 = keyswitch, 1 make
10 cm of 10-way flat cable

line, pins 9 and 10 of K1, is connected to the relevant terminal on the CD board. The earth line, pins 7 and 8 of K1, is connected to the relevant terminal in the CD player. Pins 1 and 2, 3 and 4, and 5 and 6 of K1 respectively, are connected to the terminals of the 'play', "next" and 'store' key switches of the CD player respectively. All these connexions are made by a short length of 10-way flat cable.

MEM switch S1, TRANSFER switch S2 and the red LED should be housed on the player's front panel in a convenient position.

Finally, verify that the aid works satisfactorily. One common fault is that the contents of the aid's memory are not transferred correctly to the player's memory. This is invariably caused by the square-wave generator operating at too high a frequency. The remedy for this is setting P1 to a higher resistance value. ■



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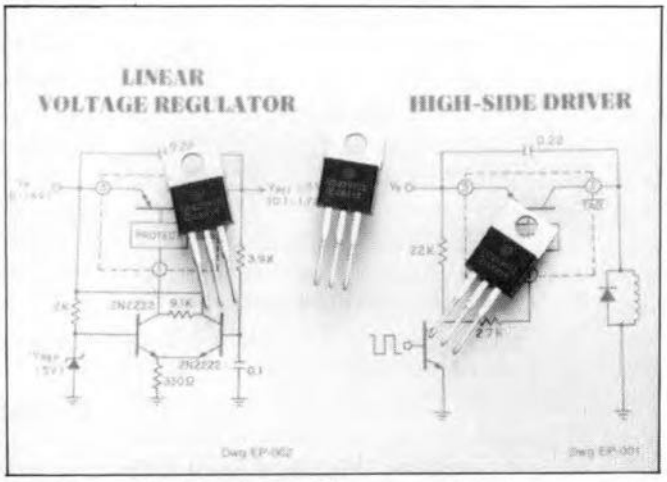
IC5 = 74HCT123
IC6 = 4516 (NOT 74HCT4516!)
IC7 = 74HCT40105
IC8 = 74HCT32

Miscellaneous:
K1 = 10 pole male header
S1,S2 = keyswitch, 1 make
10 cm of 10-way flat cable

PROTECTED HIGH-SIDE DRIVER



Designed for use as a general-purpose, single-channel, high-side (sourcing) power driver, Sprague's UDN2901Z is a smart power IC that can functionally replace p-n-p darlington power transistors in many applications.

Over-current protection has been designed into the device and is actuated between 1.5 A and 2.4 A. It protects the device from output short circuits with supply voltages up to 25 V. When the maximum driver output current is reached, the output drive is reduced linearly. If the over-current condition continues, the thermal shutdown operates, limiting the junction temperature. SOA protection ($V_{CE} \geq 15$ V) is provided by limiting peak current as a function of the voltage across the device.

Though the device is p-n-p-like in its functional behaviour, it is actually a composite p-n-p/n-p-n darlington with several notable differences, including increased current gain, reduced gain bandwidth, and increased input threshold voltage. The device will always draw some standby current owing to the current requirement of the protection circuitry. When the input is OFF, the protection features are disabled.

The UDN2901Z is intended for use as a high-side driver. Typical applications include use as a pass transistor in linear voltage regulators or (with an external ground clamp diode) as a relay/solenoid driver. Owing to the nature of the protective circuitry, the device is protected when operating in either the linear condition or a "saturated" mode (e.g., when driving relay/solenoid loads). The device should NOT be used as a low-side driver (p-n-p emitter follower configuration).

The UDN2901Z is supplied in a 3-lead JEDEC power-tab TO-220 plastic package for operation over a temperature range of –20 °C to +85 °C. For automotive and industrial applications, the UDQ2901Z can be supplied for operation down to –40 °C.

Source:
Data sheet 29310.30 from Sprague, 115 Northeast Cutoff, Box 15036, Worcester, Mass. 01615-0036; (508) 853-5000 or Sprague Electric UK Ltd, Salbrook Road, Salfords, RH1 5DZ; telephone (0293) 517878.

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $T_{TAB} \leq +70°C$, $V_S = 14$ V.

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Functional Supply Range	V_S		1.5	14	45	V
Collector-Emitter Breakdown Voltage	BV_{CEX}	$I_{OUT} = 10mA$, $I_{IN} = 0$	45	–	–	V
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_{OUT} = -1$ A, $I_{IN} = -10mA$	–	1.0	1.3	V
		$I_{OUT} = -1.4$ A, $I_{IN} = -10mA$	–	1.2	1.6	V
Collector-Emitter Sustaining Voltage	$V_{CE(sus)}$	$I_{OUT} = -1.4$ A, L = 2 mH	40	–	–	V
Reverse Input Current	$I_{BK(REV)}$	$V_{IN} = V_S + 0.5$ V	–	–	10	µA
Standby Current	$I_{OUT(STEV)}$	$V_{CE} = 14$ V, $I_{IN} = 0$	–	160	350	µA
		$V_{CE} = 16$ V, $I_{IN} = 0$	–	340	700	µA
		$V_{CE} = 45$ V, $I_{IN} = 0$	–	4.5	–	mA
Quiescent Current	$I_{OUT(CR)}$	$I_{IN} = -500$ nA, $V_{CE} = 14$ V	–	2.0	2.5	mA
		$I_{IN} = -500$ nA, $V_{CE} = 40$ V	–	5.8	7.5	mA
Current Limit	I_{OUTMAX}	$I_{IN} = -10mA$, $V_{CE} \leq 14$ V	–1.5	–2.0	–2.4	A
		$I_{IN} = -10mA$, V_{CE} 40 V	–0.2	–0.5	–0.7	A
Static Forward Current Transfer Ratio	h_{FE}	$I_{OUT} = -1.0$A, $V_{CE} = 5$ V	200	400	–	–
Thermal Shutdown	T_J		–	160	–	°C
Junction-to-Tab Thermal Resistance	$R_{\theta JT}$		–	–	3.1	°C/W

NOTE: Negative current is defined as coming out of (sourcing) the specified device pin.