THE ELECTRONICS MAGAZINE WITH THE PRACTICAL APPROACH
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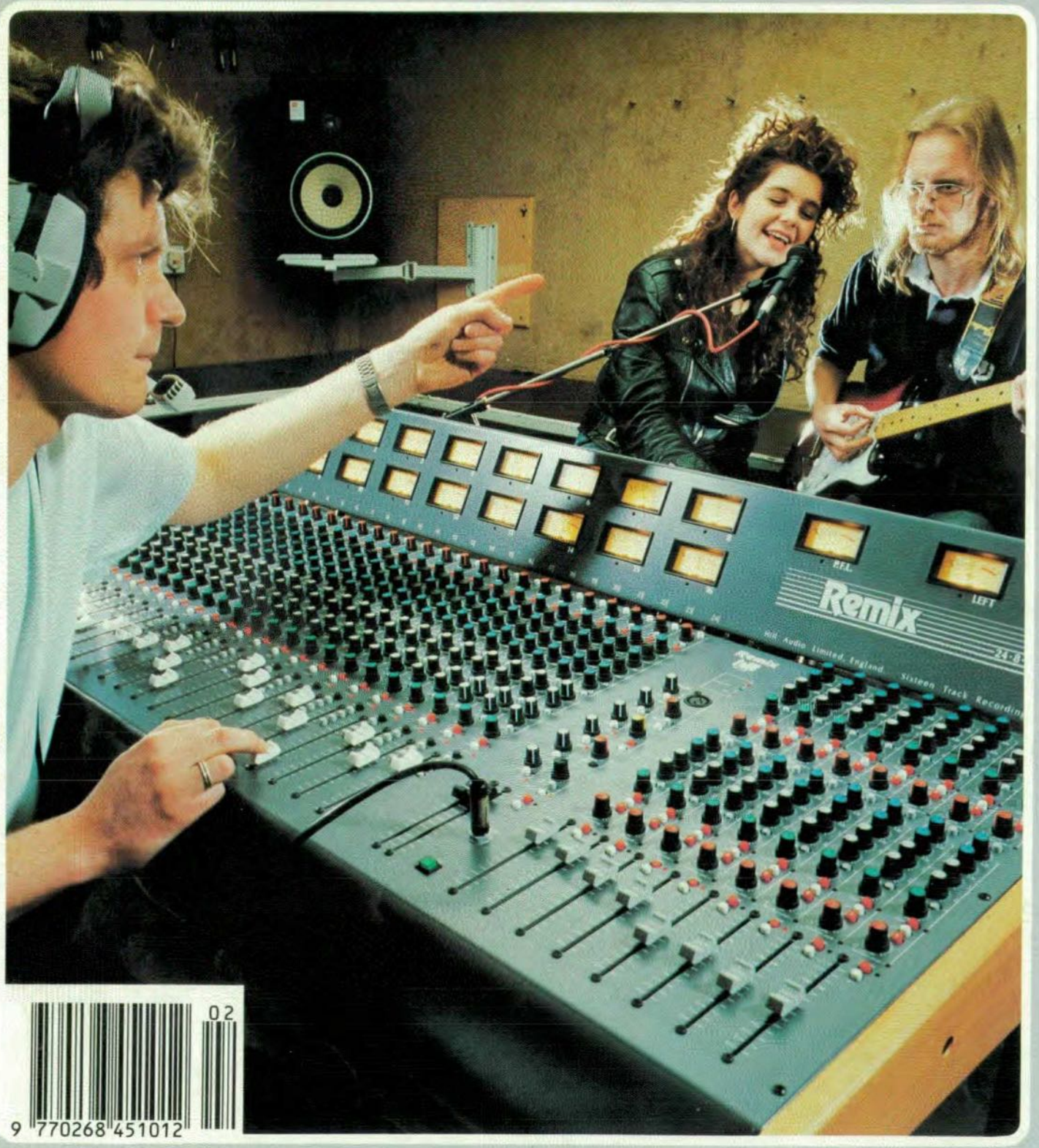
Elektor Electronics

Feedback Killer
PC Radio
Video Mixer (2)
Printer Initialization Aid
Current Sensors
Bucket Brigade Devices



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Elektor Electronics

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February 1990
Volume 16
Number 175

Theme of the month in March will be Components

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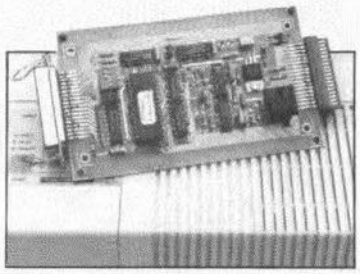
- Bucket brigade memories
- Surge plug
- Pause switch for camcorders
- Low-cost V/I display module
- SAVE decoder: Part 2
- Temperature compensation for LCD modules

Front cover
New singers and musicians, like Kathy and Ian shown here, can now set up their own home recording studio, using the 16-track console developed by Remix to professional standards but at a non-professional price.
The Remix has proved attractive not only to bands, composers and song-writers who want to mix and record at home, but also to smaller, mid-priced commercial music and film studios.
Features include: 6 auxiliary sends, separate tape inputs, peak and status LEDs, +4 dB to –10 dB selectable, 8 bus with 16-track monitoring, 8 effects returns, 100 mm smooth action faders, direct outputs on all channels, send and return patch points throughout, and monitoring with equalization.

CORRECTION

In the description of the photograph on the front cover of the December 1989 issue of *Elektor Electronics*, we stated that the 4.5 m dia. antenna had won a 1989 Queen's Award for Technological Achievement. This was based on wrong information. In fact, Precision Metal Ltd, the designers and manufacturers of the antenna, received a 1989 Queen's Award for Export Achievement.



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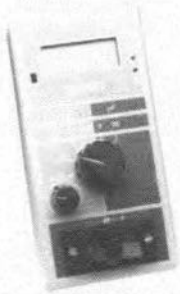

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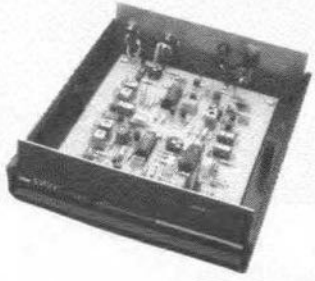

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INITIALIZATION AID FOR PRINTERS

A. Rigby

Many computer users have difficulty in changing printer settings without the help of a manual or handbook. The circuit presented here allows one of sixteen pre-programmed printer settings to be called up at the flick of a switch. Very useful for a good many computer programs that lack a real printer driver, the initialization aid is a low-cost and simple-to-build circuit.

You are working hard on a BASIC program which is almost finished, and hard copy on paper is required to do the final debugging. Since the program is fairly long, you think it wise to set the printer to condensed characters at 8 lines per inch. The printer manual is consulted and the following command is typed in the direct command mode of GWBASIC:

```
LPRINT CHR$(15);CHR$(27);"0";
```

We think you will agree that pushing a small button on the printer initialization aid is a lot easier than having to look up eight or so ASCII characters, and typing them into the computer whilst observing the correct order, brackets and delimiters.

In the above example, BASIC fortunately allows the printer to be set to the required mode, albeit in a rather complex way prone to many errors. There are, however, many programs that lack even the most rudimentary means to set the printer to a particular character or paper format. For such programs, the initialization aid is a useful peripheral, provided its setting is not overridden by a printer initialization string prefixed to each printable file by the program in question.

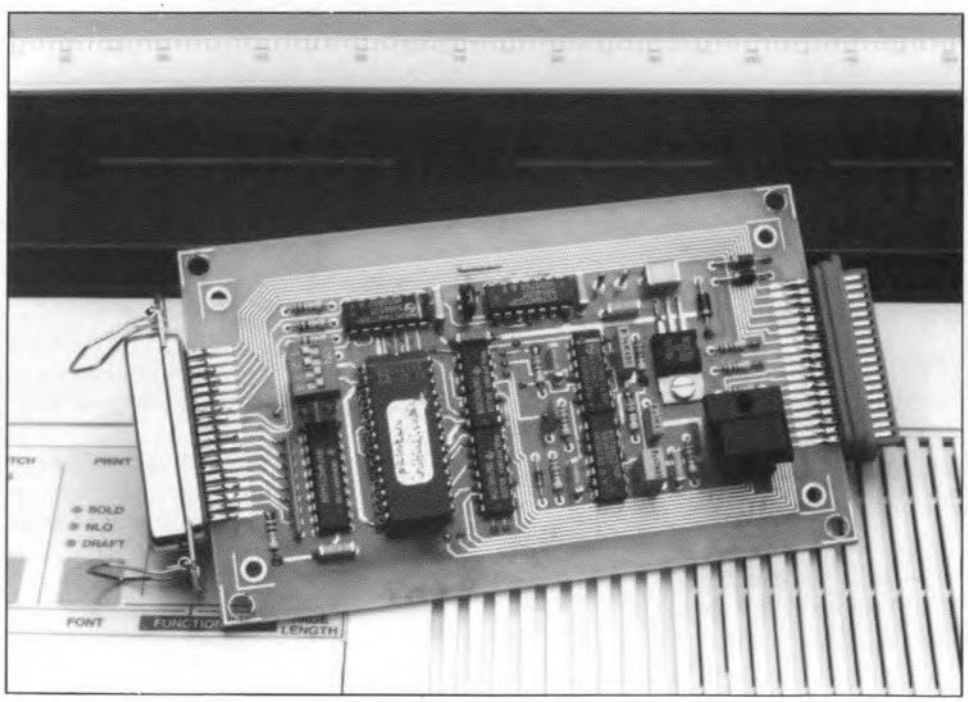
Basic operation

The flowchart in Fig. 1 illustrates the basic operation of the circuit, which is inserted between the computer's Centronics port and the parallel input of the printer. The diagram shows the functional blocks in the circuit as well as the interrelated timing at which these blocks operate.

At power-on, the circuit is reset and forms a straight 36-way connection between the computer's Centronics port and the Centronics input on the printer. No change is made to the previously established printer setting, and the computer can send printer files as before.

When S_2 is pressed, data buffer IC_8 blocks the datastream from the computer. The circuit actuates the BUSY line to force the computer to stop sending data. Meanwhile, the data outputs of the EPROM, IC_7, are enabled, so that the byte at the currently addressed location in the EPROM is sent to the printer. A strobe pulse is generated to signal to the printer that a byte is held ready for transmission. Since the start of the first strobe pulse coincides with the moment the EPROM datalines are enabled, the strobe pulse is delayed by about one microsecond to ensure stable levels on the datalines. After the $\overline{\text{STROBE}}$ output line is actuated, the circuit enters a wait loop to allow the printer to process the databyte. Depending on the position of jumper JP_1, the circuit waits for a negative pulse transition on the BUSY or $\overline{\text{ACK}}$ handshaking line from the printer. When the transition arrives, the EPROM address counter is incremented by one. The counter starts at the lowest address, nil, by virtue of the power-on reset, and the fact that the circuit stops automatically when the counter reaches nil. In the latter case, the "all 16 bytes sent?" loop in the flowchart is left via the "yes" exit, and the circuit forms a straight connection between the computer and the printer until S_2 is pressed again.

All 16 bytes stored in the EPROM are to the printer under the control of strobe pulses, which are started with the aid of the delayed BUSY or $\overline{\text{ACK}}$ printer signal. The delay allows some time for the address counter to reach the next higher output state. When all bytes have been sent, the same delay is used to reset the circuit to its start configuration.



16×16 in control

A part of the circuit drawn in Fig. 2 consist of a set of printed-circuit board tracks called the control bus. This bus takes all Centronics control signals not used by the initialization aid from the input- to the output connector. Two lines, C18 and C35, form an exception, because they may be used to power the circuit. Whether or not they can be used for this purpose depends on the printer used. Diodes D_2, D_3 and D_4 form an OR function that allows the circuit to be powered by different supplies. In case the printer lacks a +5 V output on its Centronics connector, the circuit is powered by a 9 VDC mains adapter via D_2 and voltage regulator IC_9. If the printer supplies +5 V via line C18, the circuit is powered via D_3. If +5 V is available on line C35, D_4 is used for the same purpose. The current consumption of the circuit does not exceed 50 mA.

As already discussed, the circuit is reset automatically the moment the supply voltage is present. Bistable FF_2 is reset by R_9-C_2, and in turn clears address counter IC5. Bistable FF_1 is configured as

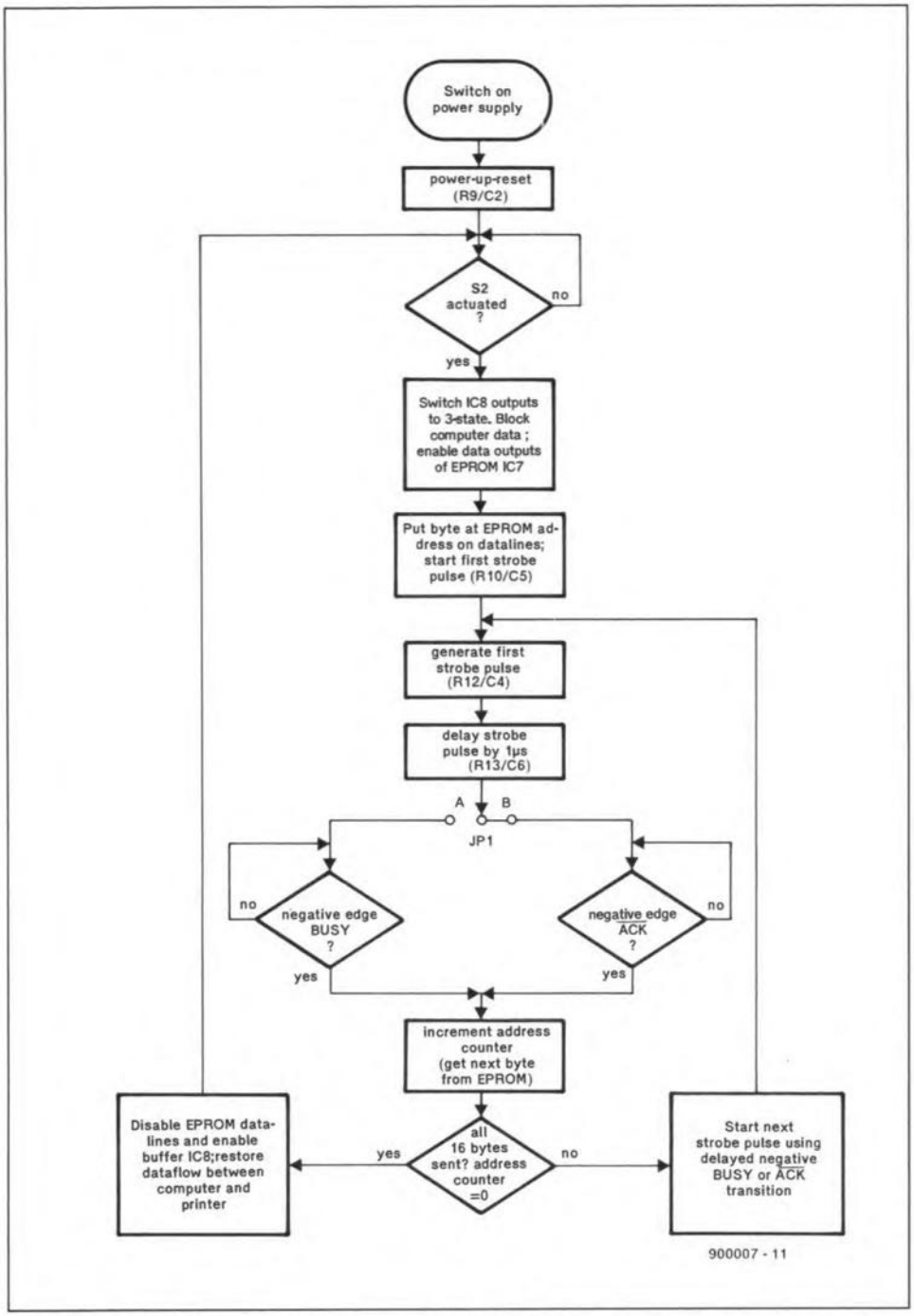


Fig. 1. This flowchart illustrates both the structure of the circuit an the pertinent timing.

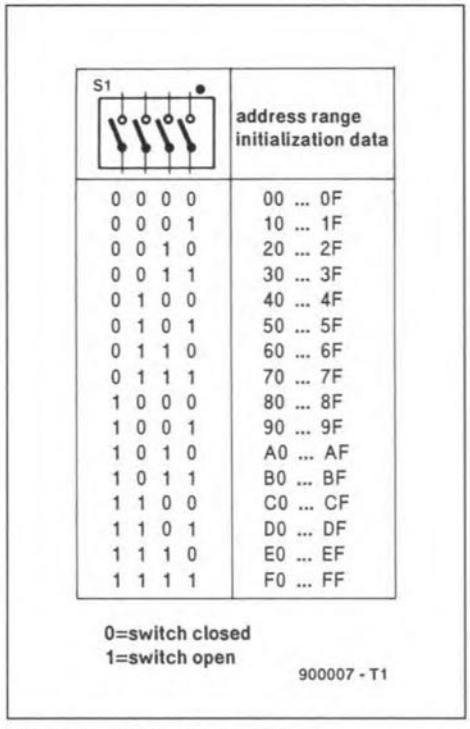


Table 1. DIP switch settings.

a monostable multivibrator (MMV) and does not require a power-on reset because it goes to the stand-by state on its own. At this stage, the circuit functions as a 36-way connection between the computer at the input (K_1) and the printer at the output (K_2). The two devices are connected via three-state inverter/buffer IC_8, inverters N_9–N_{16} and the gates inserted in handshake lines BUSY, $\overline{\text{STROBE}}$ and $\overline{\text{ACK}}$.

When S_2 is pressed, its contact noise is eliminated by debounce network R_7-C_1. The short pulse generated by C_1-R_8 prevents the initialization sequence being restarted on completion if the switch has not been released in the mean time. Actuation of S_2 causes FF_2 to be set. The resultant high level at the Q output of FF_2 causes the outputs of three-state buffer IC8 to be switched to the high-impedance state, and the BUSY and $\overline{\text{ACK}}$ inputs of the computer to be taken high by N_1-N_{17} and N_2-N_{18} respectively. The low level at the $\overline{Q}$ output of FF_2 enables the databuffers in EPROM IC_7, and ends the reset state of counter IC_5. The first strobe pulse is generated by FF_1 which receives at its $\overline{S}$ (set) input a short pulse from the $\overline{Q}$ output of FF_2 via network R_{10}-C_5. The length of the strobe pulse is determined by R_{12}-C_4. Capacitor C_4 slowly discharges after FF_1 has been set, and resets the bistable. Consequently, output $\overline{Q}$ goes high, so that C_4 is rapidly charged again via D_1. This ensures that FF_1 is ready to generate the next strobe pulse.

The strobe pulse is delayed by about one microsecond in network R_{13}-C_6 to allow sufficient time for the EPROM data to reach output connector K_2. Gates N_8 and N_{19} feed the strobe pulse to the printer.

The circuit waits until the printer is ready to accept a new command by monitoring either BUSY or $\overline{\text{ACK}}$. The selection between these handshaking signals is made by the user with jumper JP1; the two are equally suitable, provided the printer supplies the relevant signal. Whatever signal is used, the negative pulse edge signals readiness to accept a new character. The pulse edge clocks address counter IC_5 and causes a new strobe pulse to be generated. The start of the strobe pulse is, however, delayed by R_{11}-C_3 to prevent another pulse being generated when the 16th (last) byte has been sent to the printer. This delay is used by the circuit to block FF_1 before it receives a new clock pulse. The end of the printer initialization sequence is marked by output QD of the address counter going low when count 16 is passed. The change from 16 to 0 causes FF_2 to be clocked, so that FF_1 is blocked — hence, the clock pulse generated in the mean time by R_{11}-C_3 has no effect. The toggling of FF_2 also resets the circuit to its initial state.

The circuit is fully compatible with the Centronics interface on the computer as well as on the printer by virtue of pull-up resistors and open-collector TTL drivers respectively. DIP switch block S_1 selects one of 16 printer initialization strings which have been pre-programmed in the EPROM. The selected address ranges in the EPROM are listed in Table 1. If frequent changes are expected in the setting of this switch, it may be replaced with a more ergonomical type or a set of switches, e.g., four miniature SPST types or a thumbwheel switch.

Construction

The construction of the circuit on the double-sided, through-plated printed-cir-

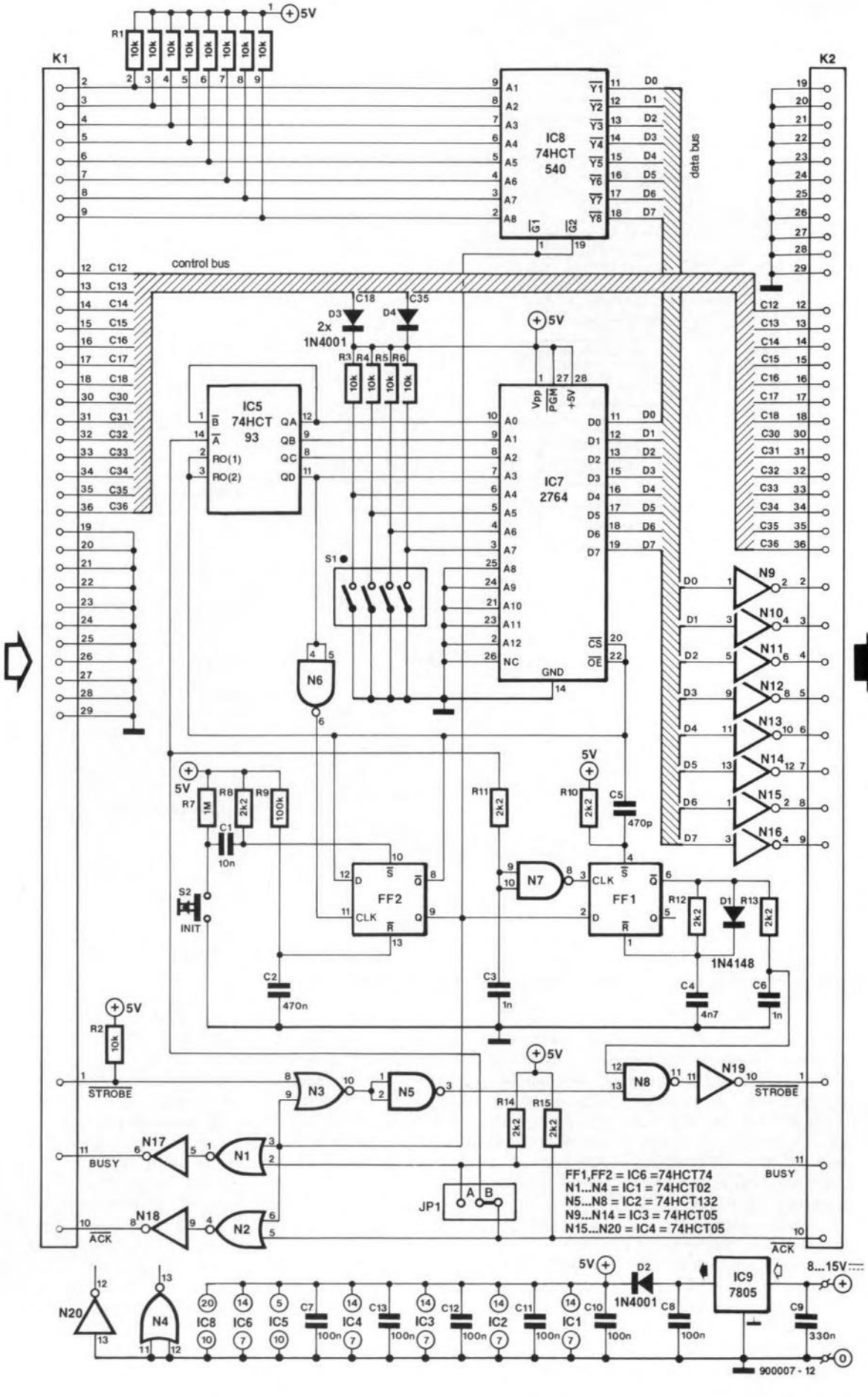


Fig. 2. Circuit diagram of the printer initialisation aid, a very useful peripheral device for advanced computer users.

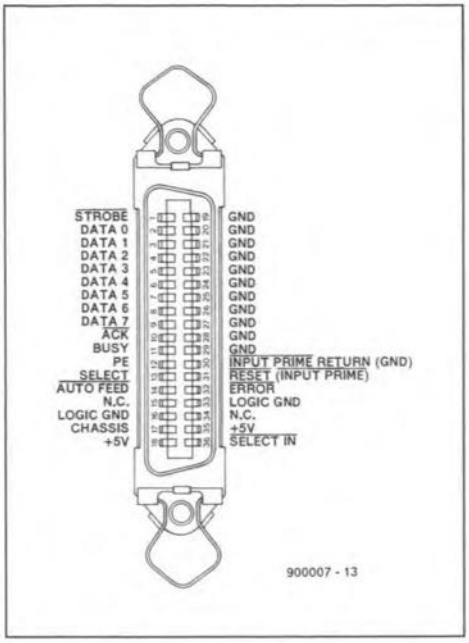


Fig. 3. Centronics connector pinning.

cuit board shown in Fig. 4 is straightforward. The pins of the Centronics connectors are simply pushed over the relevant copper fingers at the edges of the board (mind the position of pin 1 of each connector). Next, solder the fingers to the pins, taking good care to avoid short-circuits between adjacent pins. Bolt the voltage regulator direct on to the board — a heatsink is not required.

Printer command strings

Upon completion of the board, the EPROM must be loaded with data. The manual supplied with your printer should give ample information on command strings to achieve the settings you require. The circuit allows a maximum of 16 command strings to be programmed, each with a fixed length of 16 bytes. The mini EPROM programmer described in Ref. 1 is suitable for loading the 256 bytes. If the required initialization sequence is shorter than 16 bytes, the remainder must provide null characters (00), or any other character which is ignored by the printer (again, consult your manual).

The sequence of commands to be programmed in the EPROM Type 2764 is first tested 'on line' with the aid of, say, GWBASIC. Document the final versions of the command strings. Next, compile the

```
10 RESTORE
12 OPEN "lpt1:" FOR OUTPUT AS #1
20 FOR N=1 TO 16
30 READ X
40 PRINT #1,CHR$(X);
50 NEXT N
55 CLOSE
60 DATA &H54,&H45,&H53,&H54
65 DATA &H00,&H00,&H00,&H00
70 DATA &H54,&H45,&H53,&H54
75 DATA &H00,&H00,&H00,&H00
```

900007 - 14

Fig. 5. GWBASIC test program listing.

databytes to be programmed from

databyte = 255–data.

This inverts each byte to negate the inversion in the output buffers.

Reference:

1. Mini EPROM programmer. *Elektor Electronics* January 1990.

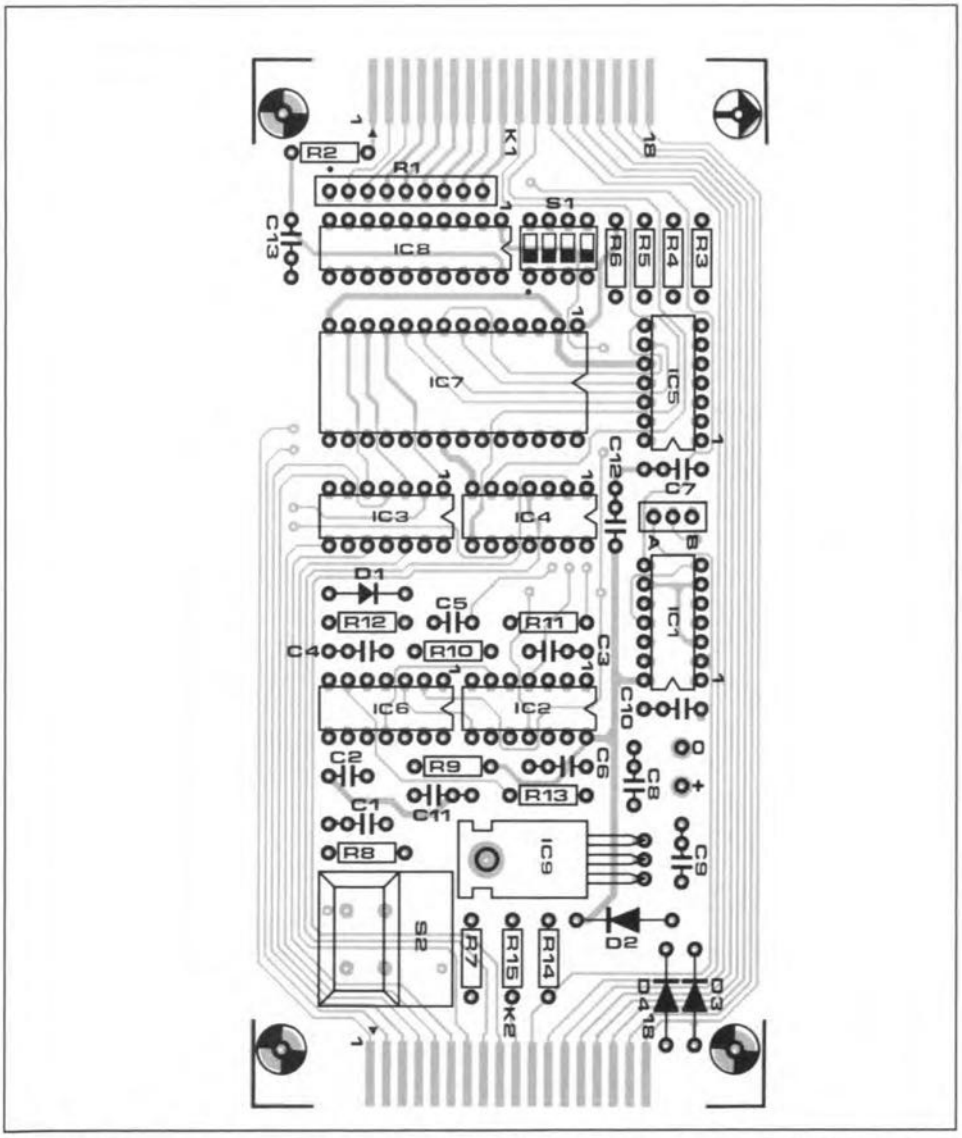


Fig. 4. Component mounting plan for the double-sided, through-plated circuit board.

Parts list

Resistors:
R_1 = SIL resistor array 8×10k
$R_2 - R_6$ = 10k
R_7 = 1M0
R_8;R_{10};$R_{11} - R_{15}$ = 2k2
R_9 = 100k

Capacitors:
C_1 = 10n
C_2 = 470n
C_3;C_6 = 1n0
C_4 = 4n7
C_5 = 470p
C_7;C_8;$C_{10} - C_{13}$ = 100n
C_9 = 330n

Semiconductors:
D_1 = 1N4148
D_2;D_3;D_4 = 1N4001
IC_1 = 74HCT02
IC_2 = 74HCT132
IC_3;IC_4 = 74HCT05
IC_5 = 74HCT93
IC_6 = 74HCT74
IC_7 = 2764 or 27C64(A)
IC_8 = 74HCT540
IC_9 = 7805

Miscellaneous:
K_1 = 36-way female Centronics connector with straight pins.
K_2 = 36-way male Centronics connector with straight pins.
S_1 = 4-way DIP switch block.
S_2 = ITW Dataswitch push-button.
3-way pin header.
Jumper.
PCB Type 900007 (double-sided; through-plated; see Readers Services page).

CAPACITANCE METER

D. Folger

A capacitance meter is indispensable for checking capacitors with illegible or incomprehensible values printed on them, and for matching capacitors in, for instance, higher-order filters. The instrument presented here is based on a simple circuit, has a handy size and five measurement ranges.

To own a capacitance meter with a maximum error of 1% and a capacitance range of 1 pF to 1 F is wishful thinking for many electronics enthusiasts because such an instrument is not affordable, if it is at all available. Fortunately, not many applications require a capacitance meter with such impressive specifications. Consider, for instance, the selection of capacitors for a higher-order audio filter: here, the relative difference is much more important than the absolute value, and a simple capacitance meter may be used with impunity to select matching capacitors from an available lot.

Measurement principle

The measurement principle used is fairly standard — see Fig. 1. The heart of the circuit is formed by a time-base which triggers a monostable multivibrator (MMV). The time constant, t, of the time base is set to a value that exceeds the maximum monostable delay. The MMV output changes from low to high on the negative edge of the time-base signal. The time it takes for the MMV to revert to the start state, t_w, is proportional to the value of the capacitor under test, C_x. Since the duration of the measurement cycle is determined by t, an integrator may be used to provide a voltage which is proportional to the value of C_x.

MAIN SPECIFICATIONS

Measurement ranges:	2 nF; 20 nF; 200 nF; 2 µF; 20 µF with overflow indication
Max. resolution:	1 pF
Max. error:	≤5%
Display:	3½ digit LCD
Scale factor:	nF/µF
Power supply:	9-V PP3 battery
Current consumption:	10–20 mA

Circuit description

In spite of the relatively simple measurement principle described above, the practical circuit presents a number of possible problems related to the translation of the unknown capacitance into an accurately determined numerical value.

The time-base is formed by a 1-MHz quartz crystal and an oscillator/divider, IC2. Output Q13 supplies a frequency of 1 MHz/16,384 = 61.035 Hz. This signal triggers IC3b, one of two MMVs contained in the Type TLC556 LinCMOS dual timer. The choice of the oscillator frequency is a compromise between the stability of the read-out and acceptable current consumption when relatively large capacitances are measured.

Given a time constant

$t = 1/61.035 = 16.4$ ms,

a maximum monostable time of 10.5 ms and a maximum capacitance of 20 µF, the resistor R in the RC delay network is simple to calculate from

$t_w = 1.1RC$

$R = 10.5/(1.1 \times 20\ \mu F) = 477\ \Omega$

A practical value of 475 Ω (1%) is used since this is available in the E96 series. The other measurement ranges are created by multiplying the basic value of R by the capacitance range factor, i.e., 10: R = 4k75 for the 2 µF range; R = 47k5 for the 200 nF range, R = 475k for the 20 nF range; R = 4M75 for the 2 nF range.

The output signal of IC3b has a duty factor t_w/t and requires averaging to obtain a direct voltage proportional to the duty factor and, therefore, to the value of C_x. Integration capacitor C12 is charged via potential divider R14-P3-R15 if the MMV output is high, and discharged if the MMV output is low. This arrangement produces an average voltage,

$U_2 = U_{1(H)}(t_w/t)$

Note, however, that because of the adjustable potential divider the high level, $U_{1(H)}$, is lower than the high output level provided by the MMV. The maximum value of U_2 is not reached immediately, but after a delay af about 600 ms, which corresponds roughly to the time constant of the integration network.

The 150 pF capacitor connected in parallel with C_x is required as a minimum capacitance in the external RC network of the LinCMOS timer. Without C8, the MMV may not be triggered reliably if small capacitors (in the pF range) are tested. The resultant off-set is compensated with the aid of a second MMV, IC3a, of which the external configuration is almost identical to that of IC3b.

The low voltage, U_L, at the output of the second integrator is used as a reference for U_H. Capacitors C7 and C8 and resistors R4–R12 determine the time delays set with the MMV, and must, therefore, be close-tolerance types.

Spurious triggering and incorrect capacitance indications may occur if measured values exceed the maximum of a particular range. Each measurement cycle is, therefore, stopped after 12 ms. As shown in Fig. 3, the remaining 4 ms are used to discharge the capacitor under test via FET T2. The timing of the discharge

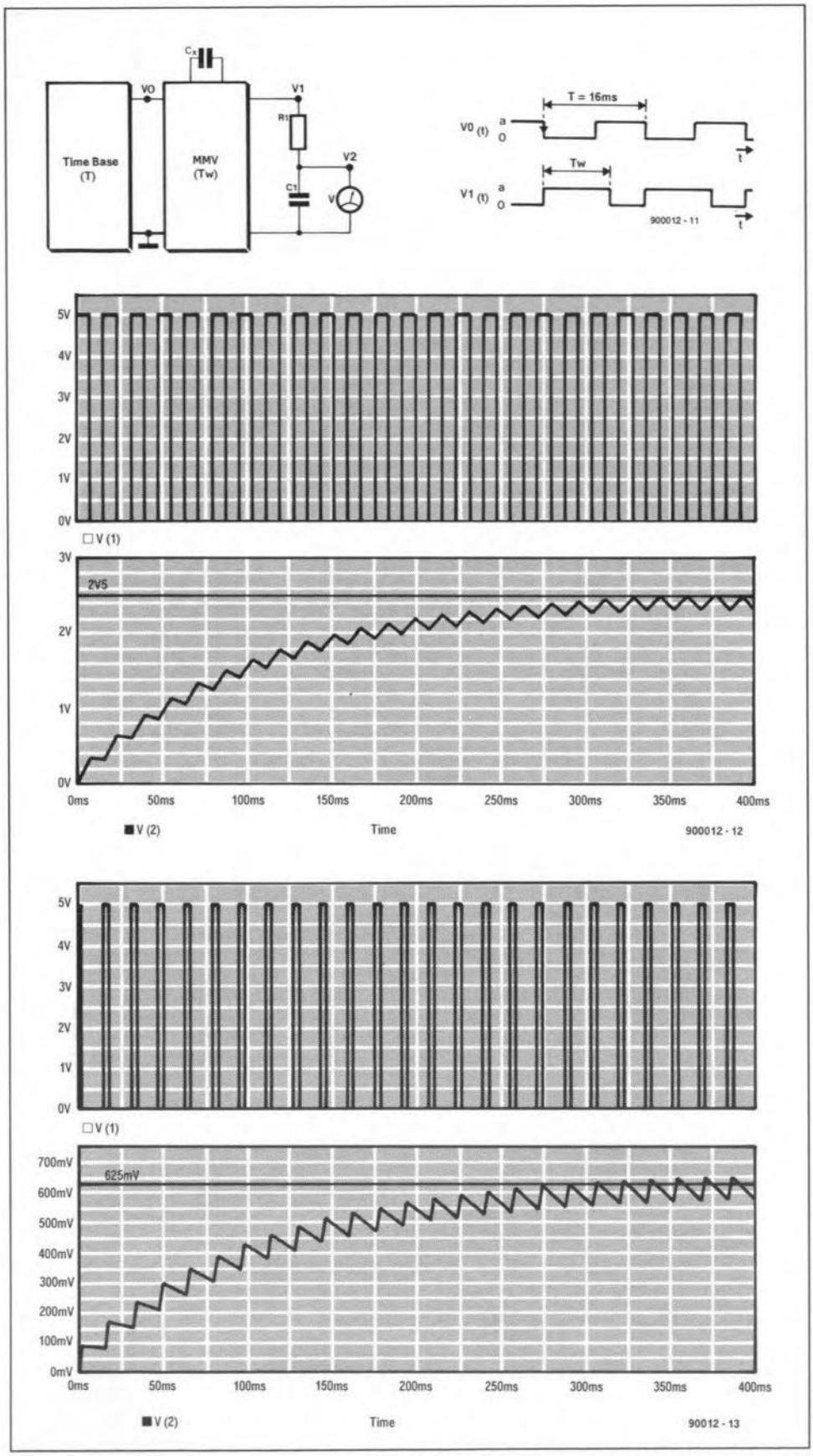
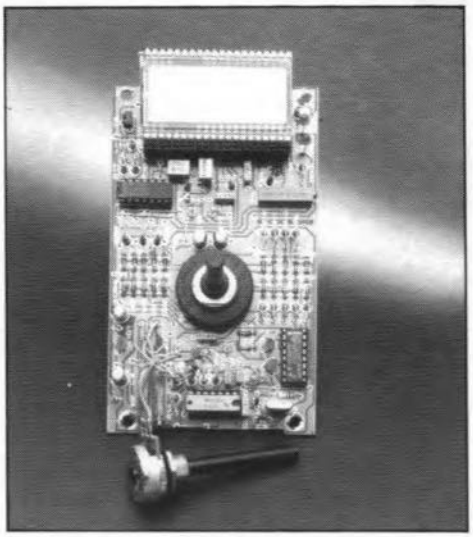


Fig. 1. Measurement principle and graphs to illustrate the operation of the *R-C* integrator.

period is arranged by the AND diode configuration of D_3 and D_4 at the Q12- and Q13-outputs of IC_2. These diodes cause the MMV output to remain permanently high when a too large capacitor is connected. In this condition, the voltage at the two MMV outputs causes the LC display to indicate '1'. The measurement error introduced by T_2 is compensated by its counterpart, T_1, in the other MMV circuit.

The display circuit is based on the well-known Type ICL7106 A-D (analogue-to-digital) converter with integrated 3½-digit LCD (liquid crystal display) driver. The ICL7106 is used in a standard application circuit with the decimal point



switching arranged by S_{2b}, D_{15}–D_{19} and N_1–N_4. The scale factor (nF or µF) indicators, D_1 and D_2, are driven by a diode circuit, D_{20}–D_{24}.

The power supply of the circuit is of a less usual configuration: a Type 79L05 voltage regulator is inserted in the negative supply line to create a supply with +5 V and −4 V outputs. The non-regulated negative voltage is applied as bias to the ADC in the ICL7106, which requires that the voltage at the V− input (pin 26) is always 1 V below that at IN HI.

The circuit around T_3 controls the LOW BAT symbol on the display. With R_{19}=220k, this circuit is actuated when the battery voltage drops below about 8 V.

Construction and adjustment

The complete circuit is built on a printed-circuit board that fits into an ABS, standard-size hand-held enclosure with integral battery compartment. The circuit to the right of the dashed line in the circuit diagram, and diodes D_{15}–D_{24}, may be omitted if the capacitance meter is used in conjunction with a digital multimeter that assumes the display function.

The population of the PCB should not present problems. The high-value 1% resistors, R_8 and R_{12} (4.75 MΩ), may be difficult to obtain in small quantities. They may, however, be selected from a batch of 4.7 MΩ 5% types with the aid of a DMM.

Fit two four- or five-way terminal blocks on to the front panel of the enclosure for connecting the capacitors to be tested. Be sure to use high-quality terminals to avoid problems with wear and tear of the contacts. A two-way loudspeaker terminal block for wire insertion is a fine alternative to multi-way blocks since it provides fairly wide contacts which allow capacitors with different terminal spacings to be inserted.

Large capacitors of which the wires can not be inserted into the terminal blocks on the instrument must be connected with test leads. Do not use these leads for small capacitors, since the wire capacitance will make the indicated value worthless. P_1 is

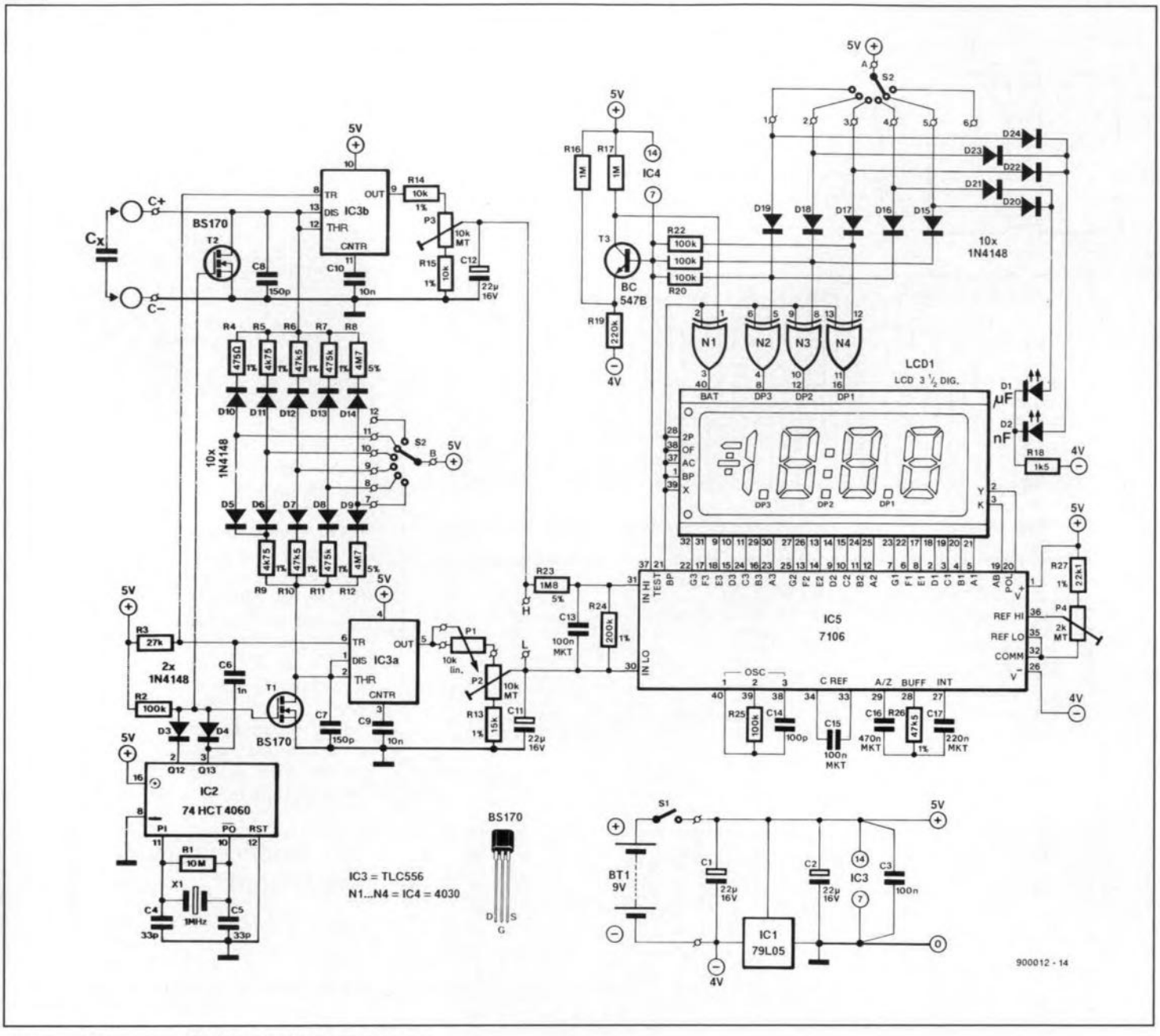


Fig. 2. Circuit diagram of the capacitance meter.

either a preset with an adjustment spindle or a potentiometer with a 4 mm spindle. It allows test lead capacitance to be compensated.

The accuracy of the instrument is determined mainly by the quality and tolerance of resistors R9–R12.

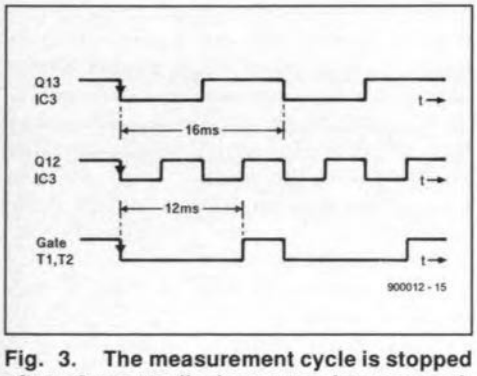
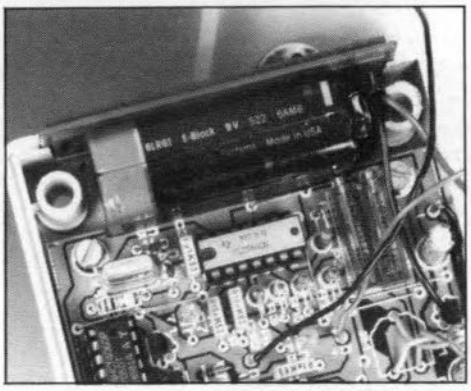


Fig. 3. The measurement cycle is stopped after 12 ms to discharge too large capacitors.

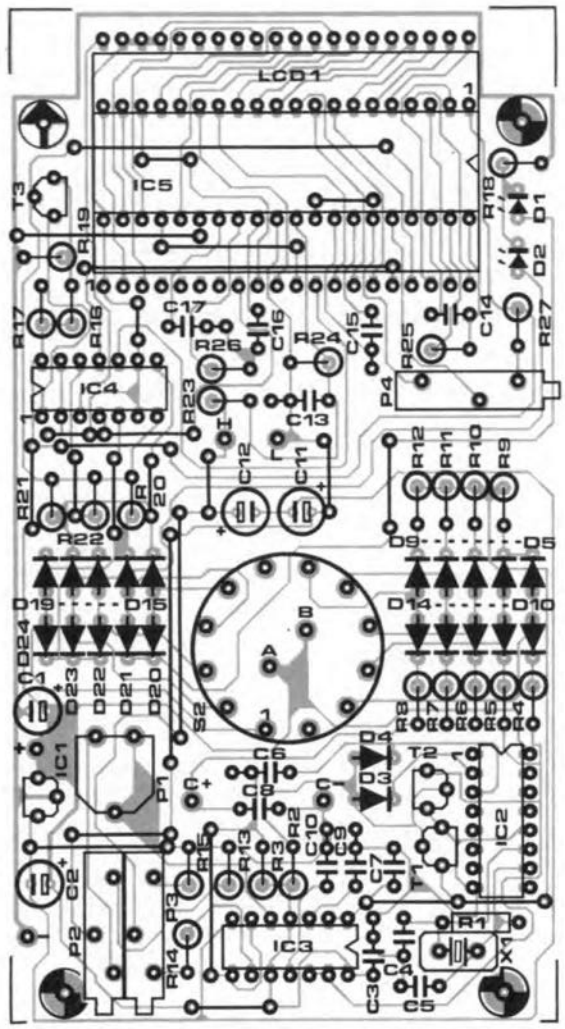
Connect a 1% or 2% polystyrene (styroflex) or silver-mica capacitor with a known value in the lowest measurement range (e.g., 1 nF). Set S_2 to the 2 nF range, set P_1 to the centre of its travel and P_2 and P_3 to maximum resistance to ground. Connect the reference capacitor, and adjust P_4 until the correct value is displayed. Disconnect the reference capacitor and adjust the zero-indication of the meter with P_2. Repeat the adjustments of P_2 (capacitor connected) and P_4 (capacitor disconnected) until the indicated value and the zero indication are both correct.

DMM as display

The value of the test capacitor must be adjusted with P_3 instead of P_4 if a DMM set to the 2 V range is connected to points L and H. The 'meter-zero' control, P_1, is replaced by a 5.11 kΩ 1% resistor in this case because the adjustments for meter zero and capacitor value interact. Set P_3 to maximum resistance to ground, and adjust P_2 until the DMM reads 0 V. Connect the reference capacitor and adjust P_3 until the correct value is indicated. Repeat the adjustments of P_2 and P_3 as detailed above for P_2 and P_4.



Close-up of the battery compartment.



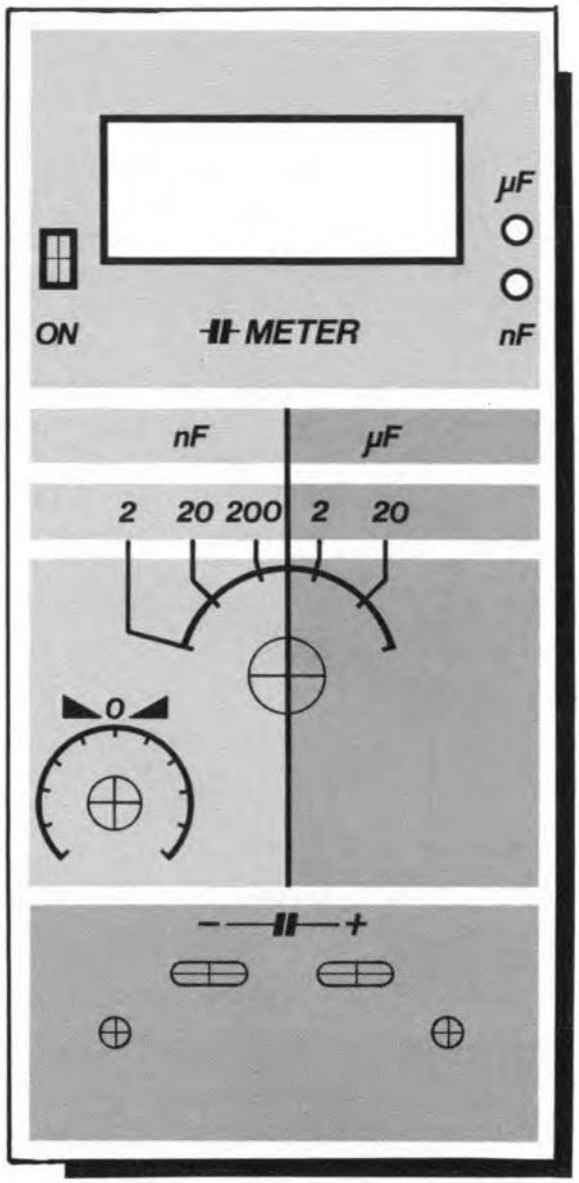


Fig. 4. Component mounting plan of the printed-circuit board for the capacitance meter (left) and suggested front-panel lay-out (right).

Parts list

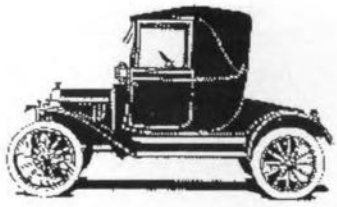
Resistors:
R_1 = 10M
R_2;R_{20};R_{21};R_{22};R_{25}=100k
R_3 = 27k
R_4 = 475Ω 1%
R_5;R_9 = 4k75 1%
R_6;R_{10};R_{26} = 47k5 1%
R_7;R_{11} = 475k
R_8;R_{12} = 4M7 5% (see text)
R_{13} = 15k 1%
R_{14};R_{15} = 10k 1%
R_{16};R_{17} = 1M0
R_{18} = 1k5
R_{19} = 220k
R_{23} = 1M8 5%
R_{24} = 200k 1%
R_{27} = 22k1 1%
P_1 = 10k linear potentiometer with 4 mm spindle or 10k preset for horizontal mounting with spindle.
P_2;P_3 = 10k multiturn preset
P_4 = 2k multiturn preset

Capacitors:
C_1;C_2;C_{11};C_{12} = 22µ; 16 V; radial
C_3 = 100n
C_4;C_5 = 33p
C_6 = 1n0
C_7;C_8 = 150p polystyrene (styroflex)
C_9;C_{10} = 10n
C_{13};C_{15} = 100n MKT
C_{14} = 100p
C_{16} = 470n MKT
C_{17} = 220n MKT

Semiconductors:
D_1;D_2 = LED; 3 mm; red
D_3 – D_{24} = 1N4148
T_1;T_2 = BS170
T_3 = BC547B
IC_1 = 79L05
IC_2 = 74HCT4060
IC_3 = TLC556 (LinCMOS)
IC_4 = CD4030
IC_5 = ICL7106

Miscellaneous:
S_1 = miniature slide SPST slide switch.
S_2 = 2-pole 6-way PCB-mount rotary switch.
X_1 = 1 MHz quartz crystal.
LCD_1 = general-purpose 3½-digit LC display.
9-V PP3 battery with clip and leads.
Hand-held ABS enclosure, e.g., Monacor PLG750BN (160×80×75 mm).
Loudspeaker terminal block.
PCB Type 900012 (see Readers Services page).

CAR THEFT DETERRENT



by David Butler

Cars seem to attract thieves, probably because of the relative ease of entering them. Anyone who has locked their keys inside will testify that a bent coathook can usually secure an early reunion. The deterrent proposed is aimed at discouraging casual joyriders who want not want to risk setting off an alarm – even if, as here, one did not exist. In fact, the deterrent is simply an alarm type indication that, if accompanied by suitable warning stickers, should provide basic protection. It must be stressed, of course, that this deterrent does not act as an alarm and it would be wise to invest in a security system, such as an immobilizer or a Krookloc.

The idea of a dummy alarm is not new, but the present design adds more credibility by the use of a single dual function LED. When the ignition is on, the LED radiates a steady green light to show that the 'system' is 'disarmed'. When the ignition is switched off, the LED emits a flashing red light to simulate 'alarm enable'.

The success of this idea rests with displaying the LED prominently (say, next to the ignition switch) and not telling anybody that it is just a flashing light! The project is inexpensive, simple to construct and install, and performs a worthwhile function.

Features:

Deters casual joyriders from stealing your vehicle.

Inexpensive, simple design.

Compact dimensions.

Easy to install (3 wires).

Circuit description

The circuit is designed around a dual function LED. This device looks like a normal 5 mm diameter clear LED, but has three terminals. The casing actually houses a green LED and a red LED driven by a flasher unit. The cathodes of the LEDs are commoned to the centre pin. When a voltage in the range 4.75–7.0 V is applied to the 'R' terminal, the red LED will flash at a rate of about 1.5 Hz. The green LED is connected to the other terminal (indicated by a flat on the casing) and requires a series current limiting resistor to operate from any supply.

The relay used is of extremely small dimensions, and has a single-pole change-over contact set. The coil is energized by the +12 V ignition circuit in the car, with back e.m.f. protection provided by D2.

The LED terminals are connected to the relay contact set so that normally the red flashing LED is actuated (ignition off state). The regulator circuit formed by R1, D1 and C1 provides a fixed voltage for both LEDs. This was chosen to avoid problems

COMPONENTS LIST

Resistors:
R1 = 390R; 0.25 W; ±5% or better; carbon
R2 = 220R; 0.25 W; ±5% or better; carbon

Capacitor:
C1 = 100n; ceramic

Semiconductors:
D1 = 5V1; 400 mW; zener diode
D2 = 1N4001
LED1 = continuous green/flashing red LED
(Maplin Electronics order code QY99H)

Miscellaneous:
RLA = micro miniature single pole change-over contacts; 12 V 320R coil
(Maplin Electronics order code BK47B)
PL1 = 4-way right-angle PCB type plug
SK1 = 4-way housing plus contacts
5 mm LED clip
PCB or veroboard
In-line fuseholder with 150 mA 20 mm fuse (if required)

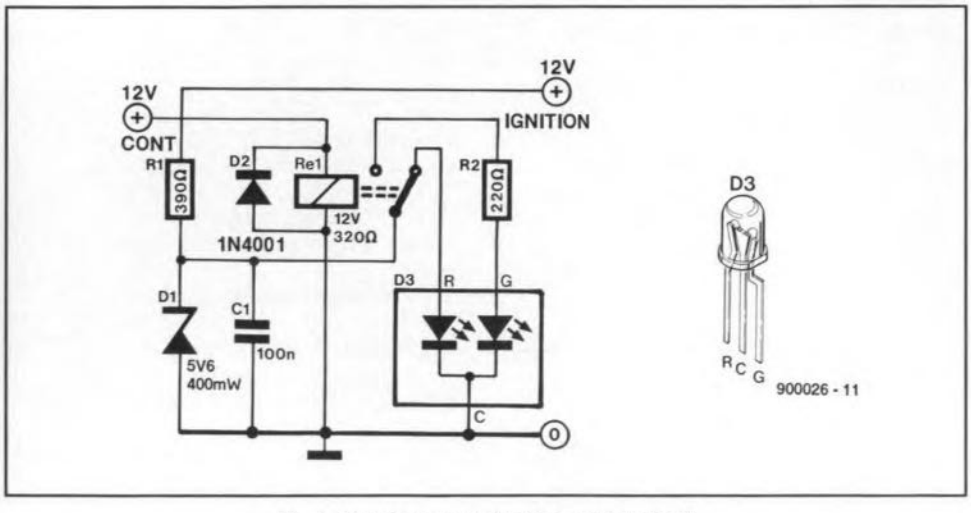


Fig. 1. Circuit diagram (ignition switched off).

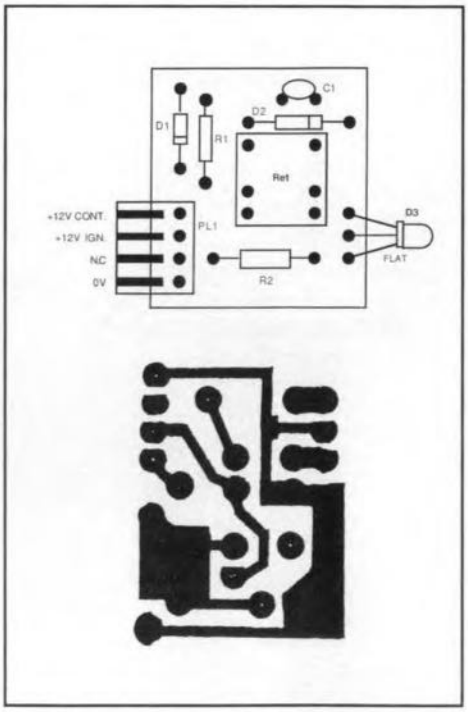


Fig. 2. Printed-circuit board of the deterrent. The component side is shown true to scale.

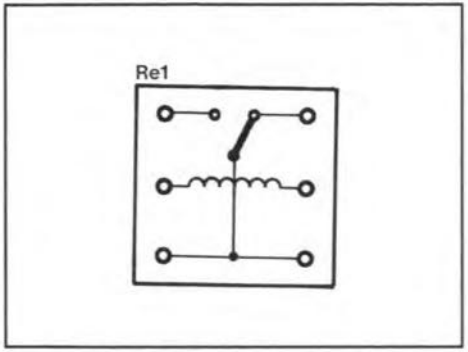


Fig. 3. Pinout of the relay (seen from the base.)

with the car's voltage supply.

The circuit consumes about 50 mA when the ignition is on and around 15 mA with the ignition switched off.

Construction notes

The prototype was constructed on a scrap of vero board and then transferred on to a PCB (see Fig. 2). Although the method of construction is not important, care should be exercised in connecting the polarized components: D_1, D_2 and the LED.

Installation notes

The prototype unit was installed in the author's Metro, which conveniently has a spare blanking plate next to the rear screen heater switch. This is quite close to the ignition switch and would be instantly noticed by any curious potential thief.

No doubt, other vehicles will have similar places to mount the LED, which requires a 6.35 mm dia. hole.

Once the LED is mounted, three wires run from the PCB may be connected to it with the aid of Scotchlock type break-in terminals. Usually, the set of wires leading to the radio can be used: +12 V continuous means that +12 V is available even when the ignition is switched off; +12 V ign means that the +12 V line is switched via the ignition.

For extra electrical protection an in-line fuse holder with a 150 mA fuse may be used: this rating depends on that of the car fuse fitted to the circuit being used.

Apart from these brief notes, no other fitting instructions can be given as each vehicle will vary.

Generally, the unit should be fitted away from sources of direct heat, with the LED displayed in a prominent position where it does not distract the driver.

CALSOD NOW EVEN MORE VERSATILE

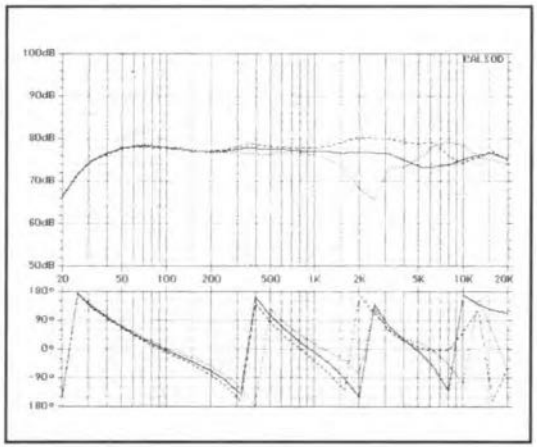
EA-742

The computing and optimalization of loudspeaker enclosures is nowadays normally effected by computer. One of the programs that enables the complex calculations to be carried out on an IBM PC desktop computer is CALSOD, the first version of which was reviewed in this magazine last year. We have recently received an improved version of this program that offers even more possibilities to the professional designer to approach realistic sound reproduction.

Designing loudspeaker enclosures requires such extensive measurements and calculations nowadays that it has become virtually impossible without the use of a computer and a suitable program. Last year we reviewed* CALSOD, a unique combination of a simulation and an optimalization program. We then thought that there was very little left to be desired. None the less, the designers have succeeded in adding some more facilities to their latest version 2.00, which bring the results even more closely to realistic sound reproduction.

The new version offers the possibility of working with a coprocessor. This is an especially welcome addition for XTs, since computations on these of three- or four-way systems are relatively slow (but still a lot faster than with comparable programs). However, this facility is merely to do with speed of processing.

To us, the most interesting addition is the RAB sub-module. This makes it possible to calculate the frequency characteristic of the entire system at a given angle (both horizontal and vertical) with respect to the listening axis, for instance, ±30°. Even in the optimalization of the filters this off-axis response may be taken into account. It is thus possibe, for example, to design a filter whose characteristic remains within certain limits for an off-axis response of ±10° with respect to the listening axis (see illustration above).



The loudspeaker placement has also been extended. The original version enables the loudspeaker location to be calculated in a three-dimensional space: the new version makes it possible to take into account that loudspeakers are placed at an angle (for instance, in case of a backward sloping enclosure front). Also, the effective diameter of the drive units may be taken into account, so that the program may make provision for the radiation pattern of each individual drive unit.

Apart from optimalization of the filter components to obtain a given characteristic, it is now also possible to optimalize the impedance of an individual loudspeaker or of the entire system. To that end, compensation networks are added that are calculated by the computer in a manner that keeps the impedance in a predetermined frequency range within a given percentage of a certain value. This is a very useful facility for compensating the behaviour of individual loudspeakers and for straightening out the impedance characteristic of a complete system, to ensure that the power amplifier is connected to a truly resistive load.

There is also a 'student' version (1.20) of the program available at a sharply reduced price ($A99.00). This version offers all the facilities we have discussed. Its data files are compatible with Version 2.00 ($A349.00) so that transfer to the professional version at a later date is facilitated.

CALSOD is available from the designers, **Audiosoft, 128 Oriel Road, West Heidelberg 3081, MELBOURNE, Australia.** It may also be obtained from **Old Colony Sound Lab, P O Box 243, PETERBOROUGH NH 03458, USA**, or, in Europe, from **Audio Specialists, Weichselstrasse 22, 1000 BERLIN, Federal Germany.**

**Elektor Electronics*, January 1989, p. 62

INTRODUCING OP-SERIES OPAMPS

J. Ruffell

Dozens of new, improved operational amplifiers are introduced every month by leading IC manufacturers around the world. A number of high-performance opamps from the 'young' OP-series are described in relation with construction projects featured in this magazine over the past year or so. The reasons for preferring these new devices over, say, a Type 741 are manifold and call for an introduction to opamp selection criteria.

Designing a wide variety of clever electronic circuits on the basis of ideal operational amplifiers is fairly easy. In not a few cases, however, the efforts remain paper designs after the disappointing results obtained with practical constructions. The problem is clear: the ideal opamp does not exist. The ideal model does have its uses, however, because it allows the operation of complex circuits based on opamps to be analysed and understood.

In practice, the ideal opamp is only useful for the design of low-performance circuits, and for function analyses. In all other cases, the most important non-ideal characteristics must be taken into account. The relative importance of all the design parameters involved depends on the type of circuit in which the opamp is to be used. In an alternating-voltage amplifier, for instance, off-set drift is less important than the slew rate. Conversely, the performance of a DC amplifier is limited by off-set drift rather than the slew rate.

Distinguishing between the important and the not so important opamp characteristics on the basis of the function of the circuit not only raises the quality of the final product, but also avoids needlessly complex calculations. Clearly, a well-

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \le T_A \le +125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-07A MIN	OP-07A TYP	OP-07A MAX	OP-07 MIN	OP-07 TYP	OP-07 MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	25	60	—	60	200	μV
Average Input Offset Voltage Drift Without External Trim	TCV_{OS}	(Note 2)	—	0.2	0.6	—	0.3	1.3	μV/°C
With External Trim	TCV_{OSn}	$R_P = 20k\Omega$ (Note 3)	—	0.2	0.6	—	0.3	1.3	μV/°C
Input Offset Current	I_{OS}		—	0.8	4	—	1.2	5.6	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 2)	—	5	25	—	8	50	pA/°C
Input Bias Current	I_B		—	±1	±4	—	±2	±6	nA
Average Input Bias Current Drift	TCI_B	(Note 2)	—	8	25	—	13	50	pA/°C
Input Voltage Range	IVR		±13	±13.5	—	±13	±13.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	106	123	—	106	123	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	5	20	—	5	20	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$, $V_O = \pm 10V$	200	400	—	150	400	—	V/mV
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±12	±12.6	—	±12	±12.6	—	V

NOTES:
1. OP-07A grade V_{OS} is measured approximately one minute after application of power. For all other grades V_{OS} is measured approximately 0.5 seconds after application of power.
2. Sample tested.
3. Guaranteed by design.

Parameter	Conditions	LM741A/LM741E Min	LM741A/LM741E Typ	LM741A/LM741E Max	LM741 Min	LM741 Typ	LM741 Max	LM741C Min	LM741C Typ	LM741C Max	Units
Input Offset Voltage	$T_A = 25°C$ $R_S \le 10\ k\Omega$ $R_S \le 50\Omega$		0.8	3.0		1.0	5.0		2.0	6.0	mV mV
	$T_{AMIN} \le T_A \le T_{AMAX}$ $R_S \le 50\Omega$ $R_S \le 10\ k\Omega$			4.0			6.0			7.5	mV mV
Average Input Offset Voltage Drift				15							μV/°C
Input Offset Voltage Adjustment Range	$T_A = 25°C$, $V_S = \pm 20V$	±10				±15			±15		mV
Input Offset Current	$T_A = 25°C$		3.0	30		20	200		20	200	nA
	$T_{AMIN} \le T_A \le T_{AMAX}$			70		85	500			300	nA
Average Input Offset Current Drift				0.5							nA/°C
Input Bias Current	$T_A = 25°C$		30	80		80	500		80	500	nA
	$T_{AMIN} \le T_A \le T_{AMAX}$			0.210			1.5			0.8	μA
Input Resistance	$T_A = 25°C$, $V_S = \pm 20V$	1.0	6.0		0.3	2.0		0.3	2.0		MΩ
	$T_{AMIN} \le T_A \le T_{AMAX}$, $V_S = \pm 20V$	0.5									MΩ
Input Voltage Range	$T_A = 25°C$							±12	±13		V
	$T_{AMIN} \le T_A \le T_{AMAX}$				±12	±13					V
Large Signal Voltage Gain	$T_A = 25°C$, $R_L \ge 2\ k\Omega$ $V_S = \pm 20V$, $V_O = \pm 15V$ $V_S = \pm 15V$, $V_O = \pm 10V$	50			50	200		20	200		V/mV V/mV
	$T_{AMIN} \le T_A \le T_{AMAX}$, $R_L \ge 2\ k\Omega$, $V_S = \pm 20V$, $V_O = \pm 15V$ $V_S = \pm 15V$, $V_O = \pm 10V$ $V_S = \pm 5V$, $V_O = \pm 2V$	32 10			 25 			 15 			V/mV V/mV V/mV

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Fig. 1. Main specifications of the OP07 and OP07A compared to those of the 741A/E/C.

founded choice can only be made on the basis of knowledge and experience.

Infinite amplification and input impedance and zero output impedance are probably familiar terms in relation to opamps. The real thing, however, starts with off-set voltages, input bias currents, noise, slew rate, and many other factors.

Opamp technology

Several integration technologies are used in the production of opamps. In their quest for the ideal opamp, manufacturers are faced with a real dilemma: improvement of one opamp characteristic results in degradation of another. Inevitably, a particular integration technology is linked with near-optimum performance in one or a few respects only. A clear example of this vicious circle is that an increase of the slew rate is inevitably coupled to increased current consumption. Although not all opamp characteristics can be optimized at the same time, today's production techniques do allow improvements in the performance to be achieved if the aim is clearly defined. This results in a particular opamp performing better than another in the same application. The use of the most favourable production technology for a particular characteristic has resulted in many opamp families with many members. Currently, the four major technologies are bipolar, BiFET, BiMOS and LinCMOS (Ref 1).

Off-set and drift

Bipolar opamps such as the ubiquitous 741 consist of npn and pnp transistors. Bipolar amplifiers have the best specifications as regards stability of the input off-set voltage. This characteristic is often referred to as input voltage drift, or the temperature co-efficient, dU_{os}/dT, of the input off-set voltage.

Field-effect transistors are less easy to match than bipolar transistors, and as a result BiMOS and BiFET opamps generally suffer from the resultant drift effects. Modern bipolar opamps such as the Type OP07 are specified for a maximum off-set voltage drift of 1.3 µV/K, although values better than 0.2 µV/K are no exception.

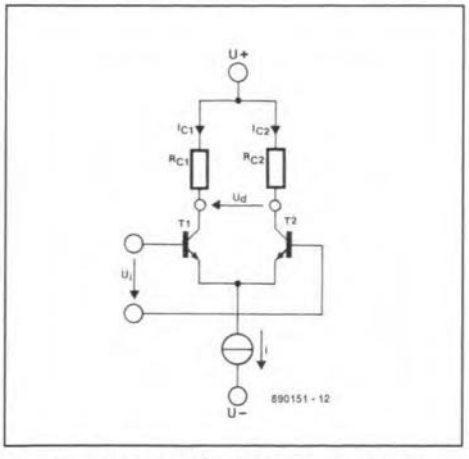


Fig. 2. Standard bipolar opamp input.

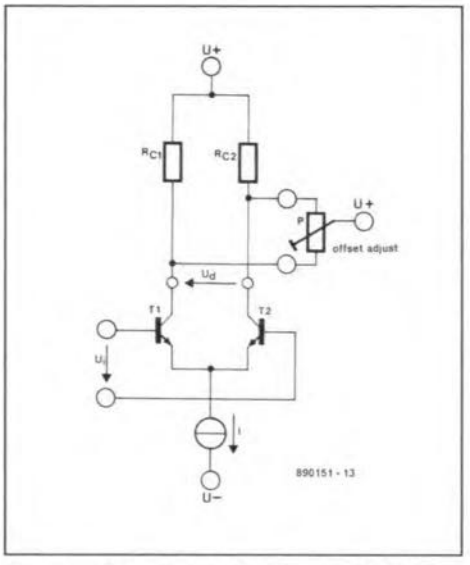


Fig. 3. Opamp input with external offset compensation preset.

This means that the drift specification of the OP07 is roughly 15 times better than that of the 741.

Extracts from the datasheets of the OP07 and the 741 are given in Fig. 1. Clearly, the OP07 has a smaller drift, and the absolute value of the off-set voltage is also lower. Apparently, the drift specification may be improved by keeping the absolute off-set voltage, U_{os}, small.

Zener-zap trimming

This technique is used to reduce U_{os} of the OP07 to a value smaller than 200 µV without the use of external components. The function and operation of zener-zap trimming is best explained by studying the cause of the off-set voltage.

The basic structure of a standard bipolar opamp input circuit is shown in Fig. 2. The output voltage, U_d, is the potential difference between the collectors of T1 and T1:

$$U_d = \Delta [I_{c(T1)}R_{c1} - I_{c(T2)}R_{c2}]$$

If the collector resistors R_c are equal in both branches, $U_d = 0$ if $I_{c(T1)}$ equals $I_{c(T2)}$. Also, assuming that T1 and T2 are perfectly matched, i.e., identical, equal collector currents result in equal threshold voltages $U_{b\text{-}e(T1)}$ and $U_{b\text{-}e(T2)}$. From this it follows that the output voltage, U_d, can only become zero if the input voltage, U_i, equal to

$$U_{b\text{-}e(T1)} - U_{b\text{-}e(T2)}$$

is also zero. In practice, T1 and T2 are never identical, so that the threshold voltages at $I_{c(T1)} = I_{c(T2)}$ are always (slightly) different. Hence, U_i must be made equal to the off-set voltage to achieve $U_d = 0$ V.

In most opamp circuits, the output voltage is made zero by applying the required bias voltage to the input terminals. Some opamps, however, have separate terminals that provide access to internal components. This allows an external trimmer potentiometer to compensate the off-set voltage without the need of a zero-adjust circuit at the sensitive inputs of the opamp. The principle is illustrated in the circuit diagram in Fig. 3.

The designers of the OP07 have gone a little further, however, as shown in Fig. 4: the collector resistor consists of a number of series-connected individual resistors, of which two have a zener diode in parallel. In the production process, the off-set voltage is reduced to the minimum value immediately after the chip is ready. Accurately controlled current pulses are applied to blow ('zap') one or more zener diodes, which then turn into shorting wires.

This automatic 'zener-zap' process allows off-set voltages to be reduced to 50 µV (typical). In some cases, provision is made to compensate even that level with the aid of an external trimmer preset, which is usually included in a resistive bridge circuit. This arrangement is used because the temperature co-efficients of the components in the bridge have a much smaller effect than those in the circuit in Fig. 3.

All these goodies may lead you to start replacing all 741s by OP07s just like that. Remember, however, that the resultant improvement in the circuit performance, if at all required, does not come cheap: the OP07 is about 10 times as expensive as the 741.

Input bias current

At room temperature, bipolar transistors have a much higher input bias current than JFETs (junction FETs), although this current is virtually temperature-independent. The input bias current of BiFET opamps roughly doubles for every ten de-

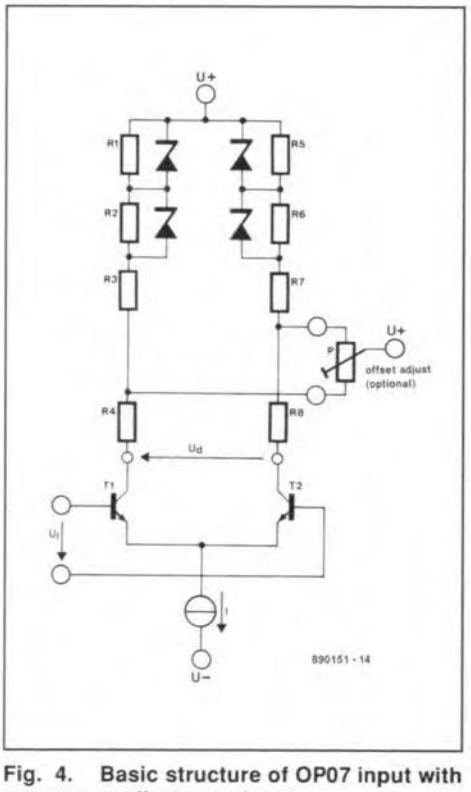
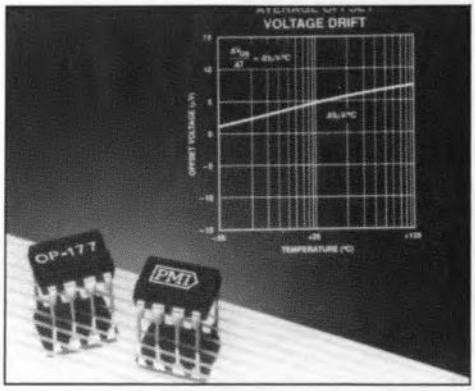


Fig. 4. Basic structure of OP07 input with zener-zap collector resistors.

grees of temperature rise. In general, the input bias current (at normal operating temperatures) of a commonly used BiFET opamp such as the TL074 is often higher than that of a good bipolar type. This should not be taken to mean that BiFET opamps do not have advantages over bipolar types, since they offer much higher slew rate values in many cases. The BiFET Type OP16, for instance, has a slew rate of 25 V/µs, which makes the device about 75 times faster than the OP07 and the 741.

BiMOS opamps such as the Type CA3140 have MOSFET inputs and a bipolar output circuit. Their input bias current is strongly temperature-dependent owing to the presence of integrated input protection diodes.

The use of current mirrors in the OP07 has resulted in a drastic reduction of the input bias current with respect to the 741: designers should allow for about 50 nA for the OP07 compared with 500 nA for the 741.



Opamp selection

Summarizing the above, the choice of an opamp is governed by the type of circuit it is used in. Broadly speaking, there are five application areas for opamps:

- general purpose
- low-power
- micro-power
- high-speed
- high accuracy

Each of these applications requires a particular type of opamp for optimum performance. Each opamp family, in turn, has members that are tailored to give optimum performance in one respect only.

The overview in Table 1 may prove useful as a first guide to opamp selection. The right-hand column gives the best-known types in a particular series.

Application area	Primary characteristics	Opamp type
general-purpose	low-cost	LM741; OP02 (=741 upgrade)
low-power	low supply current (I<1 mA)	TLC271; OP21
micro-power	very low supply current (I<100 µA)	TLC271; OP20
high speed	high gain-bandwidth	LF356; CA3140; OP15; OP16
high accuracy	low input off-set; high DC gain; high CMRR	OP07; OP77; OP27 (low-noise)

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-177A MIN	OP-177A TYP	OP-177A MAX	OP-177B MIN	OP-177B TYP	OP-177B MAX	UNITS
Input Offset Voltage	V_{OS}		–	4	10	–	10	25	µV
Long-Term Input Offset Voltage Stability	ΔV_{OS}/Time	(Note 1)	–	0.2	–	–	0.2	–	µV/Mo
Input Offset Current	I_{OS}		–	0.3	1.0	–	0.3	1.5	nA
Input Bias Current	I_B		–0.2	–	1.5	–0.2	–	2.0	nA
Input Noise Voltage	e_n	f_o = 1Hz to 100Hz (Note 2)	–	118	150	–	118	150	nV_{RMS}
Input Noise Current	i_n	f_o = 1Hz to 100Hz (Note 2)	–	3	8	–	3	8	pA_{RMS}
Input Resistance Differential-Mode	R_{IN}	(Note 3)	26	45	–	26	45	–	MΩ
Input Resistance Common-Mode	R_{INCM}		–	200	–	–	200	–	GΩ
Input Voltage Range	IVR	(Note 4)	±13	±14	–	±13	±14	–	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±13V	130	140	–	130	140	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V	120	125	–	115	125	–	dB
Large-Signal Voltage Gain	A_{VO}	R_L ≥ 2kΩ, V_O = ±10V (Note 5)	5000	12000	–	5000	12000	–	V/mV
Output Voltage Swing	V_O	R_L ≥ 10kΩ R_L ≥ 2kΩ R_L ≥ 1kΩ	±13.5 ±12.5 ±12.0	±14.0 ±13.0 ±12.5	– – –	±13.5 ±12.5 ±12.0	±14.0 ±13.0 ±12.5	– – –	V
Slew Rate	SR	R_L ≥ 2kΩ (Note 2)	0.1	0.3	–	0.1	0.3	–	V/µs
Closed-Loop Bandwidth	BW	A_{VCL} = +1 (Note 2)	0.4	0.6	–	0.4	0.6	–	MHz
Open-Loop Output Resistance	R_O		–	60	–	–	60	–	Ω
Power Consumption	Pd	V_S = ±15V, No Load V_S = ±3V, No Load	–	50 3.5	60 4.5	–	50 3.5	60 4.5	mW
Supply Current	I_{SY}	V_S = ±15V, No Load	–	1.6	2.0	–	1.6	2.0	mA
Offset Adjustment Range		Rp = 20kΩ	–	±3	–	–	±3	–	mV

NOTES:
1. Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically less than 2.0µV.
2. Sample tested.
3. Guaranteed by design.
4. Guaranteed by CMRR test condition.
5. To insure high open-loop gain throughout the ±10V output range, A_{VO} is tested at –10V ≤ V_O ≤ 0V, 0V ≤ V_O ≤ +10V, and –10V ≤ V_O ≤ +10V.

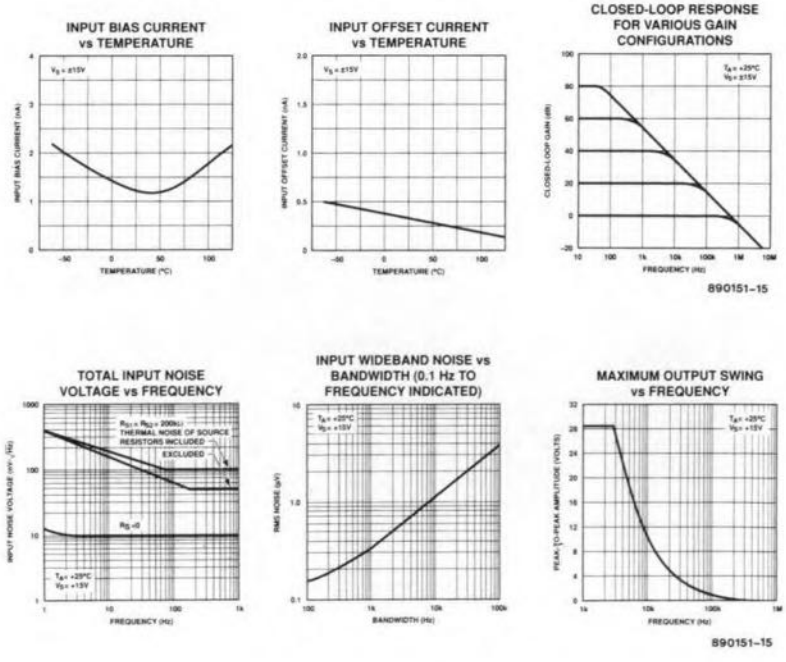


Fig. 5. Introducing the OP177 ultra-precision opamp (*illustrations courtesy Precision Monolithics Inc.*)

Reference:

1. LinCMOS circuits. *Elektor Electronics* July/August 1989, p. 20 ff.

SAVE DECODER

890165-I

Part 1: Operation and technical background

P.N.P. Wintergreen

The scrambling system employed for the BBC-TV Europe and the now defunct Premiere channel on the Intelsat-VF11 TV satellite is generally classified as a low-level video encoding scheme. Based on controlled interference in the video spectrum it is, however, not so simple to defeat with traditional filter designs that have already caused much hair-pulling and teeth-gnashing among technically inclined dish owners. The decoder discussed here leaves traditional filters for what they are, yet offers a perfectly decoded picture at a cost of £25 or so.

The Intelsat-VF11 TV satellite is positioned in geostationary orbit at 27.5° west, and can be received in large parts of western Europe if a dish of 1.2 m or larger is used. The BBC-TV Europe programme is transmitted at 10.987 GHz with vertical polarization. The channel is encoded according to the SAVE (*sound and vision encryption*) system, with occasional changes in the interference frequency used.

Tackling SAVE

The SAVE scrambling system looks relatively simple at first glance, because the encoding is effected entirely in the frequency domain. This is in contrast to many other analogue encoding systems, which use signal inversion in combination with amplitude-shifting and frame and/or line polarity control (Ref. 1).

In the SAVE system, the video signal from the TV studio has its amplitude reduced by 50% before it is inverted. The original amplitude is then restored by the addition of a pure sine-wave with a frequency of about 94 kHz. This encoding scheme has prompted many technically inclined dish owners to design and build a wide variety of filters, only to find that the interfering signal is much harder to get rid of than expected. This is mainly because any residual interfering signal, however small, gives an irritating effect on the TV screen. As found out the hard way, the 94 kHz notch is simply not capable of ensuring a perfectly stable picture.

Without a suitable decoder, a SAVE-encoded video signal produces a totally unintelligible picture. In principle, the signal becomes at least visible by inverting it and doubling the amplitude. Although these measures result in a picture that can be recognized on many TV sets, the quality is very poor owing to the interfering carrier that is still present at its full level. The suppression, in particular, of the interference poses considerable problems if conventional filter techniques are used.

The phase and amplitude recovery of the 94 kHz interference signal is affected by the video signal, and designers must take into account that this can have an infinite number of instantaneous amplitude-frequency configurations because the spectrum is a function of the current picture content, which changes in real-time.

A narrow 94 kHz filter, however, will give reasonable results in many cases. A crystal filter as used in communications receivers is ideal for this function. Unfortunately, crystal filters are notoriously expensive and hard to obtain, especially for a non-standard frequency like 94 kHz. These problems may be resolved, however, by a compensation circuit with a PLL (*phase-locked loop*), and a VXO (*variable crystal oscillator*) that functions as a VCO (*voltage controlled oscillator*). An advantage of this arrangement is that it can be designed to operate at a multiple of 94 kHz.

The block diagram of Fig. 1 shows the basic structure of a VXO-PLL (Ref. 2). Although not used for the present design, the principle merits a short discussion. The crystal is cut to order for one particular interference frequency around 94 kHz. In practice, however, the interference frequency is changed on an irregular basis, so that a number of crystals are required when BBC-TV Europe is to be decoded. Clearly, this is a relatively expensive solution since the station operators can change the interference frequency within a certain range, requiring new crystals to be cut. The present decoder is much more

SAVE DECODER

- low-cost design; no cut-to-order quartz crystal(s)
- complete suppression of SAVE interference
- L-C oscillator with amplitude and phase control loops for optimum stability
- simple-to-connect to any indoor unit
- standard clamped video output: 1 V_{pp}/75 Ω
- automatic switch-over between non-encoded and SAVE-encoded channels
- automatic search for interference frequency within 1.5 kHz band

flexible in respect of frequency control because it is based on an *L-C* oscillator that uses inexpensive components, and works at 94 kHz. A number of special techniques, combined with 'all-analogue' signal processing have resulted in a stop-band filter (*notch*) whose performance in respect of selectivity comes close to that of a crystal filter.

The low-cost decoder presented here features automatic processing of any SAVE-encoded video signal that contains an interfering carrier between about 93 kHz and 94.5 kHz, so that BBC-TV Europe (f_i=93,275 Hz) is reliably recognized and decoded, irrespective of the current interference frequency.

Spectral analysis

The frequency spectra of Fig. 2 illustrate the basic operation of *pre-* and *de-emphasis* techniques used in the present decoder. The spectrum of Fig. 2a shows the typical amplitude distribution, within the frequency range from 0 to 500 kHz, of a video signal. It should be noted that the drawing is purposely simplified: the spectrum applies to a completely black picture, while the effect of the raster synchronization pulses is not shown. The simplified spectrum with line sync components and the interference signal is, however, still useful for a basic analysis.

The frequency range between 90 and 95 kHz is shown enlarged in the lower spectrum of Fig. 2a. Clearly, the interference carriers are quite close to the sixth harmonic of the line frequency. The frequency differences are small — only 475 Hz in the case of BBC-TV Europe, and 575 Hz in the case of Premiere — and make selective suppression of the interference frequency fairly difficult because the phase and amplitude of the sixth harmonic of the line sync must be left completely unaffected. If this condition is not met, the picture is visibly distorted. Hence, a simple notch is unsuitable for building a reliable SAVE-decoder.

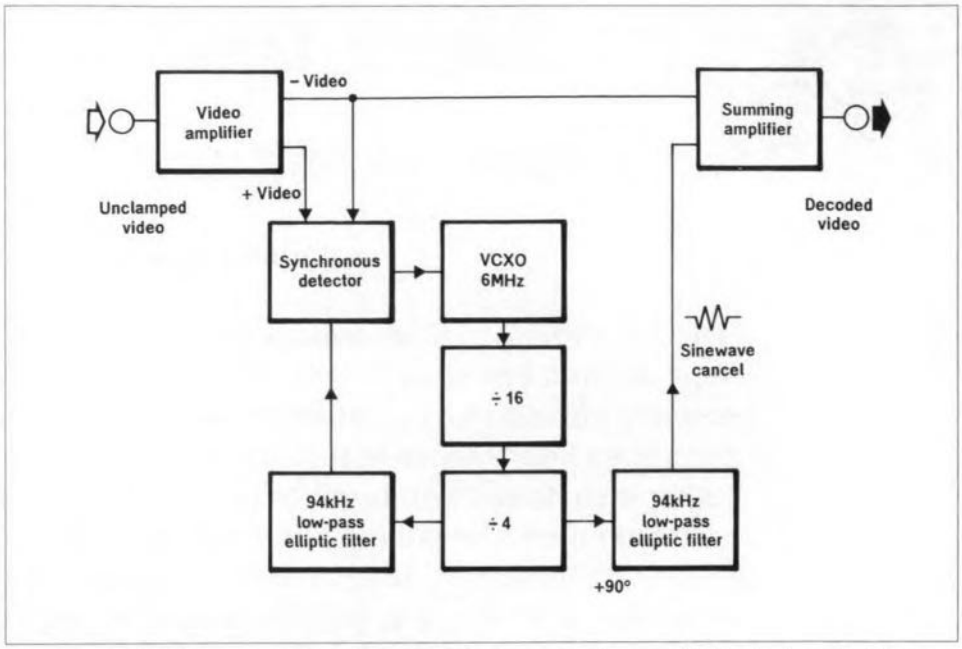


Fig. 1. The first approach to a SAVE decoder is nearly always a VCXO design. The inherent disadvantages are, however, relatively high cost and the 'one channel, one crystal' rule (source: Ref. 2).

For those less familiar with video techniques, it may come as a surprise that the interference signal must be amplified before it can be suppressed. Pre- en de-emphasis are used to achieve this. These techniques are applied in FM communications systems to improve the signal-to-noise ratio. At the transmitter side, a certain part of the frequency spectrum of the modulation signal is given a greater amplitude, which is reduced again in the receiver by a matched filter to restore the original signal level. Ideally, the frequency response between the input of the transmitter and the output of the receiver is flat because the pre- and de-emphasis filters are closely matched by means of complementary curves.

A two-section *L-C* filter in the present

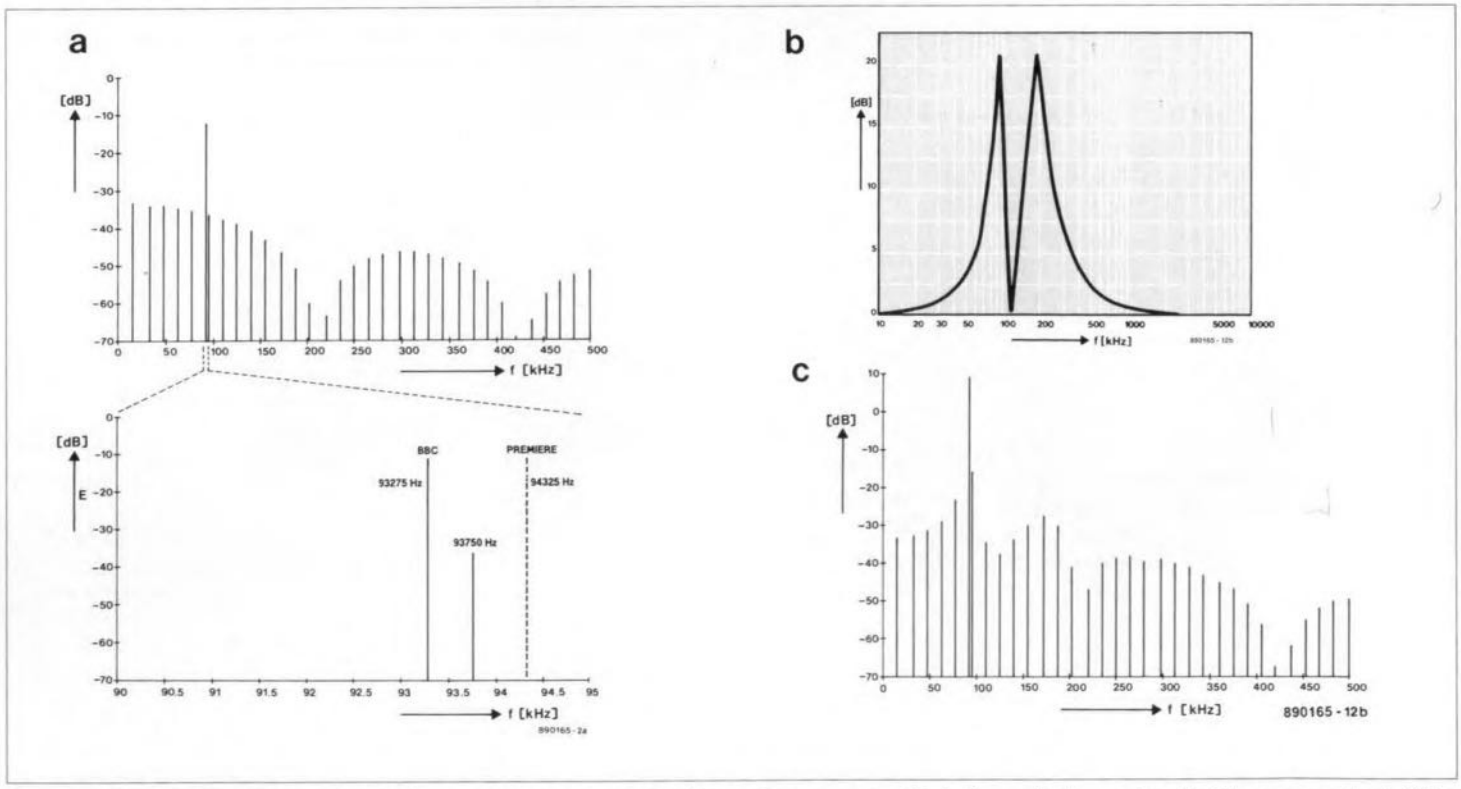


Fig. 2. Frequency spectrum of a SAVE-encoded video signal with no picture content (2a); theoretical pass-band of the pre-emphasis filter (2b); and the result of the pre-emphasis operation on the original spectrum (2c). It should be noted that the spectra shown are theoretical and purposely simplified.

SAVE decoder raises frequency components around 94 kHz and 188 kHz about 20 dB with respect to the rest of the video spectrum. The theoretical pass-band curve of this filter is shown in Fig. 2b, and its effect on the spectrum of Fig. 2a is apparent from Fig. 2c. The interference signal has the highest amplitude in the latter spectrum.

The control principle adopted for the SAVE decoder requires the second pass-band at 188 kHz. The analogue control circuit that is to supply the regenerated 94 kHz signal does not have filters to ensure a well-defined phase response, and multiplication of the 94 kHz signal inevitably produces a 188 kHz component. Owing to cross-talk, a part of this component ends up in the video signal, where it produces interference. This is prevented, however, with the aid of a de-emphasis filter, of which one section is tuned to 188 kHz.

Since the interference frequency is always an odd multiple of the interlace frequency (25 Hz), residual levels of the 94 kHz signal that remain after decoding are virtually unnoticed owing to the optical averaging function of the human eye.

After removal of the 94 kHz component, the signal amplitude must be restored to the level before pre-emphasis. This is achieved with a de-emphasis filter whose pass-band curve is accurately dimensioned to form the inverse of the pre-emphasis curve.

Block diagram

The basic operation of the SAVE decoder is best described along the lines of the block diagram shown in Fig. 3.

The heart of the circuit is formed by an *L-C* oscillator, which is controlled by loop circuits for amplitude and phase. In principle, the regenerated 94 kHz sine-wave is added to the scrambled video signal. The amplitude of the regenerated sine-wave is identical to that of the interference component, but the phase is opposite. This is achieved with the aid of a control circuit that is capable of continuously monitoring, and, if necessary, correcting, the phase and the amplitude of the regenerated 94 kHz signal. The oscillator used is a voltage-controlled Colpitts type based on an *L-C* tuned circuit with a relatively high Q-factor. In combination with a double loop filter that forms part of a PLL, it ensures good phase stability of the regenerated sine-wave when the circuit is locked.

The block diagram shows that the unclamped video signal supplied by the satellite-TV receiver is amplified before it is passed through the pre-emphasis filter discussed above. The output signal of the two-stage *L-C* filter is compared to that of the 94 kHz oscillator. The phase comparator is an analogue multiplier available in IC Type XR2208 from Exar. The result of the multiplication operation is a difference frequency that is fed to the first loop filter. This filter is realized with the opamp available in the XR2208. When the circuit is not locked, the first loop filter is given a bandwidth of a few hundred Hz to enable the PLL to lock on to sufficiently strong signals in a frequency band of about 1.5 kHz around 94 kHz. The PLL does not lock on to signals below a certain threshold level, so that, for instance, the sixth harmonic of the line frequency can not switch the circuit to the decoding mode. Without special measures, however, the sixth harmonic of the line frequency is likely to cause problems once the PLL has locked on to, say, the SAVE-encoded BBC-TV Europe signal. In that condition, the phase comparator supplies 475 Hz, the frequency difference between the sixth harmonic and the interference signal. Without a correctly dimensioned loop filter, this difference frequency gives rise to phase modulation of the VCO, which, in turn, leads to incomplete compensation of the interference. The result is an annoying interference on the TV screen.

The solution to this problem has been found in automatic bandwidth reduction of the loop filter. After the PLL has locked, the loop filter is given a pass-band of about 15 Hz rather than a few hundred Hz. This arrangement requires high VCO stability, however, since frequency deviations can only be corrected relatively slowly. Fortunately, the *L-C* oscillator used meets this requirement, so that a phase-locked reference signal is obtained. What remains is control of the amplitude, and a shift of phase by 90°. Both functions are realized by an operational transconductance amplifier (OTA), a Type LM13700 from National Semiconductor. A useful background on OTAs can be found in Ref. 3.

The VCO reference signal is passed through an amplitude control circuit and an integrator before it is added to the input signal after pre-emphasis. The result of the addition is phase-shifted by 90° and fed to a multiplier that determines the frequency difference between its input signals. Evidently, the difference is 0 Hz only when the VCO frequency equals the interference frequency. As shown in the 'Theoretical background' inset, complete compensation is achieved when the amplitude of the 94 kHz VCO signal equals

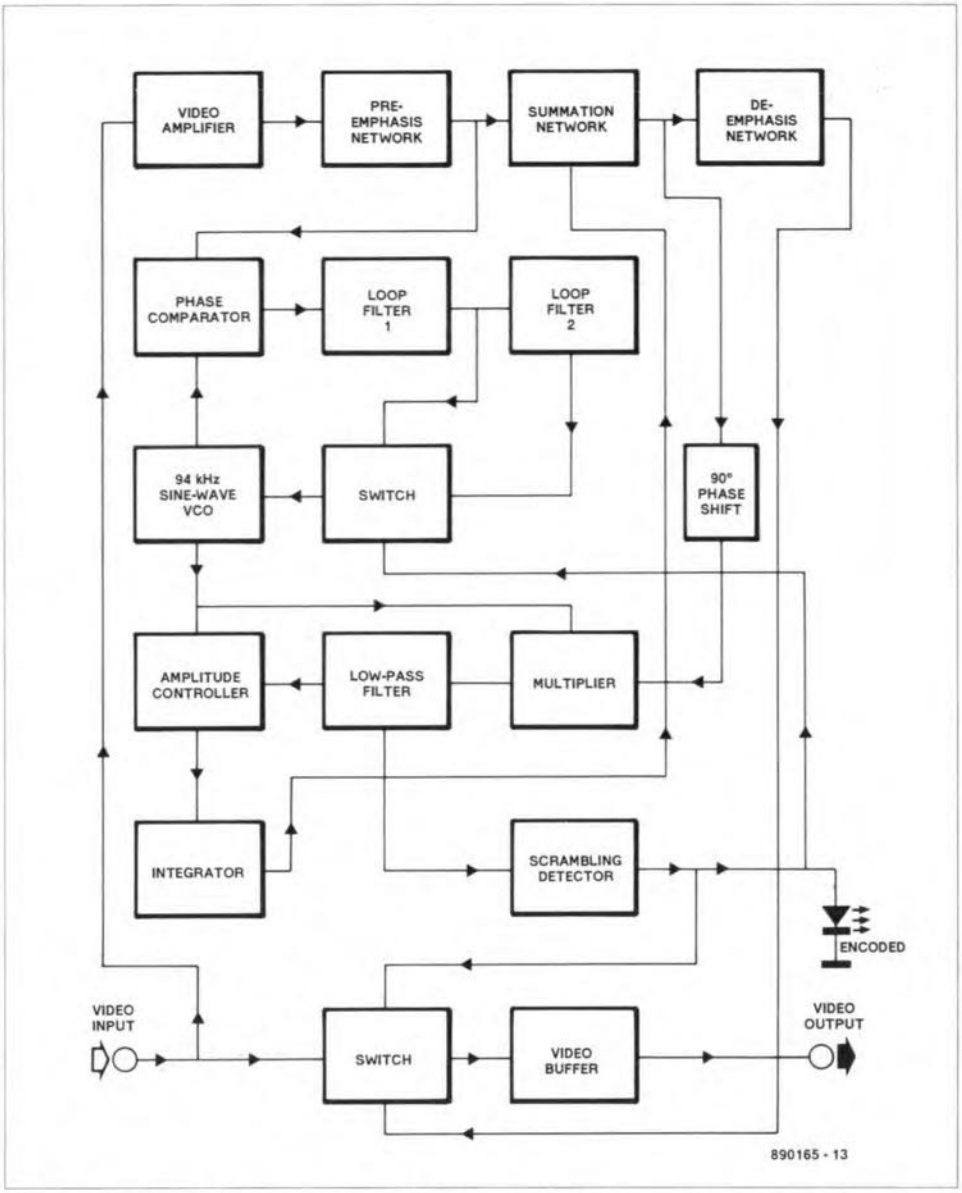


Fig. 3. The block diagram of the SAVE decoder is fairly complex. The operation of the circuit is based on a 94 kHz *L-C* VCO surrounded by control loops for amplitude and phase.

the amplitude of the interference signal. The control loop performs automatic corrections to the amplitude of the VCO signal until a stable condition is reached. Once aligned, the decoder is, therefore, insensitive to small amplitude variations of the input signal, and other forms of instability.

The integrator that shifts the phase of the VCO signal by 90° gives a frequency-independent phase shift, and is located after the amplitude control circuit. An additional benefit of the integrator is its ability to suppress harmonics generated by light distortion. These harmonics are suppressed at 6 dB per octave.

The control voltage for the amplitude controller is used to light a LED that indicates the decoding of a SAVE signal. When the LED lights, the loop filter is automatically switched to reduced bandwidth, and the output signal of the de-emphasis network is fed to the video buffer with associated clamping circuit. The decoded video signal has an amplitude of about 1 V_{pp} at a load impedance of 75 Ω, and is suitable for direct connection to a monitor or remodulator.

From theory to practice

The previously discussed functions are easily found back in the circuit diagram of Fig. 4. The unclamped video signal from the satellite-TV receiver must have an amplitude of at least 0.5 V_{pp}. Components P_1, C_1, R_3 and ES_1 take the non-encoded video signal to amplifier T_5. From there, it is passed through clamping circuit D_1-D_2-T_6 before it is applied to output buffer T_7. The output amplitude is set to 1 V_{pp} into 75 Ω with the aid of preset P_1.

The pre-emphasis *L-C* filter in the collector line of T_1 supplies a video signal with a 94 kHz component of about 3 V_{pp} when the receiver is tuned to a SAVE-encoded TV channel. The transistor works as an inverting amplifier. Capacitor C_7 feeds the signal with the 94 kHz component to the phase comparator in IC_3, where it is multiplied with the VCO signal applied via C_{18}.

Phase control

The 94 kHz Colpitts VCO built around FET T_8 is tuned by means of a direct voltage applied to dual variable capacitance diode D_7. The circuit around D_6 and T_9 is an amplitude stabilizer. When the amplitude of the oscillator signal exceeds a certain level, T_9 conducts via D_6, and draws current through R_{44}. This causes the drain current of the oscillator FET to drop to a level at which the feedback gain in the

Theoretical background

1. Pre- and de-emphasis

Current source T_1 uses pre-emphasis impedance *Z* formed by L_1-L_2-C_4-C_5-R_6 to generate a signal voltage at TP1:

$$U_{B(T1)} = U_i$$
$$U_{E(T1)} \equiv U_i$$

$$I_{C(T1)} \equiv -I_{E(T1)} = -U_i / R5$$

$$U_{TP1} = I_{C(T1)} (Z + R7) = -U_i (Z+R7) / R5$$

Since T_3 offers high current amplification, *Z* is hardly loaded.

The regenerated 94 kHz sine-wave is added in anti-phase to the video signal. Emitter follower T_4 forms a virtually ideal voltage source for the de-emphasis impedance, *Z*:

$$U_{B(T4)} = U_{E(T4)} = -U_i (Z + R7) / R5 + u_p \sin (\omega t + \varphi)$$

where
$\omega = 2 \pi 94000$ [*rad/s*]

The decoded video signal across R_{15} may be written as

$$U_{R15} = U_o$$
$$U_o = R15 / (R15 + Z) U_{E(T4)}$$

$$U_o = \frac{R15}{(R15 + Z)} [-U_i \frac{(Z + R7)}{R5} + u_p \sin (\omega t + \varphi)]$$

The input voltage, U_i, may be written as

$$U_i = U_{video} + u_p \sin (\omega t + \varphi).$$

Owing to noise in the input signal, the residual 94 kHz component, U_{res}, has to be taken into account:

$$U_o = R15 / (R15 + Z) (-U_{video} (Z + R7) / R5 + U_{res})$$

$$U_o = -U_{video} \frac{R15 (Z + R7)}{R5 (Z + R15)} + \frac{R15}{Z + R15} U_{res}$$

With $R_7 = R_{15}$:

$$U_o = -R15 / R5 \; U_{video} + R15 / (Z + R15) U_{res}$$

$$U_o = -1.23 \; U_{video} + R15 / (Z + R15) U_{res}$$

When pre-emphasis network L_4-C_9 (*Z*) resonates at 94 kHz, it forms a very high impedance. R_{13} alone then determines the impedance of *Z*. With $R_{13} = 2700\Omega$:

$$U_o = -1.23 \; U_{video} + 0.09 \; U_{res}$$

Correctly aligned, the pre- and de-emphasis networks yield more than 20 dB suppression of the 94 kHz component, without distorting the video signal.

2. Amplitude control circuit

The frequency of the amplitude control voltage, U_{reg}, is 0 Hz if the regenerated frequency equals the frequency of the interference voltage, U_i:

$$U_{reg} = \int_0^{\infty} \sin(\omega t) [(U_i - U_{reg}) \sin (\omega t)] \, dt$$

$$U_{reg} = \int_0^{\infty} 0.5 (U_i - U_{reg}) [1 - \cos (2 \omega t)] \, dt$$

The integrator gives virtually complete suppression of the 188 kHz component, so that:

$$U_{reg} = \int_0^{\infty} 0.5 (U_i - U_{reg}) \, dt$$

This equation can be solved if $U_i = U_{reg}$, which corresponds to complete compensation.

3. 90° phase shifter

Pin 5 of OTA1 supplies a sinusoidal current, I_o, which is integrated by C_{29}:

$$I_o = i_p \cos (\omega t)$$

$$U_{C29} = 1 / C \int_0^{\infty} I_0 \, dt$$

$$U_{C29} = 1 / C \int_0^{\infty} i_p \cos (\omega t) \, dt$$

$$U_{C29} = \frac{i_p}{\omega C} \sin (\omega t)$$

where
$\omega = 2 \pi 94000$ [*rad/s*]

The phase is shifted 90° independently of frequency.

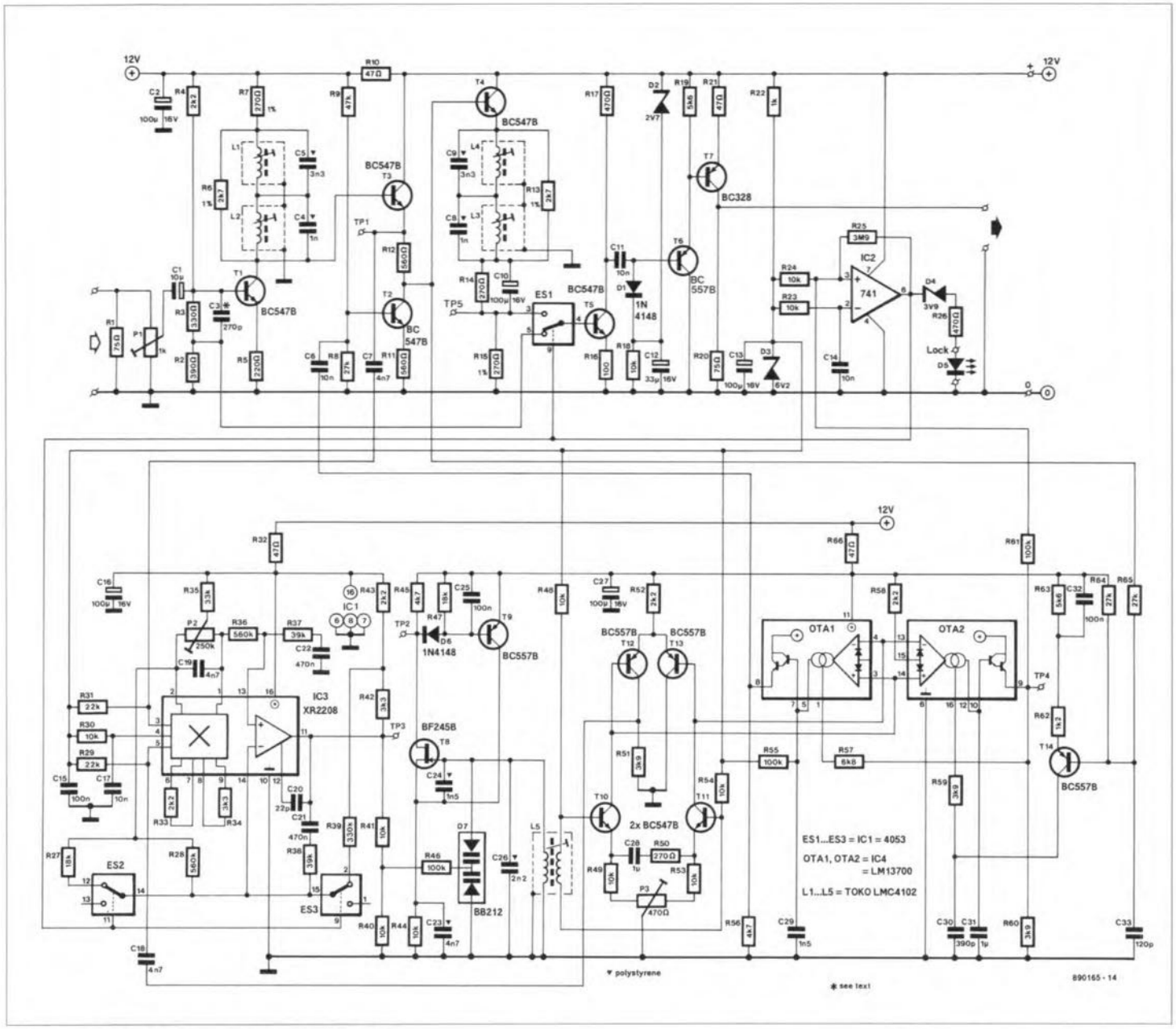


Fig. 4. Circuit diagram of the SAVE decoder.

oscillator is unity. The result is a clean and stable oscillator signal that is coupled out inductively via L_5. Transistors T_{10} and T_{11} amplify the oscillator signal and convert it into a symmetrical current that is fed to the pair of diodes at each of the parallel-connected OTA inputs (IC_4).

The OTA inputs are also connected to T_{12} and T_{13} to form a *gain-cell*. In principle, a gain-cell provides linear conversion of an input signal into an output signal. The gain of the cell is determined by a current supplied by an external source. In the present case, this control current emanates from R_{52}, while the basic gain of the cell is defined by the ratio R_{52}:R_{58}.

The 94 kHz signal is taken asymmetrically from the collector of T_{12} and fed to the phase comparator via C_{18}. The difference frequency is available as a balanced signal between pins 1 and 2 of the XR2208. The balanced difference signal is passed to the opamp in the XR2208, by means of networks R_{28}-R_{38}-C_{21} and R_{36}-R_{37}-C_{22}.

Depending on whether the PLL is locked or not, the bandwidth of the loop filter is changed by ES_2 connecting R_{27} in parallel with R_{28}, and ES_3 selecting a different R-C network at the output of the opamp in the XR2208. The control voltage is passed to the varicap via R_{41} and R_{46}. This closes the phase-locked loop.

Amplitude control

The amplitude of the regenerated 94 kHz sine-wave is determined with the aid of a current sent into pin 1 of OTA_1. This current is supplied by OTA_2, which works as a multiplier. The result is that pin 5 of OTA_1 supplies a sinusoidal current to integrator C_{29}. The mathematical deduction in the 'Theoretical background' inset demonstrates that the phase is shifted 90° independently of frequency. The voltage developed across C_{29} is fed back into the IC via pin 7, and reappears buffered at pin 8. The regenerated, amplitude-controlled and 90° phase-shifted 94 kHz signal is fed to T_2 via C_6, and from there to summation point T_2-R_{12}. This forms the nucleus of the circuit: the interference disappears against its regenerated counterpart, which has the same amplitude but the opposite phase.

The summation signal is taken through the de-emphasis network in the emitter line of T_4. The first of the two *L-C* sections removes residual 94 kHz levels, and the second ensures sufficient suppression of the 188 kHz component. The decoded signal is fed to the clamping circuit via ES_1.

The amplitude control circuit receives its error signal from the summation point, via R_{65}. Components C_{33}, R_{64}, R_{65}, C_{30} and R_{59} shift the phase of the error signal by 90° so that it can be used for driving multiplier OTA_2. This supplies a current that is integrated by C_{31}. The resulting voltage on this capacitor is buffered by the darlington transistor in the OTA, and serves to supply the control current to the previously mentioned gain cell (OTA_1) via R_{57}. This closes the amplitude-controlled loop.

The construction and alignment of the decoder will be described in Part 2 of this article.

CONTENTS

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We regret that owing to legal restrictions we can not publish "SAVE decoder – Part 2" as planned. At the same time, supply and design difficulties have made it necessary to postpone "Sinewave inverter"; no new date can as yet be given for its publication.

DESIGN IDEAS

The contents of this column are based solely on information supplied by the author and do not imply practical experience by *Elektor Electronics.*

WAVEFORM MODULATION OF THE MAINS VOLTAGE

by A.M. Karailiev

In order to simplify the transmitter and to improve the noise immunity of the remote control receivers described in his earlier article*, Mr Karailiev here offers another method of modulating and demodulating the mains voltage.

A thyristor, rated at not less than 25 A, is connected directly across the mains supply. It is controlled by a circuit as in Fig. 1 in a manner to make it conductive for a time Δt µs at the end of every positive half cycle of the mains voltage.

The programming unit is an integrated circuit Plessey Type SL120, or SGS Type L120, or equivalent.

Assume that the thyristor will short-circuit the mains at the instant this reaches a value of +24 V – see diagram in Fig. 2. Then,

$$u = U_{max} \sin \omega t = U_{max} \sin(2\pi t/T)$$

or

$$24 = 310 \times \sin 2\pi \times 50 \Delta t.$$

Since, for a small angle, $\sin\theta = \theta$,

$$24 = 310 \times 2\pi \times 50 \Delta t, \text{ and}$$

$$\Delta t = (24 \times 10^6) / 310 \times 2 \times 50 = 246 \text{ µs}.$$

Thus, for a period of 246 µs, the mains voltage is practically zero and this manifests itself, at minimal power dissipation, in a distortion signal on the mains voltage. It is interesting to note that since the signal is caused by a lack of voltage, it will not be attenuated by the power lines, so that it will be detectable over fairly large distances.

Type of modulation

The effect of the momentary short circuit of the mains voltage will be a change of its sinusoidal waveform, so that we may speak of waveform modulation. However, as the depth of modulation is defined by the angle θ during which the short circuit occurs, or by the time duration of the short circuit, other definitions of the type of modulation may be applied.

Readers are advised that modulating the mains voltage in the United Kingdom is subject to the provisions of British Standard BS6839. Further information on the subject may be obtained from BIMSA (BEAMA Interactive and Mains Systems Association), Leicester House, 8 Leicester Street, LONDON WC2H 7BN, Telephone 01-437 0678.

Demodulation

The information on the mains voltage is extracted from it by means of a circuit as shown in Fig. 6. The instantaneous voltage, u, at the secondary of the input transformer, Tr, is

$$u = U_{max} \sin(2\pi t/T)(T \pm t)$$

and this is represented graphically in Fig. 3.

If the full-wave rectified voltage (U_{max}= 17 V) is applied to the inverting input of an operational amplifier acting as a zero crossing detector, and a direct voltage of 0.25 V is applied to the non-inverting input, the output of the detector will consist of 93.66 µs wide pulses at a pulse rate equal to twice the mains frequency.

When the positive voltage applied to the non-inverting input is higher then the voltage caused by the modulation, the pulse spacing (pulse repetition period) decreases. When, however, the voltage caused by the modulation is higher than that applied to the non-inverting input, the pulse spacing increases – see Fig. 4.

In the absence of modulation, the zero crossing detector should be adjusted to make the width of the output pulses as

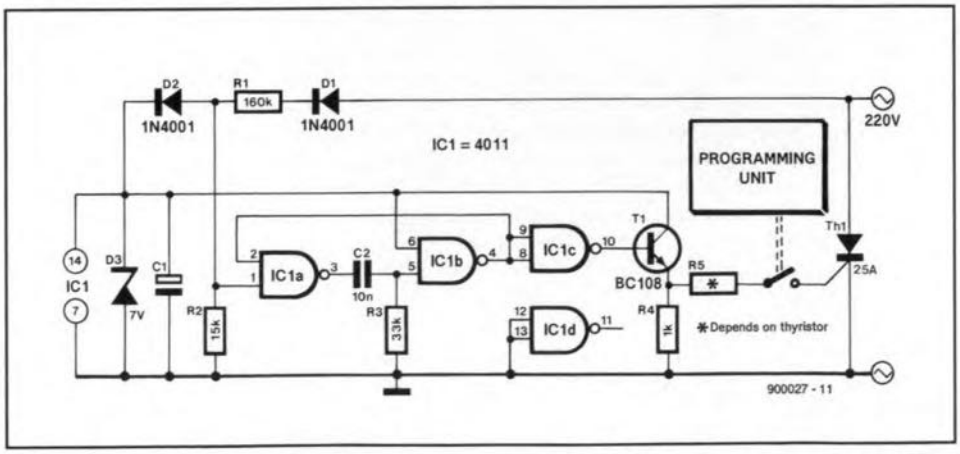


Fig. 1. Basic control circuit for the modulator; the value of R5 depends on the type of thyristor.

* "Mains Signalling", *Elektor Electronics*, November 1988, p. 27.

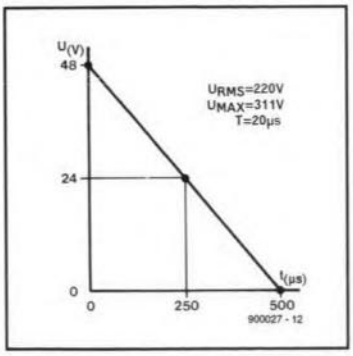


Fig. 2.

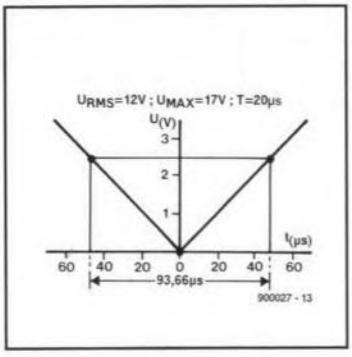


Fig. 3.

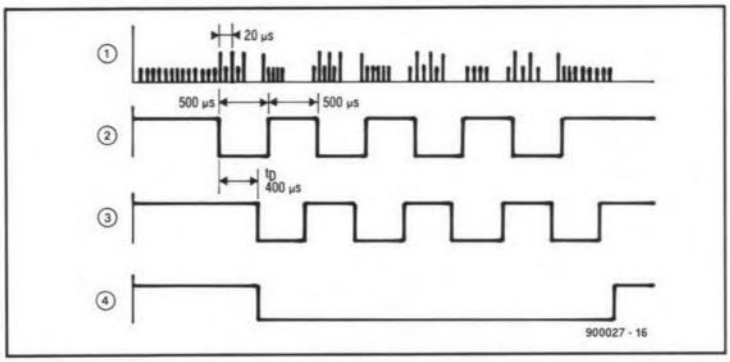


Fig. 5. Pulse diagrams at selected points in the circuit of Fig. 6. The numbers at the left correspond with the circled numbers in Fig. 6.

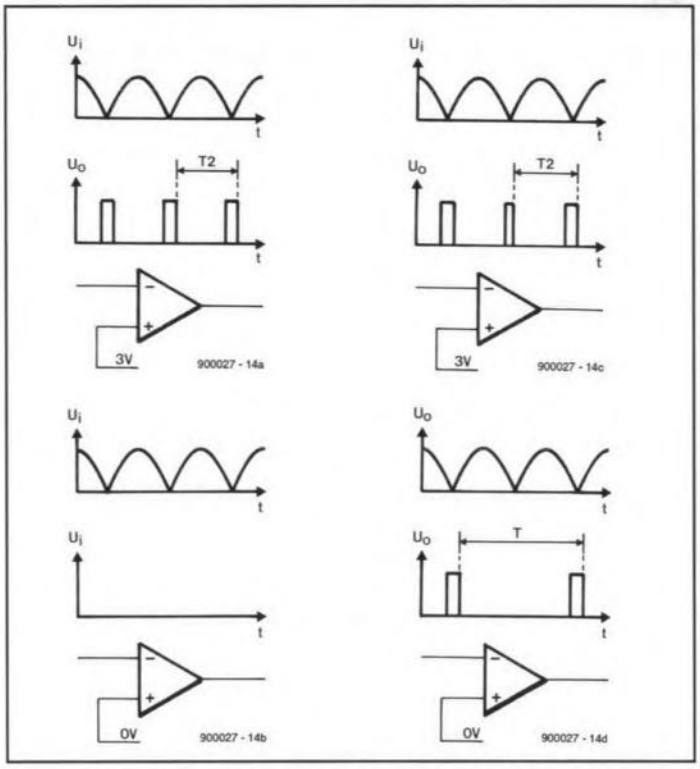


Fig. 4. In diagrams a and b there is no modulation; in diagrams c and d, modulation is present.

small as possible. For example, if the detector produces pulses 100 µs wide in the absence of modulation, and a modulated signal with a depth of modulation of 250 µs is applied, the width of the output pulses will increase to 300 µs. If the detector is made more sophisticated, it may produce pulses only when there is modulation present and no pulses at all in the absence of modulation.

Receiver

In the circuit of the receiver shown in Fig. 6, T1 serves as the zero crossing detector. It should preferably be a germanium type to ensure minimum-width pulses in the absence of modulation.

Network R3-R4-C3 forms a charge/discharge circuit that converts the pulse-width modulation into pulse-amplitude modulation. The pulse height can be adjusted by R3, so that monostable IC1 may be triggered only by pulses above a certain height.

The monostable is retriggerable and produces a long output pulse at its pin 12 when there is modulation present. Here, the length of the pulses is predetermined at 500 µs. Shorter pulses will be suppressed by a noise protection circuit consisting of R6-R7-C6 and the two Schmitt triggers contained in IC3.

The output pulses of IC1 are counted by IC4. When the pulse train ceases, retriggerable monostable IC2 emits a pulse that is applied to the clock input of D-type bistable IC5. This causes the contents of one stage of the counter to be transferred to IC5, which acts as a latch. Since IC4 is a four-stage counter, it is thus possible to control four different devices or machines.

Diagrams of the pulses at selected parts of the circuit are shown in Fig. 5.

The higher noise immunity of the receiver as compared with that in my earlier article is obtained because:

1. its input is open to the signal and closed to noise, since the thyristor short-circuits all noise;
2. of the noise protection circuit;
3. of the special form of the signal (absence of voltage). ■

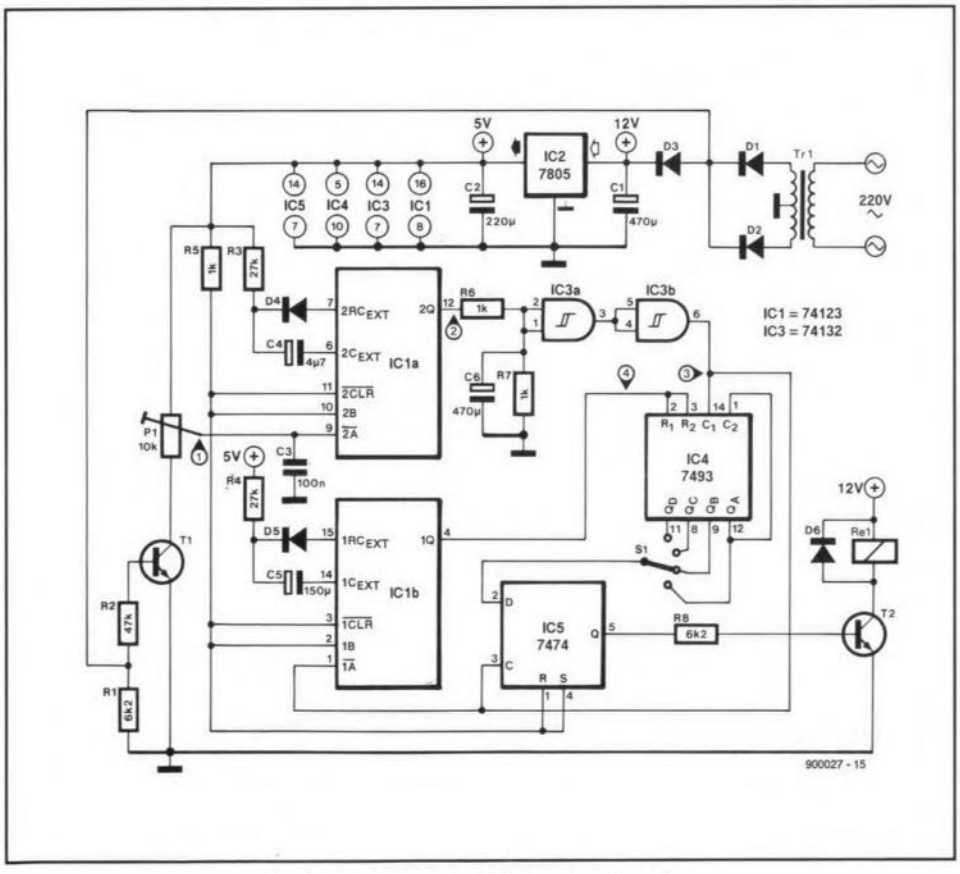
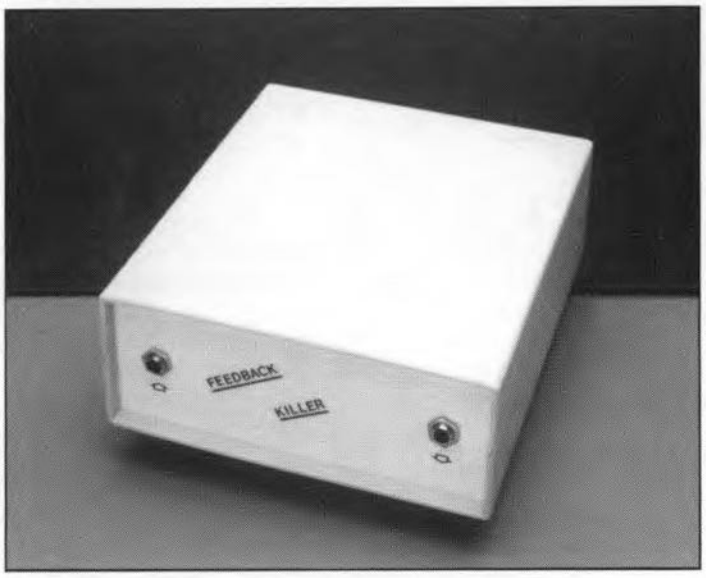


Fig. 6. Circuit diagram of the proposed receiver.

FEEDBACK KILLER

T. Giffard

This circuit helps to prevent feedback in public address (PA) systems. Feedback occurs at relatively high volume settings when a microphone is held too close to a loudspeaker. The effect is characterized by whistling or howling sounds that are annoying to the audience, the sound engineer and, of course, the speaker on the stage.



Feedback is a constant source of worry to mixing desk operators in the backstage line, since the now shrill then howling sounds always seem to occur unexpectedly, and tend to irritate both the performers on the stage and the audience, who respond with boos, catcalls and plugging of ears. No good this equipment!

At a certain frequency, or frequencies, the phase shift in the closed loop formed by the microphone, the amplifier, the loudspeaker and the listening room is 0 degrees, 360 degrees or a multiple thereof. If, in this situation, the amplifier gain is greater than the room attenuation, the feedback signal rises to a level at which it tops all other sound. This is the well-known high-pitch whistle: the PA system oscillates.

Figure 1 illustrates what happens. The sound produced by the loudspeakers is reflected by the room or by objects or persons in the room, and is subsequently picked up by the microphone. The phase shift and attenuation depend on the acoustic parameters of the listening room (note that the audience forms a moving part of the room and must be taken into account as regards the loudspeaker positions).

Evidently, the best way to prevent feedback is to place the microphones in positions where they are unlikely to pick up reflections from the loudspeakers. Sound technicians know a lot about microphone placement and often spend hours on small adjustments of the monitor loudspeakers. However, many artists are inclined to take the microphone from its stand the moment they are on stage. This requires great attention on part of the sound technician, since there remains a large risk of feedback occurring.

The circuit described here raises the sound level at which the feedback starts by a few decibels. This should not be taken to mean that it makes feedback impossible: only the point at which the effect starts is shifted to a much higher level.

The risk of feedback occurring is reduced by creating a small frequency difference of 1 Hz to 30 Hz between the amplifier input- and output-signal. This operation causes the frequency of a (potential) feedback signal to be raised a little so that the condition for oscillation is no longer satisfied.

Block diagram

A number of modulation techniques may be applied to obtain a fixed frequency shift between an amplifier input- and output-signal. In practice, virtually all these techniques make use of amplifiers, filters and mixers.

The block diagram of the feedback killer is shown in Fig. 2. The principle of operation is fairly simple. The input signal is passed through two all-pass filters whose output signals have a phase difference of 90°. These signals are multiplied with two clock signals that are also 90° out of phase. The resulting signals are added. As shown by equation (A) in Fig. 2, the multiplication and addition operations produce a new signal of a fre-

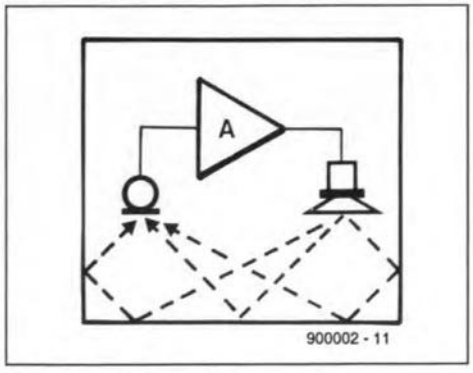


Fig. 1. Sound reflections.

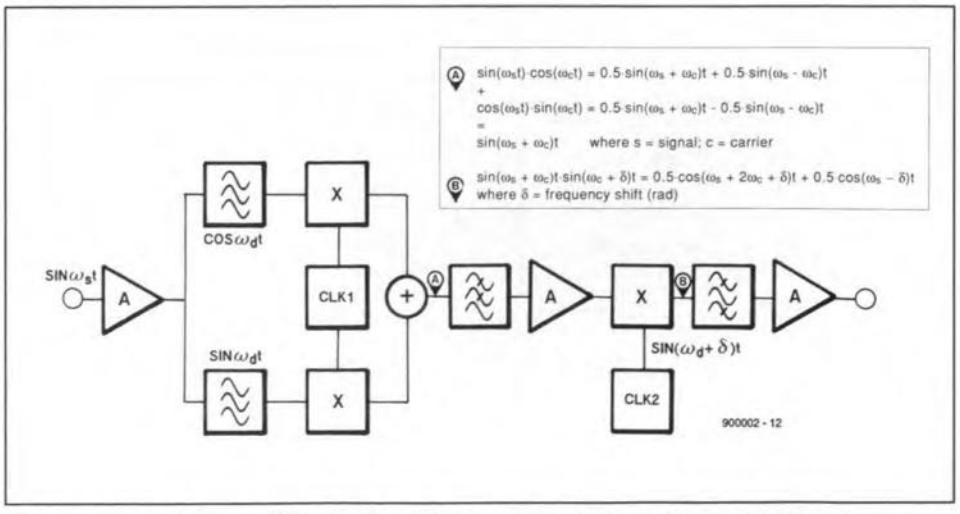


Fig. 2. Block diagram of the feedback killer, and its mathematical background.

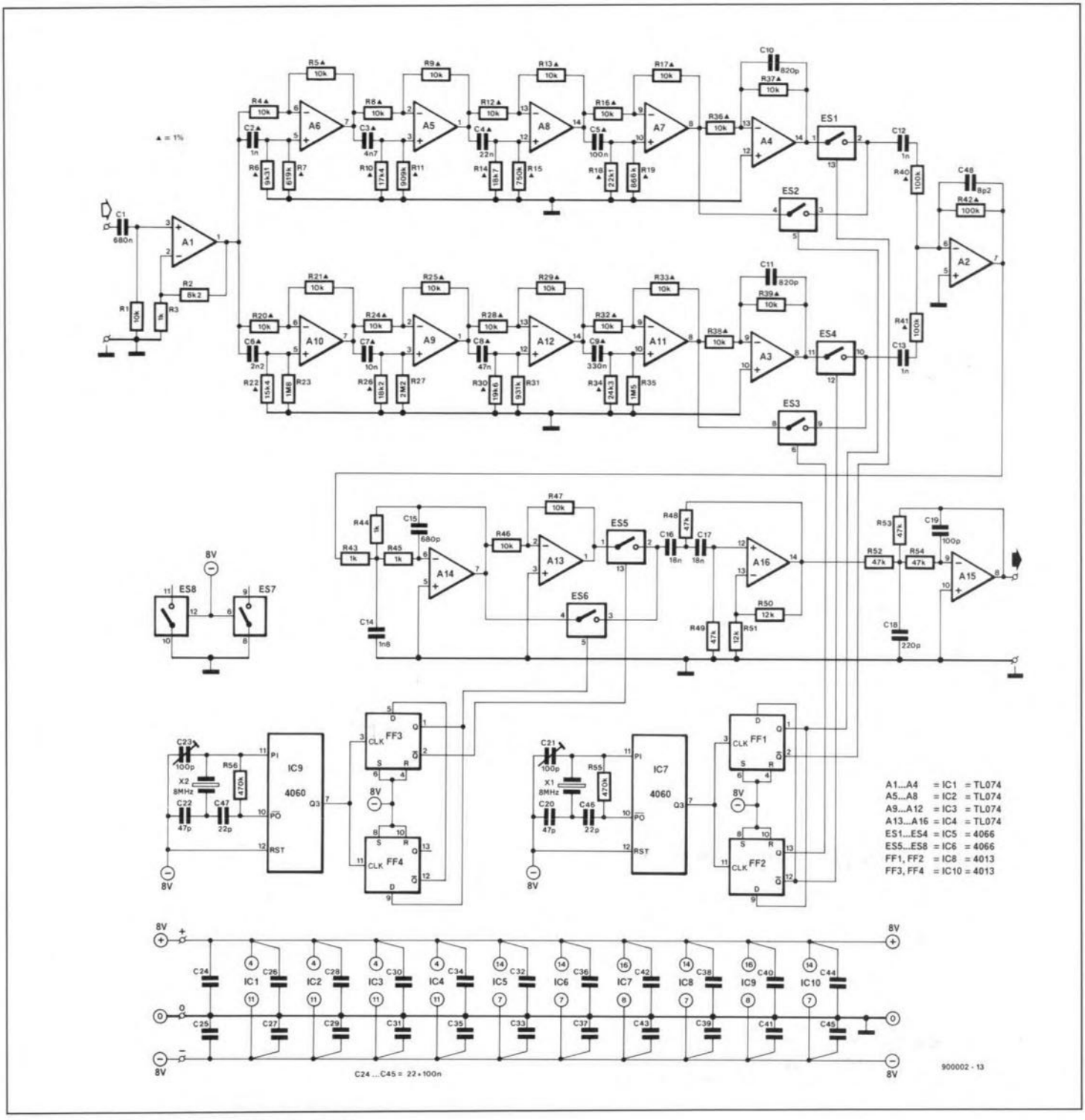


Fig. 3. Circuit diagram of the feedback killer.

quency equal to the sum of the frequency of the input signal and the frequency of the carrier with which it is mixed. The upshot is that the input signal is shifted over a small range in the frequency spectrum. Although the equation shows that the sum signal is a single frequency component only, it should be noted that this is only valid if the input signal is shifted exactly 90°. Unfortunately, this is only possible in theory. Any practical circuit produces spurious signals that cause amplitude-modulation (AM) of the mixer output signal. The all-pass filter used in the feedback killer ensures a phase shift of very nearly 90° over a frequency range of 50 Hz to 7 kHz.

The output signal of the mixer is taken through an active low-pass filter. This operation is required because the input signal is multiplied by 90°-shifted rectangular waves, rather than a sine-wave and a cosine-wave which would have given rise to a considerably more complex circuit. From Fourier analysis, a rectangular wave is composed of a fundamental frequency and an infinite number of odd-numbered sine-wave harmonics as

$$4/\pi(\cos(\omega t)-1/3\cos(3\omega t)+1/5\cos(5\omega t) \ldots$$

The amplitude of the harmonics decreases with frequency. The use of two 90°-shifted rectangular waves results in a series of sine-wave products and a series of cosine-wave products. The harmonics are removed in the previously mentioned low-pass filter, so that only the wanted mixer product remains.

There are two ways of shifting the input signal over a small range (1 Hz–30 Hz)in the frequency spectrum: 1) use a low-frequency modulation signal or 2) mix the signal a second time with a signal of which the frequency is almost the same as that of the first rectangular wave. Next, remove the undesirable sidebands with the aid of a filter.

The second principle is adopted in the feedback killer. Two carriers of a relatively high, but slightly different, frequency

are used.

The sum signal, A, obtained from the first mixer is filtered before it is mixed with a carrier, $\sin(\omega_c+\delta)t$, where δ is the required shift in radians. The resulting signal, B, may be expressed as shown in Fig. 2. In the equation, $-\cos(\omega_s+2\omega_c+\delta)t$ is an unwanted sideband, and $\cos(\omega_s\delta)t$ the modulated input signal shifted by an amount δ in the frequency spectrum. If the carrier frequency is relatively high (approx. 125 kHz), suppressing the unwanted sideband is relatively easy with the aid of a band filter, which doubles as a filter for the sidebands that are generated by the use of rectangular waves in the second clock generator.

Circuit diagram

Figure 3 shows the circuit diagram of the feedback killer. The essential blocks in the circuit are an all-pass filter around IC2-IC3, an output filter around A15 and A16, and two clock generators around IC7–IC10. The audio signal is buffered by A1 before it is applied to the all-pass filter which introduces a phase shift of 90±0.5° for signals between 50 Hz and 7 kHz. The filter components have a tolerance of 1% to ensure that the deviation from 90° remains as small as possible (remember that the number of unwanted sidebands rises with the deviation from 90°). The frequency range of the all-pass filter restricts the practical use of the circuit to speech. The feedback killer, must, therefore, not be used with singers or musicians, since the absolute frequency shift upsets harmonic relations and so causes the performers to play or sing out of tune.

The all-pass filter is followed by a buffer, A3-A4, which introduces a phase shift of 180° required for the first multiplication with the rectangular signal supplied by the first clock generator. The multiplication proper is effected by electronic switches ES1–ES4 as illustrated in Fig. 4. The non-inverted and the inverted sine-wave is passed during the positive and negative half-cycle of the clock signal respectively.

Opamp A2 adds the two mixed signals, and supplies, in principle, the components of which the rectangular wave consists. The frequencies of the components are, however, raised by the frequency of the input signal. Opamp A14 suppresses all unwanted higher harmonics generated by the use of rectangular-wave clock (carrier) signals. As a result, the sum signal contains only the mixing product of the input signal and the fundamental frequency of the clock signal. The 'digital mixer' approach uses fewer components than an equivalent all-analogue (sine-wave/cosine-wave) circuit, and has the additional benefits of lower cost and the absence of adjustments.

The filtered signal is available in inverted form after opamp A13, and is mixed a second time with a clock signal. Like the first mixer, the second one uses electronic switches. The frequency difference between the two clock signals determines the effective frequency shift of the input signal. The output signal of the second mixer is taken through a second-order high-pass filter, A16, and a second-order low-pass filter, A15, to remove all unwanted harmonics. The AF output is a virtual copy of the input signal: the only difference is that it covers a slightly different range in the frequency spectrum.

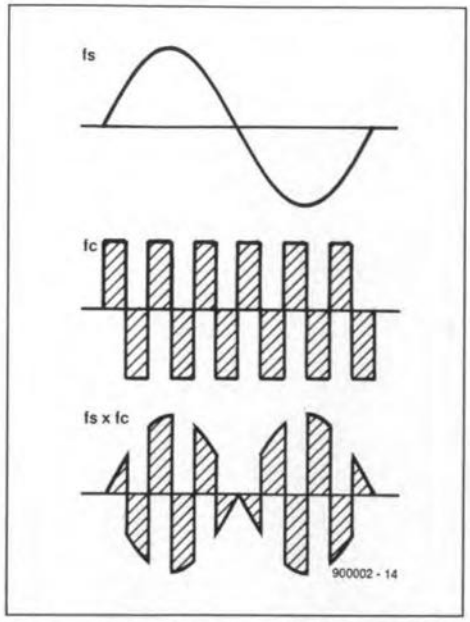


Fig. 4. Principle of frequency multiplication with the aid of electronic switches.

The clock generators around IC9 and IC7 are identical with a Type CD4060 oscillator/divider and an 8 MHz quartz crystal as the frequency determining element. The Q3-output of each CD4060 supplies the oscillator frequency divided by 16, i.e., 500 kHz. The two bistables (FF1-FF2 and FF3-FF4) secure the required phase shift of 90° between the two clock signals. In this operation, the clock frequency is divided by four, so that the carriers have a frequency of 125 kHz. The trimmer capacitors in the crystal oscillators allow the frequency shift applied to the AF input signal to be adjusted to requirement.

Components

The capacitors in the all-pass filter are preferably 1%-tolerance polystyrene ('styroflex') or silver-mica types, although the board allows MKT (plastic encapsulated multi-layer polytherephtelate) types to be fitted also. These capacitors from Siemens generally have a tolerance of 5%. Note that when MKT capacitors are used, there is little point in using 1% resistors. The use of 5%-tolerance components in the all-pass filter increases the amplitude modulation of the output signal.

Two types of PTFE foil trimmer, 10×5 mm raster and 5×7.5 mm raster, may be used in positions C21 and C23. Do not use ceramic types: they are not partly transparent as PTFE foil types and do not therefore allow the set capacitance to be deduced from the position of the rotor relative to the stator blades.

Be sure to use quartz crystals and CD4060's from one and the same manufacturer and, if possible, from a single batch (look at the production date indication, the type and batch number).

The circuit is a combination of analogue and digital electronics and has, therefore, relatively many decoupling capacitors to keep cross-talk and interference to a minimum. Fortunately, there is virtually no tolerance or quality requirement for the decoupling capacitors, so that inexpensive types may be used with impunity.

Construction and adjustment

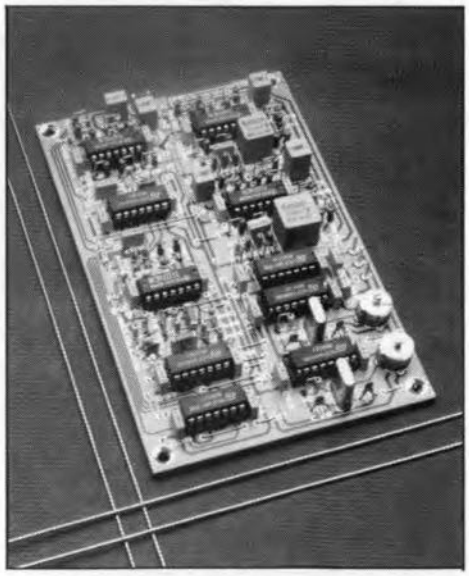
The circuit is preferably constructed on the single-sided PCB shown in Fig. 5. The construction is entirely straightforward and best started with fitting the wire links. Note that a fair number of resistors is mounted upright.

The adjustment of the circuit is simple. As already discussed, the frequency shift of the audio signal is determined by the frequency difference between the two crystal oscillators. This frequency difference is set with the respective trimmers, C21 and C23.

The function of the circuit is relatively easy to check. Set both trimmers to about one-third of their travel. Connect a two-channel oscilloscope to the input and the output of the feedback killer. Apply a sine-wave to the input and synchronize the top channel of the scope. The circuit works if adjustment of one of the two trimmers causes the (output-) signal on the lower channel to start moving horizontally across the scope screen.

The frequency shift required for optimum suppression of feedback depends largely on the equipment used, the power ratings and anticipated sound levels, and, of course, the acoustic characteristics of the listening room. Finally, it will be clear that the effect of the circuit is less noticed at relatively small frequency shifts.

The circuit draws less than 50 mA from a regulated ±5 V to ±8 V power supply. ■



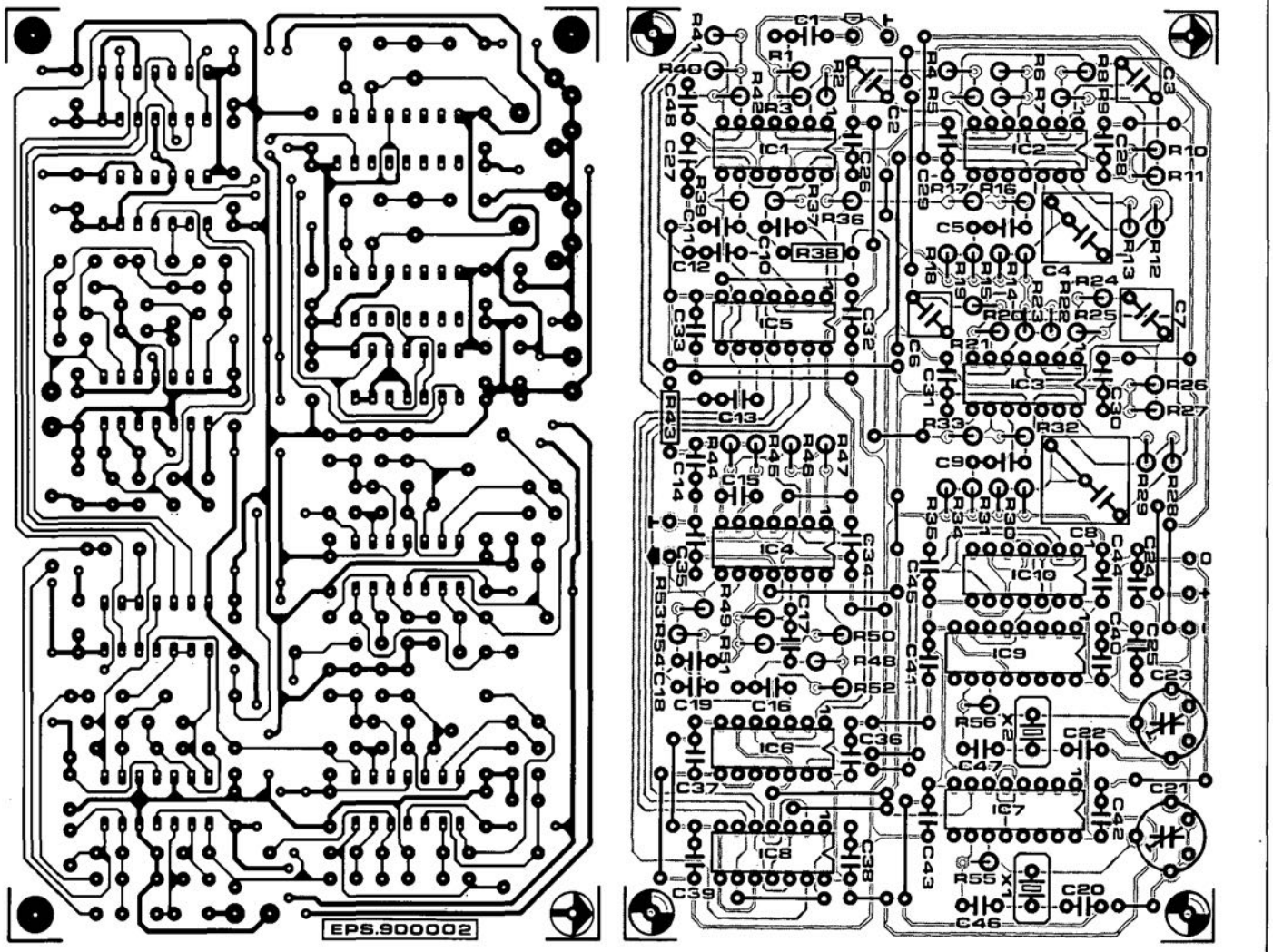


Fig. 5. Track layout and component mounting plan of the printed-circuit board for the feedback killer.

Parts list

Resistors:
R_1 = 10k
R_2 = 8k2
R_3;R_{43};R_{44};R_{45} = 1k0
R_4;R_5;R_8;R_9;R_{12};R_{13};R_{16};R_{17};R_{20};R_{21};R_{24};R_{25};R_{28};R_{29};R_{32};R_{33};R_{37};R_{38};R_{39};R_{46};R_{47} = 10k 1%
R_6 = 9k31 1%
R_7 = 619k 1%
R_{10} = 17k4 1%
R_{11} = 909k 1%
R_{14} = 18k7 1%
R_{15} = 750k 1%
R_{18} = 22k1 1%
R_{19} = 866k 1%
R_{22} = 15k4 1%
R_{23} = 1M8
R_{26} = 18k2 1%
R_{27} = 2M2
R_{30} = 19k6 1%
R_{31} = 931k0 1%
R_{34} = 24k3 1%
R_{35} = 1M5
R_{40};R_{41};R_{42} = 100k 1%
R_{48};R_{49};R_{52};R_{53};R_{54} = 47k
R_{50};R_{51} = 12k
R_{55};R_{56} = 470k

Capacitors:
C_1 = 680n
C_2 = 1n0 1%
C_3 = 4n7 1%
C_4 = 22n 1%
C_5 = 100n 1%
C_6 = 2n2 1%
C_7 = 10n 1%
C_8 = 47n 1%
C_9 = 330n 1%
C_{10};C_{11} = 820p
C_{12};C_{13} = 1n
C_{14} = 1n8
C_{15} = 680p
C_{16};C_{17} = 18n
C_{18} = 220p
C_{19} = 100p
C_{20};C_{22} = 47p
C_{21};C_{23} = 100p trimmer
C_{24} – C_{45} = 100n
C_{46};C_{47} = 22p
C_{48} = 8p2

Semiconductors:
IC_1 – IC_4 = TL074
IC_5;IC_6 = 4066
IC_7;IC_9 = 4060
IC_8;IC_{10} = 4013

Miscellaneous:
X_1;X_2 = quartz crystal 8 MHz.
PCB Type 900002 (not available ready-made through the Readers Services).

PC RADIO

This FM radio, designed by ELV GmbH, consists of an insertion card for IBM PC-XTs, ATs and compatibles and is available as a kit or a ready-built and aligned unit. The radio has an on-board AF power amplifier for driving a loudspeaker or a headphone set, and is powered by the computer. A menu-driven program is supplied to control the radio settings.

Take a look around many modern offices and you will notice PC users or terminal operators wearing headphones while sitting in front of their screens. In most cases, a portable radio or cassette recorder is placed on the desk or near the PC to lighten the work with a little music without annoying colleagues.

This PC radio with integrated power amplifier is constructed on an insertion card that can be plugged into any free bus extension slot on the motherboard of an IBM PC-XT, PC-AT or compatible computer running under MSDOS control.

The PCRADIO menu screen (control program version 1.2).

Control program and cursor keys

The control software for the radio is supplied on a 5¼-inch MSDOS formatted diskette with 360 KByte capacity. After the computer is switched on, this disk is inserted into one of the disk drives. Use the DOS to select the relevant disk drive and type PCRADIO to load and run the control program, which is automatically configured for the graphics adapter card used in the computer. The cursor keys are used to select the menu areas shown on the introductory photograph. The adjustments that can be made include bass, treble, volume, manual or automatic tuning and a signal-level- dependent muting. The volume area is selected as a default when the program is started. The left and right keys on the cursor keypad allow the volume to be reduced or increased respectively, while a coloured horizontal bar on the screen indicates the relative setting. A further volume indication is provided by a large two-digit number to the right of the bar. The volume setting can take values between 0 and 63.

The up and down cursor keys select the menu areas. Pressing ↓, for instance, moves the PC radio setting from the volume to the treble area, which uses a coloured bar and a two-digit indication like the volume setting. Pressing ↓ again selects the bass setting. Here, again, the ← and → keys may be used to change the setting.

The next area reached by pressing ↓ from the bass area is the tuning control. Press the → and ← keys to tune up and down respectively. The frequency step size in the VHF FM band is 10 kHz. The tuning rate is increased automatically to about 2 MHz per second if the ← or → keys are depressed longer than necessary for a single keystroke. The fast tuning feature allows the full VHF FM broadcast band to be covered in about 10 seconds.

Manual tuning is accomplished by typing the required frequency on the number keys. Automatic station scan is selected on pressing the ↑ or ↓ key. In this mode, the ← and → keys select between scanning up or down from the current frequency. The scanner stops when a station is received. If the band is empty (hardly likely these days) or if the stations are too weak, the radio automatically reduces its detection threshold and starts a new scan. The high sensitivity mode may also be entered by pressing the scan cursor keys twice within one second at the start of the station scan.

The relative field strength of the received station is indicated in the lower left-hand corner of the screen. The 'mute' function allows the level to be defined below which the AF amplifier of the radio is automatically muted. This function eliminates noise between stations as the scan mode is in operation. It is selected via the ↑ and ↓ keys, while the ← and → keys allow the mute level — displayed in a different colour — to be adjusted to individual requirement. Reception of very weak signals is made possible by moving the mute bar to the extreme left of the screen.

The menu area in the lower right corner of the screen is reserved for the station name, provided this is among the ones listed to the left of the screen. Any station can be pre-programmed. When it is listed, it may be selected rapidly by pressing the associated function key F1 through F10.

Stations are pre-programmed as follows. First, tune to the desired station, then hold the SHIFT key depressed before pressing the function key to define the station number in the list. Next, type the station name on the keyboard and press ENTER.

The PCRADIO control program is left on pressing ESC (escape). Next, the user is asked whether or not the previously made changes to the settings and the station list are to be saved or cancelled. After going through this menu, the user is returned to the DOS prompt. The radio remains on, however, using the current settings, although the control program is removed from the computer's memory. The computer is ready to load and run other software at this stage.

For advanced PC users

The following information is aimed at advanced PC users, allowing them to use a number of special features of the PC radio.

The PC radio kit is supplied with a diskette that, apart from the previously described user software, contains a documentation file, READ.ME, and an installation program, INSTALL.EXE. Hard copy of the (ASCII-) READ.ME file is obtained in the usual way by typing CONTROL-P followed by TYPE READ.ME and a carriage return. Turn off the printer again by typing CONTROL-P.

The PCRADIO program may be made memory-resident by calling it up with a switch: PCRADIO /I <CR>. The program may be called up while another program is running by pressing the two SHIFT keys simultaneously. This key combination may be changed to requirement as detailed further on. The radio settings in use may be changed as described earlier, but they can not be saved to disk in the resident mode of the control program. The PCRADIO program is left by pressing the ESC key. It may be cleared from the resident program memory by typing PCRADIO /R from the DOS prompt.

The installation program allows a number of hardware and software parameters to be pre-defined. Its menu starts with the I/O address, which has been set to default 300H on the PCB as well as in the control program. Changes may be made as required. Next, the system checks if the PC radio card can be addressed in the selected I/O area.

The next menu step allows the user to define the key combination for calling up the memory-resident program. The default is the left and right SHIFT keys on the keyboard. Depending on whether other memory-resident programs use the same combination, this may be changed via a submenu.

Block diagram

With reference to the block diagram in Fig. 1, a special feature of the VHF tuner block that receives the signal from the external aerial is that it contains an IF (intermediate frequency) stage as well as an audio preamplifier. This allows the output of the tuner to be connected direct to a tone control section, which has direct voltage inputs for the bass, treble and volume settings. The output signal provided by the tone control stage is applied to an on-board AF power amplifier capable of driving a 4 Ω loudspeaker.

The control voltages for the tuner and the preamplifier/tone control section are provided by digital-to-analogue converters (DACs) which translate the binary values obtained as digital combinations from the PC bus via a databuffer into corresponding voltage levels. A 12-bit DAC supplies the tuning voltage for the variable capacitance diodes (varicaps) in the FM tuner. The field strength voltage is sent to the computer via an A-D converter. The DACs for volume-, bass and treble control are 6-bit types which offer ample resolution for the purpose.

Circuit description

The circuit diagram of the PC radio is given in Fig. 2. The operation of the four main circuit sections that make up the PC radio is discussed under separate headings.

VHF FM tuner

The aerial signal is applied to the mixer inputs of the TDA7021, pins 12 and 13, via bandfilter L_1-C_{27}-C_{28}-C_{29}. The bandfilter suppresses signals outside the VHF FM broadcast band. In the configuration used, the Type TDA7021T single-chip FM receiver achieves a sensitivity of about 4 µV. The local oscillator frequency is determined by external components L_2-C_{30}-C_{32} and varicap KD_1. The LO is tuned by applying a direct voltage between 0 V and 10 V to R_{71}. The IF amplifier on board the TDA7021T operates at 76 kHz, and uses only three external capacitors, C_{33}, C_{34} and C_{35}. The field strength (f-s) output of the chip, pin 9, supplies a current of about 20 µA when a strong station is received, and about 150 µA when no station is received. This current is passed through R_{74} on which it causes a proportional voltage. Capacitor C_{41} eliminates short variations of the field strength voltage.

The amplified IF signal is internally demodulated, and the resultant AF signal is applied to an on-board AF amplifier. The AF output voltage of the chip has an amplitude of about 80 mV_{pp} at pin 14.

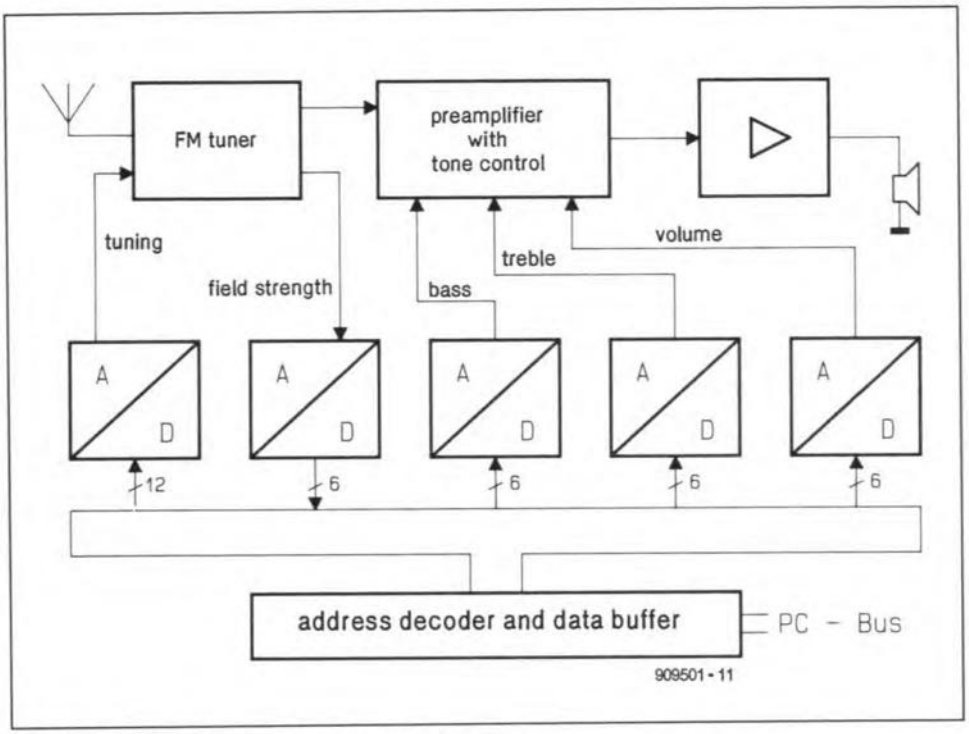


Fig. 1. Block diagram of the PC radio card.

Tone control

The Type TDA1524A preamplifier/tone control chip receives its input signal via C_{42}. The second input of the chip, pin 4, is decoupled by C_{43} because the stereo mode is not used in this application. Direct voltages applied to pins 1, 9 and 10 enable the tone and volume parameters to be set with the aid of the internal electronic potentiometers. Capacitors C_{44} and C_{45} and resistor R_{77} are used for the bass control, while treble control is effected with C_{46}. Resistor R_{95} is optional, and selects between linear and contour operation of the preamplifier. If chip output pin 17 supplies a current between 1.5 mA and 10 mA, the preamplifier works linearly. If the current is smaller than about 0.5 mA, the loudness/contour correction is actuated.

The bass response of the TDA1524A also depends on external components. R_{77} may be omitted, and C_{45} or C_{44} may be replaced by a wire link to limit the low frequency range.

The chip receives its supply voltage via pin 3. The chip supply voltage is cleaned and buffered by C_{48} and C_{47} respectively.

AF power amplifier

The AF output signal at pin 11 of the TDA1524A is coupled out with C_{49} and taken to input pin 1 of an integrated AF power amplifier, IC_{16}, a Type TDA2030. This chip provides a voltage amplification of about 8 as well as the necessary current amplification in its power output stage.

Since the chip output is at about half the supply voltage, a coupling capacitor, C_{53}, is required to connect the loudspeaker. Components R_{83} and C_{56} suppress any tendency of the AF amplifier to oscillate.

Digital section

The description of the digital section of the PC radio card is best started at the address decoder. This consists of an 8-bit comparator, IC_4, for the base address, and two 1-of-4 decoders in IC_3 for the addresses within the selected block. Address lines A2 through A9 are applied to the comparator to achieve block decoding. The base address is set with jumpers Br_1 through Br_8. Omitting jumpers Br_1 and Br_2, for instance, selects base address 300H, the default setting of the card (consult Table 1 for the address assignment).

When the CPU in the PC addresses I/O location 300H (A8 and A9 are high), output $\overline{P=Q}$ of IC_4 goes low. Assuming that the I/O access is a write operation (i.e., pin 4 of IC_2 is low), pin 15 of IC_3 goes low also. Depending on the bit combinations on address lines A0 and A1, one of four outputs Y0 through Y3 changes to low. If, for instance, address 302H is selected, pin 11 of IC_{3b} goes low and provides a latch pulse for IC_7. The 8-bit word on the databus is latched into D-type register IC_7, which holds the bass setting.

The four 6-bit D-A converters are discrete types set up around four 8-bit latching registers, IC_6 through IC_9, and associated R-2R ladder networks. The voltage at the output of each ladder is programmable between 170 mV and 3.2 V in 64 steps.

Circuit IC_9, an 8-bit latch, is used for driving the 12-bit D-A converter, IC_{10}, as well as for field strength measurement.

The 12-bit DAC receives an 8-bit word from IC_9, and 2-bit words from IC_7 and IC_8. The DAC reads these words from address BASE+1. The reference voltage for the DAC is provided by voltage divider R_{62}-R_{63} at pin 19. Opamp IC_{11a} supplies a voltage between 0 V and −1 V in 4,096 (10^{12}) steps. This voltage is amplified and inverted by a further opamp, IC_{11b}. Resistors

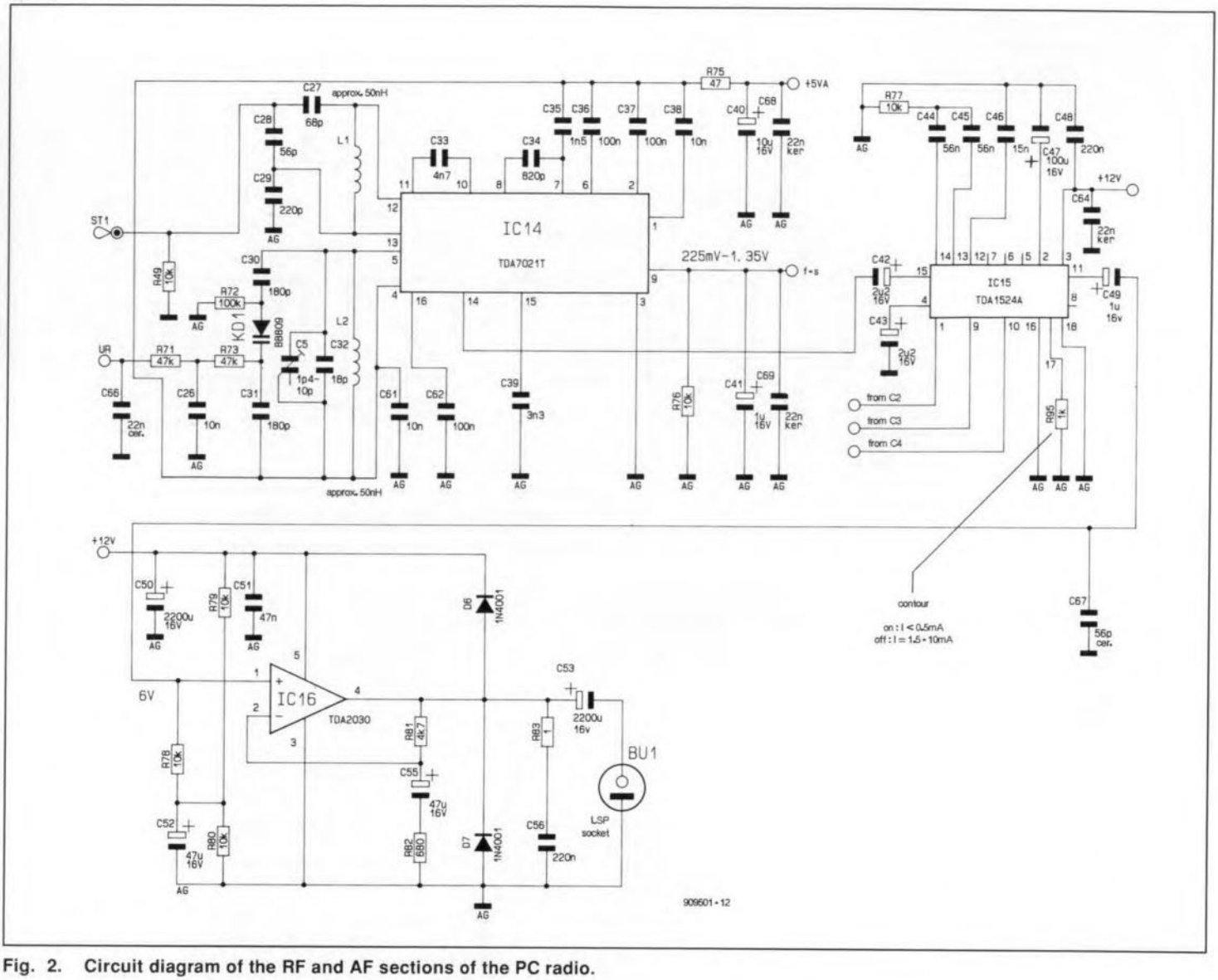


Fig. 2. Circuit diagram of the RF and AF sections of the PC radio.

R_{71} and R_{73} feed the tuning voltage to the varicap in the FM tuner. The gain of the second opamp is adjustable over a relatively wide range to allow the tuning range required to cover the FM band to be set with preset R_{92}.

The field strength voltage provided by the TDA7021T is applied to pin 10 of opamp IC_{11c}. A field strength indication of 0 on the screen corresponds to about 1.35 V, and one of 63 to about 245 mV. The opamp raises the field strength voltage to a level at which pin 12 of comparator IC_{11d} is held at a voltage of between 0 V and 4 V. The DAC built around IC_9 and the R-2R network allow the comparator threshold at pin 13 of IC_{11d} to be changed. The output state of the comparator can be requested at I/O address BASE+1 via buffer IC_{12a}. Since the output voltage of the opamp can take values between –5 V and +12 V, R_{69}, R_{70}, D_4 and D_5 are required to limit the voltage to 0 V and 5 V.

The remaining three drivers in IC_{12} are used to check the addressing of DACs IC_6, IC_7 and IC_8.

The circuit is reset at power-on by a 100-ms long low pulse at pins 1 and 2 of IC_{5a}. This causes bistable IC_{5c}-IC_{5d} to be reset via gates IC_{2a} and IC_{5b}. Transistor T_1 short-circuits the voltage at pin 1 of the TDA1524A to ground to reset the internal electronic volume potentiometer. After 100 ms, pin 4 of IC_5 reverts to logic high, and it can be set, i.e., pin 6 can be made low, by a read operation to address BASE+2 via IC_{3a}. Depending on the position of jumper JP_1, the radio may also be switched

Off-set address	read operation	write operation
0 (base)	D5 – D0 = 6-bit DAC for volume control	D0 = comparator output for field-strength measurement
	D6 = not used	D1 = control bit 1
	D7 = control bit 1	D2 = control bit 2
		D3 = control bit 3
+1	D5 – D0 = 6-bit DAC for bass control	latch data into 12-bit DAC
	D7; D6 = D9; D8 for 12-bit tuning DAC	
	D7 = control bit 2	
+2	D5 – D0 = 6-bit DAC for treble control	turn on AF
	D7; D6 = D11;D10 of 12-bit tuning DAC	
	D7 = control bit 3	
+3	D5 – D0 = 6-bit DAC for field-strength	turn off AF
	D7 – D0 = D7 – D0 for 12-bit tuning DAC	

Table 1. Input/output address assignment on the PC radio card.

to mute when the PC is reset. Another possibility to control the mute function exists in a read operation to address BASE+3 (IC3a pin 7).

All supply voltages for the circuit are taken from the PC expansion bus. Note, however, that the 5 V supply for the analogue circuits is provided by voltage regulator IC13.

Construction

The complete circuit is built on a double-sided through-plated printed circuit board supplied with the kit. The size of the

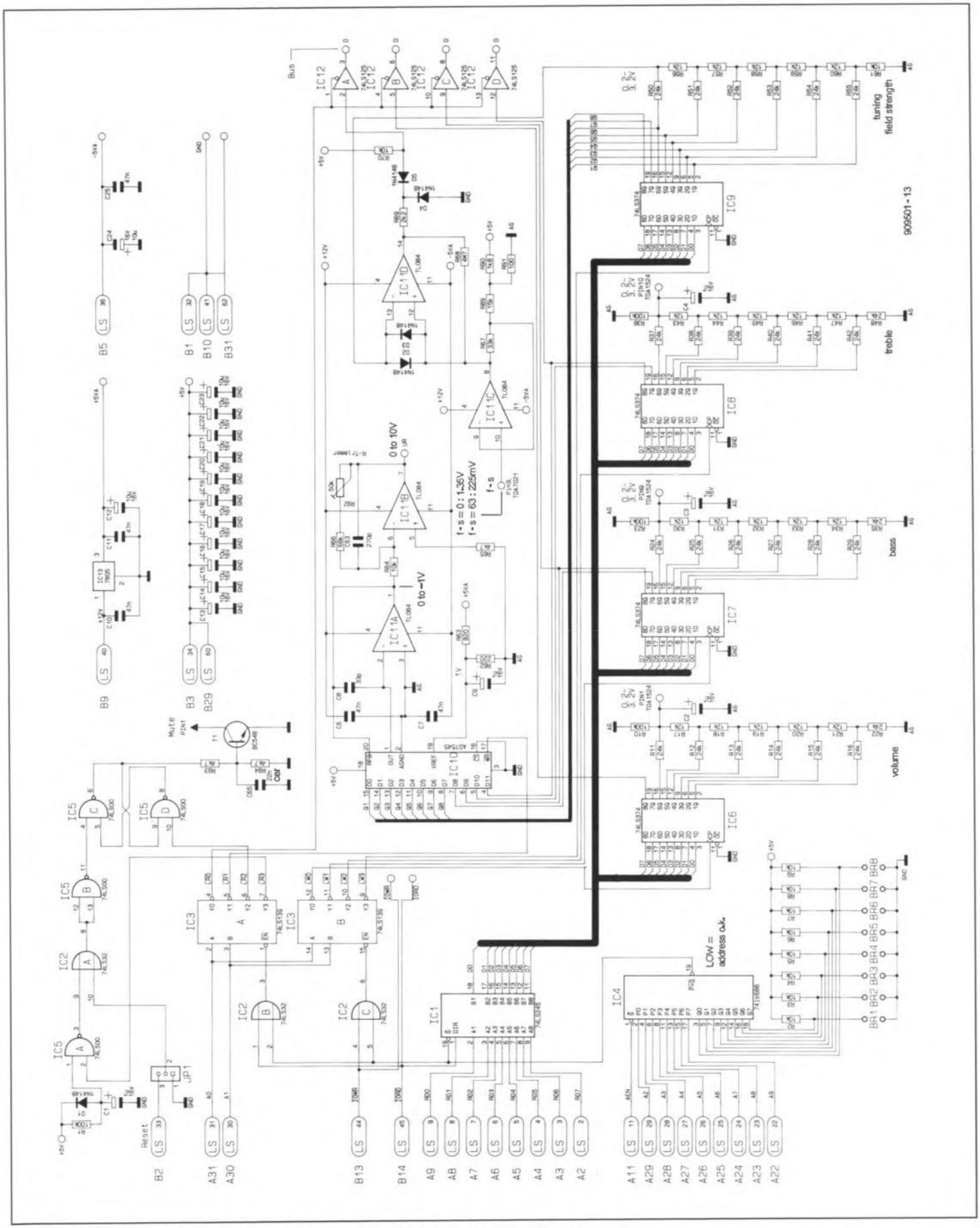


Fig. 3. Circuit diagram of the digital section and the PC-interface of the FM radio card.

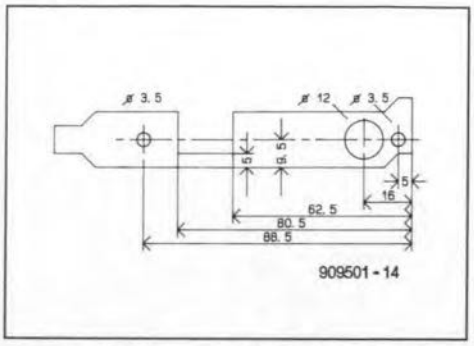


Fig. 4. Cutting and drilling details of the aluminium support bracket.

board is 230×108 mm.

Start with fitting the low-profile components as per the indications on the component overlay (Fig. 5) and the parts list. Proceed with the taller components. Since the board is through-plated, soldering at the component side is not required. Leave the wire terminals of C_{50} and C_{53} longer than usual to enable these capacitors to be bent towards the board as shown in the photograph. The TDA2030 and its heat-sink are also mounted horizontally and secured on to the board with an M3 bolt.

The TDA7021T FM receiver chip is an SMA (surface-mount assembly) type which requires great care and precision in handling as well as soldering. First place the IC on to the board. Next, position it accurately with the aid of a pair of tweezers so that the terminals align with the solder areas. Use a low-power solder iron with a fine tip and a power rating of not more than 16 W to solder one of the corner pins of TDA7021T to the associated track. Next, use a sharp device to align the other IC pins with the tracks below. Heat the pins briefly in rapid succession while applying very little solder.

Interconnect the points marked A and those marked B on the PCB with an insulated wire of 0.4 mm^2 cross-sectional area or larger.

The position of the tin-plate screen around the FM tuner section on the PCB is shown in the top view of the completed printed-circuit board in Fig. 5. Bend the screen in the form of a rectangle and join its ends by soldering. Place the screen so made vertically on to the component side of the PCB, and align it with the PCB edges. This is necessary for the PCB support bracket which is secured to the screen later. Solder the screen to the PCB, applying a generous amount of solder tin from the inside, but taking care not to damage components by overheating. Be sure to cover the entire length of the screen, i.e., do not solder it to the PCB in just a few locations. Next, bend and fit a similarly shaped, but lower, screen on to the component side of the PCB, opposite the screen just mounted. Drill a hole in the taller screen for the aerial input socket (9.4 mm dia.).

Use an M3×6 mm bolt, a washer and a nut to secure a small aluminium bracket to the lower side of the PCB. Next, prepare a standard PCB support bracket as shown in Fig. 4. Secure this bracket and the aerial input socket to the screen on the PCB. Solder the socket to screen, and secure the support bracket to it with two M3×6 mm bolts and nuts. Connect a short piece of insulated wire between the signal pin of the socket and point ST1 on the PCB. Note the position of C_5 on the PCB and drill a hole in the metal cover to be mounted on to the screen at the component side of the board. This hole serves to access C_5 with a trimming tool. Solder the covers to the two screens.

Install the PC radio card into the computer, and screw the support bracket to the back panel. Do not forget to check that this panel is connected to ground of the PC — this is essential for the FM tuner on the PC radio card. Finally, connect an FM aerial via 75 Ω coaxial cable.

Parts list

Resistors:
R_{83} = 1Ω0
R_{75} = 47Ω
R_{91} = 100Ω
R_{62} = 220Ω
R_{82} = 680Ω
R_{63} = 820Ω
R_{95} = 1k0
R_{90} = 1k8
R_{69} = 2k2
R_{65};R_{81};R_{93};R_{94} = 4k7
R_2 – R_9;R_{49};R_{61};R_{64};R_{70};R_{76} – R_{80} = 10k
R_{17} – R_{21};R_{30} – R_{34};R_{53} – R_{47};R_{56} – R_{60} = 12k
R_{89} = 15k
R_{11} – R_{16};R_{22};R_{24} – R_{29};R_{35};R_{37} – R_{42};R_{48};R_{50} – R_{55} = 24k
R_{67} = 33k
R_{71};R_{73} = 47k
R_{66} = 68k
R_1;R_{10};R_{23};R_{36};R_{72} = 100k
R_{68} = 4M7
R_{92} = 50k preset V

Capacitors:
C_{32} = 18p
C_8 = 33p
C_{28};C_{67} = 56p
C_{27} = 68p
C_{30};C_{31} = 180p
C_{29} = 220p
C_{63} = 270p
C_{34} = 820p
C_{35} = 1n5
C_{39} = 3n3
C_{33} = 4n7
C_{26};C_{38};C_{61} = 10n
C_{46} = 15n
C_{64};C_{65};C_{66};C_{68};C_{69} = 22n ceramic
C_6;C_7;C_{10};C_{11};C_{25};C_{51} = 47n
C_{44};C_{45} = 56n
C_{36};C_{37};C_{62} = 100n
C_{48};C_{56} = 220n
C_1 – C_4;C_9;C_{41};C_{49} = 1µ0; 16 V
C_{42};C_{43} = 2µ2; 16 V
C_{12} – C_{24};C_{40} = 10µ; 16 V
C_{52};C_{55} = 47µ; 16 V
C_{47} = 100µ; 16 V
C_{50};C_{53} = 2200µ; 16 V
C_5 = 40p trimmer

Semiconductors:
IC_{10} = AD7545
IC_{15} = TDA1524
IC_{16} = TDA2030
IC_{14} = TDA7021T (SMD)
IC_5 = 74LS00
IC_2 = 74LS32
IC_{12} = 74LS125
IC_3 = 74LS139
IC_1 = 74LS245
IC_6 – IC_9 = 74LS374
IC_4 = 74LS688
IC_{11} = TL084
IC_{13} = 7805
T_1 = BC548
KD_1 = BB809
D_6;D_7 = 1N4001
D_1 – D_5 = 1N4148

Miscellaneous:
Bu_1 = loudspeaker socket.
Qty 1: SK13 heat-sink
Qty 1: coax socket.
Qty 1: 3-way pin header.
Qty 1: jumper.
Qty 1: aluminium bracket.
Qty 1: tin-plate for screening
Qty 3: screw M3×6.
Qty 1: screw M3×8.
Qty 4: nut M3.
Qty 1: metal cover.
Solder pins.
90 mm insulated wire, min. 0.4 mm^2.
140 mm silver-plated wire.
3 m coaxial cable.

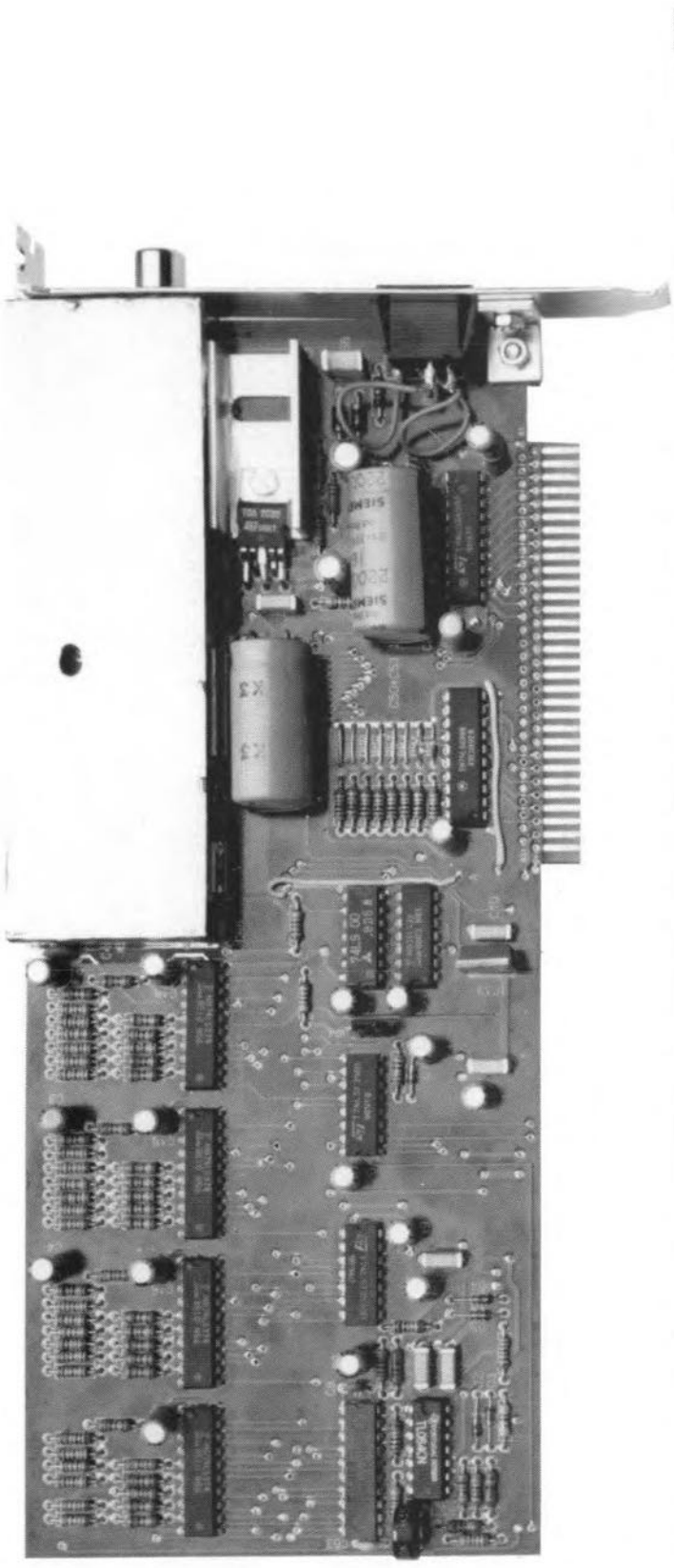
A complete kit of parts for the PC radio is available from the designers' exclusive worldwide distributors (regrettably not in the USA and Canada):

ELV France
B.P. 40
F-57480 Sierck-les-Bains
FRANCE
Telephone: +33 82837213
Fax: +33 82838180

Also see ELV France's advertisement elsewhere in this issue.

Adjustment

Start the PC radio program from floppy- or hard disk. Use the menu to set the frequency to that of a station in the lower range of the FM band, e.g., to 88.5 MHz. Align C_5 with an insulated trimming tool until this station is received (use a second radio as a reference). Next, set a receive frequency near the top of the band, e.g, 104 MHz, and adjust R_{92} until a previously selected station is received. If the adjustment of C_5 is correct, the frequency shown on the menu screen corresponds to the transmit frequency of the station.



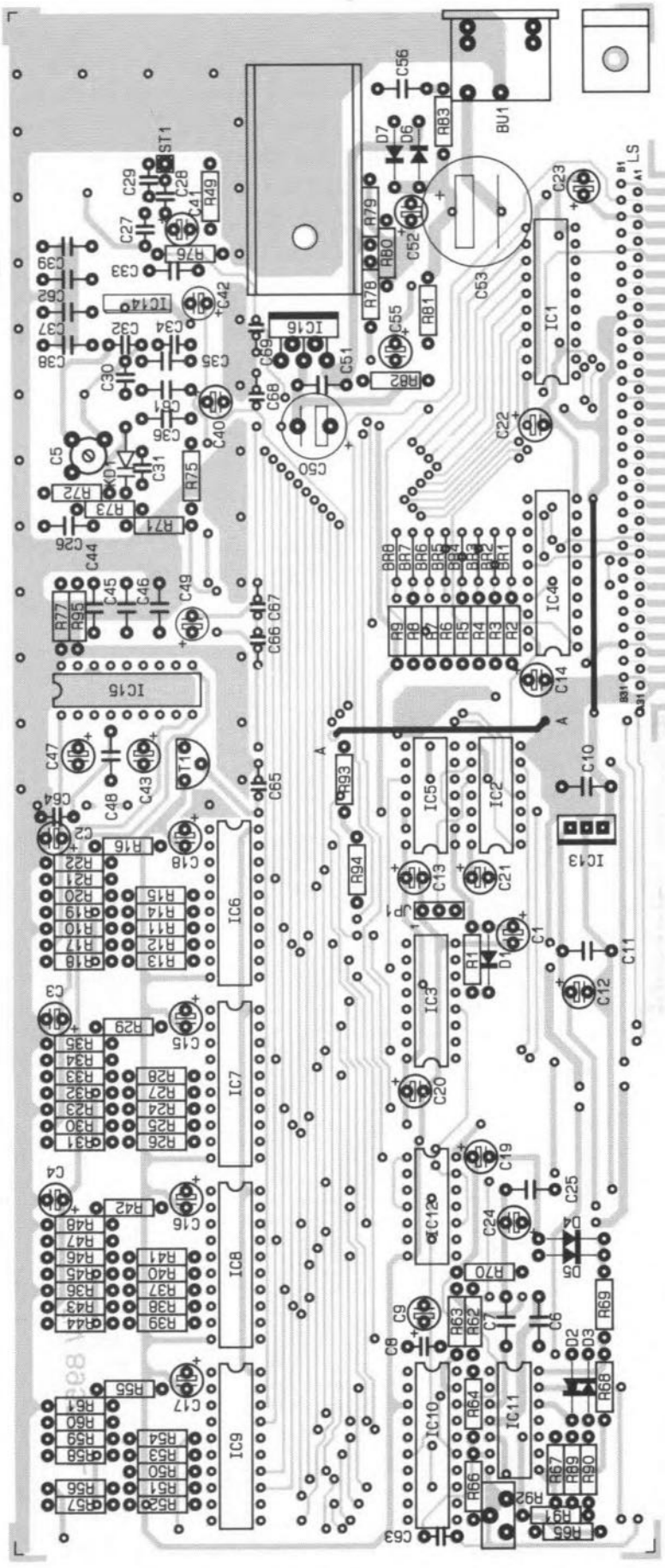


Fig. 5. Top view of the completed PC radio card with the screening installed (left) and the component mounting plan (right).

AC-DC CURRENT SENSORS

Current may be measured without introducing losses in its path with the aid of the well-known series current transformers with clip-on probes or reed sensorsin which a contact is closed by the presence of a magnetic field. These devices suffer from a serious drawback, however: they can not measure direct currents. The sensors described here depend on the Hall effect and are suitable for measuring both alternating and direct currents.

The Hall effect

The Hall effect is observed in thin strips of metal and in some semiconductors. When a strip carrying current is placed in a magnetic field that is perpendicular to the strip's plane, a voltage appears between opposite edges of the strip that, although it is weak, will force a current through an external circuit.

The force due to the magnetic flux density, B, on a charge carrier of charge e and drift velocity, v, is equal to evB. This force displaces the carriers and sets up a non-uniform charge distribution that gives rise to an electric field, E. At equilibrium, the force on the charge carriers, eE, due to this field just balances that due to the flux density:

$$eE + evB = 0.$$

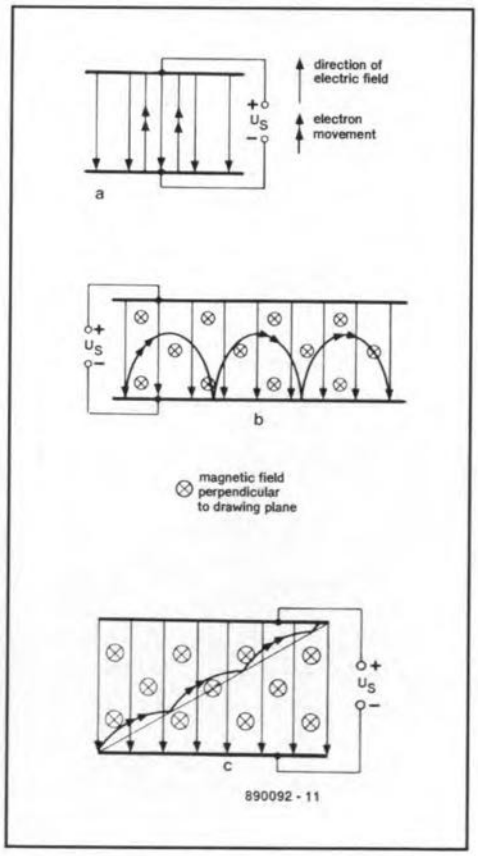


Fig. 1. Movement of electrons in: (a) an electric field; (b) a homogeneous electro-magnetic field in a vacuum; and (c) in a degenerate semiconductor material.

The drift velocity is related to the current density, j, by

$$j = nev$$

where n is the number of charge carriers per unit volume. Thus, the electric field is related to the vector product of the magnetic flux density and the current density by:

$$E = -R_H(jB)$$

where R_H is the Hall coefficient that is equal to $1/ne$. The electric field results in a potential difference, U_H, the Hall voltage, across the material.

In some materials, the direction of the field is reversed, which means that these materials have a positive Hall coefficient. This indicates that in these materials the current is carried by positively charged carriers, that is, by holes.

Electrons in an electric field move in straight lines as shown in Fig. 1a, whereas in an homegeneous electro-magnetic field they follow cycloidal paths (Fig. 1b). In degenerate semiconductor materials, they can not follow such paths owing to frequent collisions with atoms of the semiconductor material. Because of these collisions, the electrons lose velocity and this results in a waning of the magnetic field, since the strength of that field is directly proportional to the velocity of the charge carriers. The electrons are consequently attracted more strongly by the electric field as shown in Fig. 1c.

When a wafer of semiconductor material is connected as shown in Fig. 2 and placed in a magnetic field, an e.m.f., the Hall voltage, U_H, is generated across the longer sides of the wafer. Because of this, the wafer is called a **Hall generator.** The level of the e.m.f. is directly proportional to the strength of the magnetic field. If the direction of the field is reversed, the direction of the voltage also changes by 180°. Within certain limits, the e.m.f. is

$$U_H = R_H jB / d$$

where d is the thickness of the wafer. Note that the Hall voltage is inversely proportional to the thickness of the material.

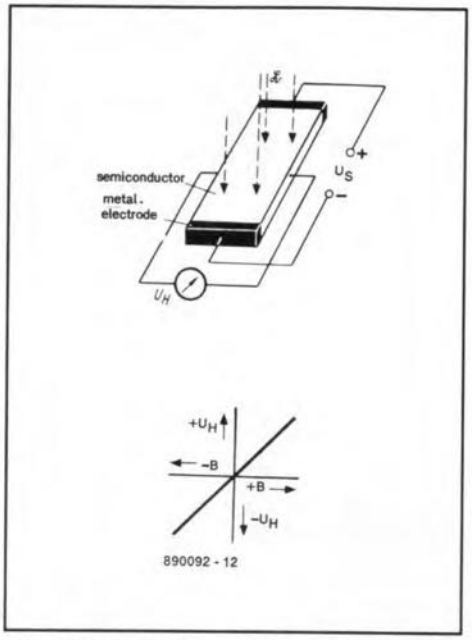


Fig. 2. The Hall voltage, U_H, is generated across the longitudinal sides of a Hall generator.

Hall generators have come more into vogue with the arrival of semiconductor materials such as indium antimonide (InSb) and indium arsenide (InAs), which have a high electron mobility, resulting in a large Hall coefficient, and a low specific resistance. Table 1 gives a comparison of the electron mobility (average drift velocity per unit electric field), v, in copper and a number of semiconductor materials.

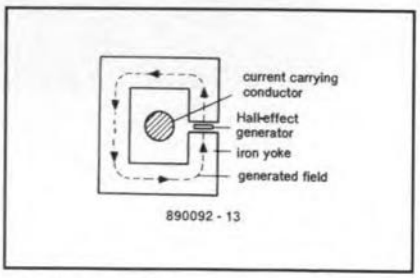


Fig. 3. With the Hall generator in the air gap of the iron yoke of a current sensor, the Hall voltage is directly proportional to the current flowing in a conductor that is at right angles to the cross-sectional plane of the yoke.

Material	Type	Drift velocity ($cm^2\ V^{-1}\ s^{-1}$)
copper	metal	27–43
silicon	group 4 semiconductor	1350
germanium	group 5 semiconductor	3900
InAs	$A^{III}\ B^{V}$ semiconductor	23 000
InSb	$A^{III}\ B^{V}$ semiconductor	65 000

Table 1. Electron mobility in copper and a number of semiconductor materials.

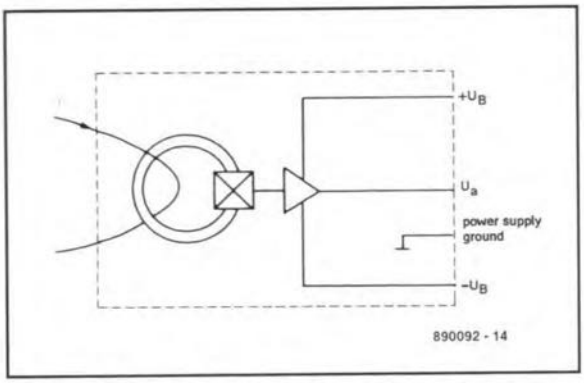


Fig. 4. Basic circuit of a direct-reading current sensor.

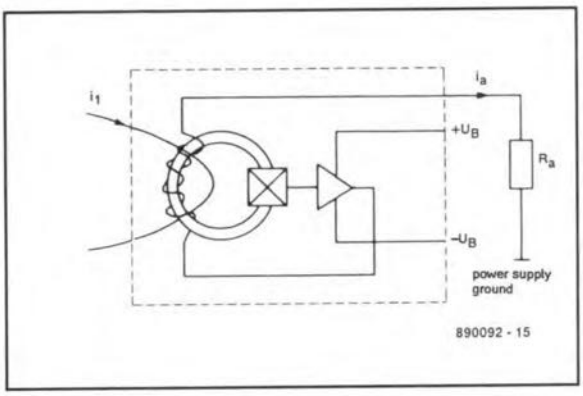


Fig. 5. In a compensating current sensor, the Hall element generates a current in a secondary winding.

Parameter	Direct-reading	Compensating
Current rating	150–3000 A	100–250 A
Nominal output	10 V	100 mA
Nominal output impedance	10 kΩ	50 Ω
Supply current	15 mA	8 mA
Supply voltage	±15 V	±15 V
Ambient temperature	0–80 ° C	–25 to +70° C
Measuring accuracy	≤2%	≤0.5%
Linearity	≤1%	≤0.1%
Drift with temperature	≤250 ppm/° C	≤50 ppm/° C
Max frequency	10 kHz	75–300 kHz
Response time	±30 µs	±1 µs
Output signal:		
Offset	≤20 mV	≤1 mA
Drift	20–50 mV	0.05–0.1 mA
Hysteresis	≤25 mV	≤0.2 mA
Drift with temperature	≤1 mV/° C	≤12 µA/° C
Drift with supply voltage	≤0.1–10 mV/V	≤0.01–0.03 mA/V

Table 2. Comparison of parameters of direct-reading and compensating sensors.

Note that in spite of the high value of v in indium antimonide this material is not used much because of the fairly large change in v with temperature: over the temperature range 20–120° C, for example, the value of v changes by a factor 5.

Practical sensors

In practice, the wafer thickness is of the order of 1–5 µm, which not only gives a larger Hall voltage, but also enables the wafer to be used in very small air gaps necessitated by weak magnetic fields. This may be seen in the schematic representation of a sensor in Fig. 3, in which the Hall voltage is directly proportional to the current flowing through a conductor that is perpendicular to the cross-sectional plane of the yoke of the sensor.

There are two types of Hall-effect current sensor: direct-reading and compensating—see Fig. 4 and Fig. 5.

The main advantage of the direct-reading type lies in the minimal losses it causes, which is, of course, particularly important when large currents are measured. The amplified output voltage, u_a, is directly proportional to current i_1.

The compensating type is particularly useful at higher frequencies—see Table 2. The current to be measured is coupled magnetically to a secondary winding on the yoke. The Hall element serves as a detector for the magnetic '0' which is induced with the aid of an auxiliary (compensating) current fed into the secondary winding. This compensating current is a very precise measure of the primary current. This type of sensor is eminently suitable for measuring square-wave currents.

Equivalent parameters of the compensating sensor may be determined from a four-quadrant diagram as in Fig. 6. If, for example, the r.m.s. value of the current to be measured is 100 A, its peak value is 150 A, and the maximum ambient temperature is 70° C. Drawing lines at right angles to the three corresponding axes gives a load resistance of 40–50 Ω. ■

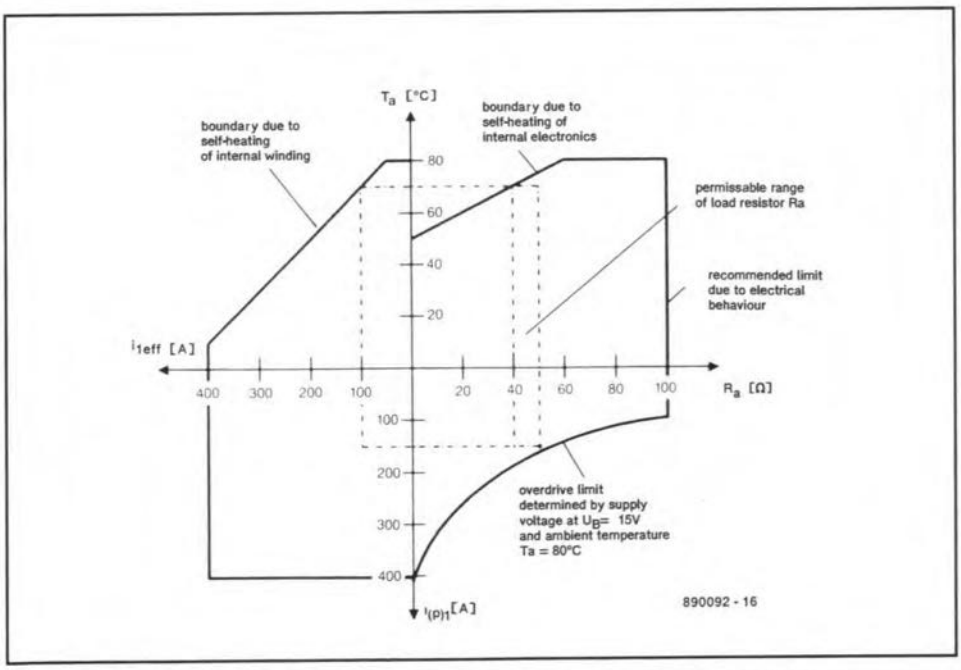


Fig. 6. The operating parameters may be determined from a four-quadrant diagram.

VIDEO MIXER

87304-II

PART 2: MODULATION BOARD

A. Rigby & G. Dam

Last month's introductory article described the general setup of the video mixer, and discussed the operation and construction of the video switching board. This month we turn our attention to the modulation board which supplies two sets of modulation waveforms that together put many attractive picture mixing, wipe, fade-in and fade-out effects at your disposal.

As already discussed in Part 1 of this article, the video mixer consists of three blocks: a video switching board, a modulation board and a keyboard. These blocks form the basic configuration of the mixer as shown in Fig. 1 in last month's instalment. The modulation board and the keyboard receive a number of synchronization signals and the supply voltage from the video switching board. The keyboard circuit supplies all the necessary control signals to the video switching board and the modulation board.

Effects waveforms

All picture mixing effects provided by the video mixer, and all combinations thereof selected by the user, are based on three elementary waveforms: the triangle, the ramp (linearly rising sawtooth) and the parabola. All three are available in the horizontal (line-synchronous) as well as the vertical (raster-synchronous) picture plane.

All picture mixing and combination effects rely on the switching between two video sources. A left-to-right wipe (curtain) effect, for instance, requires a circuit that switches between two video sources at accurately defined instants in the picture line. The HSW signal is used for this purpose. Similarly, the VSW signal is used if the wipe effect is required vertically (top-to-bottom). Both HSW and VSW are rectangular signals whose duty factor is controlled to obtain the wipe effect. The required duty factor variation is secured with the aid of a comparator that compares a ramp voltage to a reference voltage set with the wipe control (a slide potentiometer on the front panel of the video mixer). The other picture mixing and effects are obtained by combining different patterns, horizontally as well as vertically.

Block diagram

The waveform generators for the mixing effects are shown to the left in the block

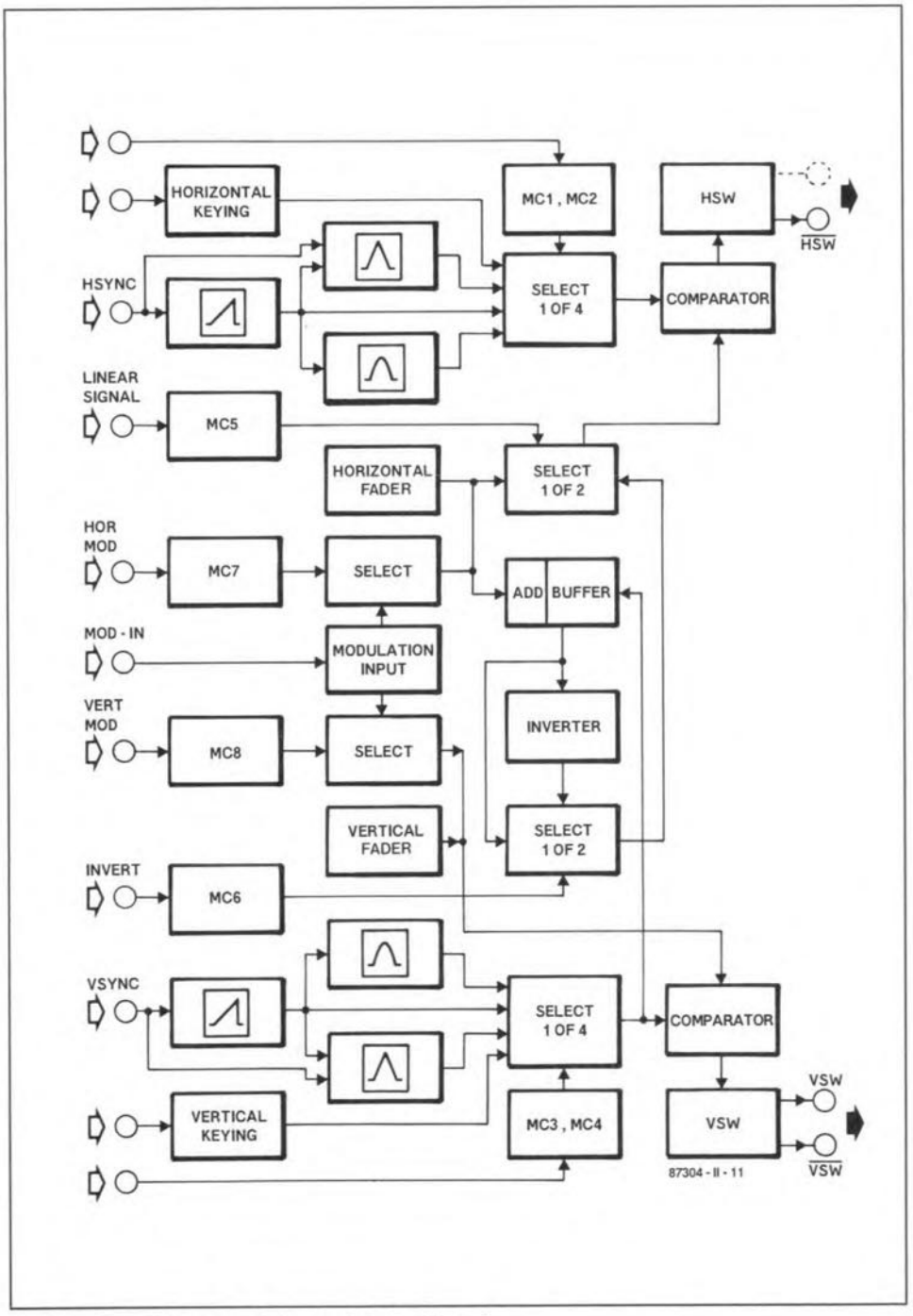


Fig. 6. Block diagram of the modulation board.

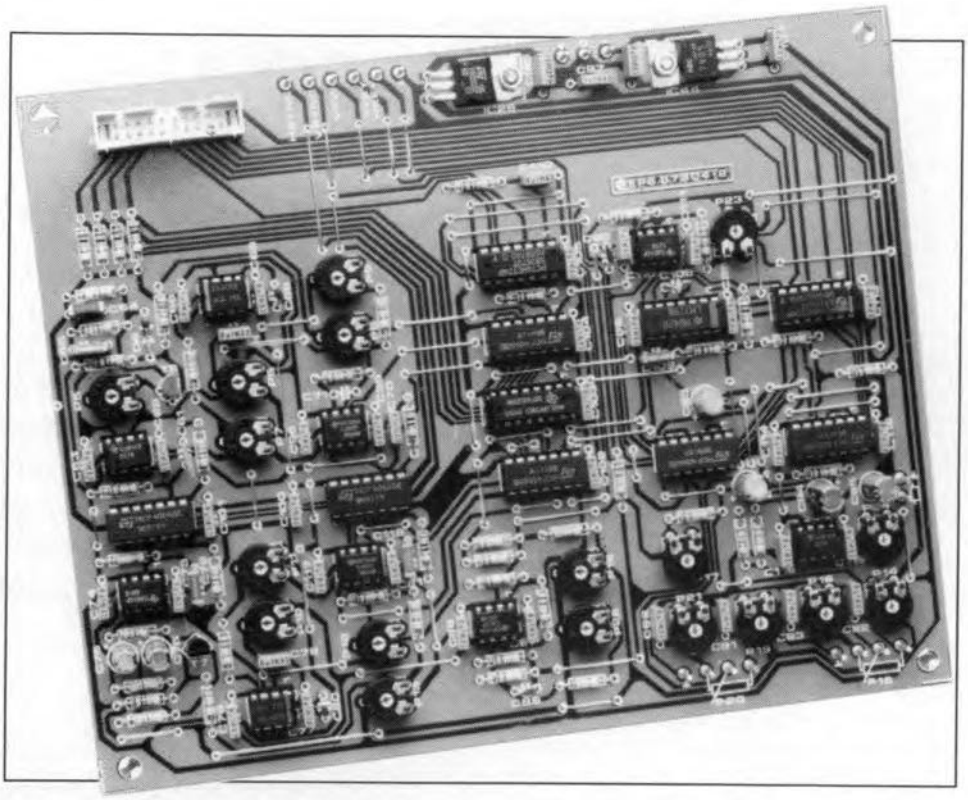
diagram in Fig. 6. Since the same waveforms are in principle required horizontally and vertically (only the frequency is different), almost identical generators are used. In both cases, the waveforms are synchronized with the video signal. The parabola- and triangle waveforms are derived from the ramp voltage. All three waveforms are applied to comparators via electronic switches. Depending on their function, the comparators supply either a horizontal (HSW) or a vertical (VSW) switching signal.

A separate modulation input allows additional control over the selected effect. The modulation signal applied to this input may be synchronous or non-synchronous in relation to the picture. Depending on the available video material and the applied waveform, remarkable and sometimes quite unpredictable effects may be obtained in addition to the ones normally provided by the video mixer.

The horizontal and vertical keying inputs, finally, enable 'home-made' patterns to be added to the picture.

A buffer and an inverter feed the selected vertical waveform to the horizontal comparator, which compares it to the waveforms generated in synchronism with the horizontal line pulses. The inverter may be switched on and off by a control on the keyboard. Depending on the levels applied to the comparator, an HSW signal is supplied that switches between two video sources at a particular instant in the picture line. This combination of vertical and horizontal waveforms allows fairly complex mixing effects to be realized.

The vertical waveforms are available in non-inverted as well as inverted form. The selection is made by the user with the aid of a keyboard control, and allows two video signals to be transposed on the screen. Taking the previously mentioned vertical wipe effect as an example, the invert control allows the 'top' and the 'bottom' pictures to change places in the mixed image.



Circuit description

The circuit diagram of the modulation board is given in Fig. 7. The three-stage horizontal waveform generator is shown in the top left hand corner. The almost identical vertical waveform generator is found in the lower left-hand corner. The following description of the operation of these circuits refers to the horizontal waveform generator, IC_{26}-IC_{27}-IC_{28}-IC_{29a}, T_6 and IC_{40}.

The HSYNC signal is applied to the waveform generator to ensure that this is synchronized with each picture line. During the HSYNC pulse, capacitor C_{61} is discharged via N_{47}, so that integrator IC_{26} can start from zero at the end of the pulse. The result of the integration is a line-synchronous ramp voltage at the output of IC_{26}. To produce a triangle voltage, the ramp is first converted into a rectangular wave by comparator IC_{27}, which compares the instantaneous amplitude of the ramp to the reference voltage at the wiper of preset P_6. The rectangular signal so obtained is applied to integrator IC_{28a}, which charges or discharges C_{70} as the output of IC_{27} goes high or low. The result of this second integration is a triangle voltage at the output of the opamp.

The horizontal synchronization pulse, HSYNC, causes the integrator capacitor, C_{70}, to be completely discharged via N_{51} at the start of each picture line. Preset P_6 determines the switching level of the comparator and with it the symmetry of the triangle voltage, while preset P_7 sets the amplitude.

Transistor T_6 converts the triangle voltage applied to its base via preset P_5 into a parabolic voltage, which is subsequently amplified by IC_{28b}. The amplitude and the off-set voltage of the parabolic waveform are adjusted with presets P_8 and P_9 respectively.

The vertical waveforms are obtained in a manner similar to the horizontal ones. However, the frequency is 50 Hz instead of 15,625 Hz, and VSYNC is used to ensure vertical synchronization to the mixed picture.

Demultiplexers IC_{29a} and IC_{29b} together determine the waveform selection for the mixing effects. This selection is accomplished in conjunction with electronic switches N_{52}–N_{55} and N_{56}–N_{59}. Depending on the logic levels on control lines MC1-MC2 (IC_{29a}) and MC3-MC4 (IC_{29b}), either the ramp-, triangle-, parabola- or KEY- signal is used. The selected signal is applied to opamp IC_{34a} for comparing to the voltage at the inverting input which takes either a steady voltage or one of the vertical waveforms.

The signal at the non-inverting input of IC_{34a} is selected by electronic switches N_{61} or N_{63}. To ensure that the effects selection remains in synchronism with the raster, these switches are controlled in complementary fashion by bistable IC_{33b}. The other bistable in the 74HCT74 package, IC_{33a}, functions as a monostable multivibrator. It is clocked with VSYNC and supplies short pulses at its $\overline{Q}$ output. These pulses clock IC_{33b} and time the instant it latches the logic level of control line MC5 connected to its D (data) input. The latched level is subsequently transferred to the Q and $\overline{Q}$ outputs.

The direct voltage supplied by the horizontal FADING control, P_{15}, may be applied to the input of IC_{34a} by switching on N_{63}. The toggling of the $\overline{HSW}$ signal supplied by inverter N_{38} determines the border between the mixed pictures — in other words, the location (or instant) in the picture line at which the switching between the two video sources takes place. Presets P_{14} and P_{16} serve to give potentiometer P_{15} its maximum usable range, i.e., the width of the picture. Capacitor C_{84} allows an alternating voltage to be superimposed on to the direct voltage at the wiper of P_{15}. This alternating voltage is taken from the external effects input and first buffered by IC_{37}. If the external input is not used, the negative terminal of C_{84} is taken to ground by switch N_{66}. This is done to prevent noise being picked up, which would cause interference in the mixed picture.

The modulation signal supplied by IC_{37} is also applied to comparator IC_{34b}, which adds it to the direct voltage supplied by vertical FADING control P_{20}. The selected vertical waveform is applied to the positive input of the comparator. The output signal is VSW or $\overline{VSW}$ which indicates the vertical (raster-synchronous) switching instant.

Series-connected opamps IC_{35a}-IC_{35b}-IC_{36} form a precision inverter or buffer for the vertical effects waveform selected by the user via N_{56} – N_{59}. Presets P_{17}, P_{18} and P_{22} are adjusted to cancel off-set voltages

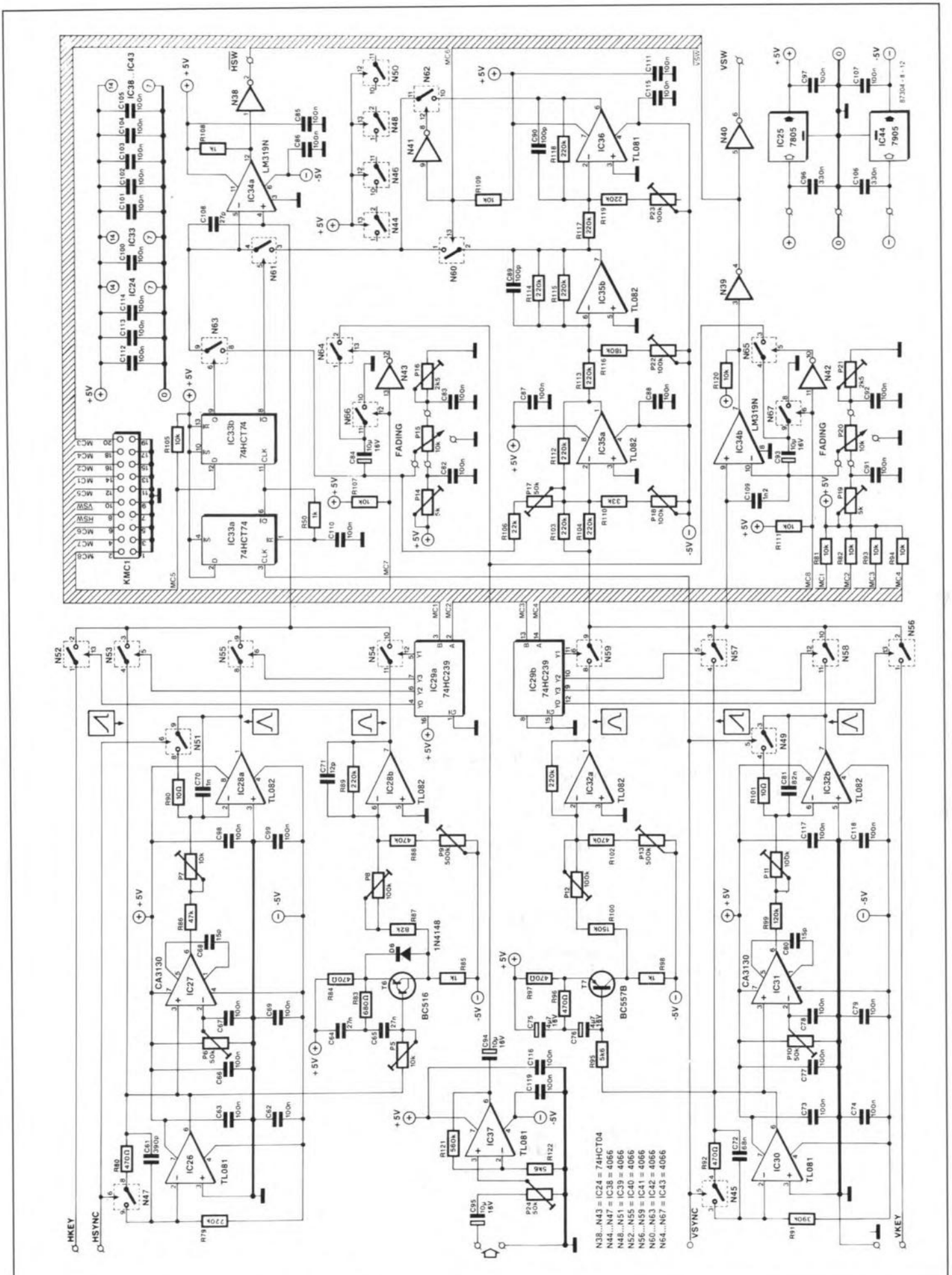


Fig. 7. Circuit diagram of the second unit in the video mixer, the modulation board.

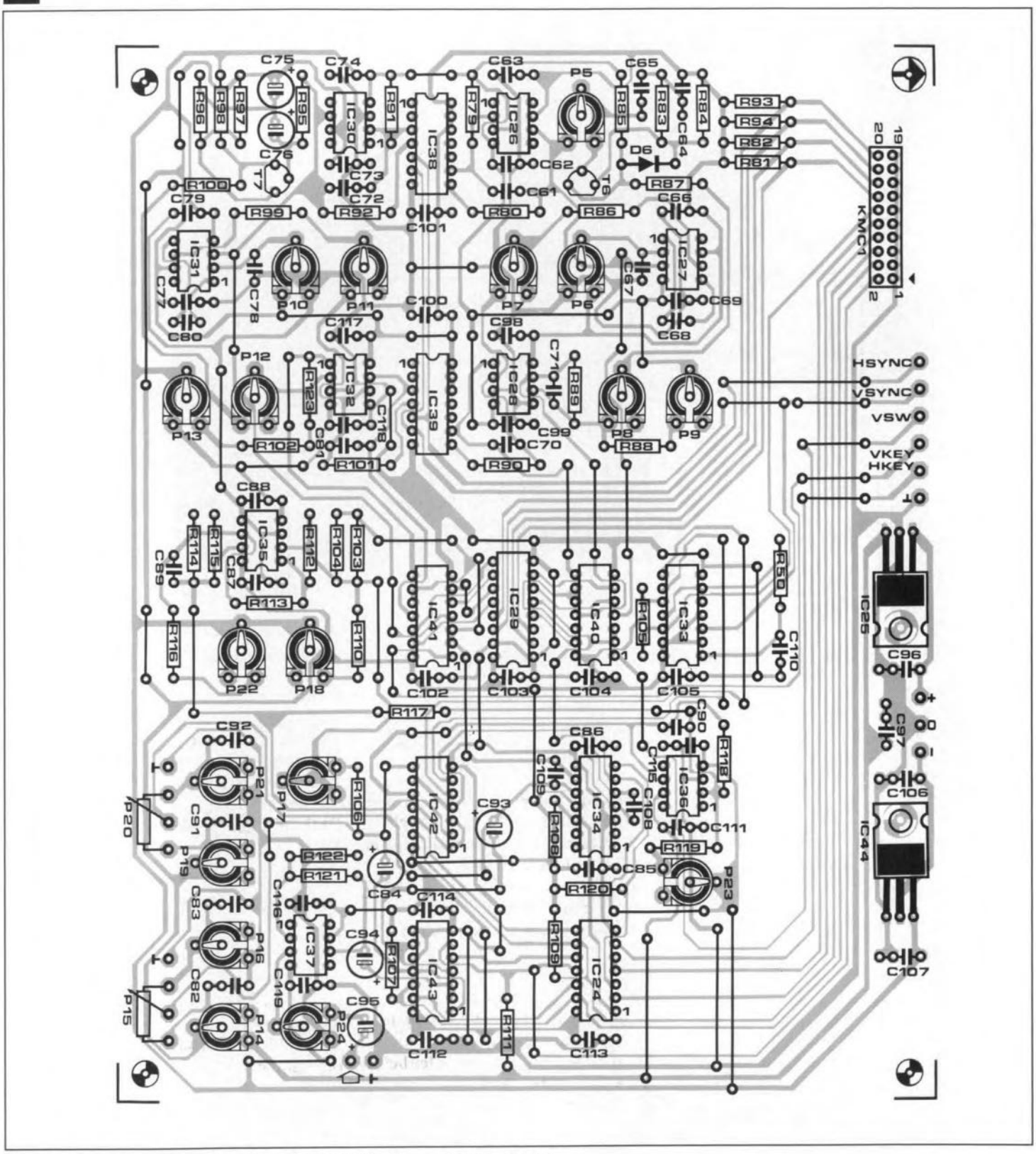


Fig. 8. Component mounting plan of the PCB for the modulation board.

in the three stages. The fairly extensive compensation is required to ensure that the output of IC36 supplies the exact inverse of the signal applied to the external effects input. Control line MC6 is used to select between the inverted and non-inverted version of the vertical effects voltage.

Construction

The single-sided printed-circuit board for the circuit is shown in Fig. 8. Construction should not present problems to the experienced electronics constructor at whom this project is aimed.

Start the construction of the board with fitting all the wire links. Next, mount the solder pins, connectors and IC sockets, if used. Check your work so far and proceed with the passive parts and the single diode. Be sure to observe the polarity of the electrolytic capacitors and the diode. Next, mount the voltage regulators and bolt them straight on to the board — heatsinks are not required. Lastly, plug the ICs in their sockets or, if sockets are not used, solder them direct on to the board. The slide potentiometers are mounted on to the keyboard PCB to be discussed in Part 3 of this article. Set all presets on the modulation board to the centre of their travel.

To be continued next month

Part 1 of this article appeared in the January 1990 issue of *Elektor Electronics*.

Parts list

Resistors:
R79 = 220k
R80;R84;R92;R96;R97 = 470Ω
R81;R82;R93;R94;R105;R107;R109; R111 = 10k
R83 = 680Ω
R50;R85;R98;R108;R120 = 1k0
R86 = 47k
R87 = 82k
R88 = 470k
R89;R103;R104;R112 – R115;R117 – R119; R123 = 220k
R90;R101 = 10Ω
R91 = 390k
R95;R122 = 5k6
R99 = 120k
R100 = 150k
R102 = 470k
R106 = 22k
R110 = 33k
R116 = 180k
R121 = 560k
P5;P7 = 10k preset H
P6;P10;P17 = 50k preset H
P8;P12;P11;P18;P22;P23 = 100k preset H
P9;P13 = 500k preset H
P14;P19 = 5k preset H
P15;P20 = 10k linear slide potentiometer (not on PCB)
P16;P21 = 2k5 preset H
P24 = 50k preset H

Capacitors:
C61 = 390p
C62;C63;C66;C67;C69;C73;C74;C77;C78; C79;C82;C83;C85 – C88;C91;C92; C97 – C105;C107;C111 – C119 = 100n
C64;C65 = 27n
C68;C80 = 15p
C70 = 1n0
C71 = 12p
C72 = 68n
C75;C76 = 4µ7; 16 V radial
C81 = 82n
C84;C93;C94;C95 = 10µ; 16 V radial
C89;C90 = 100p
C96;C106 = 330n
C108 = 27p
C109 = 1n2

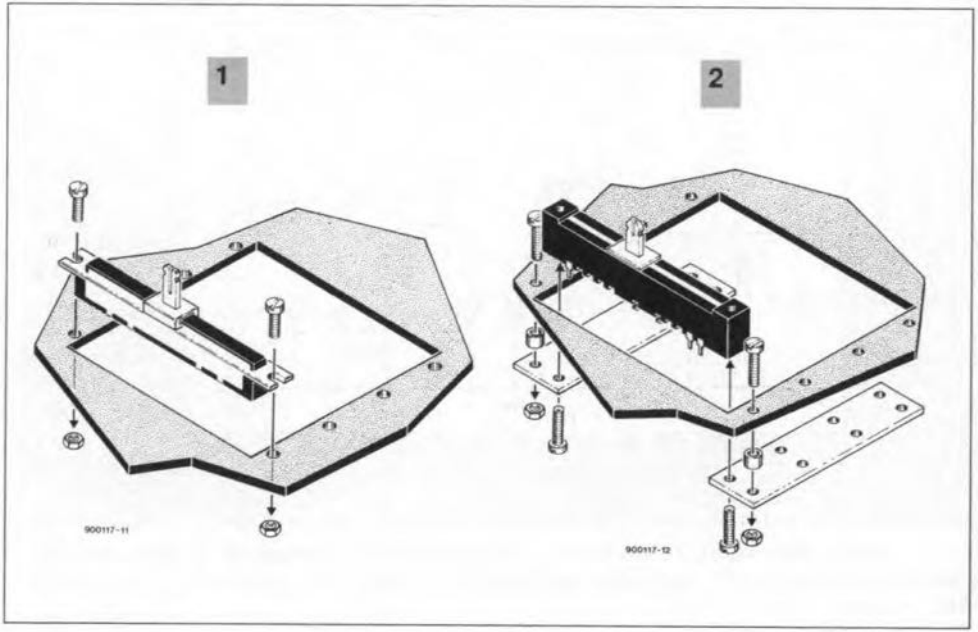
Semiconductors:
D6 = 1N4148
IC24 = 74HCT04
IC25 = 7805
IC26;IC30;IC36;IC37 = TL081
IC27;IC31 = CA3130
IC28;IC32;IC35 = TL082
IC29 = 74HC239
IC33 = 74HCT74
IC34 = LM319N
IC38 – IC43 = 4066
IC44 = 7905
T6 = BC516
T7 = BC557B

Miscellaneous:
KMC1 = 20-way PCB header.
PCB Type 87304-2 (see Readers Services page).

SLIDE POTENTIOMETERS IN THE VIDEO MIXER — AN UPDATE

We understand that the mounting of the slide potentiometers in the video mixer published last year has caused a small difficulty with some constructors.

There appear to be two types of slide potentiometer around, which, although they have the same track length, are mounted differently. In some cases, the type with two mounting lugs (Fig. 1) requires a few washers, or short PCB spacers, to be positioned at the right height above the PCB. The second type (Fig. 2) has two holes through the potentiometer body. To enable this type to be secured to the PCB, mount two small support plates and two spacers at the track side of the PCB, as shown in Fig. 2. The length of the spacers is determined by the required height of the slide potentiometer above the PCB surface. ■



"Video Mixer", *Elektor Electronics* January, February and March 1990.

THE DIGITAL MODEL TRAIN

PART 11 – THE MONITOR UNIT

87291-X

by T. Wigmore

The monitor unit enables the system to read signals from, for instance, the rails. This makes it possible to determine the position of any train at any one instant. Monitor units are indispensable where track sections are protected via a host computer or if the running schedule is controlled by the computer.

The monitor units have eight digital inputs and 62 of them may be used, so that a total of 496 inputs can currently be provided in the system, but this number may be doubled in the future.

Note that the monitor units are not exchangeable with decoder Type s88 from Göppinger. Those decoders have 16 inputs and are interconnected via a 6-way instead of a 5-way connector.

The circuit of the monitor unit is fairly simple as may be seen in Fig. 70. It is based on an 8-bit shift register Type 4014 (IC1) that reads the parallel data at the eight inputs serially. The inputs are not connected direct to the parallel load pins of the register but via eight R-S bistables (IC2 and IC3). This is done in this manner because the serial reading of the monitor units can only take place when the host computer has issued a status request instruction via the RS232 bus.

The bistables in the monitor units also ensure that even very short input signals to the system are acted upon.

Resistors R1–R8 form some protection for the inputs and also, in conjunction with C1–C8, suppress noise pulses.

Self diagnosis

When requesting the status of the monitor units, the system loads the position of the eight bistables in IC2 and IC3 into the shift register, IC1, via a pulse at pin 1 of K1. The bistables are reset automatically by the trailing edge of this pulse. After the data have been loaded, the system reads them serially from the shift register. If more than one monitor unit is used, the shift registers are cascaded so that they may be read as one large shift register.

The number of data bits that the system has to read does, of course, depend on the number of monitor units in use. To prevent time being wasted in reading data of non-connected monitors units, the system carries out a self-diagnosis at power-up and reset, when the number of connected monitor units is determined automatically. All bistables are then reset and read immediately.

The serial input of the last shift register is shorted to the positive supply line via R18, which causes the system to read eight times '1' immediately after the data of the last monitor unit have been received. In this way, the system knows that the last unit has been read.

At each subsequent status request, the system takes account of the number of actually connected units. This self-diagnosis causes a small limitation: on power-up, it is not permissible for all eight inputs of a monitor unit to be active simultaneously, because that would indicate that the unit was the last in the row.

If the status of a non-connected unit is requested, the error LED lights. The number of monitor units may also be determined via a separate RS232 instruction (see Table 8 in last month's instalment).

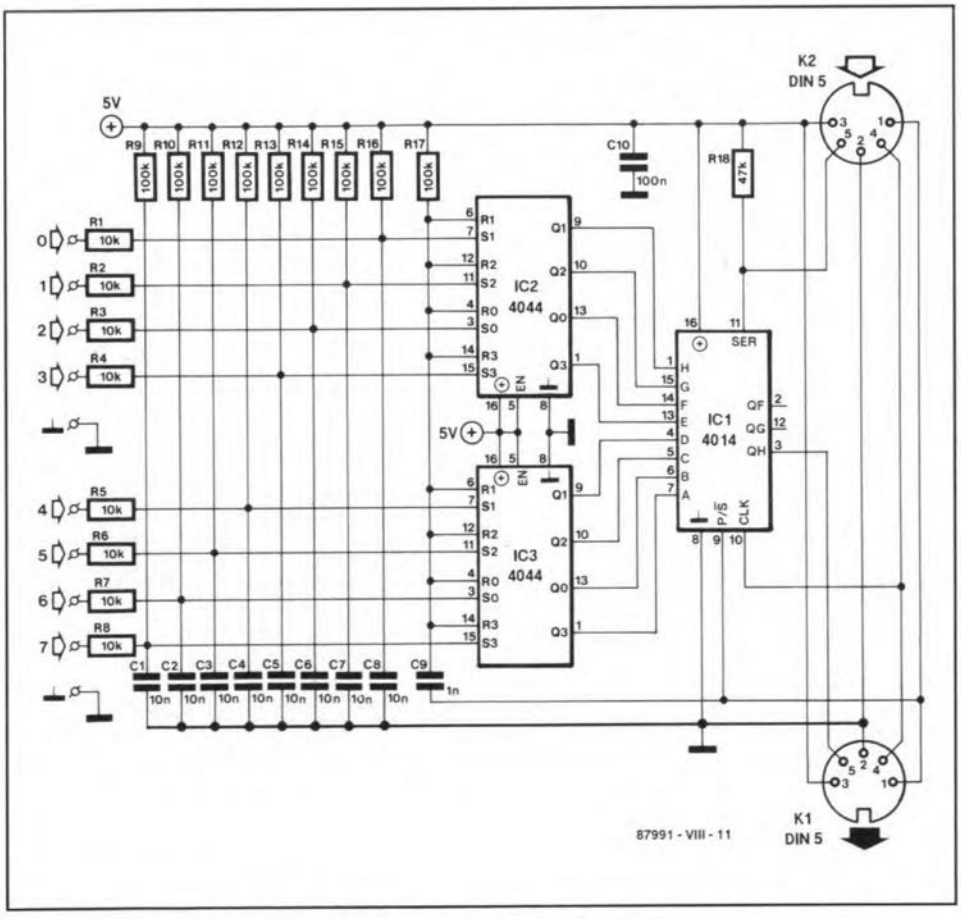


Fig. 70. Circuit diagram of the monitor unit.

Construction

The construction of the monitor units is simple and is best carried out on the PCB shown in Fig. 71.

Before the board is fitted in the enclosure specified in the components list, two corners (indicated on the board) should be cut away as shown in Fig. 73.

The monitor units are interconnected via fairly inexpensive 5-way DIN connectors. If they are going to be used in fixed locations, soldered connections, with or without the use of soldering pins, are, of course, perfectly all right.

Connexions to the inputs may also be

soldered, but if the board is fitted in an enclosure, preference should be given to the use of 2.5 mm plugs and sockets.

Connecting up and actuating the inputs

Monitor units are interconnected via K1 and K2. The arrow shown near these connectors in Fig. 70 must always point to the mother board. If this is not observed, the system will not work, although nothing more disastrous will happen.

All connector pins must be connected to the same numbered pin on the connectors in other units, preferably by the use of ready-made non-twisted, 5-core DIN cable. The total length of cable between the units is of no importance to the correct operation of the system.

In principle, a monitor unit is actuated when the brown wire or rail of the system is connected to earth. For this purpose, two earthing points are provided on the PCB. It is also possible to actuate it by connecting an input to the red wire of the system, but not if the system is in the STOP mode.

Electronic train detection

Signalling to and from locomotives and coaches is often performed with the aid of reed relays. Both from a technical and an aesthetic point of view, this is not a good way of doing it: electronic means are invisible and seldom fail (which can not be said of reed relays).

If Märklin rails are used, M-sections are available in which one rail is isolated from the 'metal gravel' base. This isolated section is simply connected to one of the inputs of a monitor unit.

Where K-rails (which are isolated from each other) are used, a section of one rail may be isolated from that rail by two saw cuts as shown in Fig. 72. The length of this section should be at least as long as the largest wheel base of locomotives and coaches used: this results in one long signal instead of a series of shorter ones. Cut the rail at an angle rather than straight across: in that way trains will have a smoother ride over the section.

Where a standard rail system is used, the detection methods shown in Fig. 74 or Fig. 75 should be used.

The isolated section of rail in Fig. 74 is powered via two anti-parallel-connected diodes. It does not matter whether the diodes are connected to the brown or the red terminal. Rails sections from which no signal is required may be connected direct to the booster unit.

A disadvantage of the method in Fig. 74 is that only powered rolling stock can be detected. If a train loses one or more coaches, these will be 'invisible' to the system. Therefore, the circuit in Fig. 75 may be preferred. The output of the comparator in that circuit is actuated when a relatively high resistance exists between the two rails. By providing coaches with a 10 k resistor as shown in Fig. 76, they can also be detected by monitor units.

Status requests

The status of monitor units can be requsted only via the RS232 interface. After power-up or a reset, one or more groups of two bytes from two successive monitor units (that is, groups of 16 inputs) are sent in response to each status request instruction. This is done in this way to ensure full compatibility with the Märklin Digital System. However, as explained in Part 10, if desired, the monitor units may be made to react individually.

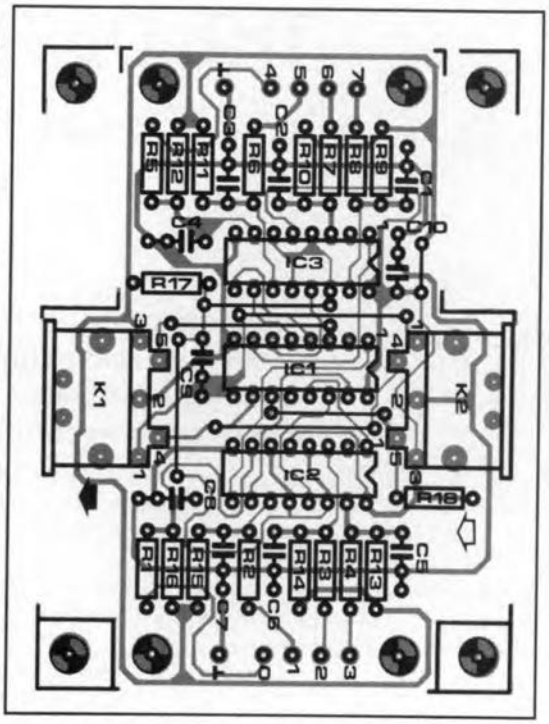


Fig. 71. Printed circuit board for the monitor unit.

COMPONENTS LIST

Resistors:
R1–R8 = 10 k
R9–R17 = 100 k
R18 = 47 k

Capacitors:
C1–C8 = 10 n
C10 = 100 n

Semiconductors:
IC1 = 4014
IC2; IC3 = 4044

Miscellaneous:
K1; K2 = 5-way DIN connector for PCB mounting
Enclosure: OKW Type A9407111
10 pairs of 2.5 mm plugs and sockets (see text)
PCB Type 87291-8

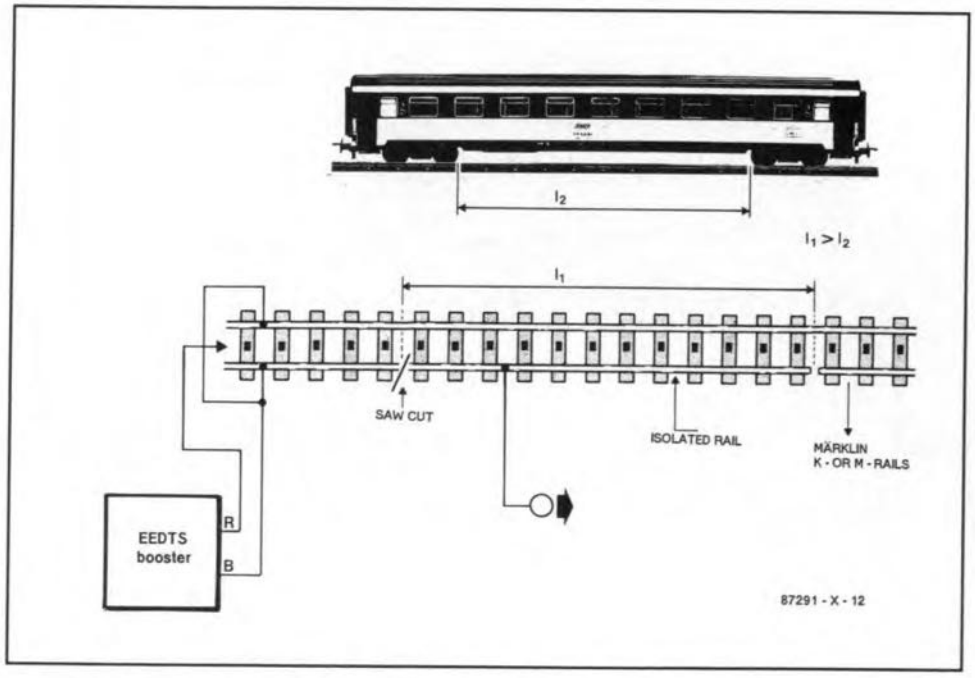


Fig. 72. How to connect an isolated section of the track to a monitor unit (black arrow points to input on monitor unit). In the illustration, use is made of Märklin rails.

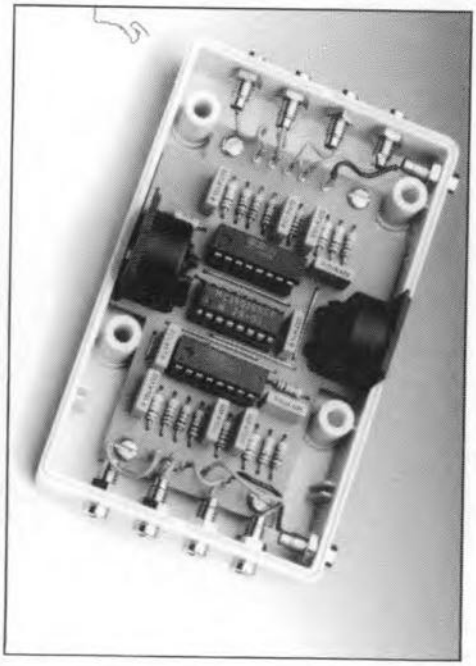


Fig. 73. The finished board fitted in the specified enclosure; note the cut-away corners.

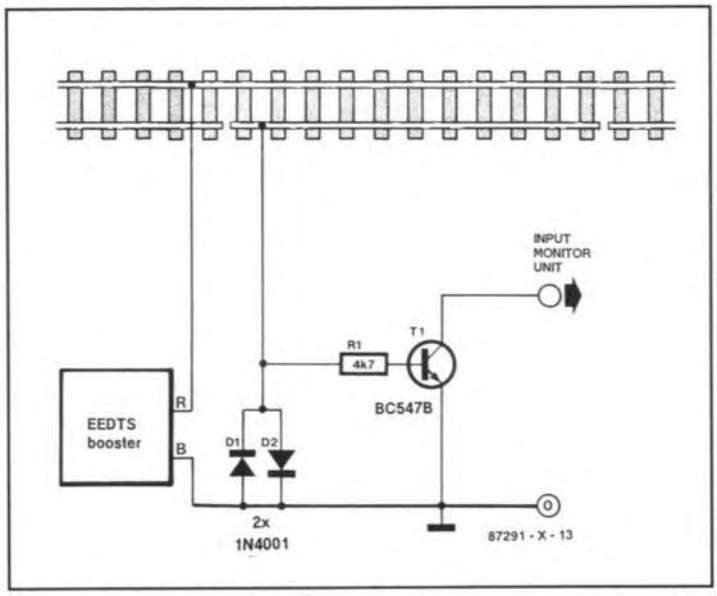


Fig. 74. This circuit for electronic train detection can locate only powered rolling stock (locomotives and coaches with lighting).

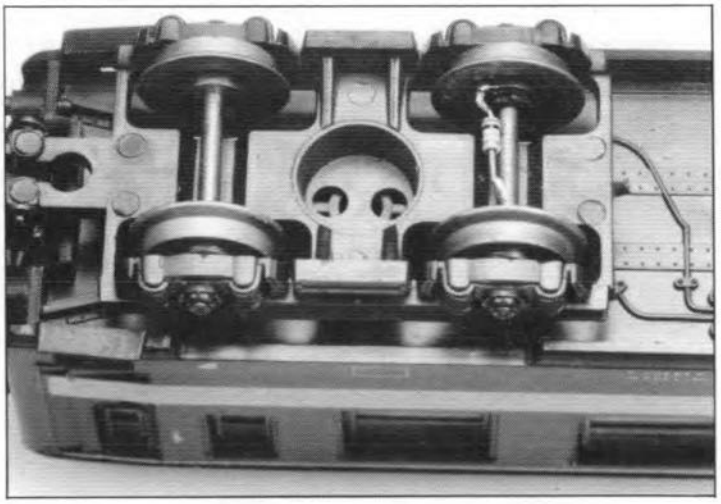


Fig. 76. Providing non-powered rolling stock with a 10 kΩ resistor enables it to be detected with the aid of the circuit in Fig. 75.

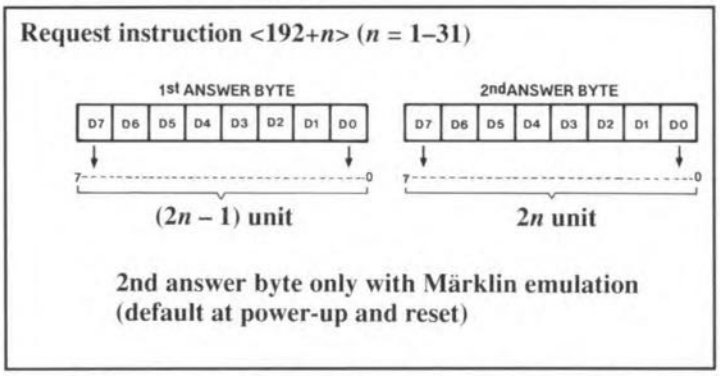


Fig. 77. Composition of bytes sent by the system in response to a status request via the RS232 interface.

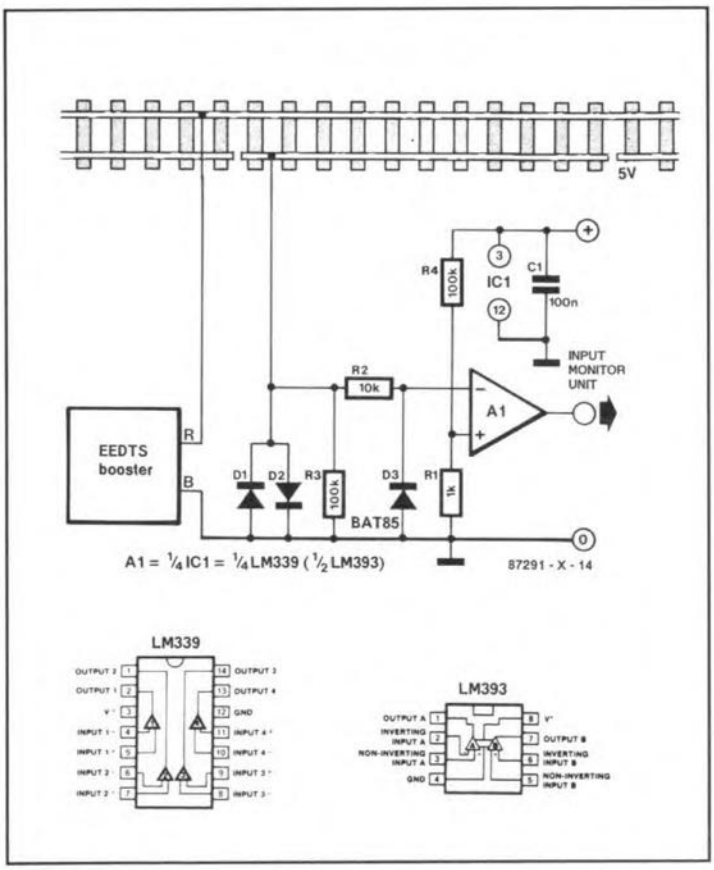


Fig. 75. Circuit of a sensitive detector system that is actuated by a relatively high resistance between the two rails.

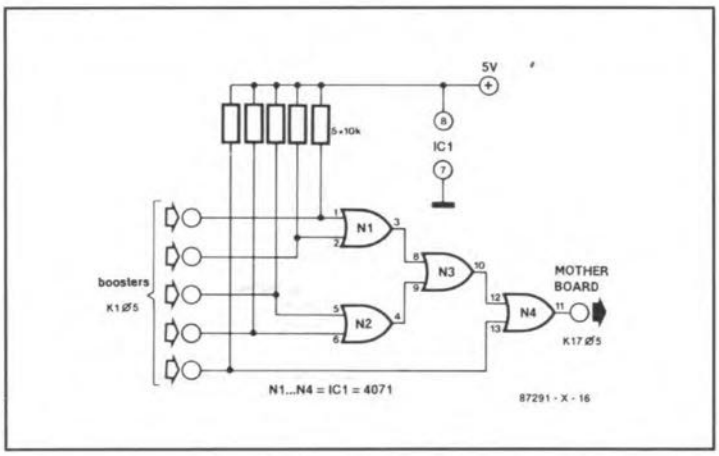


Fig. 78. Additional circuit for obtaining proper overload protection when more than one booster is used.

System miscellany

Locomotive decoders (Part 2).
It appears that loc decoders can be affected by switching instructions intended for points and signals. This can be prevented by increasing the value of R1 from 12 kΩ to 33 kΩ or even 39 kΩ.

Switching decoders (Part 4).
An error has occurred in the circuit diagram and components list. Circuits IC5 and IC6 should be Type ULN2003 and not ULN2001 as stated. The decoder will work with the ULN2001 but not entirely to specification.

Using more than one booster (Part 6).
If the size of the track makes it necessary for several booster units to be used (when each booster powers a section of the track), a small addition is necessary to provide adquate overload protection. The circuit for this is shown in Fig. 78. It is basically a composite OR gate that detects overloads in up to five booster units. If any one booster unit becomes overloaded, the entire system is placed in the STOP mode.

Parts published so far.

Part 1. Märklin system (description).
Part 2. Loc decoder (description).
Part 3. Loc decoder (construction).
Part 4. Universal signal and switching decoder.
Part 5. Description of Elektor Electronics system.
Part 6. Booster unit.
Part 7. Mother board (description).
Part 8. Mother board (construction).
Part 9. Keyboards.
Part 10. RS232 Interface.

INTERMEDIATE PROJECT

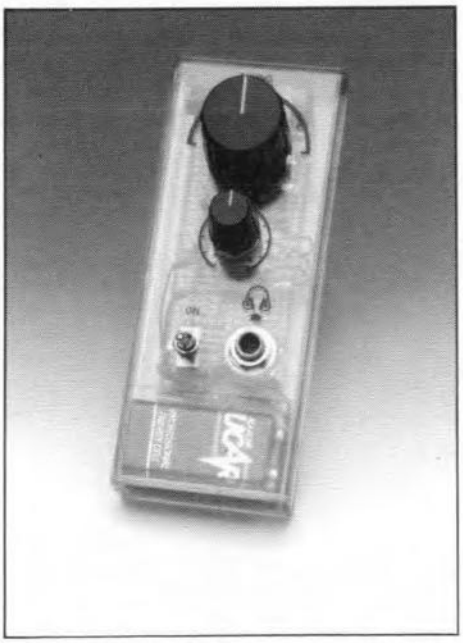
A series of projects for the not-so-experienced constructor. Although each article will describe in detail the operation, use, construction and, where relevant, the underlying theory of the project, constructors will, none the less, require an elementary knowledge of electronic engineering. Each project in the series will be based on inexpensive and commonly available parts.

8. Reflex MW AM receiver

J. Bareford

Radio techniques even at the most fundamental level will continue to fascinate electronics enthusiasts because a handful of components work the miracle of wireless reception. This month we save a once popular circuit from oblivion. The radio fascination catches on with this reflex AM receiver, sporting one tuned circuit for medium-wave reception.

The so-called direct conversion receiver forms the basis of all radio receivers. In its most rudimentary form, it provides an aerial input, a tuned circuit to select the wanted RF signal from many others transmitting in the same band, and a detector to extract the modulation signal (i.e., the information) from the carrier. In a more elaborate design, an RF- and an AF- amplifier may be used before and after the detector respectively. The direct conversion receiver differs from the super-heterodyne receiver in that it does not use frequency conversion of the received RF signal at any stage. Although the direct conversion receiver can not stand comparison with the selectivity of the superhet, it is none the less interesting to build as a first ever electronics project. Again making the comparison with the superheterodyne receiver, the direct conversion type is inexpensive, uncritical, and free of interference effects. What is more, it provides quite acceptable sound quality.



Flashback or start

The circuit diagram of the simplest of receivers, the direct conversion type without RF or AF amplification, is shown in Fig. 1. The combination of an inductor in parallel with a variable capacitor forms a tuned circuit that resonates at the transmit frequency of the station to be received. One side if the tuned circuit is connected to ground, the other side to a small capacitor that takes the RF signals from a long-wire aerial. The detector, a semiconductor diode, is connected to a tap on the inductor. This is done to reduce the loading (damping) effect on the tuned circuit, which would degrade the selectivity. The RF component, i.e., the carrier, is shorted to ground by a capacitor at the anode of the diode. The resulting AF component can be heard in the high-impedance earpiece connected across the capacitor. The one advantage of the circuit in Fig. 1 is that it does not require a supply voltage. The disadvantages, however, are more important: sensitivity is poor, and the AF output signal is too small in many cases.

The addition of a FET (field-effect transistor) and a resistor as shown in Fig. 2 results in a better receiver. The FET provides considerable AF amplification and at the same time, by virtue of its high input impedance, allows the detector to be connected to the 'top' of the tuned circuit. This makes this type of receiver fairly sensitive.

It is definitely worth while to build the circuit of Fig. 2. A few hints: use a wire aerial of at least 5 metres, and connect ground of the circuit to the water supply

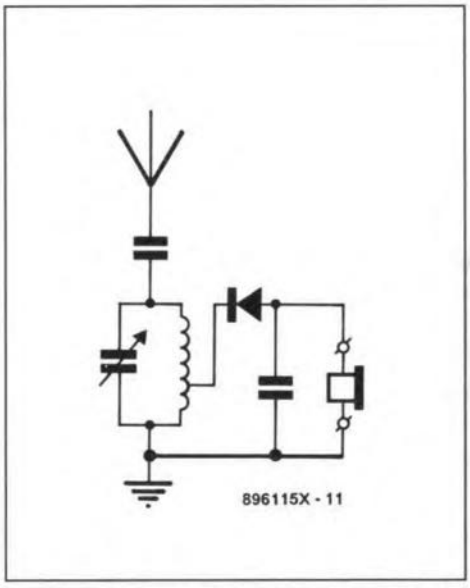


Fig. 1. The one advantage of the diode receiver is that it does not need a power supply. The circuit is, however, useless without a large aerial and an earth connection.

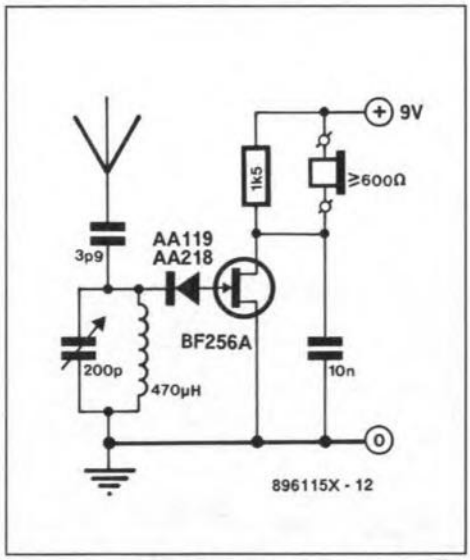


Fig. 2. The amplifier in this modified diode receiver raises the sensitivity of the basic design considerably.

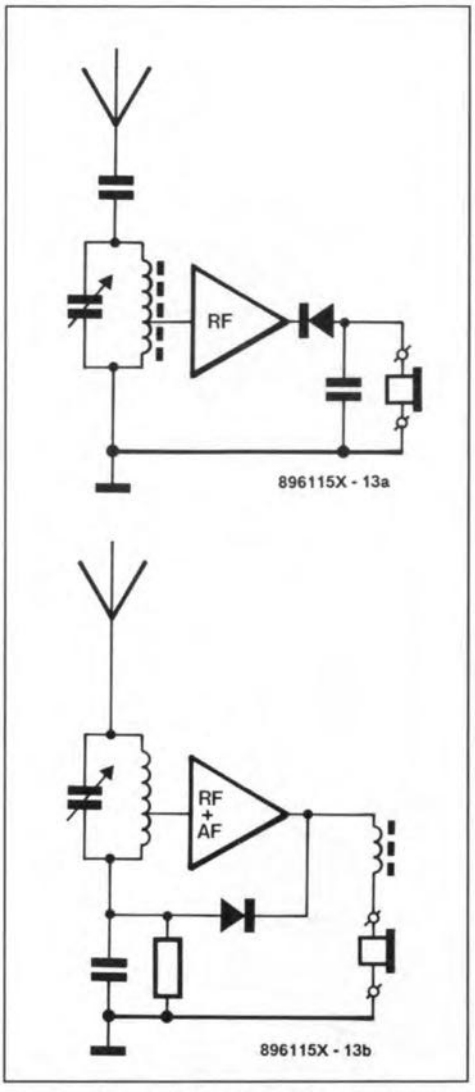


Fig. 3. Extending the direct-conversion receiver with an amplifier for RF signals only (3a) and one that provides gain for RF as well as AF signals (3b).

or the central heating system. The inductor is made by winding 85 turns of 0.2 mm diameter (SWG36) enamelled copper wire on a 10-cm long ferrite rod. The receiver draws about 4 mA from the 9 V battery.

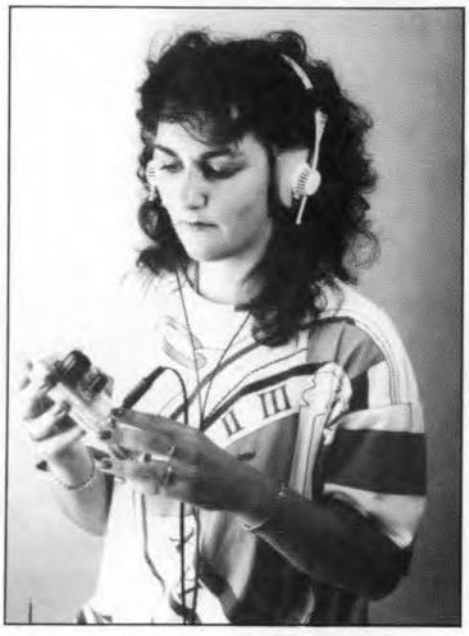
RF amplification

It will be clear that an RF amplifier as drawn in Fig. 3 is required if the receiver in Fig. 2 is to work with a much smaller (shorter) aerial, and without the connection to earth via the water supply or the domestic CH system. Also note that the germanium diode has a threshold voltage of about 200 mV, which makes reception of signals below this level impossible — weaker signals are simply not detected. If the RF amplification is high enough, the tuned circuit may double as an aerial, obviating the long wire. A second tuned circuit, identical to the one already used, may be added to improve the selectivity. A further improvement that requires no extra components is shown in Fig. 3b. A choke is connected to the output of the RF amplifier, and the detector is not connected to the headphones, but fed back to the 'cold' side of the tuned circuit. The result of this configuration is that the amplified RF signal is 'forced' towards the detector because it is blocked by the choke. After detection, it is applied to the input of the amplifier. Since the choke does not present a high reactance to AF frequencies, the amplifier raises the demodulated signal to a level suitable for driving earphones. In other words: RF and AF amplification are provided by a single amplifier. This forms the principle of the reflex receiver.

Enter two MOSFETs

Transistors are available today that improve the performance of the good old reflex receiver considerably. Figure 4 shows the circuit diagram of a receiver based on the reflex principle and developed as a result of many experiments. Dual-gate MOSFETs Type BF981 are used. One functions as an AF amplifier that obviates passive components, and the other as an AF/RF amplifier with very high input impedance.

The heart of the receiver is formed by T1. Resistors R3 and R5 provide the gate-2 bias voltage, which is decoupled by C4. Capacitor C5 similarly decouples the drain voltage. The tuned circuit of the receiver is formed by L1-C1. The inductor is wound on a small ferrite rod which forms the aerial. The RF signal at the 'top' of the tuned circuit is fed to gate-1 of the MOSFET via C1. The extremely high gate impedance of the transistor eliminates all likelihood of damping, and obviates a tap connection or a coupled winding. All this simplifies the construction of the inductor and increases the sensitivity of the receiver because at the same (high) load resistance, the voltage at the top of the tuned



circuit is higher than at a tap towards the earthy side. The RF signal amplified by T1 is blocked by L2 and consequently arrives at detector D1-D2-C3-R2 via coupling capacitor C3. The detector also functions as a voltage doubler circuit. Resistor R1 feeds the rectified signal back to gate-1 of the MOSFET, which functions as an AF amplifier. The amplified AF signal passes through L2 and is coupled out via C7 to the volume control, P1. Transistor T2 raises the AF signal to a level suitable for driving lightweight headphones.

Compact

The low number of components and the use of a small ferrite rod enables the reflex

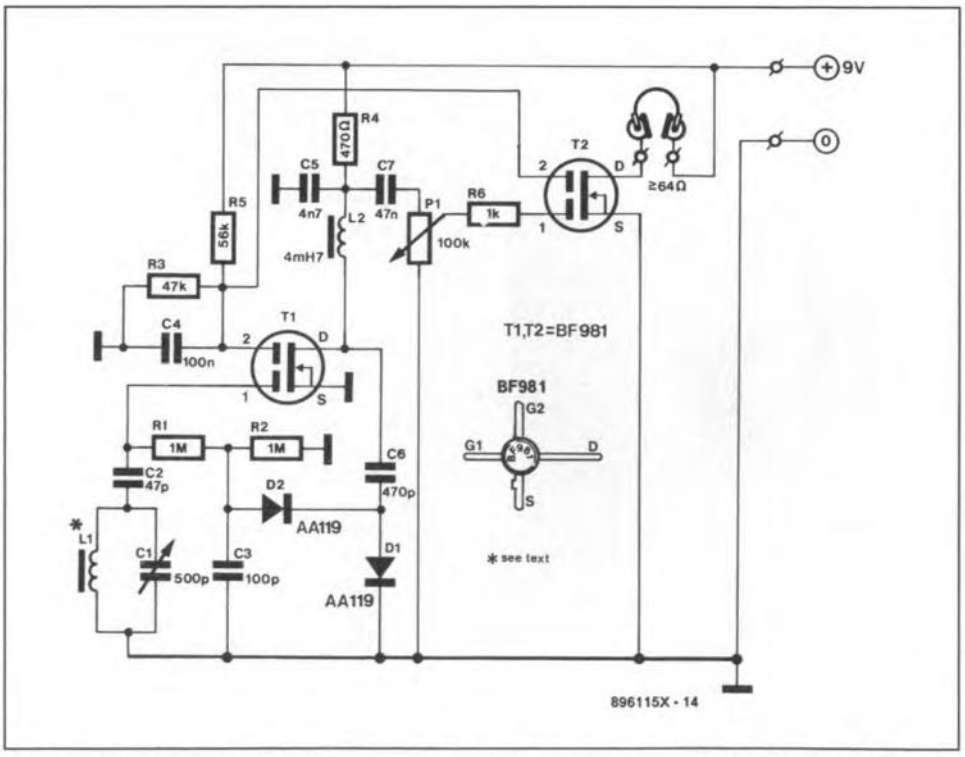


Fig. 4. Circuit diagram of the reflex receiver based on dual-gate MOSFETs. The *L-C* tuned circuit at the input doubles as a compact aerial for medium-wave reception.

receiver and the 9 V battery to be built into a miniature enclosure of the size of, say, two match boxes.

If you consider size less important and at the same time want to go round constructional problems, build the circuit on Universal Prototyping Board Size-1 as shown in Fig. 5. Pay attention to the orientation of the MOSFETs: when in doubt look at the pinning given in the circuit diagram (transistor viewed from the top). Choke L_2 is a ready-made type. The aerial is made from 70 turns of 0.2 mm diameter (36SWG) enamelled copper wire wound on a 4-cm long, 10-mm diameter ferrite rod. The rod is secured on to the PCB with the aid of plastic ties as shown in the photograph. The two diodes may be replaced by almost any other small-signal germanium type such as the OA90 or OA95. Do not use silicon types: their threshold voltage is too high for this application.

The receiver is connected to a pair of headphones with a minimum impedance of 64 Ω. This perhaps less usual value is simple to achieve by connecting the two 32 Ω earpieces of the headphones in series.

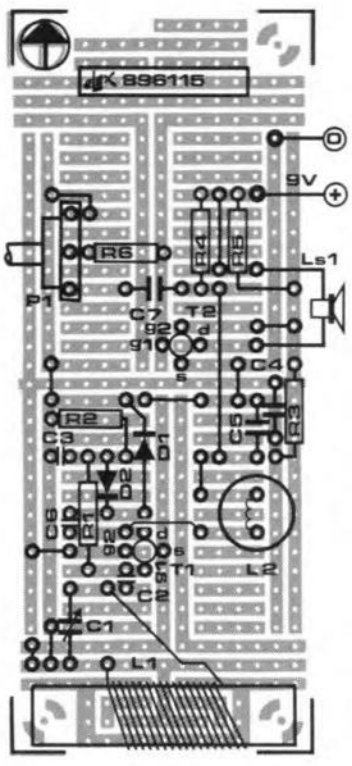


Fig. 5. Suggested construction of the receiver on ready-made PCB Type UPBS-1.

Parts list

Resistors:
R_1;R_2 = 1M0
R_3 = 47k
R_4 = 470Ω
R_5 = 56k
R_6 = 1k0
P_1 = 100k logarithmic potentiometer

Capacitors:
C_1 = 500p mica foil tuning capacitor *
C_2 = 47p
C_3 = 100p
C_4 = 100n
C_5 = 4n7
C_6 = 470p
C_7 = 47n

Semiconductors:
D_1;D_2 = AA119
T_1;T_2 = BF981 *

Inductors:
L_1 = wound on ferrite rod * (see text)
L_2 = 4mH7 choke, e.g., Toko 181LY-472 *

Miscellaneous:
S_1 = miniature on/off switch.
Headphones; impedance ≥ 64Ω (2×32Ω)
PCB Type UPBS-1 (see Readers Services page).

* Suggested supplier: Cirkit, Park Lane, BROXBOURNE EN10 7NQ. Telephone (0992) 441306. Fax (0992) 464457.

CORRECTIONS

Hard disk monitor

December 1989, p. 54
The parts list is not in agreement with the circuit diagram, and should be modified to read:

$R_1 - R_7$;R_{11};$R_{13} - R_{16}$;R_{20} = 100k
C_1–C_{11} = 22n

Simple transmission line experiments

September 1989, p. 38
The value of R_2 in the experiment should be 225 Ω, not 43 Ω.

Logic analyser with Atari ST

October 1989, p. 30
Please add to the parts list:
R_3;R_4;$R_5 - R_{12}$ = 100k
C_6 = 100n
The control program (ESS111) is suitable for **monochrome** systems only.

LF/HF signal tracer

December 1989, p. 22
The resistor next to preset P_3 on the printed-circuit board should be labelled R_{23}, not R_{36}.

I/O extension for Archimedes

November 1989, p. 14-15
The parts list should be modified to read:
IC_3 = 6522-2
The circuit diagram in Fig. 2 contains an error: R_4 should be connected between ground and the +input of IC_1. The printed-circuit board is all right and requires no modification.

Intruder alarm

November 1989, p. 45-47
The references to C_3 in lines 6 and 7 of the last full paragraph on page 45 should read C_1.

The reference to R_5 in the third paragraph under **Alarm sensing** should read R_9.

The first full sentence in the centre column on page 47 should read

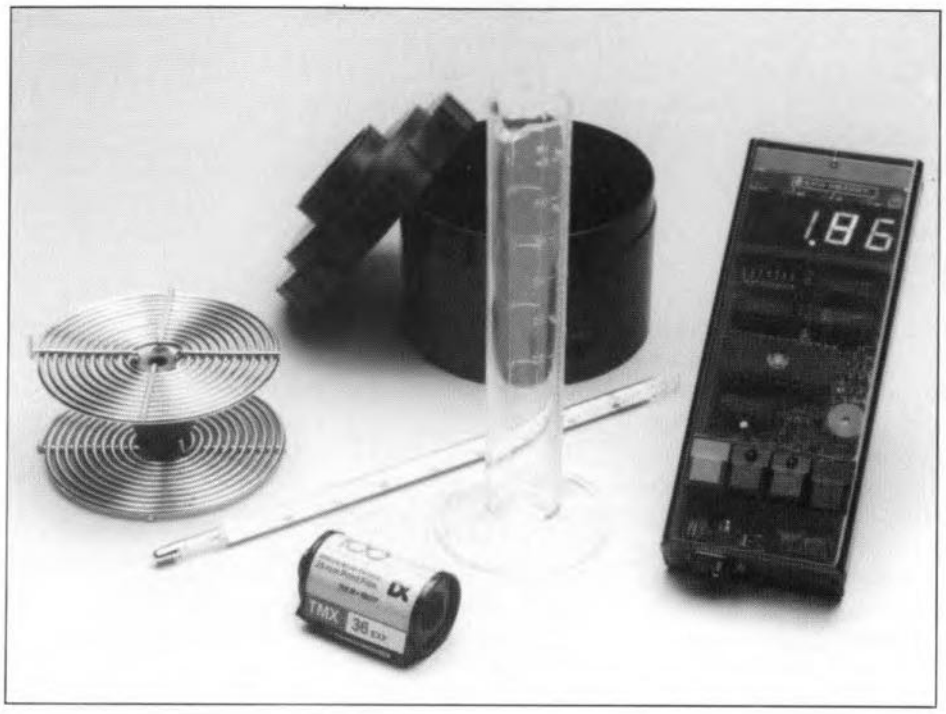
'Two assurance bleeps are generated: one at the instant of switch-on, and one as the exit door is opened for departure before the end of the 15-s switch-on delay.'

In the circuit diagram, Fig. 2, the diode across Bz_1 should be numbered D_{10}, not D_{12}. Capacitor C_2 is missing: it is an 10 µF electrolytic type connected between the +12 V and ground rail. Finally, the inset text 'D1...D8 = 1N4148' should read D1, D2,D3,D5,D6,D7,D8,D10,D12=1N4148.

3½-digit SMD voltmeter

November 1989, p. 37-41
The obsolete half-digit LED display Type HD1108 from Siemens may be replaced by Telefunken's Type D29xPK, where 'x' indicates the colour: 0 for red, 1 for amber, 2 for green and 3 for yellow. These displays are also available under new type indications as TDSR3120, TDSO3120, TDSG3120 and TDSY3120 respectively. Telefunken also manufactures equivalents for the HD1105: the type numbers are TDSR3150, TDSO3150, TDSG3150 and TDSY3150.
Distributor information on Telefunken components from **AEG (UK) Ltd. • 217 Bath Road • SLOUGH SL1 4AW. Telephone: (0753) 872101. Fax: (0753) 872176.**

DARK-ROOM CLOCK



A. Rigby

Timing is an essential factor in any dark-room. Keeping a constant eye on the clock while the photograph is being developed, however, is a nuisance, and makes it impossible to attend to other activities. The low-cost timer described here can be programmed to give accurately timed audible signals as a reminder to flip the development tank, add the fixative, remove PE paper, and so on.

The quality of photographic reproductions can be kept constant only if the development tanks are flipped, and baths are changed or stirred in good time. A timing error of a couple of seconds can be tolerated in some cases, but longer delays, caused by other activities in the dark-room, may result in an unusable print.

The present clock offers a number of selectable alarm functions and a maximum time lapse of 30 minutes, which is ample for most dark-room activities. The clock is a compact unit to prevent it taking up too much space in the dark-room.

The block schematic diagram in Fig. 1 shows the general structure of the dark-room clock. The 2 Hz clock generator affords simple selection of a number of differently timed alarm sounds. The 2 Hz clock signal is applied to a binary counter whose (non-used) least-significant output bit counts half-seconds. The 11 other output lines of the counter are connected to the address inputs of an EPROM that converts the 11-bit counter value into control signals for a 4-digit multiplexed LED display. This function requires 7 of the 8

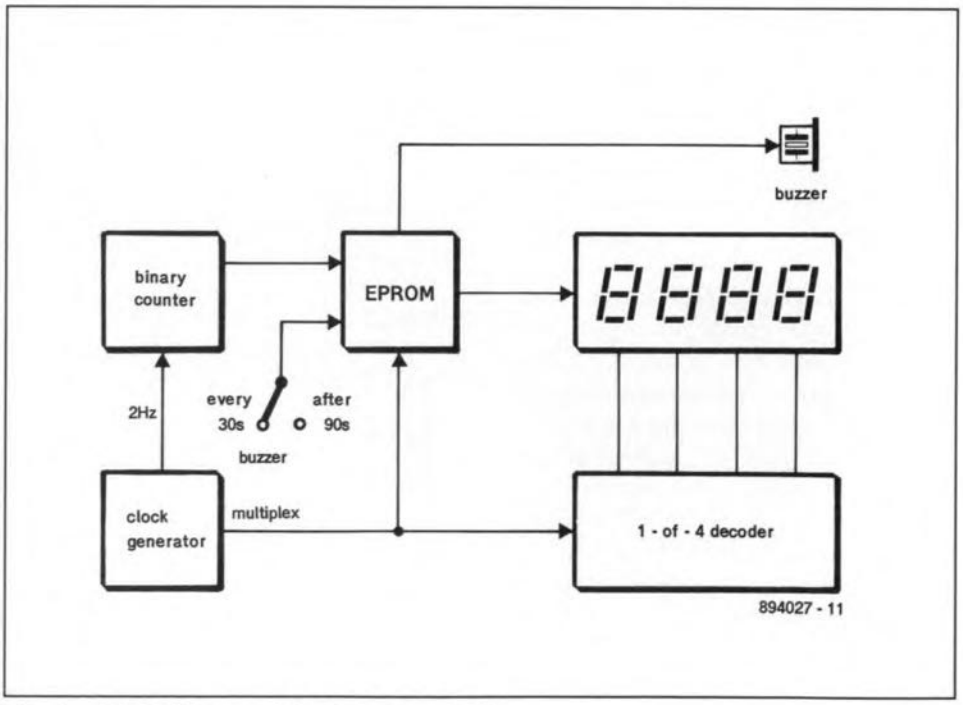


Fig. 1. Block diagram of the dark-room clock.

EPROM data outputs. The remaining bit is used for the control of an alarm sounder.

EPROM as a decoder

The EPROM used in the dark-room clock is essentially a programmable logic device (PLD), whose combined functions allow the remainder of the circuit to be kept relatively simple. The 8 output lines of the EPROM are used for display segment control and sounder control. Each address location in the EPROM is programmed to supply a bit pattern that determines whether a display segment is lit or not, and whether the sounder is actuated or not. Table 1 lists the bit patterns for numbers 0 through 9. The sounder is actuated by adding 80H (bit 7 goes high) to the values shown. Table 2 shows how these bit patterns are stored in the EPROM, and illustrates the functions of its address inputs, which, given the application, may also be considered decoder inputs.

The most-significant (MS) address input, A13, divides the EPROM address space into two blocks. One of these ensures that the sounder is actuated every 30 seconds, which is useful during the development of films. The other block is pro-

Bit	D6	D5	D4	D3	D2	D1	D0	HEX
segment	g	f	e	d	c	b	a	
read-out								
none	0	0	0	0	0	0	0	00
0	1	1	1	1	1	1	1	3F
1	0	0	0	0	1	1	0	06
2	1	0	1	1	0	1	1	5B
3	1	0	0	1	1	1	1	4F
4	1	1	0	0	1	1	0	66
5	1	1	0	1	1	0	1	6D
6	1	1	1	1	1	0	1	7D
7	0	0	0	0	1	1	1	07
8	1	1	1	1	1	1	1	7F
9	1	1	0	1	1	1	1	6F

D7 = "1": buzzer on. D7 = "0": buzzer off

Table 1. The databits loaded into the EPROM control the display segments and the time-lapse buzzer.

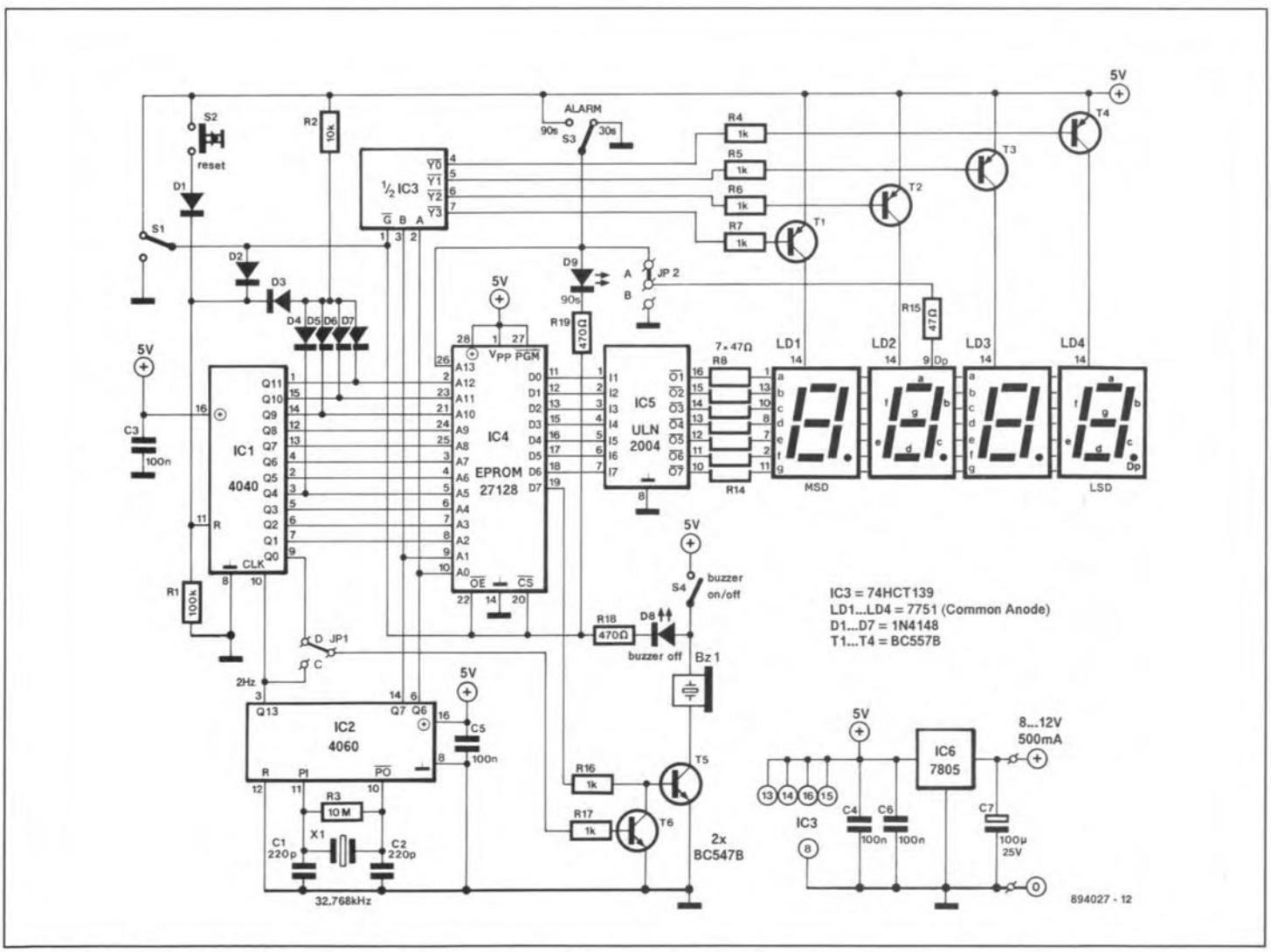


Fig. 2. Circuit diagram of the dark-room clock. The heart of the circuit is formed by EPROM IC4.

buzzer	lapsed time	digit	address (hex)	data (hex)
every 30 s	0 minutes, 0 seconds	seconds (units) seconds (tens) minutes (units) minutes (tens)	0000 0001 0002 0003	BF BF BF 80
	0 minutes, 1 second	seconds (units) seconds (tens) minutes (units) minutes (tens)	0004 0005 0006 0007	06 3F 3F 00
	17 minutes, 30 seconds	seconds (units) seconds (tens) minutes (units) minutes (tens)	1068 1069 106A 106B	BF CF 87 86
	29 minutes, 58 seconds	seconds (units) seconds (tens) minutes (units) minutes (tens)	1C18 1C19 1C1A 1C1B	7F 6D 6F 5B
	29 minutes, 59 seconds	seconds (units) seconds (tens) minutes (units) minutes (tens)	1C1C 1C1D 1C1E 1C1F	6F 6D 6F 5B
	248 bytes, not programmed		1C20 ⋮ 1FFF	FF ⋮ FF
after 90 s	0 minutes, 0 seconds	seconds (units) seconds (tens) minutes (units) minutes (tens)	2000 2001 2003 2004	BF BF BF 80
	1 minute, 30 seconds	seconds (units) seconds (tens) minutes (units) minutes (tens)	2168 2169 216A 216B	BF CF 86 80
	29 minutes, 59 seconds	seconds (units) seconds (tens) minutes (units) minutes (tens)	3C1C 3C1D 3C1E 3C1F	6F 6D 6F 5B
	248 bytes, not programmed		3C10 ⋮ 3FFF	FF ⋮ FF
A13	A12.....A2	A1, A0		

Table 1. EPROM organization.

grammed to supply a single alarm after 90 seconds, which is useful for the development of PE (*poly-ethylene*) paper. The development time of PE paper is normally stated as about 60 seconds, but 90 seconds is often found to give better darkening and quality of reproduction.

The time in seconds is applied as an 11-bit binary number to EPROM inputs A2 through A12. This arrangement results in four bytes that hold the segment patterns for the LED displays to be selected every second. Address lines A0 and A1 are driven by two signals that control the multiplexing of the 4 displays. Summarizing the above, the EPROM functions as a circuit that decodes binary time information into a multiplexed 7-segment control signal.

The circuit

The circuit diagram of Fig. 2 shows that the clock generator is formed by IC_2, a Type 4060 14-bit counter with on-board oscillator. The oscillator signal is divided by 2^{14}, so that output Q13 supplies a 2 Hz signal. Outputs Q6 and Q7 supply the multiplex signals that cause each display to be turned on and off at a rate of 128 times per second.

The 2 Hz signal is fed to the clock input of binary counter IC_1. This 12-bit counter/divider counts the seconds lapsed since the circuit was started. The use of binary counting in combination with an EPROM allows such a simple seconds counter to be used — the perhaps more conventional alternative would have required at least 8 standard ICs, or two or three specialized ones. The EPROM used in this circuit is available ready-programmed.

The reset circuit of IC_1 has 3 inputs with an OR function provided by D_1-D_2-D_3. The counter is cleared (reset to zero) either when RESET key S_2 is actuated (D_1), or when the circuit is switched to the stand-by mode by S_1 (D_2), or when 1800 seconds have lapsed since the last reset (D_3). The last function is realized with the aid of D_4–D_7 that reset the counter within a few nanoseconds after it reaches state 1800 (11100001000_2).

The lapsed time is passed to EPROM IC_4, whose function has been detailed earlier. The decoded and multiplexed 7-segment signals on datalines D0–D6 are buffered by Darlington array IC_5 before being applied to the cathodes of the LED displays.

The signal on EPROM dataline D7 controls sounder Bz_1 via driver T_5. The sound of the piezoelectric buzzer is made a little less disagreeable by interrupting it with the aid of T_6. A wire link, JP_1, is fitted to provide 3 sounder options:

- position 'C' for two pips of a quarter of a second each;
- position 'D' for a single pip of half a second;
- no wire link for a single pip of one second.

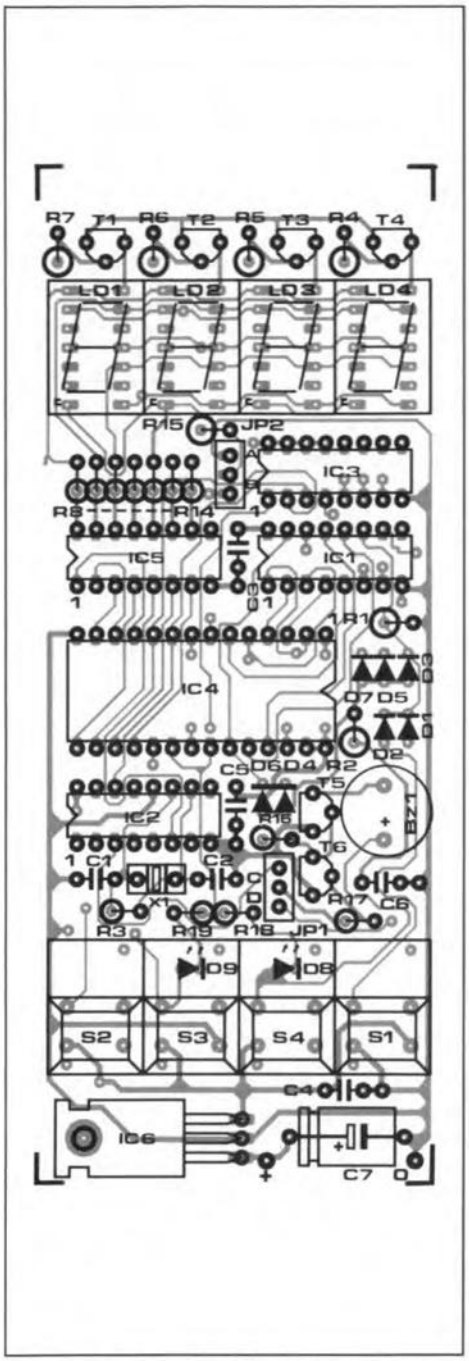


Fig. 3. Printed-circuit board for the dark-room clock. The board is double-sided, but not through-plated.

Parts list

Resistors:
R1 = 100k
R2 = 10k
R3 = 10M
R4 – R7;R16;R17 = 1k0
R8 – R15 = 47Ω
R18;R19 = 470Ω

Capacitors:
C1;C2 = 220p
C3 – C6 = 100n
C7 = 100µ; 25 V

Semiconductors:
D1 – D7 = 1N4148
D8;D9 = LED; red; 3 mm
LD1 – LD4 = 7751 (common anode)
T1 – T4 = BC557B
T5;T6 = BC547B
IC1 = 4040
IC2 = 4060
IC3 = 74HCT139
IC4 = EPROM 27128. Available ready-programmed under order number ESS 583 (see Readers Services page)
IC5 = ULN2004
IC6 = 7805

Miscellaneous:
S1 = locking SPDT switch with black key cap. ITW Type 61-2010400+.
S2 = SPDT switch with red key cap. ITW Type 61-1010000+.
S3;S4 = locking SPDT switch with integral LED and black key cap. ITW Type 61-2030401+.
X1 = quartz crystal 32.768 kHz.
PCB Type 894027 (see Readers Services page).
Enclosure: Heddic Type 222*.

+ ITW Switches • Division of ITW Limited • Norway Road • Hilsea • PORTSMOUTH PO3 5HT. Telephone: (0705) 694971.

* Emtek Electronic Products Limited • Unit 19a • Industrial Estate • Stanton • BURY ST. EDMUNDS IP31 2AR. Telephone: (0359) 511155.

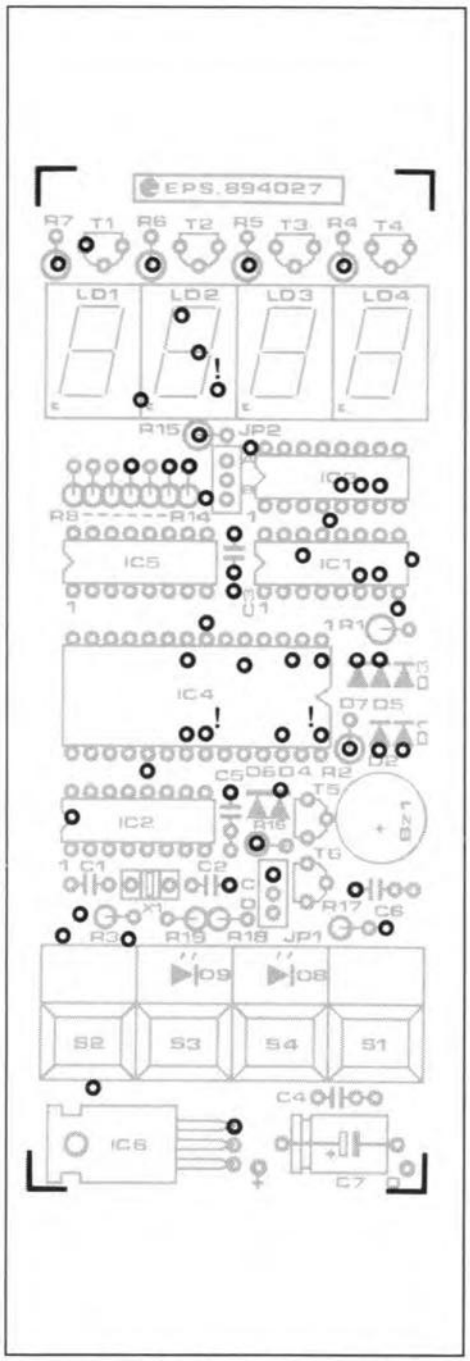


Fig. 4. Showing the locations of the holes that must be through-plated before any components can be fitted.

For reasons of safety, and to keep its overall cost down, the dark-room clock is powered by a mains adapter with a direct, unregulated output voltage of 8–12 V. Regulator IC6 reduces this voltage to 5 V. A real on/off switch is not provided. Rather, the circuit is switched to stand-by with S1. The counter is reset to zero, the displays and LEDs are turned off, and the EPROM is switched to its low-power standby mode. The clock is not re-actuated until S1 is switched on again.

Construction

The dark-room clock is built on the double-sided, not through-plated, printed-circuit board shown in Fig. 3. This board is available ready-made.

Figure 4 shows the locations of the holes that must be through-contacted by inserting a short piece of wire, and soldering it at both the component side *and* the track side of the board. This arrangement obviates having to solder the ICs direct on to the board, although this is perfectly permissible in this case. Note that the white overlay print must be removed at the component side before the spots can be soldered properly.

The 3 exclamation marks shown in Fig. 4 indicate PCB design errors that are, fortunately, simple to correct. The holes near pins 22 and 28, towards the 'IC4' mark on the overlay, must be connected to the associated holes that receive the IC pins (or IC socket pins) *at both sides of the PCB*. In the case of pin 22, the missing connection is at the track (EPS) side of the board: a little extra solder tin applied during the mounting of IC4 will bridge the gap between the spots. The extra connection for pin 28 is made at the component side of the board with the aid of a piece of thin wire that connects the holes. Before fitting this wire, remove the white overlay printed on the hole for IC pin 28. Insert the tip of a sharp pencil in the hole to ensure that it remains open when the wire is soldered to the spot.

Make the connection between R15 and LD2 with a short length of insulated wire fitted at the track (EPS) side of the board. A track is provided at the component side, but this makes fitting LD2 rather difficult if the centre pin in the right-hand row of the display is to function as a through contact.

The fitting of the remainder of the components should not present problems.

If the Heddic Type 222 enclosure stated in the Parts List is used, the switches must be raised by mounting them on IC sockets

```
program clock;

var
count : word;
i, j, k, l : integer;
g : file of byte;
displayandsound : array[0..9] of byte;

const
{The display array contains the databyte for each display value}
display : array[0..9] of byte =($3f,$06,$5b,$4f,$66,$6d,$7d,$7,$7f,$6f);
hexff : byte =$ff;       {used for a blank position in the eprom}
hex80 : byte =$80;       {used for a blank display segment with sound output}
hex0 : byte =$0;        {used for a blank display segment without sound output}

begin
  assign (g,'clock.dat');                              {Open the desired filename}
  rewrite (g);
  for i:=0 to 9 do displayandsound[i]:=display[i]+$80;     {Include sound bit}

                                {Calculate a readout in minutes and seconds}
  count:=0;                                              {Reset the displaycount}
  for i:=0 to 2 do                {Maximum count is 29 minutes and 59 seconds}
     for j:=0 to 9 do
        for k:=0 to 5 do
           for l:=0 to 9 do
              if  count mod 30 = 0         {Check if count is a multiple of 30}
              then
              begin {Calculate the four display bytes including the sound bit}
                 write (g,displayandsound[l]);
                 write (g,displayandsound[k]);
                 write (g,displayandsound[j]);
                                                          {Leading-zero blanking}
                 if displayandsound[i]<>displayandsound[0]
                    then write (g,displayandsound[i])
                    else write (g,hex80);
                 count:=count+1;

              end
              else
              begin                              {Calculate the four displaybytes}
                 write (g,display[l]);
                 write (g,display[k]);
                 write (g,display[j]);
                                                       {Leading-zero suppression}
                 if display[i]<>display[0] then write (g,display[i])
                                           else write (g,hex0);
                 count:=count+1;
              end;
                                          {Fill the remaining part with $FF}
  for i:=1800*4 to $1fff do
  begin
     write (g,hexff);
  end;
                                            {Calculate a readout in seconds}
  count:=0;                                          {Reset the display count}
  for i:=0 to 1 do                                {Maximum count is 1999 seconds}
     for j:=0 to 9 do
        for k:=0 to 9 do
           for l:=0 to 9 do
                    {Check if count is a multiple of 90 and smaller than 91}
              if  (count mod 90 = 0) and (count<=90)
              then
              begin {Calculate the four display bytes including the sound bit}
                 write (g,displayandsound[l]);
                 if count < 10 then write (g,hex80)     {Leading-zero blanking}
                               else write (g,displayandsound[k]);
                 if count < 100 then write (g,hex80)    {Leading-zero blanking}
                                else write (g,displayandsound[j]);
                 if count < 1000 then write (g,hex80)   {Leading-zero blanking}
                                 else write (g,displayandsound[i]);
                 count:=count+1;
              end
              else
              begin                              {Calculate the four display bytes}
                 write (g,display[l]);
                 if count < 10 then write (g,hex0)      {Leading-zero blanking}
                               else write (g,display[k]);
                 if count < 100 then write (g,hex0)     {Leading-zero blanking}
                                else write (g,display[j]);
                 if count < 1000 then write (g,hex0)    {Leading-zero blanking}
                                 else write (g,display[i]);
                 count:=count+1;
              end;
                                          {Fill the remaining part with $FF}
  for i:=$2000+2000*4 to $3fff do
  begin
     write (g,hexff);
  end;
  close (g);                                                    {Close the file}
end.
                                                                    894027-13
```

Fig. 5. Listing of the Turbo-Pascal program used to compile the content of the EPROM. The IF COUNT statements allow you to change the timing intervals to individual requirement. Like the EPROM content, the program is divided in two parts: the first provides the data for the minutes and seconds read-out, and the second the data for the seconds read-out (0–1800 s). These blocks may be interchanged. EPROM data is written to file CLOCK.DAT.

(cut off the non-used pins of 14-way low-profile types). Also note that the LEDs in the key caps are best removed and replaced by types with long terminals that can be soldered direct to the PCB. Use a drill or a small file to modify the IC socket if a part of it is in the way of the LED terminals.

The switches are 'Digitast'-like SPDT (single-pole, double-throw) models with an integral LED. With the exception of S_2, they remain locked in both positions. If difficult to obtain locally, the switches may, of course, be replaced by suitable equivalents with the same electrical function, mounted on to the front panel of the enclosure, and connected to the circuit by short wires.

CORRECTIONS

DC-AC converter

July/August 1989, p. 49-51

Only when used in conjunction with the external timebase circuit, the 4047 in the converter supplies an output signal with a duty factor other than 0.5. This causes the primary transformer winding to become saturated, and the dissipation in the power transistors to rise to uncontrollable levels. To prevent this happening, fit wire links 2–3 and 4–5 to keep the 4047 operating in the astable mode. Connect pin 2 of the timebase circuit (100 Hz signal) to pin 3 of the 4047 via a 10 kΩ resistor. Remove R_1 and C_1 from the main converter board.

Attention: none of the above changes applies to the free-running version of the power converter.

Simple AC millivolt meter

January 1990, p. 22-25

In the circuit diagram, Fig. 1, the voltage shown at the base of T_5 is measured with respect to the positive supply rail.

Dark-room clock

February 1990, p. 62-66

The value of R_{17} (1 kΩ) is best increased to 10 kΩ to prevent T_6 overloading the Q13 output of IC_1, which may cause erroneous clocking of IC_1.

In Fig. 4, pin 9 of IC_1 should also be circled to indicate that a through-contact wire must be fitted in the relevant PCB hole.

Vocal eliminator

July/August 1989, supplement p. 5-6

Pins 5 (+input) and pin 6 (–input) of opamp A_2 must be transposed in the circuit diagram.

Voice recorder from Texas Instruments

June 1989, p. 43-45

The supply voltage pin numbers of IC_2, IC_3 and IC_4 are given incorrectly in the circuit diagram in Fig 6.

Pins 18 of IC_2 and IC_3, and pin 4 of IC_4, must be connected to ground. Pins 9 of IC_2 and IC_3, and pin 8 of IC_4, must be connected to +5 V.